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A Hybrid Multi-Path CMOS Magnetic Sensor with 76 ppm/°C Sensitivity Drift and Discrete-Time Ripple Reduction Loops

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Abstract: This paper presents a temperature-insensitive magnetic sensor system for contactless current measurements. To simultaneously achieve wide bandwidth and low noise, the proposed system employs a multi-path structure with a set of spinning current Hall sensors in its low frequency (LF) path and a set of pick-up coils in its high frequency (HF) path. The Hall sensors and pick-up coils are used in a differential sensing arrangement that naturally rejects common-mode magnetic field interference, e.g. due to the earth's magnetic field. A common-mode AC reference field can then be used to continuously stabilize the sensitivity of the Hall sensors, which, unlike that of the pick-up coils, is quite temperature dependent. In this design, the ripple reduction loops in the Hall sensor readout are implemented in a discrete-time manner, and so occupy 20% less area than a previous continuous-time implementation. Over a -45˚C to 105˚C temperature range, the proposed system reduces Hall sensor drift from 22% to 1%, which corresponds to a temperature coefficient of 76 ppm/˚C.

I. Introduction

Magnetic sensors are widely used in many applications for control, protection and diagnostic purposes. In low power applications such as consumer electronics, current sensing is usually done using shunt resistors for high accuracy [1]. However, in high voltage and high power environments such as in industrial and automotive applications, galvanic isolation is required, which complicates the use of shunt-based current sensors. Instead, magnetic sensors can be used to indirectly sense current by sensing the associated magnetic field. This approach also offers more flexibility, allowing systems to be retrofitted without breaking existing current traces [2].

Present industrial trends toward higher efficiency and lower cost have led to the use of compact switched-mode power supplies based on small inductors, which must then be operated at higher frequencies [3]. State-of-the-art switched-mode power supplies typically operate at frequencies well above 1 MHz [4]. In order to measure the currents in such systems, sensors with wide bandwidth, e.g. >1 MHz, are required. Such sensors are also required in overload or short-circuit protection modules [5, 6] to ensure that fault currents are rapidly detected, e.g. within 1 μs, to avoid catastrophic failures.

Hall-Effect sensors (Hall sensors) have found widespread applications due to their excellent linearity, CMOS compatibility and hence, low cost. In the presence of a magnetic field, electrons will experience a Lorentz Force, as shown in Fig. 1. Therefore, positive and negative charges will accumulate at the terminals V_{out+} and V_{out-}, respectively. The force exerted by the resulting electric field counterbalances the Lorentz Force experienced by the electrons and establishes a thermal equilibrium state [7]. The output voltage V_{out} is then proportional to the strength of the input magnetic field and to the current density (I_{bias}/t), where t is the thickness of the sensor. The time required to establish equilibrium is related to the relaxation time of electrons, which is in the order of 10^{-14} s [7]. This indicates that the Hall Effect is a fast physical phenomenon, which can potentially achieve bandwidths of several GHz. In the 60's, in fact, they were widely used for micro-wave measurements [8].

However, in CMOS processes, Hall sensors are commonly realized as n-well plates,

which usually exhibit significant offset, ranging from 10 – 50 mT [9, 10]. This is orders of magnitude greater than many signals of interest, e.g. the earth's magnetic field, which ranges from 25 to 65 μT [11]. The origins of this offset can be understood by regarding a Hall sensor as a Wheatstone bridge, as shown in Fig. 2, which will be unbalanced by the inevitable n-well inhomogeneity. Fortunately, as shown in Fig. 3, this offset can be suppressed with the help of the spinning current technique [12]. By periodically alternating (or spinning) the relative positions of the Hall sensor's biasing and readout terminals, magnetic signals will be up-modulated to f_{spin} and can thus be distinguished from the DC offset. A demodulator can then be used to detect the magnetic signal and simultaneously up-modulate the offset of both the sensor and its readout circuitry into AC ripple. The spinning current technique can be considered to be quite similar to chopping, and confers a similar reduction of 1/*f* noise and drift.

Due to the n-well's anisotropic resistivity, the value of the various resistances in the Wheatstone bridge model will depend on the direction of its biasing current [13]. Furthermore, due to the voltage drop across the n-well, the thickness of the depletion region between it and the p-substrate will not be uniform. As a result, the value of the various resistances in the Wheatstone bridge model will be systematically different, with the resistances connected to ground (Fig. 3) being slightly smaller than the other two [7]. The magnitude of the offset generated in the two phases of the spinning current technique will thus vary, resulting in a net residual offset. To reduce this, the spinning current technique usually consists of 4 phases, which employ all 4 possible biasing directions of the n-well [14]. With this method, residual offsets of about 10 μT can be

achieved [14]. This can be further reduced, to 4 μT, by applying an 8-phase spinning sequence to an octagonal n-well plate [15].

Since a Hall sensor's offset is usually much larger than the desired magnetic signal, the amplitude of the up-modulated spinning ripple is quite large, and must be reduced. Conventional approaches use low-pass filters, which unfortunately also limit the sensor's bandwidth. Increasing the spinning frequency f_{spin} can alleviate this issue, but usually results in a higher residual offset [16] due to the increased frequency of charge injection and switching transients. As a result, the bandwidth of low-offset CMOS Hall sensors is typically rather low (<100 kHz) [16]. In [17], this constraint was addressed by using three orthogonal ripple reduction loops (RRLs) to continuously measure and suppress the spinning ripple *before* amplification. Together with multi-path and multi-sensor techniques [18], an un-trimmed Hall sensor system achieved 40 μT offset and a flat bandwidth of 400 kHz. However, the RRLs in [18] were implemented in a continuous-time manner, and so occupied a relatively large chip area.

Since a Hall sensor is essentially a resistor, its SNR decreases with an increasing bandwidth. In a bid to achieve both wide bandwidth and high resolution, Hall sensors and pick-up coils were combined in a multi-path architecture [19, 20]. As shown in Fig. 4, the crossover frequency f_{cross} defines the frequency beyond which the pick-up coils, due to their superior SNR at high frequencies, should take over from the Hall sensors. As shown in Fig. 5, this is realized with the help of a transimpedence amplifier (TIA), which low-pass filters the Hall signals and integrates the coil signals. The noise

bandwidth of the system is thus limited (to 2 kHz), while the coil extends the sensor's bandwidth (to 3 MHz) with, in principle, no added noise. The crossover frequency f_{cross} is set by the TIA's RC feedback network. As such, a smooth transition between the two paths is guaranteed even in the face of temperature changes and process spread. To achieve a flat bandwidth, the sensitivity of the Hall sensor is matched to that of the pick-up coil by adjusting the Hall sensor's biasing current. However, primarily due to changes in carrier concentration, the sensitivity of a Hall sensor is quite temperature dependent, and will drift more than 20% from -70˚C to 170˚C [7]. This is in contrast to the sensitivity of the voltage-output pick-up coils, which is essentially temperature-independent.

To address this problem, Hall sensor sensitivity can be adjusted using temperature information acquired by an on-chip temperature sensor. With this approach, a sensitivity drift of 30 ppm/˚C has been achieved from -40˚C to 120˚C [21]. However, this method requires accurate characterization of both the Hall and temperature sensors over the entire temperature range, which is time consuming, and thus, costly.

Alternatively, as shown in Fig. 6, the Hall sensor's sensitivity can be continuously monitored with the help of an AC magnetic field reference generated by on-chip coils [22]. The corresponding output signal V_{ref} can then be locked to a constant set-point, which effectively stabilizes the Hall sensor's sensitivity. Without on-chip temperature sensors, a sensitivity drift of 50 ppm/˚C can be achieved [22]. However, the reference signal must be located at a frequency outside the sensor's signal bandwidth, and so this approach is impractical for wide-bandwidth designs.

To avoid a loss of bandwidth, this paper proposes a sensitivity stabilization scheme that uses a common-mode reference field generated by a set of on-chip coils. This approach exploits the fact that the differential sensor arrangement used for current measurements naturally rejects common-mode fields, thus allowing system sensitivity to be continuously monitored without interfering with differential signals. The rest of the paper is organized as follows: details of the proposed system, including the discrete-time RRLs, are described in Section II. Measurement results are shown and discussed in Section III. The paper concludes in Section IV.

II. System Implementation

The proposed system is briefly illustrated in Fig. 7. A set of coils generates a common-mode AC magnetic field which is superimposed on the differential magnetic signal induced by the current flowing through a primary trace on a PCB. Both these fields are picked up by two sets of Hall sensors, and then amplified. Subtracting the amplifiers' output results in a differential channel, whose output is proportional to the differential magnetic field, and in which the contribution of the common-mode field is canceled. Conversely, summing their outputs results in a common-mode channel, whose output is proportional to the common-mode field, and in which the contribution of the differential field is canceled. The output of the common-mode channel V_{ref} can then be used to monitor and stabilize the Hall sensor's sensitivity. The frequency of the common-mode field can now be safely located within the sensor's bandwidth, since it is strongly attenuated in the differential channel.

A. g_m-based Hall sensor readout in a hybrid magnetic sensor system

The block diagram of the overall system is shown in Fig. 8. It inherits the HF path design from our previous work [20]. A transconductance g_{m_coil} converts the outputs of a pick-up coil into currents, which are integrated by the TIA. To preserve the offset performance of the LF path, a coupling capacitor C_{AC} is used to block the offset of g_{m_coil}. A DC servo loop then prevents the output of g_{m_coil} from clipping.

To minimize their initial offset, each Hall sensor in the LF path consists of four orthogonally-coupled Hall plates [23]. The spinning current technique is then used to further reduce this offset. In [19], the Hall sensors were read out by a capacitively-coupled instrumentation amplifier (CCIA), which, however, required a large input capacitor to achieve low noise. In this work, an area-efficient gm-based readout scheme is used, since two readout channels are now required to simultaneously extract the differential and common-mode signals.

As shown in Fig. 8, the differential channel is realized by two g_m stages (g_{m_HS}) that convert the outputs of the two Hall sensors into currents, which are demodulated and subtracted to extract the differential signal. A TIA combines this signal with the output of the HF path. In a similar manner, the common-mode channel is realized by summing the two g_{m_HS} outputs. The combined sensitivity of the Hall sensors and g_{m_HS} can be stabilized by locking this output current to a set point. For flexibility, the temperature control loop is implemented off-chip, and is discussed in more detail in Section III.

To suppress the spinning ripple, two sets of triple RRLs feed offset compensation currents directly into the two Hall sensors. This is in contrast to our previous work [20], in which the RRL's acted on the output of a pre-amplifier. Since their offset is cancelled by the RRLs, the Hall sensors produce relatively small output signals (in the order of 100 μV), which greatly simplifies the design of g_{m_HS}. The residual ripple will then be limited by the mismatch between the three g_{m_HS} stages. To minimize this, they are implemented as a single g_m stage with three output branches, which consume a total current of about 500 μA, as shown in Fig. 9 [24]. Each branch has its own common-mode feedback loop, only one of which is shown in Fig. 9. To match the common-mode level of the Hall sensors' outputs to that of the g_{m_HS} input pair, a resistor R_C is inserted between the Hall sensors and ground, as shown in Fig. 8.

B. Discrete-time triple RRLs

In this design, the outputs of the two Hall sensors are individually processed to simultaneously extract differential and common-mode signals. The continuous-time implementation of the triple RRLs, as in [18, 19], would then occupy considerable chip area, mainly due to the need to realize three independent analog integrators. In this design, the integrators are implemented as up/down counters in an area-efficient discrete-time manner [25].

Fig. 10 shows the output waveform of a typical 4-phase spinning-current Hall sensor. Its output during each of the four spinning phases $V_{1\text{-}4}$ can then be expressed in terms of

the magnetic signal V_{Hall} and three offset components V_{os1}, V_{os2} and V_{os3} as follows:

$$V_1 = V_{Hall} + V_{os1} + V_{os3} \quad (1)$$

$$V_2 = V_{Hall} - V_{os1} + V_{os3} \quad (2)$$

$$V_3 = V_{Hall} + V_{os2} - V_{os3} \quad (3)$$

$$V_4 = V_{Hall} - V_{os2} - V_{os3} \quad (4)$$

Offsets V_{os1} and V_{os2} can be directly extracted by computing $V_1 - V_2$ and $V_3 - V_4$, respectively. Information about V_{os3} is, however, contained in $V_4 - V_1$ and $V_2 - V_3$:

$$V_4 - V_1 = -V_{os1} - V_{os2} - 2V_{os3} \quad (5)$$

$$V_2 - V_3 = -V_{os1} - V_{os2} + 2V_{os3} \quad (6)$$

Equations (5) and (6) indicate that V_{os3} can be extracted from these signals, provided that V_{os1} and V_{os2} become sufficiently small, i.e. after the other RRLs have settled. This means that one of the three offset components can be extracted from the outputs of every two adjacent spinning phases, allowing the reuse of hardware and hence, saving chip area.

The implementation of the RRLs is shown in Fig. 11. The output current of g_{m_HS} during two spinning phases is directly integrated by an auto-zeroed integrator. A comparator senses the polarity of the integrator's output, and increments or decrements the appropriate up/down counter (one for each RRL). The digital outputs of the three counters are then combined and applied to three DACs, which generate the appropriate compensation currents via g_m stages. According to the algorithm shown in Fig. 10, the offset components V_{os1} and V_{os2} are updated once every three spinning cycles. V_{os3} is updated twice every three spinning cycles, and will settle after V_{os1} and V_{os2} become

sufficiently small. From equations (5) and (6) it should be noted that the contribution of V_{os1} and V_{os2} in the V_{os3} error signal appears with alternating polarity, and so V_{os3} will, on average, remain stable until the other two loops settle. At steady state, the residual offset $V_{os1\text{-}3}$ will be limited to ± 1 LSB. The effectiveness of the discrete-time RRLs is similar to that of our previous implementation [18, 19], however, its initial start-up time is somewhat longer, about 360 ms worst-case at an f_{spin} of 41.65 kHz.

Exploiting the auto-zeroing phase of the integrator, a discrete-time comparator is used, as shown in Fig. 12. Thanks to the large gain of the preceding integrator, its offset requirement is quite relaxed. With g_{m_HS} = 1 mS, 10 µs integration time and C_{int} = 20 pF, a comparator offset of 1 mV results in a residual offset of 2 µV at the Hall sensor outputs, which can be achieved with careful layout.

To avoid becoming stuck in local limit cycles, the DACs used in the RRLs need to be monotonic. For area-efficiency and simplicity, the operation of the up/down counters and DACs is emulated by a multiplexed switched-capacitor (SC) integrator, as shown in Fig. 13. In Φ1, a reference voltage V_{ref} is sampled on a sampling capacitor C_s. During Φ2, depending on the comparator outputs, the charge stored on C_s is either added to or subtracted from one of three integration capacitors $C_{os1\text{-}3}$. The opamp in each integrator consists of a folded-cascode OTA and a pair of source followers to drive its common-mode feedback loop, as shown in Fig. 14. In this design, C_s = 150 fF, $C_{os1\text{-}3}$ = 10 pF and V_{ref} = 50 mV result in a step-size of 0.75 mV. With a compensation g_m = 4 µS and R_{Hall} = 1 kΩ, the residual ripple at the input of g_{m_HS} can be reduced to 3 µV. To maximize the

input linear range of the feedback g_m stages, a 250 kΩ resistor is used to degenerate the input differential pair, as shown in Fig. 15.

To avoid voltage spikes due to compensation currents, the spinning Hall sensors are controlled by two groups of clocks phi1-4 and out1-4, as shown in Fig. 16. During spinning phase transitions, clocks out1-4 briefly disconnect the Hall sensors and g_{m_HS}, allowing the biasing current and compensation current to settle. In this design, the dead band in out1-4 is set to 4 ns.

III. Experiment Results

The proposed system was fabricated in a 0.18 μm CMOS process, and the chip photo is shown in Fig. 17. The total area is 2.8 mm × 2.9 mm = 8.12 mm^2. The pick-up coils in the HF path are built with metal traces, with a dimension of 1 mm × 2 mm. To avoid any high frequency cross-talk, the pick-up coils are placed away from the readout circuitry, and shielded by metal plates connected to ground. The common-mode coils for temperature stabilization are placed right on top of the Hall sensors, and have a measured resistance of 220 Ω. The triple RRLs region for the left Hall sensor (highlighted in blue), occupies an area of about 0.5 mm^2, which is about 20% smaller than our previous continuous-time implementation [18, 19].

To verify the performance of the triple RRLs, Fig. 18 shows the FFT of the system's output when the HF path is disabled. With f_{spin} = 41.65 kHz and zero magnetic field, the

RRLs can reduce the spinning ripple from over 1 mT down to 21 μT at 83.3 kHz ($2f_{spin}$). This residual ripple is limited by the mismatch between the current mirrors in the g_{m_HS} stage. At f_{spin} = 41.65 kHz, the residual ripple is reduced to 2.9 μT, which is solely limited by the step size of the switched capacitor integrator in the RRLs. The residual ripple can be further reduced by increasing f_{spin}, at the expense of greater residual offset [17]. The sub-harmonics in the FFT plot are due to the fact that the modified RRL scheme is multiplexed between three ripple components, and it therefore under-samples the spinning ripple.

The lead-frame pads of traditional packages, as shown in Fig. 19 (a), are known to generate eddy currents in response to high-frequency magnetic fields, which, in turn, distort the sensor's high frequency response [20]. To avoid this, a chip-on-board (COB) technique is used to mount the die directly on top of a PCB trace, with the added benefit of reducing the actual distance between the sensors and the primary current and their accurate alignment, as shown in Fig. 19 (b). This results in a current-to-magnetic transfer function of about 0.43 mT/A. After trimming at 30˚C, each Hall sensor is biased by a 2 mA (0.5 mA/plate) current, resulting in a sensitivity of about 71.4 mV/T. With both LF and HF paths active, the system achieves a flat frequency response with a bandwidth of 3 MHz, as shown in Fig. 20.

To accurately evaluate the proposed sensitivity stabilization scheme, a temperature independent common-mode magnetic field reference is generated by feeding a square wave current with a constant amplitude into the on-chip common-mode coils. This is

realized by placing the coils in the feedback of an off-chip inverting amplifier, which is driven by an 80 Hz clock through an off-chip resistor, as shown in Fig. 21. In this design, the increase in coil resistance with temperature limits the amplitude of the square wave current to ±10 mA.

In principle, a reference current can be generated on-chip by combining a bandgap reference with the thin-film resistors available in the chosen process. With an accurate bandgap reference, e.g. [26], the effectiveness of the temperature stabilization will be preserved, as demonstrated by the negligible difference between the off-chip [21] and on-chip [27] realizations of a previous sensitivity stabilization scheme.

The output currents of the common-mode channel are synchronously demodulated, and read out by an off-chip TIA, whose averaged output voltages V_{out} are compared to a set-point by a comparator. The comparison results then increment or decrement a DAC by 1 LSB, which adjusts the Hall sensors' biasing current by 5 μA.

Fig. 22 shows the measured system frequency response to 3 A_{rms} currents at an ambient temperature of 105˚C from 100 Hz to 12 kHz (f_{cross} = 2 kHz). For these measurements, the temperature of the die was estimated to be about 150˚C, mainly due to the heat dissipated in the relatively narrow (1 mm) PCB trace. Without the temperature stabilization scheme, a 2 dB gain mismatch can be observed across the frequency range. When activating the proposed stabilization scheme, this gain mismatch can be fully corrected. Up till 12 kHz, no gain mismatches can be observed

between the HF and the stabilized LF paths.

The gain drift of the system is quantitatively characterized in an oven from -45˚C to 105˚C. Driven by a spectrum analyzer, a primary current is generated outside the oven. The system outputs are directly analyzed by the same spectrum analyzer to extract the gains at the excitation frequencies. The measurement results are summarized in Fig. 23. Without sensitivity stabilization, the LF path gain at 800 Hz drifts as high as 22%, which is caused by the sensitivity drifts of both the Hall sensors and g_{m_HS}. With the proposed sensitivity stabilization scheme, the gain drift can be reduced to 1%, corresponding to a maximum temperature coefficient of 76 ppm/˚C, which is comparable to the state-of-the-art [21, 22].

Similarly, the sensitivity of the HF path is characterized at 86.22 kHz. The HF path gain drifts from -10% to 7%, which was not observed in measurements up to 12 kHz (Fig. 22). This is because at high frequencies, the skin effect causes current crowding at the surface of the conductor. This, in turn, increases the trace's impedance and its temperature, thus reducing the amplitude of the primary current flowing through the shunt resistors. In addition, the high frequency magnetic field will interact with its surrounding components. The permeability of some of these will be temperature-dependent, therefore influencing the current-to-magnetic field transfer of the primary current. Together with the non-linearity of gm_coil due to the large coil voltage swing, this may result in additional sensitivity drift. Nevertheless, the sensitivity of the HF path is comparable to the performance of other coil-based magnetic sensors [28].

Table I summarizes the performance of this design in comparison to other state-of-the-art CMOS low-drift magnetic sensors. Compared to low drift Hall sensors with other temperature stabilization schemes, the proposed scheme achieves comparable gain accuracy as [21] and [22], while the bandwidth is at least 6× higher. Compared to other coil-based magnetic sensors like [28], the proposed system can cover the full bandwidth including DC while achieving similar gain accuracy.

IV. Conclusions

This paper presents a hybrid magnetic sensor built of Hall sensors and pick-up coils with its Hall sensor gain drift continuously stabilized. The proposed sensitivity stabilization scheme exploits the common-mode rejection of differential current sensing systems by injecting an AC common-mode magnetic field reference, through which the system sensitivity can be actively monitored and hence, stabilized. With this approach, the overall Hall sensitivity drift can be reduced from 22% to 1% in the temperature range from -45˚C to 105˚C. This is equivalent to a temperature coefficient of 76 ppm/˚C. Furthermore, the triple RRLs for spinning current Hall sensors are implemented in a discrete-time manner, which occupies 20% less chip area compared to the previous continuous-time implementation. By combining the sensitivity stabilized Hall sensors and the temperature-independent pick-up coil the overall system achieves a flat bandwidth from DC to 3 MHz.

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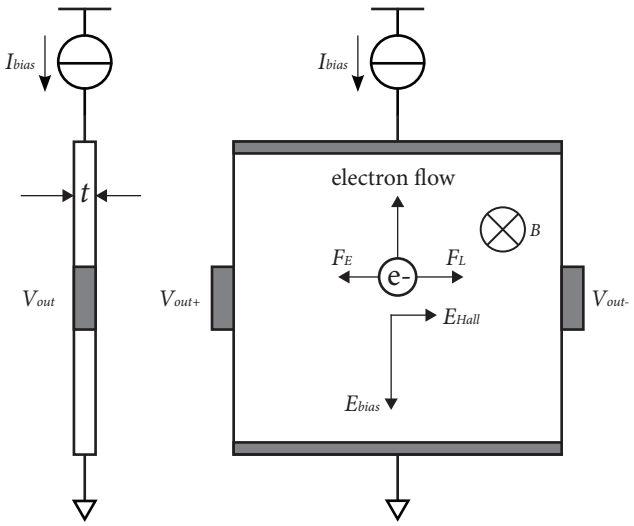

Fig.1 Side (left) and top (right) views of a Hall Effect sensor

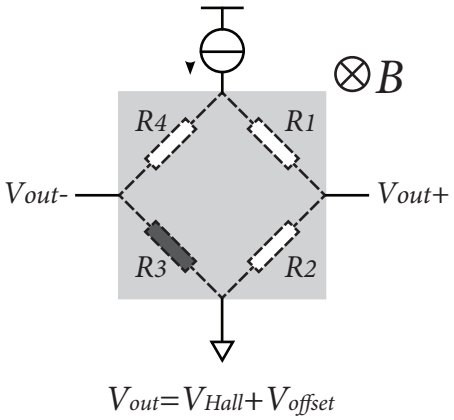

Fig.2 The Wheatstone bridge model of Hall sensors.

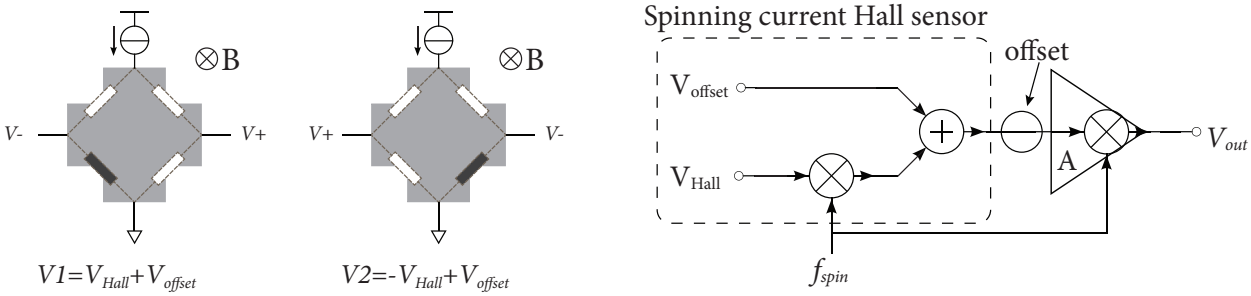

Fig.3 Spinning current Hall sensors (left) and its readout (right).

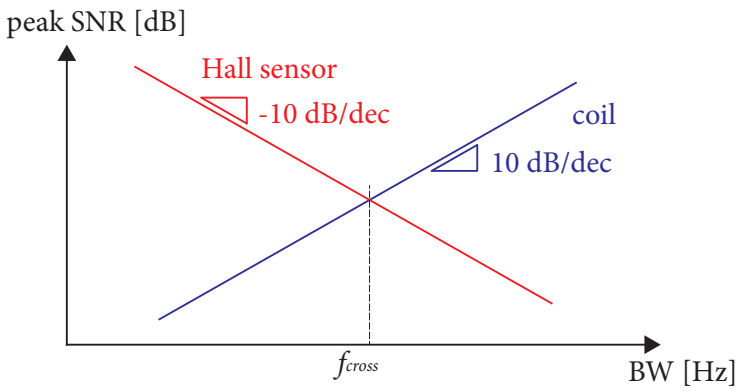

Fig. 4 Peak SNR plots of Hall sensors and coils

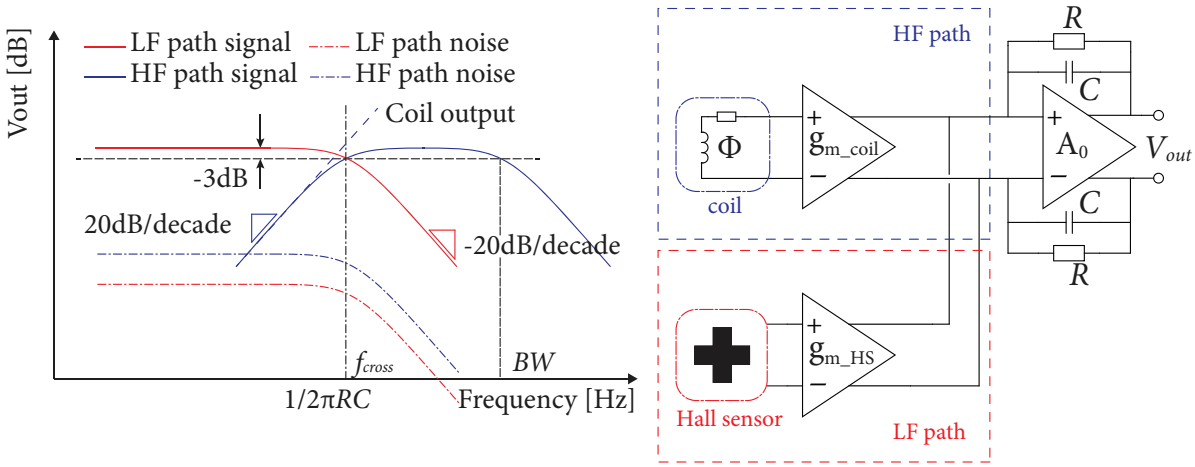

Fig. 5 The combination of Hall sensors and pick-up coils

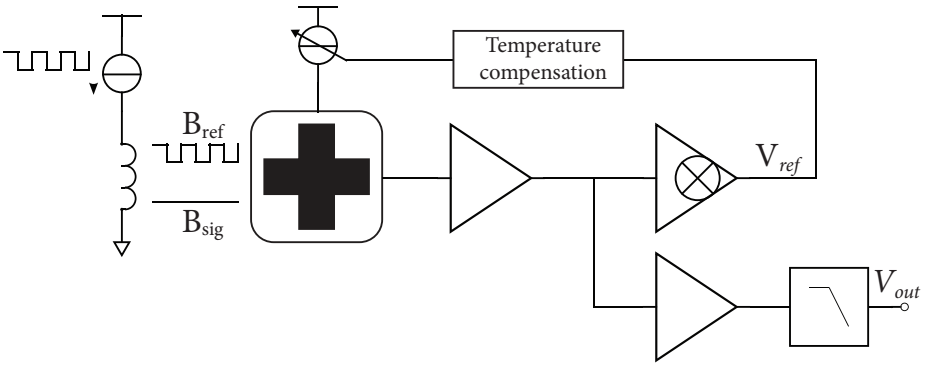

Fig. 6 Closed-loop temperature control using on-chip coils.

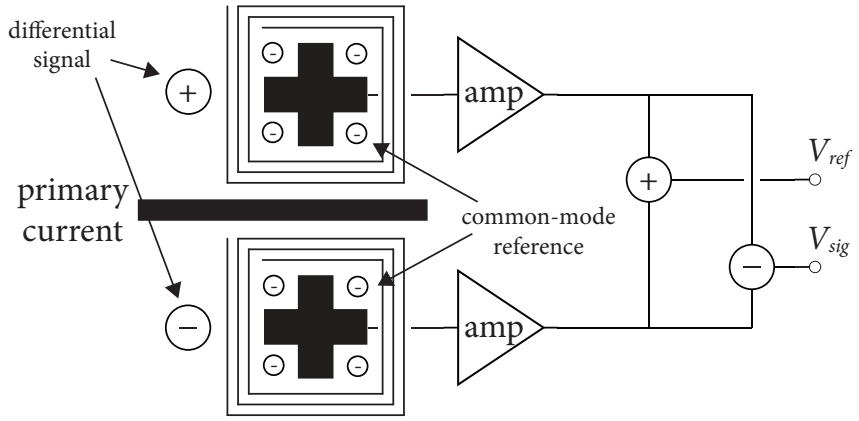

Fig. 7 Sensitivity extraction via an on-chip common-mode AC reference field.

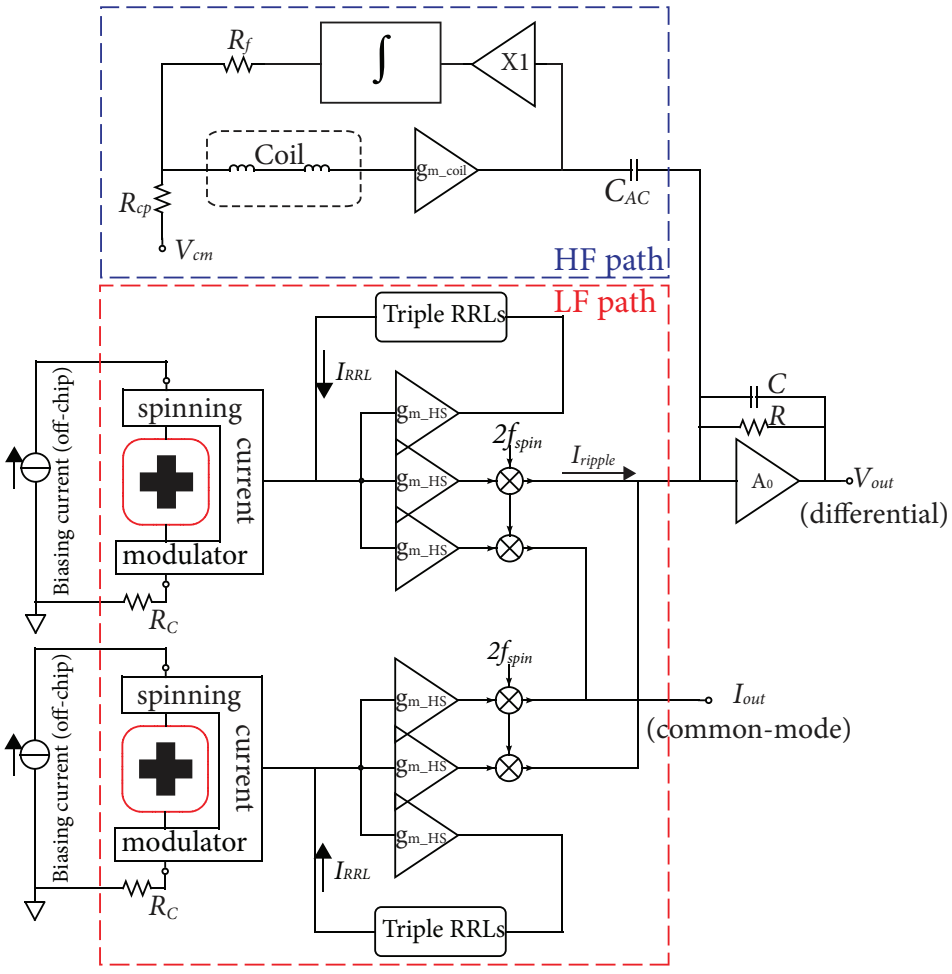

Fig. 8 Block diagram of the complete system.

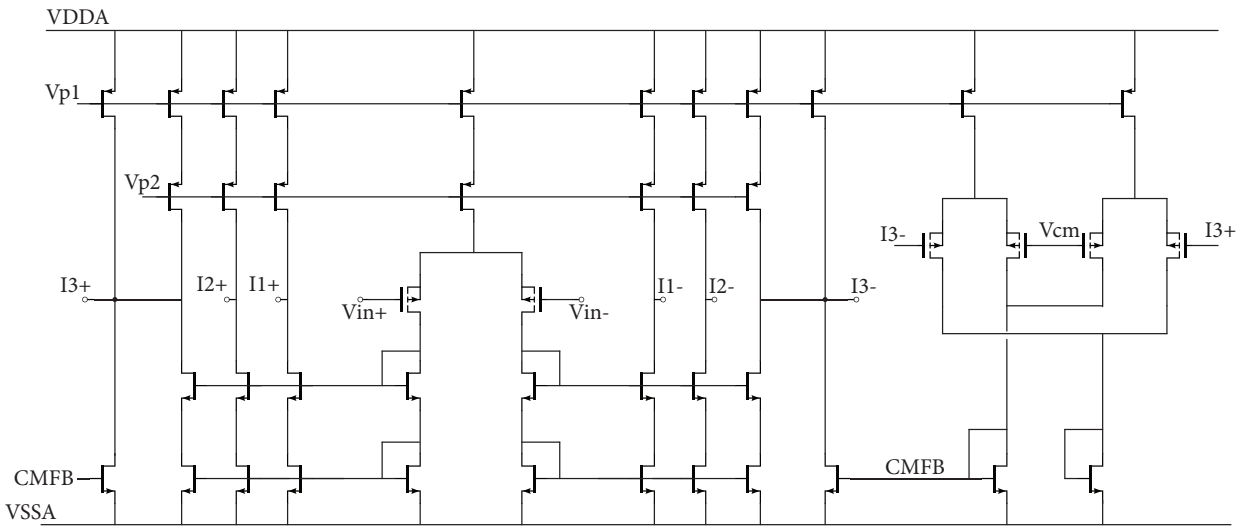

Fig. 9 Circuit diagram of g_{m_HS}.

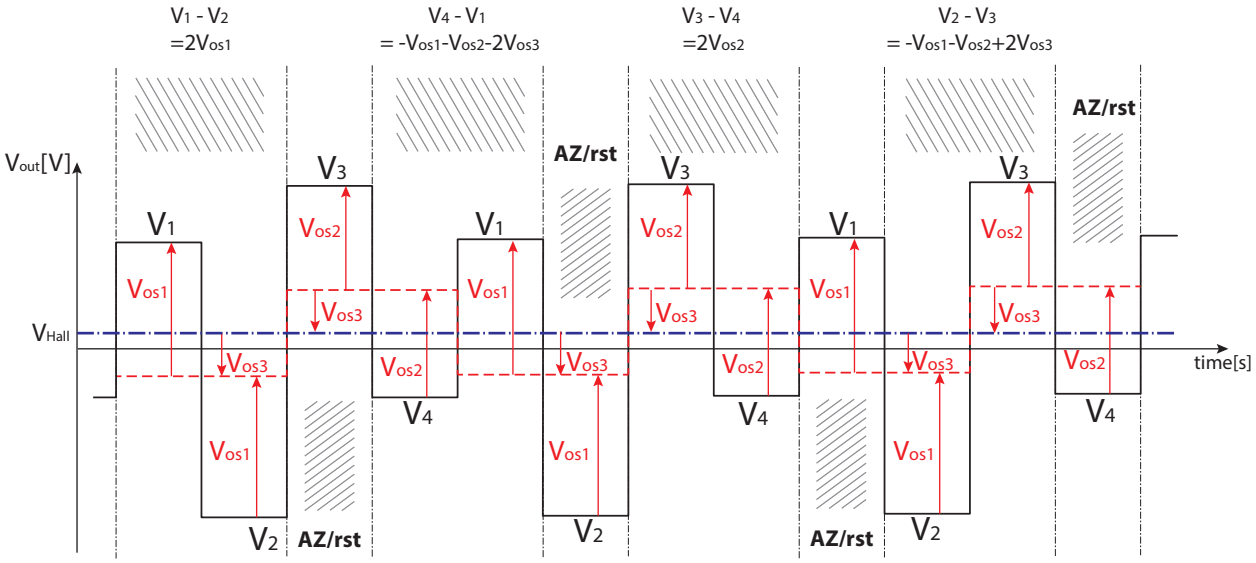

Fig. 10 Illustration of triple RRL scheme.

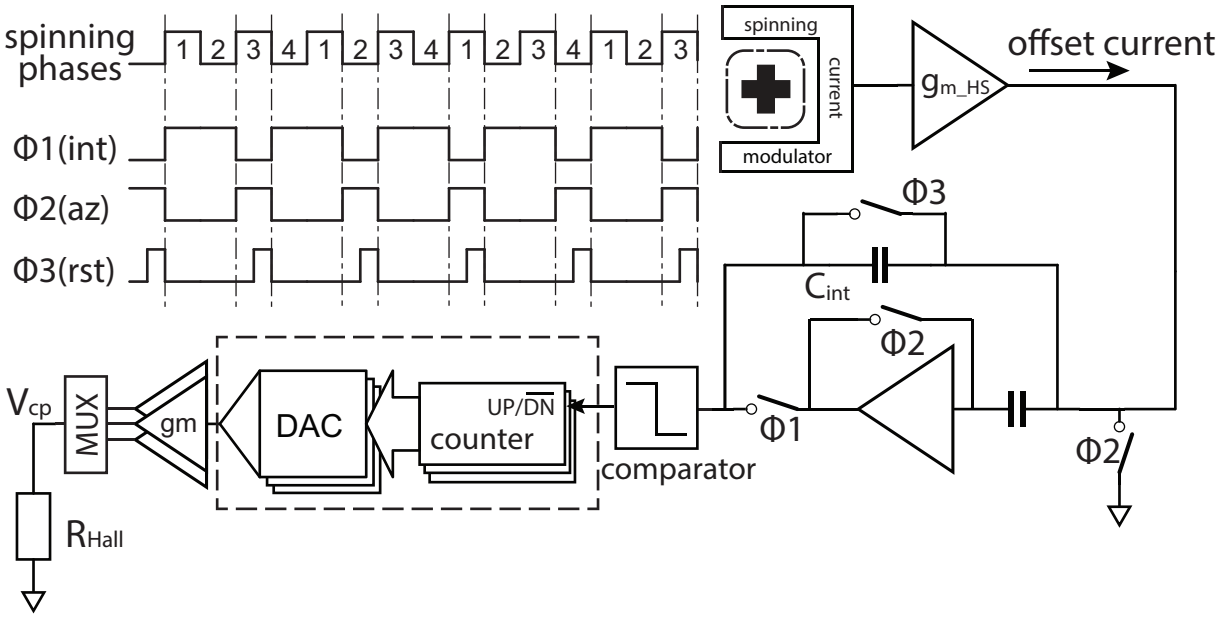

Fig. 11 Discrete-time implementation of the triple RRLs.

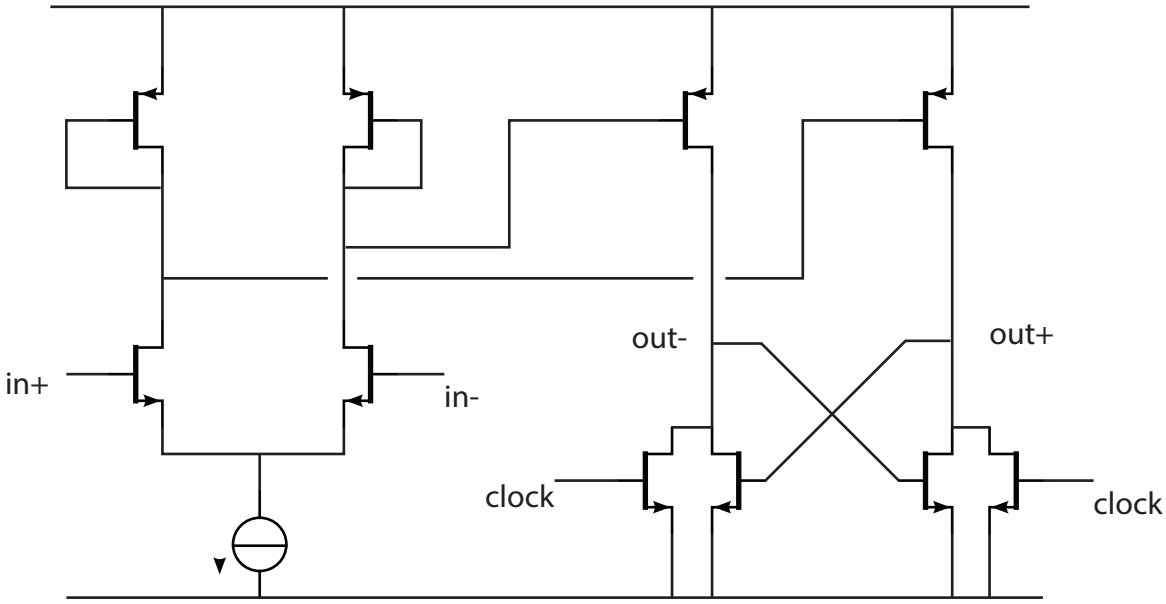

Fig. 12 Circuit diagram of the comparator.

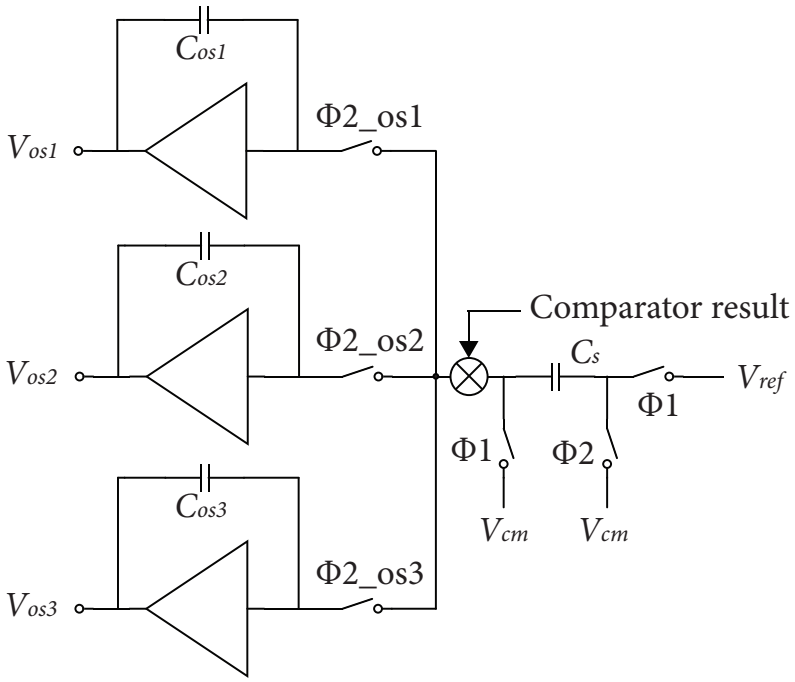

Fig. 13 switched-capacitor (SC) integrator implementation of up/down counters and DACs.

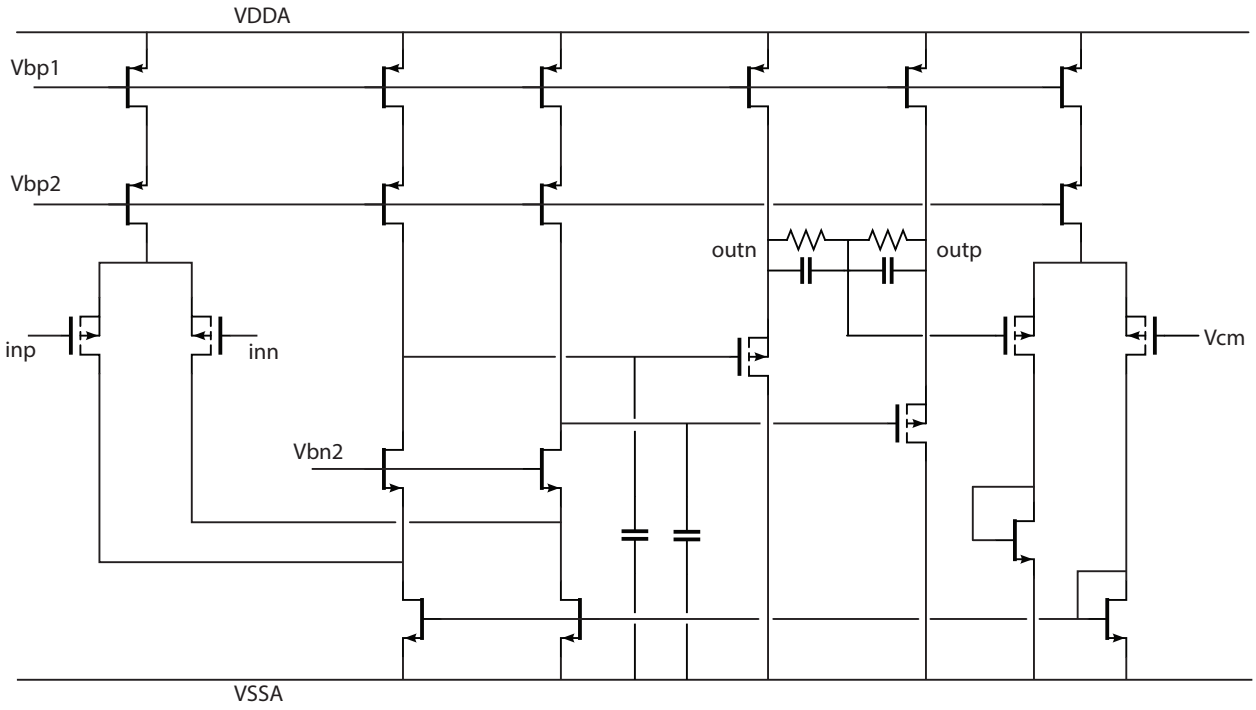

Fig. 14 Circuit diagram of the opamp used in the switch-cap integrators.

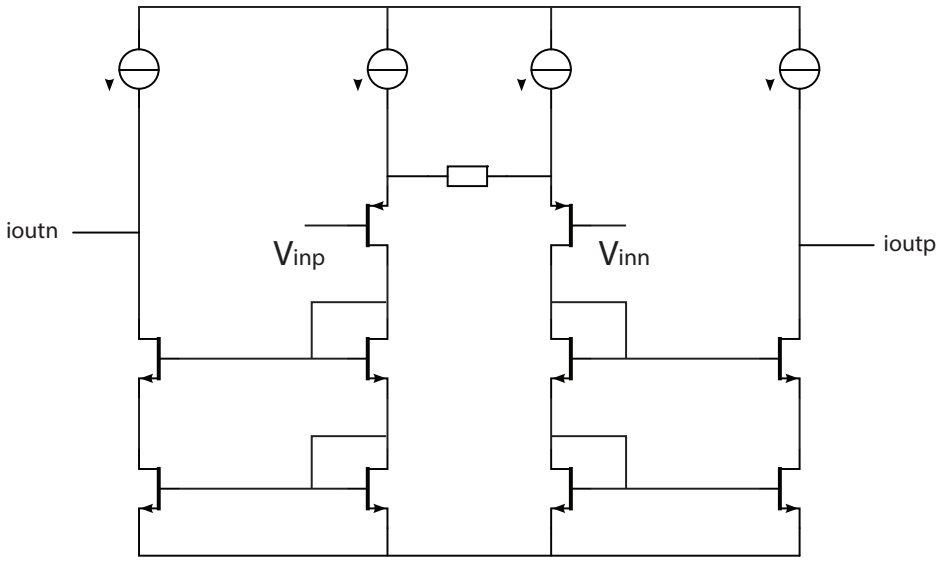

Fig. 15 Circuit diagram of the feedback g_m stage in RRLs.

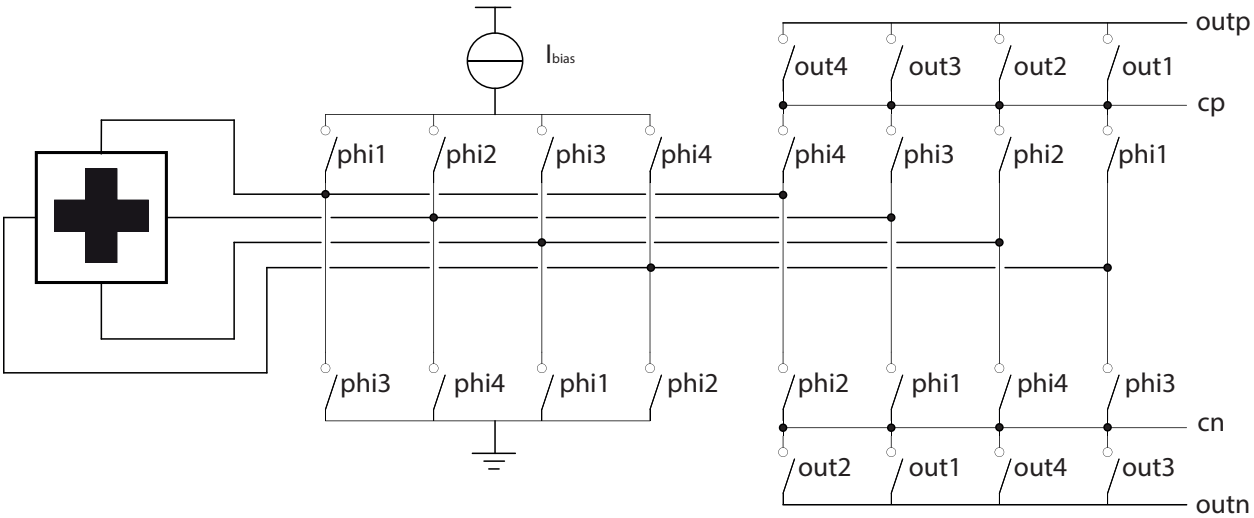

Fig. 16 Circuit diagram of the spinning current switches.

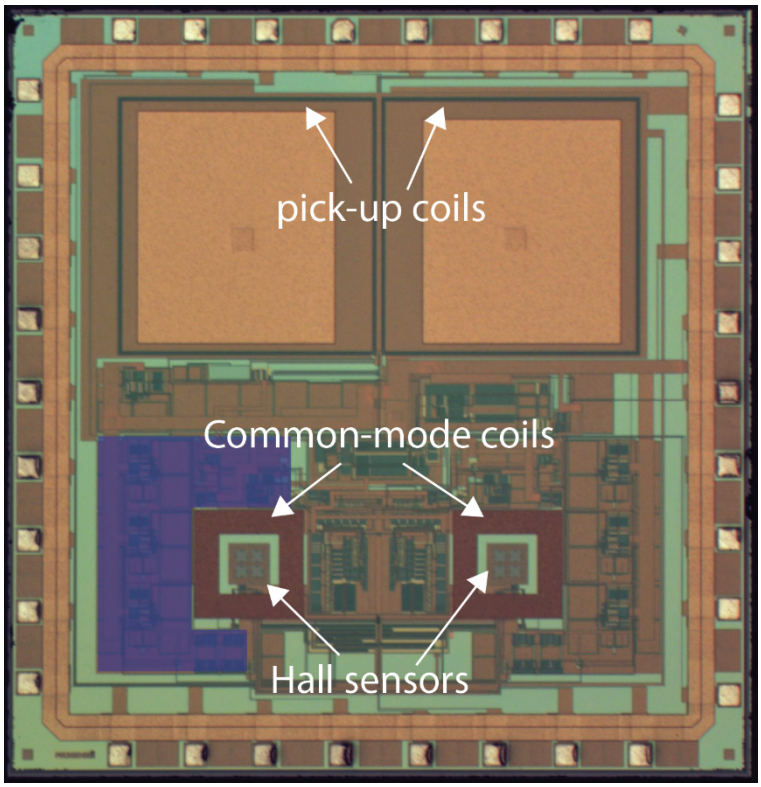

Fig. 17 Micro-chip photo of the proposed system

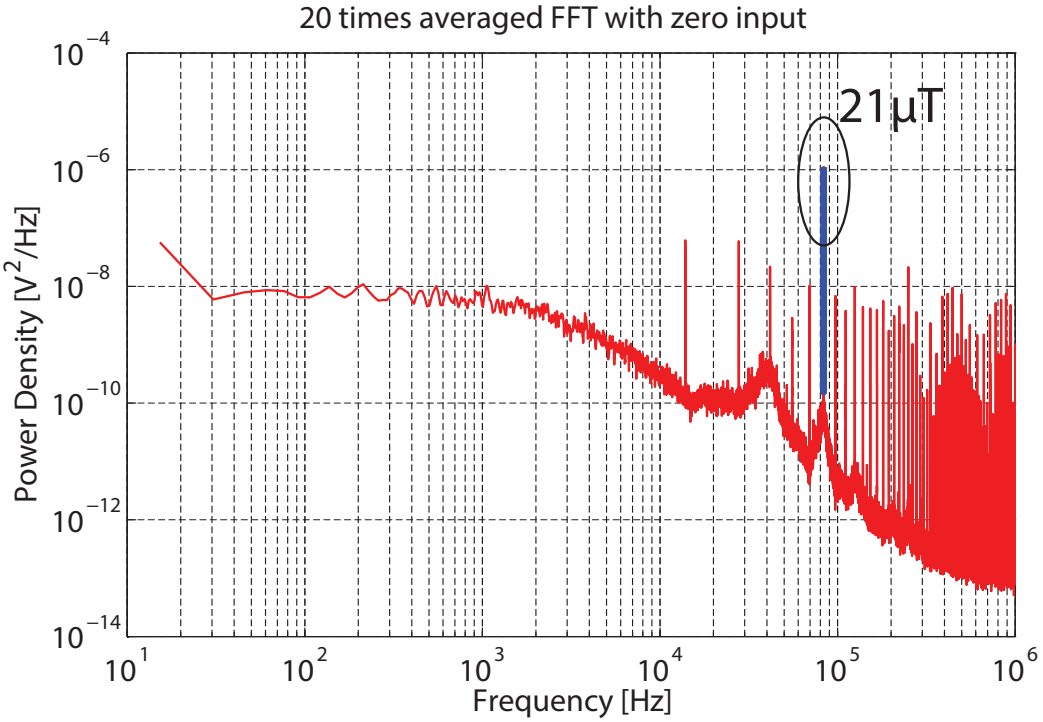

Fig. 18 FFT plot of system output with the HF path disabled and zero magnetic field.

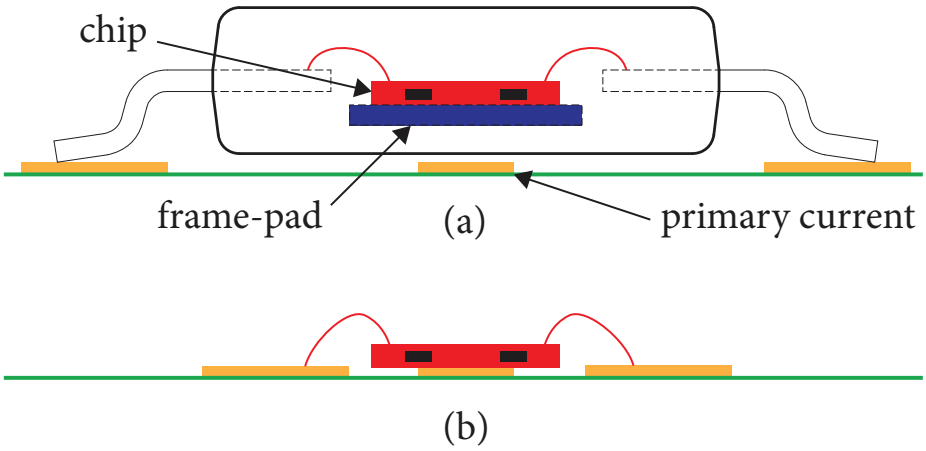

Fig. 19 Cross-section of (a) traditional package and (b) chip-on-board (COB)

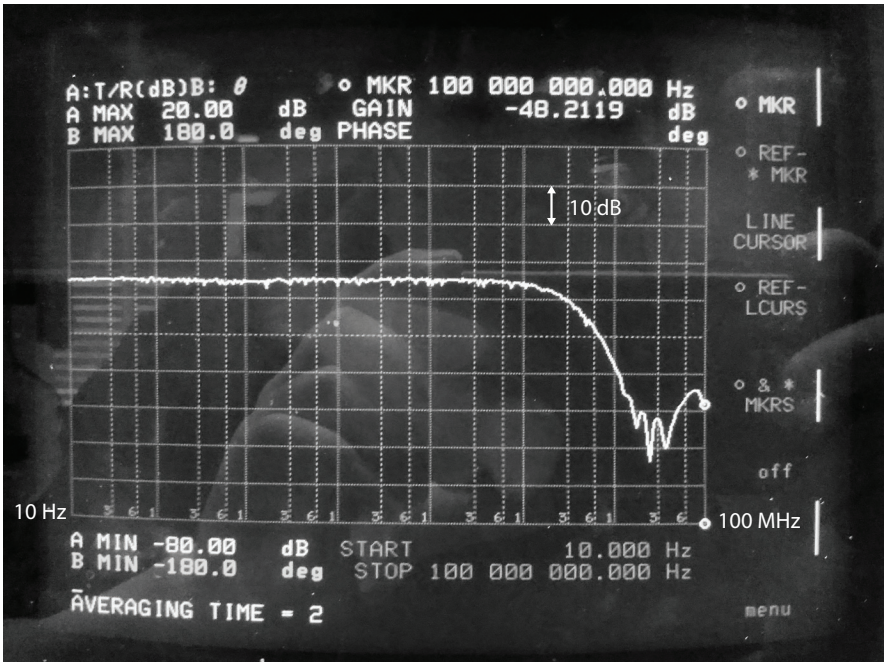

Fig. 20 Measured frequency response.

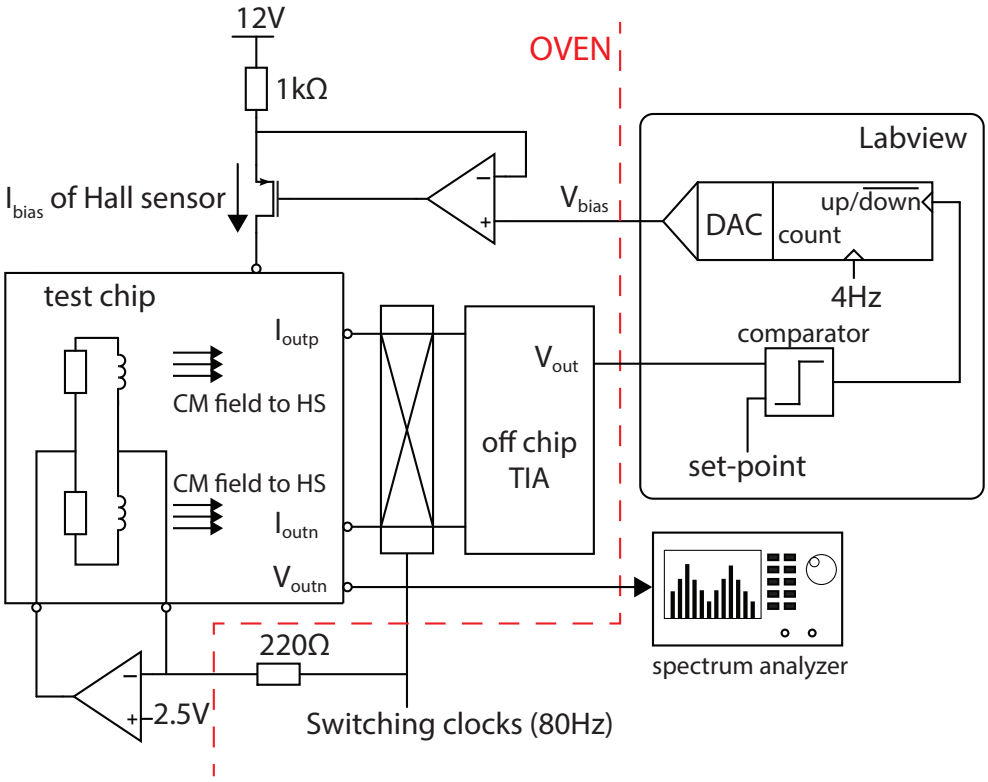

Fig. 21 Temperature stabilization test setup.

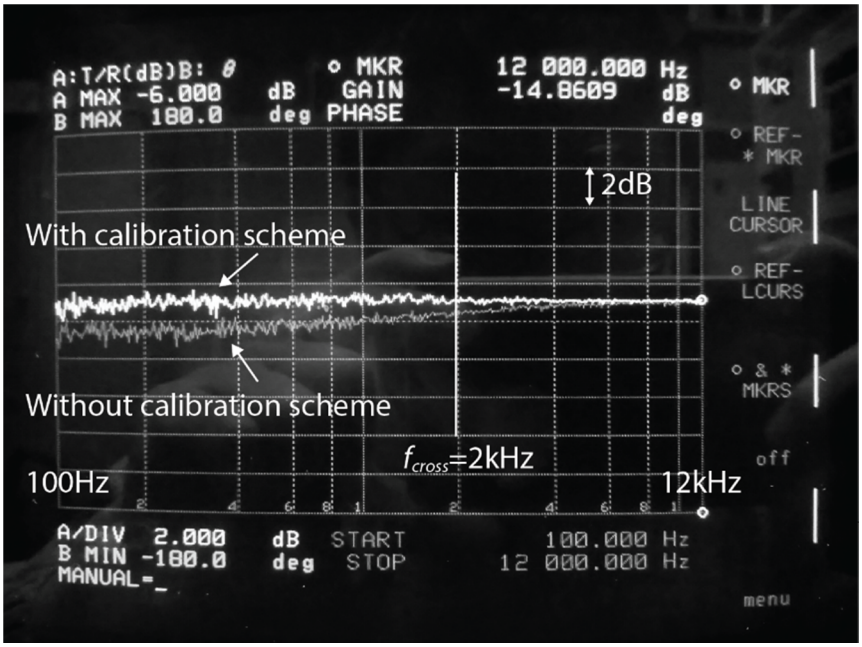

Fig. 22 Measured frequency response from 100 Hz to 12 kHz at 105˚C.

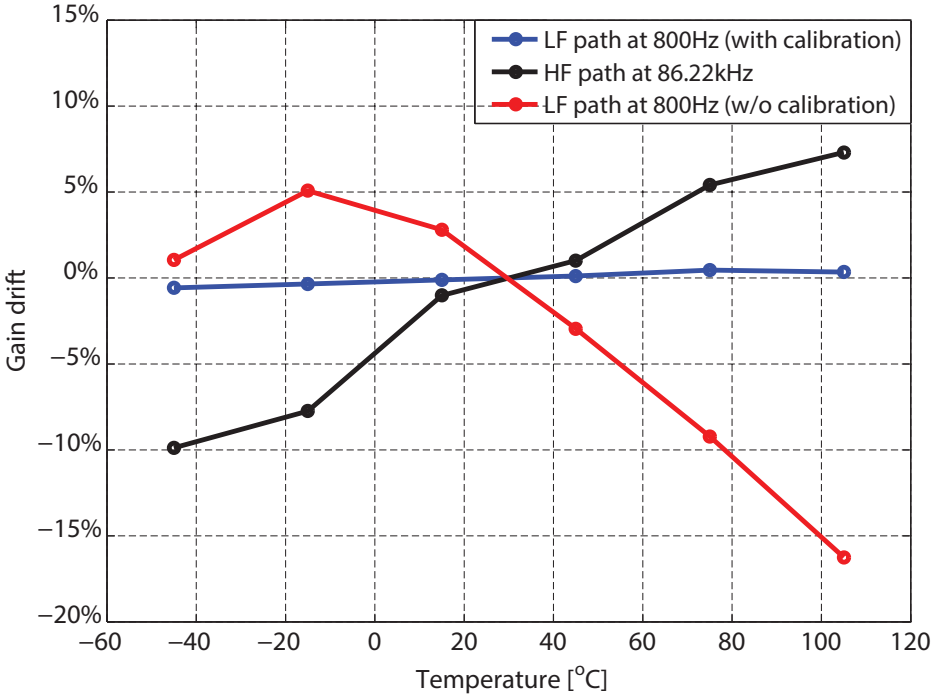

Fig. 23 Measured gain drift from -45˚C to 105˚C.

Source	This work		[20]	[21]	[25]
Technology	0.18 µm		0.35 µm	0.8 µm	N/A
Power supply	5 V		5 V	5 V	2.7 – 5.5 V
Supply curreent	9.2 mA*		12 mA	N/A	7 mA
Temperature compensation	Closed loop		Open loop	Closed loop	N/A
Sensitivity drift [ppm/˚C]	76 (LF)	1100 (HF)	30	50	800**
Area [mm^2]	8.12		3.5	11.5	N/A
Input range	± 7.8 mT		± 400-2.2 mT	± 50 mT	N/A
Bandwidth	3 MHz		125 kHz***	500 kHz****	50 kHz–1 MHz
Offset	80 µT		N/A	N/A	N/A

* Off-chip components not included
** >20% full scale input
*** Calculated based on spinning frequency
**** Theoretical value

Table I. Comparison table.