Electrical characterisation of matched pairs for evaluation of integrated circuit technologies

Electrical characterisation of matched pairs for evaluation of integrated circuit technologies

Proefschrift

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Chapter 1

An introduction to parametric mismatch fluctuations

1.1 What's in a name?

what's in a name? that which we call a rose
by any other name would smell as sweet

William Shakespeare
Romeo and Juliet
(act II, sc. II)

'matching and mismatch'

This thesis is dedicated to improving electrical measurement methods and characterisation techniques for understanding and evaluation of parametric mismatch fluctuations of integrated circuit components. The obtained knowledge helped to improve IC technologies and lead to better electronic circuit performances and higher product yields.

Integrated circuits are the electronic engines that drive and control practically all electronic equipment and information exchange in our society. An integrated circuit (IC) is often called silicon chip or die (plural dice or dies) or silicon crystal. An IC consists of many electronic components or elements (transistors, resistors and capacitors) that are manufactured simultaneously on a single piece of silicon. Integrated circuit components are often called devices.

Electronic design of IC's is based on thorough understanding of electronic circuit principles, mathematics, semiconductor device models and computer-aided-design (CAD) tools.
An IC is generally assembled from smaller electronic building blocks (sub-circuits), each built from a handful to several hundreds of devices. Examples of such building blocks range from elementary digital logic cells like inverters, memory cells and flip-flops, to analogue circuits like (operational) amplifiers, filters and data converters. A single integrated circuit, such as a personal computer chip, can contain up to tens of millions of devices. A complete IC performs electrical signal conditioning (amplification, filtering, conversion), data retrieval (memories), and mathematical operations.

Manufacturing of integrated circuits is done in dust-free fabrication facilities (fabs, clean rooms), where silicon wafers are converted to electronic components and IC's through

a complex succession of photo-lithographical steps and physical and chemical treatments. IC manufacturing equipment and processing methods are prone to changes and variations over time and place (e.g. varying process temperatures and chemical concentrations). This implies that the electrical behaviour of IC components also shows substantial variations or spreads. These spreads, specified as acceptance limits, often span tens of percents. One of the main challenges of (integrated) electronic circuit design is to cope with such spreads. The produced IC must meet the product performance specifications (speed / gain / bandwidth / accuracy), irrespectively of the actual electrical performance of the devices with which it is built (within the acceptance limits).

IC devices that are placed close together within one circuit block show much better equality than the spreads given by the overall process spread specifications. This is because such devices are -by definition- manufactured at the same time, with the same equipment and processing conditions. Such components are called matched components. Two closely spaced identical IC devices that are part of one particular circuit (function) are called a matched pair.

Many analogue electronic building blocks are based on, or benefit in terms of performance from, the availability of supposedly identical (matched) IC components. Figure 1.2 shows an example of part of an integrated circuit with several identical transistors and resistors.

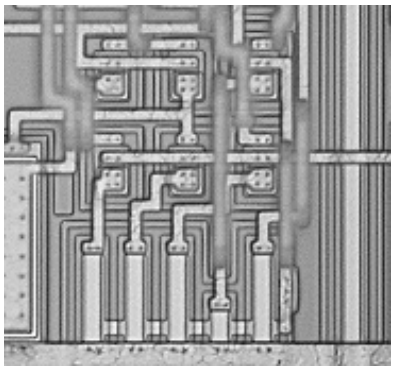

Figure 1.2 Microscopic photograph of part of an integrated circuit block with several adjacent identical transistors and resistors.

Despite the inherent processing similarity for closely spaced devices, small electrical performance differences can always be observed. Such differences are called mismatch (or offset). When a large group (population) of matched pairs is measured, the mismatch varies from pair to pair. More specific, it is generally observed that mismatch demonstrates time independent random fluctuations. These statistical fluctuations are generally attributable to random microscopic device architecture fluctuations, such as statistical variations in the number of dopant atoms, built-in electrical charges or edge roughness. The overall (statistical) mismatch variation that circuit designers must take into account for meeting the required performance of an analogue circuit block is generally indicated with the term matching.

Mismatch is either specified for measurable device quantities, such as the current for a specific bias condition, or for parameters associated with specific device models, such as the threshold voltage of a MOSFET. Matching, or more precise parametric mismatch fluctuations (PMF), can be quantified through measuring the parametric mismatches of a population of closely spaced matched pairs, for instance through measuring a particular matched pair that is placed on all dice of a silicon test wafer (figure 1.3).

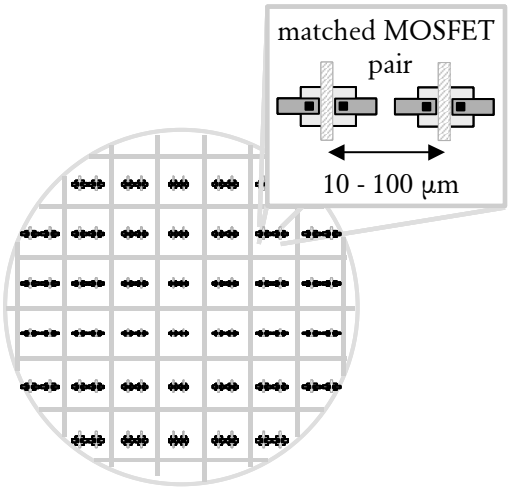

Figure 1.3 The matched pairs on the different chips of a wafer form a population. Variations from chip to chip are much larger than variations from transistor to transistor within a pair.

The statistical estimator associated with a population of mismatch observations ΔP/P of parameter P is identified with $\sigma_{\Delta P/P}$, representing the parametric mismatch fluctuations standard deviation (figure 1.4).

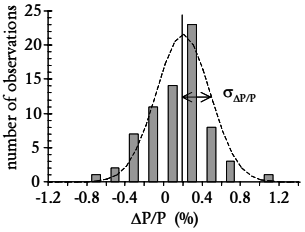

Figure 1.4 Example of a histogram of mismatch observations. $\sigma_{\Delta P/P}$ represents the parametric mismatch fluctuations standard deviation.

When analysing the statistical properties of parametric mismatch fluctuations, it is not uncommon that besides a random component of the mismatch (fluctuations), the average or the median $\mu_{\Delta P/P}$ of mismatch observations of a population of matched pairs deviates significantly from zero (figure 1.5). In such cases, the term systematic mismatch is used. Many electronic circuit designers prefer the term offset. Systematic mismatch is generally attributed to undesired deterministic (hence not random) device construction asymmetries, associated with photo-mask artefacts, layout design errors, or asymmetries in the surroundings of the matched components, which are common for the entire population of pairs.

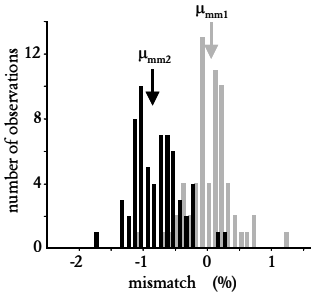

Figure 1.5 Example of systematic parametric due to asymmetric layout surroundings. The median of population 2 (black columns) is about 1% smaller than median_1 (grey columns).

Figure 1.6 depicts a typical example of a matched pair test structure that is used to measure mismatch. The purpose of such test structures is to measure the mismatch with electrical measurement systems, quantify the statistical parametric mismatch fluctuations, assess the magnitude of the fluctuations, and identify the physical causes.

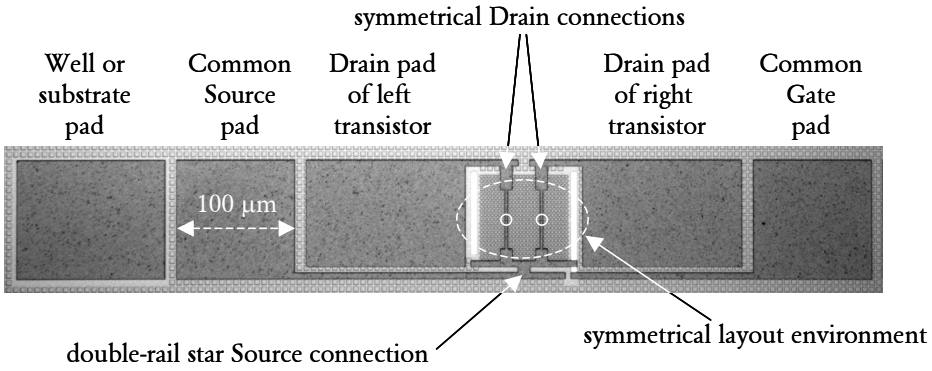

Figure 1.6 Microscopic photograph of a matched pair test structure with carefully designed contact pads and connections to the transistors. Magnification≈ 160 X. The two MOSFET's (W/L=2 µm/1µm) are found inside the white circles. The transistors are placed in a field of identical transistors and accessed through a symmetrical metal connection frame that assure optimum identicalness of the access resistances and local mechanical stress.

The noun 'match' is considered to trace back to the old English gemæcca, standing for 'mate' or 'equal to another' [m-w 'match']. The modern English descriptions for ‘match’ include 'a person or thing equal or similar to another' [m-w 'match']. According to this definition, the term 'matched pair' is an appropriate description for a pair of devices that the electronic circuit designer expects to be identical. The term matching is used far more extensively than in the meaning as treated in this thesis. In fact, the terms matching and mismatch are encountered abundantly in science, as well as in many parts of the human culture and society. In science, or more in particular in engineering, the term matching generally refers to the degree of equality of a particular material property or characteristic quantity, at the interface between two (not necessarily identical) parts of a system. In the fields of mathematics, computer sciences, biology, astronomy and linguistics the term matching is also encountered frequently.

The perfect match also is of paramount interest in many other aspects of our human society. In most persons' lives, the search for a suitable partner and/or the perfect place to live and work in required considerable attention and energy. One could wonder whether the socio-cultural interpretation of a perfect match is not contradictory to the definition that is commonly used in engineering. Whereas in the latter the perfect match refers to equality, in the human society the perfect match is often more about differences, or rather complementariness, than about equality. Sure enough, a substantial degree of consensus on the main issues of life forms an indispensable element of a good match, but it is in fact the complementary qualities of people that determine the real and lasting value of the perfect match. On top of that, it cannot be denied that the differences (the mismatches) between allegedly good matches make life challenging and interesting. In the context of this thesis, one then arrives at a remarkable similarity. Matching studies for integrated circuit components are aimed at achieving the perfect match in the sense that observed parameter differences of the devices should be as small as possible. Nevertheless, the biggest satisfaction about research in this field no doubt is obtained when the differences are unexpectedly large! It cannot be denied that the professional joy of a mismatch characterisation specialist is based quite often on the misery of his esteemed colleagues, the process technologists and circuit designers (speaking about a mismatch…).
Uniting the right research subject and person for the study underlying this thesis undeniably resulted in a perfect match. The research work on which this thesis was based is best described as an omnivorous banquet, feasting on practically anything that appeared to have some relation with parametric mismatch, and statistical semiconductor device parameter fluctuations.
The menu selection perfectly matched the author's appetite (as well as the chef's choice) for silicon device measurement and characterisation techniques. It cannot be denied that over 25 years of experience in this field contributed to the choice of the cuisine. Moreover, the yearning to comprehend the fundamental details and limitations of IC technologies, and the thrill to be able to derive what is right or wrong about a particular IC technology, based on DC parametric measurements, found a fruitful match in this research project. This association with a festive banquet leads to one of the other definitions of the word 'match', namely ‘mate’. In old English, the word gemæcca, is considered to be related to another word for 'mate' namely gemetta. The latter is used in the sense of 'guest at one's table' [m-w 'mate']. The reader of this thesis is sincerely invited to join this banquet and share some of the hopefully enjoyable courses in this search for better IC processes.

The five chapters of this thesis follow the menu of a conventional gourmet dinner.
Chapter 1 provides the appetizers, such as definitions and a historical literature overview, and lays the foundation for the coming courses through an overview of the author's published work on mismatch characterisation. Chapter 2 symbolises the starter, namely the matched pair test structure. The starting point of every successful electrical characterisation experiment is a well-designed test structure. For mismatch characterisation, this is even more important as one is generally interested in quite subtle parametric effects. The first main course is the fish. Indeed, chapter 3 is a lot about fishing. The choice of a good measurement system and construction of dedicated measurement and data analysis algorithms are required to be able to catch the subtleties of small statistical parametric mismatch fluctuations. The meat is served in chapter 4, based on some examples of parametric mismatch fluctuation studies that proved instrumental for gaining valuable insights in IC process architecture fluctuations. Coffee, pastry, liquors (and cigars for some) are left for chapter 5, summarising the conclusions of the work of this thesis. Of course this also is the moment of the dinner to speculate about future developments and to thank all those who contributed in word, deed and thought to this work.
As with any good meal, the underlying idea of this thesis is that a good balance must be achieved between the dishes. Only if the test structures are correct, the measurements accurate enough, the statistical analysis sound, and the technological / physical interpretation confirmed, the meal is complete and satisfying.

The lasting justification for the work underlying this thesis is that the accumulated results have proven multiple times that studying the statistical properties of parametric mismatch for populations of matched pairs reveals valuable knowledge about the microscopic device architecture of IC-components. These insights are used to improve IC technologies, leading to better electronic circuit performances and higher product yields. As such, the work as described in this thesis forms a new direction in the field of parametric process characterisation.

1.2 What's in the history?

For small signal analogue electronic circuit design, differences between supposedly identical circuit elements have always been treated as stochastic events. Historically, this might be traced back to the 'pick and match' techniques that were applied when an electronic circuit was assembled from discrete components, selected (and matched) from a (pre-tested) stock of discrete transistors or resistors. With the introduction of integrated circuits, the nature of mismatch of electronic circuit components changed in two ways. In the first place, the circuit designer (or manufacturer) did no longer have the possibility to 'hand-pick' (pre-test) the supposedly identical components, as they were manufactured together on the same semiconductor crystal. However, as the circuit designer has no control over process spreads and fluctuations, the resulting electrical mismatches henceforward had a random appearance from the user's standpoint. This meant that for integrated circuit performance tolerance calculations the statistical properties of the mismatch between matched components became an intrinsic process performance parameter. On the other hand, the advantage of realising a particular circuit functionality based on 'matched' components on the same crystal was of course, that the components were practically identical to begin with. Realistic prediction of the magnitude of the stochastic (in)equality (matching) of IC devices has long been a misty subject, driven by 'old lore', horror stories and cooking (trade) secrets. High precision small signal analogue IC design should definitely be seen as a form of Art [Hast01]. Many of the most demanding mixed-signal circuits and systems are (still) realized through trial and error iteration loops, not in the last place because many (stochastic) mismatch effects are not understood or, at least a-priori (during the initial design cycles), not properly quantified and specified. This implies that knowledge on how to achieve certain circuit functionality with high precision matched components has always been a matter of listening carefully to the advice of experienced analogue designers and layout artists on what to do and what not in a particular technology.

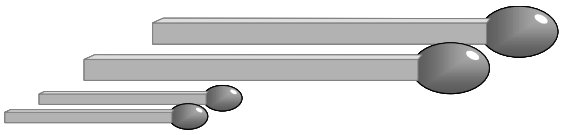

Figure 1.7 First rule of matching: 'large devices match better'.

In the scientific literature, Hoeneisen and Mead were the first to introduce the subject of 'doping fluctuation limitation' in MOS devices (in 1972) [Hoen72]. In 1975 Keys was the first to quantify the effects of Poisson statistics ('randomness in the distribution of impurity atoms') on MOSFET threshold voltage fluctuations [Keyes75]. The pioneering systematic publications on studies of parametric mismatch fluctuations for integrated circuit components must be attributed to McCreary et al. [McCr81] and Shyu et al. [Shyu82&84], dealing with mismatch issues for MOS technology and switched capacitor applications. Lakshmikumar and co-authors [Laks86] first demonstrated that the application of Poisson statistics on MOSFET parameter fluctuations leads to a relation between the mismatch standard deviation of the most common MOSFET parameters and one-over-the-square-root of the area of the devices that are used for the pairs ('1/√WL'). This behaviour, in the modern matching literature often referred to as 'Pelgrom-behaviour' (after [Pelg89]), forms the elementary characteristic that is generally determined for the parametric mismatch fluctuation performance of a device type in a particular technology. Figure 1.8 gives some arbitrary examples of such 1/√WL scaling of the standard deviation of the threshold voltage mismatch for n-channel MOSFET pairs.
The relevance of this example is discussed in more detail in chapter 4 of this thesis.
It must be noted however, that already long before publication of the works discussed above it was 'common knowledge' in the circles of analogue circuit designers that large device pairs yielded better matching performance than those made of smaller dimensions ('large devices match better', figure 1.7).

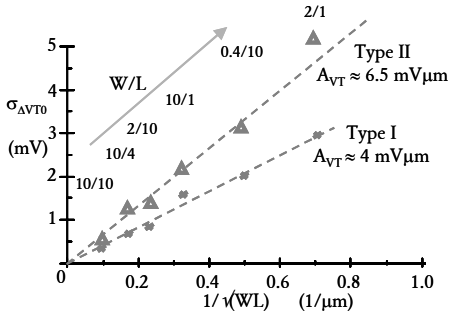

Figure 1.8 Example of relation between device area and standard deviation of threshold voltage mismatch fluctuations. The two types represent different microscopic device architectures.

For a long time, edge (pattern) roughness due to photo mask making, photolithography and etching was seen as the major cause for matched pair mismatch in integrated circuits. Enlarging the dimensions of the components proportionally reduces the effects of these variations. This notion is for instance suggested in the standard work on design of analog integrated circuits by Gray and Meyer [e.g. Gray&Meyer's 2nd, page 392]. On the same page, some graphs demonstrate relations between the mismatch standard deviation and device dimensions for ion-implanted resistors and bipolar junction transistors. Quite often however, information of this kind was not available, and designers had to rely on their gut feeling and search for an optimum through trial and error. In fact, Gray and Meyer (page 393) suggest "The increase in die size and resulting cost generally limits the size of the devices that can be used, but in case of the precision operational amplifier, the input transistors and resistors are generally made as large as practicable". Evidently, speed-accuracy-power (and noise) trade-offs in modern high speed and high performance systems like high performance A/D and D/A converters, place significantly more stringent demands on modern analogue circuit designer's skills (as well as their CAD tools)! [Stey97, King05].

Pelgrom et al. approached parametric mismatch fluctuations from a different direction. They generalised the problem of stochastic device mismatch, based on the central limit theorem of probability theory. By combining (mismatch) probability theory with Fourier transforms to account for random and spatial deterministic effects, a very elegant general mismatch description is obtained. Random local fluctuations are represented in this theory through a 'white noise (spatial independent) contribution', whereas a 'low-frequency contribution' is used to describe deterministic parametric gradients [Pelg89]. The mathematical and physical assumptions that underpin Pelgrom's approach are very important for the philosophy behind some of the work as presented in this thesis. Therefore, they are repeated below.

- the occurrences of microscopic mismatch generating events are mutually independent.
- the effect of a disturbance on a parameter is so small that individual contributions can be summed.
- the total mismatch in a parameter is composed of many events of the mismatch generating process.
- the events have a correlation distance much smaller than the device dimensions.

Under these conditions Pelgrom derived that the standard deviation $\sigma_{\Delta P/P}$ of a parametric mismatch $\Delta P/P$ of parameter P will be inversely proportional to the square-root of the active area $\sqrt{(WL)}$ of the matched component or:

$$\sigma_{\Delta P/P} = A_{\Delta P/P} / \sqrt{(WL)}$$

In which the A-factor $A_{\Delta P/P}$ forms a characteristic process quantity related to the microscopic device architecture fluctuations responsible for the measured parameter fluctuations. This result is in line with the derivation of Laksmikumar et al. [Laks86], based on Poisson statistics applied to the elementary physical quantities like dopant atoms, fixed charges and interface states.
One of the most elegant outcomes of Pelgrom's work is that, although this work was primarily focussed on MOSFET mismatch, the same assumptions and theory can be applied to the matching of other types of IC-elements when the primary assumptions hold. This means that no matter whether one is studying matched MOSFET's, matched resistors, matched capacitors or matched bipolar junction transistors, the same basic $1/\sqrt{(WL)}$ relation can be expected if the four primary conditions as listed above are met for the mismatch generating mechanism!
A few arbitrary examples are depicted in figure 1.9.

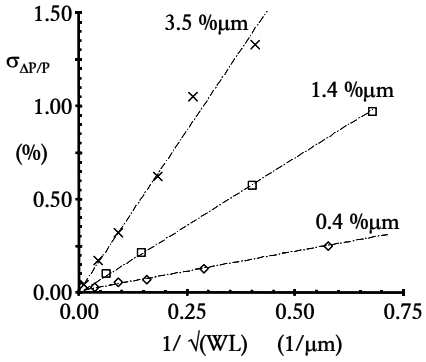

Figure 1.9 Some examples of $1/\sqrt{}$ (area) relation between active device area and mismatch fluctuation standard deviations. Diamonds: resistor mismatch of p-type diffusion resistors; Squares: Collector current mismatch of NPN transistors; Crosses: resistor mismatch of poly-Si resistors.

The 1/√(WL) relation has been revisited frequently in the literature. In the more recent publications, the authors focussed on the implications of random dopant fluctuations. Mizuno et al. for instance, discussed threshold voltage fluctuations from the perspective of large memory arrays [Mizu94]. Other groups explore the effects of random dopant fluctuations on MOSFET performance down to sub 0.1 μm dimensions, using stochastic device simulations (like for instance, Stolk et al. [Stol98] and Asenov [Asen98]). Horstmann et al. presented experimental MOSFET threshold voltage matching measurements that show that (with their method of fabricating transistors), the 1/√(WL) relation remains valid down to transistors with 50 nm channel lengths [Hors97b]. On the other hand, the elementary 1/√(WL) relation forms a recurring subject of debate in the literature [e.g. Bast95, Love96, Wong96, Dren99b, Croo00]. Several groups (in fact most groups!) that studied matching behaviour seem to conclude that the elementary relation proves inadequate to describe their mismatch observations. Such 'funny behaviour' does not necessarily mean that the 1/√(WL) relation is wrong. It merely implies that for that particular set of observations this model does not describe the observations adequately, or in other words, that the underlying mismatch mechanism does not comply with the elementary assumptions of the 1/√(WL) relation. Such observations have resulted in matching model refinements such as, for instance, short channel effects on the threshold voltage [Love94T, Bast95], Source/Drain resistance (theta) effects [Wong96, Croo99], resistor perimeter effects [Dren99b], as well as the relevance of correlations between fluctuating parameters [Serr99, Dren99b].

However, as is often the case in science and industry, from an initial nuisance, an unexpected effect often turns into an interesting opportunity! Indeed, these seeming 1/√(WL) model discrepancies often form in fact a very important signal about the matching performance of a particular technology! Later in this thesis, several examples are discussed, that demonstrate that a discrepancy from the 1/√(WL) model indeed helped to identify the technological cause of the mismatch. An example of such a signal is depicted in figure 1.10. This and other examples are discussed in more detail in chapter 4 of this thesis. Some of these were already discussed in our own publications [Tuin97b, Tuinh03b], but other groups have also elaborated on the value of the area-scaling deviations [e.g. Difr00, Love94T].

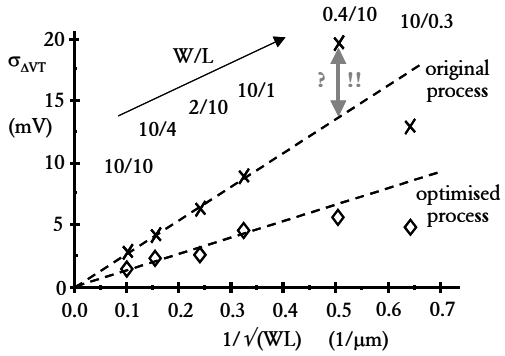

Figure 1.10 $\sigma_{\Delta VT}$ vs. 1/√(WL) for p-channel MOSFET's from [Tuin97b]. A process change results in a strong reduction of the A-factor as well as a distinctly different area-scaling behaviour.

Over the past decade, the scientific foundation for the field of parametric mismatch fluctuations characterisation has received substantial solidifications. This can primarily be attributed to the strongly increased impact of PMF on the performance of mixed-signal as well as ULSI (embedded) memory IC's. The elementary 1/√(WL) area-scaling law predicts that parametric mismatch fluctuations increase with the ever-decreasing minimum device dimensions. Indeed, it is observed in the most advanced deep-submicron technologies that random parametric fluctuations for minimum size devices are of the same order of magnitude as the parametric ranges given by traditional worst-case corner models. This explains the needs for better mismatch models, new statistical circuit design methods and better understanding of the causes of parametric mismatch fluctuations. The number of matching related papers in the scientific literature has seen a steady increase since the early 1990's [Dren99Th]. In particular, the studies summarized in PhD theses by Bastos (1998), Drennan (1999), Difrenza (2002) and Croon (2004) have contributed to a much wider understanding of the use and limits of parametric mismatch fluctuations.

1.3 What's in a number?

As mentioned before in this chapter, electrical performance spreads of integrated circuit components generally run in the tens of percents over the lifecycle of their technology. The main motivation for the widespread use of matched components in analogue circuit designs is that the analogue designer can base certain circuit functionalities on the assumption that closely spaced identically designed devices show an equality of performance that is substantially better than predicted by the spread ranges. The questions that are raised at this point are: how equal should matched components be, how equal can they be, and what does that mean for characterisation techniques for parametric mismatch fluctuations?

Mixed-signal circuits need parametric mismatches below 1%

For signal processing, one always needs to discriminate the signal information from the signal disturbances. This is done either through differential signal evaluation or by comparing with a reference of some sort. This implies that non-linearity in the signal processing due to unanticipated device inequalities (mismatches) may show up as gaps, distortions, or other wrong interpretations of the signal. Hence, process spreads, common for all components of a building block, in essence only affect the overall speed and/or power consumption of the entire block. Parametric mismatch fluctuations on the other hand, can affect the signal interpretation. Therefore, a 1% mismatch (or offset) between two devices in a chip is often more devastating for a mixed signal chip than a 10% spread across a wafer. A simple example can put this 1% level into perspective (figure 1.11).

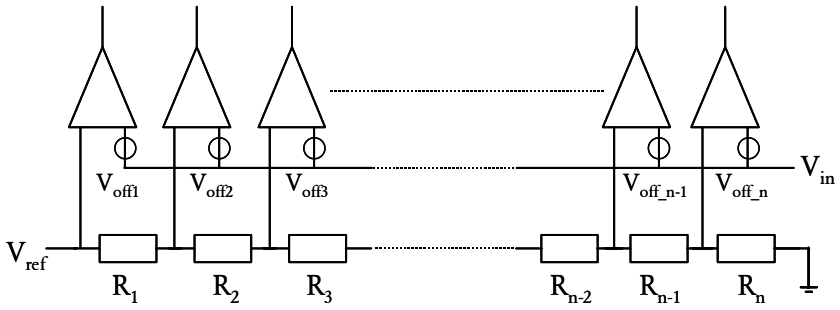

Figure 1.11 Schematic diagram of a resistor ladder ADC configuration. The resistor elements (Ri) as well as the comparators' offsets (V_{offi}) must have mismatches less than 0.5 x intended LSB.

Suppose one wants to convert an analogue sample (V_{in}) into a binary code with a simple resistor ladder voltage divider, a reference voltage, and a set of comparators. For an 8-bit analog- to-digital converter (ADC), this implies that the least significant bit (LSB) equals to $1/2^8$ or 0.39% of the full scale. This means that the resistor elements (R_i) of the ladder must 'match' better than 0.5 x 0.39%. A 12-bit resolution converter corresponds to 0.024% and a challenging '14-bitter' requires 0.0061% or 61 ppm's! For the (randomly fluctuating) offset voltages (V_{offi}) of the comparators, dominated by the mismatch between the two differential input transistors of the amplifier, the same reasoning can be applied. If one assumes a peak-peak voltage signal of 1 Volt, a 10-bit converter will divide this in 1024 levels, meaning that each step between the levels (LSB) corresponds to $1/2^{10} < 1$ mV. The random input offset voltage (e.g. the threshold voltage mismatch of the differential MOSFET input pair, or the V_{be} offset of the BJT input pair) must therefore be less than 0.5 mV.

Silicon devices reluctantly render mismatches below 1%

Whereas parametric process spreads easily run into the tens of percents, parametric mismatches can indeed be reduced to levels well below 1%, albeit that this does require special attention. In the first place, small mismatch necessitates large devices. If one excludes process disasters and some very unsuitable device architectures, a gross simplification learns that parametric mismatch fluctuation A-factors for most silicon device types are in the range of 1 to 10%μm (see for instance figure 1.9). Hence, when these devices follow the common $1/\sqrt{(\text{area})}$ scaling law, one can indeed create mismatches substantially below 1% by making the device dimensions large enough. For instance, using a device-type with a 1%μm mismatch A-factor, 8-bit (1%; 40 dB) resolutions can be reached with device areas of the order of 1 to 10 μm^2. A 0.01% PMF (for instance for a 12-bit high resolution ADC) would require matched devices with areas of over 10^4 μm^2 each! Apart from their large (expensive) silicon-area consumption, components of such dimensions can only be used in integrated circuits at the expense of substantial increase of the device capacitances (resulting in speed / bandwidth loss) and/or excessive power consumption. However, at parametric uncertainty levels below 1%, many other seemingly minor physical semiconductor device disturbance effects tend to become relevant. A notorious example is formed by mechanical stress. Due to the complex construction of integrated circuits, with many layers and different materials, local mechanical stress differences are frequently encountered. In particular asymmetrical metallisation patterns on or near matched devices often results in unanticipated stress differences. Through the piezo-resistance or –junction effects, parametric changes of the order of 1 to 5% are quite common.

Chapter 4 of this thesis discusses several examples of such encounters. A parametric change of a few percents not seldom goes unnoticed in the total specification ranges and parametric fine-tuning of an IC technology, but at a parametric mismatch level, they can be huge! Moreover, stress effects have a remarkable span. This implies that a local stress source can affect silicon devices that are tens of microns away. This is exemplified in [Tuinh04a], were we show that the systematic mismatch impact of mechanical stress falls-off roughly by a factor of two for every 10 microns of additional distance. This places a major burden in terms of extra area and layout skills required for high precision small signal (matched) circuits, as the layout environment of as much as 40 to 80 microns around the matched components must be identical when mismatches substantially below 1% are required!
In addition to environmental layout effects, parametric gradients associated with wafer processing non-uniformities may form a mismatch limitation. Well-controlled production technologies generally show parametric gradients of the order of 1%/cm (1 ppm/μm) or better. This means that for carefully designed matched devices with design-pitches typically less than 100 μm, distance effects are negligible. This may however not always be the case for larger systems on chip when the circuit architecture requires matching specs to be maintained over distances up to several millimetres.
These examples demonstrate why it is not always trivial to reach mismatch levels below 1%. In this sense, parametric mismatch fluctuation studies serve as a kind of microscope, as they suffer from / reveal subtle effects about IC technologies that generally remain hidden during standard process control and parametric tests.

Parametric measurement accuracy

The fact that process spreads are generally of the order of tens of percents also has implications on the performance of standard semiconductor parametric measurement systems.
Again allowing an oversimplification, one can state that measurement systems that are used to characterise and control the electrical performance of integrated circuit technologies are aiming at measurement accuracies of the order of 1% (and 1 mV). The actual measurement hardware of production parametric testers is usually based on 12- to 16-bit DAC's (sources) and 16- to 20-bit ADC's (meters), hence significantly more resolution than 1%. Common parametric measurement algorithms however, are generally tuned for reaching sufficient accuracy (1%, 1 mV) at the highest possible speed (typically tens of milliseconds). This makes sense, as many thousands of measurements are to be collected for assessing the performance of each lot of wafers that is processed in a fab that varies tens of percents anyway. This implies however that special precautions are required for precise parametric mismatch measurements.

It may be inevitable to acquire better / dedicated measurement hardware, but usually it is possible to make much more accurate mismatch measurements with the existing hardware. By careful selection of biasing and measurement settings, a significant accuracy boost can usually be achieved. Chapter three of this thesis is largely devoted to discussing possibilities and limitations of measurement systems for parametric mismatch assessment. In the most general sense, it can be stated that (mismatch) measurement accuracy can be traded-in for measurement speed. This immediately identifies the dilemma of PMF measurements, namely, as mismatch measurements are by definition looking at statistical effects, one wants to be able to measure sufficiently large populations (as fast as possible) to provide statistically significant PMF estimators. This means that one generally cannot spend more than a couple of seconds to a few minutes (for extreme precisions!) of measurement time per device.

Matching categories

Although it may again come across as a gross generalisation, a surprising similarity can be identified with respect to the levels at which high precision matched circuit realisation becomes difficult, compared to where mismatch measurements become hard.

- Relative mismatches at a level of 5 to 10 percents can generally be measured without any precautions or dedicated measurement algorithms. In circuit design, such levels are usually easily reachable as well (unless the smallest device dimensions must be used). At these levels (small devices), adjacent layout effects (mechanical stress variations) are generally negligible compared to spread and mismatches.
- Below 1% the challenges start. Up to the 1% level, layout symmetry in high precision small signal circuits must be maintained up to a level of 20 microns from the matched components. This also is the limit below which measurement algorithms require extra care. Good selection of bias conditions and integration times are required, while it may be worthwhile to keep an eye on the short-term repeatability of the measurements.
- Below 0.1%, we come to levels where most measurement systems reach their specification limits. Repeated measurements are necessary, long integration times inevitable, range changes must be avoided, and offsets of meters and sources may begin to affect the results. On the circuit design side everything must be done correct as well. Large components (order 100 μm^2 and larger) are required, extreme care must be taken to avoid offsets due to unforeseen voltage drops and parasitic resistances. Layout symmetry (including adjacent layout features) must be maintained up to 40 to 80 microns around the matched components.

- Below 0.01%, dedicated measurements systems and algorithms are inevitable. Regular hardware offset checks must be performed. Continuous monitoring of system noise and short-term repeatability are unavoidable. Relatively large current levels must be used (mA-levels). Such levels require Kelvin-sensing to avoid effects of probe-pad resistance effects. Precision of long (multiple) measurements may be hampered by temperature variations in the measurement lab. For analogue circuit designs, this is the true nightmare arena. Theoretically, it is possible to reach these kinds of precisions with extremely well engineered device architectures, but in practice disturbances come from everywhere. Layout symmetries must be maintained to distances over hundreds of microns (at least for silicon devices).

1.4 What's in the project?

The insights and results that are presented in this thesis were acquired at Philips' Natuurkundig Laboratorium in Eindhoven since 1992 in the so-called 'Limits of Matching' project, essentially a one-person Philips Research project supported by Philips Semiconductors. This project was initiated as a follow-up on successful practical and theoretical work on MOSFET matching by Pelgrom and co-workers in the eighties of the previous century [Pelg89]. Moreover, the project fitted-in very well with one of Philips Research's strategic intentions to maintain its well-recognised strong knowledge position in analogue and mixed-signal integrated circuits.
The main goal of this project is to gain more insights into physical mechanisms that cause mismatch, with obviously as underlying -and most important- objective, to improve the matching performance of Philips' IC technologies and Philips Semiconductors chips.
Different types of matched IC elements (Resistors, Capacitors, MOSFET's and Bipolar Junction Transistors) were studied for many of Philips Semiconductors' and (Philips Research's) different flavours of IC technologies. Matching studies ranged from typical analogue bipolar (and even discrete) devices, via high performance mixed-signal (Bi)CMOS, down to evaluation of new device constructions for future process digital CMOS generations. The multitude of devices and technologies that were investigated during this project resulted in a unique collection of examples of what can be achieved in terms of matching of IC elements as well as things that can (and do) go wrong.

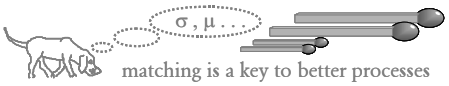

Figure 1.12 Symbols of the 'Limits of Matching' project.

Contributions to the art

The work that underpins this thesis has resulted in the open literature papers listed in part 1 of the Bibliography. The remainder of this section briefly summarises the main contributions of these papers to the field of parametric mismatch characterisation. These contributions are grouped according to the three main topics of this thesis:

- matched pair test structure improvements
- enhancements to statistical high precision DC parametric mismatch measurements and data analysis techniques
- process and device architecture fluctuation interpretations

Matched pair test structures

Detailed discussions on suitable test structures for characterisation of parametric mismatch and fluctuations were practically non-existent in the open literature prior to our regular entry into this field. The introductory paper [Tuin94] and several tutorial short course lectures at the main forum for semiconductor process and device characterisation, the international conference on microelectronic test structures (ICMTS), served as a basis and reference for many later test structure discussions. Mismatch characterisation test structures now form a regular subject at this conference. Most of our contributions were very well received and on three occasions, this resulted in being honoured with the best paper award at this specialists' conference.

- In the ICMTS97 paper [Tuin97a], we expanded our initial work on metal coverage effects on MOSFET mismatch [Tuin96b], using a comprehensive set of (a)symmetrically covered MOSFET matched pairs in different orientations. This demonstrated quite convincingly that mechanical stress forms the explanation for a remaining systematic offset after solving the hydrogen passivation problem that caused the initial (IEDM96) mismatch problem.
- The awarded ICMTS2000 paper on characterization of systematic transconductance mismatch in MOSFET's [Tuinh00a] comprised a combination of test structure design issues and measurement system evaluation and improvement. By careful assessment of hardware and software limitations, a new systematic mismatch effect (CMP metal tile placement) of the order of 1% and below could be demonstrated.
- The third paper that was awarded, at ICMTS 2002, dealt with an extreme case of systematic mismatch reduction for high precision resistor ladder layouts for 14 bit ADC applications [Tuinh02a]. By employing a new test structure approach based on prober sub-site steps and a dedicated data analysis procedure it proved possible to identify and improve extremely small ($<$0.05%) systematic mismatch effects associated with nm-scale mask-writing artefacts.

Furthermore, we are regularly referenced in the matching characterisation field for our so-called floating Gate capacitor mismatch characterisation technique [Tuin95, Tuin96a]. This is a technique that uses standard DC parametric measurement systems for measuring capacitor mismatch through a capacitive voltage divider and a Source follower transistor to monitor the voltage at the common point of two supposedly equal capacitors. This approach has been followed quite extensively and several refinements have been proposed by other groups.

The Common Emitter & Common Collector test structure approach for characterising matched BJT pairs was introduced in [Tuin94] and discussed in more detail in [Tuin98]. This test structure architecture was proposed to make optimum use of the number of contact pads and perfectly suited for high precision (down to 100 ppm) mismatch measurements using a standard bench-top parametric measurement system such as the HP4156. For many years, this approach

resulted in the most accurate as well as best reported matching results for bipolar transistors. More recently, our current mirror test structure approach for characterising adjacent layout effects [Tuinh03a, Tuinh04a] has attracted considerable attention.

Mismatch measurement and analysis techniques

Novel elements of mismatch measurement and analysis techniques that we investigated and reported covered a wide range of subjects. In [Tuin96a and Tuinh01a] measurement system noise suppression and the impact of low frequency device noise are discussed. In [Tuin98, Tuinh00a, Tuinh02a, Tuinh03a, Ewert05] we carefully considered various measurement system limitations and the importance of robust statistical analysis techniques and statistical uncertainty assessment. Furthermore, we reported the impact of threshold voltage mismatch extraction technique on the perceived process performance assessment. This was done in collaboration between several matching characterisation groups [Croo02a].
When the literature on parametric mismatch fluctuation characterisation is analysed, one cannot but admit that (statistical) characterisation hard- and software is apparently seen by most people as an inevitable but hardly appealing part of mismatch characterisation. Unfortunately, it must be concluded that many matching related papers presented at conferences or in journals suffer from elementary measurement and analysis mistakes. It is in fact with this in mind that chapter 3 of this thesis was written. It discusses best practices for mismatch characterisation in the hope that some of the regularly encountered errors will be avoided in the future.
Recently, we reported the results of our own efforts to combine such best practices in our latest high precision mismatch characterisation system [Ewert05]. This Keithley 4200 SCS based system has set the standard for high precision mismatch measurements to an entirely new level. We achieved short-term repeatabilities of better than 10 ppm for challenging BJT mismatch measurements. Moreover, we demonstrated that the C-coded test libraries, running on a fast built-in processor provide the statistical analysis power and graphical user interface that make mismatch characterisation studies a lot more efficient and much less prone to unexpected measurement and statistical errors.

Microscopic device architecture fluctuation interpretation

In contrast to characterisation techniques, characterisation and interpretation of microscopic device offset and fluctuation effects result in publications that are generally more appealing. On one hand, this is due to the unquestionable attraction of subtle stochastic device physics effects underlying parametric mismatch observations have for many IC process technologists and physicists. On the other hand this is quite understandable, as proper identification of such

effects often leads to process or layout improvements and hence product yield and profit gains ('matching is a key to better processes'). During this thesis work, several interesting new, or recurring, mismatch effects were identified and reported.

- Parametric gradients can affect the observed mismatch fluctuations. NPN BJT Quads matched pair test structures with relatively large active device dimensions can be used to identify such cases. The first time this was actually reported was in [Tuin94]. Later, several other authors have addressed this same subject.
- One of the most valuable highlights was the work underpinning the 1996 IEDM paper [Tuin96b]. In this paper, we reported the impact of metal coverage on MOSFET matching. We found that Ti/TiN/Al metallisation over MOSFET's inhibits the imperative (hydrogen) passivation of the Si / SiO_2 interface. Apart from the identification of a highly interesting (mismatch) effect, this work proved extremely beneficial for the technology's performance, as the yield of several important mixed-signal products increased considerably after introducing an optimised anneal procedure.
- As a follow-up of the hydrogen passivation study mentioned above, we investigated we systematic mismatch effects due to metal coverage of MOSFET's [Tuin97a]. In essence, demonstrated that asymmetrical metal coverage could be detrimental for current matching up to a level of several percents. We found that mechanical stress as built-up during the back-end process is responsible for the observed asymmetrical mismatches. It may seem quite unlikely that circuit designers would dare to place such metal asymmetries near, or even on critically matched pairs, but in reality there are many circuit implementations where a designer is tempted to 'forget' such simple rules, in particular when there is no quantitative evidence or reports of the hazards. This work proved useful for persuading designers not to experiment lightly with such layout solutions.
- A study leading to enhanced BJT product yields was reported only recently in [Tuinh03c], but in fact was based on work that was conducted early in the project. We demonstrated that the emitter poly-mono interface layer treatment for NPN BJT's in advanced BiCMOS technologies can have devastating effects on the base current mismatch, up to a level where it hampered the yield of particular ADC products. By improving processing steps prior to the poly-Si deposition, the yield could be brought to acceptable levels.
- Another instance where parametric mismatch fluctuation studies were instrumental to BJT product yield enhancement is also briefly touched upon in [Tuinh03c]. In this particular example, an unexpected area scaling effect, caused by horrendous base current mismatch fluctuations for narrow emitter devices, resulted in the conclusion that a diffusion barrier to prevent alloying / pitting of the emitter metallisation provided insufficient protection.

Although the actual parametric fluctuations of the large emitter area products proved too small to affect the parametric yield seriously, we found that the same alloying mechanism that caused the mismatch fluctuations was also responsible for a significant (functional) yield loss (Emitter-Base shorts).

- One of the most thrilling examples of how characterisation of matched pairs can contribute to process improvements formed the basis of the 1997 IEDM paper [Tuin97b]. This study showed for the first time, that gate depletion and boron penetration effects contribute significantly to threshold voltage mismatch fluctuations of deep submicron MOSFET's. Apart from the fact that this provided interesting new insights into a (dominant) device fluctuation mechanism, this particular result proved extremely valuable as this was a first example where excessive parametric mismatch fluctuations were found to limit the yield of digital circuits, in this case embedded SRAM blocks in large SoC's. Again, it proved possible to bring the process yield back to par by improving the process (fine-grained poly and appropriate spike anneals). Since then, the parametric mismatch fluctuation sensitivity of embedded SRAM's has remained an important process architecture and control issue [Stolk01, Tuinh02b].
- The most striking result of [Tuinh00a] proved the observation that (carelessly placed) CMP dummy tiles can affect the systematic mismatch between MOSFET pairs. This has resulted in significant commotion in the analogue circuit design and layout world as this means that extra precautions must be taken to avoid undesired systematic mismatch effects due to (automatic) placements of CMP dummy features.
- Another technological as well as scientific highlights of the project was the so-called 'decaborane example', presented at the 2000 VLSI symposium [Tuinh00b].
  We demonstrated increased stochastic fluctuations in MOSFET's that were fabricated with decaborane channel implants (fragmentation bombs) compared to those fabricated with regular boron implants. This turned out to be a clear and direct demonstration of stochastic nature of the ion implantation process.
- One of the novel results added to the 2001 IEDM invited paper [Stolk01] was the first demonstration of the potential benefits of metal gates for MOSFET threshold voltage mismatch fluctuation reduction.
- A heritage of our gate morphology optimisation work was also highlighted in this paper, showing for the first time in the open literature that it 'pays' to work on the matching performance during the process engineering phase (even in a 0.18 micron CMOS production line).
- In [Dubo02] we were the first to report threshold voltage mismatch degradation due to

(poly-Si grain orientation related) ion implantation channelling through the Gate, which could be repaired through various technological measures, such as adjusting the implant energy, applying an amorphous scattering layer, and using fine-grained poly.

- In [Pine04] we reported for the first time the occurrence of significant mismatch fluctuation enhancements for MOSFET's in the subthreshold regime, which severely limit the attainable low-power leakage specs of many deep-submicron CMOS technologies.
- In [Tuin02a] we reported for the first time that mechanical stress due to metallisation asymmetries affects the mismatch of very high precision matched elements (below 0.1% levels) up to many tens of microns away from the supposedly equal resistor ladder elements. By careful layout optimisation, we were able to reach a DNL level that was limited by (within spec) nanometer dimensional deviations of the photo masks.
- In [Tuinh03a] we were the first to demonstrate in a consistent manner that transistor connections and asymmetries of the layout environment around matched NPN BJT's affect the quality of high precision current mirrors [below 0.25%].
- In [Tuinh04a] we demonstrated that the systematic mismatch effects due to stress caused by asymmetric adjacent layouts, affects high precision MOSFET current mirrors to approximately the same level as BJT mirrors. Moreover, we were the first to quantify the span of layout asymmetries and found those to decay roughly with a factor 2 per 10 microns of additional distance. For analogue circuit designers this work yielded the rather shocking conclusion that for high precision building blocks, layout symmetry must be maintained up to as far as 40 to 80 microns around the matched components.
- In [Wils05] we showed for the first time that it is possible and useful to combine selected TEM observations with BJT mismatch measurements. The occurrence of an unexpected area-scaling deviation of the base current mismatch standard deviation led to the identification of a new mismatch mechanism, namely enhanced local base currents due to local encroachment of the emitter silicide towards the poly-mono interface in advanced double-poly BJT's.

In addition to the publications summarised above, over 50 -not publicly accessible- lectures were given at many different sites (Philips Research, Philips Semiconductors fabs and design centres, Technical University of Delft, ST-Microelectronics, National Semiconductors, HP labs, CERN and Motorola). Since 1997, a lecture on Matching of MOS transistors (developed and presented in turns with M. Pelgrom and M. Vertregt) forms a regularly recurring and highly appreciated subject in several of MEAD electronics' advanced engineering courses on transistor level analogue and low-voltage / low-power circuit design of (these courses are organised in conjunction with EPF-Lausanne and EuroPractice).

1.5 What's in the rest of this thesis?

The purpose of the project underlying this thesis was twofold: in the first place the goal was to improve IC devices in terms of parametric mismatch fluctuation performance. Mismatch performance is crucial for many of Philips' integrated circuits and systems. Improving PMF device performance requires detailed understanding of the physics of microscopic device architecture fluctuations as well as of the technology that is used to make the devices. Through measuring and benchmarking many different devices and technologies, we found that subtle new device effects appear frequently at low mismatch levels. These effects are not seldom overlooked during the development of new technologies (because their impacts are small compared to the common –digital- device performance indicators), but they can prove devastating for high precision analogue circuits. However, and this leads to the second purpose for this thesis, it also turned out rather quickly that at the levels these devices need to be characterised, additional demands are placed on test structures and measurement methods. Matched pair test structures must be defined and laid-out with more care, careful avoidance of parasitic resistances (differences), proper use of contact pads, and the highest degrees of layout symmetry. Parametric mismatch measurements must often be done at higher precisions than commonly attained (required) for semiconductor device characterisation; and since PMF is statistical phenomenon, additional care must be taken to ensure proper data interpretation (there are lies, damned lies and statistics...). Moreover, the choice of the test structure and the measurement method are often closely related to the effects that can be assessed.
Therefore, it was considered indispensable to address the three topics that correspond to the three main chapters of this thesis.

Chapter 2 is about matched pair test structure design. After introductions on the place and role of test structures in IC technology assessment and the dilemma whether to use arrays or populations of paired devices for PMF characterisation, some typical mismatch test structure issues are discussed. In this chapter, contact pad considerations and the selection and prioritisation amongst the sheer infinite number of possible parametric mismatch effects that can be studied are examined. After summarising guidelines for proper matched pair test structure design, the chapter ends with some (good and bad) examples of MOSFET and BJT matched pair test structure implementations. Chapter 3 discusses matched pair characterisation techniques. After an overview of measurement hardware considerations, and addressing the questions whether to use switch-matrices and thermo-chucks, the relevance (and various types of implementations) of short-term repeatability assessment techniques are discussed. Subsequently, some tricks of the trade related to measurement algorithm implementation for

high precision parametric mismatch measurements are reviewed, culminating in the so-called MxSy measurement algorithm. The section on data analysis techniques elucidates the relevance of safe statistical estimation and bootstrapping for PMF characterisation. This chapter is topped off with an example that demonstrates and quantifies some of the subtle problems that are encountered when parameter extraction is done at (or beyond) the capability specs of the measurement system. Chapter 4 discusses examples of matched pair characterisation as a tool for IC process evaluation. However, rather than treating the physical and technological results and phenomena in depth, the discussed cases focus on using so-called trouble signals that are used to characterise mismatch phenomena and identify abnormalities. The examples combine some of the subtleties from chapters 2 and 3 with some of the physical phenomena underlying mismatch occurrences in integrated circuits. Finally, chapter 5 summarises the main conclusions of this thesis and speculates on the outlook and future challenges of this extremely interesting, useful and profitable playing field of parametric mismatch fluctuation evaluation.

Chapter 2

Matched pair test structure design

2.1 Introduction: "if you cannot measure it, you cannot improve it"†

Parts of each integrated circuit wafer are reserved for electrically measurable test structures for verifying and/or studying the IC fabrication process. Following Lord Kelvin's reasoning, it is not illogical to suggest that electrical test structures form the foundation of all IC technology and device improvements.

Many different types of electrical test structures can be identified. Some are used to characterise thickness of layers and their CD's (Critical Dimensions), others for assessment of intra- and inter-layer continuity and isolation of all conducting layers of the IC process. An important group of test structures provides access to active and passive devices (transistors, resistors, capacitors) for assessment of the electrical performance, limitations and reliability of the most relevant integrated circuit elements. Characterisation of mismatch also requires dedicated test structures. Although matches pair test structures may appear very similar to regular device characterisation and modelling structures, they are in fact more susceptible to (minor) layout asymmetries and parasitic resistances. Therefore, matched pair test structures must be configured with a different mindset than regular test structures for process and device characterisation. Moreover, also due to the high measurement precision requirements for assessing the (often relatively small) parametric differences, matched pair test structures require additional layout precautions and considerations. This chapter discusses justifications as well as practical implementations of such measures. After a general introduction on PCM's, PEM's, MPW's and pad frames, section 2.3 explains why so-called array test structures are less suitable for fundamental research on parametric mismatch fluctuations than traditional contact pad oriented test structures. The specific relevance of contact pads for matched pair test structures is explored in more depth in section 2.4. The common practice of sharing pads among terminals for test structure design is discussed from the perspective of matched pair test structures. Furthermore, it will be demonstrated that probe-to-pad resistance fluctuations form an annoying threat that should continuously be kept in mind when designing and measuring matched pair test structures. Section 2.5 discusses matched pair test structure selection.
An overview is given of the most appropriate device geometries and layout alternatives that should be available for PMF characterisation. The problem with systematic mismatch effects and layout alternatives is that a sheer infinite number of implementations can be identified as possibly interesting for analogue circuits layout. Based on accumulated experiences and

†Sir William Thomson (Lord Kelvin). In fact, this is the theme of the ICMTS, the International Conference on Microelectronic Test Structures. This theme was introduced for the conference by one of the conference's founders, Martin Buehler [Tuto9x].

literature results, a prioritised list of suitable structures is discussed. Section 2.6 consists of two sets of guidelines for matched pair test structure design and layout. The first set focuses on conceptual choices that must be made before starting any mismatch characterisation study. The second list provides more specific layout guidelines for matched pair test structures. Section 2.7 presents a number of layout examples of BJT and MOSFET matched pair test structures. These are discussed to demonstrate that, at first sight minor (almost cosmetic), layout refinements can help to avoid uncertainties that would hamper the data analysis.

2.2 PCM's, PEM's and pad frames

A collection of electrical test structures on a product wafer is called a Process Control Module (PCM) in Philips' terminology. In the semiconductor industry alternative terms like process control structure, tester, test element group (TEG), or test bar are encountered for such collections. Electrical measurements are done on the test structures of a PCM after completing the processing. They are intended for verifying the correct execution of the process flow and to determine whether the wafer (or lot) is within performance specifications. These measurements are used to decide whether the wafers are worthwhile to proceed to product/e-sort testing and eventually dicing and packaging.

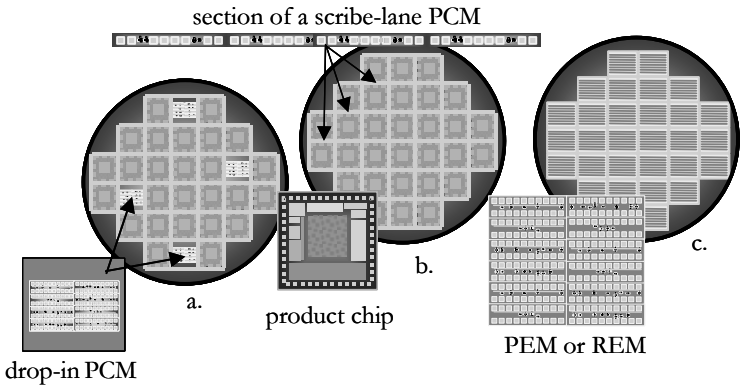

Figure 2.1 PCM's and PEM's on silicon wafers.

In older IC technologies (e.g. 1 μm lithography and larger), the test structures of a PCM were grouped in so-called drop-in positions (Figure 2.1 a). This meant that the PCM's (typically 3 to 5 per wafer) replaced potential product chips, thus reducing the possible number of product dies on a wafer. Figure 2.2 gives an example of a widely used contact pad arrangement (pad frame) for semiconductor test structures. The so-called 2xN pad frame (with N typically ranging from 8 to 24) proves convenient for probe card and measurement procedure standardisation [Tuto9x].

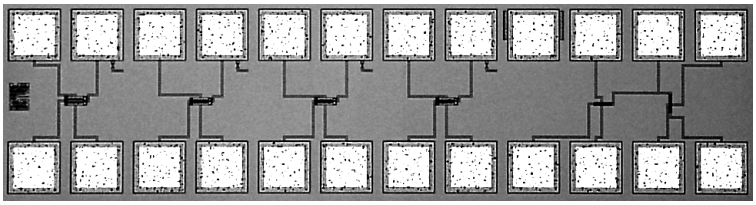

Figure 2.2 Example of a 2xN pad frame module for test structures (N=12).

In contemporary IC technologies, PCM's are placed in the scribe line (saw lane) between the product dies (Figures 2.1 b and 2.3). This saves wafer space and photo masks (reticles), and improves wafer throughput during litho processing. Since the available width in a scribe line is usually not much more than 100 μm, the contact pads must be placed 'in line' (1xM pad frame, figures 2.3 and 2.4). An additional advantage of scribe line PCM's compared to drop-in PCM's is that they are available on more positions on the wafer (at least once for each reticle exposure). This provides possibilities for more extensive characterisation, such as parametric gradients across the wafer for assessment of wafer uniformity, or statistical analyses with reduced statistical uncertainty. Due to silicon area as well as test time limitations, PCM's are always severely restricted in terms of the number of available test structures within each PCM.

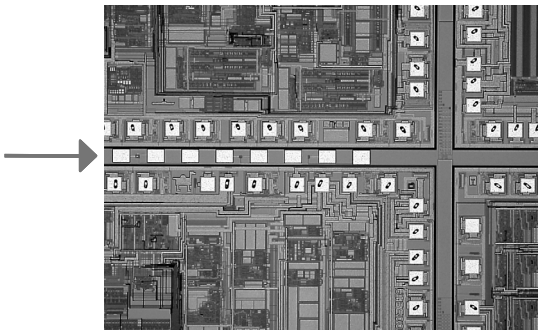

Figure 2.3 Scribe line test structure located between product dies.

Figure 2.4 Example of a 1xM pad frame module for a scribe line test structure.

For the development of new technologies, dedicated Process Evaluation Module or Mask-sets (PEM's) must be designed. PEM dies are usually much larger than PCM's since they must provide room for many more types and flavours of test structures. PEM's are repeated over the entire wafer (figure 2.1 c). A PEM is used for studying and optimising device architectures and layout rule optimisation, as well as model parameter extraction for active and passive components. Various types of functional circuits, such as small-to-medium sized memory blocks and speed benchmark circuits like ring oscillators are commonly added to PEM's. Such circuits are used to assess yield status and speed/power performance for the new technology. Reliability (lifetime) hazards of the process under development, like Electro-Migration, Electro Static Discharge susceptibility, Hot Carrier degradation and Negative Bias Temperature Instabilities are generally evaluated using a dedicated PEM version, often called Reliability Evaluation Module (REM). PEM's for high frequency or mixed-signal technologies contain sections with test structures for hf and analogue characterisation issues such as noise and parametric mismatch**.** Matching test structures in PEM's usually cover a range of matched pair device geometries (e.g. figure 2.5) as well as a set of more specialised structures related to particular mismatch hazards in the technology under development. The repetition of a PEM over the complete wafer helps to collect comfortable population sizes (40 to 100 pairs) for the statistical characterisation of parametric mismatch fluctuations.

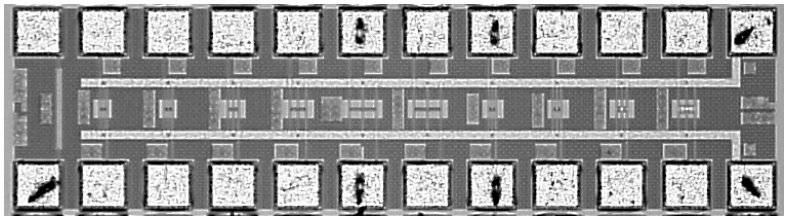

Figure 2.5 Example of a 2xN PEM module with 10 NPN BJT pairs.

Mismatch characterisation test structures are not so common in PCM's. Due to limited available space, a full range of matched pair test structures should certainly not be expected in a standard PCM. Other common arguments for not reserving PCM 'silicon real estate' for matching test structures are: too low measurement system accuracy for standard parametric test system / measurement algorithm combination, and the too low number of testable PCM's in a complete batch.

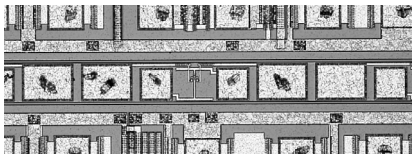

Figure 2.6 Example of an NPN BJT matched pair in a scribe line module.

Nevertheless, there are several good reasons why it may be important, useful and feasible to add at least some matching test structures to a PCM. Particularly for matching sensitive products (e.g. high resolution A/D converters), it is helpful to monitor the matching performance, as this quantity can determine the yield of the product [Pelg94, Tuinh03c]. Even when only a few mismatch observations are collected on each wafer, monitoring the mismatch over a large number of wafers from different lots can provide adequate population sizes to verify the PMF performance of a technology. Matched pair test structures in scribe line PCM modules (figure 2.1 b and 2.6) have an edge in this respect, as they are available in larger numbers on each wafer. Measurement accuracy does not necessarily have to prevent placing matched pairs in a PCM as long as the dimensions of the matched devices are chosen sufficiently small (hence yielding relatively large parametric mismatch fluctuations). Some of the matched pair test structures that are discussed in this thesis were not placed in PEM's nor in PCM's, but on so-called Multi Project Wafers (MPW's). These are the regular (quarterly, bi-monthly) tape-outs for reticle sets with test circuits and building blocks of larger systems. Such MPW's proved very useful for evaluating new mismatch test structures, to test a particular hypothesis for a suspected matching (process) disaster, to measure new effects or verify ideas for these, or just to get some mismatch characterisation material in an early test version of a technology. MPW's are generally processed very fast, and not unimportant, since MPW mask sets are processed only once, silicon area constraints are usually less stringent compared to a complete PEM that is to be used for evaluating many more aspects of the technology.

2.3 Pairs or arrays?

In the field of parametric mismatch characterisation, two major camps can be identified. On one side, there are the (old-fashioned?) groups that base their studies on populations of conventional pad frame oriented device pairs. Another (growing) group consists of those who use medium sized arrays of individually accessible devices. Despite some clearly identifiable advantages of array structures, practically all results discussed in this thesis were obtained using conventional 2xN or 1xM pad frame matched pair test structures. This section summarises the arguments for this choice.

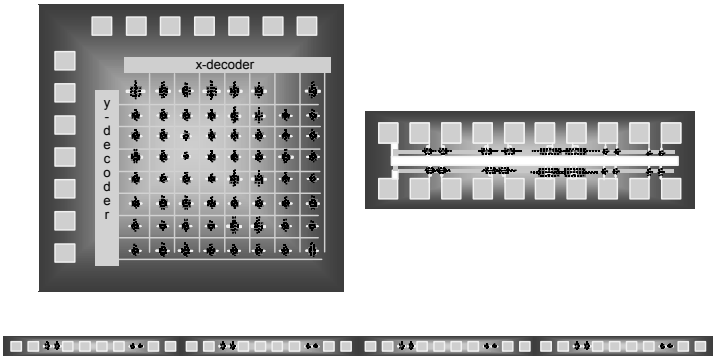

Figure 2.7 Closely spaced matched pair test structures in 2xN or 1xM pad frames (right & bottom) and an addressable array test approach (upper left).

The closely spaced, identically designed device pair is in fact the simplest test structure that meets the main requirement for studying stochastic parametric mismatch effects, namely the insensitivity for spread and spatial parametric gradients. They are relatively easy to design (layout) and least prone to design errors and adjacent layout effects. The main limitation of the use of conventional matched pair test structures is the population size per wafer. The high contact pad 'consumption' of conventional test structures prohibits placement of large numbers of pairs on a test chip. PEM's for modern technologies are generally so large that the number of testable dies (hence matched pair population size) usually ends up in the range of 30 to 100 pairs per pair design per wafer. Another drawback of the matched pair test structure that is frequently mentioned is that the layout environment and device density in a typical test chip environment can differ substantially from the circumstances as encountered in 'realistic'

integrated circuits. It is well known that dense areas of a masking layer may result in different device performance compared to those observed for single lines running in open spaces (proximity effects).

Addressable arrays of testable elements (figure 2.7 upper left) have become quite common in the world of parametric testing and IC process characterisation since their introduction in the late eighties [Blae88, Saya89]. In fact, the advantages of the array test structure are exactly the points that were mentioned above as disadvantages for matched pair structures: population size and photo-mask density. A good example of the application of arrays in the field of mismatch characterisation is the ground-breaking work of Mizuno et al. [Mizu93, Mizu94] that assesses stochastic variations of threshold voltages in relative large (8k) arrays of (memory) transistors. Several other groups have reported parametric fluctuation studies based on addressable arrays [Pava94, Niew97, Port98, Scha00, Shim02, Ohka03, Quar03, Leff03, Einf04].
Addressable arrays naturally prove particularly efficient in terms of silicon (contact pad) usage. Up to a few thousand supposedly identical devices can easily be packed and accessed in an addressable array. With fast functional testers or dedicated PC-card data acquisition systems such device populations can be measured relatively fast. Different addressing approaches for array test structures were reported in the references listed above. These range from full CMOS X- and Y-decoders, via multiplexers and shift-registers (sometimes mixed with a numbers of direct row or column pads) down to direct contact pad access of rows and columns and accessing the individual devices using the switch matrix of a parametric tester or through multiplexer PC cards. There appears to be no consensus as to which technique is the best. The approach is apparently determined by the combination of the preference and background of the person driving the project and the manpower and capital investment budgets, or available test infra structure.

The key factor for properly characterising parametric fluctuations using on-chip addressable test structures is that is must be assured that the terminals of the DUT's can be accessed while avoiding that the measurement results are affected by the switch electronics. Applying four-wire (Kelvin-sensing) techniques is inevitable to circumvent the impact of the additional series resistances of the access electronics [Blae88, Saya90, Port98, Shim03, Leff03,Einf04]. Without such precautions, addressable arrays can only be used for very low current measurements.
A more recent point of concern is to assure that junction and/or gate leakage currents of the switch transistors and address electronics do not affect the measurements [Leff03].

Disadvantages of array test structures

Apart from the dedicated skills and substantial manpower commitments that go into the design and layout of the access electronics, the following drawbacks of addressable arrays for characterising mismatch kept us from following this approach.

- Additional parametric analysis. With addressable arrays it is generally more difficult, or even impossible, to access individual components for further analysis with standard parametric measurement systems. When a mismatch measurement yields unexpected results, additional measurements on the DUT's often provide supplementary insights. Such additional measurements can range from supplementary DC I-V measurements to assess additional device parameters and leakages, to low-frequency C-V measurements.
- Layout homogeneity. Even though array test structures may show closer resemblance to realistic integrated circuits, it proves difficult to assure 'global identicalness' across an entire matrix. Several times, it was reported that the outer rows and columns of a matrix had to be skipped due to 'surroundings related' effects [Pava94, Niew97, Port98]. Placing extra dummy rows of devices around testable devices is hence obligatory for array based mismatch evaluation.
- Spatial parametric gradients. When large matrices are used (say total area more than 1x1 mm^2), the spatial parametric variations across the matrix cannot always be neglected according to some publications. This is no fundamental limitation, since the device evaluation can be done on a 'neighbour-to-neighbour' basis [Port98, Quar03] rather than on treating the entire matrix as a single fluctuating population. This can also be seen as an advantage because this may provide additional insights into the various components that contribute to the observed parametric fluctuations.
- Limited space for devices. Array test structure designs are usually based on standard address logic and interconnect pitches. Moreover, they are generally planned for a limited variety of test devices to be placed in the matrix. Consequently, the allocated space for test devices is usually rather limited as they are supposed to fit in to a standard pitch to facilitate (automate) the layout of the complete test module. This usually implies quite severe limits for the dimensions (area) of the devices that can be tested. Not only does this impede characterising devices with extreme aspect ratios, but this also limits the possibilities to experiment with the surrounding environment of the devices under test.
- Full circuit functionality**.** A traditional disadvantage that is often quoted against using addressable arrays for PCM and PEM measurements, is the compulsory full functionality of the process. This means that whenever there is a serious technology problem (say bad contacts or via's at a certain level), the address logic may prove to be malfunctioning.

Consequently, this would prohibit all parametric measurements and hence may make it impossible to assess the technological problem. This argument is not relevant for mismatch characterisation as one can argue that when the process is so immature that such elementary yield problems still hamper the process, one may not be (or at least less) interested in the mismatch fluctuation performance. Nevertheless, for more fundamental process architecture experiments, it is a painful conclusion when an interesting front-end process experiment after months of processing proves immeasurable due to a failing backend step. Keeping front-end related test structures simple and measurable after first metal processing is a 'good-practice' test structure layout guideline (see section 2.6) that is more difficult to adhere to when using the more complex addressable array approaches.

- Additional hardware. Measuring array test structures with high precision DC parametric testers usually requires additional (albeit low accuracy) sources and matrix pathways for driving the address logic, and selecting the appropriate device.
- Test time. A disadvantage of using high precision DC parametric testers for measuring array structures is that they may prove dramatically slow. Test times for standard parametric tests typically run of the order of seconds per parameter in high precision testers. This may add up to test times of up to several hours for measuring one single array (as has been 'admitted' in conference discussions and private correspondence). The most fundamental problem with such long measurement times is that it is practically impossible to maintain the temperature drift of the wafer and the measurement lab small enough to avoid that these drifts affect the mismatch results, particularly for large devices.
- Measurement hardware accuracy. A final limitation to keep in mind when designing array test structures is given by the (in)accuracy of measurement system when a fast circuit tester is used. The speed of such testers (tens of microseconds per test) is achieved at the expense of delivering significantly less accurate measurements compared to DC parametric testers. Typical specs for circuit testers and PC data acquisition cards based systems will be of the order of 0.1 to 1% for current force and measurements and 2 to 10 mV for voltage forcing and measurements. These are a factor 10 to 1000 above the typical resolution (and accuracy) of high precision DC parametric testers. This limited accuracy does not have to put off the use of functional testers for parametric fluctuation studies all together, as long as populations are investigated with relatively large fluctuations. This merely prohibits characterisation of large area devices, but may still yield useful results for small devices and/or poor processes.

The advantage: Outlier characterisation and statistical uncertainty

The (single) undisputable advantage of testing large populations through device arrays is the possibility to detect and characterise outliers, or tails in the statistical distributions.
It should be realised however, that in this context one is not merely talking about testing up to a thousand devices compared to the up to 100 pairs that are generally measured using conventional matched pair structures. One would need 4 to 5 orders of magnitude larger population sizes to characterise outlier statistics. This prohibits the use of high precision parametric test systems. In fact, the same argument holds when one wants to use array structures to reduce the inevitable uncertainty of statistical estimators considerably. Elementary statistics theory learns that the statistical uncertainty reduces with the square root of the population size. This implies that to go from a statistical uncertainty of about 10 to 20% for population sizes of up to 100 samples, one would have to bring the population size to the order of 10.000 devices to bring the uncertainty below 1%.

Conclusion

The trade-off between the array test structures and single pair approaches is basically brought back to two points, namely test chip area consumption (and measurements time) versus characterisation flexibility (and measurement accuracy). For this thesis, the single pair approach was always used. The larger design flexibility, quicker realisation and possibilities to do more extensive device measurements, also on very large matched devices, were the main arguments for this choice. The resulting limited population sizes (statistical uncertainties) never proved a problem Test chip area constraints could usually be overcome by either reducing the number of different pairs (being less greedy), or bumming available space on MPW's in return for free mismatch analysis results. Measurement and analysis time always is a limitation, no matter which test structure philosophy is used. Two days of test chip design can easily result in two months of measurements and two years of trying to understand what it all means.

2.4 Contact pad considerations for matched pair test structures

One of the most prominent features of test chips is that they consist for the most part of contact pads (figure 2.8). Such pads are intended for landing the probe needles on the metal patterns of the wafer and thus enable the contacts between the measurement equipment and the test structure. Due to the physical size and the mechanical position controllability of such probes (needles), contact pads must be made relatively large, typically of the order of 80 to 100 μm squared. This implies that contact pads are orders of magnitude larger than most of the actual structures and devices that are to be tested. Note that contact pads, the term used in this thesis, are usually called bond pads, even though most test structures are in fact hardly ever packaged and contacted using bond wires as is the case for IC product chips.

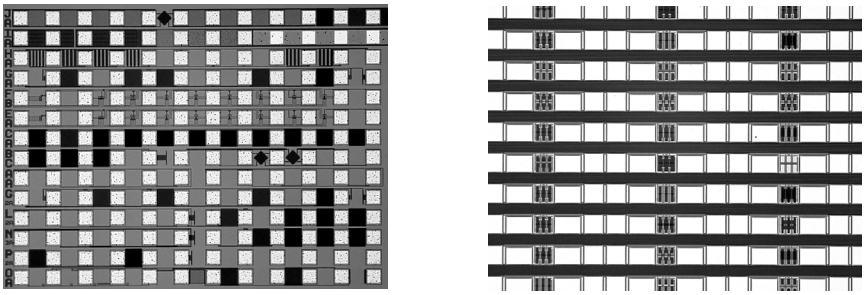

Figure 2.8 Test structures are mainly contact pads; Left: collection of 14 (1x12) pad frame (general PCM modules; Right: 30 matched pairs in scribe line configuration.

Despite their prominence and hence importance, contact pads generally do not receive much attention from test chip designers. In fact, pads are often merely treated as a nuisance: there are always too few of them to fulfil all test structure wishes, meaning that they are too large, or they prove hard to probe, implying that they are too small (see figure 2.12). The choice of the contact pad layout is usually dictated by availability of the (company or organisation standard) fixed probe-card. In the matched pair test structure literature, this situation is not different. One of the interesting challenges of mismatch characterisation is however, that one is faced with much smaller parametric effects than in ordinary (PCM and PEM) parametric measurements. In this context, even the utilization, placement and size of the contact pads may affect the measured results. Hence, this section summarizes some useful considerations about contact pads for matched pair test structures.

Effects of probe to pad resistance on matching measurements

Probably the most important contact pads related consideration for matched pair characterisation lies in the possible sensitivity of mismatch measurements for probe-needle-to-contact-pad resistance fluctuations. Depending on variables like contact pad material (Cu, Al, with or without TiN anti-reflection-coating layer), needle material, condition of the probe needles, how many times the pads are probed, contamination of the wafer surface (or needles), needle pressure, etc. significant variation of the resistance between the probe needles and the device under test can be encountered. Note for instance in figure 2.9 how much contact pads must endure during multiple characterisation sessions. Probing resistance specs for well maintained and clean needles usually read something of the order of 0.2 to 0.4 Ω. A typical rule of thumb number for the standard deviation of the probe to pad resistance variation is however something of the order of 0.5 to 1 Ω.

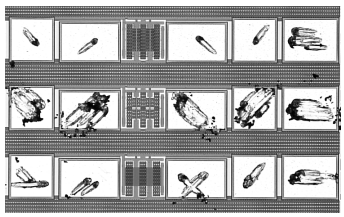

Figure 2.9 Contact pads of matched pair test structure must sometimes endure quite a lot.

Figure 2.10 gives an example of a probe to pad resistance distribution as measured by placing standard tungsten probe needles (Cascade-Microtech DCP-100) on adjacent contact pads, connected via several low-Ohmic metal lines. Whereas in this example the actual on-chip resistance (a metal bridge) between the pads was estimated to be less than 0.05 Ω, the resistance as measured through the needles varied between 0.75 and about 2.5 Ω, with a non-negligible number of high side outliers up to as much as 6 Ω. Such outliers are probably caused by oxidised or otherwise contaminated (aluminium) pads or particles on the wafer.
Compared to wafer fabrication facilities, (non-clean room) R&D electrical characterisation labs are often rather 'dusty'. This generally means that wafers that have been measured a number of times and handled with typical characterisation tweezers (the engineer's hands) are always covered with a substantial number of particles and small hairs. Some of these get picked-up by the probe needles and can hence hamper the contact between the probe needle and the pads,

causing higher contact resistances. The result depicted in figure 2.10 should be seen as a typical example of what kind of resistance values can be expected. This means that one should better be prepared to cope with these kinds of fluctuations, especially in high precision mismatch measurements.

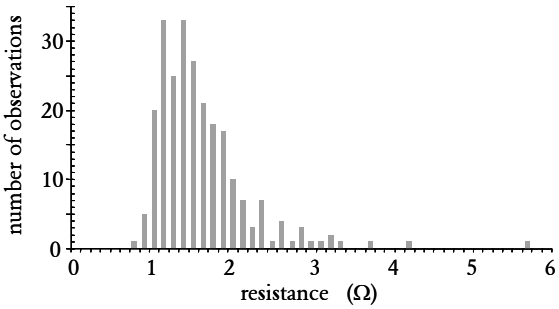

Figure 2.10 Example of a probe-to-pad contact resistance assessment.

Why low probe to pad contact resistance fluctuations can be particularly important for mismatch measurements is exemplified through the following example for mismatch measurements on bipolar junction transistor pairs. A typical A-factor for the matching of the collector current of poly-emitter NPN BJT's should be of the order of 2%μm. Measuring the mismatch of a transistor with an emitter area of 2x2 μm^2 (good transistors for mixed-signal applications; relatively large; aiming for small mismatch) hence would yield a collector current mismatch standard deviation of about 1%. A 1% collector current mismatch translates to an equivalent V_{be} mismatch of about 260 μV at room temperature. emitter probe-to-pad resistance variations would contribute to apparent V_{be} variations ($\Delta V_{be} = I_e \times \Delta R_p$). If one allows for a contribution of not more than 10% of the observed mismatch standard deviation to be associated with the probe-to-pad contact resistance variations, this implies that the maximum current in this transistor measurement would end up at no more than 26 μA when the probe-to-pad resistance variation is 1 Ω. This is well inside the operation region of interest for this type of devices. Measuring even larger transistors (e.g. for A-factor determination) with lower mismatch and larger currents (at the same V_{be}) becomes even harder if no precautions are taken to reduce the impact of the probe-to-pad resistance variation.

There are several well-known solutions to prevent that probe-to-pad resistance variations deteriorate the measurement accuracy. Four-wire (Kelvin) measurements with remote (on pad) sensing, using extra pads, or double needles are common measures in the field of high precision measurements. Whereas these types of Kelvin measurements are done routinely in many standard process control test structures (e.g. for contact resistance and low-ohmic metal layer resistance measurements), such measures are hardly ever applied for BJT and MOSFET measurements.

Sharing contact pads

Sharing of contact pads amongst test devices is a technique that is often utilised to diminish the number of required pads on a test chip. For matched pair test structures sharing of pads may seem particularly attractive, since large numbers of devices are usually required for a full-scale mismatch characterisation. Some schematic examples of MOSFET and BJT matched pair test structure modules are depicted in figure 2.11. The frequently used approach of sharing the source as well as the gate pads in MOSFET test modules (CS&CG) is shown in the top 2x9 pad frame module. The bottom part of figure 2.11 represents a Common Emitter & Common Collector layout (CE&CC) for BJT mismatch characterisation (see also figure 2.12).

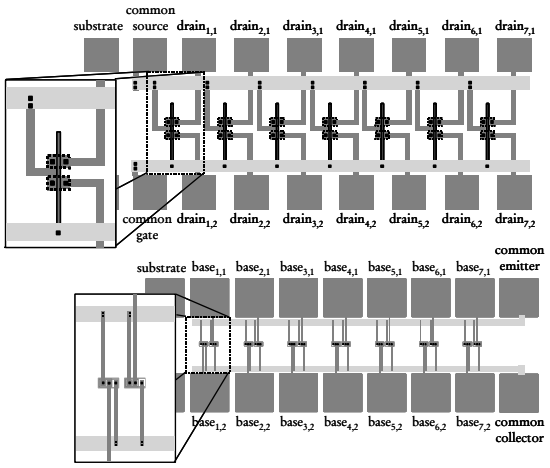

Figure 2.11 Examples of 2xN pad frame modules with matched pairs. CS&CG MOSFET pairs (top) and CE&CC BJT pairs (bottom).

Another, and in the context of this thesis more relevant reason for sharing pads (device terminals) in mismatch test structures is based on circumventing limitations of the used measurement instrumentation. Using the same pad for measuring two devices means -by definition- that the measurement hardware for biasing and/or measuring is identical for the two devices. By sharing pads, the impact of possible differences caused by needles, cables, switching matrix relays and meter and source offsets is mitigated. Hence, the measurement 'error' is equal for both devices of the pair, implying that the mismatch observation is (to first order) not affected. The Common Emitter & Common Collector matched pair test structure approach for bipolar transistors as depicted in figure 2.11 (bottom), first introduced in [Tuin94] is an example of this philosophy. Bipolar transistors generally match quite well, particularly when large emitter area pairs are used. As the collector, emitter and base currents scale linearly with the device (emitter) area, it becomes practically inevitable that large area pairs are to be measured at relatively high terminal currents (of the order of hundreds of micro-Amps to milli-Amps). With such current levels, while looking at V_{be} mismatch levels of tens to hundreds of microvolts, the impact of the probe to pad resistance and hence voltage drop fluctuation may become substantial. By sharing the high current paths (pads), the impact of such voltage drops becomes practically negligible for the mismatch measurement on the pair.

The disadvantages of sharing pads amongst multiple pairs, such as in figure 2.11 are associated with reduced characterisation flexibility and enhanced susceptibility for device leakages. For instance, sharing the gate terminal for a pair implies that it becomes impossible to characterise gate current mismatch. Moreover, using a Common Gate and Common Source connections as in figure 2.11 (top), implies that the Gate-to-Source current of all transistors in the module always flows in the Source current terminal. With the extremely thin gate dielectrics (< 2 nm) as encountered in contemporary CMOS technologies, this proves a nuisance, particularly when large transistors are combined with small transistors in one module. Comparable arguments hold for the BJT mismatch modules as depicted in figure 2.11 (bottom): when one of the, large emitter area transistors in the 2xN pad frame module has an excessive Emitter-Collector leakage, all transistors (pairs) of the module are useless. This latter disadvantage is circumvented in single pair CE&CC matched pair (scribe line) layouts as discussed later in this chapter.

Size of contact pads

The typical size for contact pads for regular (needle) probing is of the order of 80 x 80 μm^2 with a centre-pad pitch of 120 to 200 μm. For most DC parametric measurements on probe stations using fixed probe cards or micro-positioners this proves a good trade-off between probe reliability and user convenience [Tuto9x]. The choice of the pads is usually determined by the (company) standards (pad frames and probe cards) for a particular test chip or process family. As mentioned before, contact pads are the major silicon area 'consumers' on test structure chips and one is constantly tempted to limit this waste by reducing the size of the pads. From a mismatch characterisation standpoint however, there are several reasons for NOT adhering to standard pad frames and definitely reducing the size of the pads. The following arguments for choosing non-standard pad sizes are worth considering.

- Larger pads are much easier to probe, even with damaged ('hockey-stick') needles, worn-out positioner adjustment turning screws, poor (or poorly aligned) probe cards (see figure 2.12).
- Needles can be aligned and placed with lower microscope magnification when the pads are larger. This allows for a better overview over the entire test structure module and its surroundings, making it substantially easier to locate a particular test structure on the wafer.

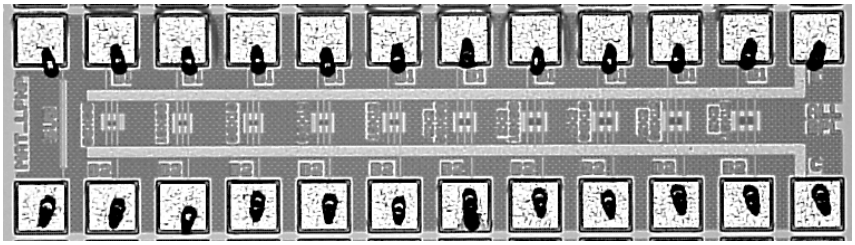

Figure 2.12 Example of (poor) probe-card needle imprints.

- Larger pads can be probed more often. If several landings are to be made on a particular pad, for instance for re-measuring or experimenting with alternative methods or biases, the aluminium is scratched off the pads (figure 2.9). With larger pad, needles can be repositioned a little bit (10 to 20 μm) to land on a 'fresh' part of the pad.
- Larger distances between the pads (e.g. pad pitches of 200 to 250 μm) also make life (work) considerably easier when working with manual manipulators. Guarded (coax) needles can pose problems when the pads are too close together as the shields of needles that are to be placed on adjacent pads touch. This is particularly cumbersome when needles have to be fitted out with ferrite beads to suppress high frequency oscillations (mainly for BJT's).
  A larger pad pitch is unavoidable when so-called Kelvin-probes are to be used. These are probe tips that in fact consist of two separate needles that must be placed on one pad (typical needle distance of 25 to 50 μm). These needles are used for four-wire resistor measurements or on-pad sensing, to assure precise voltage levels on the chip, even at higher current levels (1 to 500 mA) where the Ohmic voltage drop from needle to pad cannot be neglected. However, pad pitches of as much as 300 to 500 μm (may be required to have sufficient space to place such Kelvin probes. The required space depends on the number of Kelvin probes and the exact position and orientation of the device pair terminals.
- Finally, there is one point that ties in more specifically with the work discussed in the following chapter of this thesis on mismatch measurement methods. In several studies [Tuin98, Tuinh00a], we demonstrated the usefulness of monitoring the offset difference of two voltage sources during the matching measurements. In these experiments, this was realised by placing extra needles on the base pads for BJT's [Tuin98] or drain pads for MOSFET's [Tuinh00a]. These extra needles were attached to a differential microvolt meter, hence enabling compensation of voltage source differences that would have been interpreted as systematic mismatches. This proved doable but sometimes somewhat challenging for 80 μm pads, whereas this obviously proves significantly easier with larger (120 - 175 μm) pads (figure 2.13).

In the example shown in figure 2.13, the 'luxury' to be able to adjust the design of the contact pads for a scribe line mismatch characterisation module was exploited to increase the base pads size to 90x125 μm^2 (from the standard emitter and collector pad size of 80x80 μm^2. The base pads were also placed 'on the outside' to provide more 'manoeuvring space' for the two needles that had to be placed on each pad. An alternative solution to this hardware source offset problem is obviously to provide additional sense pads for each matched pair.

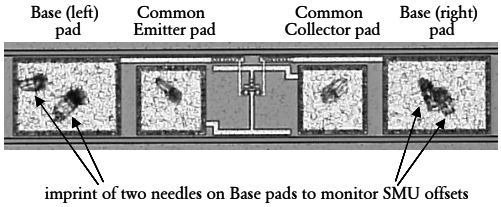

Figure 2.13 Single CE&CC matched NPN BJT scribe line pair with enlarged base pads to provide space for two needles on one pad.

DC device characterisation always is a challenge as well as a joy. However, this challenge does not always depend solely on the underlying device physics and technology. The quality of the probe station can contribute significantly to the enjoyment (or frustration). Probe stations can range from brand new top-of-the-line probers with good manipulators and sharp needles, to shaky, written-off stations, often with less than optimal microscopes and maltreated by inexperienced users. Under such diversity, we have concluded that larger contact pads, designed with the measurements in mind, are well worth the extra area and design time!

2.5 Matched pair test structure selection

A common constraint that is felt in the field of PMF characterisation and practically any other semiconductor device characterisation or modelling activity is that there always is too little silicon space available to test all demands and ideas. To make things worse, as the field of mismatch is littered with many historic horror stories, one is tempted to add as many test structure alternatives as possible (just in case). The problem with systematic mismatch effects and layout alternatives is that a sheer infinite number of implementations can be identified as possibly interesting for analogue circuits layout. Therefore, it is inevitable to restrict the number of test structures for mismatch characterisation. Based on accumulated experiences, many successful as well as disappointing experiments, discussions with other experts in the field, and some literature results, this section summarises and prioritises matched pair test structures alternatives.

Matched pair geometry selection

The starting point of any mismatch characterisation project should always be proper assessment of the parametric mismatch fluctuation area-scaling factor, as this benchmarks the microscopic device architecture fluctuations. Moreover, the A-factors are often also used for circuit design purposes. If one would have an infinite faith in the 'A-factor model', in principle only one transistor pair dimension would be sufficient to determine the A-factor. However, as discussed in chapter 1, there are several assumptions underlying the A-factor modelling approach that are not necessarily always met. Moreover, several published matching studies demonstrated that a single $1/\sqrt{(\text{area})}$ relationship does not always provide the optimum matching performance description over the entire geometry range. This makes sense, as some mismatch mechanisms are not associated with the bulk volume property fluctuations of the device, but rather perimeter related physical phenomena. Hence, in practice one must always select a range of transistor pair geometries for inclusion on a PEM. The following sections give examples of typical transistor pair geometries and the reasoning underlying the selections.

Geometry selection for MOSFET matched pairs

As a typical example of the geometries that are useful for MOSFET mismatch characterisation, a set of 22 pairs as represented in table 2.1 is proposed. This particular example is based on a 0.25 μm CMOS type of technology, but the same approach can be applied for other technology generations, primarily by adjusting the minimum quoted dimensions, or by multiplying all given dimensions with the design rule scaling factor.

	W=40	W=10	W=4	W=2	W=1	W=0.5	W=0.25
L=40	X[1,3,4,7]						
L=10		X[1,2,3,4,5,7,8a]		X[3,4,5,8a]	X[3,5]	X[5]	X[5,6,8b]
L=4		X[1,3,4,5,8a]	X[3,7,8a]				X[6]
L=2		X[3,5,8a]		X[3,7,8a]			
L=1		X[1,3,5]			X[7,9]		
L=0.5		X[1,3,5]				X[7]	
L=0.25		X[5,6,8b]	X[6]	X[1,9]	X[1]	X[1]	X[1,2,7,8b,9]
L=0.2		X[5]					

Table 2.1 Example of geometry selection for MOSFET matched pairs in a 0.25 μm CMOS technology. Columns: equal Width; Rows: equal Length. Superscripts refer to remarks in the text below.

Remarks

1. As the starting point for matching characterisation is usually based on the 1/√(area) relationship, the initial objective of the area selection is to spread out the geometries more or less equidistantly on a 1/√(area) scale.

2. For proper estimation of an A-factor it is important to cover a wide range of areas, which means spreading out the device areas from the minimum transistor area W_{min} x L_{min} to an 'infinite transistor' of the technology, e.g. a 10 x 10 μm^2.

3. For matching characterisation for analogue (mixed-signal) applications, extra emphasise should be placed on devices with 'larger than minimum' dimensions. In the analogue circuit design field it is quite common to used larger than minimum dimensions as these give higher output resistance (gain) and are less susceptible to mismatch fluctuations and spread (short channel effects). A typical high precision analogue circuit block will not use transistor lengths below two times the minimum channel length. Moreover, for determination and interpretation of the mismatch fluctuation A-factors, it proves worthwhile to have several device geometries available that are much larger than the size and the correlation distance of the microscopic physical disturbances (e.g. poly-Si grain size fluctuations). This explains the relatively strong presence in the table in the 1 to 10 μm range.

4. Analogue circuit designers will not hesitate to use 'real biggies' for their applications when they need the maximum possible matching performance or very high output resistances. Transistors with areas of a few hundred (!) square microns (e.g. W/L of 10/40 to 2/100 μm/μm)

are not unlikely. Apart from offering the possibility to provide circuit designers with the optimum matching performance information, such transistors are both useful as well as challenging from a characterisation perspective. Their use lies in the possibility to investigate possible 'saturation' effects: for large dimensions the mismatch standard deviations may not approach zero as is sometimes believed. The challenge of measuring large transistors obviously lies in their (hopefully very good) matching. This may mean that the measurement hardware and algorithms should be capable of resolving mismatch with sub 10 μV or sub 100 ppm measurement accuracy!

5. For modelling purposes as well as for identification of perimeter-related mismatch effects, both a 'length series' (constant width, varying length) as well as a 'width series' (constant length, varying width) should be available.

6. From a parametric mismatch fluctuation assessment standpoint, it proves very useful to provide several combinations of pairs with equal area but with different W/L ratios (e.g. W/L = 1/1 & 4/0.25 & 0.25/4, or 1/10 & 10/1 in table 2.1). Such combinations provide immediate and easily interpretable signals about the validity of the $1/\sqrt{(\text{area})}$ model.

7. Several authors in the matching literature have focussed their test structure selection predominantly (if not solely) on pairs (or arrays) of square devices [Pava94, Elzi96]. Although there is no fundamental reason against this practice, there obviously is a significant drawback of this choice, in the sense that it becomes impossible to separate possible width and length contributions and hence to evaluate possible technological causes for mismatch mechanisms associated with the perimeters. An advantage of using square (MOSFET or resistor) pairs only is, in the fact that some of the measurement algorithms may be easier and more accurate.
To be more precise: As the actual I-V measurements are all done in the same current meter and source ranges for the various device pairs, there is less uncertainty in the interpretation of measurement results, as one does not have to take the different offset levels and noise contributions of meters and sources into account. This may be particularly useful in a (PCM) production test environment where the noise and disturbance levels are generally higher, especially in the lower current meter ranges.

8. Most of the geometries in table 2.1 are intended for a full scale matching characterisation and modelling. Due to the rather lengthy measurement and evaluation times one would normally limit the set of testable device pairs to some four or five geometries for routine assessments of the A-factor (8^a) or for comparing different process splits. These can then be augmented by a couple of minimum size pairs for assessment of high performance digital circuits yield hazards (8^b) and as a warning against possible excessive small device effects.

9. For routine process control (PCM) measurements available test times are usually very limited,

while most high volume parametric testers and/or their measurement algorithm provide lower measurement accuracy / repeatability compared to dedicated high precision measurement systems. Therefore, it is better to stick to reasonably small devices in PCM's since these devices exhibit higher stochastic parametric fluctuations. The 1x1 or 2x0.5 pairs will generally be fairly convenient meaning that they are not too small to be excessively affected by short an/or narrow channel effects and still yield fluctuations in the millivolts and/or percents ranges that are within the measurement capabilities of most parametric testers. The W_{min}/L_{min} device pair generally exhibits the largest fluctuations and is hence easiest to characterise while it is most important for high performance digital circuits.

Geometry selection for BJT matched pairs.

For bipolar junction transistor matching characterisation (table 2.2), one can follow the same approach as discussed above for MOSFET's. For BJT's the effective emitter area $W_e x L_e$ forms the major design / layout control handle for parametric mismatch fluctuations. However, it generally makes no sense to use transistors in circuits with a larger W than L (unnecessary large base resistance). Hence, the filling of the W & L matrix is more focused on the lower left corner. A single 'odd' transistor (e.g. the LxW = 1x8 in table 2.2) may still be useful for characterisation of the perimeter effects.

	L=32	L=8	L=4	L=2	L=1	L=0.5
W=32	X					
W=8		X			X	
W=4		X	X			
W=2		X		X		
W=1		X	X		X	
W=0.5	X	X		X		X

Table 2.2 Example of emitter dimension selection for poly emitter NPN BJT matched pairs in a 0.5 μm BiCMOS technology.

Some of the same geometry choices can be observed in this table as discussed for the MOSFET devices matrix of table 2.1. Having some transistors with the same active area, albeit with different W and L combinations to evaluate possible edge and or perimeter related PMF effects is again important. In this example, the areas of some pairs are chosen such that the ratios of

the square-roots of their area forms some integer number (assume that the dimensions given above are effective dimensions). This facilitates the initial evaluation. Take for instance the 2x2 and the 0.5x0.5 pairs in table 2.2. If the 1/√area relation holds, one should see a factor of four lower mismatch fluctuation standard deviation for the 2x2 pairs, compared to the one of the 0.5x0.5 pairs. This may seem trivial, but it are such easily recognisable anchor points that always form the start of every matching characterisation study. Table 2.2 demonstrates that by choosing some 14 geometries the relevant W and L space can be covered quite adequately. The over 900 μm^2 device pair should prove a real challenge to characterise as its matching should be close to the measurement capabilities of -even the best- characterisation system. The same arguments as in the previous section apply when it comes to selecting sub-groups for standard characterisations or PCM measurements.

In bipolar transistors, there usually are several additional degrees of freedom in the layout as compared to common digital CMOS MOSFET's. Variations of the shape and number of base contacts, number and position of collector contacts, emitter constructions (walled or non-walled, multi-finger emitters) are quite common. Each of these layout approaches may yield a different transistor performance. In the circuit layout packages, devices are generally available as parameterised library elements. This implies that some sort of matching characterisation should be available for each of these standard types. Although most of such layout variations will quite likely not have a major impact on the matching performance, this is not an assumption that can always go without verification. On the other hand, it is practically impossible to characterise the entire W&L matrix of each layout style! Hence a careful selection must be made as to which will be the most likely types for the (analogue) circuit designers (probably at least the double base, double collector, single emitter type), followed by some favourites of the other design types to assess matching performance differences of the alternative layouts. An additional consideration for the geometry selection for BTJs is that larger emitter area BJT's are generally laid out with multiple parallel emitters of minimum width, and that lateral PNP transistors are often constructed using arrays of parallel unit transistor cells rather that scaling one of the dimensional parameters. Such parallel layouts may require special attention if special layout constructions are used to connect the parallel components. To first order, it is expected (and indeed reported) that matching scales with the inverse of the square-root of the number of parallel emitter fingers or unit cells [Linn98, Tuin98].

Priority	Type of Pair	Purpose	Remarks
1.	Large Area	Area scaling factors	Devices much larger than microscopic disturbances (in the range of 2x2 to 10x10 um^2)
2.	Minimum Area	Worst-case fluctuations	Device fluctuations for high performance digital circuits
3.	Analogue	Mixed-Signal (analogue) applications	Limit small dimension effects (e.g. short channel effect) 2-3 x minimum dimension
4.	Folded devices	Layout specific effect (2 directions?)	Used in many products where large effective area is required
5.	Biggies	Mixed-Signal (analogue) applications	Best matching devices; high impedance lowest fluctuations: hard to measure!
6.	Dense layout area	Evaluate litho proximity effects	Create dense surroundings (only connect two devices); compare to 1 and 2 (sparse layout)
7.	Orientation	Mismatch differences due to different device orientations.	Not a true matching effect, but relevant for circuit designers (combine with QUAD structures)
8.	Metal surroundings	Required distance of (stress) symmetry	Count on mechanical stress effects that have impact over tens of microns
9.	Distance effect	Distance effect /spatial parametric gradients	Not a real stochastic matching effect, but still relevant for many circuit designers
10.	Antenna effects	Antenna rules verification	Evaluate impact of charging due to plasma etching
11.	Gate protection	ESD protection	Check ESD effectiveness of protection
12.	Packageable modules	Effects of packaging on mismatch	Only makes sense if chip size, package, mounting, bonding, circuit density and power dissipation are comparable to product.
13.	Product specific	Select important pair for product e.g. comparator or sense amp input pair	Should include adjacent layout features as encountered in product
14.	RF devices	Verify matching at RF frequencies	Need GSG probe pad frames
15.	Parallel & QUADs	Compare large area single device with device built from minimum size unit cells	Used in many products where large effective area is required (a.o. switched caps, lateral PNP BJT's for bias current sources); dense surroundings but connect all devices (combine with 1, 4 and 5.)
16.	Topography in surroundings	required distance of topography asymmetry	Count on resist and developer flow effects that have impact over tens of microns
17.	Metal coverage	Effects of passivation and mechanical strain	Requires symmetrical as well as asymmetrical coverage (long devices preferred)
18.	Offset pairs	Intentional systematic mismatch	For measurement system and algorithm testing [Tuinh00a]

Table 2.3 A prioritised list of matched pair test structures

Alternative matched pair test structures

Apart from parametric mismatch, fluctuations as discussed in the previous section, many other, often unexpected and regularly underestimated effects can result in statistically significant systematic mismatches. Examples of mismatch causes that were reported as yield limiters are related to so-called environmental or adjacent layout effects [Greg92, Perg98, Tuinh03a]. These adjacent layout effects are generally associated with lithography (printing, developing, etching) or local mechanical stress asymmetries. Furthermore, there is a class of mismatch causes that fall into the 'what if we don't stick to the rules' category. Frequently, analogue circuit layout engineers are confronted with a design guideline that proves impractical or impossible to adhere to for a particular layout implementation. Examples of such cases are large arrays that prove impossible to wire-up when metal lines are prohibited over or near high precision matched elements, or when matched building blocks can only be realised using components that are not identical in terms of layout or orientation. Although it proves practically impossible to characterise all such cases extensively, it may be useful to add some dedicated 'what if' test structure to the matched pairs field. They can provide results that may help to dissuade circuit layout artists from not sticking to the rules.

Table 2.3 contains a prioritised list of matched pair test structures. The priority is based on a combination of experience of successful experiments and (product related) disasters. Obviously, this list can (and will) change for other types of product lines and as new product problems surface. Hence, the list given in table 2.3 should primarily be interpreted as an idea 'checklist'.

2.6 Guidelines for matched pair test structure realisation

This section discusses a comprehensive list of guidelines for the planning, definition and layout of matched pair test structures. This list is based on accumulated (good and bad) experience from comparing many different types of matched pair test structures, from our own design experiences and many 'inherited' mismatch characterisation test structures from other Philips sites and fabs, in combination with discussions with experts from other companies and institutes in the world.

Mismatch characterisation project planning

Before any layout is made, it is always worthwhile to plan the overall approach of test structures and characterisation. The following set of guidelines form a kind of checklist that can be used during the planning stage.

- What is the goal of the study? The test structure (layout) is strongly related to the available test system and parameter extraction method as well as the required parameters and /or product related issues that are to be investigated.
- Keep it simple. Matched pair test structures and their accompanying measurement methods should be as simple as possible. This facilitates reaching the best measurement accuracy, as well as interpretation of mismatch results.
- Check contact pad frame possibilities.
  - When measurements are to be performed using the standard parametric test equipment, the pad frame should be compatible with standard PCM- or PEM-like probe-card configuration (2xN pad modules or scribe line 1xM test module).
  - For dedicated mismatch characterisation systems and/or when the mismatch measurement system is equipped with individual needle positioners, or dedicated probe cards can be used, extra degrees of freedom such as large pads and larger pad pitches can be exploited, resulting in considerable characterisation (accuracy) benefits (section 2.3).
- On-wafer measurements. Mismatch measurements should be executable 'on-wafer'. This is particularly important to allow separation of spatial parametric variations from stochastic parameter fluctuations. This information usually gets lost when packaged test structures are used.
- Know your measurement system. Assess the capabilities of the measurement system and the available parameter extraction algorithms: speed, accuracy and short-term repeatability, type of wafer prober, etc. all contribute to the decision whether a particular layout approach is feasible.

- Know your test structure. Can the test structures be measured with standard DC semiconductor test equipment (PCM tester, Parameter Analyser, etc.), equipped with a (semi-) automatic wafer probe station? Match the expected test structure performance with the short-term measurement repeatability capabilities of the measurement system.
  It makes no sense to measure the mismatch of very large devices when the measurement system cannot deliver the required accuracy.
- Know your measurement algorithm. The measurement algorithms should stay as close as possible to the standard algorithms as available for regular DC parametric process characterisation (same V_T definition!). This facilitates transfer of structures and methods to development groups and/or production sites. For high precision mismatch measurements (large components) however, it usually proves inevitable that measurement algorithms must be refined to achieve better short-term repeatability, generally at the expense of prolonged measurement times.
- Know alternative characterisation possibilities. Preferably, the test structure should be laid out such to enable additional parametric measurements on each of the elements that are used for mismatch characterisations. This facilitates interpretation of unexpected mismatch observations.
- Smaller is easier. Measuring the mismatch of smaller devices is easier as the mismatch fluctuations are generally larger, but the interpretation is often more complex as more (perimeter related) effects may become significant.
- Know the product requirements. Base the mismatch characterisation approach on the requirements for the target products of the technology. Always focus on mismatch fluctuation area scaling first as this benchmarks the technology, but beware of adjacent layout effects in many products. Note from the start that it is quite easy to design an infinite number of matched pair test structures, but that it is practically impossible to measure and analyse all results.
- Beware of statistics. Plan for populations of testable pairs of one particular geometry to count at least some 60 to 100 samples on each wafer. Should the chip-count on the wafer (wafer area / test chip area) fall below 60, it is advisable to place a second instance of the matched pair module on the reticle. Settle for fewer different pairs rather than ending up with a large number of types of matched pairs at a too small population size.

Layout guidelines

After planning the matched pair test structure approach, the concrete realisation and layout of the test structures should be executed with the following layout guidelines in mind.

- 'Painfully' assure a truly identical layout of both devices of the pair, including all contacts and connections. Only use translated copies of a previously defined library element to create the pair. Assure identical orientation: all currents in the devices must flow in the same direction.
- Place the matched devices at small distance. However, from a parametric gradient standpoint there is no need to use the minimum design rule distance! Any distance of 100 μm or less should be more than sufficient. Using minimum spacing can even be detrimental due to adjacent layout effects.
- Maintain consistency in the module layout. Different pairs (geometries, layout variants) should be placed in identical pad frames and connected using the same basic interconnect frame (see figure 2.14). Such consistency helps to avoid systematic mismatches and interpretation of unexpected results.

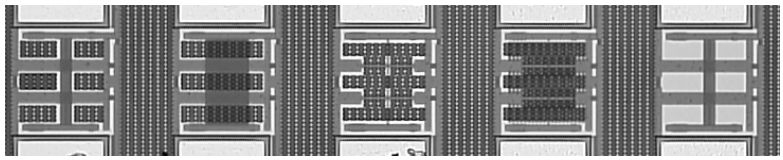

Figure 2.14 Five MOSFET matched pairs in 1xM modules (detail of figure 2.8-right) Note that an identical metal connection frame is used for all pairs.

- Plan to use only one metal layer for each matched pair test structures and their connections to the contact pads. This results in simpler structures, less prone to technology errors and with less unexpected mismatch hazards. Moreover, front-end related device architectural experiments can be measured earlier (after first metal). A simple circuit such as a matched pair (two transistors) should always be realisable using one interconnect layer. Well-dimensioned and placed front-end crossings in poly-Si are preferred over metal-1-to-metal-2 vias as the latter are more prone to mechanical stress and technological (yield) problems. Make sure that when crossings cannot be avoided, they are placed symmetrical with respect to both devices of the pair. If necessary, place a dummy crossing to improve symmetry.
- Avoid using Common pads unless required for better measurement accuracy. Common pads and the connections to the devices may give rise to undesired layout asymmetries and parasitic resistances.
- Use sense pads when large currents are required. For high precision mismatch studies and/or currents larger than 100 μA, add voltage sense (Kelvin) pads to mitigate impact of probe-to-pad contact resistance. When two needles or double-needle Kelvin probes are to be used on one pad, make pads larger and increase pad spacing (250 to 400 μm) to leave room for two separate probes. Place pads that are to be probed with two needles 'at the end' of the module to allow manoeuvring space for the positioners.
- Create identical connections between both devices of the pair and the measurement system.
  - Avoid resistance differences larger than 50 mΩ in the high current ($>$ 1 mA) connections as these may result in systematic mismatch observations.
  - Use double rail star layouts for the device terminals that are connected to a Common pad, since this assures both identical access resistances as well as symmetrical layout environments (see section 2.6).
- Never route metal lines or any other interconnect level over the matched elements as this may affect the physical and hence the electrical behaviour of (one of) the components.
- Litho effects.
  - Beware of the impact of litho proximity effects. Always create at least one comparison of a single pair in a empty field ($>$ 50 μm), in combination with the same pair in a dense array layout field (as in figures 1.6 and 2.14).
  - Avoid asymmetrical topography near one of the components as this may affect the lithography (in particular flow of photo-resist and developer). Also, beware of module identifiers in the near vicinity of the pair.

- Beware of gate protections. Although it is generally advisable to abide to design rules concerning processed induced charging (antenna effect) and ESD, there can be (seemingly minor) side effects, such as leaking protection diodes, which affect small mismatch observations. A useful test could be to add one matched pair design with protections and the same layout without protections. It should not be forgotten to maintain layout symmetry, also concerning the protection diodes and the contacts! This is unfortunately not always the case. During the common 'last minute' design rule check and chip finishing, 'forgotten' protections are sometimes carelessly added to the structure.
- Create strictly identical layout environments around matched components. Anticipate that, in the worst-case scenario, any asymmetry within at least 80 μm of one of the devices can result in statistically significant systematic mismatch observations [Tuinh04a].
  - Place the devices symmetrical with respect to all metal lines, such as Common connection rails, via's, crossings and contact pads.
  - Place single device dummies or complete dummy arrays next to / around the matched devices to create environmental symmetry. Single dummies prove sufficient against resist and developer flow effects [Haus02], but not against mechanical stress related asymmetries [Tuinh04a].
  - For ultra-critical applications (mismatch below 0.1%), extend the design patterns of all layers at least 80 μm distance from the matched devices.
  - Check the chemical-mechanical polishing (CMP) layer density rules. Design your own symmetrical metal (dummy) patterns up to the highest metal level. Beware that chip post-processing will generate dummy tiles of all CMP-ed layers.
- Avoid 'dubious' constructions. Any ambiguity in the design may give rise to doubts about the validity of the test structure when unexpected mismatch results are encountered. Layout inconsistencies and minor asymmetries may obscure the effect that is under investigation. In particular, one should be aware that the smallest layout asymmetry might result in statistically significant systematic mismatches for populations of large area devices. Due to their inherently low mismatch fluctuations, seemingly minor layout asymmetries are bound to show up as a sub-1% systematic mismatches in populations of large area pairs.
  - Avoid using minimum design rules in the connections (where possible). Over-dimension metal lines to reduce series resistance (fluctuations).
  - Avoid bends in the metal lines as much as possible. Place unavoidable bends as far away from the pair as possible.
  - Where crossing lines cannot be avoided, use at least more than four contacts or via's to reduce possible impact of (fluctuation of) parasitic resistances.

- Make life easier for tester operators.
  - Use the largest possible contact pads, extend the pad in 'unused' directions where possible.
  - Add a large module identification name or number in all major layers up to the highest metal layer (to avoid that the ID becomes indistinguishable by CMP dummy tiles). Do not place the identification right next to the pair, but rather besides the first or last pad of the module. Note that this ID is mainly intended for finding one's way around on a big test chip. As this is generally done using a wafer prober's microscope with relatively small magnification, a few large (> 40 μm) characters like 'MM1' are more useful than a complete x character module name including revision number (such as '$_{\text{most mismatch 1 rev c}}$'). The latter is no doubt better for administrative purposes and design flow quality control but generally unreadable once the wafer is on the wafer prober's chuck.
- Packaged structures.
  - Keep pairs well away from crystal edges, unless the required distance to the crystal edge is the subject of study.
  - Contrary to on-wafer measurements, packaged modules should definitely always be equipped with gate protection structures. A simple (minimum size) 'back-to- back' diode will suffice for most applications, as these chips generally do not have to go through the entire torturing cycle of a product chip. Beware though that packaged modules should always be handled with extra care.

2.7 Examples of matched pair test structures

This section discusses examples of matched pair test structure realisations. For BJT as well as for MOSFET pairs, some alternative layout approaches are presented. Comments are given on how the considerations as sketched in the previous section can be translated into mismatch characterisation test structures. It should be noted that several of the following examples are 'wrong' according to some of the guidelines discussed above. Such examples are added to exemplify layout errors that are regularly encountered in matched pair test structures. The discussion of matched pair test structure examples begins with a rather exhaustive overview of BJT matched pair test structures. As many of these remarks are quite similar for MOSFET matched pairs, these are discussed with somewhat less detail.

Naming convention

The matched pair test structures that are discussed in this section are classified according to their contact pad use. Hence, a particular MOSFET test structure will be referred to as a Common Source & Common Gate (CS&CG) structure if in the matched (MOSFET) pair both of the gates are connected to one pad, both Sources to another pad and, obviously, each of the Drains to a separate pad. An equivalent structure for a bipolar matched pair would be identified as a Common Emitter & Common Base (CE&CB) pair. This should not be confused with the naming convention for measurements of (single) bipolar transistors, where 'Common Emitter' or 'Common Base' means grounding the Emitter or the Base respectively during the measurements. Indeed, for most of the NPN BJT matching measurements as discussed in this thesis, Common Base measurements are done using a Common Emitter test structure.

Substrate contacts

All DC parametric measurements on active or passive devices must be executed with Substrates or Wells connected and biased appropriately; hence somewhere in each module a Substrate or Well connection must be provided. For simplicity, these contacts and their pads are left out of most figures in this chapter, but they should definitely never be skipped in any real test structure implementation.

Scale

It is not just important which terminals are connected (together) to a contact pad, but also the symmetry in the structure and the interconnect to the pads are important. In the following examples, all matched pair test structure layouts are therefore depicted including their pads. This implies that the schematic layouts are generally not drawn to scale.

BJT matched pair test structures

In all of the following examples, the BJT's are depicted as single base contact CBE style double poly NPN transistors as represented in figure 2.15.

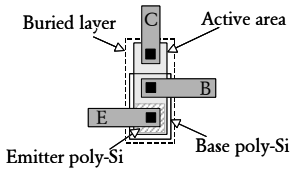

Figure 2.15 Schematic representation of the layout of a double poly NPN BJT that is used in all matched pair test structure examples.

CE&CB matched pair test structures

The simplest approach for collecting information on BJT mismatch is the based on the Common Emitter & Common Base type of matched pair test structures (figure 2.16). This structure can be measured using the well known 'long-tail-pair' current source biasing or any of the standard voltage biasing schemes in grounded Base or grounded Emitter configuration.

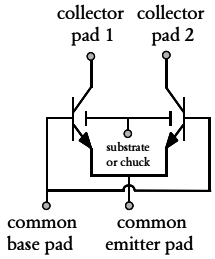

Figure 2.16 Circuit diagram of CE&CB pair.

The main advantage of this type of matched pairs is that they are easy to measure and interpret. The (relative) collector current mismatch can be measured at varying current density levels. If specifically requested by circuit designers, the collector current mismatch can easily be

converted to a V_{be} mismatch[†]. The main drawback of this matched pair test structure is that the individual base currents (and hence also the individual current gains) of the two transistors cannot be measured, which means that valuable information on the microscopic transistor architecture fluctuations (emitter construction) cannot be assessed. Nevertheless, this is the most commonly encountered BJT mismatch characterisation approach. It corresponds well with the use of NPN BJT pairs in many circuit applications (e.g. differential pairs in amplifiers or comparators, or in current mirrors).

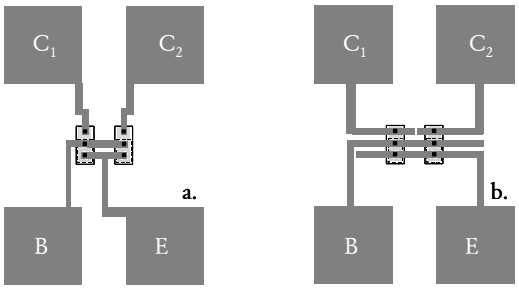

Figure 2.17 Two implementations of a CE&CB matched pair in a 2xN padframe.

When a CE&CB pair is placed in a 2xN pad frame, one could for instance end up with one of the implementations as depicted in figure 2.17. These particular layouts (at first glance) adhere to most of the design requirements as listed in section 2.5 above, and will probably yield acceptable mismatch measurement results. Nevertheless, if it comes to realising a truly symmetrical layout, both implementations suffer from asymmetries that should be avoided.

The main problem with the layout of figure 2.17a is the asymmetry due to local mechanical stress caused by the (base connection) metallisation. When there is a significant mechanical stress effect from one of the layers in the back-end, we might see a (systematic) mismatch. Obviously the extend of this impact depends on the fabrication process; not all processes suffer equally severe from back-end related stress. One of our recent studies on the impact of metal connections on mismatch demonstrated quite conclusively that such carelessly placed metal connections are indeed discernible at a level of a few tenths of a percent [Tuinh03a].

[†] 1% $\Delta I_C/I_C$ corresponds to 259 μV ΔV_{be} @ RT in the ideal part of the Gummel plot.

Although in the matched pair implementation of figure 2.17b this asymmetry is avoided, a more serious design error in this version should definitely not be neglected! The left transistor is not connected with the same (interconnect) emitter resistance to the Common contact pad as the right transistor. In most process and device characterisation test structures in PEM's and PCM's a parasitic resistance of less than one Ohm in the connections between devices and pads is generally not taken serious. Therefore, it is not unlikely that an (in terms of mismatch test structures) inexperienced test structure 'layouter' oversees the importance of such a parasitic resistance. Note however, that the metal connection between the two emitter contacts in this example is at least of the order of 5 squares of the used interconnect level. If one assumes a sheet resistance of 50 - 100 mΩ per square, this would yield an extra 0.25 - 0.5 Ω emitter resistance for the left transistor. If these transistors are measured at an emitter current of 1 mA, this layout-induced emitter resistance difference would translate to a (systematic) V_{be} error of 250 - 500 μV, or roughly a 1 - 2% systematic collector current mismatch! This could definitely be quite significant for a well matching BJT technology, particularly for larger emitter areas. Obviously, the layout of figure 2.17b requires another refinement through using a star-connection as for instance depicted in figure 2.18a, in which also some 'cosmetic' symmetry refinements were added to correct all metallisation induced stress asymmetries.
The absence of a star connection in the base connections (in figure 2.17 as well as in 2.18a), is normally spoken a much smaller problem, as base currents are typically two orders of magnitude smaller than the emitter currents.

However, also this possible source of systematic mismatch can be avoided by changing the pad allocation as for instance depicted in figure 2.18b, where also the symmetry of the total structure layout is further refined. This realisation includes a double rail star connection for both Common terminals. The metallisation pattern of this latter layout is quite suitable as (consistent) standard layout frame for other transistor geometries and adjacent layout experiments.

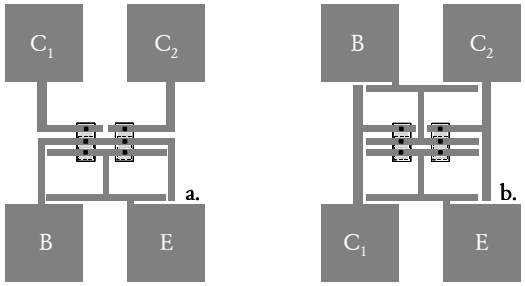

Figure 2.18 Improved layouts for CE&CB pairs.

When the matched pairs are to be characterised at low current levels, e.g. at 1 to 10 μA, which is a common current level for many high precision analogue circuits, it quite likely that all layouts from figures 2.17 and 2.18 will yield practically the same mismatch distributions so there may not seem too much to worry about. However, one should look at this from another perspective: Suppose one measures a certain population of matched pairs and the statistical characterization yields a median that deviates significantly from zero. In practice, this is not uncommon, but the problem is that this could have been by the statistical uncertainty (finite number of samples from the entire population, see next chapter of this thesis), or it could be due to a real physical offset such as an emitter size (reticle) offset. However, when one is confronted with layouts as in figure 2.17, one cannot but start wondering (worrying) whether the slightly asymmetric metal patterns near the pair or the overlooked star connections could also have caused this non-zero median. The lost time over such speculations and additional checks is much more expensive than the little extra layout time and discipline required to create a consistent, perfectly symmetrical star connected matched pair layout.

CE&CC matched pair test structures

A matched pair test structure layout approach for BJT's that was used quite extensively in the work underpinning this thesis, is formed by pairs of transistors that are laid out in a Common Emitter & Common Collector (CE&CC) configuration (figure 2.19.).

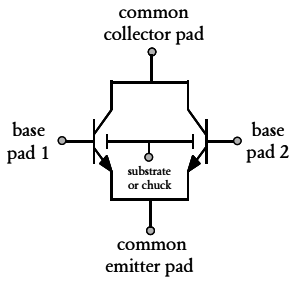

Figure 2.19 Circuit diagram of CE&CC pair.

The main advantage of the CE&CC configuration over the CE&CB is the possibility to measure the collector currents (sequentially) as well as the base currents of both transistors of the pair while keeping the pad count relatively low through saving a collector pad. A secondary advantage of the CE&CC configuration is that this approach assures that the collector currents are measured with the same current meter (no systematic due to different offsets between different meters in different SMU's). Voltage drops due to probe-needle to pad and other instrumentation interconnect resistance differences will neither have a different impact for the two transistors as the largest currents flow through the same path (pad, needle, cable).

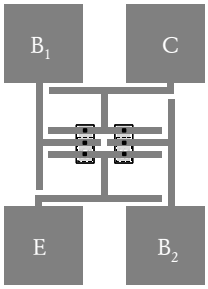

Figure 2.20 Layout implementation of a CE&CC pair in 2xN pad frame.

An implementation of the CE&CC structure is shown in figure 2.20. This layout again provides substantial design flexibility as the double rail layout (macro) can be used for pairs of different size and different spacing without having to worry about the exact interconnect line resistance. As long as the two transistors are placed symmetrical with respect to the central vertical bars, the emitter and collector resistances of both transistors of the pair will be identical. The extra metal lines provide additional (mechanical stress) symmetry in the module. This is also the reason why all metal lines are extended even though large parts of the lines do not carry any current. Note that the extra parasitic capacitances of these 'loose ends' are negligible in test structures compared to the total capacitance that is dominated by the pads.

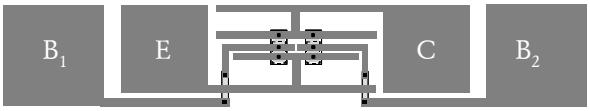

Figure 2.21 CE&CC pair in 1xM pad frame. The light grey parts in the base connections indicate crossings, one of which (to B_2) is a dummy to maintain symmetry.

The CE&CC matched pair test structure can also be realised in a 'scribe-line' 1xM pad frame layout configuration (figures 2.21 and 2.22). Note that the CE&CC pair implementation as depicted in figure 2.21 requires a crossing between the base connection and the emitter connection of at least one transistor. This can be realised using a second metal layer, but this is against the good practice to complete the entire matched pair test structure at first level metal. To avoid this, one would probably use a poly-Si under-crossing under metal-1. The extra (10 – 20 Ω) resistance in the base connections due to a poly under-crossing is usually no problem as the base currents during the mismatch measurements are typically well below 1 μA.
To maintain the symmetry in the pair, also the Base of the right transistor in figure 2.21 is equipped with a crossing, although this obviously would not have been necessary. Such strict (impedance) symmetry can be important to avoid that ONE of the two transistors suffers from high-frequency oscillations, while the other doesn't due to its slightly different capacitive (and resistive) loading and Base-Emitter coupling. In this case, this capacitive mismatch is largely mitigated by the different pad-to-pad and probe-to-probe cross-coupling capacitances.

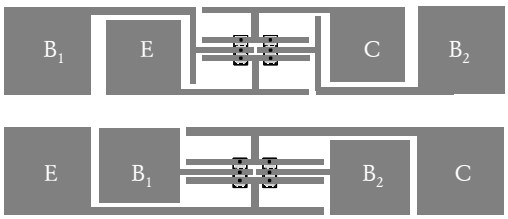

Figure 2.22 Alternative layout approaches for CE&CC scribe line matched pairs.

Two alternative CE&CC scribe line matched pair test structure implementation are depicted in figure 2.22. Obviously, such realisations have one clear advantage over the one represented in figure 2.21, namely perfect symmetry without requiring any crossing constructions.
In these examples the size, position and order of the pads are modified. The applicability of such implementations depends on the measurement system, in particular the prober. As the pads are not exactly placed 'in-line', a dedicated probe card would be required for such implementations. The order of the pads can for instance be relevant when manual manipulators (with two needles on one pad, or double needle Kelvin probes) are to be used for high precision mismatch measurements.

The CE&CC matched pair test structure configuration was used extensively, for instance for the matching characterisation of poly-emitter BiCMOS technologies. To save on the number of collector contact pads we have frequently combined CE&CC pairs into 2x9 (or 2x12) pad modules (figures 2.11, 2.12 and 2.24). Examples and interesting results from such implementations were discussed in [Tuin94] and [Tuin98].

An experience that was acquired through working with 2xN CE&CC modules is that it proves in fact more convenient not to share pads amongst multiple pairs. Rather settle for fewer device geometries than being hampered by unexpected device leakages, additional parasitic resistances and asymmetric capacitive loadings. Several times over the past years, we were limited in the characterisation possibilities by one leaking transistor (e.g. C-E leakage) that made the entire 2xN module useless. The careful reader may have noticed that the star connections to the Common emitter and Collector rails as advocated above, were not applied in the 7-pairs module of figure 2.11. Indeed, significant current dependent systematic mismatches were encountered in practice when such modules were used for mismatch characterisation of larger

area transistors at relatively high currents (mA's). Obviously, the effect of this resistance inequality in the collector rail is practically irrelevant, as the feedback through the Early effect will be negligible. An estimated 0.11 Ω difference in the emitter resistance (figure 2.23) resulted in a significant systematic mismatch which increases linearly with the collector current.

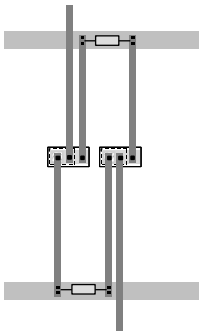

Figure 2.23 Unequal parasitic resistance in the Common Collector and Common Emitter connections of the 2xN pad frame implementations of CE&CC pairs.

In the original proposal for this module as described in [Tuin94] and depicted in figure 24, the Common Collector and Common Emitter rails were connected to two pads. This allows for voltage sensing, which would make the measurements independent of the position where the transistor is connected to the Common rails. In practice this was never actually implemented in a measurement algorithm, hence the extra pads disappeared at a certain redesign stage.

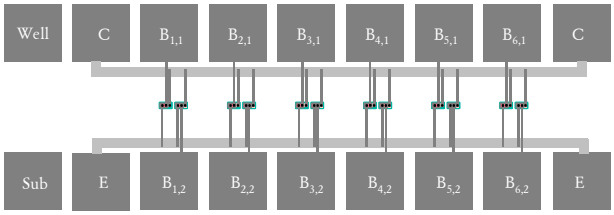

Figure 2.24 Multiple CE&CC pairs module in 2xN pad frame featuring double pads for the high current terminals.

Using the sort of layout refinements as discussed and explained in figures 2.17, 2.18, 2.21 and 2.22, such as double rail star connections, and/or changing orientation of (both) transistors (figure 2.11), the indicated 'imperfections' can largely be circumvented. The crossings in the base connections can be avoided when the Common C and E rails are allowed outside the pad frame rather than on the inside (as in figure 2.31 in the section on MOSFET pairs).
An, at first sight perhaps seemingly minor disadvantage of the CE&CC matched pair test structure is, that the capacitive coupling between the Base and the Collector is not identical for each of the transistors of a pair. The base connection of the left transistor of each pair crosses the Common Collector rail. Furthermore, there is some extra capacitive coupling due to the C and B lines running parallel over considerable distance. The transistor with base connection to the lower pad row will have a stronger coupling to the Emitter. This may seem irrelevant for a (DC) mismatch measurement. However, we have in fact encountered occasional problems where the mismatch results originally suggested an outrageously large systematic mismatch between two transistors in such a module. Closer evaluation of the measurements revealed however that one of the two transistors of the pair was oscillating during the measurements, whereas the other did not! Occurrence of such oscillations is often just a matter of a trifle extra feed-forward coupling. In the problems mentioned above, the oscillation was suppressed by biasing the pair in a lower current regime, indeed resulting in the disappearance of the unrealistically large systematic mismatches.
An inescapable consequence of the CE&CC test structure approach is that the two transistors of the pair cannot be measured simultaneously, at least where it concerns the main (collector) current mismatch. Hence, time sequential measurements are obligatory for this test structure. The main problem that is associated with this time differences is that the temperature of the wafer and/or the measurement equipment is not necessarily identical. This could contribute to an apparent parametric difference that is not due to device mismatch. When looking at small parametric differences of 0.1% and below, this effect cannot always be neglected, in particular for very lengthy measurements. The impact of temperature variations during measurements is discussed in detail in chapter 3 of this thesis.

Some alternative BJT matched pair test structure realisations

CE matched pairs

Drennan et al. claimed that they were hampered by junction leakage problems with the CE&CC approach. They circumvented this problem by assigning another collector pad to the matched pair [Drenn00]. Lau et al. followed the same layout approach [Lau03]. When translated to the schematic layout drawings as used in the figures in this chapter, Drennan's matched pair test structures implementation look as depicted in figure 2.25.

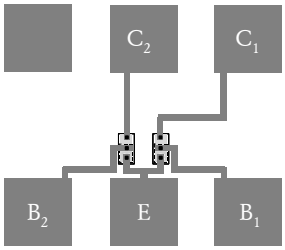

Figure 2.25 CE BJT matched pair implementation as reported by Drennan et al. .

This implementation provides full parametric mismatch characterisation flexibility. The central placement of the emitter star connection right above the Common emitter pad is well conceived (low resistance, good stress symmetry). Due to the 2xN pad frame and the odd number of required pads for each pair, this resulted in a slight asymmetry of the two collector connections. This can be 'repaired' easily, for instance by using the 'free' pad for the left Collector and the middle pad for the Substrate connection. The parasitic (interconnect) resistance difference in the collector lead would result in a (most likely) negligible systematic difference (Early effect).
A stronger effect can be expected due to mechanical stress effects due to the different shapes of the collector connections. The surprisingly large impact of such so-called 'bent collector connections' was reported in [Tuinh03a].

Differential V_{be} mismatch measurement
An entirely different BJT mismatch characterisation approach that is sometimes encountered, focuses on direct V_{be} offset measurements rather than on current mismatch measurements. For this measurement method, extra pads must be added to the matched pair test structure to connect the microvolt-meter as well as the bias current sources (figure 2.26).

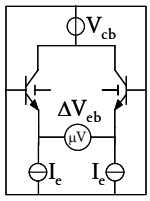

Figure 2.26 Common Base measurement circuit using a microvolt meter to measure V_{EB} offset.

An example of a test structure implementation of this approach is shown in figure 2.27. This layout certainly provides plenty of freedom to do all desirable parametric mismatch measurements, but an approach like this is quite 'pad hungry'. Moreover, the measurement instrumentation should indeed be capable to measure the offsets with sufficiently high (nanovolt!) resolution. The main reason however why this structure is less suitable for high precision mismatch measurements is that the Emitter voltage of the two transistors is affected by the probe-to-pad resistance, which is not necessarily equal for the two transistors.

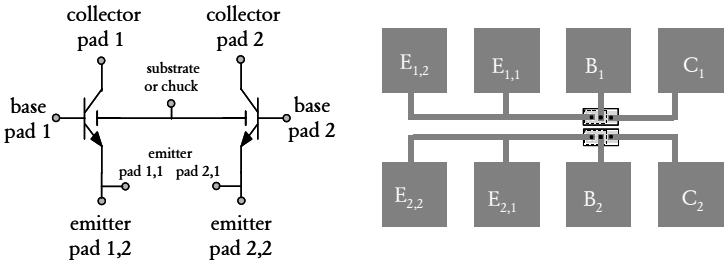

Figure 2.27 Schematic representation of a BJT matched pair test structure with double emitter pads for direct sensing of V_{EB} mismatch.

Figure 2.28 Two implementations of matched pair that consist of two individually padded (discrete) transistors.

Stepped discrete pairs

Another approach that can be (was) applied for characterising BJT mismatch was an idea, originally born out of necessity, but in practice turned out to have some interesting advantages. During the evaluation of a particular matching problem of a process flow in which discrete double poly NPN transistors were the main product we were forced to evaluate mismatch using the products dies instead of using dedicated matched pairs (as these were simply not available on some interesting product engineering wafers). This omission was circumvented by programming a prober movement step from one transistor to its counterpart in the 'pair', being another discrete transistor, typically a few hundred μm away. From a measurement system perspective, this approach is advantageous, as this technique results in fact in the only measurement method where measurement hardware (needles, probes, cables, matrix paths, sources and meters) is identical for the measurement of the two transistors. For characterisation systems without switching matrix, the 'stepped discrete pair' approach brings the additional advantage that there is no need for meter and/or source offset compensation, as each transistor is by definition measured using the same hardware. The fact that only three needles are used (four including Substrate), may be useful when ferrite beads are required to suppress oscillations, or when large Kelvin probes are used. Moreover, it is quite unlikely in this approach that one of the transistors of a pair starts oscillating, while the other remains 'quiet'. The additional time between the measurements of the two transistors that is attributed to the extra prober movements (of the order of 1 second) will not likely contribute significantly to the measurement inaccuracy. The main disadvantage of this approach is again found in the needle-to-pad contact resistance fluctuations. This makes the use of double (Kelvin) needles on the emitter pad inevitable. The additional stepping from one transistor to the other (and back and forth again if short-term repeatability is to be monitored as well will result in additional wearing of pads (see figure 2.9). This will become a problem if the same population is to by measured multiple times under different conditions. Figure 2.28 depicts two possible implementations of

the 'discrete pairs' approach. Note the extension of the base connection to an H-bar in metal in implementation A. This shape again improves the equality and consistency of the metal connections and provides the flexibility to place transistors with different geometries and layout styles in the same frame. Again, as in the previous layout approaches, many variant can be derived of this layout. Version B displays an equivalent metallisation symmetry, while the rotation of the transistor provides the possibility to probe the Emitter on a larger pad ‘at the end of the module’, giving more space for a double-needle Kelvin probe, that is inevitable for larger devices and/or emitter currents larger than 10 μA.

MOSFET matched pair test structures

For MOSFET matched pair test structures, many of the same arguments hold as those for the BJT examples treated in the previous section. The most often-encountered test structures layout for MOSFET's is the Common Source & Common Gate (CS&CG) approach. However, equivalent to what was discussed above for BJT's, a Common Source & Common Drain (CS&CD) approach has certain advantages, depending on the measurement system and preferred measurement algorithm.

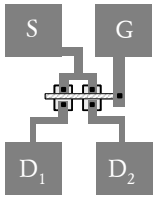

Figure 2.29 Prototype of the CS&CG MOSFET matched pair test structure.

CS&CG matched pair test structures

The prototype for the CS&CG matched pair test structure approach is shown in figure 2.29. Most implementations of this prototype structure combine multiple matched pairs into a single 2xN pad array. For such modules, it is quite common to extend the Common Source as well as the Common Gate rail to other pairs. This obviously saves pads and hence space, or allows more pairs within the available silicon area. Figure 2.30 gives an example of the layout approach we have used extensively for several of our own studies [e.g. Tuin96b and Tuin97a].

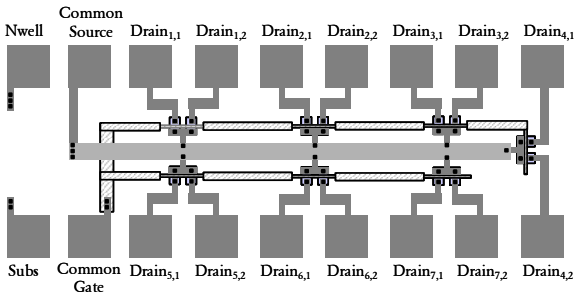

Figure 2.30 Example of a 2xN pad frame module with multiple CS&CG MOSFET pairs.

The layout approach as sketched in figure 2.30 was used extensively for several experiments and did provide many useful results. Scrutiny of this layout does reveal however, several possible (and indeed quite sensible) refinements. For instance, the currents are not flowing in identical directions for all matched pairs. Obviously, for the two transistors of each pair, the current directions are identical, but an uncertainty remains between the different pairs in the module. This is again an example where one could argue how relevant such differences can be. There may be a few physical reasons that could result in a difference between the pairs 1,1&1,2 compared to 5,1&5,2 but they will most likely be quite small. In fact, we did test this once in a particular technology, and could find no significant differences. But then again, that is not really the point here! What is far more important is that one must want to avoid any uncertainty in the layout. If for whatever reason a pair yields a distribution with a standard deviation that does not follow the expected (1/√(area)) behaviour, or yields a small, but statistically significant systematic mismatch, one does not want to be confronted with the additional uncertainty of a layout flaw. Mismatch characterisation is all about subtle effects, and as figure 2.31 demonstrates, the module could have easily been adapted to a more symmetrical layout single metal version without any crossings. Not only the pairs orientation issue is resolved in this module, but the entire placement of the pairs with respect to the Common (metal) lines and contact pads is much better in accordance with the symmetry guidelines for matched pair test structures given in the previous section. Obviously this improvement can only be used if the design rules and module (pitch) requirements for the (standard) pad frames allow for running metal lines 'outside' the pad frame and in between the pads.

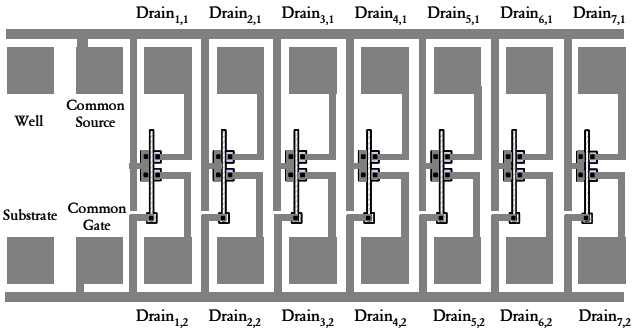

Figure 2.31 Improved layout symmetry for CS&CG MOSFET pairs in 2xN pad frame module.

Comparable to what was discussed for BJT matched pair test structures, we also switched over from 2xN pad frames to 1xM scribe-lane based versions of the CS&CG matched pair test structure approach [Tuinh00a, Tuinh00b]). An illustration of such a module is schematically depicted in figure 2.32. Examples of silicon implementations are shown in figures 2.8 and 2.9. The trade-off here is again (test chip) area versus consistency. The layout of figure 2.32 is kept symmetrical with respect to the surroundings by embedding the pair in a frame of lines (using star connections). Also, note the extension of the poly-Si gate to add some additional symmetry.

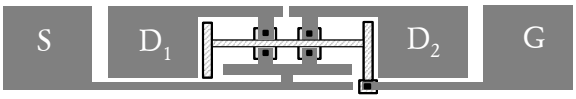

Figure 2.32 Scribe-line version of a CS&CG MOSFET matched pair.

CS&CD matched pair test structures

As discussed before in this thesis, sharing the 'large current (>100 μA) terminals' of both transistors in a pair may result in better repeatability of the mismatch measurements. As the voltage drop over the (fluctuating) needle-to-pad resistance is common to both transistors in a pair, its fluctuation does not contribute to the mismatch observation. Figures 2.33 gives 2xN and 1xM pad frame implementations of the CS&CD matched pair test structure approach.

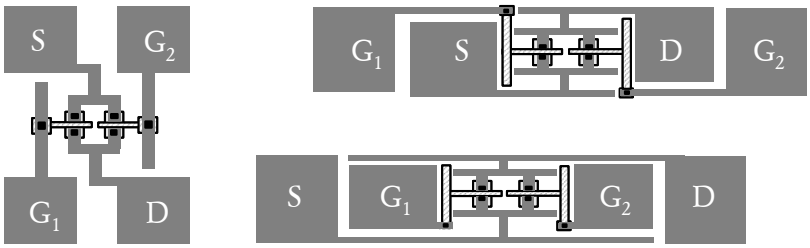

Figure 2.33 Examples of CS&CD MOSFET matched pair layouts.

Obviously, the CS&CD approach again prohibits measuring the transistors simultaneously (except for the gate current mismatch). An advantage of the availability of independent gate pads is that this enables characterisation of gate current mismatch. As high performance CMOS technologies move towards gate dielectrics thickness below 2 nm, the gate currents are becoming a significant part of the currents flowing in the transistors. Hence, one should automatically become interested in the fluctuation characteristics of these advanced dielectrics. Structures as depicted in figure 2.33 provide the possibility to measure gate current mismatch fluctuations. However, once the gate currents become significant, it probably will be necessary to distinguish between gate leakage to Source, Drain and Substrate regions independently. This means that a more appropriate structure again becomes a CS pair, comparable to a (modified) CE example discussed above (figure 2.25), or the 'stepped discrete pair' as depicted in figure 2.28 for, as this provides independent access to all device terminals.

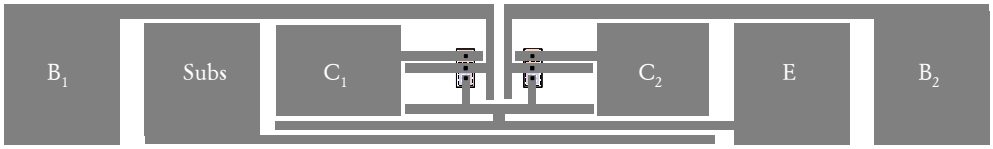

Figure 2.34 Schematic layout representation of the ideal BJT matched pair test structure.

Conclusion

When all arguments discussed above are combined with accumulated parameter extraction experiences and encountered probing and measurement hardware limitations as discussed in chapter 3 of this thesis, the preferred (ideal) matched pair test structure layouts for BJT's and MOSFET's can be configured as depicted in figures 2.34 and 2.35.

Note that these (pad-hungry) matched pair test structure realisations are 1xM pad frame implementations with Common Emitter or Common Source, accessed through a double-rail star connection to assure identical resistance. All other transistor terminals are separately padded out. A compulsory Substrate or Well contact pad helps to maintain access resistance symmetry to the outside pads. These implementations provide maximum measurement flexibility, perfect layout symmetry while using only one metal layer without any crossings (except for the low-current Substrate or Well contact). The pads on the outside are chosen to provide extra room for double probe needle positioning for Kelvin-sensing or offset monitoring as discussed in chapter 3 of this thesis.

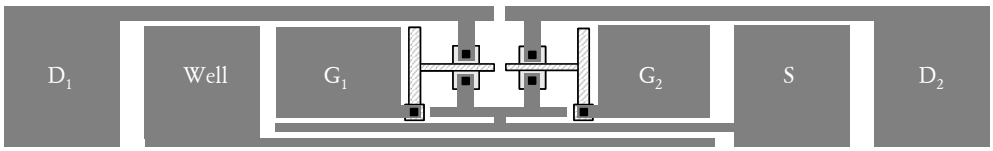

Figure 2.35 Schematic layout representation of the ideal MOSFET matched pair test structure.

Chapter 3

Matched pair characterisation techniques

3.1 Introduction: "door meten tot weten"[†]

Parametric measurements form the proof of the pudding for all IC technology fabrication lines. Test structures that are placed on every wafer in PCM's or PEM's are measured using DC I-V measurement systems. Based on the resulting parameters it is decided whether a wafer meets the electrical performance specifications. A typical DC parametric measurement system consists of five elements:

- Wafer prober. This machine holds the wafer and manoeuvres it such that the test structure's contact pads (on the wafer) are brought in contact with the probe needles.
- Connections between the contact pads and the measurement instruments. Probe needles, probe positioners or probe card, cables and often a switching matrix or multiplexer card.
- Measurement instrumentation. Voltage- and current sources, and voltage- and current meters controlled by a computer. Modern systems are based on so-called SMU's (Source / Monitor Units or Source / Measure Units), each being a combination of four instruments that can either force a voltage and measure (monitor) the current in the branch or force a current and measure the voltage on the node.
- Measurement algorithms. Control the connections, set the biases, measure the responses and calculate the parameters.
- Data analysis. Database, electrical specifications, and statistical data analysis and decision software.

This chapter discusses special demands and refinements that are required for the high precision parametric measurement and statistical data analysis techniques for evaluation of matched pairs. As in the previous chapter, it must be realised that parametric mismatch measurements, although essentially not different from ordinary semiconductor parametric measurements, often do require special attention. While standard parametric measurements generally require measurement precisions of the order of 0.1 to 1%, mismatch measurements may have to be done with substantially higher precisions. Moreover, since parametric mismatch fluctuations are stochastic phenomena, large numbers of measurements must be collected (in a relatively short time), and statistical estimators must be derived with care. Hence, the art of matched pair characterisation can be divided into two major components: high precision parametric measurements, and careful statistical analysis of the population of collected mismatch

[†] The often used (abused) quote 'to measure is to know' is attributed to Lord Kelvin (William Thomson). It cannot be denied however that Kamerlingh Onnes' motto '*door meten tot weten*' (through measuring to knowing) testifies of more respect for the art of correctly measuring and interpreting physical phenomena.

observations. Elements of both these fields are discussed in this chapter. Section 3.2 focuses on hardware related choices and issues for high precision matched pair measurements. The subjects range from specific equipment choices with associated measurement algorithm trade-offs, to the relevance of temperature-instabilities on high precision mismatch measurements. An important, albeit often underexposed element of mismatch characterisation is the so-called short-term repeatability (STR) of the mismatch measurement method. This is discussed in section 3.3. The STR determines the lower limit of the mismatch standard deviation that can realistically be obtained with the measurement system and used mismatch measurement algorithm. Moreover, the STR of the mismatch measurement provides valuable information about the performance and status of the measurement system and the STR forms a useful measure to assess the effectiveness of measurement algorithm improvements. Several STR assessment techniques are compared in this chapter. Section 3.4 discusses some specific tricks of the trade of high precision parametric mismatch measurement. The importance of avoiding measurements near meter and source range transition points is demonstrated, and possibilities of built-in source offset monitoring are explored. An important element of high precision parametric measurements is the application of multiple observations for each measurement. The rationale behind this technique is explained and the workhorse of most of our mismatch measurements, the M9S5 algorithm is discussed. Section 3.5 deals with (statistical) data analysis techniques that are relevant for mismatch evaluation. The advocated safe standard deviation estimation technique is based on five pillars, namely a-priori knowledge, median estimation from multiple observations, range filtering of observables, the blunt axe method, and graphical verification of populations using normal scaled cumulative probability plots. Furthermore, this section discusses the relevance of statistical uncertainty assessment, in this work practically always based on the bootstrap technique, which is also briefly explained.
As in the preceeding one, this chapter on characterisation techniques ends with an example. The discussed case exemplifies some of the common pitfalls and hazards that are frequently encountered when doing parameter (mismatch) extractions at, or beyond the accuracy specifications of the measurement equipment.

3.2 Matched pair measurement hardware considerations

As pointed out before in this thesis, in matched pair characterisation there is a strong relation between the matched pair test structure, the measurement algorithm, and the measurement hardware. Already during the test structure's definition and design phases, choices are made that determine how the mismatch measurements should (or could) be done. This section discusses some of the considerations for the measurement hardware as used in this work.

Measurement system and prober

Practically all measurements reported in this thesis were collected using a measurement system (figure 3.1) that consists of an Agilent HP4156A precision semiconductor parameter analyzer without switching matrix and a Cascade-Microtech Summit 12k probe station without thermo-chuck.

Figure 3.1 At work with the HP4156/CM 12k mismatch measurement system.

This system was originally selected for this study, based on its attainable 1 fA measurement specifications. Such very low current measurements do not play a significant role in the field of parametric mismatch characterisation. This choice was based however, on the assumption that a system concept that can handle such low currents must be extremely well shielded and guarded. It was anticipated that such good shielding and guarding would also be beneficial for reaching the best possible measurement precision for parametric mismatch measurements. Our 4156 system (figure 3.2) was augmented with a 41501 expander with two additional (medium power) SMU's. This provides the total mismatch measurement system with four high precision SMU's (with double triaxial actively guarded cabling), two medium power SMU's, two non-measuring voltage sources and two voltage meters.

Figure 3.2 The 4156 front panel and back plane (including 41501 expander) with double triaxial cabling for the HRSMU's.

IBASIC programs were used for most of the mismatch measurements reported in this thesis. IBASIC stands for Agilent's Instrument BASIC programming language. In our system, a typical IBASIC mismatch measurement program controls the complete statistical characterisation of one population of matched pairs. After some initialisation, the program prompts the measurement hardware to measure the two devices, calculates parameters and mismatches, stores results in a data-file and then prompts the prober to move to the next test site (next pair). When the entire population of a particular pair on a wafer is measured, statistical data analysis is performed (raw data analysis, outlier filtering, safe estimation, and bootstrap analysis; see later in this chapter). Finally, the statistical estimators are displayed on screen and stored in the data file. After brief evaluation of the results and some administrative tasks, the prober is re-aligned to the first die on a new pair, after which the IBASIC program is started again for another type of pairs. The main advantage of using IBASIC as control language on the internal controller of the 415X parameter analyzer is the seamless translation of common I-V-graphics-based manual measurements into the automated measurements that are required for statistical characterisation. Through the GP-IB instrument bus, bias conditions can be modified, and external instruments (like the prober) controlled. A disadvantage of the IBASIC approach is the slow program execution of the controller (the good old 68000 microprocessor), which poses severe limitations with respect to statistical data analysis at runtime.

In a later stage of the project, our HP4156 was replaced by an 8-SMU Keithley 4200 Semiconductor Characterization System (figure 3.3). This system is equipped with a (Pentium IV) Windows driven computer board, allowing the use of compiled C-code for data analysis and display. The SMU's with remote pre-Amps (figure 3.4) are controlled individually through

a built-in fast instrument bus, allowing fast execution of dedicated ultra high precision measurement algorithms, with arbitrary bias point selection and instrument setting control. With this system, it also proves feasible and very useful that the statistical characterisation of a population of pairs (using C-coded User Test Modules) can be augmented with detailed interactive tests of individual pairs or devices. The greater computing power of the built-in controller is exploited to incorporate the graphical and numerical statistical analysis techniques discussed later in this chapter [Ewert05]. The Summit series semi-automatic wafer probe stations (figures 3.1, 3.3, 3.4) were designed by Cascade-Microtech to enable on-wafer ultra-low leakage current measurements down to the femto-Amp levels. The guarding and isolation techniques required for this type of low-level measurements had been known for many years, but it was not until Cascade and HP worked together to built a wafer prober in combination with a high precision parameter analyzer (the 4156), that this type of measurements became available as an of-the-shelve system.

Figure 3.3 A Keithley 4200-SCS in the mismatch characterisation system.

From a high precision parametric measurement perspective, important features of the Summit 12k prober are the so-called micro-chamber and the shielding and active guarding of the cables and probes. The micro-chamber functions as a Faraday-cage around the (moving) wafer chuck. The micro-chamber also proves quite effective in terms of light shielding. This implies that the prober does not have to be placed inside a cabinet. This results in easy (microscope) wafer inspection and manipulator access. Moreover, as no doors or curtains need to be closed, bouncing and scratching needles on pads is considerably reduced.

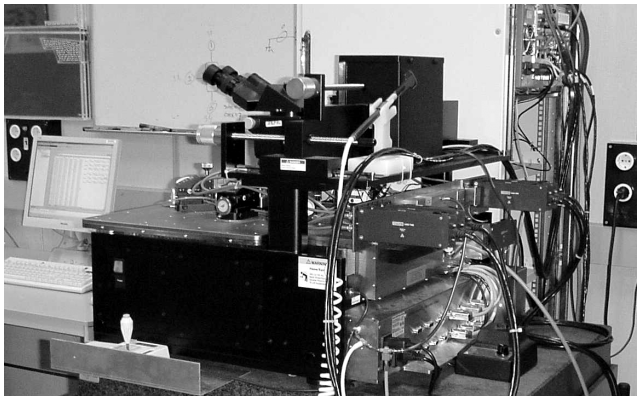

Figure 3.4 Wafer prober with remote pre-amps seen from the rear.

For the high precision mismatch characterisation measurement system, as configured for this work, we aimed for maximum flexibility in terms of the measurement (probing) approach. This is primarily driven by the fortunate circumstance that for this research project, we must work with wafers and test structures that are fabricated in different fabs. This implies however that one must be prepared to characterise a multitude of test structure layouts, based on different standards, coming from different local fab cultures. Therefore, we chose to work with manual probe positioners (figure 3.5) rather than using fixed probe-cards. This provides total independence of the actual contact pad arrangement and matched pair test structure layout. The DCM-200 positioners (manipulators) prove very user-friendly, and provide active guarding in both force and sense connections up to well inside the micro-chamber. A limitation of working with such (rather bulky) manipulators is the limited number of positioners that can be placed on the prober platen. On our system, we are restricted to six (or seven) positioners on the platen (figures 3.5). However, six needles (plus a chuck connection) prove sufficient for most matched pair measurements. As discussed in the previous chapter of this thesis, such hardware limitations should be taken into account during the definition of the test structure, but the reality is different when test structures from different fabs and cultures are to be measured.

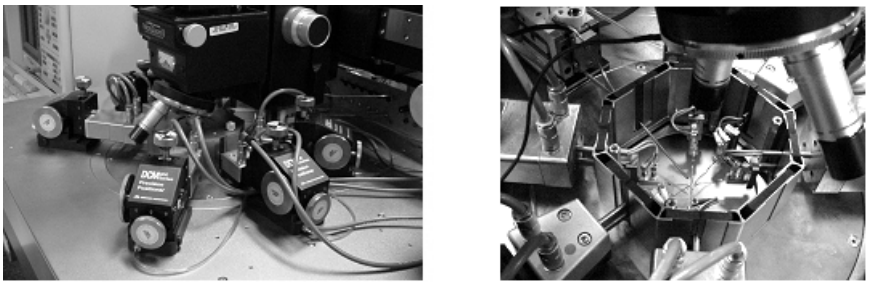

Figure 3.5 Platen of the C-M 12k prober with six DCM positioners. On the right, the microscope is raised and the cover of the top hat removed, showing the six needles and a PT100 sensor.

To switch or not to switch

Most automated semiconductor measurement systems are equipped with so-called point-to-point or pathway switching matrices. In essence, a switching matrix provides the capability to connect any of the sources and meters in a measurement system with any of the pin cables, and eventually via the test-head, probe-card adapter or manual manipulators to the needles and contact pads of the test structures. In a general process characterisation test environment, switching matrices are indispensable as they provide the flexibility to characterise many different types of test structures. From a high precision parameter extraction standpoint, switching matrices provide useful possibilities, such as reversing polarities of the connections to the instruments to compensate instrumentation offsets [Killm].

Known disadvantages of switching matrices are associated with extra parasitic resistances, fluctuations due to wear-out or degradation of switches, and thermo-voltage offsets caused by temperature non-uniformities in the measurement system. The main reason however why we decided not to use a switching system in our mismatch characterisation system was driven by several bad experiences while measuring BJT matched pairs as a result of oscillating transistors. Therefore, we added two extra SMU's to the standard four in a parameter analyzer, which provide the extra biasing and measurement capabilities required for measuring two simultaneously probed transistors.

Temperature control

One of the main concerns for reaching ultra-high mismatch characterisation precision is the question how to deal with temperature variations during the measurements. Measurement labs are usually climate controlled. In practice, this implies that temperature fluctuations in labs vary from +/- 0.5 °C up to +/- 2 °C around the preset temperature. The temperature of the wafer can again be quite different from the lab temperature. The magnitude of this deviation depends on power dissipation in, on, or near the prober and on the thermal time-constants of the chuck and prober. Wafer chucks of (semi-) automatic wafer probers like the C-M 12k or the Electroglas 2k & 4k do warm-up quite considerably during operation, primarily due to the dissipation of the chuck movement motors. Chuck temperature increases of as much as 10 to 15 °C above the lab temperature are encountered on PCM-tester probers such as the Electroglas 2k or 4k. On a very different scale, we measured 0.2 to 0.5 °C temperature rises inside the micro-chamber when the microscope lamp is not switched off on our C-M 12561 prober.
The common solution to such temperature uncertainties is to equip the wafer prober with a so-called thermo-chuck with temperature sensor and controller, which through heating and/or cooling can maintain the wafer at a preset temperature. Thermo-chuck systems however, do have significant disadvantages for high precision mismatch measurements. Thermal chuck systems are generally considered more prone to EMC disturbances than non-thermal chucks. Resistive heaters or Peltier cooling/heating elements inside thermal chucks tend to give rise to switching and/or severely enhanced power line (50/60 Hz) signals in the Substrate. These can deteriorate low-level measurements. There are signs in the recent literature and spec-sheets that major improvements in thermo-chuck design have been achieved [Einf04].
To put the importance of temperature uncertainties for parametric mismatch measurements into perspective, some typical temperature coefficients for common transistor observables are given in table 3.1. These values, found in standard textbooks, indicate that temperature uncertainties of more than 5 °C can definitely not be neglected for most semiconductor device parameter measurements. Such wafer temperature uncertainties during measurements would affect the control specs of some of the main parameters of an IC process. Therefore, thermo-chuck temperature controllers are generally considered indispensable. A high quality thermal chuck system will for instance have control specs of the order of +/- 0.1 °C, but chucks specified at +/- 0.5 °C are no exception.

This brings us to the question whether a thermo-chuck system is required for mismatch measurements. There are two sides to this question. In the first place, one can argue that the two devices of a matched pair at small distance on a silicon test wafer are at the same

temperature. On the other hand, there is the question whether mismatch itself is sufficiently temperature independent to live with the quoted temperature uncertainties of up to 10 °C of an uncontrolled chuck. To begin with the latter, it can be argued that it is quite likely that most parametric mismatch mechanisms are temperature independent in the temperature range of interest for most integrated circuits. If one for instance accepts that dopant fluctuations (driving MOSFET V_T or BJT Gummel numbers) are the main sources for mismatch fluctuations, it becomes quite unlikely that the mismatch changes over temperature, as practically all dopants, charges and interface states are electrically active in the common integrated circuit operating temperature ranges between 300 and 400 Kelvin. This assumption is supported by the experience from well-designed electronic circuits, such as bandgap voltage references where the mismatch indeed is shown to be practically temperature independent [e.g. Pelg89].
The first assumption however, namely the equality of the temperature of both devices during the measurement, in practice proves less obvious than it may seem. In many parametric measurement algorithms, the two transistors of a pair are in fact not measured simultaneously but sequentially. This implies that the temperature inequality between the devices is actually determined by the temperature drift of the wafer (chuck) between the measurements of both devices. That this is not always negligible is demonstrated in the remainder of this section.

Parameter / Observable	Typical Temperature coefficient
BJT Collector current	6 to 8 %/°C
V_{EB}	-1 to -2 mV/°C
h_{FE}	7000 ppm/°C
MOSFET Subthreshold current	5 - 7 %/°C
Threshold Voltage	1 to 3 mV/°C
Mobility	-0.9 to -1.1%/°C

Table 3.1 Typical temperature coefficients of transistor parameters

Quite often (time consuming) measurement precision enhancement precautions must be taken in mismatch measurement algorithms. This can result in a significant time gap between the measurements of the devices of the matched pair. Intervals of up to tens of seconds between measurements of matched components are not uncommon. This implies that the chuck temperature problem is in fact more related to how quickly does the chuck (wafer) temperature change than what the actual temperature of the chuck is; or approaching it from the other side, namely how quickly do the measurements have to be completed to assure that chuck temperature changes do not affect the mismatch observations.

Temperature stability during DC I-V measurements

To study the effects of a thermo-chuck controller (TCC) on a parametric measurement, the following experiment was conducted. A particular MOS transistor was measured during a period of 300 seconds on two different systems (figure 3.6). The first dataset is collected on one without a thermo-chuck (C-M 12k prober with micro-chamber; syst1). The second is measured on one with a thermo chuck set at room temperature (at about 22.5 °C; Electroglas 2k semi-automatic wafer prober with Temptronic TP317B & 150 mm chuck; syst2+TCC). Subsequently, the thermo-chuck controller was switched off, the prober was left to stabilise for about one hour, and then the transistor was measured again on the same system but now with the TTC switched off (syst2-TCC). The (10/0.25 NMOS) transistor was biased in the subthreshold region (@V_{GS} = -0.1 V) yielding a current level of about 200 pA.
The measurements were done with an HP415x at long integration at one-second intervals.

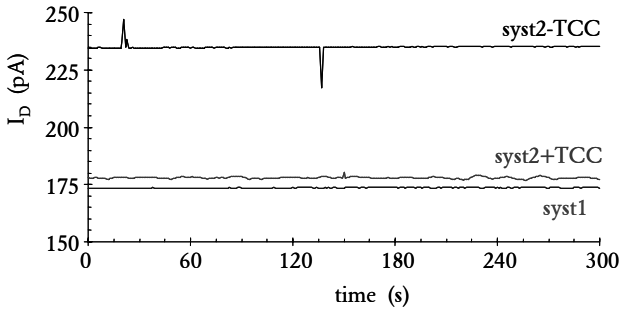

Figure 3.6 Drain current measurement of N-channel MOSFET under constant (subthreshold) biasing.
syst1=HP4156&CM12k; syst2=HP4155&EG2k; +TCC=ThermoChuck controller ON; -TCC=OFF

Figure 3.6 demonstrates several interesting features about this kind of measurements and measurement systems. In the first place, the absolute differences between the currents may seem surprisingly large, considering this was the same transistor each time, but this is merely an effect of the actual wafer temperature during the measurement. The difference between 'syst1' and 'syst2+TCC' is about 3%, which corresponds to about 0.5 °C (using table 3.1). The observed difference between the '–TCC' and '+TCC' version should not come as a surprise either. This difference is about 30%, which corresponds to a chuck temperature difference of about 5 °C. As mentioned above, such temperature differences are not unlikely for the Electroglas probers that dissipate a significant amount of power in the linear motor that drives the chuck

position. Other striking features of figure 3.6 are some relatively large current spikes. These spikes have nothing to do with the temperature, but they will be discussed later in this chapter. At the y-axis scale of figure 3.6, the current fluctuations around their own average hardly reveal anything. All three curves are probably quite acceptable for standard parametric tests, although most people will judge the '+TCC curve' somewhat noisier. Such noise is generally attributed to the extra fluctuations coupled-in through the chuck but this is certainly not the case here. This is demonstrated by plotting part of the results as relative current fluctuations (figure 3.7). This figure depicts the relative current fluctuations during the final 2.5 minutes of all three experiments. Each curve is in this case normalised by its own median during the interval.

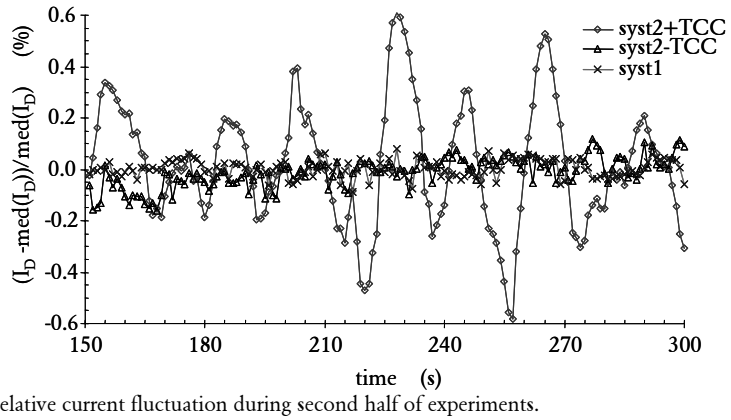

Figure 3.7 Relative current fluctuation during second half of experiments.

From this figure it is obvious that the noisy +TCC curve is in fact dominated by deterministic periodic variations due to the control circuit of the thermo chuck system. Variations of about +/- 0.5% are observed, corresponding to a quite reasonable +/- 0.1 °C temperature swing. However, what is quite discomforting for mismatch measurements is the periodicity of these temperature variations. Within a timeframe of about 10 seconds, the temperature goes from minimum to maximum. This is particularly harmful for time-sequential mismatch measurements, as in such measurement algorithms it may very well be the case that the second device of a pair is measured between 2 and 20 seconds later compared to the first device. Note that a 1% change of the parameters may fall well into the range of interest for a mismatch measurement. When the temperature controller is switched off (syst2-TCC), the stability improves substantially.

The syst1 curve hardly drifts at all during the measurements (< 1 ppm/s). The fluctuations are in this case dominated by noise fluctuations of the transistor as discussed in [Tuinh01a]. The syst2 prober is placed in a large light-tight cabinet, which apparently is more susceptible to temperature drifts. Trend-analysis on temperature drift of the –TCC curve in figure 3.7 yields a slope of approximately 10 ppm/s, which at 6% /°C corresponds to about 0.01 °C/minute. The observed current noise is practically equal to the syst1 measurements, which indicates that the noise contribution from the chuck itself is negligible.

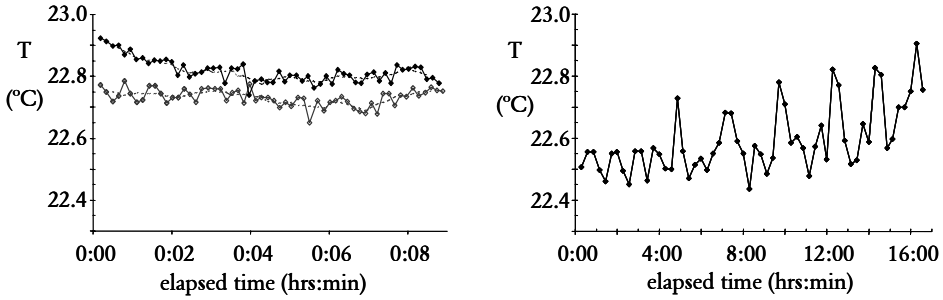

Figure 3.8 Examples of temperature observations inside the prober. Left: short measurement (dashed lines: 5-point moving average); Right: long measurement.

Based on observations and experiences as discussed above, it was decided to configure our high precision parametric mismatch measurement system without thermal chuck system. By leading a PT-100 temperature resistor probe into the micro-chamber (figure 3.5), the micro-chamber temperature is monitored a few millimetres above the wafer. Figure 3.8 shows results of temperature measurements inside the micro-chamber of the prober. This is the same prober as used for syst1, be it this time with the Keithley 4200 as measurement system and placed in a different measurement lab (figures 3.4, 3.5). This experiment demonstrates the impact of the measurement lab's air conditioning unit. The temperature readings were collected during mismatch measurements of complete populations. The temperature is measured at the start of the mismatch measurement of each pair. The time axis represents the elapsed time since the first measurement (pair) of the population. Some noise is evident in the measurements (corresponding to a temperature measurement uncertainty of about 0.05 °C, but also some remarkable trends can be recognised. The left graph shows measurements during a fast

mismatch assessment. The measurement time of the total population takes approximately 9 minutes. The temperature (e.g. 5-point moving average) varies less than about 0.1 °C during these tests. The right graph in figure 3.8 shows the temperature in the micro-chamber during an extremely long (17 hours!) mismatch measurement. Note the much larger temperature variations that are encountered during these measurements, in particular after about 5 hours of measurements. Long measurements are usually started at the end of the regular working hours, in these cases at about 5 o'clock in afternoon. The much larger variations hence start between 9 and 10 in the evening. This behaviour is probably attributable to a change in the setting of the regulator of the air conditioning unit in the measurement lab.

A practical rule of thumb that can be derived from the observations presented and discussed above is that the wafer temperature inside the (C-M 12k) prober under normal measurement conditions tends to rise and fall during a measurement session at a rate of about 0.01 to 0.02 °C per minute (0.3 to 0.6 °C/hr). If the time difference between the measurements of the two devices is of the order of 10 seconds to 1 minute, a temperature difference during the measurements of the order of 0.002 to 0.01 °C is to be expected. This corresponds to apparent mismatch observations ranging from 3 to 20 μV or from 100 to 700 ppm's (table 3.2).

Type of Parameter or Observable & temperature dependence	Monotonous chuck temperature gradient (0.6 °C/hr) Elapsed time between measurements	
	10 s (0.0017°C)	60 s (0.01 °C)
V_T&V_{EB}@2 mV/°C	3.4 μV	20 μV
I_C&I_{OFF} @7%/°C	118 ppm	700 ppm

Table 3.2 Estimated parametric differences attributable to temperature changes during time between measurements.

A controlled thermal chuck system with temperature gradients of up to 0.2 °C per 10 seconds (figure 3.7) yields quite different numbers. Apart from the 2 orders of magnitude larger (faster) fluctuations, there is another difference between the impact of a temperature change from the controlled chuck compared to the much slower changes associated with lab environment and uncontrolled chuck heating. A slow temperature drift will result in a systematic mismatch as the first tested component of the pair is always measured at a slightly lower (or higher) temperature

than the second component. The ‘controlled’ chuck on the other hand, will probably result in an increased mismatch standard deviation, as the elapsed time between the two measurements will generally not be in phase with the variation of the chuck temperature.

The numbers from table 3.2 can also be used to derive how much time there is available for a complete mismatch measurement. For this thesis’ mismatch characterisation system, we are looking for mismatch numbers with a lower limit of about 10 μV for offset voltages and 100 ppm for BJT current mismatch values. This implies that there are about 10 to 30 seconds to complete a set of measurements on a pair. For an HP4156 type of measurement system, measurement file loading and bias changing via the GP-IB bus, this is doable, but certainly not ample. Common numbers that are used for the measurement programs as used in this thesis range from an average of about 6 seconds (MOSFET's) up to 40 seconds (BJT Base and collector currents) per pair, when a fairly limited number of measurement repeats is used (typically 9; see section 3.4.4). If one forgets about GP-IB based types of measurement programs and move to more production oriented parametric testers like the Keithley S400 and S600, Agilent’s 4073,
or the Keithley bench-top 4200 SCS, one can measure significantly faster. Typical numbers on a production parametric tester for a “connect/force/measure” sequence would be of the order of about 15 to 120 ms for a typical measurement. This means that it is possible to characterise a pair of devices well within a few seconds, even when multiple measurements are involved. This alleviates temperature stability constraints considerably.

Note that time / temperature drift considerations as discussed above can (must) also affect fluctuation measurements on medium and large size array test structures as discussed in section 2.2 of this thesis. The long time-windows, during which the many supposedly equal devices of an array are measured, imply that temperature drifts form a limitation that certainly must be considered when small mismatch effects (larger device areas) are to be studied.

3.3 Short-term repeatability assessment

A key element for any high-precision parametric mismatch characterisation study is the assessment of the mismatch measurement precision limit of the used measurement system. Parametric datasets are -by definition- noisy. Therefore it is important to know which part of the observed fluctuations is attributable to the actual parameter fluctuations in the population, and/or which part is due to disturbances from the measurement system (or even noise from the devices under test). Examples of the impact of such uncertainties are discussed in many of our publications on mismatch measurement techniques and subtle mismatch effects [e.g. Tuin96a, Tuin98, Tuinh00a, Tuinh01b, Tuinh02a, Croon02a, Tuinh04, Ewert05]. Statistical assessment of the short-term repeatability (STR) proves a useful tool to obtain information on the actual performance of the measurement system and consequently on the precision of mismatch measurements. Essentially, any STR assessment method is based on re-measuring the (mismatch) parameter of interest. When the measurement repetition is done within a short time frame, say less than a minute, the difference between the observations can be considered as mainly attributable to system and device noise and EMC disturbances. When there is a longer time gap between the measurements, temperature drifts of the devices and/or the measurement hardware may be non-negligible. The short-term repeatability is not only determined by the measurement system, but it is to a large extent attributable to the used measurement algorithm. Consequently, the STR of mismatch measurements can usually be improved considerably by adjusting such variables as instrument control settings (integration time, delay time, filtering) and through multiple measurements.

Several methods can be devised to assess the short-term repeatability of a mismatch measurement system/algorithm. A number of those, along with their merits and disadvantages are discussed in this section. The following nomenclature is used for comparing these methods.

- Assume one is determining the mismatch fluctuation estimators $\sigma_{\Delta P}$ and $\mu_{\Delta P}$ of a population of N pairs of devices. The mismatch ΔP_i is defined as the difference $P_1 - P_2$ between the parameter (P) of the devices 1 and 2 of the i-th pair.
- When the same pair is re-measured, a $\Delta\Delta P_i$ can be calculated as the difference between two (independent) observations of ΔP_i.
- When this $\Delta\Delta P_i$ is determined for all pairs of the population, a standard deviation $\sigma_{\Delta\Delta P}$ can be estimated.

The resulting $\sigma_{\Delta\Delta P}$ estimator forms a sensible measure for the repeatability (uncertainty) of the mismatch measurement ΔP_i, be it that the calculated $\sigma_{\Delta\Delta P}$ should be divided by $\sqrt{2}$, as the determination of each $\Delta\Delta P_i$ involves two times the number of (noisy) observations as used for the determination of ΔP_i

Measurement uncertainty can also be approached from a different side. Let's assume that a mismatch standard deviation $\sigma_{\Delta P,obs}$ was measured (observed). This estimator includes the real device mismatch fluctuation as well as a (system/algorithm related) noise contribution. These can be denoted as $\sigma_{\Delta P,mm}$ and σ_{syst} respectively. The variances of these independent variables add up, hence, $\sigma^2_{\Delta P,obs} = \sigma^2_{\Delta P,mm} + \sigma^2_{syst}$. According to these definitions, σ_{syst} corresponds to $\sigma_{\Delta\Delta P}$ through $\sigma_{syst} = \sigma_{\Delta\Delta P}/\sqrt{2}$.

There are two ways to apply STR information in high precision mismatch characterisation studies:

- Correct the observed mismatch standard deviation. When the noisy component of the STR is independent of the actual mismatch distribution (statistically uncorrelated), the variance of the system-induced component (σ^2_{syst}) can be subtracted from the total observed fluctuation variance ($\sigma^2_{\Delta P,obs}$). This yields the real mismatch variance belonging to the population that is measured ($\sigma^2_{\Delta P,mm}$). Hence, in terms of standard deviations: $\sigma_{\Delta P,mm} = \sqrt{(\sigma^2_{\Delta P,obs} - \sigma^2_{syst})}$. This approach can be useful when one is measuring relatively small mismatch standard deviations that are close to the system's short-term repeatability limit.
- Warning signal. In practice, one should avoid applying the correction approach as described above. Much rather should one use STR information as a safeguard and make sure that measurement's fluctuations do not significantly affect the mismatch fluctuation standard deviation. If this condition is not met, it makes more sense to work on an improved measurement algorithm than to subtract measurement noise from the mismatch information. As a rule of thumb, one should set a limit for acceptable system noise by assuring that $\sigma_{\Delta P,obs}$ is always larger than 3 x σ_{syst}. When this is the case, one can be sure that the actual mismatch standard deviation is not affected more than 10% ($<1/3^2$) by the system noise. That this is not always trivial, even for simple mismatch measurements, is for instance shown in [Croon02a].

The remainder of this section discusses merits and limitations of four techniques for STR assessment.

i. The re-measured population approach

The most elementary technique to assess the STR of a mismatch standard deviation is based on simply measuring the entire population of matched pairs twice within a reasonable time frame. This provides two types of information. In the first place, one gets the mismatch standard deviation estimators for both measurements. What one hopes to see at least is that both measurements yield approximately the same numbers. Although this may seem reassuring, the fact that the estimators are the same does not say much about the precision of the individual mismatch measurements. Therefore, the mismatch observations of both measurements must be point-to-point correlated and the standard deviation $\sigma_{\Delta\Delta P}$ must be calculated. The 're-measured population' approach is demonstrated in figures 3.9 to 3.11, which are based on two consecutive mismatch measurements of a population of 66 (fairly large) W/L=40/0.24 n-channel MOSFET's from a 0.18 μm CMOS technology. The transistors were measured with a linear region (V_{DS}=0.1 V), fixed gate-bias 3-point V_T/Beta/Theta extraction method [Tuinh00a, Croo02a]. The two measurement sequences were done with approximately 16 minutes in between. The mismatch fluctuation standard deviations for ΔV_T and $\Delta\beta/\beta$ of the two measurements are given in table 3.3. The normal scaled cumulative probability plots (NSCPP) for the V_T and beta mismatch are shown in figure 3.9. Those who are not familiar with the NSCPP are referred to section 3.5 for a brief explanation of this type of graph.

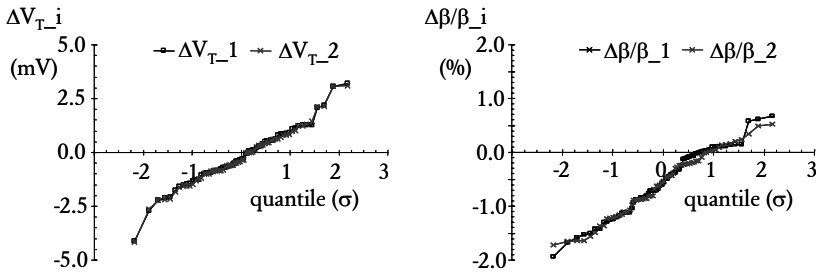

Figure 3.9 STR assessment type i. Cumulative probability plots of ΔV_T and $\Delta\beta/\beta$ of a complete population measured twice.

	V_T mismatch	beta mismatch
$\sigma_{\Delta P,obs}$ from first measurement	1.287 mV	0.609%
$\sigma_{\Delta P,obs}$ from second measurement	1.289 mV	0.581%

Table 3.3 Mismatch fluctuation standard deviations of two consecutive measurements. Note: The number of decimals in this table is physically spoken ridiculous. They are shown in the table to demonstrate there is at least a numerical difference. Such differences are not statistically significant at this population size!

Both the table as well as the graphs show that there is a very good agreement between the two measurements. Particularly the equality of the shape of the two cumulative probability curves for the ΔV_T is striking, suggesting that this is an example with excellent short-term repeatability. The two measurements indeed yield a (statistically) insignificant 2 μV standard deviation difference. The $\Delta\beta/\beta$ curves in figure 3.9 indicate a slightly poorer short-term repeatability for the $\Delta\beta/\beta$ measurement. Nevertheless, as table 3.3 indicates, one should not be worried too much about this larger system induced fluctuation, as the observed mismatch fluctuation standard deviation difference (0.61% vs. 0.58%) is statistically insignificant for the used population size. The short-term repeatabilities $\sigma_{\Delta\Delta VT}$ and $\sigma_{\Delta\Delta\beta/\beta}$ were subsequently calculated from the two sets of observations:

	V_T mismatch	β mismatch
Short-term repeatability $\sigma_{\Delta\Delta P}$ ($\sqrt{2}\ \sigma_{syst}$)	91 μV	0.125%

Table 3.4 Short-term repeatability standard deviations according to method i.

The short-term repeatability standard deviation $\sigma_{\Delta\Delta VT}$ was found to be below 100 μV. As this implies that $\sigma_{\Delta VT,obs}/\sigma_{\Delta VT,syst} > 20$, the effect of the system/algorithm is entirely negligible. Note however, that although the mismatch standard deviation estimators from the two test were only 2 μV apart (table 3.3), the estimated system noise (σ_{syst}) is almost 65 μV (table 3.4). For the Beta mismatch, the 0.13% short-term repeatability number may seem significant compared to the observed mismatch numbers (0.6%). However, as $\sigma_{\Delta\beta/\beta,obs}/\sigma_{\Delta\beta/\beta,syst} > 6.5$, the resulting correction by subtracting the variances lead to $\sigma_{\Delta\beta/\beta,mm}$'s of 0.603% and 0.574% respectively, still be well within the statistical uncertainty limits.

Point-to-point scatter plots of the two consecutive sets of measurements provide more insights into the repeatability behaviour of the system / measurement algorithm. For the example discussed above, these are shown in figure 3.10. The correlation between the parameters of both

measurements indeed proves excellent. As expected, the repeatability is visibly better for the threshold voltage mismatch than for the current factor mismatch.

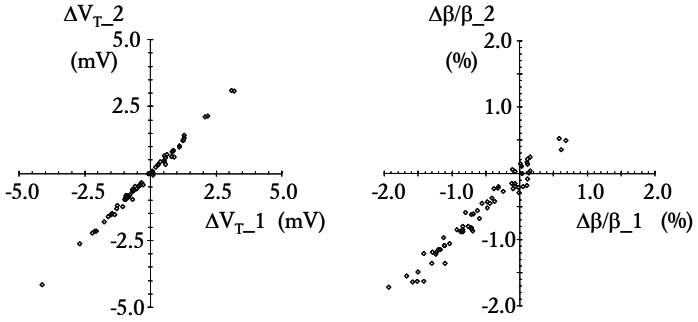

Figure 3.10 STR assessment type i. Scatter plots of ΔV_T and $\Delta\beta/\beta$ of a complete population measured two times.

The larger uncertainty of the beta mismatch measurement may be attributable to noise of the transistors [Tuinh01a]. Another source of uncertainty in this STR assessment technique is that the second time the probes are placed on the pads, the probe-to-pad resistance will be slightly different. This resistance difference will show up more pronounced in the beta's compared to the V_T's. The normal scaled cumulative probability plots of the $\Delta\Delta P_i$ populations for this example are shown in figure 3.11.

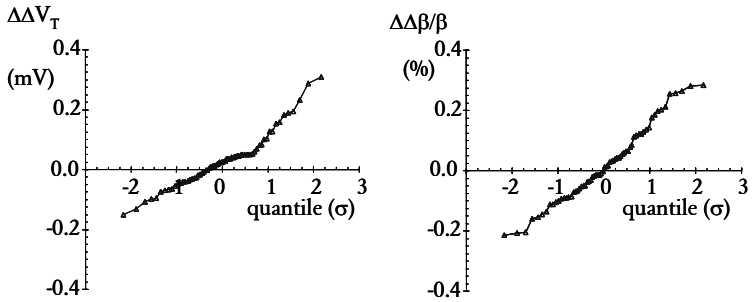

Figure 3.11 STR assessment type i. Cumulative probability plots of $\Delta\Delta V_T$ and $\Delta\Delta\beta/\beta$ derived from measuring a population twice.

To first order, these normal scaled probability plots appear reasonably straight lines, indicating the distributions are more or less Gaussian, be it somewhat more so for the beta than for the threshold voltage. The puritan statistician will (no doubt) find food for thought here, but at the low-level for this example ($< 100\ \mu V$), this is not relevant for this parametric mismatch study.

The main disadvantage of this STR determination technique is that there is a relatively long time interval between the observations of both distributions, as one has to wait at least an entire measurement session before the second test can be started. This may give rise to a systematic difference ($\mu_{\Delta\Delta P}$) due to drift of the measurement equipment and the prober/chuck/wafer. In the example discussed above, the recorded temperature drift was checked to be below the resolution of the micro-chamber sensor ($< 0.1\ °C$).

The major advantages of the 're-measure population' STR determination technique are that it is simple and does not require any changes or additions to the measurement program. Furthermore, it does not consume additional measurements (time) when one is not interested in (or worried about) the STR. Finally, it forms a good representation of all aspects of the measurement algorithm since it also involves prober movements, and inherent fluctuations of probe needle to contact pad resistance fluctuations.

ii. The re-measured single pair approach

An even simpler approach for assessing the short-term repeatability performance of a particular measurement system/algorithm is to run the standard measurement program (N times) on one particular pair by suppressing prober movements. Again, no measurement / data analysis program adjustments are required. Using this approach, a single pair is treated as the entire population, which means that the regular median and standard deviation estimators are automatically calculated. Obviously, the median in this case is not necessarily zero, as one is simply measuring one sample from the population. The obtained standard deviation is a direct measure for the system/device noise contribution.

	V_T mismatch	Beta mismatch
Median : $\mu_{\Delta P}$ (not relevant)	-0.276 mV	-0.293%
Standard deviation : $\sigma_{\Delta P}$ ($=\sigma_{syst}$)	31 μV	140 ppm

Table 3.5 Extraction of short-term repeatability using one pair

As an example, results are shown of measuring (the last) pair of a population of 66 W/L = 10/10 N-channel MOSFET's from the same wafer as the example discussed above. The results are summarised in table 3.5, the corresponding cumulative probability plots are shown in figure 3.12. Note that in this technique, $\sigma_{\Delta P}$ is equal to σ_{syst} as the same number of measurements is used as for the mismatch measurement.

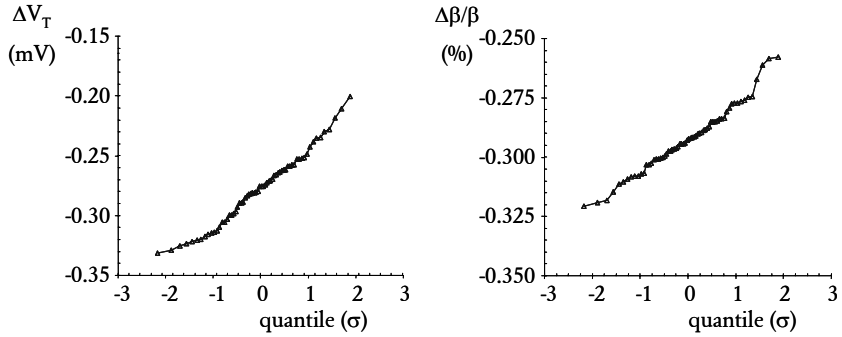

Figure 3.12 STR assessment type ii. Cumulative probability plots of ΔV_T and $\Delta\beta/\beta$ of a single pair measured 66 times.

The standard deviation numbers from table 3.5 are again (more than) reassuringly low, suggesting that there is ample short-term repeatability for almost any type of MOSFET using the tested measurement system / algorithm combination. The numbers are in fact significantly lower than those obtained using the previous method (table 3.4). This is not further investigated at this point, but could for instance very well be attributed to the fact that the transistors as used for method i. (W/L=40/0.24) have a significantly smaller area, hence larger noise. Moreover, the drain currents of the transistors of the example for method i are about 2 orders of magnitude higher. This means that the impact of probe needle to pad resistance fluctuations, that do play a (minor) role when stepping from die to die, may have contributed quite significantly in the former example, while they do not show up with method ii (no stepping & lower current!).
Note that the single pair technique can only be applied when both elements of the matched pair are probed simultaneously. When the test structure and/or the measurement system is based on a sub-site step between the two elements of the (see Chapter 2), this technique cannot be used, as the required number of steps (66 in this case) would damage the pads so severely,

that the later measurements become useless due to probe-to-pad contact failures.
The main drawback of method ii is that (by definition) no information on the contribution of the probe needle to pad contact resistance fluctuations can be obtained. By combining results from methods i and ii on pairs from one population, it should in principle be possible to separate these contributions.

iii. The DUT 1-2-1-2 technique

A third method that is applied regularly in our studies, is based on measuring the mismatch of each pair twice, each time the probe needles are placed on a pair. This method is particularly well suited for algorithm/system testing and searching for improved repeatability algorithms, or when characterising ultra small mismatch numbers. In the latter case, one can benefit from the inherent availability of the short-term repeatability to correct the observed standard deviation for possible system or device noise contributions. For the DUT 1-2-1-2 method, at each die a $\Delta P_{i,1}$ as well as a $\Delta P_{i,2}$ and hence a $\Delta\Delta P_i$ are obtained. This gives the population of $\Delta\Delta P_i$'s that is used to estimate the STR when the wafer is measured. Contrary to the previous two methods, this technique requires measurement algorithm changes, as the STR assessment must be an integral part of the algorithm. It involves more calculations, extra array space and additional statistical analysis. Of the methods considered so far, this method is least susceptible to equipment and/or temperature drifts, as the time between the two mismatch assessments is minimal. The resulting $\sigma_{\Delta\Delta P}$ must be divided by $\sqrt{2}$ to obtain the (σ_{syst}) system contribution.

This method is demonstrated using results from a poly-emitter NPN BJT mismatch assessment experiment with a population size of 85 samples. The 10x1 μm^2 (LxW) devices were placed in scribe-lane compatible CE&CC modules (figure 2.6). The measurements were standard Common Base measurements with a V_{EB} of –0.77 V resulting in typical collector and base currents of 67 μA and 0.69 μA respectively.

	$\Delta I_C/I_C$ mismatch	$\Delta I_B/I_B$ mismatch
Mismatch : $\sigma_{\Delta P/P,obs}$	1.8%	6.0%
STR: $\sigma_{\Delta\Delta P/P}$ ($\sqrt{2}\ \sigma_{syst}$)	110 ppm (0.011%)	330 ppm (0.033%)

Table 3.6 Example of combined mismatch and short-term repeatability measurement on poly-emitter NPN transistors by repeated measurements on each die.

Table 3.6 summarises the obtained mismatch fluctuation standard deviations and the method iii STR results for both the mismatch of collector and base currents. With $\sigma_{\Delta I/I,obs}/\sigma_{syst}$ ratio's of over 200, this particular measurement system/algorithm demonstrates excellent short-term repeatability performance for this particular technique, leaving plenty of room to assess the mismatch fluctuation standard deviations of considerably larger emitter area devices.
Note that a collector current mismatch standard deviation of 1.8% corresponds to an equivalent V_{be} mismatch standard deviation of about 0.47 mV. Moreover, the 0.011% STR implies that this was assessed with a measurement system induced V_{be} uncertainty of no more than 3 μV!
The corresponding cumulative probability plots of $\Delta\Delta I_C/I_C$ and $\Delta\Delta I_B/I_B$ are shown in figure 13. The significantly worse base current STR is probably attributable to the fact that the base current is two orders of magnitude lower than the collector current, hence measured in a lower meter range that is apparently more prone to noise.

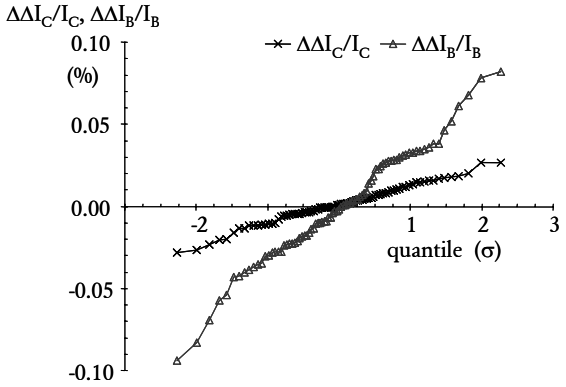

Figure 3.13 STR assessment type iii. Cumulative probability plots of $\Delta\Delta I_C/I_C$ and $\Delta\Delta I_B/I_B$.

The main advantage of the DUT_1-2-1-2 method is that the short-term repeatability information always comes along with each mismatch distribution. This can prove very useful as watchdog. For the majority of the populations, the information is of no consequence, as the repeatability of a well-constructed mismatch measurement algorithm is usually more than adequate. On the other side, if an unexpected high standard deviation appears, the first (re-assurance) check is the STR, to verify whether something went wrong during the measurements.

That measurements do go wrong occasionally is demonstrated by the following example. A 96 sample (WxL=10x0.8) double-poly matched pair population was measured using the same measurement system/algorithm as discussed above. V_{be} was set at –0.74 V, resulting in typical collector and base currents of 11.4 μA and 0.27 μA respectively. The resulting $\sigma_{\Delta\Delta Ic/Ic}$ and $\sigma_{\Delta\Delta Ib/Ib}$ are listed in table 3.7. Although the current levels are quite comparable to the previous example, the short-term repeatability standard deviations are more than an order of magnitude worse.

	$\Delta I_C/I_C$ mismatch	$\Delta I_B/I_B$ mismatch
$\sigma_{\Delta\Delta P/P}$ (before outliers removal)	0.39%	0.25%

Table 3.7 An example of a warning signal from the short-term repeatability estimator that something went wrong during the measurements. Compare to table 3.6 for expected performance.

The initial concern at this point was that this strong STR degradation could have been due to the rather unfortunate choice of the collector current, which in this case is uncomfortably close to a range transition of the current meters. Figure 3.14 shows however, that in this case the poor STR was cause by a few obvious outliers.

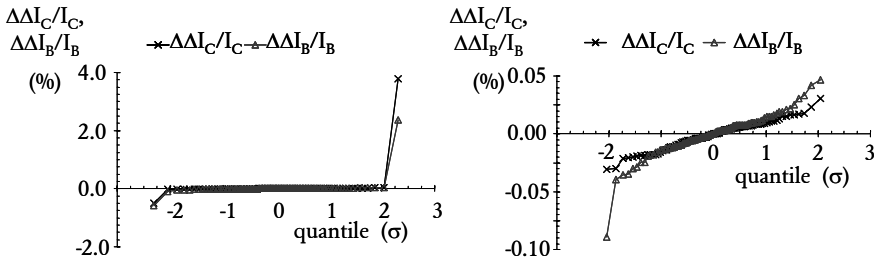

Figure 3.14 STR assessment type iii. Cumulative probability plots of $\Delta\Delta I_C/I_C$ and $\Delta\Delta I_B/I_B$ before (left) and after removal of highest and lowest observations.

Both for the collector current as well as for the base current STR graph, a clear high and a low outlier occurred. Note that a few-percent outlier is disastrous in terms of short-term repeatability, while it would probably go un-noticed in a general parametric test. With the repeatability available for each pair, it becomes quite easy to discard the two outliers, resulting in the STR cumulative probability plot on the right of figure 3.14. In fact, in this case a third outlier becomes apparent, be it that this one only occurs in the base current. After removing also this observation, the actual system/algorithm induced short term repeatabilities come back to respectable values of below 0.02% (table 3.8). The causes for such outliers will practically always remain guesswork, as they usually do not repeat upon re-testing. In this case, probing problems does definitely not cause it, as both measurements for the $\Delta\Delta P/P$ determination were done during the same probe-down. Most likely, mains power net disturbances generated by neighbouring equipment cause such deviations. Note that the scale of the observed outliers is quite comparable to the spikes that were encountered in figure 3.6. This type of disturbances is discussed in more detail, later in this chapter.

	$\Delta I_C/I_C$ mismatch	$\Delta I_B/I_B$ mismatch
$\sigma_{\Delta\Delta P/P}$ (after outliers removal)	0.012%	0.015%

Table 3.8 Short-term repeatability estimator after removing outliers.

Other studies where this built-in short-term repeatability assessment technique proved valuable, was when BJT matched pairs were characterised that were (on the edge of) oscillating. If all went well, this should have been avoided by carefully checking the I-V characteristics, but sometimes one is a little closer to an oscillation edge (or a range transition) than anticipated. Moreover, due to parametric gradients and parasitic capacitance differences across a wafer, transistors may oscillate on one side of the wafer while they remain quiet on the other. Oscillating transistor were indeed found a number of times to respond to the short-term repeatability check algorithm with a significantly worse short-term repeatability.

The main disadvantage that can be attributed to the algorithm as sketched above, is the additional (doubled) measurement time for each pair. Particularly on our HP4156 based measurement station, switching-over from one measurement set-up to the other in the IBASIC program, including some bias settings via GP-IB commands proves relatively slow. The typical time to measure a pair of BJT's (both base currents as well as collector currents) adds up to about 20 seconds on this system. This practically doubles for the in situ (type iii) repeatability measurement. Such measurement times may place a significant burden on tester time.

Forty seconds per pair for a typical population of 60 to 90 pairs brings the total measurement time for one device geometry to 40 to 60 minutes. When quite a few different geometries are to be characterised (with several interesting batch splits in the box), one is easily tempted to half the measurement time by skipping the short-term repeatability measurement. Another disadvantage of this method is that the estimated STR does not include the fluctuations attributed to probe-needle-to-pad resistance fluctuations, as the needles generally don't move between the two measurements on a particular pair, although this could easily be built into an algorithm should this be considered desirable.

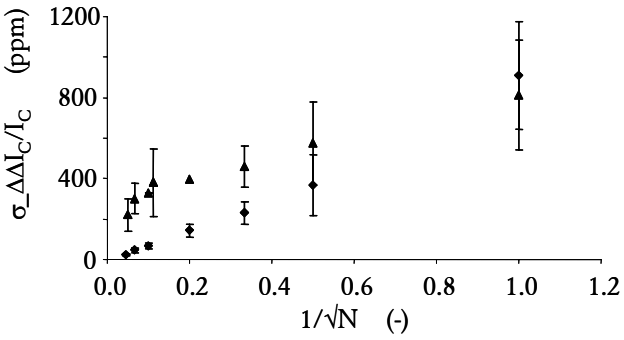

Figure 3.15 STR as a function of the number of observations N used for each measurement. Whereas the STR for the DUT(1-1-2-2)$_N$ algorithm (diamonds) follows the $1/\sqrt{N}$ behaviour down to the tens of ppm's regions, the traditional DUT(1-1)$_N$-(2-2)$_N$ method (triangles) saturates around 200 ppm.
Error bars represent the (bootstrap) experimentally determined statistical uncertainties.

iv. The DUT $(1\text{-}1\text{-}2\text{-}2)_N$ technique

As suggested before in this thesis, and discussed in more depth later in this chapter, it is often possible to boost the precision of mismatch measurement algorithms through repeated measurements of each device. However, as measurement repeatability improves theoretically with the square root of the number of observations, two orders of magnitude more measurements are needed to reach a factor ten better STR. Such large numbers of observations are often impractical due to their excessive time consumption. Measurement times can easily run up to 5 to 10 minutes per pair when a few hundred observations are used. Hence, this measure should only be considered for extremely demanding (large device) pairs. Moreover, in practice such long measurement times do not necessarily result in better STR's. Temperature induced drifts and EMC disturbances of devices and/or equipment will limit the STR at these time scales. On our HP4156-based system, this proved the limiting factor to reach the best possible STR, which in practice generally ended somewhere in the neighbourhood of about 100 ppm (0.01%). As this level is in fact more than adequate for most mismatch measurements, this barrier was not relentlessly pursued on this system. With the introduction of the more versatile Keithley 4200 system, it proved feasible to take the STR performance significantly further (figure 3.15). This figure is copied from [Ewert05] in which we discuss the possible STR improvement, as well as the limitation due to the time lag between repeated measurements. In this paper, we compared two STR assessment methods that can be identified as DUT $(1\text{-}1)_N\text{-}(2\text{-}2)_N$ and DUT $(1\text{-}1\text{-}2\text{-}2)_N$ respectively. In the former, device 1 is measured 2N-times, followed by 2N measurements of device 2. N denotes the number of measurement repeats. Each device is measured twice, yielding two sets (of N measurements) of P_1 and P_2, hence two sets of ΔP_i's and one set $\Delta\Delta P_i$. The problem of the DUT $(1\text{-}1)_N\text{-}(2\text{-}2)_N$ method is that when N gets large, the time between the measurements on device 1 and device 2 becomes too long to neglect temperature and equipment drifts. In the latter method (DUT $(1\text{-}1\text{-}2\text{-}2)_N$), devices 1 and 2 are each measured 2 times sequentially, while this sequence is repeated N times. The impact is demonstrated in figure 3.15. Note that the DUT $(1\text{-}1\text{-}2\text{-}2)_N$ method yields an STR improvement curve that scales nicely with the inverse of the square-root of the number of observations (down to sub 50 ppm STR's), while the DUT $(1\text{-}1)_N\text{-}(2\text{-}2)_N$ method clearly saturates above 200 ppm.

Conclusion

STR assessment forms an indispensable element of the development of new mismatch measurement algorithms, as this provides the possibility to distinguish between the actual device mismatch and measurement fluctuations that are attributable to the measurement system. The STR determines the lower limit of the mismatch standard deviations that can realistically be obtained with the measurement system and used mismatch measurement algorithm. Moreover, STR assessment can also be used to monitor the stability of the measurement system even when it is used well below its accuracy specifications, as is often the case. This section discusses four STR assessment techniques with their merits and limitations. Two of these require off-line data analysis, while the more advanced ones are integrated into the measurement algorithm and data analysis. The choice as to which technique is most appropriate depends on the requirements and possibilities. In practice, the decision will always be based on the trade-off between the required (extra) measurement time, versus the manpower that must be invested into the design and implementation of new measurements/analysis algorithms. In fact, the main conclusion is that it is more important to do regular STR checks than exactly which technique is used. The ideal solution, which was implemented in most of the mismatch assessment algorithms as used in this thesis, is when the STR assessment is integrated into the mismatch measurement algorithm. This allows continuous monitoring of the system's performance, providing extra confidence in the mismatch estimators when the STR estimators are sufficiently small, and immediate feedback when hardware problems or measurement disasters, such as poor probe contact, seriously affect the obtained estimators.

3.4 Matched pair measurement algorithm considerations

When algorithms and bias conditions are chosen with care, mismatch measurements can generally be improved considerably, or at least it can be avoided that certain system peculiarities deteriorate the STR and accuracy performance of mismatch measurements.
Therefore, a number of measures, considerations and solutions for realising high precision DC parametric mismatch measurement algorithms will be discussed.

Source and meter ranges

For high precision mismatch measurements, it is extremely important to know the exact properties of the measurement system, particularly into which physical ranges the sources and meters of a system are divided. This must help to avoid that mismatch measurements are deteriorated by taking some readings on one side of a range transition while others are taken at the other side, or that range transition artefacts affect the measured results of one of the supposedly equal devices. Typically, range transitions occur in decades. Vendors and systems differ with respect to the exact transition points. Examples were encountered of meters switching over around the 1, 10, 100, or 2, 20, 200, or 4, 40, 400, or 5, 50, 500 readings. Range transitions are usually well documented in the measurement system documentation. However, sometimes surprises do occur in this respect. An example is discussed in [Schm01], where we found that a particular (Keithley 400) tester actually switches at a 5% lower level than reported in the system documentation. Other meters were found to switch in fact at the “1.05“ levels. On another system, the Keithley 4200 SCS bench-top semiconductor characterization system, current meter range transitions are at different levels (0.5, 5. 50, etc.) when the meters are used in auto-ranging, compared to when fixed range settings are used (1, 10, 100). Moreover, it must be realised that in auto-ranging mode meters switch range at a different level when they range up compared to when they range down. This hysteresis is built in to avoid range oscillations for measurements at the range transition point.

Equipment manufacturers naturally do their utmost to hide range transitions through accurate calibration and hardware as well as firmware measures. Nevertheless, range transitions are often detectable by performing a simple sweep measurement across a decade. If the current readings do not display a visible step (which they often don't, especially on log-scale plots), the best way to reveal the range transitions is by taking a numeric derivative dI/dV of the obtained curve. The max-g_m plot as derived from the linear region transfer characteristic with small V_{GS} step size (figure 3.16), proves a suitable graph for monitoring range transitions when characterizing MOSFET's.

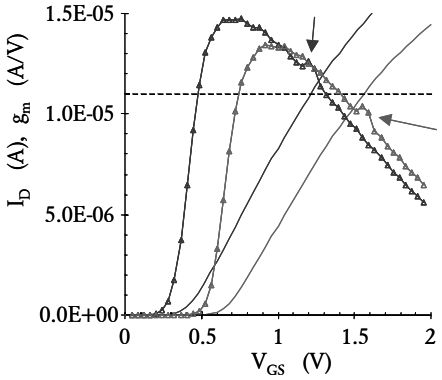

Figure 3.16 Example of a range transition artefact in the linear region transfer graphs for MOSFET's at two substrate biases. A (0.5%) offset in the higher range, around the 11 μA range transition, is practically invisible in the current, but yields a hump for the derivative (gm).

Problems at range transitions are generally attributable to offset and/or gain differences in the instrumentation of the sources and meters. In the case of figure 3.16, an (artificial) offset of no more than 0.5% was added to the readings above 11 μA. Such an error could give rise to a substantial increase of the apparent pair mismatch when one of the devices of the pair is characterised a just above 11 μA while the other is measured just below 11 μA. Regular system calibration helps to avoid problems due to range transition offsets.

Another example of a measurement hardware related issue is depicted in figure 3.17. In this case, the spikes (or gaps) correspond to three current meter range transitions for the drain current measurement, at 0.1, 1 and 10 μA respectively. This particular problem was associated with a (0 V) SMU, connected to the Source of the transistor in which the current was also measured during this experiment. The artefacts disappear when the Source current is not measured (figure 3.17, right). This could indicate a timing problem in the ADC, but more likely, this can be attributed to a minor voltage drop across the SMU. The h_{FE} characteristics (I_C/I_B as a function of V_{EB}) also are very useful graphs to help spot range transition artefacts as well as oscillations for BJT measurements.

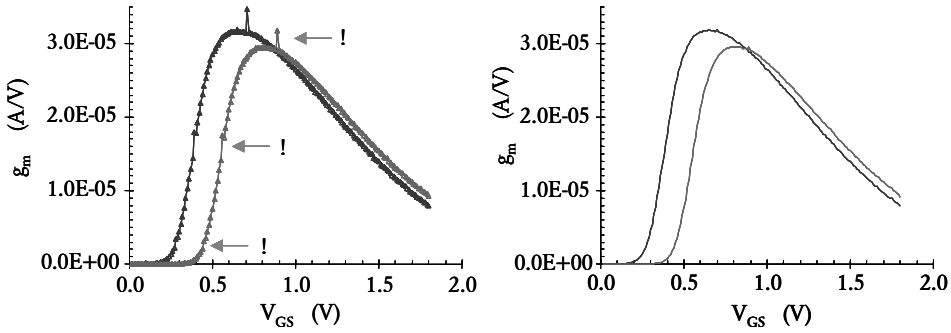

Figure 3.17 Example of range transition artefacts in the MOSFET linear region drain current (gm) graph (left). By changing the measurement algorithm, the artefacts disappear (right).

Hardware switching artefacts in measurement systems are particularly likely to surface in sweep measurements across a large number of current decades. Such transitions also reveal themselves as spikes in the curves. An example that clearly reveals a range transition artefact is depicted in figure 3.18. The Gummel plot of the NPN transistor (left) shows no sign of conspicuous behaviour, but the h_{FE} plot clearly demonstrates that one should stay away from the V_{be}=0.58 V bias point. A good test for such hardware-induced spikes is to verify whether they can be affected (reduced) by increasing wait- and/or integration times of the measurements. In the case of figure 3.18, such measures had no effect. The spike in this case is probably attributable to the relay that bypasses the pre-Amp of the Keithley 4200 SMU. A useful indication is to check whether a spike just involves one data point (as in figure 3.17 and 3.18) or more (as in figure 3.16). The former is most likely related to a hardware settling or switching issue.

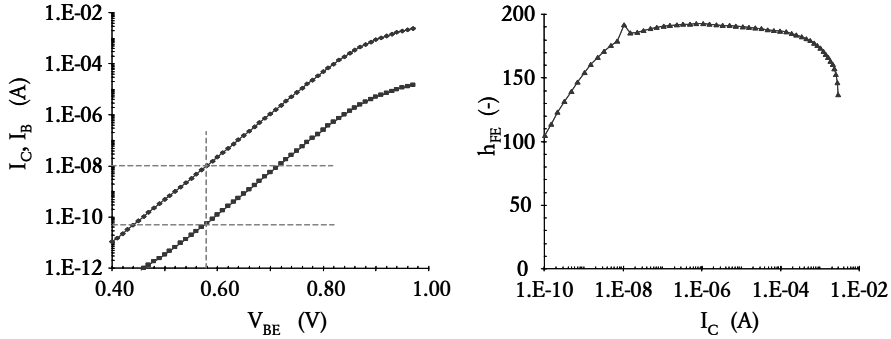

Figure 3.18 Example of a range transition artefact in the h_{FE}-plot for an NPN BJT. The spike coincides with the 50 pA range transition of the base current measurement.

Another occasionally encountered problem is that bipolar transistors begin to oscillate in a particular range, while they were quiet in the range below. It is easily imaginable that this can be attributed to changes of the impedance levels of meters and sources, which, in combination with the transistor, create the positive feedback (oscillation) condition. Figure 3.19 presents an example of a BJT measurement that can yield undesirable surprises when the transistors are characterised at relatively high current levels. Whereas the characteristics behave quite decently on one side of the wafer (open symbols), the same transistor clearly starts to oscillate at another position on the wafer (solid symbols), while the I-V characteristics appear identical for low currents.

Source and meter offsets

For device measurements well below 1%, or of the order of 100 μV, offsets in measurement instrumentation are generally not negligible. Good and regular calibration of measurement equipment is important to maintain the instrumentation in optimum condition, but instrumentation offsets of the levels of a few tens of microvolts are practically unavoidable in most parametric measurement systems. In principle, such offsets do not always have to pose problems. If, for instance, a current meter or voltage source is used in an identical fashion (same bias, range and compliance) by both elements of the pair (and hence by the entire population of pairs), its offset is virtually of no consequence for the observed mismatches. Through choosing the appropriate test structure, this condition can be exploited (chapter 2 of this thesis).

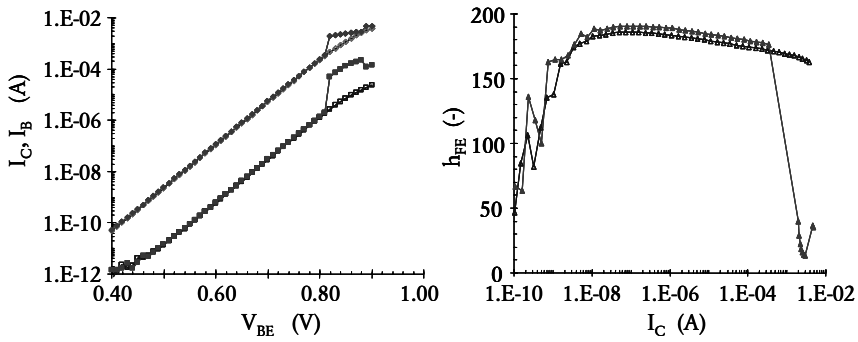

Figure 3.19 Example of Gummel and h_{FE} plots for two transistors of a population. Whereas one transistor (open symbols) remains quiet over the entire measurement range, another member of the same population (different place on the wafer; solid symbols) starts to oscillate at a collector current level of 500 μA.

Instrumentation offsets usually remain reasonably constant, once the instruments have been switched on for at least two hours to allow them to reach their steady state temperature and the system has done it's internal calibration. By regularly monitoring these offset voltage drifts we found that they can generally be considered as constant (at least within 10 - 20 μV) during a typical measurement session on our system [Tuinh00a, Tuin98]. The actual value of the offset depends on the system. Whereas measurements with the good-old 4145 parameter analyzers used to be hampered by offsets of the order of up to hundreds of microvolts, we found that its successor (Agilent HP4156A) typically yields voltage offsets in the tens of microvolts (figure 3.20 left) In this graph, the Voltage offset between two (Base) SMU's is depicted. These data were collected during several subsequent BJT population mismatch characterisation sessions. Each point corresponds to the SMU offset (both SMU's at COMMON) prior to measuring the pair. The offsets are measure with built-in microvolt meter using additional needles on the base pads. On the right, a comparable measurement is shown for a Keithley 4200 based measurement. Base SMU's both at +1 mV, actual voltage biases are measured using the SMU's own ADC's.

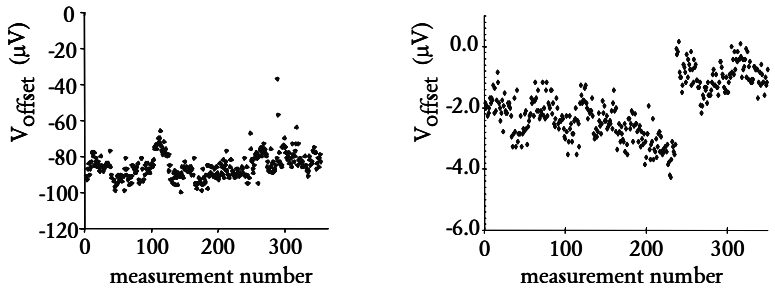

Figure 3.20 Examples of voltage offsets between two Base SMU's during CE&CC matched BJT pair mismatch measurements. Left: HP4156A; Right: 4200-SCS. Note that the two graphs have different vertical axes scales.

Voltage offsets in the measurement circuit result in a systematic component in the mismatch distribution. It depends on the type of device study whether such systematic mismatch observations can be neglected. For small device pairs, where the random component of the mismatch is generally large, one can usually neglect the systematic component associated with the instrumentation offsets. For large components, instrumentation induced systematic mismatches will show up relatively more pronounced.

For very critical studies, e.g. for those where the impact of surroundings related disturbances is studied, some special tricks can be applied to verify whether the observed systematic mismatch is due to the instrumentation. A useful exercise is to repeat the measurement of a population with suspected systematic mismatch but with interchanged transistors. The idea is to let the system (the measurement and analysis program) 'think' it is measuring one transistor of a pair, where it is actually biasing and measuring the other. On a system with manual manipulators, this is easily done by simply swap the positions of the needles. Sometimes this can only be achieved by rotating the wafer. Another method that we have applied regularly is by exchanging SMU cables, hence leaving the probe needles in their original positions. On measurement stations with fixed probe cards and fixed cabling, this is obviously not possible. If the cable- (or probe-) switch can indeed be applied, the result of the mismatch estimation of the complete population of pairs should yield an equal but opposite systematic mismatch if it is indeed caused by the devices. If the systematic mismatch component has the same sign and magnitude for both distributions, the systematic mismatch is caused by the measurement instrumentation.

A mixture of systematic device mismatch and system offset results in observed medians that do not have the same magnitude after interchanging the devices. A useful technique to investigate the capability of a system to characterise systematic mismatches is to add a small but significant intentional offset in a particular set of matched pair test structures. An example of this was discussed extensively in [Tuinh00a], where we intentionally made MOSFET pairs with +/- 1% dimensional offsets (10/10 matched with 10/10.1 and 10/10 matched with 10/9.9).

Alternative techniques to cope with a voltage offset are based on actually measuring the offset, and correct the observed mismatch for the measured source offset [Tuin98, Tuinh00a].
This can be done either for each pair, or just once for an entire population. As discussed more in depth in [Tuin98] this proved particularly relevant for BJT mismatch characterisation, while we also demonstrated its feasibility for characterising subtle current factor mismatches in MOSFET's [Tuinh00a]. In the HP4156-based system, this was realised through a second pair of needles on the base pads (CE&CC BJT's) or drain pads (CS&CG MOSFET's) to measure the difference between the respective ground levels of the SMU's (figure 3.20 left).
The Keithley 4200 system has a significant advantage in this respect, as it provides the possibility to actually measure (with a 22 bit ADC) the output of the voltage sources (16 bit DAC's), see figure 3.20 (right).

When it comes to source and/or meter offset cancellation possibilities, parametric test stations equipped with switch matrices have a major advantage over those without a matrix.
When using a full fledged parametric tester, it is normally spoken relatively easy to built-in features like swapping sources, flipping high and low connections, reversing bias polarities and current directions, etc. into the measurement algorithms [Killm]. Such measures are generally not used in standard parametric test libraries as the achieved improvements are often hardly worth the extra costs in terms of measurement time (except for high precision measurements or typical low voltage measurements like metal VanderPauw or via contact resistance measurements). Moreover, a measurement system within specs is supposed to be accurate enough for most standard parametric test work. For specific high precision mismatch measurements, on the other hand, such refinements can prove useful indeed.

A final remark concerning offset cancellation has to do with the so-called auto calibration feature of measurement systems. Systems like the HP41xx semiconductor parameter analyzers by default perform regular self-calibrations during (or rather in between) measurement sessions. This is of not much consequence for most standard device assessments using bench top measurement stations, but this can create nasty surprises during lengthy mismatch characterisation measurements as this may severely impact mismatch observations. Self-calibration is executed at regular intervals (typically every half hour). HP parameter analyzers do this by adjusting the common ground (offset) level as well as the gain of each individual SMU. For the HP4145, adjustments of up to a few millivolts were not uncommon, whereas in the more advanced HP415x family adjustments are encountered up to a level of +/- 100 μV. For Common-Base BJT measurements, adjustment of the "Common" is particularly devastating as this results in a change of V_{be}. If such an adjustment (for whatever reason) would occur during a mismatch characterisation session (in the middle of measuring a particular population), it could easily ruin the statistics. A significant change of the systematic mismatch within a single population will result in an increase of the standard deviation and a bi-modal distribution. Therefore, although this self-calibration seems well meant and is probably required to maintain the accuracy specs of the measurement system over longer periods, it is absolutely compulsory to switch-off auto-calibration for mismatch characterisation.

Multiple observations

As in practically any (engineering) field, the art of accurate semiconductor device measurements is built on a combination of science, history (experience) and a certain amount of gut feeling. Many good practices that are used in this field are remnants from older studies, often surviving via horror tales and archaic measurement algorithms. A typical example of such a practice that is not always equally well understood is the habit to measure a data point more than once. A genuine historic horror story argument is based on the belief that it is possible to improve the needle-to-pad contact by first forcing a current through the needle to burn or blow away the thin isolating layer on a contact pad or to open-up a poor contact in the DUT. Although there is no doubt that these phenomena did (or do) occur, it is not to be hoped that this draconic measure is required for any high precision mismatch characterisation study. It is also sometimes suggested that the dissipation of a measurement heats the device so that a second measurement is done at a more stable device temperature. However, as thermal time-constants in silicon wafers are of the order of microseconds, while normal measurement times run in the (tens of) milliseconds, it is quite unlikely that heating during DC measurements can contribute significantly to observed on-wafer measurement instabilities. Contrary to such horror

story arguments, several good reasons for using multiple measurements can be identified as being instrumental for achieving the optimum mismatch measurement precision performance.

Power line cycle integration mode measurements

In the first place, it is always recommendable to do high precision DC measurements in integration mode and choose the integration time in phase with the (mains) net cycle, as this significantly reduces the susceptibility to power net EMC disturbances. This implies integrating the measured signal over at least one Power Line Cycle (1 PLC = 20 ms @ 50 Hz).
The 'fast' or 'short' measurement system settings of bench-top semiconductor characterisation systems generally collect a single measurement in 3 to 10 ms. When the system setting is changed to 'medium' or 'normal' (1 PLC), this increases to about 25 to 65 ms per data point. As one generally has to count on total measurement times for high precision mismatch measurements of the order of 1 to over 40 seconds per pair, the impact of the extra 20 to 60 ms integration time per measurement point is generally acceptable. Integrating over one or more PLC's was shown to give significant improvements over shorter measurements when looking for measurement repeatabilities below 1% [Tuinh01a]. Multiple power line cycle (nPLC)-measurements are often available in standard parametric measurement equipment. 'Long integration' on an HP4156 implies integration over 16 PLC's. The 'quiet mode' on the Keithley 4200 relies on integration over three PLC's.

First data point exclusion

An odd example of the use of multiple reading algorithms for accurate mismatch measurements is probably just related to the instrumentation hardware and firmware of the A/D converter of the HP4156. When a time sample sweep is taken over several samples (using normal or long integration), it is regularly observed that the very first data point is significantly lower (about 0.015%) than subsequent readings (figure 3.21). This effect is probably caused by a slightly marginal delay choice or settling time for the ADC. An effect of this magnitude is negligible for most mismatch studies except for some extreme high precision device studies and layout feature artefacts such as described in [Tuinh02a]. Such slightly lower first point observations, mixed with some of the other 'just to make sure' arguments, like charging cables, filling-up of interface states in the device, etc, made us decide to always stick to the multiple reading approach for BJT and resistor mismatch characterisation. For MOSFET mismatch measurements, no evidence for the necessity of this measure was encountered so far. Nevertheless, we stick to this habit, either through multiple sample measurements, or by simply always starting a measurement voltage sweep at one voltage bias step below the actual range of interest.

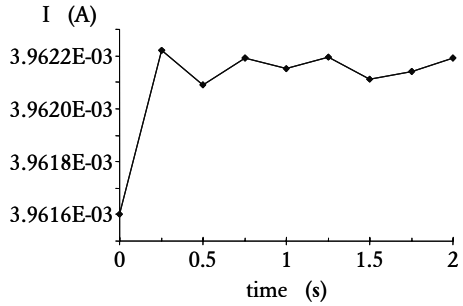

Figure 3.21 An example of a lower first meter reading (Note the y-axis scale).

Noise averaging

When parametric measurements are performed in a noisy test environment, it is generally accepted that one can reduce the impact of this noise on the observed parameters by taking multiple meter readings, and subsequently average over the accumulated observations.
If the noise is frequency independent, the uncertainty of the observation reduces with the square root of the number of readings (also see section 3.2). This was demonstrated quite extensively in our work with floating-gate capacitor mismatch test-structures [Tuin96a].
In that study, we demonstrated that a standard production parametric tester in a noisy test-lab environment could be applied to enable mismatch measurements down to 100-ppm levels. However, we had to rely on hundreds of repeated measurements to reach sufficient short-term repeatability to obtain reliable mismatch numbers for the large geometry (capacitor) pairs.
The disadvantage of such measures is that they generally result in very long measurement times. Apart from the time it takes to execute such long measurements, drift of the measurement system may limit the attainable mismatch measurement accuracy (section 3.1 of this thesis).

Typical numbers for noise levels as encountered during high precision DC measurements should be expected in range of 0.02 to 0.1% (figure 3.22). For small transistors, the contribution of the (1/f) noise and Random Telegraph Signals may pose a lower limit to the beneficial effect of repeated measurements [Tuinh01a]. Through careful construction of the measurement algorithm, it proves possible to reach sub 10 ppm STR's for large devices on our Keithley 4200. This approach was discussed in detail in [Ewert05] and the key result is summarised in figure 3.15 of section 3.2.

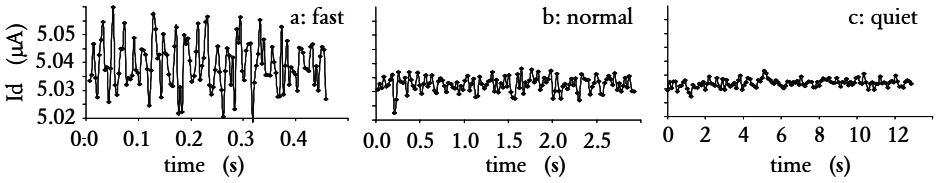

Figure 3.22 Example of drain current measurement for three different measurement system settings (fast, normal, quiet). Measurement times per data point are 3.7, 23.6 (1 PLC integration) and 103.9 ms respectively. These correspond to relative current fluctuation standard deviations of 1700, 550 and 290 ppm respectively.

EMC disturbances

In a general-purpose measurement lab, it proves practically unavoidable that a certain number of measurement readings are affected by power-line and EMC disturbances. In an energy intensive environment like an integrated circuit fabrication facility, where high voltage and/or high power equipment is continuously switching on and off, a substantial degree of power-line disturbances (and cross-talk through the air) is practically unavoidable. The surprisingly large range of disturbances that are picked-up by a measurement system in a fab environment is for instance demonstrated in [Schm01]. A notorious DC measurement deteriorator is a microscope power supply of a neighbouring measurement system in the same lab. Simply switching a microscope lamp on (or off) does often result in a significantly higher or lower current reading. An example of this was in fact shown earlier in figure 3.6 of this chapter. Figure 3.23, is a zoom-in on of the '–TCC spikes' of figure 3.6. Note that the observed spikes represent measurement errors of the order of 5 to 10%.

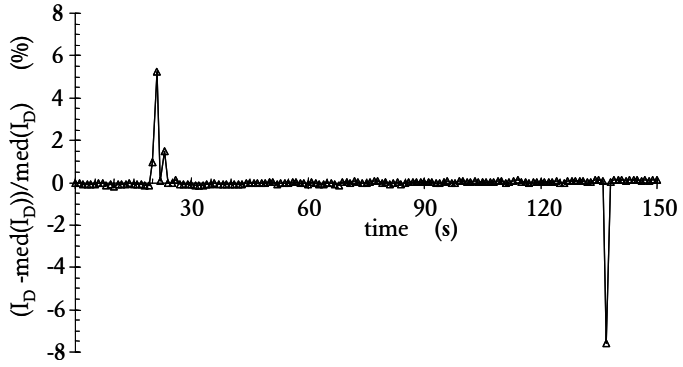

Figure 3.23 Current meter reading spike due to switching of a microscope power supply on a neighbouring test station.

In this example, indeed a colleague was doing device measurements using a manual probe station and flipping his microscope light on and off. Once this was recognised, a number of experiments on different measurement systems was performed to verify if they were equally affected by equipment switching of other stations in the same lab. All our 4155, 4156, and 4200 systems, with various types of probers, suffer from the kind of observations a depicted in figure 3.23. Spikes with the same signature were also made through electrostatic discharges. When wearing a synthetic sweater, it was observed that simply stepping out of an office-chair could create an (audible) spark, powerful enough to disturb common BJT measurements. The good news of such spikes is that they usually affect only one data point. This was verified in additional experiments through deliberately flipping a microscope light on and off during comparable sweeps (with various integration conditions). This single data point disturbance effect implies that a multiple measurement scheme with additional data filtering can work quite effectively for avoiding the impact of such peaks.

A more severe measurement disturbance is depicted in figure 3.24. This example shows the impact of a GSM phone on a DC base and collector current time-sweep for a CE&CC matched pair biased in Common base measurement configuration. The (1 PLC) measurements were collected roughly every 43 ms during a total period of about 3 minutes. Initially, the measurement was started and left to settle, after which a phone call was made using the conventional (wired) phone inside the measurement lab to a GSM phone. The receiving phone was about 10 metres (a corridor and two rooms) away from measurement station when the call was made. At around the thirtieth second the phone responded, and so did the measurement

system! The peaks in the current reach a level of about 1 to 2% increases (see lower left expansion). The standard deviations of the current fluctuations are estimated at 0.3 to 0.4%. Subsequently, the phone was carried to the measurement room. In the period between 60 and 100 seconds, the call was continued in the measurement room close to the probe station. Current increases of up to 10% are observed during this period. Note the asymmetry of the signal. Due to the non-linear (exponential) voltage dependence of the transistor, the noise reveals itself as a current increase. This is a good indication that the noise signal is picked-up by the transistor under test, and not in the (Keithley) measurement system. When the phone call is ended, the noise levels drop back to quite acceptable 0.02% standard deviations (lower right expansion).

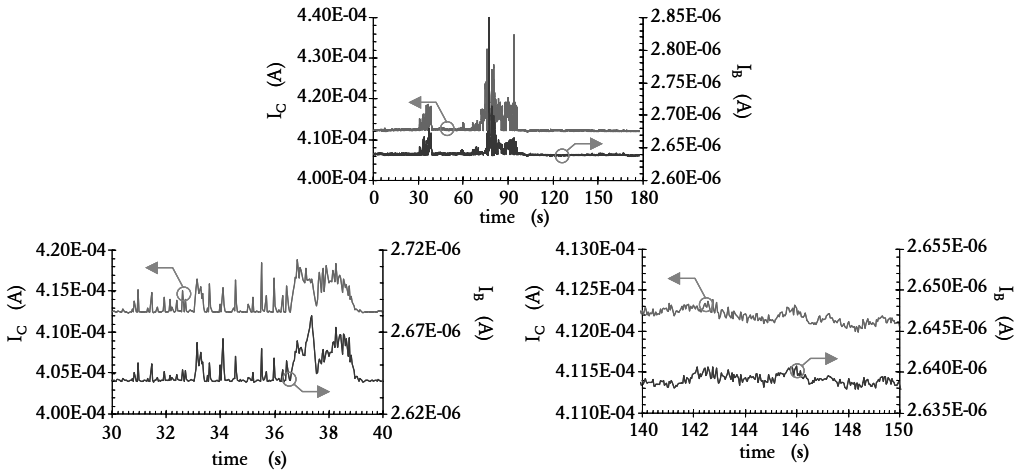

Figure 3.24 Impact of a GSM phone call on a BJT measurement.

Multiple observation measurement algorithms form a relatively good protection against many EMC disturbances. When a number of observations of the same measurement are available, statistical analysis techniques can be used to filter the disturbances away. Obviously, it is practically impossible to safeguard against somebody holding a mobile phone conversation near a high precision measurement system, but many of the smaller single-event disturbances can be dealt with quite effectively. The following section describes the M9S5 algorithm that forms the workhorse of most of our high-precision mismatch studies.

The M9S5 measurement algorithm

Based on many studies and STR comparisons of different algorithms, we have found that it proves beneficial to build our high precision parametric mismatch measurements on a multiple observation algorithm. However, having decided for this, there still is the question how to treat the statistical evaluation of the collected observations. There are several possibilities.
The most common approach is to calculate a simple average of the collected observations. This is for instance used in [Tuin95] for reaching sub 100-ppm short-term repeatabilities of capacitor mismatch measurements on a standard Keithley S450 parametric production tester. The disadvantage of averaging is that the calculated mean is relatively strongly vulnerable for EMC spikes as shown in the previous section. As many as 1000 observations would be required to bring a single 5% spike down to an error level of 50 ppm. This is a rather fruitless approach, as the chance of catching a multiple spike increases due to the length of the sampling (see figures 3.23 and 3.24). A much more robust technique therefore is to use median selection rather than averaging.

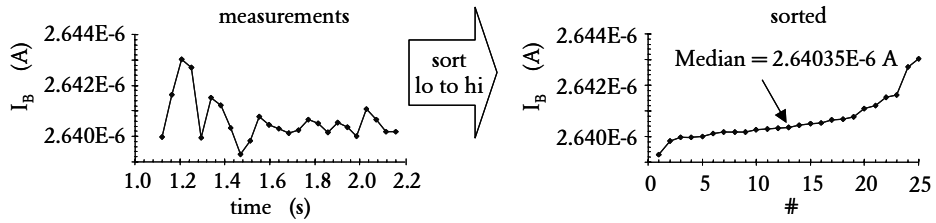

Figure 3.25 Example of an M25S13 measurement point selection.

This insight led us to adopt the so-called MXSY measurement approach, which is applied for practically all high precision mismatch measurements discussed in this thesis.
The algorithm Measures X samples of a particular measurement point, sorts the data low to high, and subsequently Selects the median (Y-th point, with Y = INT((X+1)/2)). Figure 3.25 demonstrates the algorithm for an arbitrary M25S13 example.

In the implementation of our mismatch measurement algorithms, we always provide the possibility to vary X. In practice we used values of X=5 to X=99 on the HP4156 and X=1 up to 499 on the Keithley 4200 SCS (see figure 3.15). X is generally chosen as an odd number. This gives an unambiguous median estimator, which represents a real measured value.
With an even population size, most median estimation algorithms will calculate the average of the middle two observations. For most studies reported in this thesis, we used the M9S5 version of this algorithm. M9S5 provides good protection against outliers. On an HP4156, the time for collecting the nine readings typically adds up to 1 to 5 seconds (figure 3.26), depending on the integration time and delay between the readings. The additional uploading of the results via the GP-IB bus takes about 5 seconds. On the Keithley 4200, the nine (1 PLC) measurements effectively take a little over half a second (partly due to the internal ADC calibration).
The required time for uploading of data is negligible (micro seconds) as this involves a fast internal bus and a C-program.

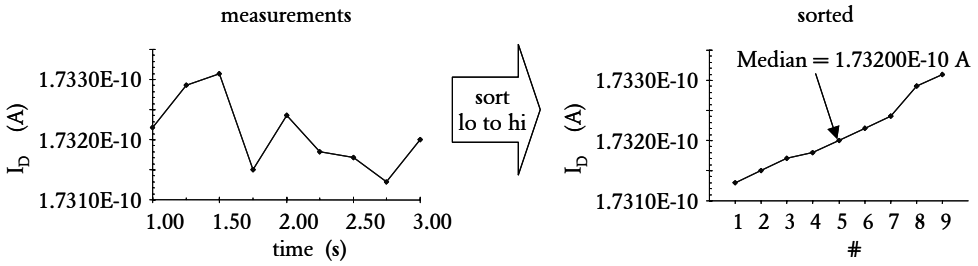

Figure 3.26 Example of an M9S5 measurement on an HP4156.

The MXSY measurement algorithm theoretically provides the possibility to reach infinitely small measurement uncertainties. In theory, the measurement uncertainty should decrease with the square root of the number of used measurements. However, in practice it is our experience that it is not so obvious to reduce the measurement uncertainty significantly below 1000 ppm. The most likely reason for this is that during the, often lengthy, measurements for high X values, temperature drifts of the devices and/or the sources and meters become the limiting factors. Typical measurement precision numbers that are reachable on standard parametric measurement systems are of the order of 0.01 – 0.1% (see also section 3.2). On the Keithley 4200-SCS we implemented a more elaborate intertwined multiple reading algorithm that provides better protection against drifts [Ewert05]. Using this approach we were able to reach sub 10 ppm STR's for BJT's and even much better sub 1 ppm STR's for more linear devices.

3.5 Data analysis techniques for mismatch characterisation

"Lies, damned lies and statistics…" Statistics is a widely studied and documented art. Many good textbooks are available for those who want to sharpen their minds on fluctuating data sets of all possible nature or (must) get more information from less data. Despite this abundance of expertise on statistics, it is amazing (not to say annoying) to note the ignorance that is often displayed in publications on a statistical subject as matching. Take for instance the certainty that is often suggested by the number of digits behind the decimal point in publications on matching. Some authors do not hesitate to present mismatch fluctuation area scaling factors with a number of digits behind the decimal point that suggest a population sizes that are at least 4 orders of magnitudes larger than the ones they actually used. Despite effectives measures to improve the measurement accuracy as discussed in the previous sections, matched pair studies are practically always limited by a the statistical uncertainty as a result of the limited population size. Moreover, statistical estimators are often impacted by outliers as well as by the nature of their distribution. Hence, one should always be cautious and stay alert whether the calculated estimators do indeed describe the fluctuation behaviour of the studied observable.

The majority of the results as reported in this thesis were derived from populations of matched pairs evaluated per wafer**.** Our standard measurement approach, as presented extensively in [Tuin98] and [Ewert05], is to set-up the prober for a particular wafer pattern and subsequently aligning the needles/manipulators to contact a particular matched pair. The measurement program then steps through all the pairs on the wafer. When all pairs of this particular geometry are measured, the program analyses the collected population of observables (parameters) and mismatch observations in terms of their statistical estimators. After summarising and storing the results, the system is available for another population of pairs, implying re-aligning the needles and restarting the measurement program. This approach means that the standard evaluation unit is formed by the population of pairs of one geometry or layout, on one wafer.
An advantage of the chosen method is related to the possibility to evaluate both the parametric spread as well as the mismatch as a function of the position on the wafer. As will be exemplified later in this thesis, this can provide useful information about the mismatch mechanism. Furthermore, the chosen approach provides feedback points early on in the data collection process, as one is forced to collect and administrate the results of different populations one by one. When unexpectedly high mismatch numbers, or excessive numbers of discarded devices are encountered, one can immediately react by verifying the wafer map, checking the needle alignment, re-measuring the population, do short-term repeatability checks etc.

Most mismatch fluctuation studies require several dozens of populations to be measured and evaluated. Consequently, several thousands of mismatch characterisation runs as sketched above were completed over the past years. This explains why a relatively large effort was spent on devising a set of statistical evaluation tools that can provide reliable statistical estimators of a population of mismatch observations right after completion of the measurements. The following sections discuss practical techniques that were found useful to assure the highest possible confidence in the obtained estimators.

Safe standard deviation estimation

Usually, the parametric mismatch fluctuation standard deviation forms the most relevant parameter for mismatch characterisation as it is subsequently carried forward to the Pelgrom plot to determine the intrinsic process performance parameter with respect to mismatch fluctuations, the A-factor. Primarily to avoid that outlier measurements have a strong impact on the observed statistical mismatch estimators we have always used rather conservative estimation techniques. The term safe estimation is used for this pragmatic approach. This approach consists of the following five-tier procedure for statistical mismatch evaluation.

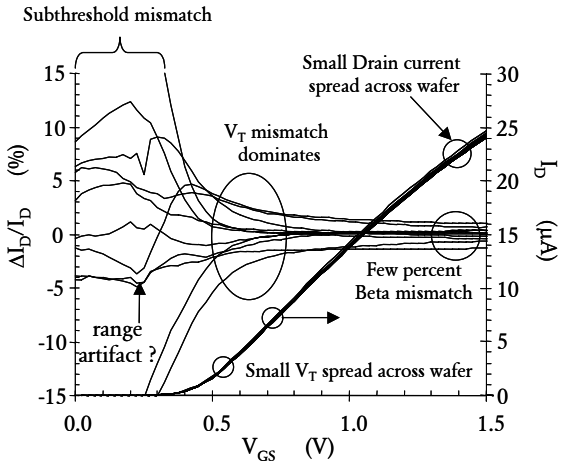

Figure 3.27 Example of linear region transfer curves and drain current mismatch sweeps. Note the three independent mismatch mechanisms in the mismatch curves. Beta mismatch, VT mismatch and subthreshold mismatch.

Tier 1: Look before you leap

An important initial step, before all pairs on the wafer are accurately measured and analysed, is to obtain a rough feeling about the spatial parametric variation as well as the mismatch variation across the wafer. This can be achieved by probing several matched pairs across the wafer and perform standard I-V curve sweeps, preferably combined with some kind of mismatch sweep curve. The mismatch sweep is a standard I-V curve, plotting a mismatch variable as a function of the main bias voltage variable (figures 3.27 and 3.28). Using the append function of parameter analyzers multiple times often results in an, at first sight, messy set of graphs, that nevertheless yields useful information. In the first place, mismatch sweeps can be used to select the appropriate biasing for the actual mismatch measurement. They can also help to avoid dangerous bias conditions (range changes and/or device oscillations). Secondly, this technique can be used to verify whether one has selected the appropriate population of test sites; for instance that one is not contacting pairs too close to the edge of the wafer, or that a (large) part of the wafer that does not function or suffers from excessive parametric variation due to processing or equipment failures. Finally, the mismatch sweep curves usually show a standard shape. This implies that a collection of them immediately provides a rough estimate of the mismatch number we can anticipate (are we talking 0.1, 1 or 10% like fluctuations). Moreover, as indicated in figures 3.27 and 3.28, they usually display a number of independent fluctuation mechanisms, each active in different operation region. This rather time-consuming step is not required for each pair, but certainly when a new type of wafer/process/test structure is to be started, it proves worthwhile to reconnoitre the wafer quite extensively using this manual/graphical technique.

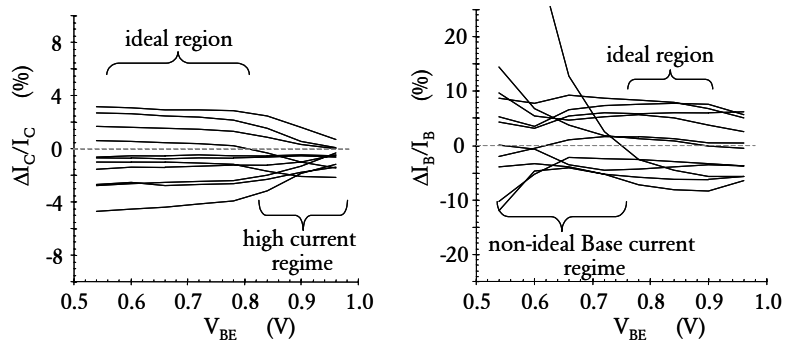

Figure 3.28 BJT mismatch sweeps. Left: Collector current mismatch; Right: Base current mismatch. Note the occurrence of two independent mismatch fluctuation mechanisms for the I_C as well as for I_B.

Tier 2: Always use multiple observations
A second measure that helps against unreliable statistical results is associated with outlier measurements. Outliers are frequently encountered in noisy test environments. A good countermeasure against power line spikes and other EMC disturbances is implemented through using multiple observations for each measurement point, combined with sorting and median assessment. For critical studies, we always apply the MXSY (generally M9S5 or M5S3) algorithm (combined with 1 PLC ADC integration), as discussed extensively earlier in this section.

Tier 3: Parametric range filtering
The third useful precaution against odd measurements is called range filtering. This technique is used as a safety measure against defective devices (short or open circuit) and/or gross measurement errors like miss probing. Outlier filtering techniques are commonly used in parametric test evaluation for process control (PCM testing). A very popular technique in this field is the so-called (iterative) 3-sigma filter method. In our studies, a somewhat more heuristic filtering approach is used, based on a priori knowledge of the devices under test. The technique consists of applying an acceptance range of the observables or parameter (hence not the mismatch between them) around the median of its own population. The acceptance range is an independent input variable in the statistical data analysis program. Typical numbers for the acceptance range are 10 to 50% for currents or gain factors (in BJT's) and 50 to 200 mV for threshold voltages (in MOSFET's). This technique has several characteristic features, some of which are clear advantages over other techniques, while others are just important to know.

- In the first place, while doing matching measurements, one is generally not 'working in the dark' with respect to the anticipated performance of the matched elements. When the wafers arrive at the matching characterisation station, a lot of a priori knowledge is available about the wafers / technology. Hence, one should usually be able to define a sensible acceptance range of the particular device performance based on the process documentation and/or the PCM measurements.
- For determining the acceptance range, one can also make good use of the mismatch sweeps discussed in this section, as they provide an initial guestimate of the parametric fluctuation as well as the mismatch fluctuation.
- Using the (initial) median observation rather than the average, for setting up the acceptance range is a way to be less dependent on the occurrence of outliers, since the median value is much less affected by outliers.
- An advantage of this filtering approach is that one knows (in fact defines) beforehand what the acceptance range of the parameters or observables is. So one does not have to search

through an iterative scheme why a particular pair was discarded. The range filtering algorithm contains no moving boundaries other than the centre position of the range defined by the median.

- What initially may seem slightly confusing is that this range screening should primarily be applied to the observable parameters (V_{T1}, V_{T2}) of the individual elements of the pair, and not (or at most additional) to the calculated mismatch parameter (ΔV_T). The screening is primarily intended for discarding defective devices or faulty measurements, not necessarily strange mismatch observations. Note for instance that when two elements of a pair are both shorted (due to a defect or insufficient etching of the first metal layer), the two components are useless, while their mismatch may be negligibly small! Such zero mismatch occurrences would reduce the observed standard deviation if they were not kept out of the population. This can only be achieved by screening at the device parameter level.
- It is good practice to mark discarded pairs with an error code. Preferably, this code should indicate which of the device parameters was flagged as out of range. This is particularly important to be able to trace afterwards what the dominant failure mechanism (if any) is for the matched devices under investigation.
- It can occur that an acceptance range is chosen on the small side. For instance for very small devices it is not unthinkable that the random fluctuation component rises above the spatial parametric variation component (spread) as observed for large devices. Another reason why it may be useful to keep track of the causes for discarding transistors is that this may provide valuable information about process weaknesses.
- If an acceptance range is chosen too small, pairs can be flagged out, of which upon scrutiny one concludes that there is no real indication of a true defect or a gross measurement error. In such cases, usually the mismatch also looks quite normal. This obviously agrees with one of the basic assumptions of stochastic fluctuations, namely that the stochastic component of the mismatch is to first order independent of the primary parameter value. Hence, a seemingly bad parametric value that is flagged to fall beyond the screening range (say a pair near the edge of the wafer) can still fit perfectly well within the regular mismatch statistics. This also explains occurrence of the following type of event that was encountered several times when the screening range for a particular parameter (e.g. the base current of a BJT) was set too narrow, resulting in an unrealistic large number of discarded pairs. After the cause of the large number of rejections was identified (with help of the error code), the population was re-measured with the screening range set significantly wider. In some of these cases it was found that the mismatch standard deviations of the second set of

measurements turned out lower than the standard deviations obtained from the original (smaller) sets of accepted pairs, while the parametric spread of the accepted population was significantly larger due to the increased screening range. This is the result of the uncertainty in the estimated standard deviation due to the limited population size combined with the fact that the mismatch was indeed practically independent of the observable. This learns that one should take care that screening ranges are not set too tight. In fact, the screening range should only be used to discard real defect devices and gross measurement errors and device defects rather than a kind of quality assessment of the parametric spread of a technology.

- Rejected pairs (defects) do show up regularly in populations of matched pairs. Apart from the arguments sketched above, one can wonder how it is possible that one can encounter disposable observations all together. Integrated circuits are built from tens of thousands to tens of millions functional elements. In this perspective, it seems very unlikely that while measuring a meagre 60 to 200 transistors (30 to 100 pairs), one can encounter a defective device. The frequency of their appearance depends on the maturity of the technology under investigation. For development lots, one or two outliers (up to 5% of the matched pair population) are not uncommon and usually associated with die-positions near the edge of the wafer. On wafers that are produced in well-yielding production lines, indeed the number of discarded pairs is generally negligible (much less than 1% of the population). The most controversial situations arise when wild research lots are being evaluated for matching performance implications of a particular device architecture choice. Lots, processed with experimental process steps in less well-controlled fabs with sub-optimal equipment, may be hampered by a significant number of failing pairs, up to as high as 30%. Fortunately, we have been able to derive some very interesting and useful results from such disaster lots, be it that some extra care had to be taken with analysing the validity of the data (who mentioned lies, damned lies and statistics?).

Tier 4: The blunt axe in statistics

The fourth security measure that is built into our statistical analysis routines is based on the practice to discard the highest and lowest two mismatch observations of each population. This may seem (and indeed is), a rather draconic measure, hence its name. A statistical mathematician W. Rey originally suggested the so-called blunt axe approach as a useful technique for mismatch characterisation. His experience, based on numerous statistical analyses of research experiments in many different areas of Philips Research, was that with experimental data sets (as opposed to theoretical data sets) there practically is always something wrong.

Measurement errors or unexpected / unexplainable outliers can force one to spend disproportionate amounts of time and energy to explain something that may be not relevant and often proves unrepeatable, hence unexplainable anyway. Therefore, Rey suggested discarding the highest and lowest 5% of the data points before calculating a standard deviation estimator. This approach, an element of Rey's so-called 'robust statistical methods' [Rey] (in combination with rank-linear estimation), was translated in all of our algorithms into discarding the two highest and two lowest observations. This corresponds with 5% for a typical matched pair population size of 40 pairs. Although the blunt axe method may seem crude, an over-kill, and an almost certain source of underestimating standard deviations, in practice it cannot but be admitted that this approach is indeed very useful for mismatch characterisation. It does occur (surprisingly, frighteningly) often that a distribution is contaminated with one or more unexplainable outliers. One of our standard practices is to make normal-scaled cumulative probability plots [Ewert05], which instantly reveals outliers. Indeed, we observe frequently that a quite decent Gaussian distribution is spoiled by one or more outliers. An example of such a distribution was for instance depicted in figure 3.14. It was already suggested that such disturbances could be associated with power net induced or other EMC disturbances. Another frequently encountered measurement error cause is attributable to (dust) particles on the wafer that stick to the probe needles.

As the prime interest of the work as presented in this thesis is to increase understanding of the main stochastic (and systematic) mismatch effects, we find it much better not to spend too much time and energy on such possible outliers, hence our adherence to the blunt axe method. This saves time in the sense that one can accept the majority of the standard deviations as is, from the measurement / statistical estimation program. Despite the clear practical advantage mentioned above, the disadvantage of the blunt axe method obviously is that if there are no outliers in the population, one still throws away the two highest and lowest values. This means by definition that the standard deviation estimator of the remaining population is lower than the one of the original population. The impact of this underestimation depends on the size of the original population. To demonstrate and quantify this, figure 3.29 shows the reduction of the standard deviation for five population sizes as a function of the number of discarded highest and lowest observations. Each point in this graph is based on 51 sets of independent random (normal distributed) populations. After sorting each population, the standard deviation of each set was determined for the entire set as well as the axed-versions. Subsequently the median of these standard deviations were determined and the relative value of the axed standard deviation compared to the one based on the original sets of 21, 41, 61, 81

and 101 samples was plotted in the figure. Figure 3.29 indeed confirms that a substantial underestimation can result from discarding the highest and lowest points. For a typical matched pair population size of 60 to 100 pairs on a wafer, the underestimation is of the order of 10 to 15% when the two highest and two lowest points are discarded. This underestimation should be weighted against the disadvantage of an erroneous overestimation of the standard deviation due to inevitable and unpredictable outliers. Since these outliers do happen occur surprisingly frequently, the 10 to 15% should in fact be interpreted as an upper boundary of the underestimation error.

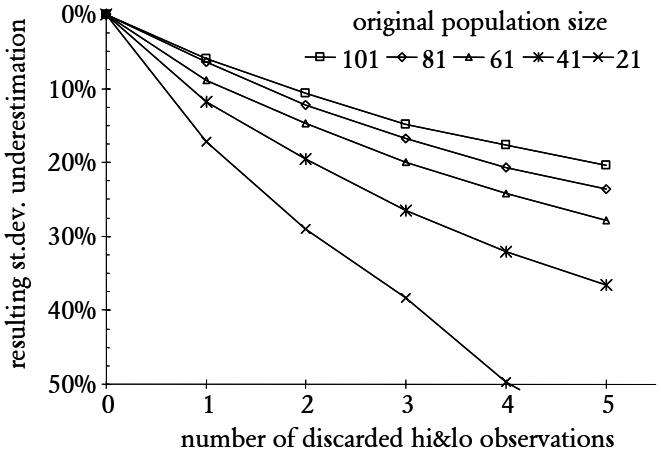

Figure 3.29 Underestimation of standard deviations due to blunt axing.

Tier 5: Inpection of normal-scaled cumulative probability plots

The final security measure that is built into our more advanced mismatch analysis programs is based on visual inspection of the population of mismatch observations (and the STR) using normal scaled cumulative probability plots (NSCPP). In this type of graph, the (sorted) mismatch values are represented on the vertical axis, whereas the horizontal axis represents the cumulative probability in terms of quantiles of the standard normal distribution. This type of graph transforms the (sorted) mismatch observations to a straight line if they are distributed

according to a normal Gaussian distribution. The slope of the line hence represents the standard deviation of the population. The quantile=0 value (vertical axis crossing) represents its median. Visual verification of the straightness of the line (normality of the population) is in fact an engineer's way (carpenter's eye) to the formal mathematical rank-linear method. If the slope of the NSCPP varies strongly from quantile to quantile, the distribution must be far from normal.

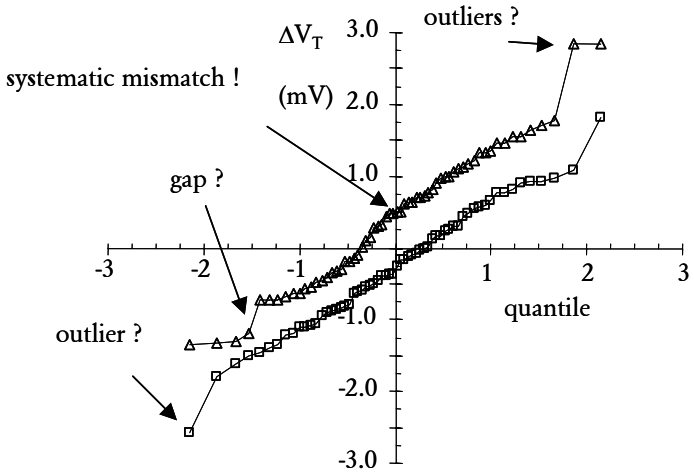

Figure 3.30 Two examples of NSCPP's of VT mismatch measurements of two populations with approximately equal standard deviations but significantly differently medians. Also note a couple of disputable outliers that are discarded in the safe estimation's blunt axe technique.

Throughout this thesis, examples of the NSCPP are used to visualise observed effects on measured populations. Apart from the visual assessment of the standard deviation and the median, normal scaled probability plots can also give additional indications about the population like occurrence of a outliers (figures 3.14 and 3.30), multi modal distributions, or gaps in the distributions. Finally, yet not unimportantly, one occasionally encounters apparent quantisation effects due to limited resolution of an A/D converter in the meter as for instance reported in [Tuin96a], or due to porting too few digits to the analysis program. Obviously, displaying a possible statistical disaster in an NSCPP provides no solution on how to deal with them, other than that a warned person counts for two. The last thing one should

let happen is to calculate the resulting standard deviation from funny distributions blindly, or even worse, use such a suspicious standard deviation for building models, starting process improvement actions, or basing process documentation (design manual) on them.

Most spreadsheet programs and/or statistical data analysis programs provide this type of plot. In the current Microsoft driven PC world, one can do this quite simple using Excel using data sorting and create the quantile axis using NORMSINV(N/(M+1)), with N the rank number and M the population size.

[www.greytrout.com/manuals]: NORMSINV is the inverse of the cumulative standard normal distribution function. The syntax is NORMSINV(P) where P is a probability value ($0 < P < 1$). NORMSINV returns the value X such that the integral from minus infinity to X of the standard normal distribution function is equal to P. P must be greater than 0 and less than 1.

The mathematical formulation is given by: X, such that $P = \int_{-\infty}^{X} \frac{1}{\sqrt{2\pi}} e^{-\frac{t^2}{2}} dt$

Another form of the cumulative probability plot that is encountered (more often) in the literature is plotted with the cumulative probability on the vertical axis in percents and the fluctuating quantity on the horizontal axis. This type of graph has the advantage that one can quite easily obtain a feeling for the probability of a certain mismatch occurrence without having to translate quantiles (sigma's) to percentages. There also is a normal scaled version that also has the property that it yields a straight line when the distribution is Gaussian (see for instance figure 4.8 of this thesis). The type of NSCP graphs as advocated in this section (with the quantile scale on the x-axis) has as advantage that the slope dy/dx of the probability plot immediately yields the standard deviation (including its variation along the curve).

Bootstrapping

Another very useful statistical technique for evaluation of the statistical properties of relatively small populations that was again suggested by W. Rey, is the so-called bootstrap technique [Diac83]. This technique provides quantitative numbers for the statistical uncertainty associated with the estimators that are calculated from limited population sizes.

The bootstrap technique can be described as follows (figure 3.31): from a population of N mismatch observations with estimators μ_{mm} and σ_{mm}, a new population of N samples is drawn randomly. Hence, some of the original observations may appear multiple times in the new population, while others are not picked at all. From this new population, new statistical estimators $\sigma_{\#1}$ and $\mu_{\#1}$ are calculated. This procedure is repeated M times (with M typically ranging from fifty up to a few thousand) yielding populations of the estimators $\mu_{\#i}$ and $\sigma_{\#i}$. From these, the medians μ_μ and μ_σ and standard deviations σ_μ and σ_σ are calculated. The μ_μ and μ_σ are generally quite close to the original estimator μ_{mm} and σ_{mm} as obtained from the original distributions (as they should be). σ_μ and σ_σ are good measures for the statistical uncertainty of the original estimators μ_{mm} and σ_{mm}. These uncertainty estimators can be as safety precautions or sanity checks. In the first place, (three times) the calculated standard deviations provide reasonable error bars in graphs with the calculated estimators (e.g. the Pelgrom plots). Although most engineers and scientists know that any estimation process is prone to an uncertainty interval, embarrassingly, many publications and documents on matching characterisation report numbers with 3 and sometimes even 4 or 5 digits, whereas a 10% or more uncertainty interval should have been attached to these numbers. A bootstrap algorithm provides a good estimate for this interval. In the same ballpark, the uncertainty interval for the median observation is very useful in case of doubt whether an occurring systematic mismatch (test structure or measurement system offset) is significant.
Another useful application of the uncertainty interval σ_σ obtained with the bootstrap technique is that it can be used to generate a warning for the existence of outliers in the population under evaluation. This is particularly useful when not all populations are (can be) monitored visually using the graphical normal-scaled cumulative probability plots (logistically this can be a problem). A bootstrap analysis subroutine can be attached to the standard screening and statistical estimator determination program. How effective this can work is demonstrated in figure 3.32. In a 61-sample population with 2% standard deviation, the lowest point was adjusted manually with an extra offset, ranging between 1% and 1000%.

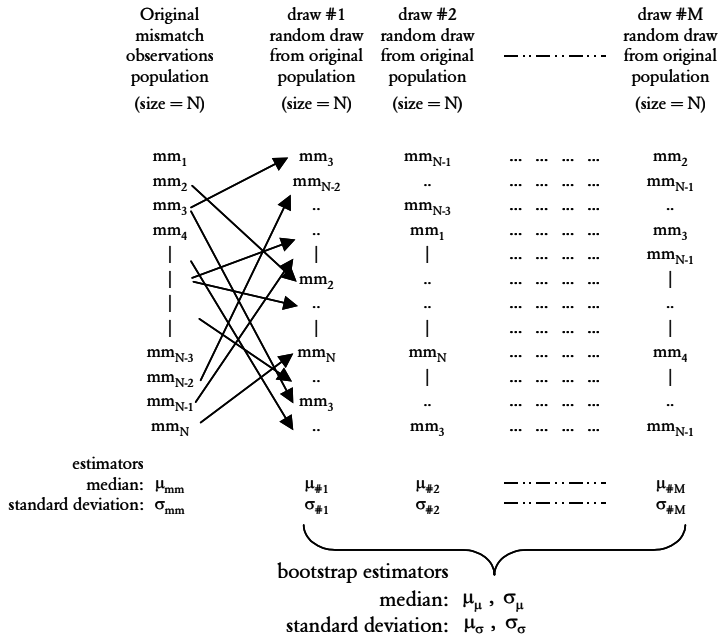

Figure 3.31 The bootstrap method for assessment of statistical uncertainty.

The left graph in figure 3.32 shows the NSCPP for the 10% extra error. Obviously, no one would have any difficulties to pick out this one outlier from this graph, but if the cumulative probability plot is not made, it proves relatively hard to figure out anything is wrong.
The overall standard deviation increases in this case from the original 2.04% to 2.69%.
A statistically significant increase, but when the standard deviation is not known a-priori (which is usually the case for a new process or process option), this probably remains unnoticed. Also, mind that a 15% mismatch, meaning that one of the two parameters of the matched pair is between 10 and 20% different from the same parameter of its neighbour, would more often than not pass through a normal parameter-screening algorithm.
By using bootstrapping however, one can see that the uncertainty of the standard deviation (σ_σ) increases much more pronounced: from 0.16% ($\approx \sigma/\sqrt{(2N)}$) to about 0.60%.

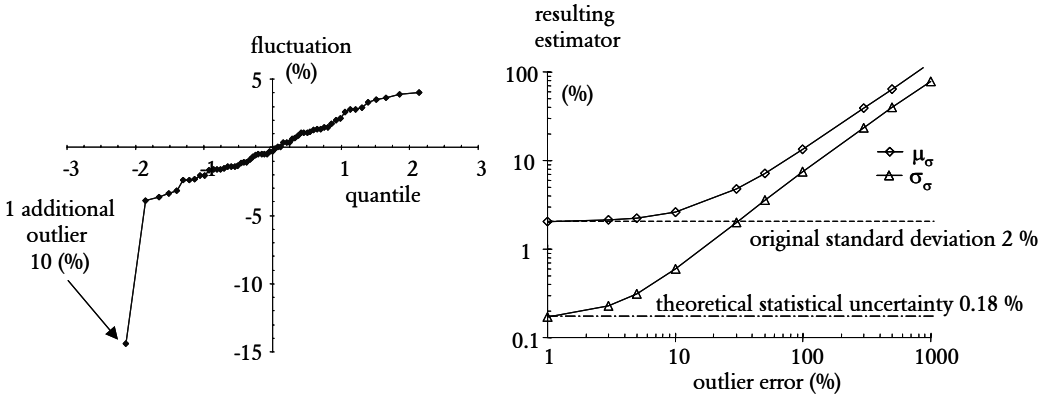

Figure 3.32 Example of impact of outliers on bootstrap estimators. Left: NSCPP with an additional -10% offset on the lowest point. Right: Impact of one additional outlier on bootstrap estimators as a function of the additional offset added to the lowest point. Dashed line is the original (2%) standard deviation; Dot-Dashed line the theoretical (0.18%) statistical uncertainty.

The right graph in figure 3.31 displays the sensitivity for the standard deviation and its uncertainty as a function of the magnitude of the single additional outlier.
This demonstrates that monitoring the statistical uncertainty with bootstrapping indeed is a rather sensitive method. Obviously, it is realised that the bootstrap method is no panacea for all measurement errors. If the additional –10% error had occurred on the highest observation (+ 4%), the resulting impact would have been much less pronounced. Moreover, obviously our safe estimation method would have removed the single outlier in figure 3.32 through the blunt axe procedure.

3.6 An example

This chapter is topped off with an example of the difficulties, challenges, or fascinating observations (depending on one's mood and/or available time) one can run into when attempting to assess and understand subtle mismatch fluctuation effects, at the edge of, or in fact beyond, the specifications of the measurement hardware. These examples were encountered during the data analysis for the 'decaborane study' that turned out a very convincing demonstration of the random fluctuation nature of ion implantations [Tuinh00b].
The experiment and the results are discussed in more detail in section 4.4 of this thesis.
This section focuses on measurement hardware and statistical analysis problems that were encountered during the evaluation of the results.

To apprehend the problems and the nomenclature of the case discussed in this section, the following details of the experiment are relevant.

- The parametric mismatch fluctuation measurements were performed on CS&CG matched pair test structures, depicted in figure 3.33. As we were studying a typical bulk fluctuation effect, populations of W/L=10/10 device pairs were selected for this threshold voltage fluctuation study.

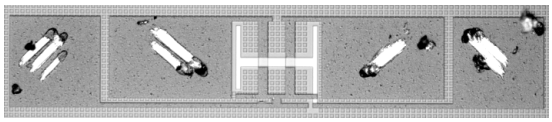

Figure 3.33 MOSFET W/L = 10/10 CS&CG matched pair test structure.

- The measurement circuit is depicted in figure 3.34. The threshold voltage (mismatch) measurements were done using the fixed V_{GS} 3-point technique [Tuinh00a, Croo02a] on the HP4156/C-M12k mismatch characterisation test station. The two transistors are measured with a sequential measurement algorithm. In the first step, Drain_1 is biased at V_{DS}=0.1 V and Drain_2 is set at 0.0 V. A gate voltage sweep then catches the three appropriate gate bias points (<0.6, 1.0, 1.8> or <0.9, 1.2, 2.0>, depending on the V_T of the transistors). Then, Drain_1 is set to zero and Drain_2 to 0.1 V and the other transistor is measured at the same gate biases. An additional trick in the algorithm is that the transistor currents are not measured in the drain SMU's, but in the (common) Source SMU. This has as advantage that the currents are determined using the same current meter. If the currents

had been measured in the drain terminals, the offset differences between the two current meters in SMU-3 and SMU-4 would have affected the mismatch observations. Note that our measurement system is not equipped with a switching matrix. This implies that common offset cancellation techniques such as source and meter swapping and/or reversing are not possible. The instrumentation difference that cannot be circumvented in the used method/algorithm is the possible voltage difference between the two drain voltages[†].

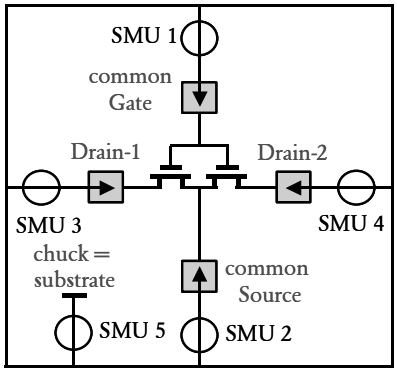

Figure 3.34 Measurement circuit for CS&CG MOSFET matched pair test structure.

- The expected threshold voltage mismatch fluctuation standard deviation was of the order of 0.5 mV. As the short-term repeatability for this measurement station/algorithm was assessed earlier as being significantly better than 50 μV [Tuinh00a] (and section 3.2 of this thesis; type ii STR assessment), it was expected that the impact of the measurement system on the mismatch fluctuation standard deviations would be negligible, even at this seemingly challenging fluctuation level.
- The population size (per wafer) was 62 pairs.
- The technological experiment encompassed three different attributes: dopant level, gate oxide thickness and ion implantation technique. Two dopant implantation doses (indicated 'L' for 1.7×10^{12} cm^{-2} and 'H' for 3.5×10^{12} cm^{-2}) and two gate oxide thicknesses (4 and 6 nm)

[†] There are methods to achieve this for very critical studies, such as offset monitoring [Tuinh00a] and/or voltage conversion (set the voltage on the common Source side (-0.1 V), and 0.0 V (System COMMON) on the active Drain) combined with COMMON offset monitoring as in [Tuin98].

were available. The main purpose of the experiment was to establish the difference between the three V_T-adjust ion implantation recipes, namely Boron (indicated as group 'B'), co-implanted Boron and Hydrogen ('B+H'), and decaborane $B_{10}H_{14}$, denoted as group 'Db'.

- The availability of two sets of matched pair test structures on the (CMOS) mask set was exploited fruitfully in this 'n-channel only' experiment. Through appropriate implant mask usage, one flavour of the V_T-adjusts was implanted in one of the sets (N-MOST's or P-MOST's) while another flavour was implanted in the other set, on the same wafer. Hence, although the populations were all n-channel devices, the ones measured on the NMOST modules are identified with the capital N, and those measured on the PMOST modules with a P. The experimental set-up was full factorial (12 combinations), fabricated on 24 wafers, yielding four supposedly identical populations per combination (N- and P-modules are assumed identical).

General overview of mismatch fluctuation measurements

Table 3.9 is a copy of the master table of the mismatch fluctuation measurement results of all available populations of 10/10 pairs. This table contains the essential information as recorded in the lab-journal. Obviously, a table like this is hard to comprehend and not very interesting reading material. Nevertheless, it was reproduced here in whole, to serve as an example of what the usual bowl of data looks like after a couple of days of measurements. From such a point onwards, the unravelling of the results generally takes several days or even weeks.

The success of this decaborane experiment was evident from the start of the measurements and evaluations, as the decaborane populations yielded consistently higher mismatch fluctuation standard deviations compare to the Boron implanted populations. The (wafer) medians of the threshold voltage (3rd column) confirm the expected equality of the equivalent B, B+H and Db groups. The raw standard deviations σ_{VT} (column 4) signify the very good parametric gradient control over the wafer (with the exception of the #1 wafer which is the guinea pig for several equipment adjustments).

group	population wafer #	module N or P	median V_T (V)	raw σ_{VT} (mV)	$\mu_{\Delta VT}$ (mV)	$\sigma_{\Delta VT}$ (safe) (mV)	# def.	T (°C)	measurement date
Db, 4 L	1	P	0.310	19	0.37	0.77	5	22.9	Nov-10
“	2	N	-	-	-	-	-	-	n.a.
“	3	P	0.299	1.2	0.27	0.52	0	22.9	Nov-10
“	4	N	-	-	-	-	-	-	n.a.
B+H, 4 L	3	N	0.303	3.0	0.26	0.33	0	23.1	Nov-10
“	4	P	-	-	-	-	-	-	n.a.
“	5	N	0.301	3.1	0.30	0.29	1	23.2	Nov-10
“	6	P	0.300	2.9	0.20	0.30	0	23.3	"
B, 4 L	1	N	0.305	78	0.21	0.31	7	23.0	"
“	2	P	-	-	-	-	-	-	n.a.
“	5	P	0.302	1.3	0.32	0.29	0	23.2	Nov-10
“	6	N	0.302	1.3	0.18	0.31	0	23.3	"
Db, 6 L	7	P	0.304	2.5	0.17	0.75	0	22.5	Nov-11
“	8	N	0.294	3.9	0.33	0.64	0	22.5	"
“	9	P	0.296	3.8	0.36	0.70	0	22.8	"
“	10	N	0.290	4.0	-0.02	0.69	0	22.8	"
B+H, 6 L	9	N	0.299	2.7	0.22	0.51	0	22.7	"
“	10	P	0.298	2.7	0.13	0.42	0	22.9	"
“	11	N	0.298	2.9	0.30	0.38	0	22.9	"
“	12	P	-	-	-	-	-	-	n.a.
B, 6 L	7	N	0.298	2.5	0.20	0.44	0	22.4	Nov-11
“	8	P	0.298	2.3	0.15	0.44	0	22.6	"
“	11	P	0.298	3.1	0.04	0.42	0	23.0	"
“	12	N	-	-	-	-	-	-	n.a.
Db, 4 H	13	P	0.485	1.5	0.31	0.63	0	23.1	Nov-11
“	14	N	0.486	1.4	0.24	0.50	0	22.1	Nov-9
“	15	P	0.480	1.2	0.23	0.56	0	23.2	Nov-11
“	16	N	0.476	1.4	0.41	0.54	0	23.3	"
B+H, 4 H	15	N	0.490	0.9	0.32	0.33	0	23.1	"
“	16	P	0.487	0.9	0.20	0.38	0	23.3	"
“	17	N	0.487	0.9	0.21	0.38	0	23.3	Nov-12
“	18	P	0.484	1.1	0.18	0.33	1	22.5	"
B, 4 H	13	N	0.492	1.0	0.20	0.36	2	23.6	Nov-11
“	14	P	0.491	0.9	0.24	0.37	0	22.2	Nov-9
“	17	P	0.490	1.3	0.24	0.33	1	22.3	Nov-12
“	18	N	0.488	1.3	0.27	0.38	2	22.4	"
Db, 6 H	19	P	0.511	4.4	0.29	0.84	0	22.7	"
“	20	N	0.515	4.4	0.25	0.81	0	22.8	"
“	21	P	0.507	4.6	0.28	0.82	0	23.0	"
“	23	N	0.512	5.1	-0.25	0.72	0	22.7	Dec-08
B+H, 6 H	21	N	0.520	4.2	0.32	0.61	0	22.8	Nov-12
“	22	N	0.519	4.4	-0.19	0.45	3	22.6	Dec-08
“	23	P	0.518	4.5	-0.17	0.41	0	22.7	"
“	24	P	0.513	4.5	-0.30	0.39	0	22.7	"
B, 6 H	19	N	0.517	3.5	0.05	0.58	0	22.6	Nov-12
“	20	P	0.519	4.3	0.29	0.59	0	22.8	"
“	22	P	0.520	2.8	-0.33	0.46	1	22.6	Dec-08
“	24	N	0.514	5.2	-0.38	0.39	2	22.7	"

Table 3.9 Master table of the decaborane mismatch experiment.

The V_T mismatch fluctuation standard deviations all seem to follow the intended process splits at least qualitatively. The medians of the mismatch fluctuation assessments yield acceptable values. There appears to be a statistically significant systematic mismatch component of the order of 0.2 mV. Since the values are always less than the standard deviation for each population, at the time of the measurements, this was deemed acceptable.
This somewhat careless assessment is moderated later in this discussion.

The number of (range filtered) defects (column 7) was not negligible for some populations. Most of these were seen on the guinea pig wafer, which is not uncommon. Most other fails could be retraced as probing errors and poor contacts (particle between needle and pad) rather than device defects.

The prober's micro-chamber temperature is given in column 8. In general, this is a good practice, and in this case it is added to the table as an indication that temperature differences and drifts (between devices) are negligible for this study.

Finally, it is worth to realise that the measurements were spread-out over relatively long period (column 9). Initially the wafers 1 to 21 were measured (in November), while about one month(!) later, the remaining wafers and the substrate bias dependence of the mismatch fluctuation for a number of wafers were measured.

Assessment of the mismatch fluctuation standard deviations

Table 3.10 focuses on the main goal of the experiment, namely to determine whether threshold mismatch fluctuations are indeed larger for the Decaborane splits, compared to their Boron counterparts. In the table below, the V_T mismatch fluctuation estimators $\sigma_{\Delta VT(W/L=10/10)}$ for all W/L=10/10 ΔV_T populations are calculated using the safe estimation technique (remove measurement errors/defects and discard highest and lowest 2 observations). To be able to focus on the problem under investigation in this section, only the results from the second half of table 3.9, in this case the 'High dopant' populations were copied to table 3.10.

$\sigma_{\Delta VT(W/L=10/10)}$ in mV safe estimation per wafer	Group T_{ox} , Dope level			
Dopant species	4 , High		6 , High	
Decaborane	0.63	0.50	0.84	0.81
	0.56	0.54	0.82	0.72
B+H	0.33	0.38	0.61	0.45
	0.38	0.33	0.41	0.39
B	0.36	0.37	0.58	0.59
	0.33	0.38	0.46	0.39

Table 3.10 V_T mismatch standard deviations for groups 4 H and 6 H.

The results from these populations seem somewhat dispersed per group, which should always be expected anyway, due to the inherent statistical uncertainty. A common approach is to take all data of the populations with identical process conditions into one group and recalculate the standard deviations. This brings the theoretical (and usually practical) advantage that the total populations size increases (from 62 to 248), which implies that the statistical uncertainty due to the finite population size should decrease roughly a factor of two. The results from the grouped populations are listed in table 3.11 and depicted graphically in figure 3.35.

$\sigma_{\Delta VT(W/L=10/10)}$ in mV safe estimation per group	Group T_{ox} , Dope level	
Dopant species	4 , High	6 , High
Decaborane	0.61	0.91
B+H	0.40	0.55
B	0.40	0.60

Table 3.11 V_T mismatch standard deviations for groups 4 H and 6 H.

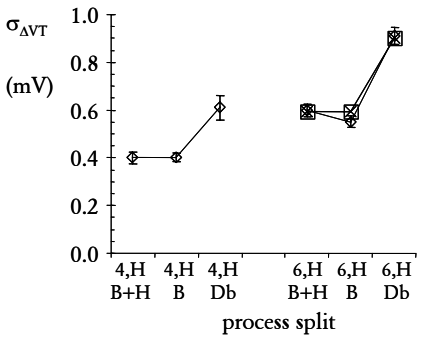

Figure 3.35 Graphical representation of V_T mismatch standard deviations of grouped populations. Diamonds: grouped results from 4 populations. Error bars calculated with bootstrap analysis. X's: prediction of 6 H groups from 4 H group results using T_{ox} scaling.

While looking at these results, at first sight it seems as if we are indeed looking at a real good news story: It appears as if two of the anticipated (hoped for) physical effects are quite clearly discernible:

- The threshold voltage mismatch fluctuations of the decaborane populations clearly stand out in each group, while the Boron and the Boron + Hydrogen groups are pretty much equivalent.
- The impact of the dielectric thickness split (4 nm in group 4,H vs. 6 nm in group 6,H) seems to be of the right order.

However, if the T_{ox} effect is calculated, the initial enthusiasm is somewhat diminished.
The X's in figure 3.35 illustrates this. The predictions (X's) were calculated for the 6H populations (thicker oxide), when the results of group 4H populations are used as anchor points. The '6H - B' results now appear to be somewhat less consistent with the T_{ox} scaling than the other results of the 6H group. This would imply that the Boron and Boron + Hydrogen populations are not as identical as expected. The discrepancy cannot be explained satisfactorily through statistical uncertainty. The statistical uncertainties $\sigma_{\sigma\Delta VT}$ (bootstrap analysis on the grouped populations) are as shown as (1 σ) error bars. As the equality of the B and B+H groups was of course one of the airbags in the experimental plan, it was investigated what caused the apparent inconsistency.

In figure 3.36, the individual population standard deviation estimators from table 3.10 are depicted graphically. As expected, figure 3.36 displays the same trends as obtained from the grouped populations, but it will also be clear that while some splits seem to yield perfectly agreeing standard deviations for the supposedly equal populations, there are others where this is clearly not the case. Moreover, the differences between the estimators in those splits are much larger than the 10 to 15% that can be explained through the statistical uncertainty with N≈62.

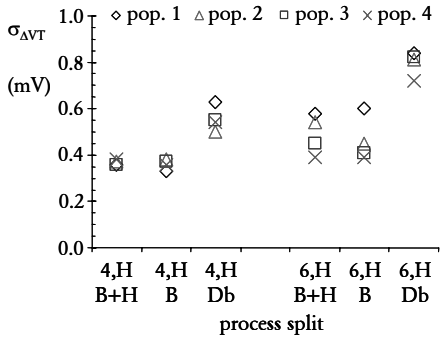

Figure 3.36 V_T mismatch standard deviations of individual populations.

In tables 3.12 the lower quart of table 3.9 is re-extracted. Together with figure 3.36 this helps to identify what went wrong in this experiment. If one looks at the four B+H populations one sees 1 population (21N) that yields a standard deviation of 0.61 mV, whereas the other 3 range from 0.39 to 0.45. A first reaction would be to discard the 21N population entirely and use a value of the order of 0.41 +/- 0.04 mV as the outcome of this particular group. This would not be fair however if one looks at the standard deviations of the supposedly equal 'Boron only' group of populations with the same oxide and doping level, which ranges from 0.39 to 0.59 mV, but in this case with two values in between that make that the highest value no longer stands out so clearly. As indicated before, a quick glance at this table does not immediately raise big matching characterisation concerns. All medians are reasonably small (less than 1 sigma). The 22N population exhibits the largest number of rejected pairs (defects).
This was the first wafer (of this mask set) on the prober since 4 weeks. The defects were probably due to a mis-probing (prober error) and some particles (or a hair) on the wafer.

group	population wafer #	module N or P	median V_T (V)	$\mu_{\Delta VT}$ (mV)	$\sigma_{\Delta VT}$ (safe) (mV)	# defects	Temp (°C)	measurement day
Db, 6H	19	P	0.511	0.29	0.84	0	22.7	Nov-12
"	20	N	0.515	0.25	0.81	0	22.8	"
"	21	P	0.507	0.28	0.82	0	23.0	"
"	23	N	0.512	-0.25	0.72	0	22.7	Dec-08
B+H, 6H	21	N	0.520	0.32	0.61	0	22.8	Nov-12
"	22	N	0.519	-0.19	0.45	3	22.6	Dec-08
"	23	P	0.518	-0.17	0.41	0	22.7	"
"	24	P	0.513	-0.30	0.39	0	22.7	"
B, 6H	19	N	0.517	0.05	0.58	0	22.6	Nov-12
"	20	P	0.519	0.29	0.59	0	22.8	"
"	22	P	0.520	-0.33	0.46	1	22.6	Dec-08
"	24	N	0.514	-0.38	0.39	2	22.7	"

Table 3.12 Lower quart of table 3.9.

So essentially, one is faced with the problem to explain why the populations of identical splits can be so different. The standard approach is in such a case to plot the cumulative probability plots and check whether the distributions are peculiar.

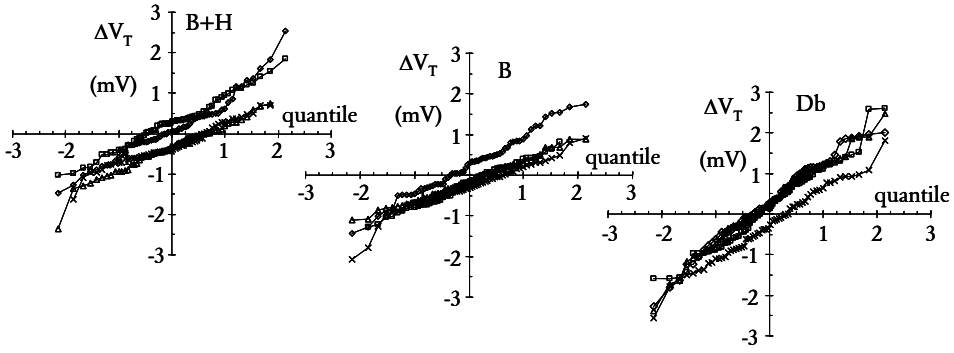

Figure 3.37 NSCPP's of the three 6H groups. Each group has four populations.

The three graphs depicted in figure 3.37 can be considered as typical examples of NSCPPs for mismatch measurements. They all form decent representations of normal distributions (straight lines). One may be tempted to see a few outliers on the high and low side, but as these are never more than two on any side, the safe estimations (discarding highest and lowest 2 observations) did discard those for the calculated standard deviations anyway (hence contribute to a more consistent standard deviation estimation). The most striking feature of the figures is however that there clearly are two groups in these graphs. There are six populations with a positive median and six with a negative median. This is summarised in the table 3.13.

$\mu_{\Delta VT}$	Db		B+H		B	
Measurement period	pop.	$\mu_{\Delta VT}$	pop.	$\mu_{\Delta VT}$	pop.	$\mu_{\Delta VT}$
November	19 P	+0.29	21 N	+0.32	19 N	+0.05
	20 N	+0.25			20 P	+0.29
	21 P	+0.28				
December	23 N	- 0.25	22 N	- 0.19	22 P	- 0.33
			23 P	- 0.17	24 N	- 0.38
			24 P	- 0.30		

Table 3.13 Again a smaller part of table 3.9. sorted by split and measurement day.

Remarkably, all populations measured in November had a positive median, while all populations measured in December clearly yielded a negative median. In the period between these two measurement sessions, the measurement system was used for a different project. The HP4156A measurement system has been switched off and on a number of times in the period between the measurements, which means that the sources and meters were re(auto)calibrated between these measurement sessions.

Note that in the three-point V_T extraction algorithm, a V_{DS} error of about 0.5 mV would be required to explain a 0.3 mV threshold voltage error[†]. The specifications of the high resolution SMU's of the HP4156 have an accuracy of 700 μV, so this may indeed have been the case. In [Tuinh01b] we reported that the short- and medium-term variations of the source voltages are generally well within 100 μV, but when the system is switched off and on, the differences are apparently larger.

[†]A V_{ds} difference between the two V_{ds}'s of the two transistors on the 100 mV programmed values (goes directly through the $(1+\delta)/2 * V_{ds}$ term in the 3point solve algorithm for V_T extraction.

The occurrence of different signs for the medians of the mismatch in supposedly identical populations explains part of the reason why one cannot take the populations together in one big group and calculate a new standard deviation. As the systematic mismatch of the B and B+H populations is about half of the standard deviation, combining two groups with opposite medians will contribute significantly to the resulting overall sigma. Moreover, also if one looks at the standard deviation estimators themselves, there appears to be an impact of the measurement period. It was already clear from figure 3.36 that also the standard deviation estimators were quite widely dispersed, but from table 3.14 one can indeed see that for all three dopant groups the standard deviation is significantly lower for the measurements in December compared to those done the month before!

$\sigma_{\Delta VT}$	Db		B+H		B	
Measurement period	pop.	$\sigma_{\Delta VT}$	pop.	$\sigma_{\Delta VT}$	pop.	$\sigma_{\Delta VT}$
November	19 P	0.84	21 N	0.61	19 N	0.58
	20 N	0.81			20 P	0.59
	21 P	0.82				
December	23 N	0.71	22 N	0.45	22 P	0.46
			23 P	0.41	24 N	0.39
			24 P	0.39		

Table 3.14 Another small part of table 3.9 sorted by split and measurement day.

In fact, this is a serious problem. The opposite sign of the systematic mismatch could obviously have been repaired for the analysis by just taking the opposite of all mismatch observations of one period before combining them with the other group. In this case, however, the outcome suggests that the measurement system had a much larger impact on the estimators than previous assessments suggested. It seems as if the short-term measurement repeatability -in fact the performance of the measurement system- is letting us down here. For 10/10 devices the short-term repeatability was expected to be of the order of 50 μV (section 3.2) and [Tuinh01b]. Now, in hindsight, it appears as if the measurement system may have been performing significantly worse. Note that in order to explain the average reduction of the standard deviation in the December period compared to the standard deviations of the November period, the extra system fluctuation contribution in November must have been of the order of

430 μV !!! † Unfortunately, a regular short-term repeatability check was not done during the experiments, so the exact development of the system's performance cannot be reproduced here.

Based on the analysis presented above, one can only conclude that in the period between November and December a combination of changing circumstances makes it quite undesirable to attempt to combine the results of the populations acquired over the two periods. Obviously, from a statisticians point of view this is a no-brainer: Taking populations together that have systematic mismatch differences of the same order as the standard deviations is not-done, and this example demonstrates this. The problem is that such differences had not been encountered before with this particular measurement system. Repeatability experiments done up to then were always significantly better than what was encountered in this example. This proved a good lesson though: one cannot be careful enough to keep an eye on the system, and one must always do some repeatability tests if for whatever reason the status of the measurement system was changed between measuring related standard deviations.

Measurement repeatability

Although it was stated above that there was no regular assessment available of the short-term repeatability, it is not so that we cannot say anything about the system's performance in this respect. To study the impact of the disturbance clustering effect of the decaborane profile, the substrate voltage dependence of the threshold voltage mismatch fluctuation was measured for eight different populations. This means that there are in fact re-measurements available for those 8 populations for zero volts on the substrate (the default setting used for all the results from table 3.9). According to the classification of short-term repeatability assessment techniques as discussed in this chapter, this is a 'type i' STR assessment be it that the time between the measurements was very long (about one month). Furthermore, a ‘type ii’ was found amongst the data, which for this example proves extremely instructive, though it must be admitted that when these measurements were actually done, its significance escaped the attentions it, in hindsight, deserved.

Table 3.16, summarises the obtained standard deviations $\sigma_{\Delta VT}$ as well as the de repeatability assessments $\sigma_{\Delta\Delta VT}$ for the eight comparable mismatch measurements. As in a regular STR assessment, $\sigma_{\Delta\Delta VT}$ represents the standard deviation of the difference between the corresponding

† $\sigma^2_{obs} = \sigma^2_{mm} + \sigma^2_{syst1} + \sigma^2_{syst2}$; with σ^2_{syst2} negligible in December yields for Db results $\sigma^2_{syst2} = (0.83)^2 - (0.71)^2 = (0.43)^2$ and (B+H) results: $\sigma^2_{syst2} = (0.60)^2 - (0.42)^2 = (0.43)^2$

ΔV_T observations. As discussed before in section 3.2, to represent the true repeatability of the ΔV_T determination this $\sigma_{\Delta\Delta VT}$ estimator should in fact be divided by $\sqrt{2}$.

$\sigma_{\Delta VT(W/L=10/10)}$ (mV)	Group T_{ox} & Dope								
Dopant species	meas. number	4 Low		6 Low		4 High		6 High	
		$\sigma_{\Delta VT}$	$\sigma_{\Delta\Delta VT}$	$\sigma_{\Delta VT}$	$\sigma_{\Delta\Delta VT}$	$\sigma_{\Delta VT}$	$\sigma_{\Delta\Delta VT}$	$\sigma_{\Delta VT}$	$\sigma_{\Delta\Delta VT}$
Decaborane	1st (Nov)	0.52	0.048	0.70	0.20	0.56	0.18	0.82	0.34
	2nd (Dec)	0.51		0.69		0.54		0.86	
B+H	1st (Nov)	0.33	0.052	0.51	0.14	0.33	0.16	0.61	0.39
	2nd (Dec)	0.32		0.49		0.33		0.49	

Table 3.16 Overview of results of repeatability checks.

These results reveal interesting insights about the measurement technique as well as the hardware. At first sight the differences between the $\sigma_{\Delta VT}$'s seem quite acceptable: for most populations, the difference between the $\sigma_{\Delta VT}$ as encountered in December did not deviate by more than 0.02 mV from the values as determined in November. This is well within the statistical uncertainty associated with the population size of 62. In particular, the repeatability standard deviation $\sigma_{\Delta\Delta VT}$ of the first two populations, 4L-Db and 4L-B+H, are quite impressive at a value of about 50 μV. This would indicate that the measurement method indeed performs as suggested in the introduction of this example.

Numbers provide insight, but the accompanying scatter plots and normal scaled cumulative probability plots are often more revealing. If one looks at the NSCPPs for the repeatability measurements of the populations 4L-Db and 4L-B+H (figure 3.36), one can indeed take from the slopes that the random components of the repeatability observations are small. This means that the devices' as well as the system's noise contributions are indeed negligible. The fact that the medians of the $\Delta\Delta V_T$ populations are at a value of -0.5 mV is consistent with the earlier observed differences between the measurements in November compared to those obtained in December. As we can safely assume that the devices' mismatches have not changed in the month the wafers were in their storage box, we must assume that the measurement station drifted quite dramatically in that period. Apparently the parameter analyzer's automatic re-calibrations and changes in lab conditions resulted in a substantial change in the output of the sources and/or the meters of the parameter analyzer, resulting in these rather dramatic

systematic threshold voltage mismatch observation difference of as much as 0.5 mV.
This is a good demonstration of one of the advices listed earlier in this chapter, namely that the measurement hardware should never be (auto-) calibrated in the middle of a measurement session. Final features worth pointing out in figure 3.38 are the outliers on the high sides of the two cumulative probability plots. They seem about 0.2 mV off compared to the other observations. These are most likely examples of EMC type of disturbances of the measurement system, like a voltage spike on the mains net or a spark discharge. Careful examination of the three (I_d) measurement points used for the V_T extractions of both devices indeed revealed that one or two of the three measurement points of one of the mismatch measurements for the (two and three) outlier mismatch observations were indeed a fraction higher than in the other case.

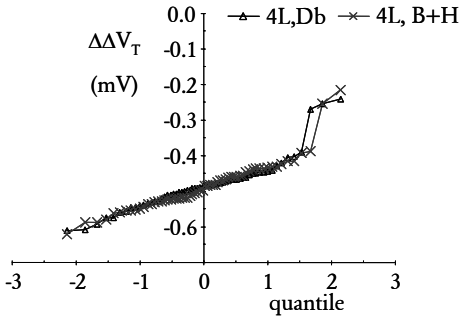

Figure 3.38 Excellent repeatability of V_T mismatch measurement. Note however the major shift of median: equipment drift.

So far for the good news about the '4 Low' results in table 3.16. Now let's take a look at the other groups' results. Although the mismatch standard deviations of the populations as measured in November and December are practically equal for the groups 6L and 4H mismatch assessments, their repeatability numbers are significantly worse (140 to 200 μV) compared to the '4 L' numbers. It seems odd that the repeatability performance of the measurement system can degrade so strongly. The original data sets were therefore re-assessed. The most probable explanation of a lack of repeatability like the one encountered here seems is a measurement hardware problem, presumably the A/D or D/A converters of the parameter analyser.

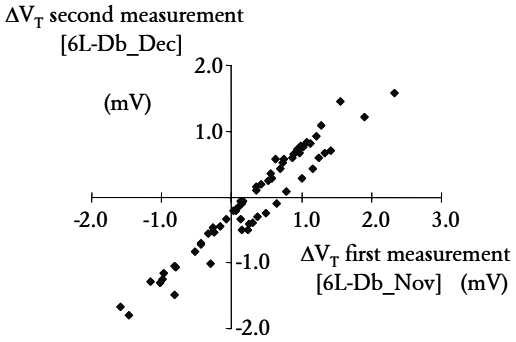

Figure 3.39 Scatter plot of V_T mismatch repeatability with two levels.

It is always difficult to re-capture the exact state of the measurement system, but is this case it proved possible to reconstruct some of the evidence from the data. A clear sign of a possible hardware problem is shown in 3.39. This figure combines the two sets of mismatch observations for the 6L-Db population. This scatter plot of the second set of mismatch measurements (December) versus the first set (November) reveals the occurrence of a pronounced second mode of the mismatch.

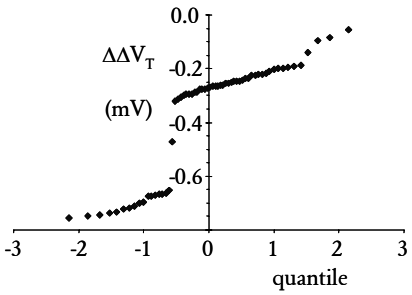

Figure 3.40 NSCPP of poor V_T mismatch repeatability with two levels.

A cumulative probability plot of $\Delta\Delta V_T$ calculated for these observations (figure 3.40) clearly reveals the two levels. Such observations generally either indicate a measurement hardware induced quantisation (meter or source range transitions, or converter bit offset errors) or one caused by a discrete time dependent device performance fluctuation like Random Telegraph Noise (RTN or RTS), associated with slow trapping and de-trapping of electrons or holes. Both these types of quantisation were encountered and reported before in the context of the work for this thesis [Tuin96a, Tuin01a]. It needs no arguing to understand that the short-time repeatability cumulative probability plot as depicted in figure 3.40 explains the degradation of $\sigma_{\Delta\Delta VT}$ from about 50 μV for the 4L populations to 200 μV for the 6L-Db. Next question is of-course, how such disastrous quantisation levels can be explained. An initial thought could be that we are witnessing an example of RTS, which can indeed result in a discrete current step during the measurement period of a typical V_T measurement [Tuinh01a]. In itself this is not very likely, as RTS observations as reported in the literature are usually measured on small transistors ($<<1\ \mu m^2$), while the transistor populations in this section all have 100 μm^2 area.

Drain current calculations

To establish whether an RTS trapping or de-trapping event could have caused these steps, or that they were caused by measurement hardware imperfections, one should know how large the steps in the currents were, and/or at which current levels they take place. As the threshold voltages (and beta's and theta's) were calculated analytically using 2 x 3 I_D-V_{GS} points, it proved possible to reconstruct the original I_D's using the original MOS transistor model that was used to transform the I-V data into the parameters. This is a useful side-benefit of the linear region 3-point direct extraction technique as its analytical parameter extraction algorithm preserves the exact input data, when the correct biases (V_{GSi}, V_{DS}, V_{BS}), and auxiliary variables (estimated body effect and $2\phi_f$) are entered. This in contrast with more complex least squares parameter fitting techniques, adaptive algorithms such as steepest slope extraction, or fixed-overdrive 3-point extraction, where the exact measurement currents cannot be retrieved from the parameters[†].

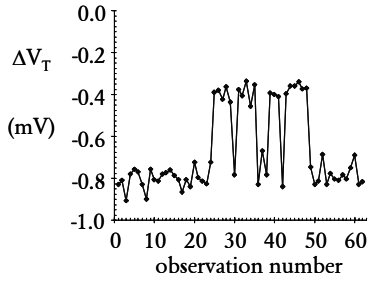

Figure 3.41 Type ii STR assessment: V_T mismatch of one pair measured 62 times. The full time scale is about 15 minutes.

In fact, this investigation started after digging-up a lucky shot 'type ii' measurement repeatability data set of one pair of the 6H-Db population. As discussed in this chapter, this is a single pair repeatability assessment done by measuring the last pair of the population 62 times.
The amazing result is depicted in figure 3.41. Apparently, the mismatch observation of this one single pair varies over time between two levels, -0.8 mV and -0.4 mV! The inverse calculations of the 3x2 drain currents from the parameters as measured 62 times on the pair are depicted in figure 3.42.

[†] Except when the measurement bias points are saved along with the derived parameters, which is usually not the case for parametric measurements.

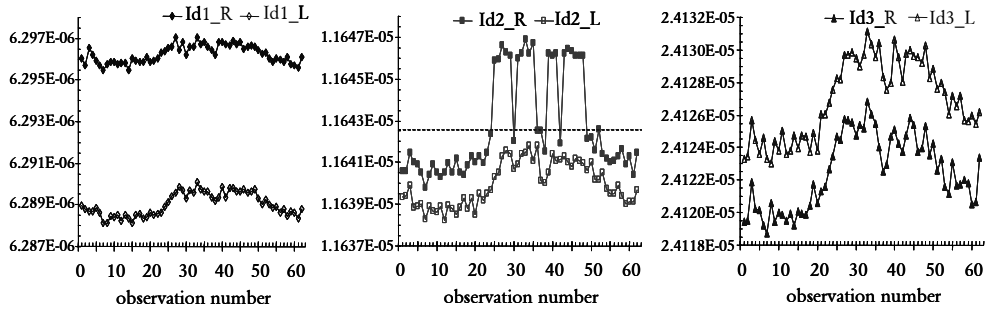

Figure 3.42 Drifts and jumps of the six currents used for a V_T mismatch assessment during a 'type ii' STR assessment. Solid symbols: Right transistor; Open symbols: Left transistor. Left graph: I_{d1}(@V_{GS}=0.9); Center graph: I_{d2}(@V_{GS}=1.2); Right graph: I_{d3}(@V_{GS}=2.0).

The most prominent feature of the three graphs in figure 3.42 is obviously the current jumps for I_{d2} of the right transistor. However, some other aspects of the graphs are worth noting. Note for instance that all currents exhibit a 1 to 2 nA random fluctuation (low frequency noise), but the dominant variations of the currents are definitely not random. Apart from the Id2_R jumps in figure 3.42, also a clear trend in the current variation is discernible in figures for all the other currents. This drift is probably associated with the (temperature related) drift of the measurement hardware, rather than temperature drift of the devices under test. The reason to believe this is primarily associated with the temperature variation rate. The maximum drift occurs between measurement 20 and 27, corresponding to about 3 minutes. It is not very likely that the temperature drifts inside the prober's micro-chamber could take place at the indicated rate. The measurement system itself however stood freely in the measurement lab, where the temperature changes are significantly faster (and larger). That most of the observed fluctuations are dominated by the measurement hardware rather than by the transistor noise, is evident as one notices the clear correlation between Id3_L and Id3_R. Several of the high and low peaks coincide in figure 3.42. This could be due to the state of the A/D converter that is used for the actual (Source) current measurements, but also caused by other common elements in the measurement set-up like the source voltage (@Common), the substrate (@ 0V) or the gates (@V_{GSi}). The jumps in Id2 are clearly the cause for the ΔV_T jumps in figure 3.41. This is seen by the fact that the ΔV_T jumps in figure 3.41 and the Id2_R current jumps in figure 3.42 occur at exactly the same observation number. The current jump apparently occurs at the point where

the current crosses the 11.6425 μA. If we follow the drift of the Id2_L, it is even visible that the Id2_R falls (temporarily) back to the lower level around observation number 37, but as soon as the other currents drift upwards again, Id2_R jumps up again. This is the clearest evidence that the jumps are really caused by measurement hardware drifts, and not associated with RTS like fluctuations. Note that the magnitude of the jumps (3.5 nA on 11.6 μA ≈ 300 ppm) is far too large to think of single electron trapping events associated with RTS: a 10x10 micron transistor with 6 nm T_{ox} at 0.5 V above V_T has approximately 2 million electrons in the channel. Hence, a single trapping event would have an impact of the order of 0.5 ppm on the current. An a-priori less unlikely explanation for the observed jump could have been that we are witnessing a meter-range transition artefact. Suppose that the initial current readings of the Id2_R (up to number 25) would have fallen in the high end of one range of the current meter, but as the drift of the system pushes all currents up slightly, suddenly the meter decides it must measure in the higher range. Due to offset and/or gain errors of the instrumentation ADC and Opamps, a jump of the order of 0.03% should not be deemed unlikely (and is, by the way, well within spec). Sure enough, according to the HP4156's spec documentation, the actual range change should be 11.5 μA, which is uncannily close to the observed value of 11.6425 μA. However, a closer inspection of other V_T mismatch measurements that showed evidence of such jumps ruled out this explanation, as for those devices the current jumps occurred at other levels, much farther away from the range transition. Hence, this leaves the suspicion to the other hardware components in the measurement system namely the DACs of the drain voltage sources SMU3 and SMU4 (figure 3.34). If we assume the 3.5 nA on 11.6 μA to be attributable to a voltage step on the 100 mV drain bias, we end up with a step of about 30 μV. On a full scale of 2 V (the range of the voltage source during this measurement), 30 μV (15 ppm) corresponds to $1/2^{16}$, which coincides with the least significant bit of the 16-bit DACs that are used in an HP4156 for voltage forcing!

Conclusion

Fortunately, problems like the ones discussed in this example are not always encountered. If they occur, they are usually not as significant as in this case. As long as the measurement repeatability standard deviation is small compared to the observed mismatch fluctuations, measurement repeatability problems do not have to affect the conclusions of mismatch studies. The reason why we went through all these extensive deliberations, lies in the fact that the decaborane experiment seemed so extremely well planned and processed that it appeared possible to characterise more subtle effects of the technological splits than is usually required for process characterisation and improvements. In fact, the (relative) outcome still is amazingly consistent as discussed in section 4.3 of this thesis. The nice outcome of the single pair repeatability assessment test in this example is that this proved an extremely lucky shot, with the one current accidentally drifting through the boundary resulting in the jumps of the ΔV_T. This study helped to explain what caused the nagging inconsistencies that became annoying when carefully analysing the bowl of data as represented in table 3.9. The main learning point was however, that during the original measurements a lot more attention should have been paid to the un-repeatability. In hindsight, it would have been wiser to use somewhat smaller transistors for the PMF study (hence higher mismatch fluctuations), and look better at the impact of the measurement conditions on the observed mismatch, but in the fire of the apparent success of this experiment, this was admittedly not done properly.

Chapter 4

IC process evaluation through matched pair characterisation

4.1 Introduction: Parametric mismatch fluctuations and yield

One of the consequences of the shrinking of device dimensions in the deep sub-micron IC technology era, is that parametric mismatch fluctuation (PMF) parameters have developed from an indispensable set of numbers for analogue electronic circuit design, into one of the limiting factors of high performance mixed-signal as well as digital VLSI systems.

Investigating and developing PMF assessments techniques, and providing PMF information for Philips' IC technologies, formed the major justifications for the start of the project underlying this thesis. The most important outcome of the work however, is that mismatch characterisation studies proved to be useful for obtaining insights into the microscopic structure of IC components. These insights were used to improve the PMF performance, but in several cases, they also contributed to the product yield of IC's running in major production lines. Parametric mismatch fluctuation studies can reveal microscopic architectural details about the fabrication technology, which are hard to obtain using other analysis techniques. Therefore, parametric fluctuation characterisation should form a standard element of the early process performance assessment for every new IC technology. Not only would this provide availability of parametric mismatch fluctuation numbers (for circuit design) early during the process development cycle, but it also provides the opportunity to improve the microscopic device architecture when the parametric mismatch fluctuation performances are not in line with reasonable expectations (potential yield loss!). The mismatch performance of any semiconductor device type is generally as deeply entrenched in the device architecture as the common process performance parameters like I_{on}, I_{off}, f_T, R_{pinch} or h_{FE}. Hence, it is usually not possible to repair poor mismatch fluctuation performance without compromising other process performance indicators.

A dilemma that inevitably goes with the desire to characterise the PMF performance early on, is that it should not be characterised too early. When a process is still under construction, electrical performance parameters can commonly be based on measuring a few well chosen golden devices, not seldom located in a particular (favourable) region of a wafer, and properly adjusted through guestimates and specmanship to represent the target performance. This approach is often unavoidable when working on a new technology, as circuit design of important lead products must generally commence long before the new IC process is stable and production ready. Parametric mismatch fluctuation characterisation on the other hand, must be based on a thorough statistical evaluation. This implies that much larger portions of each wafer must be measurable to bring statistical uncertainties to acceptable levels. Moreover, as these

statistical characterisation studies involve a lot of measurement and analysis time, they should not be started when there are severe doubts about the quality or volatility of the process[†].

Matching studies have proven to be helpful in terms of yield improvement of technologies. Besides for obvious matching limited circuits like high resolution DACs and ADCs [Pelg94], it may seem somewhat counterintuitive that parametric mismatch fluctuations, generally considered to contribute parametric spreads of no more than a few percents to the overall process spread window (tens of percents differences between corner models), can have significant impact on product yields. It must be realised however that microscopic device architecture fluctuations in contemporary deep-submicron devices can easily result in threshold voltage differences of several hundreds of millivolts in an arbitrary cell of a multi-megabit SRAM (figure 4.1). Such large differences can result in cell functionality failures.

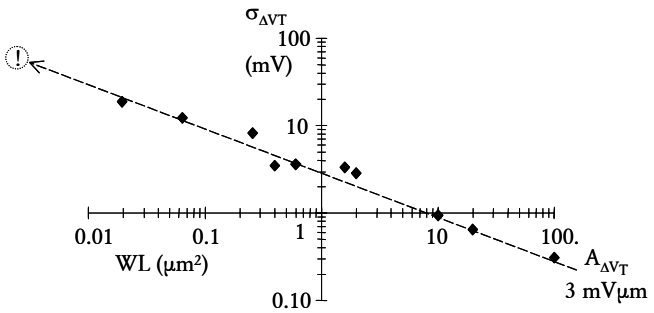

Figure 4.1 Example of measured PMOST threshold voltage mismatch fluctuations for a 0.12 μm technology (diamonds). Note that even a well-engineered 3 mVμm type of process would result in a one sigma threshold voltage fluctuations of the order of 60 mV for minimum device size (0.0024 μm^2) pairs in future (conventional 65 nm bulk CMOS) process generations.

One of the dangers of parametric mismatch fluctuation induced yield losses is that they can be misinterpreted as defects rather than a natural outcome of the statistical parametric fluctuations attributable to built-in microscopic device architecture fluctuations.
The combination of large number statistics (six sigma and more) and small device sizes is a natural stochastic reason why VLSI systems on chip with large embedded memories suffer

[†] On the other hand, process disasters provide exciting opportunities for mismatch research.

from yield losses. Another reason why mismatch studies can bring one on a track towards yield improvement, is that when looking through the mismatch magnifying glass (sub 1% parametric differences), the significance of seemingly minor effects can turn out to be more relevant than initially expected (figure 4.2). Moreover, neighbouring topography, metal coverage and local mechanical stress for instance, can unexpectedly prove to be serious performance degraders when it comes to small (sub 5%) mismatch requirements in analogue circuit applications.

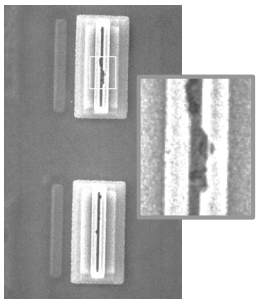

Figure 4.2 SEM pictures of a "de-processed" double-poly matched BJT pair with randomly distributed alloy pits in the emitter poly-Si that caused excessive mismatch. The same defects proved to be the root-cause of a significant product yield problem.

The remainder of this chapter discusses how parametric mismatch studies can help to improve performance and yield of IC technologies. Section 4.2 summarises the four main trouble signals that are useful for recognising abnormalities in parametric mismatch observations and statistical estimators. Subsequently, examples of typical mismatch characterisation studies are discussed. These were selected from the numerous interesting results encountered during this work.
The chosen examples are divided into three categories. Section 4.3 focuses on the occurrences of systematic mismatches and wafer position dependences as mismatch signals. Section 4.4 is about the difficulties and limitations of assessing mismatch fluctuation standard deviation area scaling factors and what that tells about microscopic device architecture fluctuations. Section 4.5 focuses on occurrences of significant deviations from the elementary $1/\sqrt{(\text{area})}$ behaviour and how the acquired insights proved useful for increasing the performance and yield of IC technologies.

4.2 Recognising mismatch trouble signals

The art of matched pairs mismatch characterisation and the associated evaluation of the processes that was used to build the devices, is not just a matter of precisely measuring many pairs and calculating the statistical fluctuation estimators. In the first place, it is about the ability to recognise and interpret signals that indicate that something is wrong with the fluctuation parameters. The four most important trouble signals that proved invaluable for recognising mismatch abnormalities as encountered in the 'limits of matching project' are discussed in this section.

Signal 1: Systematic mismatches

Systematic mismatch occurrences can be a signal that there is something wrong with the measurement system and/or that there is an (unexpected) asymmetry in the test structure. Always start by verifying that the systematic mismatch is not caused by the measurement method, and make sure that there are no obvious (unintentional) layout asymmetries or parasitic resistance differences in the layout implementation of the matched pair test structure. Re-measure the original as well as a comparable population, swap device terminals to rule out instrumentation offsets and determine the statistical significance of the estimator(s). If there still is evidence of statistically significant systematic mismatch, the combination of the test structure and the technology must be responsible and hence must provide an indication of the effect that causes the mismatch. Looking for differences between wafers, lots, or lot splits, as well as using alternative biasing or measurement techniques should provide insights on the mismatch mechanism.

Signal 2: Position independence

Theoretically, mismatch as measured using matched pair test structures should be independent of the position on the wafer. If this is not the case, and this was encountered several times in this work, this can provide valuable insights into the mismatch mechanism. Wafer position dependent (non-random) mismatch usually results in an increased mismatch standard deviation that may therefore be misinterpreted as being due to a microscopic fluctuation. When a significant wafer position dependence is detected, the mismatch cause is more deterministic in nature, hence pointing towards a different physical / technological / equipment cause.
After collecting the mismatch standard deviations for a range of device geometries, the area scaling graph of mismatch fluctuation standard deviations vs. $1/\sqrt{(\text{area})}$ can be compiled, and interpretation and guesswork can start. Figure 4.3 gives an impression of some examples of the dilemmas one is not seldom confronted with when interpreting Pelgrom plots.

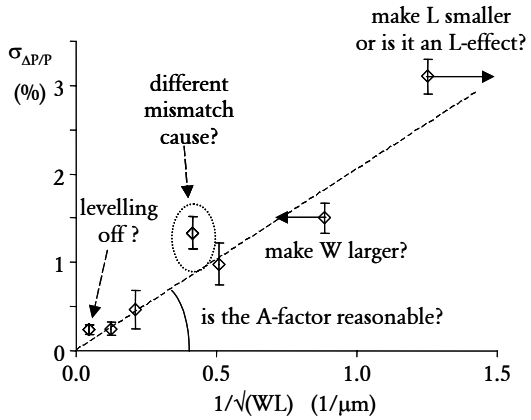

Figure 4.3 Arbitrary (artificial) example of a parametric mismatch fluctuation area-scaling graph.

Signal 3: Excessive A-factors for the large W & L devices
The prime parametric mismatch fluctuation indicator is given by the large area devices' A-factor (figure 4.2, 4.3). Parametric mismatch fluctuations are caused by intrinsic microscopic device architecture fluctuations. The best-known example is the fluctuation (Poisson statistics) of the number of dopant atoms in the active region of the device under test. However, more microscopic device construction elements, such as fixed oxide charges, interface states, layer thickness fluctuations, grain boundaries, line edge roughness, etc. fluctuate. When these fluctuations sources are statistically independent, the variances (σ^2) of their fluctuation contributions to the overall parameter fluctuations can be added, hence

$$A^2_{\Delta P} = A^2_{\Delta N} + A^2_{\Delta QF} + A^2_{\Delta QIT} + A^2_{\Delta QGB} + A^2_{\Delta Tox} + A^2_{\Delta LER} + \text{- - - - -}$$

Through comparing the best guess total A-factor with benchmarks, previous process generations, and theoretically derived matching numbers, the level is assessed. The challenge of improving the parametric mismatch fluctuation performance of technologies is in the first place to determine which of the fluctuation mechanisms dominates the A-factor, and whether it can be improved. In such cases, it is always important to assess expected A-factor differences as well as similarities between process splits and supposedly identical lots.

Signal 4: Deviations from the 1/√(area) model
When statistically relevant deviations from the elementary '1/√(area) model' are identified, it should be (and indeed generally is) possible to find feasible explanations for them.
Verify whether adjusting design dimensions to reasonable effective dimensions severely affects the perceived deviations (figure 4.3). Additional physical fluctuation causes generally increase the mismatch fluctuation standard deviation but they do not necessarily affect all device sizes to the same extend. Levelling off for very large devices (figure 4.3), another form of deviation from the elementary model, also is a warning signal. As this region corresponds to the smallest mismatch fluctuations, standard deviations in this region are the most difficult to determine correctly. Hence, levelling off can be an indication of poor measurement repeatability, poor test structure design, a problem due to large measurements currents, oscillations, etc. In theory levelling off can also be a distance (parametric gradient) effect. Large devices are farther apart and are hence more sensitive for (excessive) parametric gradients across a wafer.

4.3 Mismatch effects associated with metallisation

This section discusses the impact of metal features on mismatch. This obviously is a very important subject, as an integrated circuit can neither be made without metal connections to devices, nor without substantial amounts of metal routing fields between circuit building blocks. This section starts with a downright technology disaster. Subsequently it is shown that metal lines on, or near matched devices can easily result in systematic mismatches of the order of a few percents. Such systematic mismatches are caused by mechanical stress that is built in the wafer during aluminium sputtering. The section ends with a more subtle case in which is shown that even carelessly placed metal CMP dummy tiles can give rise to substantial systematic mismatches in high precision matched pairs. A characteristic feature of the lore of matching that is also demonstrated in this section, is that one must be very careful to port results and conclusions from one technology to another. The examples in this section clearly demonstrate that mismatch effects are very tightly related to the exact process architecture. Mismatch effects may show up in one technology and disappear again in the next.

A passivation anneal problem

This first example originated from a product yield problem that surfaced after shrinking an existing analogue circuit block from one process generation to the next. In this particular case, the matching performance of a set of common-centroid cross-coupled large-area MOSFET current sources of a D/A converter performed far below (matching) expectations. Although it was clear from the product's malfunctioning that there was a mismatch problem, it was not clear which step in the new process was responsible for this unexpected degradation. With some dedicated test structures the performance problem was analysed after which the process was improved which solved the yield problem. The original problem occurred in a circuit architecture (including the layout) that was copied from a working 0.8 μm CMOS generation circuit, duly adapted (shrunk) to the new set of 0.5 μm layout design rules. In this particular layout, a grid of metal-2 and metal-1 lines was used to construct the required binary multiples of a unit current in a common centroid cross-coupling scheme. Although this realisation with metal lines running partially over the channel regions of the MOSFET's worked fine in the 0.8 μm process, it was found that the metal running over matched transistors proved devastating for the mismatch performance in the next generation technology. This is a good example one of the typical learning cycles in the sometimes seemingly mysterious art of analogue integrated circuit layout. Although it is sort of known that metal lines running over matched components are in general not a good idea, the 0.8 μm process proved forgiving with respect to this offence. In [Tuin96b and Tuin97a] we reported the main results from this 'metal coverage study'.

The following sections focus in more detail on the typical mismatch signals in this study.

Test structure
The matched pair test structures were laid out in 2x9 pad frames as CS & CG matched pairs with asymmetric metal coverage (figures 4.4 and 2.30). A reference module containing 4 n-channel pairs and 3 p-channel pairs was copied 2 times and modified in such a way that in (the copied module) the left transistors of the pairs are (partially) covered with either metal-1 or metal-2 plates (plate tied to the Source of the transistor to avoid floating plates). In view of the product problem mentioned above, the study focussed on the possible impact of metal coverage on the mismatch for relatively large MOSFET's, with typical dimensions of 10/10, 10/4 and 2/10.

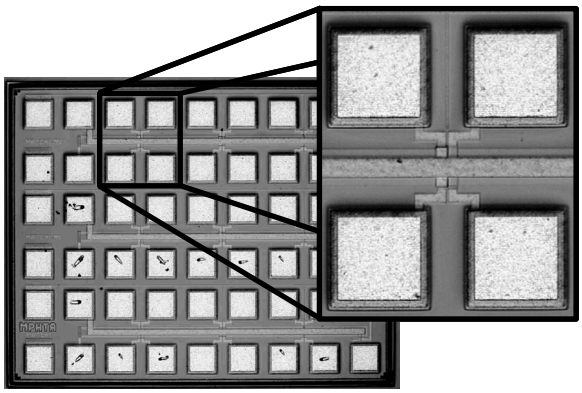

Figure 4.4 Matched pairs test module group for evaluation of asymmetrical metal coverage effects. Bottom 2x9 pad module without metal coverage; middle and top modules: Left transistor covered with metal-1 and metal-2 respectively. Right: matched pairs of which the left transistor is covered with metal-2.

Measurement method
As this investigation involved a rather gross mismatch effect, there were no challenging measurement precision requirements involved in this study. The current sources in the (DAC) application were biased in the typical analogue 10 - 100 μA range, so we chose a V_{GS}=V_{DS}=1.5 V saturation biasing for the statistical characterisation (yielding 30 μA for 10/10 n-channels, figure 4.5. left). A simple mismatch bias sweep ($\Delta I_D/I_D$ vs. V_{GS}; figure 4.5 right) already proves

more than sufficient to demonstrate that there is something severely wrong with these transistors covered with metal. Initially, it even was hard to believe that tens of percents differences could be attributed to the metal coverage of one of the pair's transistors. Several double checks were done to assure that test structures as well as all connections and hardware were in order. In [Tuin97a] several additional mismatch sweeps show that the magnitude of the mismatch also depends on the amount of metal coverage over the Gate.

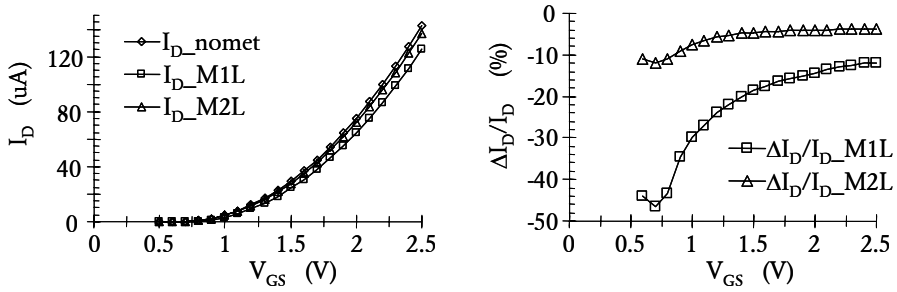

Figure 4.5 Left: Effects of metal-1 and metal-2 coverage on drain currents; Right: Mismatch sweeps of asymmetrically covered pairs.

Results and signals

Even with a simple single bias point mismatch measurement population, one can do more than just look at the standard deviations. Already while collecting mismatch sweeps by stepping across the wafer, a deterministic pattern in the magnitude of the metal induced asymmetry was noticed. To confirm this, populations of 45 drain current mismatch measurements (single bias point), both for asymmetrically metal-covered pairs as well as for pairs without any metal coverage were collected. This can easily be done using manual data collection, without semi-automatic probers or automated measurements. In a case like this, an initial investigation with rather gross effects, it is often quicker to spend an hour or so behind a probe station and a good parameter analyzer, with a piece of paper or a notebook, than spending several hours writing a fully automated measurement program. The cumulative probability plots for the two populations are shown in figure 4.6. The (safe) statistical mismatch estimators for the two populations are given in table 4.1.

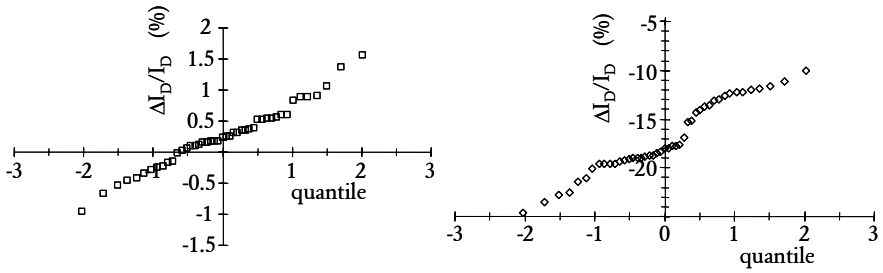

Figure 4.6 NSCPPs of drain current mismatch of pairs without (left) and with (right) asymmetrical metal-1 coverage.

nc10/10 pairs	no metal coverage	metal 1 on left MOST
median	0.24%	-18% !!!
standard deviation	0.39%	3.2%

Table 4.1 Drain current mismatch fluctuation estimators with and without asymmetrical metal-1 coverage.

The huge systematic mismatch for the asymmetrically metal-1 covered pair is obvious, while the standard deviation of this population also yields a dramatic increase compared to the pair without metal coverage. Another point worth noting is that the 'no metal coverage' distribution seems to form a much nicer Gaussian distribution compared to the one for the asymmetrically covered pairs. The suspicion that this is not a random fluctuation phenomenon is confirmed by the clear position dependence of the mismatch of the asymmetrically covered pairs.

Figure 4.7 gives a simple plot of the mismatch as a function of the chip-position on the wafer. In this particular experiment, only the upper-half of the wafer was available as the other half was undergoing an alternative treatment. The line with y=6 represents the dice just above the centre of the wafer, while y=10 formed the highest row of dice furthest away from the wafer's notch. This figure clearly demonstrates that the mismatch in this example is not random at all! A clear deterministic bull's eye pattern can be recognised. The mismatch near the centre of the wafer (-10 to -15%) is significantly smaller compared to near the edge of the wafer (-20 to -25%). From this graph, it is obvious that the observed (dramatic) mismatch standard deviation (figure 4.6 right) is not simply attributable to an enhanced contribution of a stochastic process, but largely caused by a deterministic variation pattern across the wafer. Although the statistical measurements do indeed confirm the suspected product problem cause, one should be careful

with the interpretation and quantitative outcome of these kinds of estimators as they depend strongly on which part of the wafer is measured. A simple four or five position drop-in selection (figure 2.1 a) would have resulted in an entirely different assessment of this problem compared to a full wafer evaluation.

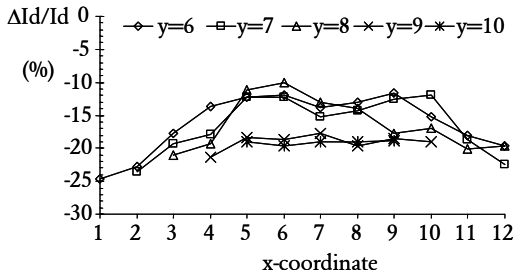

Figure 4.7 Position dependence of mismatch of asymmetrically covered pairs. Each line represents the mismatch of a row of dice. The caption corresponds to the y-coordinate of the row.

Discussion

Although this initial study was not exactly the most challenging matching characterisation project in terms of measurement accuracy, it eventually turned out to be extremely successful in terms of its impact on process yield of a process flow accepted for production. As discussed in [Tuin96b] it was found that the metal covered transistors were insufficiently (Hydrogen) passivated, leaving a large number of unpassivated dangling bonds (interface states) for the transistors that were covered with metal, resulting in a severely modified threshold voltage and current factor. The metal plates on top of the channel region of the transistors serve as diffusion barriers for hydrogen, while the Ti-TiN bottom layer also functions as a hydrogen sponge. The hydrogen passivation (forming gas) anneal at the end of the process flow was increased. Consequently, the observed mismatches decreased dramatically (figure 4.8) and the yield of several circuit blocks improved significantly. An interesting observation at this point is that a process artefact like this cannot easily be discovered using regular process evaluation test structures, as transistor modules will normally not be covered with metal plates. Nor would most technologists be very concerned with a few millivolts extra threshold voltage variation across a wafer due to interface states. Nevertheless, products and mismatch signals obtained from dedicated matched pair test structures do show there is something severely wrong with the original process.

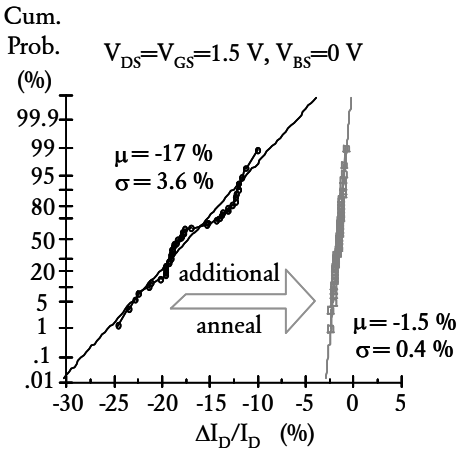

Figure 4.8 Conventional normal scaled cumulative probability plot representation of the effect of an additional forming gas anneal on mismatch observations for asymmetrical metal-1 covered MOSFET pairs (from [Tuin96b]).

Besides the results discussed above, follow-up studies of this initial work yielded some other very interesting matching related results that are discussed in the following examples.

Mechanical stress of metal coverage varies from process to process

After solving the major tens of percents mismatch disaster discussed above, it was observed that even after applying the enhanced passivation anneal, the systematic mismatch component did not disappear entirely (figure 4.8). In the original metal-coverage paper [Tuin96b], this was already attributed to mechanical stress. Mechanical stress effects in silicon were studied extensively for various application regions, ranging from active devices to packaging effects and of course sensors [Brad01, Bast97b, Mani00T]. The example discussed in this subsection demonstrates that metal coverage effects depend strongly on the back-end process architecture.

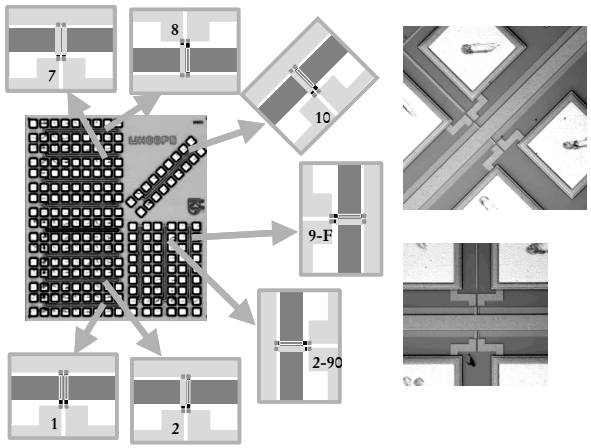

Figure 4.9 Whoops test structure with metal covered matched MOSFET pairs placed along five different orientations.

Test structure

This follow-up experiment was based on the same 2x9 pad module layout approach as in previous example; MOSFET pairs with several dimensions, left transistor covered with metal-1, metal-2 or metal-3 and reference pairs without metal coverage as well as with metal-1 on both transistors [Tuin97a]. The pair with asymmetrical metal-1 coverage is available in five orientations: regular (module 2 figure 4.9) and rotated by 45, 90, 180 and 270 degrees.
The test chip and some details are shown in figure 4.9.

Measurement method
As in the previous experiment, the measurements were done as single bias (V_{GS}=V_{BS}=1.5 V; MOSFET in saturation biasing) $\Delta I_D/I_D$ mismatch measurement; population size 99 pairs. This section focuses on measurements for the W/L=2/20 NMOST pairs, as these were found to be more sensitive for the orientation effect on the systematic mismatch than wide/long and wide/short devices.

Results and Signals
Figure 4.10 depicts NSCPPs of the drain current mismatch. The statistical estimators of the populations are given in the table 4.2.

The cumulative probability plots as well as the statistical estimators in table 4.2 indicate that the random fluctuations are quite comparable for the different structures. The medians of the distributions are statistically insignificant for the non-metal covered as well as for the symmetrically covered pairs. The asymmetrically covered pairs all yield statistically significant systematic mismatches. For the asymmetrical metal-2 covered pairs the impact (-5.7%) is large, for the asymmetrical metal-3 covered pairs the effect is significantly less (-2.3%) but still considerable.

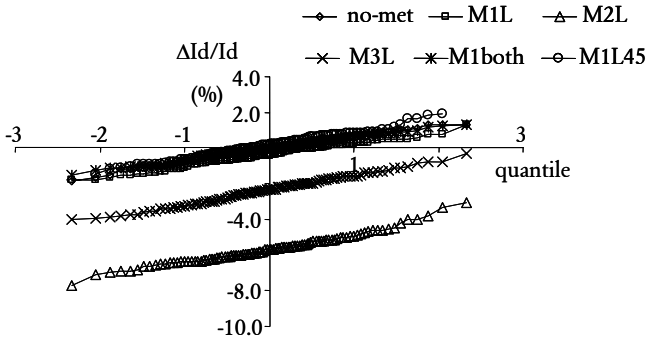

Figure 4.10 NSCPPs of drain current mismatch of pairs with different (asymmetrical) metal coverage and orientation.

nc2/20 pairs	no metal on pair (no-met)	metal-1 on both (M1both)	metal-1 on left (M1L)	metal-1 on left (45° rot.) (M1L45)	metal-2 on left (M2L)	metal-3 on left (M3L)
$\sigma_{\Delta ID/ID}$ (%)	0.62	0.56	0.58	0.63	0.69	0.74
$\mu_{\Delta ID/ID}$ (%)	-0.03	-0.04	-0.42	+0.19	-5.7	-2.3

Table 4.2 Drain current mismatch fluctuation estimators.

The systematic mismatch for the 45 degrees rotated pair deviates statistically significant (verified with bootstrapping) from the orthogonal oriented pairs. In [Tuin97a] we discussed that this is a convincing proof that this metal coverage mismatch effect is attributed to mechanical stress. It was shown by Bradley et al. that mechanical stress affects MOSFET's through mobility reduction due to the piezo-resistance effect [Brad01]. Although the estimated medians in table 4.2 are relatively large, no significant position-dependent mismatch effects were observed. This is exemplified in figure 4.11 for the non-metal pairs as well as for the asymmetrically metal-2 covered population. This implies that the mechanical stress (asymmetry) is practically constant over the wafer, which also explains why the mismatch standard deviations in table 4.2 are practically independent of the metal coverage.

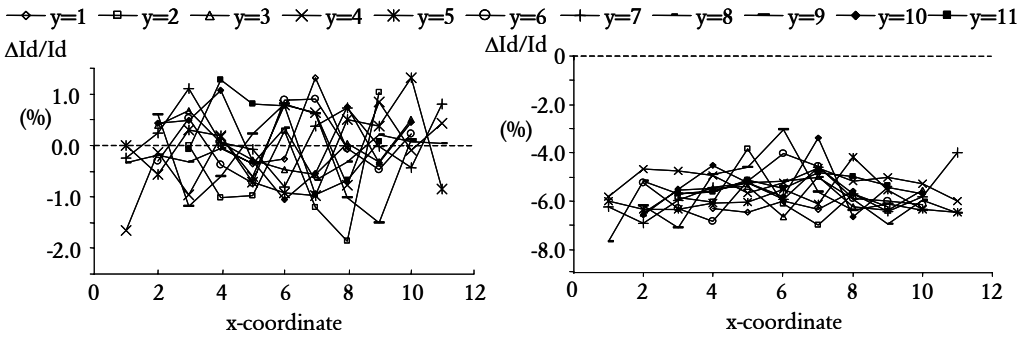

Figure 4.11 Examples of position (in)dependence of drain current mismatch as measured on rows of test chips. Left: no-metal coverage; Right: asymmetrical metal-2 coverage. The caption indicates the y-coordinate of the row

Discussion

Effects that have a significant impact in one technology may be less relevant in its successor and vice versa in the next. Good assessment of the relevance of a mismatch effect requires much better and detailed insight about the exact process architecture than can usually be obtained by circuit designers from design manuals and technology files. In the process flow for the first example of this section (a 0.5 μm CMOS triple metal process) the impact of asymmetrical metal-1 coverage proved the largest (and the impact of metal-2 and metal-3 measurable but much less severe). In the follow-up 0.35 μm CMOS technology however, the systematic mismatch for the asymmetrical metal-1 covered case is much smaller compared to asymmetrical metal-2 and metal-3 coverage. The explanation is given by the local stress differences caused by the different back-end layers. Indeed, quite significant process architecture differences can be found, when comparing the 0.5 μm process flow with the 0.35 μm process flow. The 0.5 μm process uses Ti/TiN - Al/Cu - TiN stacks for the three metal layers, while a Ti/TiN - W (plugs) - W is used for metal-1 and TiTiN - W (plug) - Al/Cu - TiN for the metal-2 and -3 layers in the 0.35 μm process. The thermal expansion (compression) and built-in stress of the metal-1 layer (CVD W) are apparently much smaller compared to the stress that is built-in during (relatively hot) Al/Cu sputtering in the latter process.

This example forms a good illustration why rules for matching performance often survive through historical design guidelines and horror stories of experienced circuit designers and technology developers.

An effect of CMP dummy tiles

A third example of the impact of back-end processing on MOSFET matching is the so-called CMP dummy tile effect. This effect was encountered while looking for ways to improve techniques for characterising small (systematic) transconductance mismatches in MOSFET's. This is reflected in the used test structure as well as the measurement method that went through considerable refinements in order to make sure that the observed systematic mismatch observations were indeed attributable to the devices and not caused by the measurement system [Tuinh00a]. To verify this, pairs with intentional (+ 1% and -1%) dimensional offsets were added, which was a novelty for matched pair test structures.

Test structure

As mentioned in chapter 2, the matched pair test structures preference had developed into CS&CG pairs in 1xM scribe line pad frame layouts (figures 2.32, 3.33, 4.23) by the time this experiment was conducted. And as this experiment demonstrates, the symmetrical connection frame indeed proves very suitable for studying subtle effects. The total MPW resulted in a measurable the population size of 45 on the (200 mm) wafers. The matching module was placed twice on the reticle. One of the secret hopes behind this double placement was that it would perhaps be possible to discern e-beam or laser-beam reticle-writing artefacts.

Measurement method

The measurement circuit is depicted in figure 3.34. The mismatch measurements were done using the fixed V_{GS} 3-point technique as described in section 3.6 of this thesis.

Results and Signals

As it turned out, even after assuring that all possible contributions of the measurement system were negligible or compensated, there appeared to be a much larger than expected (hoped) difference between distribution in the current factor mismatch of the two populations from the supposedly identical placements of the matching module (figure 4.12). The origin of this double distribution was traced back to a double placement of the mismatch characterisation module on a multi-project reticle. The observed double distribution proved to be attributable to an asymmetry of the CMP dummy tiles. Due to a combination of a slightly different CMP tile placement algorithm starting point and a layout artist who only removed the metal tiles on top of the transistors (figure 4.13) to avoid hydrogen passivation problems (as in example I of this section), a significant stress asymmetry was introduced in the #2 matched pair module. This case was discussed quite extensively in [Tuinh01b]. It is repeated briefly at this point to

emphasize that one cannot be careful enough to assure that the test structure is not the cause of a systematic mismatch observation, while on the other hand this also demonstrates that the occurrences of an unfortunate test structure accident can also turn into a useful warning.

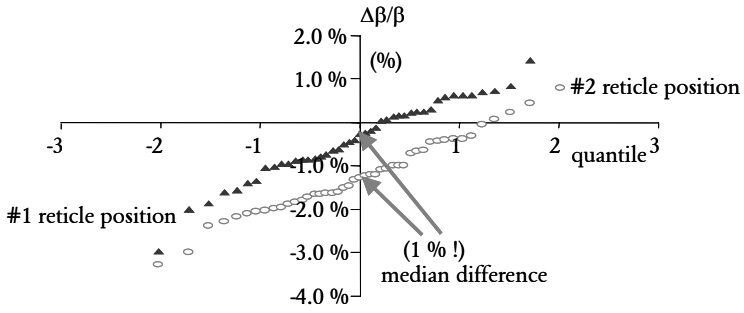

Figure 4.12 NSCPPs of current factor mismatch of two populations of pairs the same transistor dimensions on the same reticle.

A valuable outcome of this accident was that this (for the first time) created and justified awareness for the possible dangers of CMP dummy structures in high precision analogue circuit blocks. Consequently, additional chip-finishing rules were developed for well-matched analogue circuit blocks where mismatches are required below 5%.

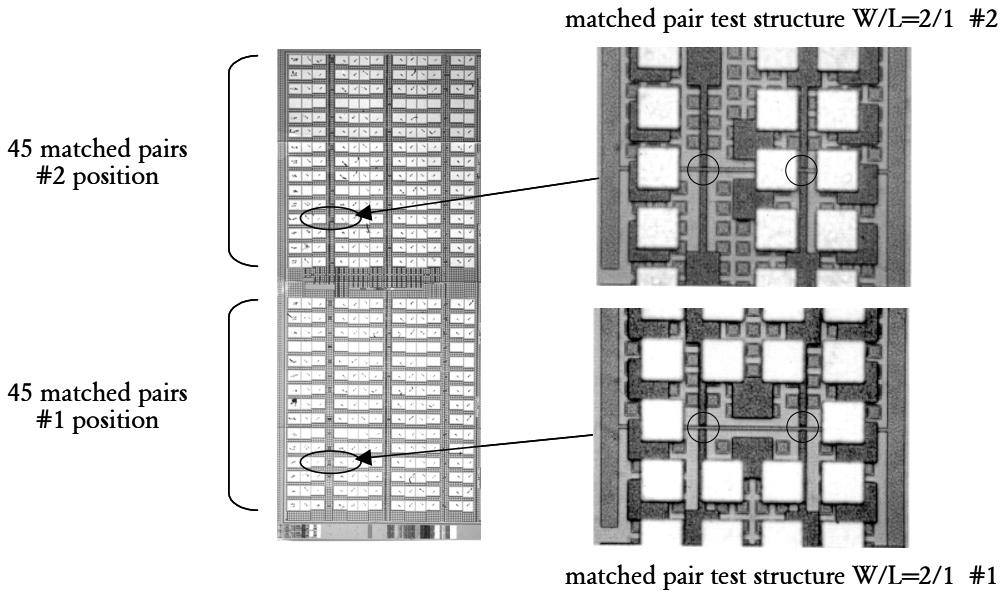

Figure 4.13 A 45-pair CMOS matching test module placed twice on the same reticle (left). Close inspection of the resulting instances revealed a significant asymmetry in the two placements due to a difference of the remaining metal-2 CMP tiles (white squares), which were removed from the transistors (inside black circles) to avoid hydrogen passivation problems.

4.4 Dilemma's of microscopic stochastic device architecture evaluation

Modelling stochastic mismatch fluctuations forms the most frequently revisited subject in the matching physics literature. It proves an attractive subject from a device physics standpoint, approachable through common semiconductors physics and calculus of statistics and can be simulated using statistical shells around 2-D and 3-D device simulation program. This implies that fluctuation models can be developed and evaluated relatively easily, without having to rely on complex technology experiments performed in expensive wafer fabs. The problem with such studies is however, that in reality it proves quite hard to obtain good quantitative agreement with measured fluctuations. The best (published) examples so far, are the studies of parametric fluctuations associated with the statistics of dopant fluctuations. Even for those it must be concluded that they can explain in most cases up to 50 percent of the observed fluctuations of real devices. Apparently, other fluctuation mechanisms contribute to, or even dominate, the real life fluctuations in integrated circuit technologies [Take97, Tuinh02b]. This assessment is not intended as mistrust in device simulations, but merely as a word of caution against their use. This opinion is largely based on the experience that stochastic fluctuations (as well as systematic patterns discussed in the previous section) often find their origin in unexpected physical or technological phenomena, which usually means that they cannot be predicted using device simulations. Obviously, (statistical) device simulations do form useful additions for enhancing the understanding of device (fluctuation) phenomena.

The most successful practical examples of evaluating stochastic mismatch fluctuations are based on comparisons against practical benchmarks, or on comparative performance optimisation studies within a particular process flow (wafer splits). Doing consistently the same, using the same test structure approach, the same measurement method (and hardware) and the same data analysis method, is the only safe way to compare statistical device fluctuation numbers. The following example discusses a successful experiment, in which we demonstrate the stochastic nature of dopant fluctuations in MOSFET's. The most spectacular results of this study, the decaborane experiment, were reported at the 2000 VLSI symposium [Tuinh00b]. Below, the project approach and results are discussed in more detail compared to the published paper.

The decaborane experiment

The decaborane experiment was set up to prove that on one wafer one can make two populations of devices with identical average DC device performance but with different -dopant fluctuation controlled- PMF characteristics.

The impact of dopant fluctuations on threshold voltage mismatch fluctuations has both been modelled [Laks86, Mizu94, Take97, Stol98] and verified using statistical device simulations [Stol98, Asen98]. Substantial experimental evidence has been published, showing that the principal relations of these models hold. It proves for instance very reassuring that V_T mismatch fluctuation scales more or less as expected over many CMOS process generations [Pelg98, Tuin02b]. Dopant increase experiments in large device matrices, as the one reported by Mizuno [Mizu94], also support the theory. The decaborane experiment aimed at manipulating the fundamental mechanism of the statistics of ion implantation determined dopant fluctuations through the introduction of a small range correlation of the microscopic disturbances. In popular terms, the experiment can be described as an attempt to degrade the threshold voltage mismatch fluctuations of n-channel MOSFET's using ion cluster bombs. By implanting ten boron atoms simultaneously rather than shooting single boron ions one at a time, enhanced fluctuation was anticipated when the implantation is performed with decaborane ($B_{10}H_{14}$) ions. Such clustering implies that one of the main assumptions underlying the Poisson statistics based derivation of the $1/\sqrt{(WL)}$ mismatch fluctuation area scaling law does not hold, namely that the individual microscopic disturbances are independent. Instead, due to the clustering of the disturbance, one can expect an enhanced fluctuation that can be modelled analogous to the conventional derivations by introducing a correlation factor (if the implanter misses once, it misses 10 times). To first order, one would expect that if all threshold-adjust implant atoms were implanted as a hypothetical mono layer in the channel, the decaborane implanted population would yield a square-root of 10 larger threshold voltage mismatch fluctuation.

Unfortunately, a first trial based on this decaborane idea did not bring the expected results. The devices with decaborane implants yielded only a marginal mismatch fluctuation increase (10 to 20%) compared to the regular boron implanted devices. The decaborane fluctuation enhancement contribution apparently drowned in other fluctuation effects. In this case, the flood was attributed to the relatively poor gate layer morphology at the time of the first experiment. As discussed in several publications [Tuin97b and Schm99], and summarised below in the next section, threshold voltage mismatch fluctuation of MOSFET's can also be affected quite strongly by the microscopic structure of the poly-silicon gate layer. Effects like

gate depletion, implantation tails through the Gate [Dubo02] and effects like the occurrence of charges and fast states or dopant fluctuations at poly-silicon grain boundaries [Difr01b, Difr03], were proven to be quite devastating for the threshold voltage mismatch fluctuation performance. After several process modifications to reduce gate depletion and eventually switching over to fine grained deposited poly-Si layers, good intrinsic matching performance (3-6 mVμm) for transistors with 3 and 6 nm gate dielectrics was achieved.
With this improved fluctuation performance, the decaborane experiment was repeated and this time with significantly more success. Mentioning this failed experiment first may seem slightly beside the point here. However, this comment was added as a demonstration of the dilemma that was introduced at the beginning of this chapter. On one hand, one cannot start early enough to monitor the matching performance of a technology, as it is determined by rather fundamental elements of the device architecture. On the other hand, one should not start too early to attempt subtle experiments and look for specific physical effects, as they may easily be drowned in other fluctuation artefacts of the technology under construction.

The experiment
Basically, the experiment consists of building different types of n-channel MOSFET's in a 0.15 μm like (C)MOS technology using different channel implantations. The regular (16 keV) boron threshold voltage adjust implant is replaced in selected populations of transistors by an implantation of decaborane ($B_{10}H_{14}$, Db) ions. The implantation energy of the decaborane ions (180 keV) was chosen to match the higher mass of the decaborane ion. Upon hitting the wafer, the decaborane ions immediately break-up (binding energy of the atoms is only an extremely small fraction of the kinetic energy of the accelerated molecules) and the individual boron atoms will proceed into the silicon with their own share of the original molecule's kinetic energy. The projected ranges of the resulting boron dopant profiles were thus practically equal for the 180 keV decaborane and the 16 keV boron implantations.

One could speculate whether the hydrogen atoms that are implanted together with the boron atoms when implanting $B_{10}H_{14}$ ions could have a beneficial (or even detrimental) impact on the transistor fluctuation performance. Hydrogen forms the indispensable passivation for dangling bonds at the silicon/silicon-dioxide interface in any MOSFET, hence the obligatory (N_2/H_2, Forming gas) passivation anneal at the end of any MOS technology. On the other hand, it is unlikely that hydrogen will remain in the silicon when it is implanted at the time of the threshold adjust as several high temperature steps are still required after the channel implant (gate-stack formation and anneals of high dose implants). To avoid uncertainties,

it was decided to add a third variant of the channel implant, namely a version where the 16 keV boron channel implant was accompanied by a 1.5 keV hydrogen implant. As before, the hydrogen implant energy was aimed at reaching the same projected range for the hydrogen atoms in the silicon as results from the (broken-up) decaborane ions.
The V_T adjust ion implantations details are given in table 4.4

group	dose low	dose high
B	$1.7x10^{12}$ cm^{-2} @16 keV	$3.5x10^{12}$ cm^{-2} @16keV
B + H	$1.7x10^{12}$ cm^{-2} @16 keV + $2.4x10^{12}$ cm^{-2} @1.5 keV	$3.5x10^{12}$ cm^{-2} @16 keV + $4.9x10^{12}$ cm^{-2} @1.5 keV
$B_{10}H_{14}$	$1.7x10^{11}$ cm^{-2} @180 keV	$1.7x10^{11}$ cm^{-2} @180 keV

Table 4.4 Ion implantation details for the decaborane experiment

The channel implantation profiles of modern CMOS processes usually consist of a cocktail of several implants like the threshold adjust implant, the (deep retrograde) well implant, an anti-punch through implant (APTI) and in deep sub-micron technologies usually a large angle tilted implant (LATID) halo or pocket implant. Only the dominant threshold adjust implant was modified in this experiment. The p-Well (boron) was implanted in all splits. Typical short channel effect reduction implants like the APTI and the halo's were skipped to avoid dilution of the expected V_T mismatch fluctuation enhancement. This rules out proper functionality of the shortest channel devices (below 0.5 μm) but is beneficial in terms of obtaining more pronounced fluctuation enhancement effects.

Test structure and measurement method
The 30 matched pairs on the used CMOS mask set (figure 4.14) were laid-out as CS&CG scribe lane module pairs (figure 4.15). As we expected to be looking for a typical $1/\sqrt{(area)}$ scaling mismatch effect (Poisson statistics of dopant fluctuations), looking at relatively large area device pairs was expected to suffice. Moreover, due to the absence of anti-punch-through implants or pockets, only the relatively long channel length devices (1 micron and larger) were measured. For the V_T mismatch fluctuation scaling plot the following geometries were selected: W/L=10/10, 10/4, 2/10, 10/1, 0.4/10 and 2/1. This provides a well-spaced set of observations on the $1/\sqrt{(area)}$ x-axis.

A standard linear region (V_{DS}=100 mV) fixed V_{GS} 3 point V_T extraction technique was used [Tuinh00a]. Before starting the statistical mismatch measurements, the shape of some transconductance curves were analysed and the three V_{GS} measurement points chosen appropriately. Practically all 'dose low' transistors yielded a threshold voltage between 0.29 and 0.31 V with a wafer spread (1 σ) of the order of 1 to 3 mV (10/10 devices). The fixed Gate-Source biases for these devices were chosen at 0.6, 1.0 and 1.8 V respectively. For the 'dose high' transistors 0.8, 1.1 and 2.0 V were used as these devices yielded threshold voltages that were typically 0.2 V higher than the 'dose low' devices. For the thicker oxide wafers the (1 σ) spread was somewhat higher (3 - 5 mV) compared to the thin oxide variants.

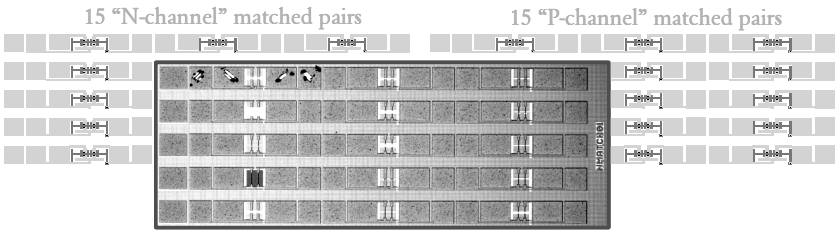

Figure 4.14 Two test modules with fifteen matched pairs each were available on the 0.15 μm CMOS technology development mask set. Inset: chip photograph.

The availability of two sets of matched pair test structures on the CMOS mask set (Figure 4.14) was exploited in this n-channel only experiment (see also table 3.9). Through appropriate (PMOST) mask usage, it proved possible to implant the single boron V_T-adjusts in one of the sets (N-MOST's or P-MOST's) while the corresponding decaborane or B+H implants were done in the other, on the same wafer. This removed all uncertainties about possible wafer split differences.

In a V_T mismatch measurement method comparison study, the used fixed bias 3-points technique was analysed and compared to other threshold voltage mismatch measurement techniques [Croo02a]. We demonstrated that this method yields a slight underestimation of the standard deviation. The typical threshold voltage sensitivity with respect to the gate bias point selection proved to be about 9 to 10 mV V_T change per 100 mV gate bias change (Table 4.6).

fixed V_{GS} biases (V)	median V_T for transistor 2 (V)	$\sigma_{\Delta VT}$ (mV)
0.5, 0.9, 1.7	0.287	0.42
0.6, 1.0, 1.8	0.298	0.44
0.7, 1.1, 1.9	0.307	0.42

Table 4.6 Effect of 3-point bias point selection on V_T extraction.

This sensitivity results in an underestimation of the mismatch standard deviation of about 10% [Croo02a]. Note however that the measured $\sigma_{\Delta VT}$ is practically independent of the gate bias conditions. The safe standard deviation estimation technique as discussed in chapter 3 was used for each (62 pairs) population. According to figure 3.29, this approach corresponds to another underestimation of the standard deviation of maximum 20%. Obviously, for (relative) comparisons of the different process architecture cases, such relative underestimations of the standard deviations have no consequence.

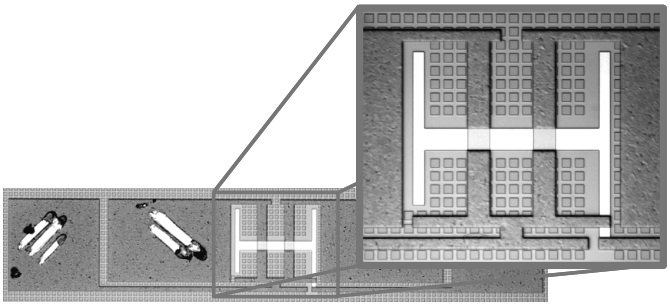

Figure 4.15 Microscope photographs of W/L=10/10 matched pair.

Parametric equality of the splits

Initial I-V measurement were done to check proper operation of the transistors and to verify that the transistors from a particular (T_{ox}, Dope_type) group indeed showed identical electrical characteristics. That this was indeed the case is demonstrated in figures 4.16. Both the output characteristics as well as the subthreshold curves show no perceptible differences between the three different dopant groups. Parametric (V_T) measurements (in this case part of the V_T mismatch fluctuation characterisation) also yielded (median) values that are practically identical, with a maximum difference of no more than 10 mV on a typical V_T of about 0.3 V for the

wafers with the thin (4 nm) gate oxide and 0.5 V for the thicker (6 nm) populations.
An example of the medians of the threshold voltages of the second transistor of each pair is given in the table 4.7.

Population	wafer	dopant group	median V_T for transistor 2 (V)
10/10"N"	8	Db (6L)	0.294
10/10"P"	8	B (6L)	0.298
10/10"N"	14	Db (4H)	0.486
10/10"P"	14	B (4H)	0.491
10/10"N"	20	Db (6H)	0.515
10/10"P"	20	B (6H)	0.519

Table 4.7 Good V_T agreements between different splits.

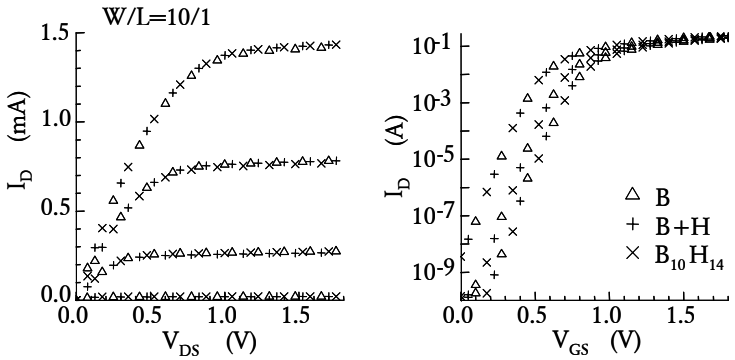

Figure 4.16 Perfect equality of DC characteristics of devices made with three different channel implantation recipes.

V_T mismatch fluctuation area scaling result
After verifying that the wafers were indeed functional and yielded identical transistor performance for the "N" and "P" modules, a typical wafer was selected for the initial mismatch fluctuation characterisation. In this case a wafer of the 'thin oxide & high dope (4H)" group was used. The area scaling results are depicted in figure 4.17.

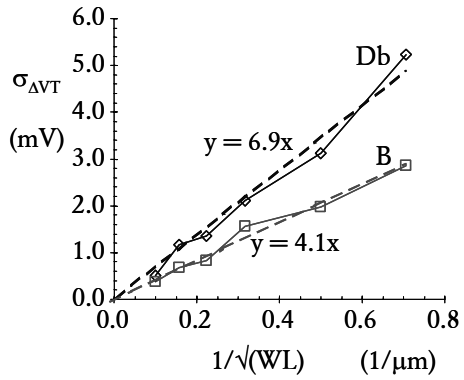

Figure 4.17 Mismatch fluctuation area scaling. Proof of fluctuation enhancements due to correlated dopant fluctuations.

The first and foremost conclusion that can be drawn from figure 4.17 is of course that there is indeed a substantial, and statistically significant, increase of the threshold voltage mismatch fluctuation, even though the dc performance of the transistors is not perceptibly different! This is exactly what we had hoped to see! A second observation is that there is a 6.9/4.1 (=1.68x) enhancement factor of the threshold voltage mismatch fluctuation due to the clustering effect of the decaborane ions implant. This is smaller that what one would expect. A first order guess would be √10. A more educated guess, taking the positions of the dopants and the contribution of the non-clustered part of the channel dopant (due to the p-Well) into account, yields a value of 2.13 [Tuinh00b], which still is substantially more than measured.

Dilemma: is it possible (and wise) to save measurement and analysis time by limiting the number of populations (device geometries) to be measured?

The mask set that was used for this experiment, in combination with the wafer size of 150 mm, yielded a population size for this experiment of 62 measurable test dice per wafer. The measurement time using the HP4156/C-M12k measurement system described in chapter 3 and the fixed V_{GS} 3-point measurement method for a single W/L population of pairs (124 transistors), is approximately 15 minutes including wafer stepping and statistical analysis. Normally this is an acceptable measurement time for assessing the mismatch performance

of a population of devices. As one would normally characterise between 5 and 10 transistor geometries and a couple of wafers to assess the mismatch fluctuation performance of a particular device type, this adds up to about 2 to 3 days of measuring (with plenty of time to analyse the data on the fly). In the decaborane experiment however, we were in fact dealing with 48 different cases. If we had wanted to do a full area scaling characterisation (at least 6 geometries) for each case, this would have resulted in unacceptably long measurement and analysis time on our research measurement set-up. Therefore, we fell back to the simplest mismatch fluctuation area scaling analysis approach, namely measuring the mismatch fluctuation standard deviation of one single (large) transistor geometry. In this case we used the W/L=10/10 transistor pairs (figure 4.15), which means that an $A_{\Delta VT}$ is simply calculated by taking 10 times the estimated standard deviation. The risk of this simplified approach is twofold. In the first place, one could be concerned about the measurement accuracy. The expected threshold voltage fluctuations in this experiment are of the order 0.5 mV for 100 μm^2 devices. This may seem fairly low, but from earlier work [Tuinh00a] we know that the measurement repeatability of the used system and measurement algorithm was typically better that 50 μV for 10/10 n-channel transistors, so that should not be a problem. The choice of the transistor geometry for doing such a single transistor A-factor estimation is a trade-off between several conflicting arguments. On one hand, the V_T mismatch measurement repeatability will become less of an issue when a smaller geometry is used as their fluctuation magnitude increases with $1/\sqrt{(WL)}$. On the other hand, one needs a sufficiently large transistor to meet the central limit theorem requirements that the correlation distance of the disturbances is small compared to the device size. This will never lead to problems when dopant fluctuation type of disturbances is causing the mismatch fluctuations. A more relevant reason to stick to large devices is to avoid the possible impact of edge effects, both in the L-directions (short channel contributions and/or edge roughness effects) as well as in the W-direction. Since in this particular experiment the pockets and/or anti-punch-through implants were omitted, shorter channel-lengths were avoided. As discussed in the example of the previous chapter of this thesis, in hindsight it would have been better if the W/L=2/1 transistor pair would have been used for the screening of all wafers. Another reason why it can be dangerous to use only one single geometry for estimating the A-factor of a particular process architecture split is simply given by the fact that the statistical uncertainty due to the limited population size becomes a limiting factor. Even for a seemingly acceptable population size of 62 pairs this can form a serious limitation. This can already be observed in figure 4.17. Although the $1/\sqrt{(WL)}$ behaviour seems to hold quite well, even at this scale one can distinguish relatively large deviations of individual populations. In particular the lowest point for the decaborane observations

(W/L=10/10 hence $1/\sqrt{(WL)}=0.1$) falls significantly below the fitted line: whereas the 6.9 mVμm fit predicts a sigma of 0.69 mV for this geometry, the measurements yielded a value of 0.50 mV. In the decaborane experiment, the statistical uncertainty could be reduced significantly by combining (up to 4) identical populations. The 24 wafers in the lot and the availability of two individually implantable modules per wafer ('NMOS' and 'PMOS') resulted in 48 populations that could be spread out over the 12 different splits (3 implant recipes x 2 doping levels x 2 oxide thicknesses). Unfortunately, not all wafer survived their long and dangerous route through a research clean room, but those populations that did come through were combined to decrease statistical uncertainty levels as much as possible. Some of the struggles that accompanied this approach were treated in depth in the example of chapter 3 of this thesis.

Results

Figure 4.18 summarises the threshold voltage mismatch fluctuation standard deviations for all process splits. The success of the total experiment is clearly proven by figure 4.18. The three features that we were looking for are clearly visible.

- The threshold voltage mismatch fluctuations of the decaborane populations unmistakably stand out in each of the four groups, while the Boron and the Boron+ Hydrogen groups are perfectly equivalent.
- The impact of the dielectric thickness split (4 nm in groups 1 and 3 vs. 6 nm in groups 2 and 4) is of the right order.
- The theoretical $N^{0.25}$ effect of roughly doubling of the channel dopant concentration is clearly distinguishable (groups 1 and 2 vs. 3 and 4).

The (3 sigma) statistical uncertainties for each group, derived by bootstrap analysis, are indicated in figure 4.18 by the error bars. The uncertainties are not equal for all groups. This is partly due to the natural statistical variation in the populations. Moreover, not all groups could be based on the planned four populations, hence automatically implying larger uncertainties. Finally, not all measurements showed equally good measurement repeatability, due to an instrumentation drift problem during the measurement period. Unfortunately, many parametric fluctuation studies fail to indicate the statistical uncertainties that should accompany any (statistical) study. In fact, figure 4.18 demonstrates why it may be tempting to omit statistical uncertainty intervals, as the interpretability of the results definitely leaves a lot more room for uncertainty compared to when the error bars are omitted. This is a typical limitation

of matching studies. There practically always are substantial uncertainties due to test structure, measurement system and statistics. It occurs quite seldom that one is able to derive numbers with less than 10 to 20% uncertainty.

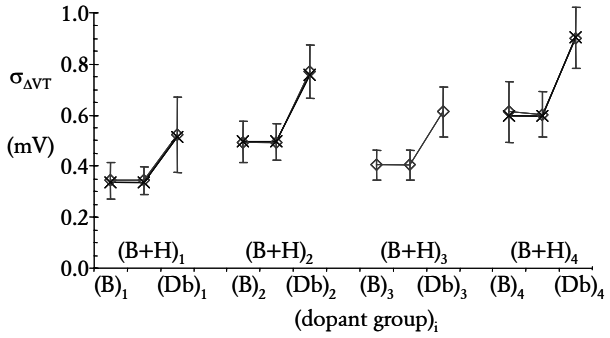

Figure 4.18 V_T mismatch fluctuation standard deviations for all 12 splits in the decaborane experiment. Diamonds: measured estimators including (3-sigma) bootstrap uncertainty bars. X's: predictions for groups 1, 2 and 4 extrapolated from group 3 results.

Despite the discussed dilemmas and uncertainties, the decaborane experiment as summarised in figure 4.18 still represents an exceptionally successful experiment. In the first place, of course by its fascinating prime result, namely that it indeed proved possible to manipulate the statistics of dopant fluctuations. Moreover, the overall consistency of the total experiment appears to defy the uncertainty that should be expected in experiments like these. To demonstrate this latter point, figure 4.18 also contains the theoretical relationships between the four main technology groups. Common MOSFET threshold fluctuation theories all yield some form of the equation $A_{\Delta VT}$=c T_{ox} $N^{0.25}$. The X's in the figure represent the prediction for groups 1, 2 and 4, when the results of group 3 (T_{ox}=6.2 nm effectively, high dope) are used as anchor (calibration) points. Each of the other standard deviations are calculated by multiplying the equivalent dopant species group with T_{ox},i / (4.2 nm) and/or (Dose,i / 3.5E12)$^{0.25}$. The agreement in figure 4.18 speaks for itself: an exceptionally impressive conformation of the common dopant fluctuation theory.

4.5 1/√(area) scaling deviations

The elementary 1/√(area) relationship between the parametric mismatch fluctuation standard deviation and the active area of the devices under test appears to be the only serious point of dispute in the matching / parameter fluctuation literature. While some papers (proudly) present that the area scaling of their measured (or even simulated) standard deviations displays good 'Pelgrom-like' behaviour (as it is often called), others claim that this behaviour is certainly not always observed and therefore almost by definition irrelevant. Some of the backgrounds behind this debate were already discussed in section 1.2 of this thesis. However, there is no reason to assume, that either of the two claims is wrong. Indeed, significant deviations from the elementary area scaling behaviour are frequently encountered. Nevertheless, as is for instance evidenced by many of the graphs shown in this thesis so far, there is good reason to believe that the 1/√(area) relationship is not entirely useless. In fact, there are two ways of looking at deviations from the elementary scaling rule.

On one side, there is a (compact) device-modelling standpoint, particularly advocated by Drennan et al. in [Dren98] to [Drenn03]. From this perspective, it is not relevant what causes such deviations. By adding width, length and area relations, while assuring a physically and statistically solid extraction approach (for instance called backward propagation of variance, BPV), it proves possible to assure that circuit designers can expect the maximum precision in their statistical circuit simulations. The physical causes underlying the observations are not important in this case, and when a well-chosen set of parameters, or combinations of parameters can do the job, fine. No need to worry about improving the process, nor for being able to predict the performance of the next process generation.

An entirely different way of looking at area scaling irregularities is to approaches them from a technology architecture evaluation point of view. The assumption then is that such irregularities may learn something about the device construction of the matched components. One of the earliest theoretical derivations of the relation between physical device architecture elements and mismatch fluctuation standard deviations by Lakshmikumar et al. [Laks86], in fact already argued that some fluctuation sources result in perimeter dominated (or enhanced) standard deviations (including $\sigma_W/\sqrt{(W^2)}$ and $\sigma_L/\sqrt{(L^2)}$ terms). Several works that are more recent discuss enhanced MOSFET threshold voltage mismatch standard deviation as typically observed for short-channel devices [Love96, Bast97a, Difr00, Difr02]. In these studies, the larger standard deviations for short transistors could be explained by properly adjusting the effective dimensions (as is common for short channel depletion charge sharing effects on the threshold

voltage), or by increasing effective channel doping (due to the so-called halo- or pocket-implantations). These are examples where the traditional fluctuation mechanism (dopant fluctuations) is assumed the main cause for the observed parametric fluctuations, but that slightly modified input parameters are required as the effective device construction elements change in the small geometry regions.

In fact, it was in one of our own studies based on poly-Si gate morphology experiments [Tuin97b], where it was first reported that enhanced (and reduced!) mismatch fluctuation standard deviations could indeed be attributed to an entirely different physical device construction element. In this particular study, the microscopic device fluctuations (the grain boundaries in the poly-Si gate of a MOSFET) have a much larger correlation distance than the conventional (dopant fluctuation dominated) fluctuations. This refers back to the fourth of the basic assumptions that are required to meet the central limit theorem underpinning Pelgrom's approach as discussed in section 1.2. When the size of the stochastic disturbances is of the same order of magnitude as the devices under test, the parametric fluctuation standard deviation as a function of the device size will not necessarily follow the $1/\sqrt{(\text{area})}$ scaling behaviour. It were in fact the surprisingly consistent (RTA) controllable deviations from the elementary area scaling model that helped the interpretation of this new mismatch fluctuation mechanism into the correct direction.

The remainder of this section discusses three examples of area scaling that deviates significantly from the conventional $1/\sqrt{(\text{area})}$ law. The first, somewhat inconclusive albeit very realistic example discusses the common dilemmas one is often confronted with in such cases. The second is formed by the study mentioned above, where the impact of the poly-silicon gate morphology on PMF was first encountered. This study led to major improvements of the microscopic device architecture of the MOSFET's in the technology where the effect was discovered, as well as for all its successors. The third example discusses a case where unexpectedly large base currents mismatch fluctuations in BJT's, led to the identification of a process weakness. This process weakness turned out to be a product yield limiter that was eliminated along with solving the mismatch disturbance.

Analysing minor (?) area scaling deviations.

This first example discusses some of the common dilemmas one is confronted with when drawing a 1/√(area) area scaling graph. When is a deviation real? Does it mean something? Is there a problem with the measurement system or the algorithm? This example is based on the threshold voltage mismatch observations on a wafer from an (experimental) 0.25 μm (6 nm T_{ox}) CMOS process flow. The original results are presented in figure 4.19.

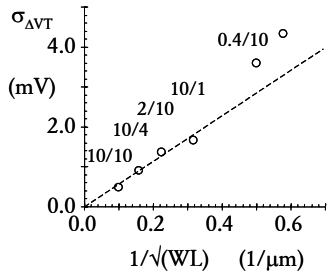

Figure 4.19 Threshold voltage mismatch fluctuation area scaling of n-channel MOSFET's for a 0.25 μm CMOS wafer. Drawn transistor dimensions are indicated next to the measured values. Dashed line forms the best guess (5.7 mVμm) A-factor based on the four largest geometries.

Test Structure

The test structures on this particular mask set were laid out in a conventional 2x9 CS&CG pad frame arrangement (figure 4.20). The two modules provide space for 14 NMOST pairs, which include some distance and orientation test pairs as well as a couple of QUAD pairs. The mismatch area scaling extraction set consists of the following pair geometries: W/L= 10/10, 10/4, 2/10, 10/1, 0.4/10 and 10/0.3. The four largest geometries are typically used for assessing the area-scaling factor.

Measurement method

All devices were measured using a standard linear region 3-point extraction technique (fixed V_{GS}). Gate biases were chosen at 0.9, 1.4 and 2.5 V. The V_{DS} was 0.1 V while V_{BS} was 0 V for all measurements. Each population consisted of 81 samples. The standard deviation estimators were calculated using the safe estimation procedure (section 3.5).

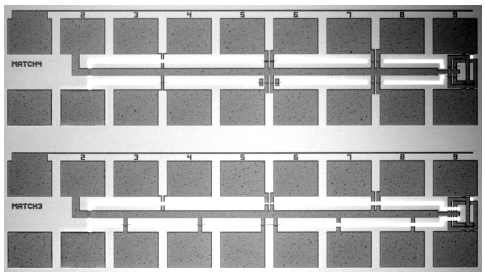

Figure 4.20 Two 2x9 contact pad matched pair test modules.

Results and Signals

The threshold voltage mismatch standard deviation area scaling graph as depicted in figure 4.19 yields several of the typical mismatch signals discussed in section 4.2. If one begins with the good news, there obviously is the excellent performance of the threshold voltage mismatch fluctuation. According to the practical MOSFET V_T mismatch area scaling benchmark (1 mVμm/nm T_{ox}) [Tuinh02c], a value of the order of 6 mVμm should be anticipated for this type of technology. These devices indeed yield a quite acceptable 5.7 mVμm (figure 4.19).
At the time of these measurements were done (October 1996), this represented the lowest V_T mismatch fluctuation A-factor ever encountered on any CMOS wafer.

Second point worth noting in figure 4.19 are the higher standard deviations for the narrow/long (0.4/10) and wide/short (10/0.3) pairs. This brings a typical statistical mismatch characterisation dilemma: Is this a real effect? Can it be explained? If so, is it something to worry about?
The points are clearly above the line derived from the large transistor dimensions. Safe estimation (range filtering & blunt axing) was used as the standard analysis technique for these measurements. However, the bootstrap statistical uncertainty information was not derived for this data set. This is an example of reason why in later stages in this work, it was decided to add the statistical uncertainty assessment as an integral part of the measurement / analysis algorithms [Ewer05]. The theoretical statistical uncertainty of a population of 82 ($1/\sqrt{(2N)} \approx$ 8%) is not sufficient to explain the deviation. On the other hand, a number of approaches can be taken for observations like these.

- Check statistics. Obviously, the first check for such mismatch fluctuation increases is to verify position dependence (randomness) and check for outliers. In this case, neither statistical irregularities nor significant position effects were observed.

- Adjust effective device dimensions. The effective areas could deviate significantly from the documented value. This could be due to a design (layout) error, a documentation error, a mask (resizing) error, or a technological reduction of the dimensions (for instance due to litho and etch or a wrong thermal budget). Note that in figure 4.19, and in many of similar cases, the horizontal axes are based on the designed W and L, hence not on the effective dimensions that should obviously be used from a device physics perspective. For an initial check as in this case, this is usually good enough, for a detailed scientific study or an accurate device modelling task, the effective dimensions should always be used.

Figure 4.21 a shows the area-scaling graph if a ΔL of -0.13 μm and a ΔW of -0.15 μm are assumed. Although this may seem tempting at first sight (engineers like simple straight lines), obviously CD offsets this large are not realistic for a 0.25 μm technology! Note however, that it has been suggested in matching circles that mismatch area scaling deviations could be a way to actually determine effective dimensions. This example illustrates that this is not such a good idea, besides from the fact that there definitely are easier ways to determine effective dimensions than one based on mismatch measurements on several hundreds of devices.

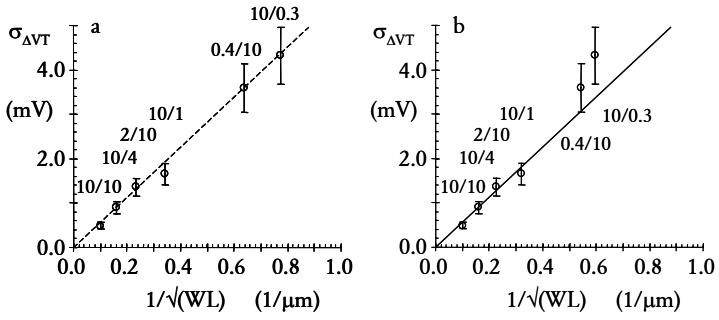

Figure 4.21 Playing with effective dimensions. (a):best fit ΔW=-0.15 μm, ΔL=-0.13 μm.
(b): best guess ΔW=-0.06 μm, ΔL=-0.02 μm. Error bars represent fixed (15%) uncertainty estimates.

Based on the simple area scaling formula $\beta=\beta_{sq}(W+\Delta W)/(L+\Delta L)$, and using the average beta's as measured with the three-point extraction (table 4.9), values of -0.06 for ΔW and -0.02 for ΔL were calculated in this case, which are more reasonable from a quarter micron technology point of view. The V_T mismatch fluctuation area scaling with these effective dimensions is depicted in figure 4.21 b. Clearly, using realistic effective dimensions is also not sufficient to explain the enhanced mismatch for the small dimension devices, even when a statistical uncertainty of as much as 15% is assumed (error bars in figure 4.21)

W/L (μm/μm)	median V_T (V)	median Beta (A/V^2)
10/10	0.566	3.03E-4
10/1.0	0.593	2.87E-3
10/0.3	0.597	9.94E-3
2.0/10	0.566	5.21E-5
0.4/10	0.569	9.08E-6

Table 4.8 some parameters of n-channel transistors from the 3-point extraction.

- Device over-scaling. Another explanation for the higher standard deviations of the small dimension device populations would be to assume that the excessive fluctuations are due to the traditional short and narrow channel effects on the threshold voltage [Love96, Bast97a, Difr02]. However, the values of the medians of the main parameters coming from the 3-point extraction given in table 4.8 provide no evidence that the measured devices are in excessive short or narrow channel transition regions. If anything, the shortest devices are in the rising part of the traditional V_T-roll-off curve (average increase of the substrate doping due to pockets- or halo-implants). Note that a 26% higher standard deviation can be explained by a 2.5 times higher average dopant according to the standard $N_A^{0.25}$ formula's. This would have been a plausible explanation for this case, were it not that this process generation was not equipped with pockets. Equally confusing is the observation that the narrow-channel effects on the V_T are practically negligible, so a dopant increase or reduction also does not seem a viable approach to describe the enhanced fluctuation for the narrow-channel devices.

- Line edge roughness. Enhanced fluctuations for small dimension devices are attributable to what is often indicated with the term line edge roughness (LER). These are dimensional irregularities that can be attributed to a collection of edge-related process steps ranging from photo mask raggedness, to photo resist exposure and plasma etch induced edge

fluctuations. Line edge roughness is currently one of the fashionable subjects in the CMOS process characterisation field. By pushing state of the art photolithography processes to the extreme, the industry is reaching device dimensions well below 40 nm without having to go to (even more expensive) radically different exposure approaches. By pushing the current techniques to the limits, with extra high sensitivity resists, lower exposure doses and contrast enhancement techniques, one is bound to run into more vulnerable process conditions where it comes to fluctuations. The number of photons and/or photosensitive chemicals required to expose the resist approaches such small values that also here Poisson statistics must apply.

In fact, this pushing beyond the limits of the photolithography process capabilities is practically always the case in research labs and IC process development lines. In the early (development) phases of the process' life, dimensional spreads tend to be large compared to when a process reaches maturity in a well yielding volume production fab. This is one of the reasons why one should always be careful not to spend too much time modelling excessive mismatch standard deviations for small dimension devices in the early stages of process development. By the time 'process engineering' is finished with their yield improvement fine-tuning of the process, most of these uncontrolled dimensional fluctuations are reduced significantly. Circuit yield is often affected very strongly by CD control, which make litho optimisation an attractive target for Process Engineering. This warning not to embark on detailed modelling early on does not mean one cannot take a good look at the data, to figure out if there are any additional indications about the possible causes. In particular, one should keep a close look at the position dependence of the mismatch, but it can also be quite instructive to make some scatter plots between the length and width related parameters such as g_m or beta and the V_T mismatch. When an enhanced fluctuation is encountered that is suspected to be related to dimensional variations, it is most likely that the parametric (dimensional) gradients over the wafer are quite substantial (more than 20% across a wafer), which indicates that the litho and etch processes are being exploited at, or beyond the edge of their capability range. When such exploitation is the case, correlations between Beta and ΔV_T and Beta and ΔBeta/beta are likely to be significant. In the example discussed in this section, no significant evidence was found of such correlations. Obviously, the designed dimensions (0.4 μm for the narrow W and 0.3 μm for the short L) are also not extremely challenging the litho limits of a potential 0.25 μm technology.

- Additional fluctuation causes. Finally, a statistically significant increase of the mismatch fluctuation such as the one encountered for the narrow/long n-channels of figure 4.19 can

also be due to the manifestation of an additional fluctuation component. If one could envisage for instance, a microscopic fluctuation source that is specifically associated with the field-isolation sidewalls of the transistor (such as additional interface states at the field isolation corner, higher doping, or a side-channel along the sidewalls), one can imagine that the parametric mismatch fluctuations also increase for narrower devices. Normally spoken one would expect that this would go together with significant changes of the main parameters themselves, hence, careful correlation analysis between various parameters and mismatches should provide hints where to look in the microscopic device architecture. As mentioned before, no such evidence was found for this particular set of n-channel populations.

The deliberations above are presented here as an example of possible lines of thinking during the evaluation of a common example. Obviously, it is acknowledged that in the five explanations above, no satisfactory answers are found to make firm conclusions on a study like this would normally mean that a significant effort would be required to find the cause of such a mismatch fluctuation enhancement. More wafers, from the same lot, as well as comparable wafers from other lots, preferably with edge-related process splits, would be required to reveal additional indications of the fluctuation causes. In cases such as the n-channel populations of figure 4.19, it is questionable, at least according to our experiences, whether the source can ever be identified. The effect is not dramatic either, hence from a modelling standpoint, one is in practice often better off by simply adding an additional fluctuation parameter, or use compact parameter binning to improve the predictions of the statistical device simulations for these narrow n-channel devices, should this turn out to be a recurring observation.

The impact of poly-silicon gate morphology on PMF

The poly-Si gate morphology investigations in fact took off when the p-channel matched pairs were measured on the wafer that was discussed and analysed above. The enthusiasm for the wafer (see Results and Signals of the previous analysis) diminished quite rapidly, when the V_T mismatch standard deviations of the p-channels (on the same wafer!) proved so much larger, that it was originally suspected that the measurement algorithm (or system) was malfunctioning. Several re-measurements and checks were performed to verify the results, but indeed the result stayed at a rather horrifying 20 mVμm (figure 4.22 b). This formed the alarm signal that triggered an extensive project that resulted in highly interesting results [Tuin97b], as well as invaluable CMOS process improvements.

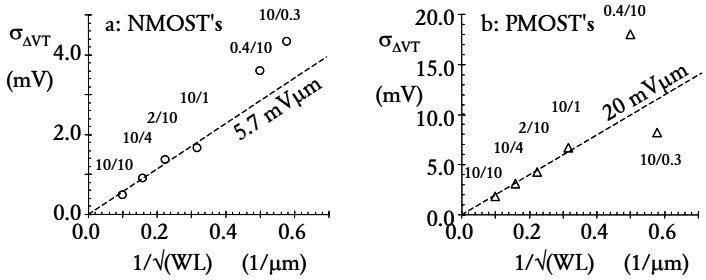

Figure 4.22 Threshold voltage mismatch fluctuation area scaling of n-channel (a) and p-channel (b) MOSFET's for a single 0.25 μm CMOS wafer. Drawn transistor dimensions are indicated next to the measured values. Dashed lines form the best guess A-factors based on the four largest geometries.

Test structure and measurement method

The same test structure design and measurement methods were used for the p-channels as for the n-channels, be it that all biases were obviously reversed and preferred gate biases were adjusted. For these devices, following three sets of gate biases were applied: [-0.9, -1.4, -2.5 V], [-1.0, -1.5, -2.5 V], or [-1.1, -1.6, -2.5 V]; depending on the threshold voltage and the shape of the transconductance characteristic. The lowest point is always chosen at, or slightly above, the peak transconductance point and the highest at the V_{DD}.

Results and Signals

The threshold voltage mismatch standard deviation area scaling graph as depicted in figure 4.22b yields two of the typical mismatch signals discussed in section 4.2. The first and foremost signal is the devastatingly high A-factor (20 mVμm) that is at least a factor three too high for this process generation. Note that the n-channel results (figure 4.22 a; same data as in figure 4.19) were obtained on the same wafer! Differences between the matching performance of n- and p-channel devices were reported before [Pelg89], but a discrepancy as large as depicted in figure 4.22 on the same wafer simply seemed impossible. Not many analogue designers would be willing to design in a process like this, so this was really a problem to address. Moreover, whereas mismatch increases of the order of 20% as discussed so far for the n-channels in this section are always hampered by the fact that one is discussing and improving in the margins of the field, working with a factor three improvement room is really an area where one can see the benefits, should this indeed be resolved. A good analogue circuit designer will probably have a little extra safety margin in his Monte-Carlo statistical simulations to safeguard against unknown, or poorly modelled effects like the 20% case discussed in the previous section, but with a factor three increase for the large area devices, no circuit designer can take the blame for any malfunctioning circuit.

The second very intriguing signal of figure 4.22b is that although the large area fluctuation component is about a factor of three too high, the fluctuation enhancement for the narrow/long population is even more pronounced, while it is reduced for the wide/short population.

Discussion

After making sure the measurements are correct, the second reaction when such disastrous device mismatch fluctuation performances are encountered is to take a more detailed look at the standard I-V characteristics of the MOSFET's. In this case (figure 4.23), the linear region I_D-V_{GS} characteristic showed an uncommon kink in the strong inversion region (around V_{GS}=-1.6V). This kink is hardly visible in the I-V graph (figure 4.23a), but its g_m plot (first derivative; figure 4.23b), clearly shows a change of device behaviour.

The shape of the g_m characteristic is important in our V_T extraction approach, as the 3-point technique requires that the three measurements must be collected in the region between the peak-transconductance point and the V_{dd}. So, as part of the standard procedure in the measurement program, the linear region graph and its derivative are measured on a few transistors to help decide where to place the measurement points.

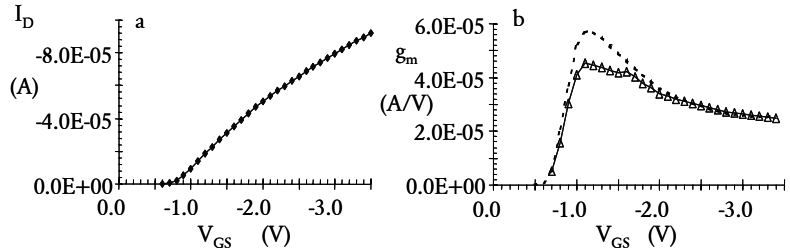

Figure 4.23 Linear region transfer and g_m graphs of W/L=10/1 P-channel MOSFET suffering from severe gate depletion. Dashed line in figure b. represents an indication of the normal g_m curve.

The shape of a g_m curve like in figure 4.23b can be explained by the occurrence of poly-Silicon gate depletion. The (second) peak in the g_m curve (in this case around V_{GS}=-1.6 V) has been observed before, and is attributed to gate inversion. Gate depletion in P-channel MOSFET's is one of the technological challenges for transistors with very thin gate dielectrics. In order to prevent that boron atoms from the p-type gate electrode diffuse through the gate dielectric (boron penetration), the temperature budget of the Source/Drain/Gate doping drive-in and activation anneals must be minimised. This also requires a restrained approach towards doping of the gate layer. The resulting, relatively low and/or not fully activated, doping levels of the gate layer may result in less effective gate-drive due to the formation of an appreciable depletion layer in the gate electrode as the transistor is driven deeper into strong inversion.

The occurrence of gate depletion is a concern for all advanced poly-Silicon gate CMOS processes as gate depletion effectively enlarges the gate dielectric thickness. A thicker gate oxide gives a lower gate capacitance and hence a lower drive current (I_{on}) of the transistors. Gate depletion as a macroscopic effect, should be expected to contribute to an increase of the dopant fluctuation component of the threshold voltage mismatch fluctuation area scaling factor $A_{\Delta VT}$. As the dopant fluctuation attributed $A_{\Delta VT}$ scales linearly with T_{ox}, an increase of the effective

dielectric thickness due to the additional depletion layer, results in a slight degradation of the matching. But as the gate depletion degraded EOT is limited to within 10% of the targeted dielectric thickness, this can not be an explanation for the three times higher than expected A-factor.

As it was suspected that the humps in the g_m-characteristics had a relation with the encountered matching problem, the occurrence of these humps was investigated in more detail. Wafers from other P-MOS uni-channel lots (from the 0.18 μm process development generation with 4.5 & 6 nm gate oxide) were analysed with focus on these humps. The following observations were made:

- at first sight, most geometries show such humps but:
- whereas the 10/10, the 10/1 and the 0.4/1 devices all showed more or less comparable behaviour, the 0.4/10 transistors had significantly stronger g_m humps. In two of the chips at the edge of the wafer, the threshold voltage appeared to be shifted by as much as 600 mV, while, as the transistor switched on, the current increased very steeply with increasing V_{GS}.
- for the shorter devices (10/0.3), the effect was considerably less, and when even shorter transistors were probed, the double g_m hump effect was practically gone.
- according to TEM pictures, the used poly-silicon layer process module yielded layers with grain sizes of the order of 0.2 to 0.5 μm.

Subsequently another set of wafers was evaluated from another lot (T_{ox} = 6 nm) that were subjected to several different Rapid Thermal Anneal conditions. A clear difference was observed in terms of occurrence of the g_m-humps. Moreover, subsequent mismatch fluctuation measurements indicated a very strong correlation between the g_m-humps and the threshold voltage mismatch fluctuation standard deviations of the 10/1 transistors (table 4.9).

Wafer	RTA condition	g_m-humps	$\sigma_{\Delta VT}$ (W/L=10/1)
14	30"@950 °C	very severe	19 mV
16	20"@1000 °C	noticeable	6.9 mV
18	50"@1000 °C	negligible	3.3 mV

Table 4.9 V_T mismatch fluctuation standard deviations from selected wafers from process development batches with different activation anneals.

To explain the correlation between the (macroscopic) g_m humps and enhanced threshold voltage mismatch fluctuations, the following key question had to be answered: What could be the microscopic device architecture fluctuation cause that could be held responsible for the mismatch fluctuation enhancement?

Based on the observations discussed above, it was postulated that the strongly enhanced mismatch fluctuations are caused by poly-silicon grains that are not doped homogeneously, and sufficiently high to avoid (local) gate depletion. Accordingly, we are dealing with a microscopically varying version of the gate depletion phenomenon. This interpretation is depicted in figure 4.24.

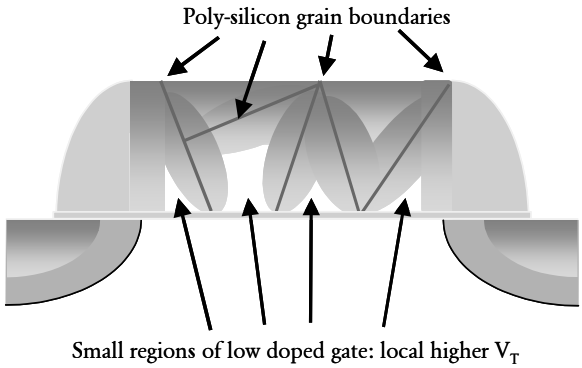

Figure 4.24 Microscopic interpretation of enhanced mismatch fluctuations. Inhomogeneous doping of poly-Si grains causes local threshold voltage fluctuations. The larger poly-silicon grains are weakly n-type in the centre, as the (intended p-type) layer was lightly n-type pre-doped.

The impact of the RTA temperature budget on the threshold voltage mismatch fluctuations (table 4.9) can hence be interpreted as an indication that the size of these low-doped regions varies. The doping process of the poly-silicon gates is depicted in more detail in figure 4.25.

The poly-Si layer is deposited as an amorphous silicon layer (0.15 to 0.2 μm thick). As soon as a temperature step is applied (e.g. n-type dopant activation prior to gate etching, or thermal re-oxidation of the formed gate prior to spacer deposition), the amorphous silicon layer crystallizes. The formed grain boundaries serve as (fast) diffusion paths for the (HDD)

Source/Drain and gate dopant. This means that during the initial part of the dopant activation anneal, the dopants diffuse quickly along the grain boundaries, after which they will gradually fill-up the grains, depending on the temperature budget and the diffusion mechanism into the poly-Si grains. This model/mechanism was discussed with silicon diffusion experts and verified through process simulations.

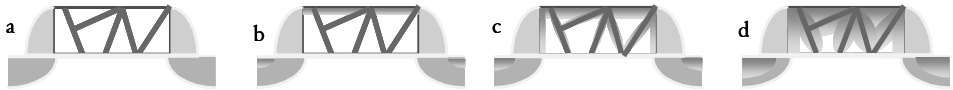

Figure 4.25 Poly-Si gate layer doping process. a: Lightly doped n-type gate with grain boundaries after LDD implant and spacer formation. b: After boron S&D HDD/gate doping implant. c: Fast diffusion of boron dopants along grain boundaries. d: diffusion of boron into the poly-silicon grains. Depending on the RTA temperature budget and the grain sizes, p-type doping levels and/or size of low-doped regions fluctuates.

The elegance of this model proposal is that the (fluctuating) size of the poly-silicon grains is held responsible for the parametric fluctuation mechanism helps to explain the strange area scaling behaviour of the threshold voltage mismatch fluctuation (figure 4.22b). According to one of the four assumptions (section 1.2 of this thesis), the size of the disturbance should be small compared to the device dimensions. With grain sizes of a few tenths of a micron and ditto device dimensions this prerequisite is not met.

In the first place, this explains why short transistors are less affected by these gate depletion induced fluctuations compared to large area devices. As the edges of the Gate along the Source and Drain side -by definition- form grain boundaries, a more homogeneous doping of the Gate is already achieved at a lower thermal budget, because the dopant can penetrate the grains from the sides. Moreover, no diffusion path can be longer than half the transistor length.
This assessment is confirmed by the observation that the g_m-humps were significantly less pronounced for the 0.3 μm transistors and even vanished completely for even shorter transistors.
The observed fluctuation enhancement for the narrow/long pairs in figure 4.22b can also be explained with the proposed local gate-depletion model. If one assumes that poly-Si grains are of the order of the transistor width, it is quite well imaginable that one of the larger grains partially, or even completely, blocks the transistor with a channel region with a significantly higher threshold voltage. This type of blocking would result in a relatively strong impact on the threshold voltage. This ties in with the strong -up to 600 mV- increase of the threshold voltages

observed for some devices. Such large variations result in relatively large mismatch fluctuation standard deviations for populations of narrow device pairs. It should be noted that the poly-Si gate usually overlaps the field-oxide (that determine the channel width) significantly.
In particular, in (Common Gate) matched pair MOSFET test structures where the transistors are placed close together, the Gates generally consist of one single slab of poly-Si (figure 4.26). This implies that there are no near-by grain boundaries as in the short-channel case.
This blocking theory is again supported by the g_m-humps observations, that were indeed more severe for the narrowest transistors with a few devices even practically blocked until the Gate reaches the inversion state.

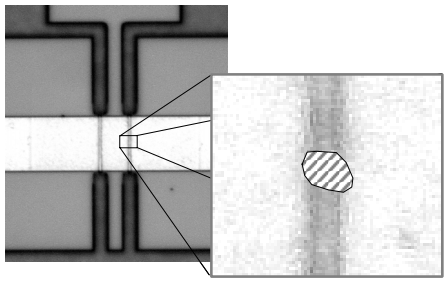

Figure 4.26 Close-up of W/L=0.4/10 matched pair (left). Right: detail of channel region of one transistor with proposed model of a single grain blocking the channel region. Note that this is merely a representation of the idea. Poly-silicon grains are not visible with this microscope.

The investigations as described so far, were followed by a number of dedicated uni-channel lots to verify the hypothesis that the amount diffusion of the dopants inside the poly silicon grains did indeed have an effect on the mismatch fluctuations. In a (P-channel) lot, the dopant activation anneal was varied from 20 s @ 970 °C to 1070 °C (figure 4.27). The gate depletion impact on the threshold voltage fluctuations (as well as g_m-humps) was confirmed almost to good to be true [Tuin97b]. The excessive mismatch fluctuation for the narrow/long devices disappeared when the activation anneal was sufficient to dope the grains completely. The same experiment also showed that when the temperature budget is too large, the competing mechanism of boron penetration could be observed (figure 4.27). This was (as expected) accompanied with an increase in the threshold voltage mismatch fluctuation. The increase of mismatch fluctuations in the boron penetration regime indicates that also this mechanism has

a random component, probably also due to the grain boundaries that start serving as the prime source for the boron penetration. A comparable experiment, involving n-channel MOSFET's also confirmed the gate-depletion signature for n-channel transistors [Tuin97b].

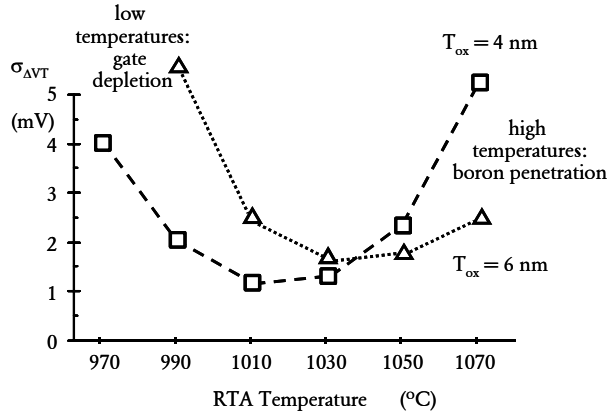

Figure 4.27 Effect of RTA temperature on threshold voltage mismatch fluctuation standard deviation of W/L=10/10 PMOST pairs: confirmation of the poly-Si grain doping theory. Squares: T_{ox}=4 nm, Triangles: T_{ox}=6 nm.

The understanding that the poly-silicon gate morphology and the Gate and Source/Drain dopant activation temperature budget can contribute significantly to the matching performance of MOSFET's is one of the most important outcomes of this thesis' study. This insight initiated experiments towards fabricating CMOS devices with the gate layer deposited at slightly higher temperatures, rendering so-called fine-grained poly. Fine-grained poly is a CVD layer that is deposited at a somewhat higher temperature (around 605 °C, as opposed to 570 °C for an amorphous layer) in a vertical, single-wafer reactor. Due to the easier nucleation and the higher mobility of the silicon atoms, the layer grows preferentially in a columnar structure with crystals that are significantly smaller (order 100 nm [Schm99]). An amorphous layer on the other hand, crystallizes uncontrolled during the first successive high temperature step. This approach now has turned into a standard technique for modern deep-submicron CMOS technologies as an inevitable requirement for keeping the stochastic parametric fluctuations under control, both for analogue applications as well as for yield control of large embedded SRAM's in SOC's [Stolk01, Tuinh02b, Difr05].

A double-poly emitter BJT mismatch riddle

The final example in this chapter also belongs to the category of matching studies where an unexpected mismatch fluctuation area scaling observation led to identification of a fundamental process architecture weakness. In this case, the devices belonged to a family of double-poly NPN bipolar junction transistors for discrete broadband NPN transistor crystals and small MMIC's for mobile telecom transceiver modules. Mismatch fluctuation measurements on a (discrete) bipolar-only version of this process architecture initiated the study discussed in this section.

The relevance of this particular case for this thesis is not given by the occurrence of an excessive mismatch fluctuation observation nor to document the struggle to unravel the riddle behind it. However, the fact that several of the test structure and measurement concepts discussed in the previous chapters were applied or even developed during the course of this particular study, justifies to place this case in this chapter as an illustration of their relevance. A most welcome surprise of this case proved moreover, that once the mechanism was understood and the process step that was responsible for the effect replaced by a more robust one, the product yield went up! Apparently, the fluctuation mechanism that was responsible for the excessive mismatch observations aggravated so severely in some of the devices that it affected the overall product yield. Therefore, this case forms another good example of how matching studies can help to gain better understanding of the microscopic device architecture, and can hence be used to improve processes.

Test Structure

The matched pair test structures for this case are divided into three types (figure 4.28):

- Elementary mismatch assessment module. Initially, one 2x9 pad PEM module was reserved for assessment of the matching performance of the double-poly NPN transistors. The CE&CC type of module (figure 4.28 upper left) included 7 pairs with emitter dimensions W_{drawn} x L_{drawn} (in microns): 0.8x2, 0.8x20. 1.6x5, 10x10, 4 fingers 0.8x80 (realistic power), spaced 0.8x20 (about 200 μm spaced to assess distance effects), and a quad 0.8x20.
  The minimum design rule for the process was 0.8 μm. By using an inside L-spacer (double poly emitter NPN) architecture, the effective emitter dimensions of the transistors were approximately 0.4 μm smaller than the drawn dimensions. The emphasize of the chosen geometries for the mismatch characterisation module was very much on investigating reasonable options for the devices based on the minimum emitter width. The application focussed on low base resistance (minimum W), relatively large power (large area, multi-

emitter finger layout style) NPN transceiver transistors.

- Extended group. Based on the initial measurements, it was concluded that the set of device geometries listed above were inadequate for unravelling the encountered matching problem. Fortunately, an MPW mask set was about to be launched, which enabled us to create a more extensive geometry range. For this set of devices, we chose for the scribe-lane type of CE&CC pairs shown in figure 4.28 lower left. The following set of WxL emitter dimension matched pairs were designed: 0.8x2.0, 0.8x4.0, 0.8x10.0, 1.0x4.0, 1.2x2.0, 1.2x4.0, 1.2x10.0, 2.0x2.0, 2.0x4.0, 4.0x4.0, 10.0x10.0, and 20.0x20.0.

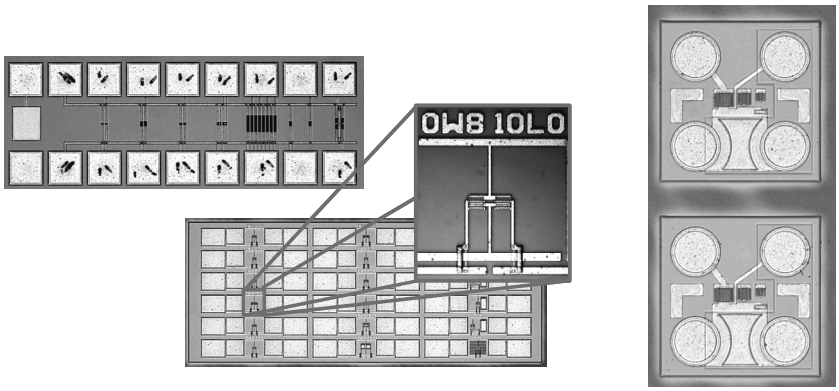

Figure 4.28 Three types for BJT matched pairs. Upper left: elementary 7 pairs CE&CC 2xN pad module. Lower left: collection of CE&CC scribe line modules (with detail). Right: Two product dice also form a matched pair.

- Product dice. A new approach towards mismatch fluctuation characterization was born out of need during this project. When searching for clues as to what could have caused the unexpected effect, some standard product wafers were used for mismatch characterisation. Transistor emitter area of this product was designed as 0.4x82 μm^2 (four fingers of 0.8x21). However, as there were no matched pairs in the process control module of these wafers, we decided to use adjacent product chips (transistors) for the mismatch fluctuation study (figure 4.28 right). With a crystal pitch of no more that 335 μm, the actual product chips were close enough that the impact of parametric gradients was negligible compared to the mismatch fluctuations.

Measurement method

The collector and base currents mismatch fluctuation measurements for these double poly-NPN BJT's are quite straightforward, be it that the largest devices should be expected to have good matching performance (of the order of 0.1%). The mismatch fluctuation standard deviations were derived for $\Delta I_C/I_C$, $\Delta I_B/I_B$ and $\Delta h_{FE}/h_{FE}$ using a single V_{BE} bias point. The bias point was chosen in the ideal part of the h_{FE} plot. In general terms, this means a collector current well above the point where the non-ideal low base current drop-off of the h_{FE} starts and below the (quasi) saturation dominated high current h_{FE} drop-off region. The first set of measurements was executed using variable V_{BE}'s, depending on the emitter area, such that all transistor geometries were biased at about 5 μA. Such a low current has as advantage that probe to pad contact resistance fluctuations are negligible. The disadvantage of this approach is however, that the transistors are not characterised at the same current density and not necessarily in the same mode of operation in terms of addressing the same microscopic disturbances. The edge of the Emitter-Base depletion layer is not exactly at the same depth. This may be relevant as this particular type of transistors with a thin Base and relatively high pinched-base resistance suffered quite severely from the reverse Early effect on the h_{FE}. Moreover, for the largest device pair of the first set of test structures (4 emitter fingers of 0.8x80), the non-ideal base current component proved so high that these pairs had to be measured at a collector current of about 50 μA (V_{EB}=-0.70 V) to stay out of the non-ideal base current region.To avoid possible inconsistencies for the interpretation, later measurements (type ii and type iii test structures) were all done at a fixed V_{EB} of -0.74 V, which meant that the collector currents ranged from about 1.8 μA for the 0.8x2 devices to well over 700 μA for the 20x20 transistors. Because the second set of transistor pairs were carefully laid out with emitter star connections, and by using the CE&CC configuration, the impact of contact pad resistance fluctuation on the mismatch measurements is negligible. What remains though, are the effects of the contact resistance fluctuations on the base contact pads. However, as the largest transistors operated with a base current of about 10 μA, a 1 Ω fluctuation results in an internal V_{BE} uncertainty of the order of 10 μV, which is still significantly smaller than the observed device mismatch fluctuations for the largest devices (0.1% $\Delta I_C/I_C$, corresponding to about 26 μV V_{BE} mismatch fluctuation). Furthermore, it was shown that if the transistors are biased in the ideal part of the Gummel-plot, the mismatch standard deviations for most BJT populations are practically independent of the current level over several decades ([Tuinh02b].

All measurements were done with a fixed V_{CB} of 1 V and the substrate at -1 V. Statistical estimators were calculated using safe estimation. The number of defect pairs that were discarded by the range-screening algorithm varied quite considerably. In the first lots, while the technology was still in a typical research phase, the number of discarded positions was (embarrassingly) high: up to 30 out of 85 probed positions. In this case, it clearly proved an unfortunate choice that all 7 pairs in the module shared the emitter and collector connection as one shorted transistor makes the entire module useless. The actual I-V measurement algorithm was based on a (double) M5S3 algorithm, with die by die monitoring of the Base-voltage common offset and with repeatability measurement as described in chapter 3 (figure 3.20) and in more depth in [Tuin98]. The "DUT 1-2-1-2" (section 3.3 of this thesis) short-term repeatability is typically 0.01 to 0.02%, hence more than adequate for all mismatch standard deviation results encountered in this example.

Results and Signals

The mismatch fluctuation standard deviations of a golden wafer for the first type of matched pairs are listed in table 4.10 below and are depicted graphically in figure 4.29.

W_{drawn} (μm)	L_{drawn} (μm)	$\sigma_{\Delta IC/IC}$ (%)	$\sigma_{\Delta IB/IB}$ (%)	$\sigma_{\Delta hFE/hFE}$ (%)	remarks
0.8	320	0.7	2.3	1.7	4 fingers 80 μm long
10	10	0.4	0.9	0.8	-
0.8	40	1.8	6.4	4.8	quad 2 x 20 μm
0.8	20	2.5	8.3	6.2	-
0.8	20	2.4	8.2	6.1	spaced pair
1.6	5.0	1.1	1.4	1.7	-
0.8	2.0	7.3	29.5	20.7	-

Table 4.10 Initial BJT mismatch fluctuation estimators of the first type of test module.

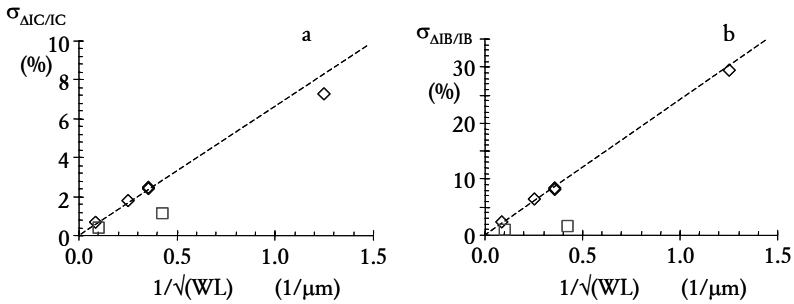

Figure 4.29 Collector current (a) and Base current (b) mismatch fluctuations standard deviation area scaling graphs for 7 double poly NPN BJT's. Diamonds: W_{drawn}=0.8 μm; Squares: W_{drawn}>0.8 μm. Effective dimensions are assumed 0.4 μm smaller than drawn. Dashed lines represent $A_{\Delta Ic/Ic}$=7 %μm and $A_{\Delta Ib/Ib}$=24 %μm resp.

Table 4.10 and figure 4.29 reveal several remarkable features (signals):

- In the first place there is the observation that the mismatch fluctuation standard deviations are much smaller for the devices with a drawn width larger than 0.8 μm compared to those determined from the W_{drawn}=0.8 μm transistors.
- When compared to benchmarks [Tuin98, Tuinh02b, Lau03, Choi05], the estimated A-factors give rise to mixed feelings. The W=1.5 and 10 μm devices would yield fairly decent matching numbers of the order of 3 %μm and 6 %μm for the collector current and base current matching respectively. For the W=0.8 μm pairs, rather horrifying 7 %μm and 24 %μm are obtained for collector current and base current mismatch fluctuations respectively.
- The fact that all the W=0.8 μm pairs all fall reasonably well on a straight line, both for the collector current as well as the base current mismatch standard deviations, indicates that microscopic random fluctuation mechanisms must be involved. However, there must be a fluctuation mechanism for the W=0.8 μm devices that is not active in the wider transistors. Note also that the (1/√(L)) relationship in figure 4.29 does not only hold for the standard layout length scaling (L=2 and L=20), but also for the quad and the fingered layout, while an additional distance has no significant impact.

- The final, and in this case relevant, peculiarity as observed in table 4.10 concerns the h_{FE} mismatch fluctuation numbers. As $h_{FE}=I_C/I_B$, one would expect that the variance of the h_{FE}-mismatch would be equal to the sum on the variances of $\Delta I_C/I_C$ and $\Delta I_B/I_B$ (assuming they are independent). In practice, this means that the h_{FE} mismatch standard deviation is larger than either the base current or the collector current mismatch standard deviations, as for instance is seen for the 1.6x5 pairs. Table 4.10 demonstrates that this is not always the case, specifically for W=0.8 μm pairs.

Independence of collector and base current mismatch is normally expected, as the collector current mismatch is usually attributed to fluctuations of the base Gummel number, whereas the base current mismatch is supposed to be determined by fluctuations of the emitter Gummel number. These two Gummel numbers are independent as they represent completely independent processing steps and microscopic construction elements (dopants, poly-mono surface recombination, interface states). However, when the emitter area fluctuates, one would expect a significant correlation between the two mismatches as both collector current and base current are proportional to the emitter area. In fact, this notion can therefore be used as a possible technique to identify emitter area fluctuations as discussed by Drennan et al. [Drenn00]. Emitter area fluctuations and perimeter roughness used to be considered the main mismatch causes for old bipolar IC technologies [e.g. Gray&Meyer]. In modern process lines with much better reduction stepper photo masks and better controlled litho and etching however, microscopic dimensional fluctuations are much smaller that they apparently used to be. During this thesis work, it was seldom encountered that area fluctuations contributed significantly to the observed parametric mismatch fluctuations. The only exceptions were some over-stretched research experiments that tried to realise the next generation process shrink using existing (outdated) equipment and resist technology. Such occurrences were never really pursued in this project, as it is likely that such effects disappear as the processes grow in maturity. Therefore, the example as discussed in this section looked tempting, as this could have been an example of an area fluctuation effect that plays a role in so many matching horror stories. However, this should be seen in the light that the particular device size (0.8 μm) of this experiment was not overly challenging for lithography at the time these devices were made (CMOS process generations were already way below 0.5 μm). The inside spacer approach results in effective emitter dimensions (0.4 μm) that were below the specifications of the litho process itself, but the 0.8x2 to 0.8x20 type of holes that were required for these transistors could not be deemed as being too difficult to manufacture.

Nevertheless, the correlations between collector and base current mismatch fluctuations were clearly there, as evidenced by the relatively low $\Delta h_{FE}/h_{FE}$ standard deviations. Representative examples of correlations between the collector current and base current mismatches are depicted in figure 4.30. Whereas in figure 4.30a, the correlation for the 0.8x20 pair is obvious (with a correlation coefficient of the order of 0.78), graph b for the 1.6x5 pair clearly lacks such correlation. The other 0.8 μm wide matched pairs yielded similar correlations as shown in 4.30a, while the 10x10 device pair behaved similar to figure 4.30b.

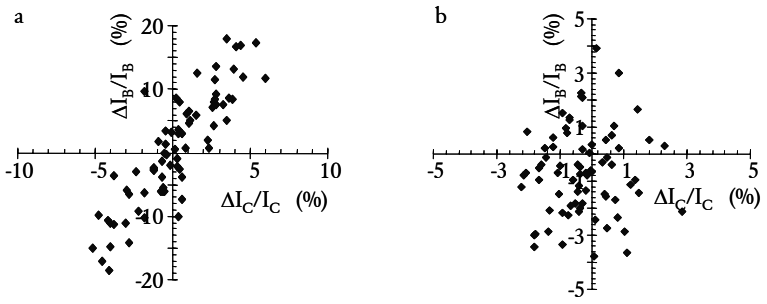

Figure 4.30 Correlations between collector and base current mismatch for WxL=0.8x20 pairs (a) and 1.6x5 pairs (b).

However, the lack of correlation for the 1.6x5 pairs places severe doubts on the assumption that dimensional variations are the main cause of the large mismatch fluctuation standard deviations encountered in this example. It is rather unlikely that a 1.6x5 would totally lack any perimeter roughness or area fluctuation that is so dominant in the mismatch fluctuations of the 0.8x20 pairs. The average effective areas are not very different between a 0.8x20 and a 1.6x5 device (7.8 vs. 5.5 μm^2), while a 10x10 transistor practically has the same Emitter-Base diffusion perimeter as the 0.8x20 device.
When emitter area or perimeter fluctuations are not the reason for the correlated base and collector current mismatch observations, another explanation must be found. Based on experience from earlier poly-emitter studies (for instance reported in [Tuinh02b]), it was suspected that the construction of the poly-mono (magic) interface layer had some relation with the correlated mismatch behaviour. One can for instance imagine that small oxide islands remain at the interface, serving as recombination centres in the Emitter (hence locally increasing the base current). Then one would have to assume that these islands subsequently

enhance the diffusion (locally) of the emitter dopants into the Base, in order to explain that the collector current also increases locally. Another explanation that was brainstormed was related to grain boundaries that are formed in the emitter poly-layer. It has been proposed by Tamaki et al. that enhanced diffusion of the Emitter into the Base is stimulated by emitter poly-Si grain boundaries [Tama91]. This could indeed give rise to an increased collector current.
And if one can believe that such poly-Si grain boundaries could also serve as enhanced recombination centres for the holes that are injected into the Emitter, that would result in an increased base current and hence a correlation. A problem with these explanations is that it becomes even harder to envisage why these mechanisms would only occur for narrow emitter devices. One would for instance have to believe that the cleaning step, prior to poly-CVD for the emitter-poly deposition would be difficult for relatively narrow emitter holes. Furthermore, the assumption that fast diffusion poly grain boundaries would occur preferentially in 0.8 μm Emitters requires a substantial amount of wishful thinking.

Status quo and dilemma
This was the point that was reached in this project by analysing just one typical (golden) wafer of a particular research lot. Several interesting mismatch observations were encountered, but the mechanism was not understood. This forms interesting food for device physicists, but there is clearly not enough evidence to solve the riddle. It seemed there was an emitter width-related effect, but this could not really be studied in detail due to the small number of matched pair device geometries that were available in the test module. Moreover, although the mismatch performance was in fact rather poor for this type of process architecture, the process owner did not really care too much. The numbers showed that the collector current matching could easily be better than 1% for long multi-finger emitter applications, and that was considered good enough as a first shot for MMIC tests. Therefore, these results were put aside for a while in the file for the unsolved riddles. In the field of parametric mismatch characterisation, one is regularly faced with such dilemmas. Is it worthwhile to take action on any suspicious effect that is encountered? It could very well be that this is a once only riddle, occurring only in this particular lot. The investigation regained momentum when wafers from other lots with the same test structures found their way to the mismatch measurement station. These wafers showed the same (if anything even worse) behaviour: poor matching performance for the 0.8 μm pairs with a clear correlation between collector current mismatch and base current mismatch that could not be observed for the wider emitter pairs. Hence, this observation could no longer be put aside as a once only effect.

More results

A first step towards gaining more insight was made by assuring the availability of a better collection of test structures. Fortunately, an MPW opportunity became available, so we could quickly design and realise the second type of test structures on a mask set (figure 4.28). The mask set was processed and, as depicted in figure 4.31, the phenomenon recurred. Clearly the narrowest transistors show a severe collector current mismatch fluctuation degradation, in this case even reaching a shocking 20 %μm, while (not very well visible in this figure at this scale) the area scaling factor for the larger than 1.2 μm transistors rested at a quite acceptable 2-3 %μm. Interesting enough, the W=1.0 μm seemed to behave as an intermediate, showing significantly larger fluctuations, be it at a more acceptable 4-5 %μm level.

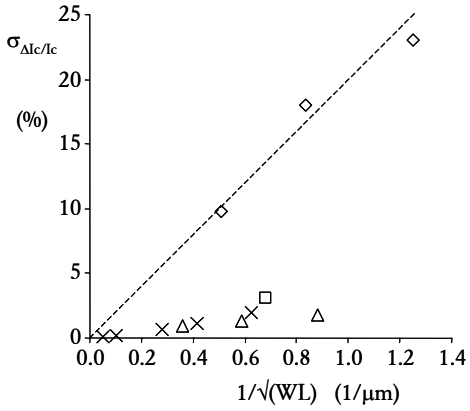

Figure 4.31 Collector current mismatch fluctuation standard deviation area scaling graph for second type of test structure set. W_{drawn}=0.8 μm (diamonds), 1.0 μm. (squares), 1.2 μm (triangles), and > 1.2 μm (X's). Dashed line represents $A_{\Delta IC/IC}$=20 %μm

In addition, the correlations re-appeared, both evidenced by the current gain mismatch and through scatter plots. A second and third wafer from the same lot showed the same results, so this left little room for excuses and statistical hideaways: This must be understood!

Table 4.11 summarises the collector current mismatch standard deviations for a few relevant geometries for three wafers (wafer 9 was used for figure 4.31). Wafer 15 came from a second part of the lot that was processed through the back-end of the process flow independently. One may be tempted to think that significant differences between these wafers are discernible in the table, but statistically these differences were tested to be insignificant.

Emitter dimension (μmxμm)	$\sigma_{\Delta IC/IC}$ wafer 9 (%)	$\sigma_{\Delta IC/IC}$ wafer 6 (%)	$\sigma_{\Delta IC/IC}$ wafer 15 (%)
4x4	0.7	0.6	0.5
2x4	1.1	0.8	0.8
1.2x4	1.3	1.1	1.2
1.2x2	1.8	1.8	1.6
1x4	3.1	3.4	3.3
0.8x4	17.8	14.5	15.8
0.8x10	9.8	9.6	9.3

Table 4.11 Collector current mismatch observations from MPW lot.

H_2/N_2 anneal experiments

An experiment that was employed to investigate the -not understood- mismatch mechanism consisted of subjecting the wafer to additional H_2/N_2 anneals. This choice was based on the results that were obtained before concerning the mismatch improvements of MOSFET's, as described in the 'metal-coverage case' in section 4.3. Although metal coverage was not the problem for these double-poly transistors, the assumption was that applying additional hydrogen anneals would prove beneficial for their mismatch fluctuation performance.
This idea was based on the suggested fluctuation mechanisms. These were both based on contributions of interface states at the poly-mono interface or at emitter poly-Si grain boundaries. Hydrogen anneals are generally considered to be beneficial against detrimental contributions of such interface states.

Large was the surprise therefore when the mismatch fluctuations on wafer 6 were indeed re-measured after the wafer was subjected to an N_2/H_2 anneal for 60 minutes. The results before and after anneal are listed in table 4.12. This was totally against anything that was expected! Instead of an improvement for the narrow emitter devices, a statistically significant -though not shocking- mismatch fluctuation degradation for the 0.8 μm wide emitter pairs is observed. What was more surprising however, was that the wide emitter pairs suffered a devastating mismatch fluctuation degeneration due to this anneal. These anneal results practically ruled out that the mechanism that was looked for, had something to do with the front-end device architecture (dopants, junction depths, dielectrics), as these are not likely to be affected at a temperature of 450 °C. Nevertheless, at this point the mismatch mechanism was still not understood.

Emitter dimension (μmxμm)	$\sigma_{\Delta IC/IC}$ wafer 6 (before) (%)	$\sigma_{\Delta IC/IC}$ wafer 6 after +60'@450 °C (%)	$\sigma_{\Delta IC/IC}$ wafer 15 (before) (%)	$\sigma_{\Delta IC/IC}$ wafer 15 after +60'@420 °C (%)
4x4	0.6	2.2	0.5	0.5
2x4	0.8	2.6	0.8	1.0
1.2x2	1.8	4.0	1.2	1.2
1x4	3.4	14.9	3.3	4.7
0.8x4	14.5	16.3	15.8	22
0.8x10	9.6	11.2	9.3	13.4

Table 4.12 Change of collector current mismatch fluctuation standard deviations for wafer 6 after additional hydrogen anneals.

The good news of an experimental outcome as shown above, is of-course that apparently the right knobs were turned, be it in the wrong direction. Therefore, it was decided to give it another spin. Another wafer was characterised with respect to mismatch fluctuations before and after anneal. In this case a lower 420 °C, 60 minutes N_2/H_2 (80%/20%) anneal was used. The results, appended in table 4.12, again show a signal, although not exactly the same as the previous experiment. Although the 0.8 μm wide emitter pairs' mismatch fluctuations still degrade significantly, the wider Emitters are not affected anymore! In retrospect, it can be concluded that this was the correct experiment, but at the time the results of table 4.12 were first evaluated, the confusion only became larger. Apparently, the 450 °C anneal was more detrimental than the lower temperature one. However, it looked as if the effect on the wide

emitter devices disappeared! As it was assumed at that time that the mismatch mechanism was associated with interface states or recombination centres, the changing signal came as a surprise. In fact, it was not realised that the temperature budget of the back-end process did indeed have something to do with the observed mismatch mechanism. How such a low temperature step could affect something as fundamentally entrenched in the device architecture, as collector and base current mismatch fluctuations remained a riddle.

From this point onwards, the search continued using product wafers with the product matched pair test structures (figure 4.28). This allowed evaluation of the mismatch performance as a function of many more process experiments that had already been performed by the process engineer, such as epi-layer thickness, over-etching of the emitter hole, inside spacer formation, and the doping of the emitter-poly. Although there was only one device geometry available on each product wafer, the analysis proved simple. It was only necessary to look for the occurrence of I_c and I_b mismatch correlation. Unfortunately, no additional clues were found. The only additional clue was that the correlation did not occur on wafers that only received a single-metal back-end.

Solution
The explanation was finally found in discussions with the product engineer. One of the production wafers had been subjected to extensive chemical analyses and one of the outcomes was that an unexpected high concentration of Aluminium was found in the Emitters of transistors. Moreover, a reliability risk was reported, associated with holes that were seen (once or twice) on SEM cross-section pictures. The accumulated insight that the observed effect had a relation with the backend (double metal is bad, and additional anneals are bad) was brought up in discussions with a back-end metallisation expert. And indeed, it was then that a sensible explanation was found that fits all observations. The assumption was made that the problem was due to the contacts on the Emitter. The Emitter's n^+ poly-silicon is contacted with a titanium / titanium-tungsten / aluminium stack. The Ti-TiW layer serves as diffusion barrier between aluminium and silicon, to avoid that the aluminium reacts with the poly and the underlying mono-silicon (alloying), causing shorts (spiking). However, titanium and tungsten belong to the category of so-called sacrificial barriers. During anneals at temperatures in the range of 400 to 500 °C titanium reacts with aluminium to $TiAl_3$ and tungsten to WAl_{12} [Wolf, Silicon Processing for the VLSI Era, Volume 2 - Process Integration, pp. 124-126]. Now all one has to assume (and this is not unlikely) is, that the step-coverage of the TiW layer is poor in the (narrow) holes that remain after the emitter poly CVD deposition (after CVD, the physical

opening is not more than 0.4 μm). When the sacrificial diffusion barrier is too thin, the layer is consumed during subsequent temperature steps. When the diffusion barrier layer is gone, the silicon of the emitter poly-silicon diffuses into the aluminium. The hole that is formed in the silicon layer is immediately filled with aluminium. This mechanism, well known from the junction-spiking phenomenon in shallow n-p junctions also depends on the crystal orientation of the silicon that reacts with the aluminium. The combination of the poor TiW step-coverage in narrow emitter holes and the (fluctuating) crystal orientation in the poly grains explains why this alloying problem appears as a random mismatch fluctuation mechanism. The fact that the weakness of the diffusion barrier is more severe when the wafers are subjected to an additional anneal is explained by the consumption of the sacrificial barrier. Indeed, wafer 6 that was exposed to a 450 °C anneal was more degraded than the wafer 15 that was subjected to a 420 °C anneal. If the thermal budget is high enough, even the largest transistors with the thickest TiW layer can get affected. The thin diffusion barrier assumption also explains why the problem only occurred on wafers that received the full double metal processing, as the total temperature budget is lower for a single metal back-end.

A confirmation of this explanation was obtained by de-processing wafer 9 (not subjected to an additional anneal), back to the emitter-poly level. Figure 4.32 shows typical examples of what matched pairs of two different emitter sizes look like after de-processing. After removing the inter-metal dielectric stack and all the metal layers (including the Ti and TiW layers), the two poly islands (p+ base poly and n+ emitter poly) remain. The imprints of the contacts on the base poly and the collectors are also clearly recognisable. In the narrow emitter transistor pair, the holes in the emitter poly are clearly visible. Some of these holes are located on the vertical edges of the emitter poly, where they are probably harmless for the transistor operation. Other holes in the 0.8x10 Emitters reach the bottom of the Emitter where the poly-Si layer contacts the mono-silicon part of the Emitter. Due to the different orientation of the mono silicon, the aluminium does not necessarily spike all the way into the mono silicon and cause an Emitter-Base short. When the aluminium of the emitter contact eats through the poly-Si, the emitter contact comes locally so close to the e-b junction that an enhanced base current results (transparent Emitter).

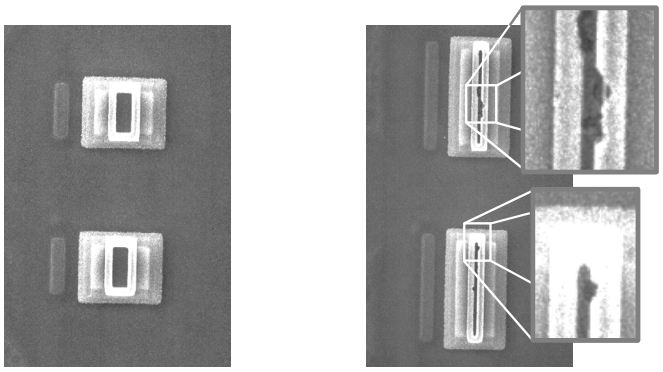

Figure 4.32 SEM photographs of de-processed double poly-Si emitter NPN matched pairs. Metals and dielectrics removed. First (Base) and second (Emitter) poly layers visible as white rectangles. WxL=2x4 (left) and 0.8x10 (right). Alloy pits are clearly visible in the narrow Emitters (insets) while such pits are absent in the wider Emitters (left).

Conclusion

When the technological cause was finally identified, a so-called stuffed TiW diffusion barrier that is sputtered in an N2/Ar ambient replaced the diffusion barrier layer. The nitrogen that is built into the TiW layer enhances the barrier properties (it dissolves slower), at the expense of a minor contact resistance increase. With this more robust barrier layer, the mysterious mismatch enhancement effect was gone. In all fairness, it must be acknowledged that the improved mismatch fluctuation performance was not the dominant reason to switch over to this other layer. The process was intended for a product line for discrete transistors with emitter area's of the order of a few hundred square microns of emitter area. Even a horrifying 20 %μm collector current mismatch A-factor contributes less than 1.5% to the parametric spread of a single 100 μm^2 emitter area transistor, which is not really something that will keep a product engineer of a discrete components fab awake at night. However, as it turned out, the stuffed TiW diffusion barrier helped to improve the yield of the product crystals significantly. Whereas the number of discarded dice due to too low Emitter-Base breakdown (or too high leakage), hovered around a rather uncontrollable 15% prior to changing the barrier layer recipe, this number dropped below 1% after the change! Any sensible product engineer would have been scared anyway, to see the kind of pits in the emitter poly as depicted in figure 4.32. It does not require much imagination to realise that if so many holes are present in the poly, not much is needed to create a junction failure here and there. A large number of failures was in fact already evident in the original matching measurements (the embarrassing failing 10 to 35 out of 85 pairs mentioned in the measurements section of this case), be it that the safe statistical analysis filtered-out most of these gross defects. What was not filtered out were in fact in many cases almost failures that increased the mismatch fluctuations considerably.

The main lesson that was learned from this study was, that the microscopic look at the transistor provided by mismatch fluctuation characterisation, could reveal weaknesses in the technology. By looking at matched pairs, a seemingly harmless 1 to 2% parametric fluctuation in the product transistors was enlarged, exposing a real device architecture hazard.

The improved understanding of the device architecture helped to increase the yield of this particular process.

Chapter 5

Concluding remarks

5.1 Overview

This final chapter formulates some general conclusions based on the work as described in the preceding three chapters of this thesis. The most important contributions to the art of mismatch characterisation as reported in the open literature were already briefly summarised in section 1.4. After a short overview of the goals and themes of this work, general conclusions are formulated. This chapter ends with a brief outlook for some of the remaining challenges in the field of parametric mismatch characterisation.

The 'limits of matching' project that formed the basis of this thesis was founded on expertise that was built-up during many decades in the fields of small signal analogue circuit design and IC layout at the Philips Research Laboratories and in Philips Semiconductors' design and characterisation groups. This work has proven instrumental to maintain and strengthen our well-recognised position as one of the worlds leading expertise centres on mismatch and parametric fluctuations. The purpose of the work underlying this thesis was twofold.
The principal goal was to improve IC devices in terms of matching performance.
However, although parametric mismatch characterisation is strictly speaking not very different from regular parametric testing, during the investigations it was quickly realised that many test structure and data extraction technique refinements were required to meet the necessary characterisation precisions for proper statistical evaluation of matched pairs.
Consequently, a second goal unfolded during the work, namely the adaptation of matched pair test structures, measurement hardware use, and measurement and analysis algorithms to high-precision parametric mismatch characterisation. This thesis forms a documentation and justification of many good (and bad) practices that were encountered in this field. It is hoped that that this may help fellow researchers in this field to avoid many of the mistakes that can be made, were made, and in fact are still encountered regularly in the literature. Nevertheless, while this search for improved mismatch characterisation techniques was ongoing, the principal goal was still pursued. The insights that were gained about microscopic device architecture fluctuations through mismatch measurements proved instrumental for improving matching performance as well as product yield of MOS and BJT devices and circuits in several of Philips' CMOS and BiCMOS technologies.

5.2 General conclusions

The three theme related chapters encompass a large number of accumulated do's and don'ts, frequently learned the hard way. These are often based on experiences from (unreported) experiments that did not work or came out completely different from what was expected. This is partly attributable to the nature of this (industrial) research project. Many of the problems that were analysed, in fact originated from problems encountered in fabs or designs. Some of these inherited problems, often including existing test structures and measurement history, formed the basis of some of the most interesting results, but also for some of the biggest failures. Hence, this thesis was not written along the lines of a standard postulate-experiment-analyse research approach. This work is rather based on the accumulated experience of over 25 years of parametric testing and silicon device characterisation. One of the things that this experience learned is that there is no single best approach for parametric characterisation, nor does it make sense to claim such. The preferred method for a particular study always depends on the process development history, the (company, fab, institute) culture, and practical matters like available equipment, manpower and budget. It is the intention of this thesis to provide some of the arguments and the way of thinking that can help to decide why and how to proceed from various stages in a mismatch characterisation project. The careful reader will hence find many useful hints and conclusions in this thesis on how to choose and realise test structures and perform measurements and analyse parametric mismatch fluctuations.
On a more global level, the following conclusions can be summarised about the topics discussed in this thesis.

1. Mismatch measurements and process evaluation studies can only be successful when test structures, measurement system, measurement algorithms, statistical analysis techniques as well as good understanding of semiconductor device physics and IC technology, are combined. A healthy dose of scepticism and an eye for (statistical) details are indispensable when trying to characterise and interpret -often subtle- parametric fluctuation effects.

2. Adherence to the guidelines discussed in this thesis has led to mismatch test structures that allow characterising subtle effects down to below 0.01% mismatches. To reach such levels, the test structures must be laid-out painstakingly symmetrical, including identical environment around matched pairs up to at least 80 microns in any direction.

3. The use of Common contact pads must be avoided as much as possible, but where inescapable for the required measurement precision, connections should be based on double-

rail (star) layouts. Additional contact pads (or larger pads) should be used for force-sense techniques to mitigate impacts of probe-to-pad resistance differences and/or to allow hardware offset compensation measurements in critical studies.

4. During this project, the preference for test structure layouts shifted from combining multiple pairs in conventional 2xN contact pad frames to single matched pair test structure layouts in 1xM (scribe-line) pad frames. Albeit at the cost of relatively high contact pad utilization, scribe-line structures have proven to enable characterisation of subtle mismatch effects. The motto here is: rather have a small group of perfect structures than a larger group where concessions must be made in terms of layout consistency.

5. Based on detailed insights of the limitations of measurement hardware and measurement algorithms, and through properly applying statistical methods, it proves possible to conduct useful parametric mismatch studies at levels that are well below the specifications of the standard parametric measurement systems used to measure the devices.

6. The currently operational mismatch characterisation system can probably be considered as the most precise and versatile mismatch characterisation system in the world. With this system, systematic mismatches and parametric mismatch fluctuation standard deviations well below 0.01 % and 10 μV were measured and analysed.

7. Temperature stabilities of the pairs (on the wafer) as well as the temperature control of the measurement room around the equipment were demonstrated to be limiting factors for ultra high mismatch measurement (0.01 to 0.1%) precisions.

8. Several useful tricks of the trade are summarised in the section on measurement algorithms and hardware considerations, culminating in the M9S5 measurement algorithm that has proven to be very robust against many EMC disturbances and hardware settling problems.

9. The short-term repeatability of mismatch measurements forms a good indication of the capabilities of measurement systems. Moreover, it was demonstrated that the STR medians and standard deviations useful indications of the exact (calibration) status of the measurement hardware. Four different techniques are discussed, each with their own merits and disadvantages. The experience of this work learned that when measurement systems are used beyond their specification limits, regular monitoring of the system's status and performance

are a prerequisite for looking at sub 1 % mismatch effects. In this sense it was argued, and painfully demonstrated in the example of section 3.6, that it is more important to perform regular STR checks (and act by it), than what technique is actually used.

10. Parametric mismatch fluctuation studies are –by definition- based on statistics. This is a burden as well as a blessing. On one hand, statistical estimators are always prone to uncertainty. Hence, one is always looking for the largest possible population sizes to reduce the statistical uncertainties, albeit at the cost of (too) long measurement times. However, as the uncertainty only reduces with the square root of the number of observations (population size), measuring larger populations can only bring very limited relief. Therefore it is inevitable that mismatch estimators are never more than an estimate of the statistical fluctuation properties, with uncertainties generally of the order of 10 %, and seldom better than 1 %. The bootstrap method as applied frequently in this thesis provides useful feedback on the (estimated) uncertainty. On the other hand, statistics can be a blessing as it helps to get rid of irrelevant disturbances such as device defects, measurement failures and/or EMC disturbances from power lines, light switches, mobile telephones, etc. By applying a so-called safe estimation technique primarily based on range filtering and blunt axing, it proves possible to derive robust estimators that are primarily limited by their inherent statistical uncertainties.

11. Mismatch studies can provide unique insights into the (fluctuating) microscopic device architecture. Such insights are very hard to obtain using other characterisation techniques (SEM, TEM, SIMS, etc.), as these generally do no provide the accuracy or the possibility to analyse large numbers of specimens to allow proper statistical assessment.

12. Several new and/or recurring parametric mismatch effects were identified, quantified and de-mystified in this work. These insights contribute to a much better understanding of mismatch effects in analogue integrated circuit layouts. Although the art of analogue circuit design and layout will always keep elements of historical (hysterical) rules and remnants of horror stories (mismatch effects tend to disappear and return in subsequent process generations), the work in this thesis showed that many of the known but ill-understood effects can be identified and sometimes solved.

13. Good collaboration between electronic circuit designers, device characterisation specialists and process technology engineers is indispensable for mismatch improvement studies.
A devastating mismatch effect can reveal itself in a product while it can go un-noticed by

regular process characterisation measurements. It often takes dedicated test structures to mimic a source of mismatch as encountered in a circuit. This is particularly true for adjacent layout effects resulting in systematic mismatch. On the other hand, without detailed knowledge of the process flow, it is practically impossible to identify precisely which technological step or part of the flow is responsible for the observed mismatches. Close collaboration with the process owners is therefore essential for improving IC technologies in terms of mismatch performance.

14. The comprehensive overviews of matched pair test structures and mismatch characterisation techniques that are presented in chapters 2 and 3 are the first of their kind, and as such, these chapters fill major gaps in the existing mismatch characterisation literature. Overall, this thesis summarises the subtleties that are required for good parametric mismatch fluctuation characterisation. Electronic circuit designers can use the results for statistical circuit simulations, but this also provides technology developers a tool for optimising fluctuation related choices in their process architecture.

15. It pays to work on matching! With better insights into the microscopic device architecture fluctuations, integrated circuit process flow can be improved. This has resulted in higher product yields for analogue (mixed-signal) circuits as well as digital systems with large (embedded) memories.

5.3 Outlook and future challenges

More than 12 years of research have passed since the start of the parametric mismatch characterisation project that forms the basis of this thesis. Numerous studies were performed on different device types, built in many different IC technologies. Countless interesting effects were encountered, many errors were made, and substantial successes were accumulated. Of these high- and lowlights, only a limited number were discussed in this thesis. However, in mismatch research it is the same as in any in depth investigation: the more one learns, the more one sees that is not yet (fully) understood.

Aside from this general wisdom, it also happens to be true that the importance of parametric mismatch fluctuations has increased tremendously over the past decade. Parametric mismatch has developed from a typical analogue design issue to a digital performance (and yield) limiter in deep submicron ULSI systems. Primarily this is the consequence of the scaling of device dimensions. Now that many construction elements are no more than a few atomic layers thick, and performances effectively determined by no more than a couple of hundred of dopant atoms, effects of natural random fluctuations have increased dramatically. It can safely be predicted that with the continued scaling towards nanometre scale dimensions, impact of fluctuations will increase and become relatively more important as long as conventional device scaling persists.

New process and device architectures, such as high-K dielectrics, alternative gate-stacks, different substrates, hetero junctions, strained layers, etc, etc, are investigated extensively as possible approaches to maintain the historical performance improvement rate of IC technologies. Introduction of such new materials and construction concepts may be beneficial in terms of speed performance of the devices, but their implications on parametric fluctuations are yet to be characterised. In view of the regular (anticipated) use of silicon unfriendly materials, it seems quite likely that device fluctuation limitations will become even more dominant.
In this perspective, one can also be assured that the current drive towards nano bio devices, although incredibly attractive from a device research standpoint, will definitely not be more forgiving in terms of performance fluctuations. Compared to the perfectly organised microscopic device architectures based on mono crystalline silicon, the inherent chaos of bio-nano systems are bound to fluctuate orders of magnitude more. As argued in this thesis however, parametric fluctuation studies are the perfect tool for investigating limitations of such systems.

60As long as silicon-based systems form the driving-force behind improving computational and data processing engines, fluctuation hazards will need to be investigated. Parametric mismatch fluctuation forms an essential element of the much larger field of variability. This latter term accumulates the overall impact of device variations due to many uncertainty sources such as photolithography variations and line edge roughness (LER), process spreads, layout (environment), stress variations, on-chip EMC disturbances and cross-talk, reliability hazards like HCI and NBTI, etc, etc, etc. Variability control and development of design concepts to cope with increasing levels of variability and uncertainty are seen as the main issues that need to be resolved to enable construction of ULSI circuits with billions of transistors.

When technology scaling indeed reaches it's final red brick wall, the IC industry will continue to look for solutions to improve processes, or build systems more cost-effective. The search for device architectures that are less prone to microscopic fluctuations will definitely remain relevant. For semiconductor device characterisation specialists, a wealth of challenging device optimisation opportunities will emerge by the time the rat race along roadmaps has reached saturation. In this race, so many quick and dirty decisions are taken and so many details taken for granted, that numerous microscopic device architectural details are in fact still unknown or poorly understood.

In conclusion, a sheer infinite number of challenges and opportunities lie ahead for interesting and useful parametric device fluctuation studies!

Summary

Electrical characterisation of matched pairs for evaluation of integrated circuit technologies
H. P. Tuinhout
Ph.D. Thesis Delft University of Technology

This thesis is about electrical measurement methods and characterisation techniques for understanding and evaluating parametric mismatch fluctuations of closely spaced supposedly identical integrated circuit components. The main goal of this study is to find ways to improve the performance of mismatch sensitive integrated circuits. A secondary objective of the work evolved from the necessity to refine characterisation techniques for high-precision parametric mismatch studies. After the customary introductory chapter on the positioning of the research underpinning this work, this thesis is divided into three themes, corresponding to its chapters 2, 3 and 4.

Chapter 2 discusses the conception, design and realisation of matched pair transistor test structures. The chapter starts with a general introduction on test chips (PEM's and PCM's) and 2xN or 1xM contact pad frames. Subsequently it is explained that maximum characterisation flexibility and attainable measurement precisions form the main reasons for preferring conventional contact-pad-limited matched pair structures to addressable array-based parametric fluctuation evaluation structures. Chapter 2 continues with an overview of the criteria for choosing contact pad frames for matched pair test structures. It is shown that the inevitable probe-to-pad contact resistance fluctuations must be taken into account in the design and measurement philosophy for matched pair test structures. It is argued that sharing of pads in matched pair test structures should be avoided as much as possible, except where it is mandatory for achieving the required measurement accuracy. In the latter case, double-rail star connections are compulsory, as they assure equality of access resistances as well as optimal environmental layout symmetry. After an overview of design guidelines for matched pair test structures, several (good as well as not so good) examples of MOS and BJT matched pair test structure implementations are discussed. It is concluded that although being a pad-hungry solution, the single matched pair in a scribe-line 1xM pad frame module with Common Source or Emitter is the preferred test structure approach for research on parametric mismatch fluctuations.

Chapter 3 is about high-precision parametric mismatch measurements and data analysis techniques. This chapter begins with a general introduction on measurement hardware choices

that were made for the system on which this thesis is based. Subsequently, it is shown that temperature control of wafer as well as measurement room can form a limiting factor for extremely high-precision mismatch measurements. This also forms the explanation why the mismatch measurement station is not equipped with a thermo-chuck controller. A substantial part of this chapter is devoted to techniques for short-term repeatability (STR) assessment of parametric mismatch measurements. This is one of the most important tools to qualify and quantify the performance of statistical parametric mismatch measurements. Of the discussed techniques, the one with embedded STR assessment integrated into the mismatch measurement algorithm is preferred as it provides protection against misinterpretations of mismatch estimators related to measurement hardware noise or other artefacts. Subsequently, a number of tricks of the parametric measurement trade are discussed. Small mismatch measurements must be based on good understanding of measurement hardware limitations such as resolution and range transitions of sources and meters. A key technique for accurate statistical mismatch characterisation is based on the use of multiple observations (as for instance in the discussed M9S5 algorithm). It is shown that multiple observations can provide vital protections against EMC disturbances and potential hardware settling problems. Finally, some statistical analysis methods are reviewed which have proven to be essential for proper assessment of mismatch estimators. Safe estimation is a five-tier robust statistical estimation approach that provides optimum protection against measurement errors and faulty devices. The inevitable limitations associated with statistical uncertainties due to limited population sizes can be quantified through bootstrapping, a technique that can again also prove useful as a warning signal against outliers. Chapter 3 is completed with an example that demonstrates some of the hazards that can be encountered when measurement equipment is used at, or beyond the accuracy specifications

Chapter 4 focuses on how parametric mismatch fluctuation studies can be used for enhancing performance and yield of IC technologies. After recapping the four main mismatch trouble signals that have proven essential for recognising abnormalities in parametric mismatch observations, several examples of successful mismatch characterisation studies are discussed. These examples are divided into three groups, namely those related to metallisation on or near matched pairs, followed by an assessment of subtle stochastic fluctuation mechanisms, and finally some examples that are based on deviations from the elementary $1/\sqrt{(\text{area})}$ behaviour. The metal related examples show that stress asymmetries associated with asymmetrical layout features can easily result in substantial mismatches of the order of 1 to 10 %. Moreover, these examples illustrate why mismatch effects tend to be shrouded by a degree of mysteriousness

from the circuit designer's perspective, as they can appear and vanish in subsequent process generations. The 'decaborane study' is discussed here as an example of the evaluation of a stochastic fluctuation mechanism that is caused by the (fluctuating) microscopic device architecture. Despite its, in terms of device physics spectacular outcome, the discussion in this thesis focuses predominantly on the dilemmas and uncertainties that are inherent to the craft of process evaluation through characterisation of matched pairs, as this is more in line with the second objective of this thesis. The final two cases in this thesis show how interpretations of deviations from the elementary $1/\sqrt{(\text{area})}$ behaviour of mismatch fluctuations have helped to identify microscopic IC device architecture weaknesses. The poly-silicon morphology example demonstrates how an excessive mismatch fluctuation area-scaling factor for large devices, in combination with significant deviations for small dimension devices, led to identification of a new mismatch phenomenon in MOS devices. The other case, the so-called double-poly BJT riddle, was initiated by observations of strongly increased mismatches for narrow transistors. The study exposed a technological weakness in the emitter contact metallisation of these double-poly emitter BJT's. Both studies eventually led to improved process flows resulting in better matching performances as well as higher product yields.

In summary, this thesis discusses the skills and techniques that are required for parametric mismatch fluctuation characterisation with matched pair test structures. The resulting tools and systems provide integrated circuits technology developers possibilities for optimising fluctuation related choices in their process architecture. The lasting justification for the work on which this thesis is founded, is that studying statistical properties of parametric mismatches reveals valuable insights into (fluctuating) microscopic device architectures, which are hard, or even impossible to obtain with other analysis techniques. Parametric mismatch studies can hence be used to improve IC technologies, leading to better electronic circuit performances and higher product yields. As such, the approach as followed in this thesis forms a new direction in the field of parametric IC process characterisation.

Hans Tuinhout, October 2005

Nederlandse samenvatting

Elektrische karakterisatie van matched pairs voor evaluatie van IC technologiën
H. P. Tuinhout
Proefschrift ter verkrijging van de graad van doctor aan de Technische Universiteit Delft

Dit proefschrift gaat over elektrische meetmethodes en karakterisatietechnieken ten behoeve van het evalueren en begrijpen van fluctuaties van parametrische ongelijkheden (mismatch) tussen transistoren van dicht bij elkaar gelegen identiek veronderstelde paren (matched pairs) in geïntegreerde elektronische schakelingen (IC's).

Elektrische eigenschappen van micro-elektronische teststrukturen (waaronder matched pairs) worden op siliciumplakken gemeten om de prestaties en kwaliteit van IC fabricageprocessen te karakteriseren. Dergelijke teststrukturen worden daartoe verbonden met metalen contactvlakken (contact pads of bond pads). Deze worden op waferprobers gecontacteerd met naalden (probes) welke met geautomatiseerde meetapparatuur verbonden zijn. Meetprogramma's besturen deze apparaten en vertalen de gemeten elektrische gedragingen naar fysische grootheden en modelparameters. Omdat twee dicht bij elkaar gelegen transistoren van een paar gelijktijdig en onder vrijwel identieke omstandigheden vervaardigd worden, is hun parametrische ongelijkheid (mismatch) veelal klein. Daarentegen blijken de gemeten mismatches stochastisch van aard te zijn. Deze stochastische mismatch verschijnselen worden veroorzaakts door fluctuaties van microscopische constructie-elementen van de transistoren zoals doteringsatomen, ingebouwde electrische ladingen, randruwheden en korrelgrenzen.

Het primaire doel van het onderzoek dat ten grondslag ligt aan dit proefschrift is het verbeteren van prestaties van geïntegreerde electronische schakelingen welke gebaseerd zijn op zo gelijk mogelijke transistorparen. Een tweede doelstelling is voortgekomen uit de noodzakelijk gebleken verbeteringen van meet- en analysetechnieken voor het karakteriseren van, meestal kleine, parametrische mismatches. Na het gebruikelijke inleidende hoofdstuk omtrent de positionering van het onderzoek, is dit proefschrift opgedeeld in drie hoofdthema's, te weten teststrukturen, meettechnieken, en procesevaluatie, respectievelijk overeenkomend met de hoofdstukken 2, 3 en 4 van dit proefschrift.

Hoofstuk 2 bespreekt het plannen, ontwerpen en realiseren van micro-elektronische teststrukturen met transistorparen (matched pair test structures). Het hoofdstuk vangt aan met een algemene inleiding over testchips (PEM's, PCM's) en het gebruik van contact pad kaders.

Vervolgens wordt uitgelegd wat de voordelen zijn van de in dit proefschrift gebruikte (conventionele) contact-pad-begrensde teststrukturen boven vaak gebruikte adresseerbare matrix-teststrukturen. De conventionele strukturen bieden meer flexibiliteit en faciliteren nauwkeuriger metingen. Daarna wordt een overzicht gegeven van argumenten die bepalend zijn voor de keuze van contact pad kaders voor matched pair teststrukturen. Er wordt getoond dat zowel voor het ontwerp van de test struktuur als voor de definitie van de te gebruiken meetfilosofie rekening dient te worden gehouden met de onvermijdelijke fluctuaties van de probe naar pad contactweerstanden. Vervolgens wordt beredeneerd dat het gemeenschappelijk gebruik van contact pads zo veel mogelijk vermeden dient te worden, tenzij dit noodzakelijk is voor het bereiken van de vereiste meetnauwkeurigheid. In dat laatste geval zijn dubbelrails sterverbindingen onvermijdelijk aangezien deze de gelijkheid van aansluitweerstanden alsmede optimale omgevingssymmetrie verzekeren. Na een samenvatting van ontwerprichtlijnen voor matched pairs, worden verscheidene (goede zowel als minder goede) uitvoeringsvormen van MOS en bipolaire transistor matched pairs besproken. Er wordt geconcludeerd dat, hoewel behept met een relatief ongunstig verbruik van contact pads, de enkele transistorpaar met gemeenschappelijk Source of Emitter, in een (1xM) krasbaan pad frame de meest geschikte teststruktuurbenadering is voor onderzoek aan parametrische fluctuaties.

Hoofdstuk 3 gaat over meetmethodes en data-analyse technieken. Het eerste deel van het hoofstuk bespreekt apparatuurkeuzes die gedaan zijn voor de meetsystemen waar dit proefschrift op gebaseerd is. Vervolgens wordt getoond dat beheersing van de temperatuur van zowel plak als meetkamer beperkende factoren kunnen zijn voor extreem nauwkeurige mismatch metingen. Dit vormt bovendien de belangrijkste reden waarom een wafer prober zonder ingebouwde plaktemperatuur beheersing te prefereren is voor hoge precisie mismatch metingen. Een substantieel deel van dit hoofdstuk is gewijd aan technieken voor van het bepalen van de korte-termijn herhaalbaarheid van mismatch metingen. Deze vormen belangrijke hulpmiddelen om de prestaties van mismatch metingen te kwalificeren en te quantificeren. Van de besproken technieken blijkt de realisatie waarbij de herhaalbaarheidsmeting geïntegreerd is met de mismatch meting, in praktijk het beste te functioneren vanwege haar inherente beveiliging tegen misinterpretatie van statistische schatters als gevolg van meetruis en andere meetartefacten. Vervolgens worden een aantal specifieke meettechnische aandachtspunten voor mismatch metingen besproken. Kleine parametrische ongelijkheden kunnen namelijk alleen goed bepaald worden als precieze eigenschappen van het te gebruiken meetsysteem, zoals resoluties van bronnen en meters alsmede overgangen tussen meet- en bronbereiken, bekend zijn en derhalve vermeden worden. Een sleutelfactor

voor nauwkeurige mismatch metingen wordt gevormd door het toepassen van meervoudige waarnemingen met mediaan selectie (M9S5 algoritme). Dit blijkt een hoogstnoodzakelijke bescherming te bieden tegen verschillende vormen van overspraak en storingen alsmede stabilisatieproblemen van de meetapparatuur. Tenslotte worden in dit hoofdstuk enige statistische data-analysemethodes besproken waarvan eveneens gebleken is dat zij essentiëel zijn voor het op de juiste manier beoordelen van mismatch schatters. De kern wordt gevormd door het zogenaamde veilig schatten, een vijf-traps statistische schattingsmethode die optimale bescherming biedt tegen meetfouten en afwijkende componenten. Tevens wordt getoond dat de onvermijdelijke beperkingen aangaande statistische onzekerheden in verband met eindige steekproefgroottes uitstekend gekwantificeerd kunnen worden door middel van bootstrapping, een techniek die (wederom) van nut blijkt als waarschuwingssignaal tegen statistische uitbijters. Hoofdstuk 3 wordt besloten met een voorbeeld waarin enige van de gevaren gedemonstreerd worden zoals men die tegen kan komen wanneer meetapparatuur op de grens van, of zelfs voorbij de nauwkeurigheidsspecificaties gebruikt wordt.

Hoofdstuk 4 laat zien hoe karakterisatie van mismatch metingen kan bijdragen aan het verbeteren van prestaties en opbrengsten van IC-technologiën. In eerste instantie worden vier probleemsignalen besproken die cruciaal zijn gebleken voor het herkennen van abnormaliteiten in mismatch studies. Vervolgens worden verschillende voorbeelden van dergelijke studies behandeld, verdeeld over drie groepen. De eerste groep omvat een drietal voorbeelden van mismatch effecten die het gevolg zijn van metaal op, of nabij transistorparen. De tweede wordt toegelicht middels een uitgebreide evaluatie van een subtiel stochastisch fluctuatie studie. Tenslotte worden een drietal voorbeelden besproken die gebaseerd zijn op afwijkingen van het elementaire $1/\sqrt{(}$oppervlakte) mismatch fluctuatiegedrag. De besproken voorbeelden van metaaleffekten demonstreren dat metaalsporen op of nabij transistorparen tot substantiele systematische mismatches van de orde van 1 tot 10 % kunnen leiden. Deze voorbeelden illustreren tevens waarom, bezien vanuit het perspectief van een circuitontwerper zonder gedetailleerde kennis van de procesreceptuur, dit soort omgevingsgerelateerde mismatch effecten gepaard (lijken te) gaan met een substantiële graad van mysterieusheid. Ze blijken namelijk te kunnen verschijnen en/of verdwijnen in opeenvolgende CMOS procesgeneraties. Het besproken voorbeeld van karakterisatie van stochastische fluctuaties, het zogenaamde decaboraan experiment vormt zonder twijfel een van de fysisch/technologische hoogtepunten van dit onderzoek. De discussie in dit proefschrift richt zich echter voornamelijk op de dilemma's en onzekerheden die inherent zijn aan de kunst van procesevaluatie door middel van karakterisatie van parametrische mismatch, hetgeen meer in lijn is met de tweede doelstelling

van dit proefschrift. De laatste twee voorbeelden van dit proefschrift demonstreren hoe interpretaties van afwijkingen van het elementaire 1/√(oppervlakte) gedrag van mismatchfluctuaties kunnen bijdragen aan het identificeren van zwakheden van de microscopische architectuur van transistoren. Een voorbeeld betreffende de morfologie van het poly-silicium van de Gate in een MOSFET laat zien hoe een excessief hoge oppervlakteschalingsfactor van de mismatch fluctuatie van de drempelspanning, gekoppeld aan substantiële afwijkingen voor kleine transistoren, geleid heeft tot het identificeren van een nieuw fluctuatiefenomeen in MOS transistoren. Het afsluitende voorbeeld in deze sectie werd geïnitieerd door waarnemingen van sterk toegenomen mismatch fluctuaties bij smalle bipolaire transistoren. Deze studie bracht daarmee een technologische zwakheid in het emittercontact van deze transistoren aan het licht. Beide voorbeelden hebben uiteindelijk geleid tot verbeterde processreceptuur en hogere produktopbrengsten.

Samenvattend, bespreekt dit proefschrift vaardigheden en technieken voor het karakteriseren van mismatchfluctuaties door middel van transistorparen. De verkregen inzichten voorzien ontwikkelaars van IC technologiën van mogelijkheden voor het verbeteren van fluctuatie-eigenschappen van IC-processen. De blijvende rechtvaardiging voor het werk dat ten grondslag ligt aan dit proefschrift is, dat het bestuderen van de stochastische eigenschappen van parametrische verschillen waardevolle inzichten blijkt te verschaffen in de (fluctuerende) microscopische architectuur van IC-componenten. Dergelijke inzichten zijn niet, of veel moeilijker, te verkrijgen middels alternatieve analysetechnieken. Parametrische mismatch studies aan transistorparen kunnen derhalve gebruikt worden om IC-technologiën te verbeteren en ze resulteren in betere elektronische circuitprestaties en hogere productopbrengsten.
De benadering zoals beschreven in dit proefschrift vormt daarmee een nieuwe richting binnen het gebied van parametrische IC-proceskarakterisatie.

Hans Tuinhout, oktober 2005.

About the author

Hans Paul Tuinhout was born April 4th, 1956 in Djakarta, Indonesia. After receiving primary education in Den Haag and Amstelveen, he completed Atheneum B secondary education, at the Casimir Scholengemeenschap in Amstelveen, The Netherlands.

In 1974, he went to the Technische Hogeschool Delft, NL, now known as Delft University of Technology, to study electrical engineering. In 1980, he received his Ir. (M.Sc.) degree in electrical engineering. His engineers' exams were completed in the Electronic Materials group, where he did his first and second engineer's assignments on conductivity measurements of amorphous silicon layers for photovoltaic cells (with dr. M. Ondris), and on a silicon stress sensor based on strained MOS capacitors (with Prof. dr. Ir. S. Middelhoek) respectively. In 1978, he completed an internship at the Philips Natuurkundig Laboratorium in Eindhoven with Ir. M. J. J. Theunissen on p-n diode leakage current characterisation of gated diodes.

In 1980, Hans Tuinhout joined the Philips Natuurkundig Laboratorium in Eindhoven (Philips Research) for a permanent research position. His initial research topic focussed on latch-up characterisation, a new subject in the days when (N-Well) CMOS technologies did not exist yet (at Philips). After a year, he switched over to process characterisation and Philips' MOS (compact) model-7 parameter extraction for the emerging 2 μm (enhancement – depletion) NMOS technology. Since then, he remained involved in parameter extraction and parametric testing for subsequent CMOS process generations, including the MEGA project, the attempt of Philips to become a player in the SRAM memory market. Amongst other responsibilities, he was part of a team that realised a Keithley S300-based PCM test system that became the standard for Philips' MOS factories.

In 1989-1990, Hans P. Tuinhout spent a sabbatical year at the ECE department of Carnegie-Mellon University in Pittsburgh, PA, USA, working with Prof. dr. Andrzej Strojwas on process and device simulations with CMU's process engineer's workbench, in combination with Philips' MOS model parameter extraction techniques.

After this period, Hans Tuinhout rejoined Philips Research and became team member in a project developing a double-poly BiCMOS technology. In this team, he was responsible for device design, being his first thorough exposure to the technology and physics of bipolar junction transistors.

Since mid 1992, with brief excursions in the fields of laser photo-diodes and integrated power devices, Hans Tuinhout worked on the subject of matching. As will be obvious from this thesis, this has become a research topic that is close to his heart. The challenge of understanding and improving IC technologies through characterisation of subtle parametric effects in silicon devices at the edge or beyond the capabilities of parametric test equipment clearly found a perfect match.

Since 1989, Hans Tuinhout is an active programme committee member as well as a frequent presenter of papers and tutorials for the ICMTS, the International Conference on Microelectronic Test Structures. In 1989, he served as technical programme chairman, and he is a steering committee member. He received three ICMTS best-paper awards for work describing mismatch measurements and test structures.

Hans Tuinhout is happily married and is the proud father of four children in the ages of 16 to 25. His other hobbies are coffee (the challenge of brewing and the pleasure of drinking the perfect ristretto), news and modern history, listening to classical music, woodworking and furniture construction, and large-format black&white photography.

Acknowledgements

The work as described in this thesis was performed at the Philips Natuurkundig Laboratorium between 1992 and 2005. This work was conducted with the help of many friends and colleagues. I want to thank all who helped and supported me.

My gratitude goes in the first place to Maarten Vertregt and Marcel Pelgrom, my matching friends at Philips Research. They have initiated, facilitated and collaborated in word and deed, in many of the experiments discussed in this thesis.

The (retired) Philips Research statistician William Rey is gratefully acknowledged for his help and guidance at putting the outcome of fluctuating observations into perspective and for setting up proper tools to analyse parametric mismatch fluctuations.

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Lee Stauffer of Keithley Instruments is thanked for enthusiastic discussions and stimulating lessons on measurement hardware capabilities and limitations.

Regular encounters with semiconductor device characterisation specialists at the international conference on micro-electronic test structures (ICMTS) provided a basis for many discussions on measurement methods and test structures that proved fruitful as well as highly stimulating. I want to thank my fellow technical committee members and many fellow authors for helping to establish the conference in a conference: the international conference on matching test structures.

Several of the projects underpinning this thesis were based on dedicated technological experiments that had to be carried out with great care and high precision to capture the subtleties of parametric mismatch. In particular, I want to thank Peter Magnee, André Montree, Wim Peters (many times!), Peter Hartogs, Jurriaan Schmitz, Peter Stolk and Nicole Wils for their efforts in this respect.

Parametric mismatch fluctuation studies generally require (indirect) interpretation of semiconductor device physics. This implies that many different microscopic device architecture sources can be assumed to have caused the observed electrical fluctuations. It is therefore essential to discuss silicon device behaviour with colleagues, to assess the credibility of a particular explanation. Fortunately, Philips Research houses a group of renowned silicon device physics experts. Their open doors, discussions, explanations and good advices are greatly appreciated. In particular, I want to thank Jeroen Croon, Anco Heringa, Bert Huizing, Johan Klootwijk, Ronald van Langevelde, Peter Magnee, Jurriaan Schmitz, Jan Slotboom, Andries Scholten, Peter Stolk, Maarten Vertregt, Frans Widdershoven, Pierre Woerlee, Rob Wolters and Reinout Woltjer.

Many other (former) Philips colleagues have contributed to this work through providing material or ideas, serving as soundboard, co-authoring papers, and giving valuable feedback. I want to thank (in alphabetical order) Wilko Baks, Pascal Bancken, Serge Bardy, Christelle Biard, Wiebe de Boer, Arend Bretveld, Hans Brugman, Hans Buyk, Charles Dachs, Peter Deixler, Ronald Dekker, Bert Dirks, Do Dormans, Jan Engel, Heinze Elzinga, Christophe Erdmann, Stefan Hausser, Gian Hoogzaad, Jasper Groot Koerkamp, Dick Klaassen, Johan Knol, Rob Lander, Jacques Lebailly, Josine Loo, Harrie Maas, Christian Mion, Antoine Moonen, Som Nath, Wibo van Noort, Rene Penning de Vries, Walter Peters, Jose Pineda de Gyves, Jarich Politiek, Youri Ponomarev, Fokke Postma, Armand Pruymboom, Angel Rodrigues, Raf Roovers, Michiel Stoutjesdijk, Dave Szmyd, Karel van der Tak, Henk Termeer, Doeco Terpstra, Eugene Timmering, Doug Trotter, Rudolf Velghe, Jan Verhoeven, Pieter Voorenkamp, Marianne Webster and Dick Wind for their help and collaboration in the past and present.

My brothers in (Ph.D.) arms, Jeroen Croon (at IMEC), Regis Difrenza (at STm), Giovanni Annelli (at CERN) and Tony Ewert (at Uppsala University), are kindly acknowledged for the work we did together and the stimulating discussions on getting a Ph.D. on parametric mismatch fluctuations.

DIMES of the department of Electrical Engineering, Mathematics & Computer Science (EWI) at Delft University of Technology, and in particular my promotor Kees Beenakker, is acknowledged for providing the opportunity to write and defend this thesis.

Jeroen Croon, Johan Klootwijk, Marcel Pelgrom and Maarten Vertregt are gratefully acknowledged for reading and correcting (the fourth) concept of this thesis.

I want to thank Nicole Wils for her dedicated collaboration in the project and for helping to bring many of the matching characterisation projects to a success through precise measurement and analysis work.

My management at Philips Research is acknowledged for defending the project for me and assuring financial support for so many years. In particular, I want to thank Wil Josquin, Mart Graef, Max Collet and Carel van der Poel for their positive feedback and support. Reinout Woltjer deserves special honours. Not only did he manage to stay my (first line defence) group leader for more than a decade, but also he had the vision to support the need to invest in world-class measurement equipment. Moreover, he admirably kept track of the multitude of mismatch projects that came on the prober, commented and corrected many of the wildest ideas, and initiated several of the most valuable mismatch characterisation projects.

My friend Peer van der Kruis is particularly acknowledged for broadening my view on the world, ranging from modern art and graphical presentation skills, through the benefits of a bit of assertiveness at the right moments, up to initiating my interest for a lot of the classical music selections (such as the Bach cello suites) that accompanied the mostly pleasant hours of writing of this thesis. I am also very grateful to Peer and Anita for designing this well-matching book and helping to take the final hurdle in getting it printed.

I want to thank all my other friends, inside as well as outside Philips, who supported me in desperate moments and regularly reminded me that I had this job to finish.

My family, Anita, Wikke, Kalle, Monne and Jelle, provide the basis from which I work whenever wanted or needed. Obviously, writing a Ph.D. thesis like this outside office hours, consumed a considerable amount of free time and vacation weeks that could otherwise have been spent with the family. I thank my children and my loving wife for the room and support that they gave me to complete this task that I set myself.

Bibliography - B1 Overview of the author's matching related publications

Results that were obtained and characterisation techniques and insights that were developed based on the work described in this thesis were quite extensively reported in the external literature. Below, a (reverse) chronological list is given of all matching related papers that contributed to this thesis. In chapter 1 of this thesis, these papers are categorized and the contributions they represented to the field of matching are briefly summarized.

[Wils05] Nicole Wils, Hans Tuinhout, Tony Ewert, Jurgen van Berkum, Monja Kaiser and Robert Weemaes, "Identification and analysis of a new BJT parametric mismatch phenomenon" BCTM-2005

[Ewer05] Tony Ewert, Hans Tuinhout, Nicole Wils and Jorgen Olsson, "Design and implementation of an ultra high precision parametric mismatch measurement system", ICMTS05 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 149 -154, 2005

[Tuinh04a] H.P. Tuinhout, A. Bretveld and W.C.M. Peters, "Measuring the span of stress asymmetries on high-precision matched devices", ICMTS04 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp 117 - 122, 2004

[Tuinh04Tu] Hans Tuinhout, "Test structures for characterization of parametric mismatch and fluctuations", Invited tutorial short course at the ICMTS04.

[Pine04] Jose Pineda de Gyvez and Hans P. Tuinhout, "Threshold voltage mismatch and intra-die leakage current in digital CMOS circuits", IEEE Journal of Solid-State circuits, Vol 39 NO. 1, January 2004.

[Tuinh03c] Hans P. Tuinhout, "Improving BICMOS Technologies using BJT parametric mismatch variation", Invited paper, BCTM03 Proceedings of the IEEE Bipolar/BiCMOS Circuits and Technology Meeting, pp. 163 - 170, 2003.

[Tuinh03b] H.P. Tuinhout, G. Hoogzaad, M Vertregt, R.L.J Roovers, C. Erdmann, "Design and Characterisation of a High Precision Resistor Ladder Test Structure", IEEE Transactions on Semiconductor Manufacturing, Vol. 16 No. 2, pp. 187-193, 2003

[Tuinh03Tu] Hans Tuinhout, "Test structures for characterization of parametric mismatch and fluctuations", Invited tutorial short course at the ICMTS03.

[Tuinh03a] H.P. Tuinhout, A. Bretveld and W.C.M. Peters, "Current mirror test structures for studying adjacent layout effects on systematic transistor mismatch", ICMTS03 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 221-226, 2003.

[Dubo02] Jerome Dubois, Johan Knol, Mike Bolt, Hans Tuinhout, Jurriaan Schmitz and Peter Stolk, "Impact of source/Drain implants on threshold voltage matching in deep sub-micron CMOS technologies", ESSDERC02 Proceedings of the European Solid State Device Research Conference, pp. 115-118, 2002.

[Tuinh02b] Hans P. Tuinhout, "Impact of parametric mismatch and fluctuations on performance and yield of deep-submicron CMOS technologies", Invited paper, ESSDERC02 Proceedings of the European Solid State Device Research Conference, pp. 95-101, 2002.

[Croon02a] J.A. Croon, H.P. Tuinhout, D. Difrenza, J. Knol, A.J Moonen, S. Decoutere, H.E. Maes and W. Sansen, "A comparison of extraction techniques for threshold voltage mismatch", ICMTS02 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 235-240, 2002.

[Tuinh02a] H.P. Tuinhout, G. Hoogzaad, M Vertregt, R.L.J Roovers, C. Erdmann, "Design and Characterisation of a High Precision Resistor Ladder Test Structure", ICMTS02 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 223-228, 2002.

[Stolk01] P.A. Stolk, H.P. Tuinhout, R. Duffy, E. Augendre, L.P. Bellefroid, M.J.B. Bolt, J. Croon, C.J.J. Dachs, F.R.J. Huisman, A.J. Moonen, Y.V. Ponomarev, R.F.M. Roes, M. Da Rold, E. Seevinck, K.N. Sreerambhatla, R. Surdeanu, R.M.D.A. Velghe, M. Vertregt, M.N. Webster, N.K.J. van Winkelhoff and A.T.A. Zegers-van Duijnhoven, "CMOS Device Optimization for Mixed-Signal Technologies", Invited paper, IEDM01 Digest of Technical Papers, pp. 215-218, 2001.

[Tuinh01c]] Hans P. Tuinhout, Jurriaan Schmitz, Frans P. Widdershoven André H. Montree and Peter A. Stolk "Statistical Characterisation of MOSFET Matched Pairs: A Powerful Technique for Studying Microscopic Transistor Property Fluctuations", Invited paper, MRS spring meeting 2001.

[Tuinh01b] H.P. Tuinhout and M. Vertregt, "Characterization of Systematic MOSFET Current Factor Mismatch Caused by Metal CMP Dummy Structures", IEEE Transactions on Semiconductor Manufacturing, Vol. 14 No. 4, pp. 302-310, 2001.

[Tuinh01a] H.P. Tuinhout, J.H. Klootwijk, W.C. Goeke, L.K. Stauffer, "Impact of Transistor Noise on High Precision Parametric Matching Measurements", ICMTS01 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 201-206, 2001.

[Schmi01] J. Schmitz and H.P. Tuinhout, "A study of measurement system noise for sensitive soft breakdown triggering", ICMTS01 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 99-102, 2001.

[Tuinh00b] Hans Tuinhout, Frans Widdershoven, Peter Stolk, Jurriaan Schmitz, Bert Dirks, Karel van der Tak, Pascal Bancken and Jarich Politiek, "Impact of Ion Implantation Statistics on VT Fluctuations in MOSFET's: Comparison between Decaborane and Boron Channel Implants", VLSI00 Digest of Technical Papers Symposium on VLSI Technology, pp. 134-135, 2000.

[Tuinh00a] Hans Tuinhout, "Characterization of Systematic MOSFET Transconductance Mismatch", ICMTS00 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 131-136, 2000.

[Schm99] J. Schmitz, H.P. Tuinhout, A.H. Montree, Y.V. Ponomarev, P.A. Stolk and P.H. Woerlee, "Gate polysilicon optimization for deep-submicron MOSFET's", ESSDERC99 Proceedings of the European Solid State Device Research Conference, pp. 156-159, 1999.

[Mont99] A.H. Montree, Y.V. Ponomarev, W.M. Baks, A.C.M.C. van Brandenburg, C. Dachs, R.F.M. Roes, J. Schmitz, P.A. Stolk, H.P. Tuinhout, "Channel formation for 0.15 □m CMOS using through-the-Gate implantation", 1999 International Symposium on VLSI Technology, Systems, and Applications, pp. 10 –13, 1999.

[Tuin99Tu] Hans Tuinhout, "Test structures and techniques for characterisation of transistor matching", Invited tutorial short course at the ICMTS99.

[Pelg98] Marcel J.M. Pelgrom, Hans. P. Tuinhout and Maarten Vertregt, "Transistor matching in analog CMOS applications", Invited paper, IEDM98 Digest of Technical Papers, pp. 915-918, 1998.

[Tuin98Tu] Hans Tuinhout, "Transistor Matching; Characterization of differences between closely spaced identical transistors", Invited tutorial short course at the ICMTS98.

[Tuin98] H.P. Tuinhout, W.C.M. Peters, "Measurement of Lithographical Proximity Effects on Matching of Bipolar Transistors", ICMTS98 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 7-12, 1998.

[Tuin97b] H.P. Tuinhout, A.H. Montree, J. Schmitz and P.A. Stolk, "Effects of Gate Depletion and Boron Penetration on Matching of Deep Submicron CMOS Transistors", IEDM97 Digest of Technical Papers, pp. 631-634, 1997.

[Tuin97Tu] Hans Tuinhout, "Transistor Matching; Characterization of differences between closely spaced identical transistors", Invited tutorial short course at the ICMTS97.

[Tuin97a] H.P. Tuinhout, M. Vertregt, "Test Structures for Investigation of Metal Coverage Effects on MOSFET Matching", ICMTS97 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 179-183, 1997.

[MEAD-match 1996 - 2005] Lectures for MEAD Inc. Advanced Engineering Courses: in circulating order: Marcel Pelgrom, Hans Tuinhout and Maarten Vertregt, "Matching of MOS transistors", Monterey, Lausanne, 1996 – 2005.

[Tuin96b] Hans Tuinhout, Marcel Pelgrom, Rene Penning de Vries and Maarten Vertregt, "Effects of Metal Coverage on MOSFET Matching", IEDM96 Digest of Technical Papers, pp. 735-738, 1997.

[Tuin96a] Hans. P. Tuinhout, Heinze Elzinga, J. T. (Hans) Brugman and Fokke Postma, "The Floating Gate Measurement Technique for Characterization of Capacitor Matching", IEEE Transactions on Semiconductor Manufacturing Vol. 9, No. 1, pp. 2-8, 1996.

[Tuin95] H.P. Tuinhout, H. Elzinga, J.T. Brugman, F. Postma, "Accurate Capacitor Matching Measurements Using Floating Gate Test Structures", ICMTS95 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 133-138, 1995.

[Tuin94] H.P. Tuinhout, "Design of Matching Test Structures", ICMTS94 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 21-27, 1994.

Bibliography - B2 Used and cited literature

[Asen98] Asen Asenov, "Random Dopant Induced Threshold Voltage Lowering and Fluctuations in Sub-0.1 um MOSFET's: A 3-D "Atomistic" Simulation Study", IEEE Transactions on Electron Devices VOL. 45, NO 12, pp. 2505-2413, 1998.

[Bast95] J. Bastos, M. Steyaert, R. Roovers, P. Kinget, W. Sansen, B. Graindourze, A. Pergoot and Er. Janssens, "Mismatch characterization of small size MOS Transistors", ICMTS95 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 271-276, 1995.

[Bast96a] J. Bastos, M. Steyaert, B. Graindourze and W. Sansen, "Matching of MOS Transistors with Different Layout Styles", ICMTS96 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 17-18, 1996.

[Bast96b] J. Bastos, M. Steyaert, B. Graindourze and W. Sansen, "Influence of Die Attachment on MOS Transistor Matching", ICMTS96 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 27-31, 1996

[Bast97a] J. Bastos, M. Steyaert, A. Pergoot and W. Sansen, "Mismatch Characterization of Submicron MOS Transistors", Analog Integrated Circuits and Signal Processing, 12, pp. 95-106, 1997.

[Bast97b] Jose Bastos, Michel S.J. Steyaert, Anelia Pergoot and Willy M. Sansen, "Influence of Die Attachment on MOS Transistor Matching", IEEE Transactions on Semiconductor Manufacturing, Vol. 10 NO. 2, pp. 209-218, 1997.

[Bast98Th] Jose Bastos, "Characterization of MOS transistor mismatch for Analog Design", Ph.D. Thesis Katholieke Universiteit Leuven, 1998

[Brad01] Arthur T. Bradley, Richard C. Jaeger Jeffrey C. Suhling and Kevin J. O'Conner, "Piezoresistive Characteristics of Short-Channel MOSFET's on (100) Silicon", IEEE Transaction on Electron Devices, Vol. 48, No. 9, pp. 2009-2015, 2001

[Choi05] L.J. Choi, R. Venegas, and S. Decoutere, "Speed-accuracy trade-off for measurement and characterization of SiGe:C HBT's, applied to a 200 GHz technology", ICMTS05 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. xxx-yyy, 2005.

[Croo99] J. A. Croon, M. Rosmeulen, S. van Huylenbroeck and S. Decoutere, "A general modelfor MOS transistor matching", ESSDERC99 Proceedings of the European Solid State Device Research Conference, pp. 464-467, 1999.

[Croon00] J. A. Croon, M. Rosmeulen, S. Decoutere, W. Sansen and H. E. Maes, "A Simple and Accurate Deep Submicron Mismatch Model", ESSDERC00 Proceedings of the European Solid State Device Research Conference, pp. 356-359, 2000.

[Croon02a] J.A. Croon, H.P. Tuinhout, D. Difrenza, J. Knol, A.J Moonen, S. Decoutere, H.E. Maes and W. Sansen, "A comparison of extraction techniques for threshold voltage mismatch", ICMTS02 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 235-240, 2002.

[Croon02b] Jeroen A. Croon, Maarten Rosmeulen, Stefaan Decoutere, Willy Sansen and Herman E. Maes, "An Easy-to-Use Mismatch Model for the MOS Transistor", IEEE Journal of Solid-State Circuits VOL. 37, NO. 8, pp. 1056-1064, 2002.

[Croon02c] J.A. Croon, E. Augendre, S. Decoutere, W. Sansen and H.E. Maes, "Influence of doping profile and halo implantation on the threshold voltage mismatch of a 0.13 um CMOS technology", ESSDERC02 Proceedings of the European Solid State Device Research Conference, pp. 579-582, 2002

[Croon04Th] Jeroen A. Croon, "Matching properties of deep sub-micron MOS transistors", Ph.D. Thesis Katholieke

Universiteit Leuven, 2004
[Croon05] Jeroen A. Croon, Willy Sansen and Herman A. Maes, “Matching properties of deep sub-micron MOS transistors”, Springer 2005.
[Deveu05] J. Deveugele, L. Yao, M. Steyaert, W. Sansen, "Mismatch characterisation of chip interconnect resistance", ICMTS05 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 183-186, 2005.
[Diac83] Persi Diaconis and Bradley Efron, “Computer-Intensive Methods in Statistics”, Scientific American, vol. 248, pp. 96-108, 1983.
[Difr00] R. Difrenza, P. Llinares, G. Ghibaudo, E. Robillart and E. Granger, "Dependence of Channel Width and Length on MOSFET Matching for 0.18 um CMOS Technology", ESSDERC00 Proceedings of the European Solid State Device Research Conference, pp. 584-587, 2000.
[Difr01a] R. Difrenza, P. Llinares, E. Granger, H. Brut, G. Ghibaudo, “Effect of Substrate Voltage and Oxide Thickness on NMOSFET Matching Characteristics for a 0.18um CMOS Technology“, ICMTS01 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp 7-10, 2001.
[Difr01b] R. Difrenza, P. Llinares, G. Morin, E. Granger and G. Ghibaudo, "A New Model for Threshold Voltage Mismatch Based on the Random Fluctuations of Dopant Number in the MOS Transistor Gate", ESSDERC01 Proceedings of the European Solid State Device Research Conference. pp. 299-302, 2001.
[Difr02] R. Difrenza, P. Llinares, S. Taupin, R. Palla, C. Garnier, G. Ghibaudo, “Comparison Between Matching Parameters and Fluctuations at the Wafer Level“, ICMTS02 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 241-246, 2002.
[Difr02Th] Régis Difrenza, “Impact des fluctuations technologiques sur l’appariement du transistor MOS des filières 0.18 et 0.12 □m”. Ph.D. Thesis Institute Nationnal Polytechnique de Grenoble, 2002.
[Difr03] R. Difrenza, J.C. Vildeuil, P. Llinares and G. Ghibaudo, “Impact of grain number fluctuations in the MOS transistor Gate on matching performance“, ICMTS03 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 244-249, 2003.
[Difr05] R. Difrenza, K. Rochereau, T. Devoivre, B. Tavel, B. Duriez, D. Roy, S. Jullian, A. Dezzani, R. Boulestin, P. Stolk, M. Woo, F. Arnaud, “MOSFET matching improvement in 65 nm technology providing gain on both analog and SRAM performances“, ICMTS05 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 137-142, 2005.
[Dren98] Patrick G. Drennan, Colin C. McAndrew and John Bates, “A Comprehensive Vertical BJT Mismatch Model“, BCTM98 Proceedings of the Bipolar Circuits and Technology Meeting, pp. 83-86, 1998.
[Dren99a] P.G. Drennan, C.C. McAndrew, "A Comprehensive MOSFET Mismatch Model", IEDM99 Digest of Technical Papers, pp. 167-170, 1999.
[Dren99b] Patrick G. Drennan, "Diffused Resistor Mismatch Modeling and Characterization", BCTM99 Proceedings of the Bipolar Circuits and Technology Meeting, pp. 27-30, 1999.
[Dren99Th] Patrick G. Drennan, “Integrated circuit device mismatch modelling and characterization for analog circuit design”, Ph.D. Thesis Arizona State University, 1999.
[Drenn00] P.G. Drennan, C.C. McAndrew, J. Bates, D. Schroder, "Rapid Evaluation of the Root Causes of BJT Mismatch", Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 122-127, 2000.
[Drenn02a] Patrick G. Drennan, “Device Mismatch in BiCMOS Technologies“, BCTM02 Proceedings of the Bipolar Circuits and Technology Meeting, pp. 104-111, 2002.
[Drenn02b] P.G. Drennan and C.C. McAndrew, “Understanding MOSFET Mismatch for Analog Design“, CICC02 Proceedings of the IEEE 2002 Custom Integrated Circuits Conference, pp. 449-452, 2002.

[Dubo02] Jerome Dubois, Johan Knol, Mike Bolt, Hans Tuinhout, Jurriaan Schmitz and Peter Stolk, “Impact of source/Drain implants on threshold voltage matching in deep sub-micron CMOS technologies“, ESSDERC02 Proceedings of the European Solid State Device Research Conference, pp. 115-118, 2002.

[Einf04] J. Einfeld, U. Schaper, U. Kollmer, P. Nelle, J. Englisch and M. Stecher, “A new test circuit for the matching characterization of NPN bipolar transistors“, ICMTS04 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 127-131, 2004.

[Elzi96] H. Elzinga, "On the Impact of Spatial Parametric Variations on MOS Transistor Mismatch", Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 173-177, 1996.

[Elzi98] H. Elzinga, “Using Test Structures to Asses the Impact of Critical Process Steps on MOS Transistor Matching“, ICMTS98 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 119-122, 1998.

[Ewer05] Tony Ewert, Hans Tuinhout, Nicole Wils and Jorgen Olsson, “Design and implementation of an ultra high precision parametric mismatch measurement system", ICMTS05 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp 149 -154, 2005

[Ezak02] Tatsuya Ezaki, Takeo Ikezawa and Masame Hane, “Investigation of realistic dopant fluctuation induced device characteristics variation for sub 100 nm CMOS using atomistic 3-D process/device simulator“, IEDM02 Digest of Technical Papers, pp. 311-314, 2002

[Gray&Meyer] Paul R. Gray and Robert G. Meyer (et al.) "Analysis and Design of Analog Integrated Circuits, 2nd, 3rd and 4th ed.", John Wiley & Sons, 1984, 1996, 2001.

[Greg92] Richard W. Gregor, "On the Relationship Between Topography and Transistor Matching in Analog CMOS Technology", IEEE Transactions on Electron Devices Vol. 39, No. 2, pp. 275-282, 1992

[Hame86] M.F. Hamer, "First-order parameter extraction on enhancement silicon MOS transistors", IEE Proceedings, Vol. 133, Pt. I, No.2, pp. 49-54, 1986.

[Hast01] Alan Hastings, "The Art of Analog Layout", Several chapters of this book provide useful hints and suggestions concerning mismatch related tricks for analogue circuit layout. Prentice Hall, 2001.

[Haus02] Stefan Hausser, Stefan Majoni, Holger Schligtenhorst and Georg Kolwe, "Systematic Mismatch in Diffusion Resistors caused by Photolithography", ICMTS02 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 247-250, 2002.

[Hoen72] B. Hoeneisen and C.A. Mead, "Fundamental limitations in microelectronics-I MOS Technology", Solid-State Electronics, Vol. 15' pp. 819-829; 1972.

[Hors97b] J. T. Horstmann, U. Hilleringmann and K. Goser, "Detailed Matching Analysis of Sub-50 nm MOS-Transistors", ESSDERC97 Proceedings of the European Solid State Device Research Conference, pp. 240-243, 1997.

[Hors98b] J. T. Horstmann, U. Hilleringmann and K. Goser, "Correlation Analysis of the Statistical Electrical Parameter Fluctuations in 50-nm MOS-Transistorss", ESSDERC98 Proceedings of the European Solid State Device Research Conference., pp. 512-515, 1998.

[Huff] Darell Huff, How to lie with statistics, Penguin Books, 1954

[Keyes75] Robert W. Keyes, “The Effect of Randomness in the Distribution of Impurity Atoms on FET Thresholds”. Applied Physics Vol. 8, pp251-259, 1975.

[Kiba91] John K. Kibarian and Andrzej J. Strojwas, "Using Spatial Information to Analyze Correlations Between Test Structure Data", IEEE Transactions on Semiconductor Manufacturing", Vol. 4, No. 3, pp. 219-225, 1991.

[Killm] Keithley Instruments, “Low Level Measurements”, 5th Edition, 1998 Keithley Instruments Inc.

[King96] Peter Kinget and Michiel Steyaert, "Impact of transistor mismatch on the speed-accuracy-power trade-off of analog CMOS circuits", CICC96 IEEE Custom Integrated Circuits conference, pp. 333-336,1996.

[Laks86] Kadaba R. Lakshmikumar, Robert A. Hadaway and Miles A. Copeland, "Characterization and Modeling of Mismatch in MOS Transistors for Precision Analog Design", IEEE Journal of Solid-State Circuits, Vol. 21, No. 6, pp. 1057-1066, 1986.

[Lau03] Guenter Lau, Wolfgang Einbrodt and Wilfried Sieber, "Improvement of poly Emitter n-p-n transistor matching in a 0.6 micron mixed signal technology", ICMTS03 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 232-237, 2003.

[Leff03] R. Lefferts and C. Jakubiec, "An integrated test chip for the complete characterization and monitoring of a 0.25um CMOS technology that fits into five scribe line structures 150um by 5,000um", ICMTS03 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 59-63, 2003.

[Linn98]Carsten G. Linnenbank, Werner Weber, Ute Kollmer, Birgit Holzapfl, Staphan Sauter, Ulrich Schaper, Ralf Brederlow, Sassan Cyrusian, Sylvia Kessel, Roland Heinrich, Erich Hoefig, Gerhard Knoblinger, Alfred Hesener and Roland Thewes, "What Do Matching Results of Medium Area MOSFET's Reveal for Large Area Devices in Typical Analog Applications?", ESSDERC98 Proceedings of the European Solid State Device Research Conference, pp. 104-107, 1998.

[Love94T] Simon J. Lovett, "Characterization of MOS Transistor Mismatch for Micron and Submicron Devices", M.Sc. Thesis NMRC - University College Cork, 1994.

[Love96] S.J. Lovett, M. Welten, A. Mathewson and B. Mason, "Characterising the Mismatch of Submicron MOS Transistors", ICMTS96 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 39-42, 1996.

[McCr81] James L. McCreary, "Matching Properties, and Voltage and Temperature Dependence of MOS Capacitors", IEEE Journal of Solid-State Circuits VOL. SC-16, NO. 6, pp. 608-616, 1981.

[Mich91T] Christopher Michael, "Statistical modelling for computer-aided design of analog MOS integrated circuits", Ph.D. Thesis Ohio State University, 1991

[Mizu93] Tomohisa Mizuno, Jun-Ichi Okamura and Akira Toriumi, "Experimental Study of Threshold Voltage Fluctuation Using an 8k MOSFET's Array", VLSI93 Symposium on VLSI Technology Digest of Technical Papers,pp. 41-42,1993.

[Mizu94] Tomohisa Mizuno, Jun-Ichi Okamura and Akira Toriumi, "Experimental Study of Threshold Voltage Fluctuation due to statistical Variation of Channel Dopant Number in MOSFET's", IEEE Transactions on Electron Devices, Vol. 41, No 11, pp. 2216-2221,1994.

[Mani00T] Dragan Manic, "Drift in silicon integrated sensors due to thermo-mechanical stresses", Ph.D. Thesis Ecole Polytechnique Federal de Lausanne, 2000

[Mont99] A.H. Montree, Y.V. Ponomarev, W.M. Baks, A.C.M.C. van Brandenburg, C. Dachs, R.F.M. Roes, J. Schmitz, P.A. Stolk, H.P. Tuinhout, "Channel formation for 0.15 □m CMOS using through-the-Gate implantation", 1999 International Symposium on VLSI Technology, Systems, and Applications, pp. 10 –13, 1999.

[Muller&Kamins] Richard S. Muller and Theodore I. Kamins, "Device Electronics for Integrated Circuits, Second Edition", John Wiley & Sons, Inc, 1986.

[m-w'match')] http://www.m-w.com/cgi-bin/dictionary Merriam-Webster On-line dictionary, keyword "match".

[m-w'mate'] http://www.m-w.com/cgi-bin/dictionary Merriam-Webster On-line dictionary, keyword "mate".

[Niew97] Mariusz Niewczas, "Characterisation of the Threshold Voltage Variation: a Test Chip and the Results", ICMTS97 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 169 – 172, 1997.

[Ohka03] S. Ohkawa, M. Aoki and H. Masuda, "Analysis and characterization of device variations in an LSI chip using an integrated device matrix array", ICMTS03 Proceedings of the IEEE International Conference on

Microelectronic Test Structures, pp. 70-75, 2003.
[Ohzo98] Takashi Ohzone, Tetsu Miyakawa, Toshihiro Matsuda, Toshiki Yabu and Shinji Odanaka, “Influence of Asymmetric/Symmetric Source/Drain Region on Asymmetry and Mismatch of CMOSFET's and Circuit Performance“,IEEE Transactions on Electron Devices, Vol. 43, No.2, pp. 529-537, 1998.
[Pava94] Aleksandra Pavasovic, Andreas G. Andreou and Charles R. Westgate, "Characterization of Subthreshold MOS Mismatch in Transistors for VLSI Systems", Journal of VLSI Signal Processing, Vol. 8, pp. 75-85, 1994.
[Pelg89] Marcel. J. M. Pelgrom, Aad C.J. Duinmaijer and Anton P.G. Welbers, "Matching Properties of MOS Transistors", IEEE Journal of Solid-State Circuits Vol. 24, No. 5, pp. 1433-1439, 1989.
[Pelg94] M.J.M. Pelgrom, A.C. van Rens, M. Vertregt and M.B. Dijkstra, “A 25-Ms/s 8-bit CMOS A/D converter for embedded applications”, IEEE Journal of Solid-State Circuits, vol. SC-29, pp 879-886, 1994.
[Pelg98] Marcel J.M. Pelgrom, Hans. P. Tuinhout and Maarten Vertregt, "Transistor matching in analog CMOS applications", IEDM98 Digest of Technical Papers, pp. 915-918, 1998.
[Perg98] A. Pergoot, P. Cox, P. Vercruysse, I. Wuyts and P. Raes, "New Method for Monitoring of Analogue Process - Evaluation of the Impact of Metalisation on the Performance of Precise Analogue Resistors", ICMTS98 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 13-17, 1998.
[Pine04] Jose Pineda de Gyvez and Hans P. Tuinhout, “Threshold voltage mismatch and intra-die leakage current in digital CMOS circuits”, IEEE Journal of Solid-State circuits, Vol 39 NO. 1, January 2004.
[Port98] Lionel Portmann, Christophe Lallement and Francois Krummenacher, “A High Density Integrated Test Matrix of MOS Transistors for Matching Study“, ICMTS98 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 19-24, 1998.
[Quar03] Michele Quarantelli, Sharad Saxena, Nicola Dragone, Jeff A. Babcock, Christopher Hess, Sean Minehane, Steve Winters, Jianjun Chen, Hossein Karbasi and Carlo Guardiani, “Characterization and Modeling of MOSFET Mismatch Of a Deep Submicron Technology“, ICMTS03 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 238-243, 2003.
[Roch04] K. Rochereau, R. Difrenza, J. Mc Ginley, O. Noblanc, C. Julien, S. Parihar, P. Llinares, “Impact of pocket implant on MOSFET mismatch for advanced CMOS technology“, ICMTS04 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 123-126, 2004.
[Rey] William J. J. Rey , “Introduction to Robust and Quasi-Robust Statistical Methods”. Springer Verlag, 1983.
[Scha00] Ulrich Schaper, Carsten Linnenbank and Roland Thewes, “A Novel Approach for Precise Characterization of Long Distance Mismatch of CMOS Devices“, ICMTS00 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 148-152, 2000.
[Scha01a] Ulrich Schaper, Carsten Linnenbank, Ute Kollmer, Hans Mulatz, Tobias Mensing, Roland Schmidt, Rainer Tilgner and Roland Thewes, “Evaluation of the Impact of Mechanical Stress on CMOS Device Mismatch“, ICMTS01 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 1-6, 2001.
[Scha01b] Ulrich Schaper, Carsten G. Linnenbank and Roland Thewes, “Precise Characterization of Long-Distance Mismatch of CMOS Devices“, IEEE Transactions on Semiconductor Manufacturing, Vol. 14, No. 4, pp. 311-317, 2001.
[Scha05] Ulrich Schaper, Jan Einfeld and Anke Sauerbrey, “Parameter Variation on Chip-Level“, ICMTS05 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 155-158, 2005.
[Schm99] J. Schmitz, H.P. Tuinhout, A.H. Montree, Y.V. Ponomarev, P.A. Stolk and P.H. Woerlee, “Gate polysilicon optimization for deep-submicron MOSFET's“, ESSDERC99 Proceedings of the European Solid State Device Research Conference, pp. 156-159, 1999.
[Schmi01] J. Schmitz and H.P. Tuinhout, “A study of measurement system noise for sensitive soft breakdown

triggering“, ICMTS01 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 99-102, 2001.
[Schroeder] Dieter K. Schroeder, “Semiconductor material and device characterization, Second Edition”, John Wiley & Sons, Inc, 1998
[Serr99] Teresa Serrano-Gotarredonna and Bernabe Linares-Barranco, "Systematic Width-and-Length Dependent CMOS Transistor Mismatch Characterization and Simulation", Analog Integrated Circuits and Signal Processing, 21, pp. 271-296, 1999.
[Serra00] Teresa Serrano-Gotarredonna, Bernabe Linares-Barranco, "A New Five Parameter MOS Mismatch Model", IEEE Electron Device Letters, 21, No 1, pp. 37-39, 2000.
[Shim02] Y. Shimizu, M. Nakamura, T. Matsuoka and K. Taniguchi, "Test structure for precise statistical characteristics measurement of MOSFET's", ICMTS02 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 49- 54, 2002.
[Shyu82] Jyn-Bang Shyu, Gabor C. Temes and Francois Krummenacher, "Random Errors in MOS Capacitors", IEEE Journal of Solid-State Circuits Vol. 17, No. 6, pp. 1070-1076, 1982.
[Shyu84] Jyn-Bang Shyu, Gabor C. Temes and Kung Yao, "Random Error Effects in Matched MOS Capacitors and Current Sources", IEEE Journal of Solid-State Circuits Vol. 19, No. 6, pp. 948-955, 1984.
[Sing89a] Rajinder Singh and A.B. Bhattacharyya, “Matching properties of linear MOS capacitors“, IEEE Transactions on Circuits and Systems , Vol. 36 No.3, pp. 465-467, 1989.
[Slotboom] A. Slotboom, “Statistiek in woorden”, Wolters-Noordhoff, 1996
[Stey97] M. Steyaert,V. Peluso, J. Bastos, P. Kinget and W. Sansen, "Custom Analog Low Power Design: The problem of low voltage and mismatch", CICC97 Proceedings of the IEEE Custom Integrated Circuits Conference, pp. 285-292, 1997.
[Stol96] Peter A. Stolk, and D.B.M. Klaassen, "The effect of statistical dopant fluctuations on MOS device performance", IEDM96 Digest of Technical Papers, pp. 627-630, 1996
[Stol98] Peter A. Stolk, Frans P. Widdershoven and D.B.M. Klaassen, "Modeling Statistical Dopant Fluctuations in MOS Transistors", IEEE Transactions on Electron Devices Vol. 45, No, 9, pp. 1960-1971, 1998.
[Stolk01] P.A. Stolk, H.P. Tuinhout, R. Duffy, E. Augendre, L.P. Bellefroid, M.J.B. Bolt, J. Croon, C.J.J. Dachs, F.R.J. Huisman, A.J. Moonen, Y.V. Ponomarev, R.F.M. Roes, M. Da Rold, E. Seevinck, K.N. Sreerambhatla, R. Surdeanu, R.M.D.A. Velghe, M. Vertregt, M.N. Webster, N.K.J. van Winkelhoff and A.T.A. Zegers-van Duijnhoven, "CMOS Device Optimization for Mixed-Signal Technologies", IEDM01 Digest of Technical Papers, pp. 215-218, 2001.
[Take97] K. Takeuchi, T. Tatsumi and A. Furukawa, “Channel engineering for the reduction of random-dopant-placement-induced threshold voltage fluctuation”, IEDM97 Digest of Technical Papers, pp. 841-844, 1997
[Tama91] E. Tamaki, T. Hashimoto, K. Watanabe, T. Shiba, "Evaluation of the fluctuation of High-Performance IDP Emitter Transistors by Using Test Structures", ICMTS97 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 189-193, 1997.
[Tera03] K. Terada, and M. Eimitsu, "A Test Circuit for Measuring MOSFET Threshold Voltage Mismatch", ICMTS03 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 227-231, 2003
[Tera04] K. Terada, and K. Fukeda, "Further study of V_{TH}-Mismatch Evaluation Circuit", ICMTS04 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 165-169, 2004.
[Tera05] K. Terada, T. Yamauchi and A. Ueki, "Physical meaning of Value Estimated with V_{TH}-Mismatch Evaluation Circuit", ICMTS05 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 165-169, 2005.
[Thew98] Roland Thewes, Ralf Brederlow, Claus Dahl, Ute Kollmer, Carsten G. Linnenbank, Birgit Holzapfl, Jan

Becker, Jens Kissing, Sylvia Kessel and Werner Weber, "Explanation and Quantitative Model for the Matching Behavior of Poly-Silicon Resistors", IEDM98 Digest of Technical Papers, pp. 771-774, 1998.

[Thibe01] Helene Thibieroz, Pat Shaner, Zeynep Celik Butler' "Mismatch and Flicker Noise Characterization of Tantalum Nitride Thin Film Resistors for Wireless Applications", ICMTS01 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 207-212, 2001.

[Tuin88] H. P. Tuinhout, S. Swaving and J. J. M. Joosten "A fully analytical mosfet model parameter extraction approach", ICMTS88 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 79-84, 1988.

[Tuto9x] For many years, the International Conference on Microelectronic Test Structures (ICMTS) has organised tutorial short courses on various aspects of test structure design and measurements. Many recognized experts in the field have contributed a wealth of information on elementary as well as advanced good practices.

[Wils05] Nicole Wils, Hans Tuinhout, Tony Ewert, Jurgen van Berkum, Monja Kaiser and Robert Weemaes, "Identification and analysis of a new BJT parametric mismatch phenomenon" BCTM 20005

[Wolf] Stanley Wolf , "Silicon Processing for the VLSI era, Volume 2 Process Integration", Lattice Press, 1990.

[Wolf&Tauber] Stanley Wolf and Richard N. Tauber, "Silicon Processing for the VLSI era, Volume 1 Process Technology Second Edition", Lattice Press, 2000.

[Wong96] Shyh-Chyi Wong, Kuo-Hua Pan, Dye-Jyun Ma, M.S. Liang and N. Tseng, "On Matching Properties and Process factors for Submicron CMOS", ICMTS96 Proceedings of the IEEE International Conference on Microelectronic Test Structures, pp. 43-47, 1996.

Colophon

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