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Low-temperature aluminum-induced layer exchange of Ge on Si for CMOS-compatible SiGe integration

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ABSTRACT

Low-temperature (≤ 350 °C) aluminum-induced layer exchange enables the integration of large-grained poly-crystalline silicon–germanium layers into silicon-based optical, electronic, and electromechanical sensors, either in post-processing or at the back-end-of-line of a CMOS flow. We systematically investigate how annealing conditions, metal composition, diffusion control layer, and Al/a-Ge thicknesses influence the crystallization process and the resulting silicon–germanium layer. Our results reveal tunable correlations between process parameters and layer properties, demonstrating that both the crystallinity and the composition of the final layer can be precisely controlled. This work provides practical guidelines for tailoring aluminum-induced layer exchange for silicon–germanium integration across diverse device applications.

1. Introduction

The integration of high-quality crystalline Si_xGe_{1-x} (SiGe) on Si is a key step toward next-generation optical, electronic, and electromechanical devices. SiGe/Si systems serve a wide range of applications, including buffer layers for the epitaxy of Ge films on Si [1,2], absorber layers for broadband optical sensors [3,4], piezoresistive and capacitive layers for electromechanical sensors [5]. Additionally, tuning the composition of the SiGe layer allows precise control over physical properties of the material, such as bandgap and lattice constant [6]. Conventional methods such as molecular beam epitaxy (MBE) [2] or chemical vapor deposition (CVD) [1,3] require high temperatures (400 °C–600 °C), high vacuum conditions (5×10^{-11} mbar–1.5×10^{-9} mbar), and often toxic gases such as silane, germane, and H_2. This not only significantly increases fabrication costs but also prevents post-processing or back-end-of-line (BEOL) integration in CMOS flows. Alternatively, aluminum-induced layer exchange (AILE) offers a low-cost, low-temperature (≤350 °C) process with no toxic precursors, compatible with post-processing and BEOL integration. Although the feasibility of AILE has been widely demonstrated [7], most studies have focused on silicon oxide substrates [8–10]. In contrast, systematic investigations of AILE directly on silicon, as well as a quantitative understanding of how process parameters influence the resulting SiGe crystal quality and composition, are still lacking. To address this gap, we conducted a comprehensive study on the effects of annealing conditions, metal composition, diffusion control layers, and initial thickness in SiGe layers grown through AILE on silicon. Our results provide new insights into process-structure relationships and offer practical guidelines for low-temperature integration in optical, electronic, and electromechanical sensors.

2. Materials and methods

The process flow of the low-temperature integration of SiGe on Si substrate is illustrated in Fig. 1.

4-inch 1–5 Ω · cm p-type Si(100) wafers were used as substrates in this work. The native oxide of Si was etched by HF (5 %). Magnetron sputtering was employed to deposit aluminum and amorphous germanium (a-Ge) layers. We identified an Al/a-Ge thickness ratio of 1:1.2 as an effective compromise between poly-Ge islands and SiGe coverage. In addition to the Al (99.999 % purity) target, generally used for AILE, we also used an Al-Si (1 wt% Si) (AlSi) target to evaluate the impact of 1 % silicon on the growth process and resulting layers. The Al and AlSi layers were sputtered at room temperature at a 1.96 nm s^{-1} and 6.25 nm s^{-1}, respectively. Before Ge deposition, some wafers were exposed to air for 30 s to obtain an AlO_x diffusion control layer of about 3 nm. Then, amorphous Ge films were sputtered at room temperature using a Ge target (99.999 % purity) at a 3.3 nm min^{-1} deposition rate. The

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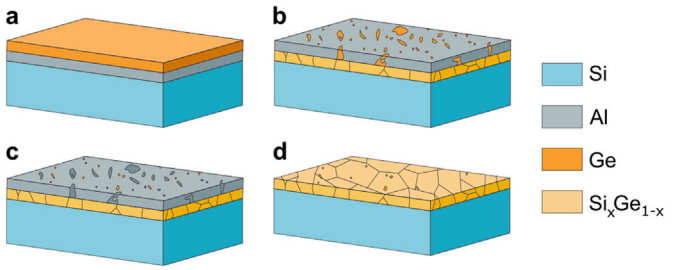

Fig. 1. Process flow of SiGe layer integration.a Metal and a-Ge sputtering. **b** Low-temperature annealing. **c** H_2O_2 (30 %) etching. **d** HF (5 %) etching.

Table 1
Fabricated samples with corresponding thicknesses of metal, AlO_x, and Ge layers.

Sample	A50	A100	A150	A300	AO50	AO100	AO300
Al[a] (nm)	50	100	150	300	–	–	–
AlO_x (nm)	–	–	–	–	50	100	300
Ge (nm)	60	120	180	360	60	120	360

[a] Samples with the same thicknesses fabricated using an AlSi target are labeled SX and SOX, where X is the AlSi thickness.

thicknesses of Al and Ge are summarized in Table 1. After deposition, wafers were diced in 2 cm × 2 cm dies. Finally, the samples were annealed at 300 °C, 325 °C and 350 °C for different periods of time in an N_2 environment. The annealing process was divided into annealing cycles to monitor the SiGe growth. Cycles of 5 h were used for the first 25 h of annealing, followed by 25-hour cycles. Each annealing cycle was preceded by a first ramp-up to 200 °C (heating rate of 4 °C min^{-1}), followed by a second ramp-up to the final annealing temperature (heating rate of 3.75 °C min^{-1}). Lastly, the top layer was removed through a two-step etching process: first, the poly-Ge islands were etched in H_2O_2 (30 %) solution; then, the Al was removed by HF (0.5 %) wet etching.

The thicknesses of the as-deposited layers were verified through cross-sectional scanning electron microscopy (SEM). The thickness of the native AlO_x layer was measured by scanning transmission electron microscopy (STEM). The growth of Al-rich regions on the surface and SiGe crystals underneath was monitored at the end of each annealing cycle by SEM. We used a neural network trained on processed SEM images to identify nucleation sites and track their evolution under different process parameters. Detailed information on neural network training and validation is reported in A. The coverage of the polycrystalline layer was investigated using SEM after a-Ge and Al removal. The composition of the layers before and after annealing was analyzed through secondary-ion mass spectrometry (SIMS). The crystal quality of the SiGe layers was studied through electron backscatter diffraction (EBSD).

SEM images used by the neural network were acquired from five regions on each die, i.e., four corners and the center. Average values for each region were used to obtain standard deviations, shown as error bars in the graphs to represent spatial variability. EBSD mapping was performed on areas of approximately 50 μm × 50 μm. The standard deviation of the grain size within the same area was calculated and plotted as error bar, indicating data dispersion. The standard deviation of the (100)-oriented fraction for different areas is shown as error bar in the graphs, representing spatial variability. SIMS measurements were conducted on two different regions of each die, and the averaged results are reported in the plots.

3. Results and discussion

Cross-sectional SEM performed after deposition revealed a negligible error (lower than 5 %) in the thicknesses. STEM showed an average thickness of 2.6 nm ± 0.7 nm of the native AlO_x layer. The observed relatively high thickness variation is consistent with the spontaneous, non-uniform growth of native oxide formed under ambient exposure.

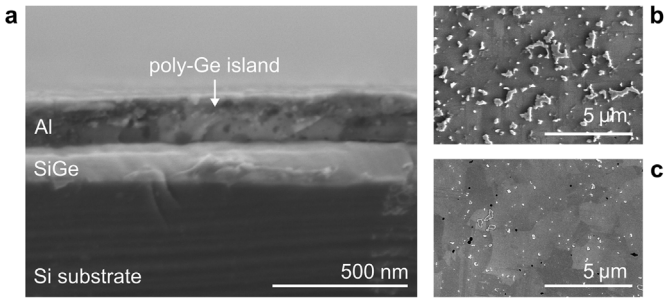

Fig. 2. SEM images of the SiGe layer. a Cross-section of A150 after 25 h at 350 °C. **b** Image of SO100 after 25 h at 350 °C and 7 min HF etching. **c** Image of SO100 after 25 h at 350 °C, 2 h H_2O_2 etching and 7 min HF etching.

All samples underwent a minimum of 25 h annealing. After 25 h, the annealing was continued until (i) the layer exchange was complete, defined as SiGe coverage greater than 95 %, or (ii) the SiGe growth saturated, meaning that two subsequent annealing cycles resulted in less than 10 % additional coverage. The total annealing time and the corresponding SiGe average coverage reached for each sample are reported in B. Missing data points in the subsequent plots correspond to samples for which the layer exchange was not completed within the applied annealing conditions.

Although the 1:1.2 Al/a-Ge thickness ratio ensures full coverage of the SiGe layer, a thicker a-Ge layer leads to the formation of residual Ge islands at the end of the AILE process [10]. EBSD analysis confirms that these islands, observed in all samples, are polycrystalline, as reported in previous studies [11,12], and have grain sizes of a few hundred nanometers. As shown in the literature [12,13], most islands stick out from the top layer and extend throughout the metal thickness down to the SiGe surface (Fig. 2(a)). This enables selective etching of poly-Ge islands through diluted H_2O_2 using the metal layer as a perfectly aligned mask [12]. Fig. 2(b-c) show that introducing the H_2O_2 etching step significantly reduced their number. However, extensive etching to fully remove them also damages the underlying SiGe layer.

To gain a deeper understanding of layer exchange dynamics, we monitored the evolution of both SiGe crystals and Al-rich surface regions during annealing. Since the upward displacement of Al accompanies the lateral growth of the underlying SiGe grains, we investigated whether the morphology of the Al-rich regions correlates with the initial Al/a-Ge properties or with the final SiGe characteristics. The neural network extracted their number, size, spacing, and total surface coverage. No correlation was found between these parameters and the initial Al/a-Ge layer thickness; therefore, these results are not further discussed in this work. However, we demonstrate that both growth rate and density of the Al-rich regions depend on annealing conditions, metal composition, and presence of an interdiffusion layer. These relationships, along with the study of the effects of the varied process parameters on the final crystal quality and composition, are discussed in detail in the following sections.

3.1. Metal composition

The first process parameter under investigation is the composition of the deposited metal layer. We found that using an AlSi target accelerates AILE to the detriment of crystal quality. As shown in Fig. 3(a), the addition of 1 % Si increases the SiGe growth rate: samples such as A100, which do not complete AILE within 25 h at 350 °C, achieve full layer exchange in 5 h when Si is introduced. In contrast, the average grain size and (100)-oriented fraction are significantly reduced (Fig.

3(b-c)). This behavior arises from the reduced density and grain size of the AlSi layer [14], which enhance Ge diffusion and increase nucleation site density, i.e., defects or grain boundaries with low surface energy. Additionally, Si grains at the substrate interface formed at the early stage of AILE [15] might act as pre-existing nuclei, further promoting the SiGe growth. Consequently, smaller, randomly oriented crystals are formed.

The Si atoms in the metal target directly affect the final composition of the SiGe layer. SIMS compositional profiles of the AILE-grown layer of samples A50 and S50 after 25 h annealing at 350 °C (Fig. 3(d,e)) reveal a slightly higher Si content (about 2 %) within the final layer and a broader Al peak at the substrate interface for the AlSi target. The Al peak results from the initial diffusion of Al atoms into the Si substrate. These atoms become incorporated into the growing SiGe layer during crystallization. Similar trends are observed for thicker layers (C).

3.2. Metal/a-Ge thicknesses

The effects of the metal/a-Ge thickness are shown in Fig. 3(b-c). Thicker metal layers result in smaller grains and a lower (100)-oriented fraction, particularly for the AlSi target. As the metal thickness increases, the nucleation sites shift within the layer [7]. For layers thinner than 100 nm, Ge atoms reach the Si substrate interface and grow epitaxially [7,16]. At higher thicknesses, nucleation also occurs at the Al/a-Ge interface and along metal grain boundaries, where specific orientations are energetically favored [7]. Thick Al layers promote (111) orientation (Fig. 3(c)). In contrast, thick AlSi layers exhibit no preferential orientation (Fig. 3(c)): reduced crystallinity and higher defect density of AlSi promote heterogeneous nucleation, resulting in a randomly oriented SiGe layer.

3.3. Diffusion control layer

Both the number and the average size of the Al-rich regions increase progressively during annealing (Fig. 4(a)). In the early stages of the process, the upward displacement of Al is driven by the stress exerted by the growing SiGe crystals, which pushes the metal toward the surface and promotes the Al-rich site formation [17]. As crystallization proceeds, the stress-driven mechanism is paralleled by Al diffusion, which contributes to the lateral growth of these regions by feeding pre-existing sites. Introducing a diffusion barrier such as AlO_x hinders vertical transport, allowing Al to emerge only through localized defects or thinner areas in the oxide layer. As a result, fewer sites are formed. However, these expand more rapidly, as the Al diffusion is funneled through a limited number of sites. This explains the slower increase in number and faster lateral growth of Al-rich regions in samples with the AlO_x interlayer.

Introducing an AlO_x interlayer also affects the crystal quality of the final SiGe layer. This layer not only suppresses Al displacement but also limits Ge diffusion and subsequent nucleation [7]. Consequently, samples with AlO_x exhibit larger grains with a preferential (100) orientation; whereas samples without AlO_x show smaller and more randomly oriented grains. This effect is particularly evident for the AlSi target (Fig. 4(b-c)), where both diffusion and nucleation are enhanced.

3.4. Annealing temperature

Fig. 5 shows how the annealing temperature affects SiGe composition and crystal quality. Sample S150 was selected for the temperature study, as it achieved full coverage after 25 h annealing at all three temperatures. Both the Si content in the final layer and the Al concentration at the SiGe/Si interface increase with temperature (Fig. 5(a,b)). The Si increase arises from two sequential mechanisms: first, the reduction in the critical amorphous layer thickness required for the nucleation, which facilitates Si incorporation into the SiGe layer [18]; second, the enhanced atomic mobility at higher temperatures, which promotes Si diffusion from the substrate into the growing layer. The effects of annealing temperature are also visible at the SiGe/Si interface, which becomes less abrupt at lower temperatures due to slower layer exchange and limited atomic mobility. The Al profile follows a similar diffusion-driven behavior: lower temperatures limit Al diffusion in the substrate at the early stage of the AILE and slow its upward displacement during the process, resulting in a lower interfacial peak and a more graded profile.

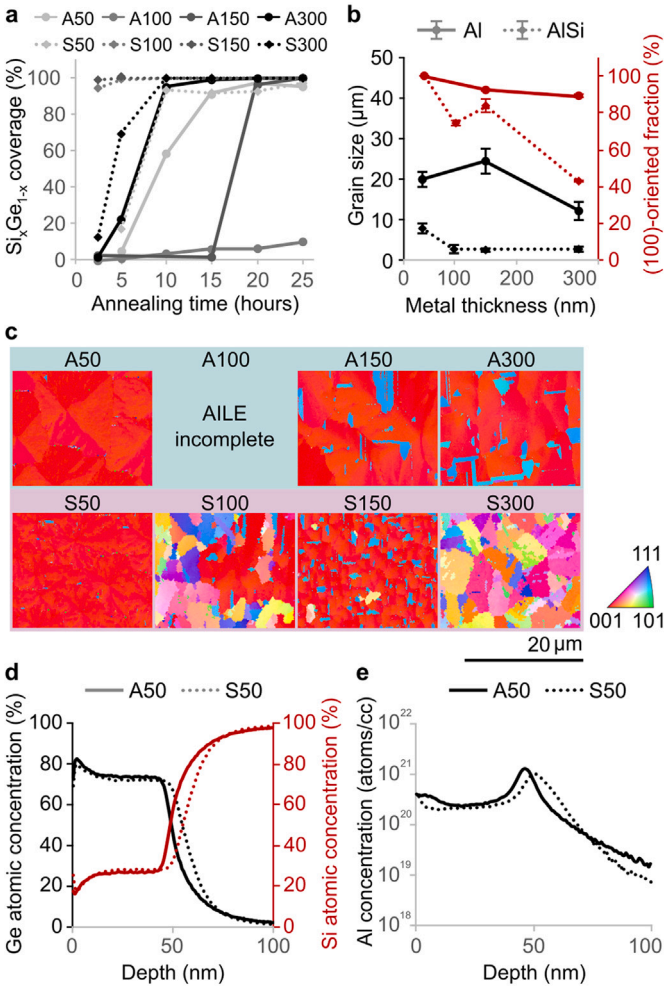

Fig. 3. Effects of metal composition and layer thicknesses. a SiGe coverage vs annealing time at 350 °C. **b** Grain size and (100)-oriented fraction of the SiGe layer vs metal thickness for samples without AlO_x after 25 h at 350 °C. **c** EBSD (IPF) maps after 25 h at 350 °C. **d** SIMS profile of A50 and S50 after 25 h at 350 °C. **e** SIMS Al concentration in A50 and S50 after 25 h at 350 °C and top Al etching.

Fig. 5(c)) shows that the crystal quality of the sample remains unaffected by temperature (Fig. 5(c)).

4. Process integration and application perspectives

The systematic investigation presented in this work provides practical guidelines for SiGe integration into silicon-based optical, electronic, and electromechanical devices.

In optical devices, grain size and crystallographic orientation play a critical role in determining optical losses and dark current, as grain boundaries act as scattering and recombination centers [19–21]. The ability to control grain size and orientation for different layer thicknesses through metal composition and interdiffusion layer enables optimization of the SiGe layer for waveguides and photodetectors, where

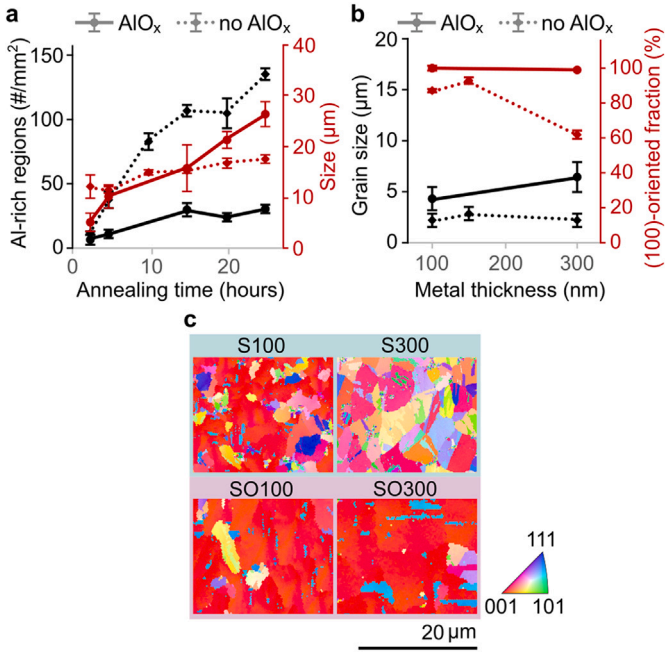

Fig. 4. Effects of AlO_x layer. **a** Density and size of Al-rich regions vs annealing time for A100 and AO100 at 325 °C. **b** Grain size and (100)-oriented fraction of the SiGe layer vs AlSi thickness after 25 h at 325 °C. **c** EBSD (IPF) maps of S100, SO100, S300, and SO300 after 25 h at 325 °C and top Al etching.

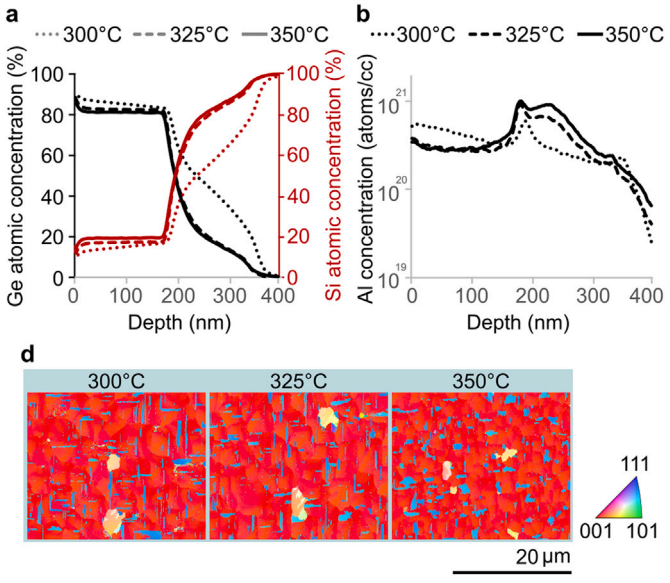

Fig. 5. Effects of annealing temperature. **a** SIMS profile of sample S150 after 25 h at 300, 325, and 350 °C. **b** SIMS Al concentration in the SiGe layer of sample S150 after 25 h at 300, 325, and 350 °C and top Al etching. **c** EBSD (IPF) maps of sample S150 after 25 h at 300, 325, and 350 °C and top Al etching.

larger grains and epitaxial layers are desirable [20,22]. The layer composition is also a key parameter for optical integration. The SIMS profiles reveal that the diffusion of both Al and Ge atoms can be modulated, albeit within certain limits. Although high doping levels reduce carrier mobility, degrading optical performance [20], metal doping can be used to create deep-level traps, allowing absorption below the bandgap [23]. Furthermore, lower annealing temperatures limit Al diffusion and create graded Al profiles, which generate enhanced internal electric fields, reducing surface minority carrier recombination [24]. Similarly, reduced annealing temperatures enable control over Ge diffusion at the SiGe/Si interface and allow for graded SiGe profiles, advantageous when fewer interface defects and high interface absorption are required [25,26].

For electronic applications, the ability to tune both grain size and doping distribution is equally critical. Larger grains reduce carrier scattering at grain boundaries, enhancing mobility [19,21]; whereas a controlled Al profile can be advantageous to improve carrier injection and collection. Indeed, compared to conventionally grown SiGe layers, AILE-grown SiGe inherently contains a high amount of Al. Previous studies on AILE show that about 10 % of the Al atoms in the layer are electrically active, resulting in typical p-type carrier concentrations ranging from 10^{18} to 10^{20} cm^{-3} [24,27]. Although such high doping levels might limit the use of these layers as channel materials in conventional CMOS transistors, they can be advantageous for other device functionalities. In particular, the Al distribution can be optimized to achieve a graded profile across the layer thickness, effectively reducing the contact barrier and facilitating charge transfer in metal/SiGe contacts [28,29]. Furthermore, AILE-grown SiGe is especially attractive for highly doped active regions, such as source and drain for three-dimensional integrated circuits [30].

In electromechanical applications, controllable grain size and composition are advantageous for both piezoresistive and capacitive sensors. In piezoresistive devices, larger grains and lower doping concentrations increase the gauge factor, resulting in improved strain sensitivity [5,31,32]. Furthermore, the presence of grain boundaries in AILE-grown films further enhances the strain response [33,34]. In capacitive devices, the composition of the SiGe layers and the resulting mechanical properties play a key role in determining sensor sensitivity [5,35].

From a process-integration perspective, the low thermal budget of AILE is fully compatible with BEOL and post-processing constraints, enabling above-IC integration of SiGe layers. Although longer annealing times are often required, the process relies exclusively on scalable, cost-effective steps such as sputtering and furnace annealing. In industrial manufacturing, batch furnace processing enables the simultaneous annealing of multiple wafers, mitigating the impact of long annealing times in high-volume production. This makes AILE attractive for industrial implementation, especially in applications where thermal budget and substrate compatibility are more critical than throughput. In addition, process parameters, such as the use of an AlSi target, can be adjusted to accelerate layer exchange when shorter processing times are required, albeit with reduced crystal quality.

Overall, the correlations established between process parameters and SiGe properties enable rational design of the AILE process, allowing the SiGe layer to be engineered according to specific optical, electronic, and electromechanical requirements.

5. Conclusion

This work establishes direct relationships between process parameters and the resulting SiGe properties. The demonstrated control over composition and crystallinity enables the rational design of high-quality SiGe layers suitable for low-temperature integration. These findings provide a versatile framework for optimizing AILE toward next-generation electronic and optical sensors.

CRediT authorship contribution statement

Lucia Crocetto: Writing – review & editing, Writing – original draft, Visualization, Validation, Methodology, Investigation, Formal analysis, Data curation, Conceptualization. **Poonam Devi:** Methodology, Investigation. **Vidharshana Sivakumar:** Formal analysis, Data

curation. **Francesco Stallone:** Resources, Methodology, Conceptualization. **Hande Aydogmus-Sasse:** Resources, Methodology, Conceptualization. **Sandra K. Raveendran:** Supervision, Conceptualization. **Padmakumar R. Rao:** Writing – review & editing, Supervision, Resources, Project administration, Methodology, Funding acquisition, Conceptualization.

Declaration of competing interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests: Lucia Crocetto reports financial support was provided by Top Consortia for Knowledge and Innovation. Lucia Crocetto reports financial support, administrative support, and equipment, drugs, or supplies were provided by ASML Netherlands BV. Lucia Crocetto reports financial support, administrative support, and equipment, drugs, or supplies were provided by Ommatidia LiDAR. Padmakumar Rao reports a relationship with ASML Netherlands BV that includes: employment, equity or stocks, and travel reimbursement. Lucia Crocetto has patent pending to ASML BV and TU Delft. ASML made an internal review through their technical publication board (TPB) for IP screening of this submission. This did not have any effects on the data or the conclusion or of the study itself. If there are other authors, they declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Appendix A. Neural network methods

SEM images contain visual information related to nucleation site growth that can be extracted through image segmentation. Initial segmentation was performed using ImageJ; however, the required processing steps varied significantly between visually similar images, motivating the use of a neural network-based approach for consistent segmentation.

Ground-truth labels were generated using ImageJ for each fabrication batch. Each SEM image is a grayscale image of size 890×1280 pixels. Scale bars and embedded text were removed by cropping, and images were padded to form square inputs with side lengths divisible by 16. The final dataset consisted of 421 images, split into training, validation, and test sets using a 70–15–15 ratio. Data augmentation was applied during training, including random horizontal and vertical flips, rotations, brightness and contrast adjustments, and Gaussian blurring, with ten augmented variants generated per image. To account for underrepresented batch phenotypes, images from rare and super-rare batches were oversampled by factors of three and six, respectively.

A standard U-Net architecture was employed, consisting of four down-sampling blocks with double convolution and max pooling. A final double convolution was applied at the bottleneck, followed by dropout with probability 0.5 for regularization. The decoder path consisted of transposed convolutions and skip connections, producing a binary segmentation mask at the output.

Model training used a weighted combination of Dice loss and binary cross-entropy loss with weights of 0.35 and 0.65, respectively, chosen empirically. Training was performed for 50 epochs with an initial learning rate of 1×10^{-5}, reduced by a factor of 10 when validation loss plateaued for at least three epochs. Final training and validation losses are reported in 2.

Table 2
Performance metrics comparing the two models.

Variable	$model_B$	$model_f$
Final training loss	0.0234	0.036
Validation dice $\pm \sigma$	0.1509 ± 0.2753	0.1251 ± 0.1229
Validation BCE $\pm \sigma$	0.3267 ± 0.9634	0.0223 ± 0.0233
Test dice $\pm \sigma$	0.2310 ± 0.3340	0.1200 ± 0.1052
Test BCE $\pm \sigma$	0.5273 ± 1.2182	0.0228 ± 0.0230
Validation global dice	0.482	0.0361
Test global dice	0.6214	0.0415

Table 3
Samples annealed at 300 °C with corresponding total annealing time and final average coverage of the SiGe layer.

Sample	Annealing time (h)	SiGe coverage (%)
A50[a]	–	–
A100[a]	–	–
A150	50	1.27 ± 0.68
A300	100	3.46 ± 0.42
AO50	75	1.89 ± 0.29
AO100[a]	–	–
AO300[a]	–	–
S50	75	0.06 ± 0.09
S100	100	97.71 ± 2.67
S150	50	99.05 ± 0.57
S300	100	60.09 ± 3.11
SO50[a]	–	–
SO100	100	98.14 ± 0.59
SO300	100	99.06 ± 0.21

[a] Not annealed at 300 °C; poor coverage already observed at 325 °C.

Table 4
Samples annealed at 325 °C with corresponding total annealing time and final average coverage of the SiGe layer.

Sample	Annealing time (h)	SiGe coverage (%)
A50	100	13.7 ± 4.8
A100	25	1.12 ± 0.36
A150	100	96.5 ± 2.4
A300	75	97.74 ± 0.10
AO50	100	98.1 ± 1.7
AO100	25	0.0 ± 0.0
AO300	25	0.0 ± 0.0
S50	100	84.49 ± 0.26
S100	25	98.68 ± 0.21
S150	25	99.83 ± 0.04
S300	50	100.0 ± 0.0
SO50	100	19.0 ± 3.1
SO100	25	99.64 ± 0.31
SO300	25	99.26 ± 0.82

The resulting segmentation masks were used for downstream analysis using the scikit-image library to identify connected regions and extract relevant physical properties. Training data, model code, post-processing scripts as well as an internal report detailing implementation in its entirety are available upon request.

Appendix B. Annealing time and SiGe coverage

Tables 3, 4, and 5 report the total annealing time and the corresponding SiGe average coverage for each processed sample at annealing temperatures of 300, 325, and 350 °C, respectively.

Appendix C. SiGe composition of thicker samples

Fig. 6 shows SIMS compositional profiles of samples A150 and S150 after 25 h annealing at 350 °C. As observed for thinner layers, the Si atoms in the metal target slightly increase the Si content in the final SiGe layer.

Table 5
Samples annealed at 350 °C with corresponding total annealing time and final average coverage of the SiGe layer.

Sample	Annealing time (h)	SiGe coverage (%)
A50	25	98.58 ± 0.42
A100	25	6.39 ± 0.88
A150	25	99.76 ± 0.12
A300	25	99.88 ± 0.02
AO50	25	94.6 ± 4.1
AO100	25	8.9 ± 2.9
AO300	25	69.3 ± 3.1
S50	25	96.8 ± 3.3
S100	25	99.76 ± 0.23
S150	25	100.0 ± 0.0
S300	25	99.99 ± 0.01
SO50	25	86.9 ± 6.4
SO100	25	99.97 ± 0.03
SO300	25	100.0 ± 0.0

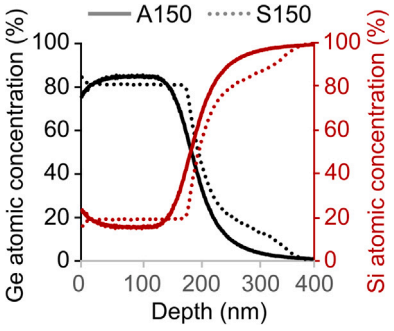

Fig. 6. Effects of metal composition. a SIMS profile of A150 and S150 after 25 h at 350 °C.

Data availability

Data will be made available on request.

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