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Performance and surge capacity evaluations of 1.2kV SiC VDMOSFETs with varied JFET width☆

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ABSTRACT

The 1.2 kV SiC VDMOSFETs with varied JFET width (L_{JFET}) are designed and fabricated in this study. The static and dynamic characteristics of each design are measured and compared. There is the best trade-off performance in the design of L_{JFET} = 1.8 μm according to FOM (BV^2/R_{on}) and FOM (C_{iss}/C_{rss}). Besides, the surge capacity and evaluation for series designs are investigated under conditions of V_{gs} = 0 V and V_{gs} = −5 V. There is a best surge capacity in design of L_{JFET}=1.2 μm, and the largest surge energy is the design of L_{JFET}=2.0 μm. Further, the surge failure mechanisms of L_{JFET} = 1.2 μm, 1.8 μm, and 2.0 μm under condition of V_{gs} = −5 V are investigated by decapsulated and FIB. Besides, the TCAD simulation was employed to theoretical analysis. The results show that the extremely high temperature was generated instantaneously under surge condition, resulting in epoxy carbonization, polysilicon melting and ILD oxide crack in failed position. Besides, the surge dissipating energy causes an instantaneous high temperature on the entire chip, resulting in aluminum remetallization. This paper would provide suggestions for device design and surge study.

1. Introduction

Silicon carbide metal-oxide-semiconductor field-effect transistors (SiC MOSFETs) is one of the most promising candidates for replacing silicon-based insulated gate bipolar transistors (Si IGBTs). These SiC MOSFETs can offer several advantages, such as fast switching frequency, low dissipating power, high thermal conductivity, and low leakage current [1–3]. The exceptional properties of SiC MOSFETs make them a promising candidate for use in power systems, such as electric vehicles, charging stations, and photovoltaic inverters [4]. In these years, the advent of innovative design and fabrication technology has facilitated the commercialisation of SiC MOSFETs in the power electronics market [5–7].

Surge capability is a critical performance that describes the ability of power devices to withstand extreme operating conditions [8]. The SiC MOSFETs with superior surge capability are critically important in power systems, as they can provide a greater safety margin for operational reliability. In these years, the SiC MOSFETs with planar gate structure (simplified SiC VDMOSFET) and trench gate structure (simplified SiC UMOSFET) are developed. Numerous studies have investigated their surge reliability and failure mechanisms. For example, Zhan et al. studied surge failure mechanism of body diode in 1200 V SiC VDMOSFET and UMOSFET, showing that the surge capability of SiC UMOSFET is inferior compared with SiC VDMOSFET [9]. JFET width, abbreviated as L_{JFET}, is one of the most important geometric parameters in reliability and characteristics for SiC VDMOSFET. However, it is

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worth noting that no work has yet been done to investigate the effect of L_{JFET} on the surge reliability of SiC VDMOSFETs. In this study, the 1.2 kV SiC VDMOSFETs with different L_{JFET} are designed and manufactured. The static properties and dynamic characteristics are analyzed. In addition, surge reliability and failure mechanisms are also investigated by experiment and physical simulation.

2. Device structure and fabrication

The 1.2 kV SiC VDMOSFETs with various L_{JFET} (1.2 μm, 1.4 μm, 1.6 μm, 1.8 μm, 2.0 μm) are designed and fabricated. In order to guarantee the uniformity of the fabricated process parameters, a multi-product wafer (MPW) design is employed with the same chip size which is 4 mm^2 including scribing region, the terminal area, and the active area. The scribing region and the terminal area are the same for all designs. Fig. 1(a) shows the cross section of critical geometric structure in SiC VDMOSFETs, including the JFET, P-Based, gate oxide, channel region, etc. The P-Based region width denoted $L_{P\text{-}Based}$ is equal to 2.6 μm. The thickness of gate oxide is 50 nm. The channel region width abbreviated as L_{ch} is 0.5 μm. The values of cell pitch are 6.4 μm, 6.6 μm, 6.8 μm, 7.0 μm, and 7.2 μm, corresponding to the L_{JFET} of 1.2 μm, 1.4 μm, 1.6 μm, 1.8 μm, 2.0 μm, respectively.

In this paper, the JFET density is a key parameter, which represents the ratio of JFET area to chip area, calculated by the following formula:

$$\rho_{JFET} = \frac{S_{JFET}}{S_{die}} \tag{1}$$

Where ρ_{JFET} is JFET density, S_{JFET} is JFET area. S_{die} is die area which is 4 mm^2 in this study. Similarly, P-Based density is defined as the ratio of P-Based area to the chip area.

In this study, the chip area of the SiC VDMOSFET comprises the scribe lane region, termination region, and active region. Across all designs, the scribe lane, termination region, and active region area remain constant. Consequently, variations in L_{JFET} reflect changes in the number of unit cells among different designs, as well as alterations in JFET density. Similarly, variations in P-Based density correspond to modifications in the number of unit cells within the chip. Fig. 1(b) displays the key stages for manufacturing process of SiC VDMOSFETs in this study. Firstly, a 6 inch N-type epitaxial wafer is cleaned, followed by etching of aligned marks. The hard mask is deposited and etched to generate ion implantation window. Then, P+ implantation is performed to construct P+ source region. P-Based implantation is performed to create P-Based region. Next, N+ source ion implantation is employed by using a self-aligned process via polysilicon deposition and etching. Light N-type implantation is performed in the active region to increase the dopant concentration of JFET region and adjust the threshold voltage. Following, the implanted ions are subjected to annealing and activation at 1700 °C for 30 min. A 50 nm thickness of gate oxide is formed through thermal oxidation. Polysilicon is then deposited and etched to construct the gate electrode. An isolated oxide layer (ILD) is subsequently formed on the polysilicon, and then it is etched between the gate and source. The gate and source contact is created and a thickness of 4 μm AlSiCu layer is deposited to generate electrode pad. A passivation layer is formed by utilizing nitride and polymide deposition. Finally, the SiC wafer is grinded from 350 μm to 180 μm. Laser annealing is used to activate the backside ohmic contact and the Ti/Ni/Ag alloy is performed to create drain electrode, meaning end of the fabrication process. The manufactured 1.2 kV SiC VDMOSFETs with varied JFET width are illustrated in Fig. 1(c).

3. Device characterization and third quadrant

The static characteristics of SiC MOSFETs with varied L_{JFET} are measured and shown in Fig. 2. The leakage current of SiC MOSFET increases with the increment of L_{JFET} when $V_{ds} > 900V$, as seen in Fig. 2 (a). Aa a result, the blocking voltage (BV) is decrease with the increment of L_{JFET}. Besides, the output characteristics, transfer characteristics, and the third quadrant characteristics for all designs are also measured. In order to compare the differences between varied L_{JFET} designs, their experimental results, including critical geometric parameters, static and dynamic performances are summarized in Table 1.

J_1.2 represents a L_{JFET} of 1.2 μm, and so on. The static characteristics including blocking voltage (BV), threshold voltage (V_{th}), specific on-resistance ($R_{on,sp}$), and third quadrant *I-V* characteristic (3rd V_F) are measured and calculated. Under the condition of $I_{ds} = 100$ μA, all the BV for varies L_{JFET} are 1647 V, 1644 V, 1626 V, 1575 V, and 1575 V, corresponding to 1.2 μm, 1.4 μm, 1.6 μm, 1.8 μm, and 2.0 μm respectively. The threshold voltages (V_{th}) are very close, which are range from 3.54 V to 3.60 V. The $R_{on,sp}$ is decrease with the increment of L_{JFET} in range of 1.2 μm–1.8 μm. There is a smallest $R_{on,sp}$ in J_1.8. The reason is that as the L_{JFET} increases, the number of cells in the chip decreases, and the number of channel resistance increases more significantly than the JFET resistance decreases. As a result, there is a larger $R_{on,sp}$ in J_2.0 than

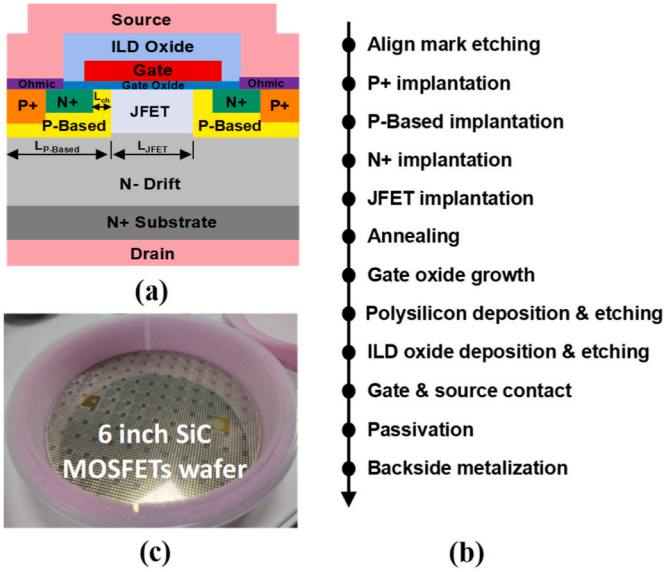

Fig. 1. (a) The cell cross section, (b) key stages for manufacturing process, (c) manufactured chip of SiC VDMOSFETs with varied JFET width.

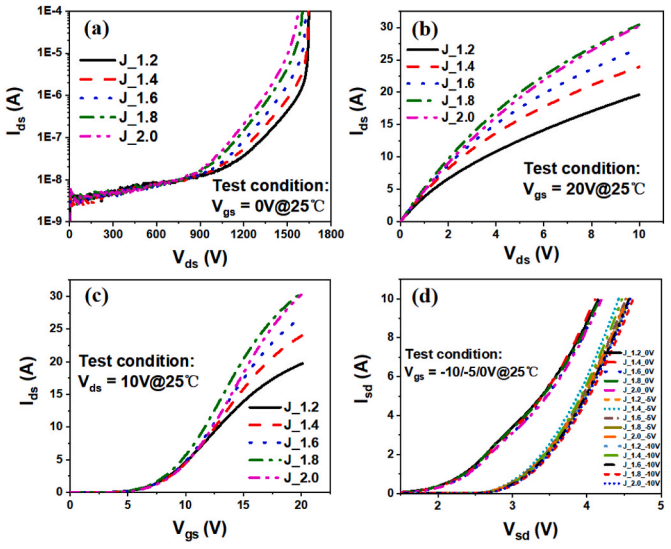

Fig. 2. (a) I_{ds} versus V_{ds}, (b) output characteristics, (c) transfer characteristics, and (d) the third quadrant characteristics of J_1.2 to J_2.0.

Table 1
Summary of experimental results.

Designs	J_1.2	J_1.4	J_1.6	J_1.8	J_2.0
JFET density	0.100	0.114	0.126	0.138	0.149
Pbase density	0.435	0.422	0.410	0.398	0.387
BV [V]	1647	1644	1626	1575	1575
V_{th} [V]	3.54	3.54	3.58	3.55	3.60
$R_{on,sp}$ [mΩ-cm^2]	13.56	9.96	9.11	8.15	8.84
3rd V_F (@8A) [V]	3.88	3.89	3.91	3.93	3.95
$C_{iss,sp}$(@V_{ds} = 800V) [nF/cm^2]	12.4	12.3	12.2	11.7	11.7
$C_{oss,sp}$ (@V_{ds} = 800V) [nF/cm^2]	495	493	494	493	493
$C_{rss,sp}$ (@V_{ds} = 800V) [pF/cm^2]	63.5	72.3	80.6	89.2	98.8
$Q_{gd,sp}$ [nC/cm^2]	388	392	396	413	466
FOM (BV^2/R_{on}) [V^2/mΩ-cm^2]	200045	271359	290217	304371	280614
HF-FOM ($R_{on} \times C_{rss}$) [mΩ-pF]	861	720	734	727	873
HF-FOM ($R_{on} \times Q_{gd}$) [mΩ-nC]	5261	3904	3608	3366	4119
FOM (C_{iss}/C_{rss})	195	170	151	131	118

*Note: J_1.2 represents L_{JFET} = 1.2 μm; BV@I_{ds} = 100 μA; $R_{on,sp}$@V_g = 20 V, I_{ds} = 9 A; 3rd V_F@V_{gs} = 0 V.

J_1.8.

The third quadrant I_{sd}-V_{sd} characteristic is very critical in studying surge performance.Fig. 2(d) shows the third quadrant I_{sd}-V_{sd} characteristics for all designs under different V_{gs} which are −10V/-5V/0V. There are almost identical I_{sd} under the conditions of V_{gs} = −5 V and V_{gs} = −10 V, meaning that the channel is completely shut off, with all the current from the source to the drain passing exclusively through the P-Based region. However, the channel is not fully shut off at V_{gs} = 0V. The I_{sd} for V_{gs} = 0 V is much larger than that of V_{gs} = −5/-10 V corresponding to the same V_{sd}. The channel is considered to be open. The channel current (I_{ch}) is calculated by using $I_{ch} = I_{sd0} - I_{sd1}$. For example, under condition of V_{gs} = 0 V and V_{gs} = −5 V, when the V_{sd} is 3.93 V, the I_{sd} is 8.0 A and 4.6 A in J_1.8. As a result, I_{ch} is 3.4 A, which cannot be neglected. During a surge process, the SiC VDMOSFETs were observed to operate within the third quadrant. However, different values of V_{gs} exert disparate effects in SiC MOSFET, which will be explored in subsequent sections.

The dynamic properties, including specific input capacitance ($C_{iss,sp}$), output capacitance ($C_{oss,sp}$), reverse capacitance ($C_{rss,sp}$), and gate charge ($Q_{gd,sp}$) are also evaluated. $C_{oss,sp}$ is found to be the same for all the designs due to equal die size. The $C_{rss,sp}$ increases linearly as L_{JFET} increases because of the linear increase in the overlap area between gate and drain. In addition, the figures of merit (FOM BV^2/R_{on}) is calculated. The largest value is observed at the J_1.8 design, which represents the best static performance trade-off between BV and R_{on}. The high frequency figures of merit (HF-FOM) are used to estimate the switching performance of SiC VDMOSFETs. There is the best HF-FOM ($R_{on} \times C_{rss}$) in the design of J_1.4, followed by J_1.8. Further, the devices with larger FOM (C_{iss}/C_{rss}) are presented desirable capacity to prevent shoot-through current during high-frequency operation. In this study, the FOM (C_{iss}/C_{rss}) are linearly decreased with the increment of L_{JFET} from 1.2 μm to 2.0 μm. In summary, the L_{JFET} with a length of 1.8 μm exhibits excellent trade-off performance in both static and dynamic properties.

4. Surge test setup

The surge test circuit diagram is shown in Fig. 3(a), in which a sinusoidal surge current pulse is generated and applied to DUT. The DC power supply charges the capacitor to store specific energy that dissipates during the surge test. The V_{gs} is generated by low voltage power supply providing specific voltage applied between gate and source. The capacitor (C) and inductor (L) are determined by the surge procedure time. In this study, the surge pulse duration is 10 ms, with C = 10.9 mF, L = 1 mH. During a surge test, the switch makes contact with point a and DC charges the C. Next, the switch contacts with point b and the C and L generate a 10 ms half-sinusoidal current passing through the DUT. The device operates in surge test. The waveforms of surge current and voltage are shown in Fig. 3(b). Additionally, the surge energy (E_{surge}) is

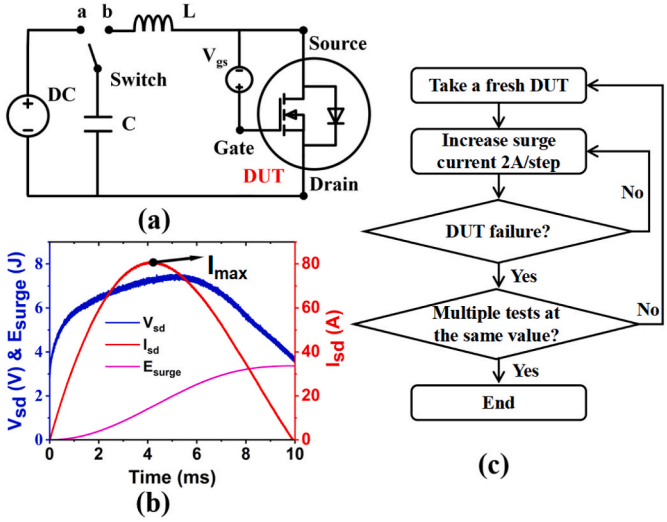

Fig. 3. (a) Surge test circuit diagram, (b) V_{sd}, I_{sd} and E_{surge} curves, (c) surge test experimental procedure.

also calculated, which presents the total energy dissipated during surge test. The calculated formula as following:

$$E_{surge} = \int_{t1}^{t2} I_{sd}(t) \cdot V_{sd}(t)\, dt \tag{2}$$

Where $I_{sd}(t)$ is the surge current during surge test and $V_{sd}(t)$ is the forward voltage drop. The t1 and t2 represent the moments of the surge test start and end, respectively.

Further, the surge capability (Cap_{surge}) is one of the most important parameters used to characterize the capacity of DUT to withstand surge current [9], which is used to evaluate the multiple of the maximum surge current to the rated current. It can be evaluated by following formula:

$$Cap_{surge} = \frac{I_{max}}{I_{rated}} \tag{3}$$

Where I_{max} presents the maximum surge current before failure, as shown in Fig. 3(b), and I_{rated} is the rated current of the device. In this paper, the I_{rated} for different designs can be measured under condition of V_{gs} = 20 V, V_{ds} = 10 V in transfer characteristic, which are 19.6 A, 23.9 A, 26.7 A, 30.4 A, and 30.2 A, corresponding to L_{JFET} of 1.2 μm, 1.4 μm, 1.6 μm, 1.8 μm, and 2.0 μm, respectively.

In order to more accurately evaluate the surge capability and surge energy of the device, the surge test process is shown in Fig. 3(c). First of

all, a fresh DUT is took to tested with a initial surge current test. Then, the surge current is increased in 2 A/step increments until the occurrence of a surge current exceeding the operational capacity of DUT resulting the DUT failure. During surge test, all the electrical characteristics are measured including V_{gs}, I_{sd}, and V_{sd}. Additionally, the test is finished until 3 times tests occurred with the same value for the same design of devices.

5. Surge evaluating results and discussion

The results of the surge test experiments under conditions of $V_{gs} = 0$ V and $V_{gs} = -5$ V at room temperatures (25 °C) are summarized in Table 2. Similar values of $I_{max,0V}$ are shown in J_1.2 and J_1.4. However, under condition of $V_{gs} = 0$ V, the I_{max} increase as the L_{JFET} increases from 1.4 μm to 2.0 μm. The difference between the minimum and maximum I_{max} values is 3 A. The surge energy was also calculated according to formulas (2), and the results are also listed in Table 2. $E_{surge,0V}$ represents surge energy at failure under condition of $V_{gs} = 0$ V. The maximum $E_{surge,0V}$ is located at J_2.0 which is about 3.693 J, indicating that the J_2.0 was subjected to the most substantial energy release during the surge test. This is consistent with the observation that J_2.0 exhibits the greatest I_{max} at $V_{gs} = 0$ V. Furthermore, the surge capacity under $V_{gs} = 0$ V, simplified as $C_{apsurge,0V}$ are also calculated using formula (3). The results demonstrate that the $C_{apsurge,0V}$ exhibits a decline with an increase of JFET width in range of 1.0 μm–1.8 μm. And the J_1.8 exhibits the lowest $C_{apsurge,0V}$. Additionally, the DUTs of varying JFET widths exhibit a near-identical I_{max} at $V_{gs} = -5$ V, which are different with that of $V_{gs} = 0$ V. According to the above discussion, there is a channel current in the surge test at $V_{gs} = 0$ V, especially in larger L_{JFET} designs The I_{max} difference is mainly due to the existence of channel currents for varying L_{JFET} during surge test. The E_{surge} with different L_{JFET} designs are mainly depends on the current density during surge tests. For the same chip area, a higher current density contributed from channel current was conducted in a larger L_{JFET} design under $V_{gs} = 0$V, while that is equal for each design under $V_{gs} = -5$V. Besides, it can be observed that the $C_{apsurge,-5V}$ exhibits a gradual decline with an increase in JFET width from 1.2 μm to 1.8 μm. There are the smallest $C_{apsurge}$ in J_1.8 for both conditions of $V_{gs} = 0$ V and $V_{gs} = -5$ V, which is the opposite of static and dynamic properties.

In order to investigate the surge capacity of DUTs deeply, the surge waveform and trajectories of J_1.8 are presented under conditions of $V_{gs} = -5$ V and $V_{gs} = 0$ V, as shown in Fig. 4. The surge waveform is employed to illustrate the variation in the I_{sd} and V_{sd} over time as the peak surge current increases until the device failure. When the surge current is increased from 81 A to 85 A in 2 A/step under condition of $V_{gs} = 0$ V, the device fails, as shown in Fig. 4(a). The I_{max} is 85 A according to measured result. In the case of $V_{gs} = -5$ V, the I_{max} is 83 A. There is about 2.0 A channel current during the surge process when $V_{gs} = 0$V. Further, the V_{sd} is extracted during surge process. Notably, the maximum V_{sd} (V_{max}) position is subject to hysteresis compared with the moment of I_{max}. Under condition of $V_{gs} = 0$ V, the I_{max} corresponds to 4.2 ms, while the V_{max} corresponds to 5.6 ms. And the phenomenon is similar in the case of $V_{gs} = -5$ V. During surge process, there are two phases for the surge trajectories of DUT, the one is rising stage and the other is falling stage. As the power dissipation increases, the junction

Table 2
Summary of experimental results.

Designs		J_1.2	J_1.4	J_1.6	J_1.8	J_2.0
I_{rated} (A)		19.6	23.9	26.7	30.4	30.2
$V_{gs} = 0$ V	$I_{max,0V}$ (A)	83	83	84	85	86
	$E_{surge,0V}$ (J)	3.578	3.526	3.613	3.654	3.693
	$Cap_{surge,0V}$	4.23	3.47	3.15	2.80	2.85
$V_{gs} = -5$ V	$I_{max,-5V}$ (A)	83	83	83	83	83
	$E_{surge,-5V}$ (J)	3.597	3.580	3.611	3.592	3.620
	$Cap_{surge,-5V}$	4.23	3.47	3.11	2.73	2.75

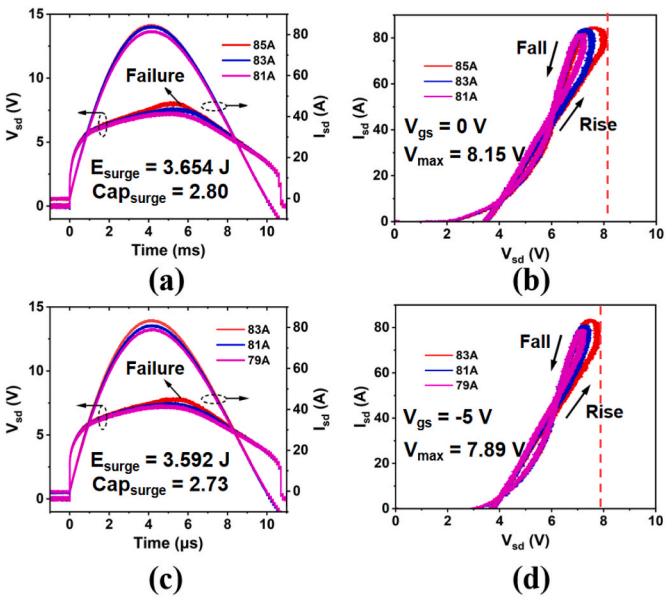

Fig. 4. (a) Surge waveforms, and (b) trajectories at $V_{gs} = 0$ V. (c) Surge waveforms, and (d) trajectories at $V_{gs} = -5$ V. DUT is J_1.8.

temperature is raised due to heat generation. The barrier of PN junction is decreased with the increment of junction temperature, and minority carrier lifetime gets higher, reducing transient resistance until it drops zero or even becomes negative. At high current, the resistive voltage that is equal to device resistance multiplied by the current. In the falling stage, since surge current initiates a decline, however, the junction temperature remains higher compared to the rising stage, further reducing the resistivity of chip due to strengthened conductance modulation. As a result, the body resistance during falling phase is smaller than that in rising phase at the same V_{sd}, contributing to voltage hysteresis. Further, the surge trajectories are also investigated, which represent the current-voltage curves under conditions of surge. As shown in Fig. 4(b), all tests exhibit a counterclockwise loop in their surge trajectories under condition of $V_{gs} = 0$ V. However, in the case of surge failure, there is a slight edge shape in I_{sd}-V_{sd} curve. The V_{max} is about 8.15 V in failed moment, while the V_{max} is about 7.89 V under condition of $V_{gs} = -5$ V. In the occurrence of a surge current exceeding the operational capacity of DUT, the device will fail, resulting in a short circuit between the gate and source and drain terminals.

Further, the surge waveforms of J_1.2 and J_2.0 under conditions of $V_{gs} = 0$V and $V_{gs} = -5$V are extracted, which are shown in Fig. 5. Clearly, the failure waveforms of these two designs are similar with that of J_1.8, indicating similar failure modes which would be suffered from transient heat dissipation and thermal shocked. For the J_1.2 design, the I_{max} is 83 A when $V_{gs} = 0$ V, and in the case of $V_{gs} = -5$ V, the I_{max} is 83 A, corresponding to the E_{surge} of 3.578 J and 3.597 J, respectively. Additionally, the I_{max} of J_2.0 is 86 An under condition of $V_{gs} = 0$ V, and the E_{surge_0V} is 3.693 J. In the case of $V_{gs} = -5$ V, the I_{max} is 83 A, corresponding to the E_{surge_-5V} of 3.620 J. As a results, there is about 3.0 A channel current in J_2.0 design during the surge process when $V_{gs} = 0$ V. However, the channel current is negligible in J_1.2 design. The reason may be larger resistance of JFET region in J_1.2 due to smaller JFET width compared to that of J_2.0. During surge process, the drop voltage of JFET region is larger than PN junction drop voltage, as a result that there is negligible current flow through channel.

According to the above discussion, the failure phenomena are similar for these designs. In order to further study the failure mechanism of these devices, the J_1.2, J_1.8 and J_2.0 after surge test failure at $V_{gs} = -5$ V are selected and analyzed by using optical microscope (OM) and scanning electron microscope (SEM). Firstly, the failed DUTs are

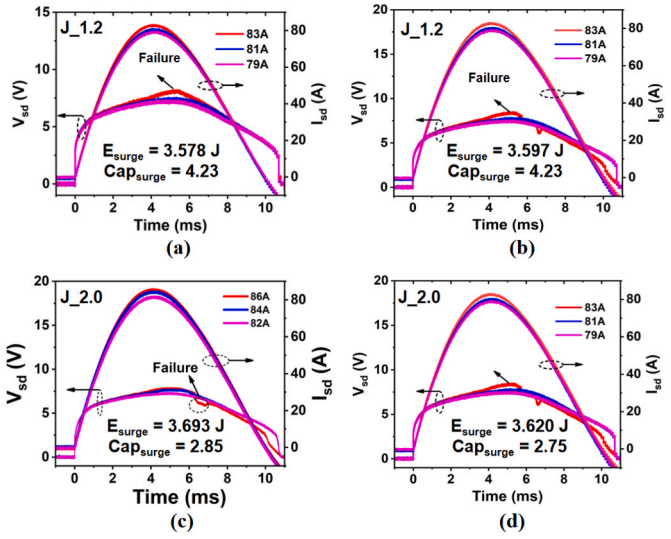

Fig. 5. Surge waveforms of J_1.2 under condition of (a) V_{gs} = 0V, and (b) V_{gs} = -5V. Surge waveforms of J_2.0 under condition of (c) V_{gs} = 0V, and (d) V_{gs} = -5V.

decapsulated and observed. Fig. 6(a)–(c) display the top views of J_1.2, J_2.0 and J_1.8 after decapsulation. Clearly, there are noticeable carbonization traces at burnt out positions in these three devices. Besides, a clear remetallization region around the bonding wires is seen in every failed devices. This suggests that the instantaneous heat generated during surge not only carbonized the molding compound, but also melted the source metal. In order to further investigate the location of the failure position, OBIRCH was used. Fig. 6(d) exhibits the thermal emission position of failed J_1.8. As can be seen, the location of thermal

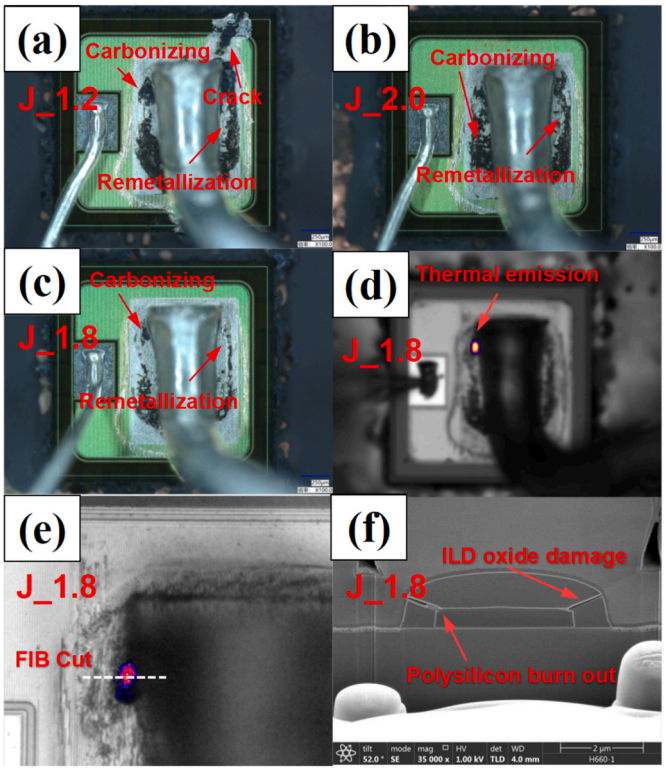

Fig. 6. Optical microscope images of (a) J_1.2, (b) J_2.0, and (c) J_1.8. (d) Failure position of thermal emission image in J_1.8, and (e) FIB cut location, and (f) SEM image.

emission is consistent with that of the carbonized position. This provides further evidence in the previous discussion. Furthermore, Focused-Ion Beam (FIB) was employed for the local cutting of thermal emission point, with the objective to conduct a more detailed failure analysis, as illustrated in Fig. 6(e). Clearly, there is a significant damage in failure cell, seeing in Fig. 6(f). The polysilicon was burned out and melted. The carbonization/melting/crack of the polysilicon is due to the heat energy accumulation which is from the surge energy dissipation caused the instantaneous high temperature in chip. The instantaneous high temperature during the surge process has exceeded the melting point of polysilicon (1410 °C). At the same time, the insulating oxide layer (ILD oxide) has also been damaged, and cracks were formed on both sides of gate polysilicon electrode. This indicates that the transient high temperature generated by the surge process causes extreme stress between the different materials, causing the oxide layer to crack. It is confirmed that J_1.8 experiences a great degree of temperature shock during surge test.

Under the condition of V_{gs} = −5 V, the surge current is mainly released through the body diode of SiC VDMOSFET. As the previous analysis that the failed mode in J_1.2, J_1.8, and J_2.0 are similar. In order to investigate the failure mechanism deeply, TCAD simulation is used to analyze the internal physical process in cell structure scale. In this study, the J_1.8 cell structure is constructed and simulated. Mixed-mode module in TCAD was applied and the simulated surge waveforms of voltage and current are calibrated under condition of V_{gs} = -5V, as shown in Fig. 7(a). There is a good match between experiment and simulation, indicating that the simulated results can basically qualitatively analyze the physical change in J_1.8 before surge failure. Further, the internal temperatures of J_1.2, J_1.8, and J_2.0 during surge processes are calculated according to the calibrated model. The results are shown in Fig. 7(b). Clearly, the internal temperature rises immediately after the start of the surge and all the temperatures of these devices are larger than the polysilicon melting point (1410 °C). Further, the current density distribution and the internal temperature distribution for J_1.8 at t = 6 ms are extracted, as shown in Fig. 7(c) and (d). Clearly, there is a high current density in N+ and P+ regions, since that all the surge current flow through the P-Based region from the N+ and P+ regions to the drift region undress condition of V_{gs} = -5V. As a result, the highest internal temperature is located at the N+ and P+ regions, which is 1433 °C. It can be inferred that the surge current passing through some cells is too large under surge condition, causing local extremely high

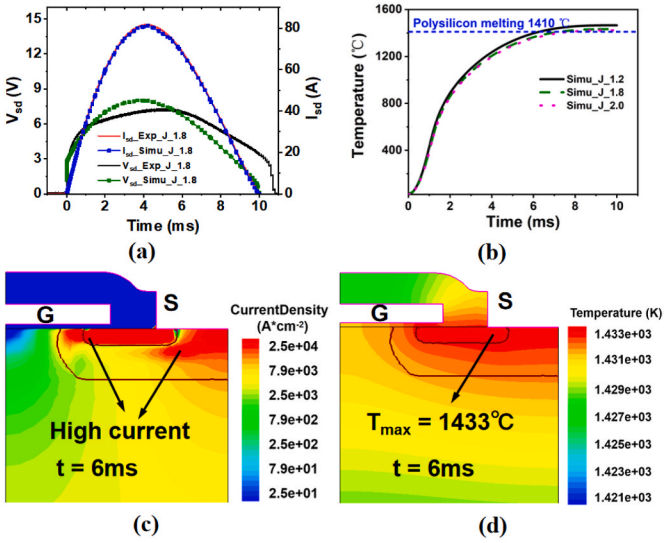

Fig. 7. (a) Simulated surge waveforms calibration. (b) Simulated temperature curves for J_1.2, J_1.8, and J_2.0. (c) Current density distribution and (d) internal temperature distribution for J_1.8 at 6 ms. V_{gs} = −5 V.

temperature, resulting in epoxy carbonization and polysilicon burnt out. Besides, such a high transient local temperature causes a very large stresses between different materials, resulting in ILD oxide crack and damage around the gate corner. At the same time, the surge dissipating energy causes an instantaneous high temperature on the entire chip, exceeding the melting point of aluminum, leading to remetallization.

6. Conclusion

The 1.2 kV SiC VDMOSFETs with varied L_{JFET} are designed and manufactured. The static properties, dynamic characteristics are tested and summarized. $L_{JFET} = 1.8$ μm exhibits more excellent trade-off performance according to FOM (BV^2/R_{on}) and FOM (C_{iss}/C_{rss}). Further, the surge capacity and evaluation for series designs were conducted under conditions of $V_{gs} = 0$ V and $V_{gs} = -5$ V. The J_1.2 has the best surge capacity, and J_2.0 has the best E_{surge}. Further, the surge waveforms of J_1.2, J_1.8, and J_2.0 are analyzed and discussed. The failed mechanism of these three designs under condition of $V_{gs} = -5$ V are investigated by decapsulated and FIB. Besides, the TCAD simulation was employed to theoretical analysis the internal physical change in J_1.8 during surge process. The carbonization/melting/crack of the polysilicon/SiO_2 is due to the heat energy accumulation which is from the surge energy dissipation caused the instantaneous high temperature in chip.

CRediT authorship contribution statement

Hou-Cai Luo: Writing – original draft, Investigation, Data curation. **Jing-Ping Zhang:** Investigation. **Ruo-nan Wang:** Data curation. **Huan Wu:** Data curation. **Bo-Feng Zheng:** Data curation. **Kai Zheng:** Data curation. **Guo-Qi Zhang:** Data curation. **Xian-Ping Chen:** Resources.

Declaration of competing interest

We would like to submit this paper to your journal **"Materials Science in Semiconductor Processing"** for publication. All co-authors have seen and agree with the contents of the manuscript and there is no financial interest to report. We certify that the paper has been neither copyrighted, classified, published, nor being considered for publication elsewhere. We are looking forward to favorable response from you.

Data availability

No data was used for the research described in the article.

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