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3.3 A Battery-Powered Hybrid Resonant Pulse-Train Generator with Adaptive Frequency Tracking and Residual Energy Recycling for Ultrasonic Implants

Xiayang Li*[1], Wenyu Peng*[1], Limitha Kumar[1], Xiaoxi Zhao[1], Cheng Huang[2], Sijun Du[1]

[1]Delft University of Technology, Delft, The Netherlands, [2]Iowa State University, Ames, IA
*Equally Credited Authors (ECAs)

Abstract

This work presents a battery-powered hybrid resonant pulse-train generator for ultrasonic wireless power transfer (US-WPT) in implantable medical devices. The ASIC integrates adaptive resonance tracking, burst-mode power regulation, a switched-capacitor–resonant architecture, and residual energy harvesting. Fabricated in 0.18µm BCD, it achieves programmable US power, 68.6% C_p-loss reduction, and 21.7% end-to-end efficiency.

Ultrasonic wireless power transfer (US-WPT) is an attractive solution for non-invasive energy delivery to miniaturized implantable medical devices (IMDs), thanks to its deep tissue penetration and excellent biocompatibility [1]. Delivering sufficient power at depths beyond 10mm requires large piezoelectric transducers (PZTs) driven by high-voltage (HV) pulse-trains to generate intense ultrasonic (US) bursts [2-3]. However, existing pulser designs face two critical challenges: (1) low efficiency under continuous HV pulsing due to repeated charging of the transducer capacitance, and (2) poor adaptability to different transducers or resonance drift caused by process and environmental variations. Most prior works target single-pulse excitation for imaging, leaving the need for an efficient, battery-powered HV transmitter (TX) for US-WPT largely unmet. Meanwhile, although many US-WPT receiver (RX) designs have recently been proposed [4-8], the lack of an adaptable and power-regulated transmitter highlights the urgent need for a new architecture that can sustain high-intensity pulse-train excitation while dynamically tracking transducer resonance and regulating the output power.

The core challenge of continuous HV pulsing arises from the intrinsic behavior of the PZT transducer, which can be modelled as a parallel capacitance (C_p) and a mechanical RLC branch [9]. While the mechanical current (I_m) dictates the acoustic output, significant dynamic loss occurs from repeatedly charging C_p, scaling with $f{\cdot}C_p{\cdot}V^2$. High efficiency is only achieved when the driving pulses are strictly aligned with the resonant frequency (f_r) and the voltage (V_{TX}) remains strictly in-phase with I_m. In practice, process variations, environmental factors, and packaging cause the actual f_r to drift, so fixed-frequency driving leads to power cancellation and efficiency degradation. Conventional class-D pulsers (Fig. 3.3.1 top-middle) provide simple continuous pulsing rely on a preset frequency and a dedicated HV rail (V_{HV}), suffering from low conversion efficiency and dynamic losses due to C_p hard-charging [10]. Resonant pulsers (Fig. 3.3.1, top-right) improve efficiency by leveraging resonant energy transfer, similar to a buck-boost converter, to generate half-sinusoidal HV pulses from a battery supply, reducing $f{\cdot}C_p{\cdot}V^2$ loss [11]. However, they only support discrete single-pulse generation and still depend on a preset pulse width, lacking adaptability to frequency drift and limiting their use as power TXs. These limitations call for a new architecture that unifies the advantages of both approaches: sustaining continuous pulse-train excitation for high US output, minimizing dynamic losses through resonant energy transfer, and adaptively tracking f_r to maintain efficiency under varying conditions.

To address these challenges, this work presents a hybrid resonant high-voltage pulse-train generator (Fig. 3.3.1, bottom). The proposed design introduces four key innovations: (1) adaptive resonance tracking, which detects and dynamically locks onto the actual resonant frequency of the PZT during operation, ensuring in-phase excitation and sustaining efficiency under process or environmental variations; (2) continuous burst-mode excitation with programmable power regulation, where both the pulse amplitude and pulse count can be tuned to maintain a desired output power level, unlike prior resonant pulsers limited to discrete single pulses; (3) a hybrid switched-capacitor (SC) resonant architecture, where the SC booster works with the resonant pulser to reduce conduction loss and deliver higher output power from a battery supply, enabling efficient drive of large PZTs; and (4) residual energy harvesting, where leftover mechanical energy is reclaimed after each burst and recycled to further enhance system efficiency. Together, these innovations enable a compact, battery-compatible pulse-train TX ASIC that provides efficient, adaptive, and power-scalable ultrasonic excitation for next-generation IMDs.

The operating principle of the ASIC is illustrated in Fig. 3.3.2. At the system level, the chip is controlled by two external digital signals: *EN* and *BU*. *EN* enables the ASIC, while *BU* defines the timing and duration of each US burst. By adjusting the frequency and pulse width of *BU*, different burst patterns can be flexibly programmed. Each burst consists of four modes: M_0 (Idle), M_1 (f_r Detecting), M_2 (Pulsing), and M_3 (Energy Harvesting). These modes correspond to different sequences of power stage configurations, or phases, shown in top-right corner of Fig. 3.3.2, with the associated configurations (Φ_0–Φ_3) detailed at the bottom.

The power stage integrates a PZT, a resonant pulser, and an SC booster, comprising three 5V switches (S_{C1}–S_{C3}), five HV Laterally Diffused MOS (LDMOS) switches (S_1-S_5), an inductor (L) and a flying capacitor (C). The hybrid SC-inductive topology boosts the input voltage of the resonant pulser to $2{\cdot}V_{BAT}$, shortening the inductor charging time and thus improves efficiency at the same output power. This faster charging also extends the applicable range of transducer frequencies, as higher-frequency PZTs allow less charging time per pulse. In Φ_0 (Open), PZT is left open to sustain its intrinsic resonance while C is charged by V_{BAT}. In Φ_1 (Inductive), V_{BAT} and C are stacked to energize L with $2{\cdot}V_{BAT}$ (solid path). The reverse current path (dotted) returns energy from L back to the battery when $I_L<0$. Meanwhile, S_5 grounds the PZT to enable zero-crossing detection ($I_m=0$), providing a reliable reference for cycle-accurate frequency tracking. In Φ_2 (Resonant), C is recharged by V_{BAT} while energy in L is transferred to the PZT (solid path). At the end of each pulse, the same configuration allows reverse transfer when $I_L<0$, with the inductor energized by the PZT. An "intense" variant of Φ_2 phase is implemented in M_2 to boost the delivered energy by turning on S_1 and S_4. In Φ_3 (Ground), the PZT is shorted to ground, preventing energy cancellation during the negative half-cycle of vibration.

The detailed burst operation is illustrated in Fig. 3.3.2 (top-right). When either *EN* or *BU* is low, the system stays in the low-power mode M_0. Once both signals go high, the system enters M_1, where a single half-sinusoidal pulse ($\Phi_1{\rightarrow}\Phi_2{\rightarrow}\Phi_1{\rightarrow}\Phi_3$) excites a weak vibration on the PZT, V_{TX}. By sensing the zero-crossing moments of V_{TX}, the resonant frequency f_r is estimated. The system then enters M_2, where continuous HV pulses are applied at the measured f_r. The sequence $\Phi_1{\rightarrow}\Phi_2{\rightarrow}\Phi_0{\rightarrow}\Phi_2{\rightarrow}\Phi_1{\rightarrow}\Phi_3$ extends each pulse width by holding V_{TX} at its peak during Φ_0, increasing the input energy per pulse. When *BU* goes low, the system transitions to M_3, in which the residual mechanical energy is harvested through the reverse sequence $\Phi_0{\rightarrow}\Phi_2{\rightarrow}\Phi_1{\rightarrow}\Phi_3$ and partially returned to the battery. The system then reverts to M_0.

The system architecture is shown in Fig. 3.3.3. It consists of a power stage, a sensor block, a digital controller, and on-chip clocking blocks. The sensor block includes two zero-crossing detectors (ZCDs) and a peak detector (PD) to monitor V_{TX} and V_R. The ZCDs provide timing information, while the PD identifies amplitude peaks; both signals are digitized for resonance estimation and real-time frequency tracking. A 100MHz on-chip voltage-controlled oscillator (VCO) and a time-to-digital converter (TDC) further quantify the resonance period. These sensing outputs are fed to a finite state machine (FSM), which coordinates the four operating modes (M_0–M_3), while a configuration controller sequences the power-stage configurations (Φ_0–Φ_3) based on the FSM commands and sensor feedback. As shown in Fig. 3.3.3 (top-right), the system applies HV pulses at resonance while maintaining phase alignment between V_{TX} and I_m to maximize energy transfer. The pulse amplitude is tuned by adjusting the inductor charging time T_C, thereby regulating acoustic output power. High-voltage switching is enabled by bootstrap drivers (Fig. 3.3.3, bottom-left), where a stacked capacitor C_{BS} provides gate overdrive for HV LDMOS devices, enabling efficient switching of S_1, S_4, and S_{C1}.

The prototype ASIC was fabricated in a 0.18µm BCD process with an active chip area of 4.92mm² (Fig. 3.3.7). Electrical measurements were first performed using a 1nF off-chip capacitor load, with a 0.68µH off-chip inductor for the resonant pulser and a 1µF off-chip capacitor for the SC booster (Fig. 3.3.4). Because a pure capacitor does not exhibit mechanical resonance, the operating frequency was externally provided by an FPGA. As shown in Fig. 3.3.4 (top-left), the chip achieves continuous pulse-train generation at 2MHz, where resonant power transfer enables soft-charging quasi-square pulses. The output amplitude is programmable from 5 to 25V; at 24.6V, the chip consumes 0.38W power and achieves a maximum C_p loss reduction of 68.6% (Fig. 3.3.5, bottom-left).

For ultrasonic evaluations, a 12×12×1.02mm³ PZT-5A transducer was used as the load, with its resonant frequency characterized at around 2.2MHz by an impedance analyzer. Driven by an external *BU* signal, the ASIC generates bursts with a 2kHz pulse repetition frequency (PRF) and 10% duty cycle (Fig. 3.3.4, top-right). A zoomed-in waveform of a single burst (Fig. 3.3.4, middle) demonstrates the full operation sequence, including f_r-detection (M_1), pulsing (M_2), and energy harvesting (M_3). The detailed waveforms for each mode are further shown in Fig. 3.3.4 (bottom). In M_1, after initialization by resetting the power stage, a single half-sinusoidal pulse is applied for zero-crossing detection to estimate f_r. In M_2, the measured pulse-train period is 456ns, confirming accurate resonance tracking at around 2.2MHz. In M_3, the residual mechanical energy is recycled, with the PZT's kinetic energy decaying rapidly.

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Figure 3.3.5 presents the acoustic measurement setup and results. Tests were conducted in a water tank using the same 12×12×1.02mm³ PZT transducer, while a fiber-optic hydrophone on a 3-axis stage scanned the acoustic field. At the focal depth of 13mm, the measured distribution (Fig. 3.3.5, top-right) shows a peak acoustic pressure of 0.392MPa at V_{TX} = 8.8V. Leveraging on-chip power regulation, the ASIC can program different output intensities, and the end-to-end (E2E) efficiency is obtained as the ratio of the received acoustic power at the focal spot to the electrical input power. The received acoustic power is evaluated by integrating the acoustic intensity over a 1mm² focal area, which corresponds to both the effective beam spot and the aperture size of practical implant receivers, providing a representative metric for E2E efficiency. As shown in Fig. 3.3.5 (bottom-right), the system achieves a peak E2E efficiency of 21.7%, which corresponds to a peak acoustic pressure of 0.392MPa at the focal spot. Compared to prior works (Fig. 3.3.6), the proposed ASIC shows higher efficiency under adaptive resonant pulse-train operation, while uniquely supporting output power regulation and residual energy harvesting, making it a promising US-WPT solution for IMDs.

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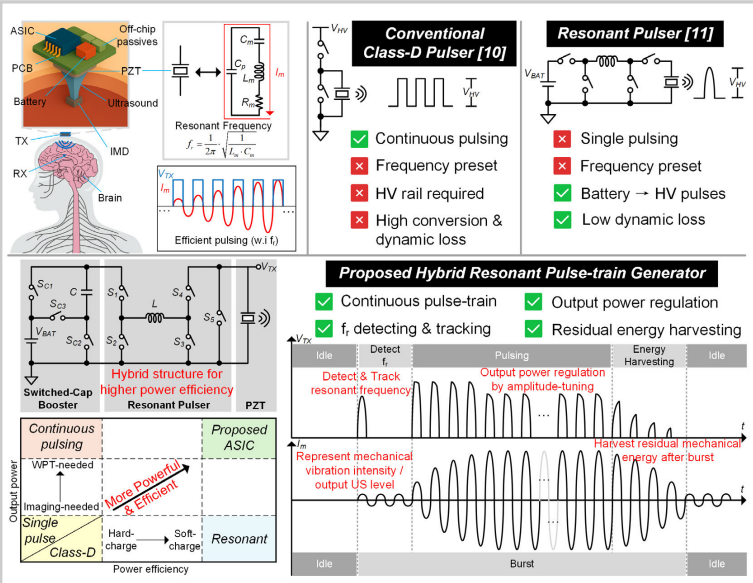


Figure 3.3.1: System concept and motivation of the proposed hybrid resonant pulse-train generator.

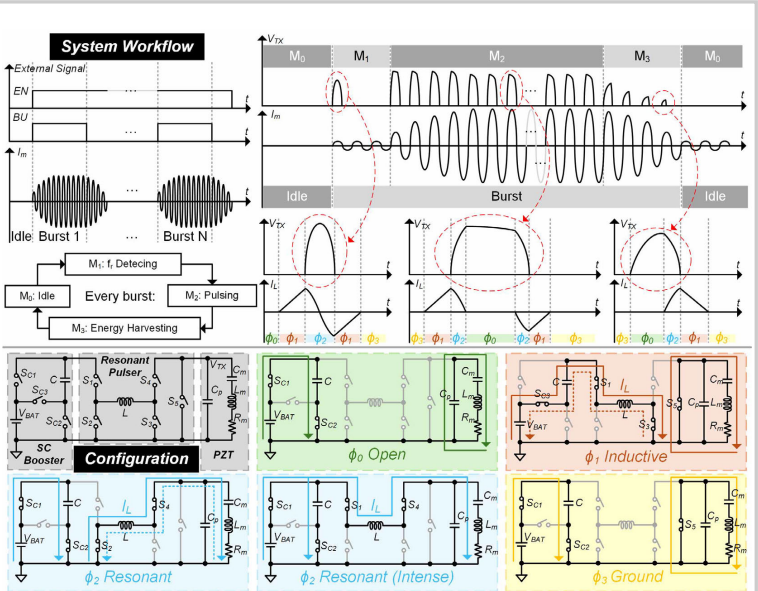


Figure 3.3.2: Operating principle and power-stage configurations of the proposed ASIC.

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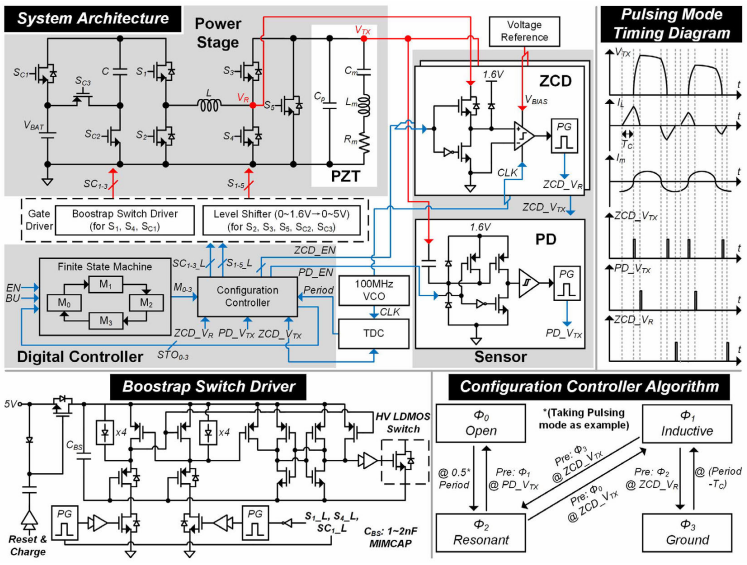


Figure 3.3.3: System architecture and circuit implementation of the proposed ASIC.

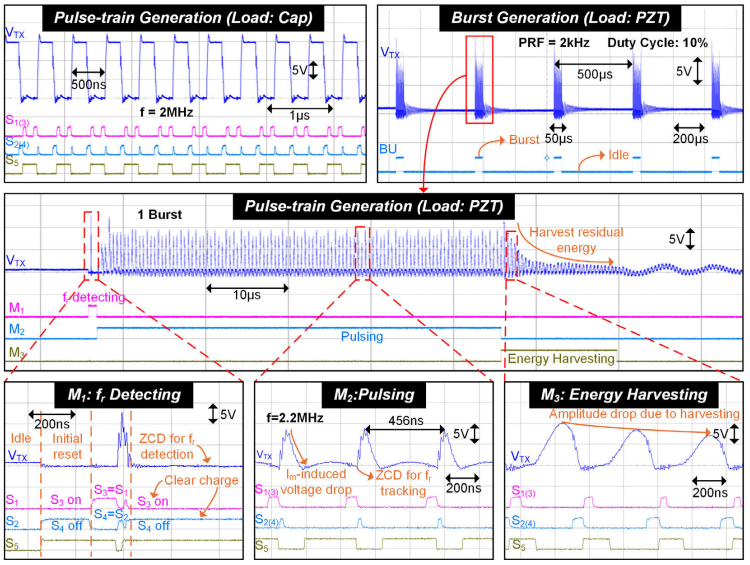


Figure 3.3.4: Electrical measurement results of both capacitor and PZT load.

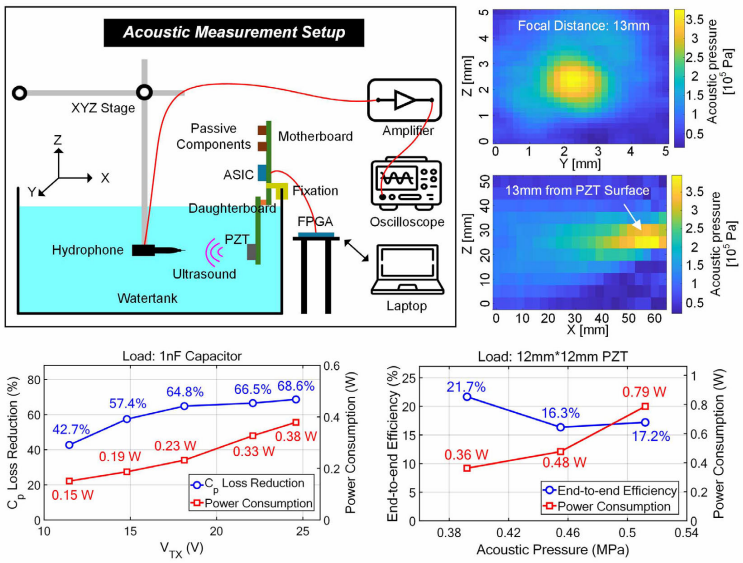


Figure 3.3.5: Acoustic measurement setup and results; C_p loss reduction and end-to-end efficiency analysis.

Comparison with State-of-the-art TX ASIC for Ultrasonic Applications

Reference	This work	Gourdouparis, ISSCC' 2024 [12]	So, JSSC' 2022 [13]	Costa, TbioCAS' 2021 [14]	Bellouki, ISSCC' 2024 [11]	Choi, ISSCC' 2021 [2]	Chen, JSSC' 2013 [15]
Application	Powering/Stimulation				Imaging		
Process	180nm BCD	65nm	180nm BCD	180nm	180nm BCD	180nm BCD	180nm BCD
Transducer	PZT	PMUT	PZT	PZT	CMUT	PZT	CMUT
Frequency	0.5-2.5MHz	7.8MHz	850kHz	8.4MHz	2.5MHz	1MHz	3.3MHz
f_r tracking	Yes	No	No	No	No	No	No
Driving voltage	5-25V (Adjustable)	4.8V	4.5V	5V	10-30V (Adjustable)	30V	30V
HV supply	Not Needed	No HV TX	External	No HV TX	Not Needed	External	External
Transducer load C_p	200pF-1.5nF	2.5pF	125pF	N/A	120pF	820pF	40pF
Measured C_p loss reduction	68.6%	46%	N/A	N/A	63%	73.1%	38%
Powering method	Pulse train generation	Beamforming	Beamforming	Beamforming	N/A		
Output power regulation	Yes	No	No	No	N/A		
Residual energy harvesting	Yes	No	No	No	N/A		
End-to-end efficiency	21.7%*	N/A	0.86%*	N/A	N/A	N/A	1%**

*Efficiency = Acoustic power @ focal spot / Electrical power from supply
**Efficiency = Acoustic power @ TX surface / Electrical power from supply

Figure 3.3.6: Comparison table of the proposed ASIC with prior state-of-the-art TX designs for ultrasonic applications.

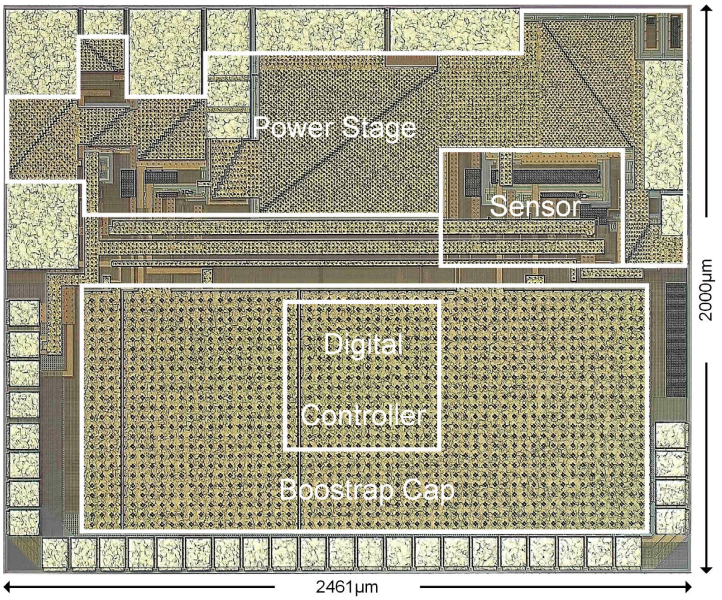


Figure 3.3.7: Chip micrograph.

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