Investigation of the inductor's parasitic capacitance in the high frequency switching of the high voltage cascode GaN HEMT

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Challenge the future

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Master of Science Thesis

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Abstract

The concept of the More Electric Aircraft, where the majority of the aircraft's secondary needs will be supplied by electrical power, is under continuous research over a number of years in order to conform the recent demand for more efficient and environmentally friendly aircrafts. Advancements in power electronics have contributed towards the realization of that demand, by introducing lightweight, high-power density and highly efficient in harsh environment power electronics. The increase in power density of power electronic systems was made feasible, so far, by developments in the semiconductors field, namely by semiconductors that can operate at higher switching frequencies and generate less power loss. Wide-bandgap devices, such as Gallium Nitride (GaN) transistors, have emerged as possible candidates to replace silicon and even silicon carbide devices in various power conversion applications offering potential benefits for high frequency power conversion due to their intrinsic material properties. Another step towards higher power densities is to utilize appropriate circuit topologies since they can reduce the stress upon the components and the cooling requirements. However, as the frequency goes up, the switching behavior of the device is not only influenced by the die itself and the device package's and circuit's parasitic elements can not be neglected any more. One of these parasitic elements is the the equivalent parasitic capacitance (EPC) of the magnetic component, which is part of almost every topology.

This thesis project aims at two things: first, to observe the switching behavior of a high-voltage cascode GaN High Electron Mobility Transistor (HEMT) under inductive clamped load condition, which is the same commutation mode for the power devices as switching in a PWM, hard-switching type converter and second, to investigate the influence of the magnetic component's EPC on the switching behavior of the GaN HEMT. For this, an analytical loss model of the device was developed and a double-pulse tester (DPT), which is considered to be a very good example of that load condition, was optimally designed and manufactured in order to verify the analytical model. Two pulses are launched to the device under test (DUT) and the switching transitions of the DUT can be captured for any desired current and voltage rating under hard-switching conditions. Moreover, when operating under that load conditions, applying active devices with reverse recovery charge has significant influence on the switching behavior of the DUT, so both cases will be examined. Finally, in order to characterize the device and eventually verify the analytical loss model, current and voltage measurements need to be taken during the turn-on and turn-off switching transitions. As the GaN HEMT is capable of switching are very high speed, there are issues and limitations that need to be taken into consideration in order to ensure the fidelity and the accuracy of these high frequency measurements.

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Chapter 1

Introduction

The trend of the More Electric Aircraft (MEA), where the majority of the aircraft's secondary needs are supplied by electrical power, is under continuous research over a number of years: the concept of an electric aircraft has been questioned since World War II [1–4]. Nevertheless, the lack of electric power generation capabilities along with the volume requirements of the power components laid the approach unfeasible. On the other hand, the rapidly developed hydraulic power systems were providing less complex systems, causing them to be adopted as the standard technology for secondary power. The recent demand for more efficient and environmentally friendly aircrafts along with the advances in power electronics and high power density electrical machines have opened up new opportunities leading the aerospace market to overcome its conservatism and renew the interest in MEA.

In this chapter a short description of the project's background will be given. In section 1.1 the basic concepts behind the realization of the MEA will be shortly described and the connection with the advancements in the area of power electronics will be made. Section 1.2 will introduce the principles behind power density increase and how the advancements in the semiconductor's field can contribute to it. Section 1.4 describes the thesis objective of this thesis project. Finally, section 1.5 gives the structure of this thesis.

1.1 More Electric Aircraft (MEA)

In conventional aircraft architectures most of the power, produced by fuel in the engines, is used as propulsive power to move the aircraft. The rest is extracted by the main engine with different principles and is converted into secondary power types in order to drive the non-propulsive aircraft systems [2], [3]:

- *Mechanical power*: obtained from the engine by means of mechanical gearboxes and used to drive hydraulic pumps, fuel pumps, lubrication pumps and electrical generators.
- *Pneumatic power*: extracted by the engine's bleeding compressor and used to power the Environmental Control System (ECS), cabin pressurization and the wing anti-icing system.

- *Hydraulic power*: obtained from the main hydraulic pump and used to drive primary and secondary flight control actuators, landing gear for deployment and braking and other ancillary systems.

- *Electrical power*: obtained from the main generator to drive subsystems like avionics, lighting, galleys and other commercial loads.

Through the years, each system has become more and more complex, so the manufactures can satisfy the increasing demands of the passengers for comfort and more facilities, resulting in reduction of the efficiency of the whole system. Moreover, these systems tended to be heavy, inefficient and required frequent maintenance, i.e. pneumatic and hydraulic systems have the drawback that a potential leakage of fluids is difficult to be detected and also not easily accessible. All these, along with the recent developments in the field of power electronic systems, fault-tolerant electric machines, electro-hydrostatic and electro-mechanical actuators have led the aerospace market towards the reduction/removal of the mechanical complexity and its replacement with electronics.

The concept of a More Electric Aircraft is based on using the electrical power for extracting and distributing these non-propulsive powers (see figure 1.1). Over the years a lot of research has been conducted regarding the benefits of an electric aircraft in the following areas [2]: *Flight Control Technology, Wing Technology, Engine Power Extraction, Flight Control Actuation, Advanced Electrical Power Systems*. Summarizing these studies, the technologies that can realize the MEA initiative can be summarized in the following four key concepts suggested by R. E. J. Quigley in [5]:

- *The engine Starter/Generator*: lightweight motors will be mounted directly on the main shaft (internal engine Starter/ Generator) allowing the elimination of the engine tower shaft and the accessory gearboxes will be replaced by electronic power converters. The starter/generator will be used to provide the aircraft electric power while it enables emergency power extraction under windmill conditions [6]. Elimination of the gearing and gear separation forces will also allow the integration of Advanced Magnetic Bearing (AMB) systems into the internal starter/generator leading to the removal of the engine oil system along with the lubrication systems.

- *Electric primary flight control actuation*: in conventional aircrafts the actuation system of the flight surfaces is realized by a centralized hydraulic system (hydraulic pumps, motors and actuators). In the current control technology, known as Fly-By-Wire (FBW), the flight control surfaces are being controlled electrically and activated hydraulically. A new control technology, known as Power-By-Wire (PBW), is examined for the concept of MEA and it aims at replacing the existing systems with electrical equivalent and using electromechanical actuators to control each surface in a de-centralized system [7, 8]. Advances in power electronics have led the FBW technology to its current stage, but further advances are needed in order for PBW to take over.

- *Integrated auxiliary/emergency Power Unit (IPU)*: electrically-driven compressors and other heating/cooling units will be used to provide cabin air conditioning, pressurization and other vital services eliminating many issues from the current mechanically-linked auxiliary power units. Consequently, a better cabin environment for the passengers will be provided along with reduction in fuel consumption.

Moreover, the elimination of the gearing will enable the use of AMB same as in the internal starter/generator.

- *A fault-tolerant Power Management And Distribution (PMAD) and motor drive system*: with ability to drive all the subsystems of the aircraft at most efficient power in order to match every load and cooling requirements. The PMAD system is constituted by power electronic converters and inverters while advancements in these areas will directly impact the viability and overall performance of the aircraft.

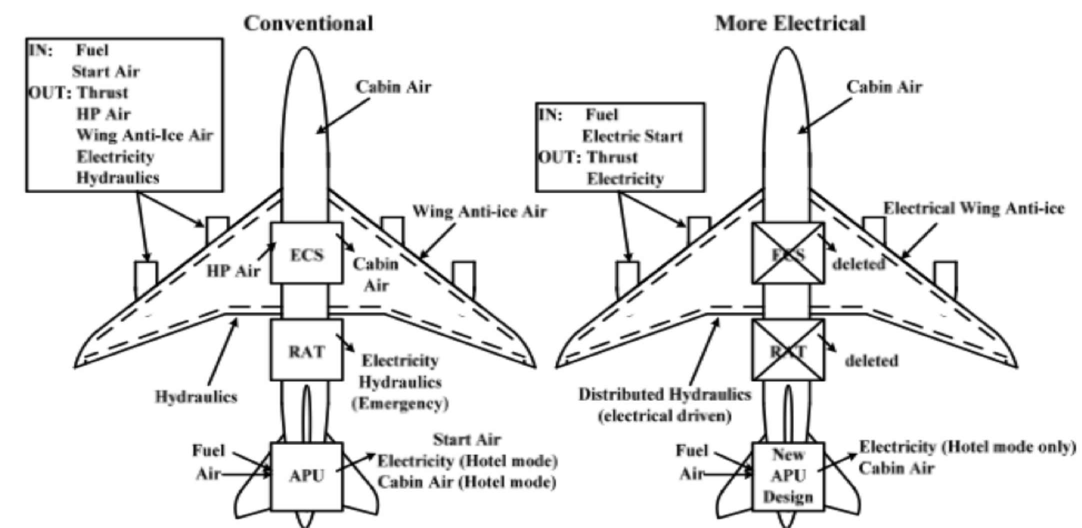


Figure 1.1: Comparison between conventional aircraft systems and MEA systems [6]

Conclusively, the electrical systems are expected to reduce the complexity, weight, operation costs and environmental impact while at the same time increase reliability, survivability and viability of the aircrafts by removing the hydraulic, mechanical and pneumatic systems. This change is also expected to have an effect upon the overall aircraft performance, since the concept addresses more energy-efficient ways of converting and utilizing aircraft power.

Looking at the four concepts listed above, it is easily observed that for the realization of each one of them, power electronics are of vital importance. Lightweight, high-power density and highly efficient in harsh environment power electronics are needed for conversion and control of the power over the distribution system of the aircraft [9–11]. However, increasing power density in power electronics modules is a complex issue and demands thorough investigation in many aspects in order to be optimized.

1.2 Power Density

There is a great desire in power conversion, during the past few years, for higher power density while maintaining the efficiency at high levels. For starters, Power Density [kw/liter], defined as the ratio of the converter output power and its volume, is the factor that defines the compactness of the converter design. Therefore, this desire is also characterized by the requirements for lower volume, lower weight and lower production costs. Since the inception of the power electronic converters, power density has increased linearly by

decade. Specifically, as it can be seen in figure 1.2 that the dc/dc converter power density increases by an order of magnitude per decade.

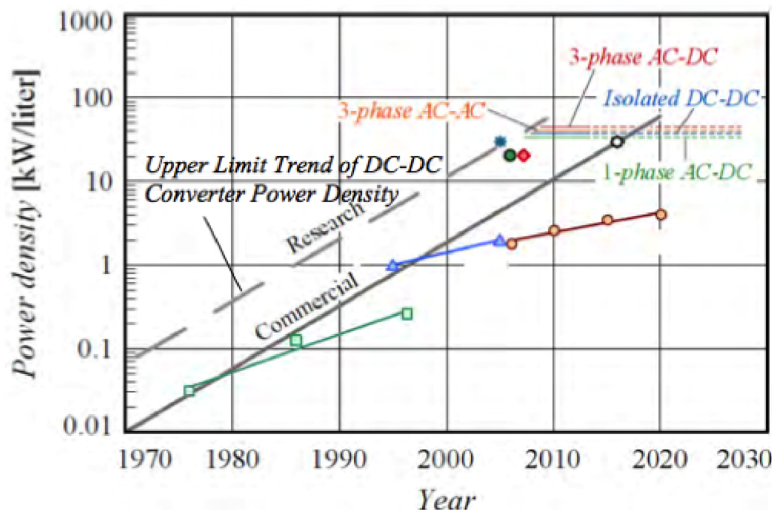


Figure 1.2: Power Density trends over the past few years [12]

The most important thing in achieving higher power densities is to understand the technological barriers that restrain this development. Therefore, the main elements that can affect the converters power density are named below:

- Power Semiconductor Modules
- Control Circuit
- Power Passive Components (filter components / transformers)
- Cooling System
- Interconnection / Packaging

The components that require the largest volume in the converter are the passive components such as capacitors, inductors, and transformers used for filtering, energy storage and cooling systems. The volume of these components is strongly related to the switching frequency of the converter. Moreover, the design of the capacitor and inductor depends on the topology of the dc/dc converter. As the switching frequency is increased, the volume of the inductor and capacitor decreases and so the overall power density increases. According to that, the increase in the power density has been achieved, so far, by increasing the switching frequency. Nonetheless, specific limitations occur at higher switching frequencies, as the switching losses of the semiconductors devices increase, proximity and core losses in the magnetic components also increase and problems occur due to parasitic inductances and capacitances of the circuit, which can no more be neglected.

Regarding the semiconductor devices, new wide-bandgap semiconductors, such silicon carbide (SiC) and gallium nitride (GaN), are being introduced over the past few years and they are considered possible candidates to replace silicon devices in many power conversion applications. GaN semiconductors present better material properties regarding the bandgap, electron mobility and electron saturation velocity than Si and SiC devices, which make them more suitable for higher frequencies and higher voltage operation. They

also have much smaller on-resistance resulting in extremely low conduction losses. Furthermore, these semiconductors have higher maximum operating junction temperatures. Consequently, since the volume of the cooling system is determined by the power loss of semiconductor power devices, by enabling reductions in losses and higher temperature operation, converter thermal management requirement can be decreased. However, utilizing these devices can not be achieved by simple replace them in the existing systems since they come with specific limitations and drawbacks:

- As the switching frequency goes up, the switching loss of device is not only influenced by the die itself, but also by the parasitic inductors of the device package and PCB layout. This, basically, puts a limit on high frequency operation and especially for hard switching operation. Device's junction capacitors also introduce significant switching loss and deteriorate the switching transition. Conclusively, soft switching technique is still critical for high-voltage GaN transistors in order to achieve high efficiency in high frequency operation [13].
- The much smaller surface of GaN devices results in changing the way the dissipated heat is being handled. Therefore, getting the heat out the GaN dies is much more challenging and spreading the heat over multiple sourced becomes necessary [14].

Another step towards higher power densities is to utilize appropriate circuit topologies since they can reduce the stress upon the components and the cooling requirements.

1.3 DC/DC Power Converters

Nowadays, dc/dc power converters mostly utilize the so called switch-mode conversion in order to convert a dc input into a controlled dc output with a desired voltage level. There are several dc/dc converter topologies, each one with different characteristics and advantages, giving the possibility to engineers to choose based on their needs. Part of every topology are the magnetic field storage components that can be used to store energy temporarily and release it later on according to the operation principles of each topology.

On the contrary, the same magnetic components will introduce limitations when higher power densities are pursued. For example, when the power converter is operating at high switching frequencies, the equivalent parasitic capacitance (EPC) of the magnetic component can no longer be neglected, as it can have significant impact on the switching behavior of the switches [15].

1.4 Thesis objective

This master thesis project is conducted in collaboration with Aeronamic B.V. in order to support the development of a high power density, high efficiency dc/dc power converter for aerospace application. The main objective is to evaluate the switching behavior of the high-voltage GaN HEMT in cascode configuration under hard-switching conditions and investigate the impact of the magnetic component's EPC on the switching performance of this device.

In order to achieve the objective stated above, there are a few research questions that have to be answered:

- How can the use of GaN devices contribute to the development of power electronics?
  - What are the advantages of these devices compared to previous ones and how can they improve the converter's performance?
  - What are the drawbacks/limitations that they have and what must be done in order to overcome them?
- Why do the parasitic elements of the circuit become more critical with the use of such devices?
  - How does the equivalent parasitic capacitance of the magnetic component influence the switching behavior of the power switches?

1.5 Thesis Layout

Based on the above objective, the thesis is organized as follows:

Chapter 2 introduces the theoretical background required during this thesis work. The principles of the dc/dc conversion are discussed along with topologies and techniques that can be used depending on the application. The concept of the power density is introduced and the reasons why the emergence of wide-bandgap semiconductors, such as silicon carbide (SiC) and gallium nitride (GaN), can contribute towards the increase of this concept are presented. Finally, the switching transitions of such devices is discussed.

Chapter 3 discusses an analytical loss model of the high voltage GaN HEMT in cascode configuration. The 600V GaN HEMT is tested under clamped inductive load conditions by a double-pulse tester (DPT) circuit. The contribution of the thesis begins in this chapter as the influence of the inductor's EPC on the switching behavior of the GaN HEMT is incorporated into the analytical model.

Chapter 4 presents issues that need to be taken into consideration when voltage and current measurements in high frequency power electronics applications are needed. Solving these issues can ensure the fidelity and the accuracy of the results. Moreover, different voltage and current measuring techniques are presented.

Chapter 5 investigates the influence of the inductor's EPC. Furthermore, it discusses the design and manufacturing of a DPT circuit in order to verify the results of the analytical model.

Chapter 6 gives the main conclusions of the thesis and recommendations for future research.

Chapter 2

High Frequency Power Converters - The Emergence of the Gallium Nitride Transistors

A lot of research has been conducted recently on the area of wide-bandgap semiconductors, such as silicon carbide (SiC) and gallium nitride (GaN), showing remarkable advantages in high-frequency and high-power applications. The capability of these devices to operate at both higher temperature and higher efficiencies promises significant improvements on the reliability and viability of the power electronic modules.

Section 2.1 presents a short description of the principles of the dc/dc conversion and an explanation of the topology operation. In section 2.2, the way of achieving higher power densities together with the limitations will be described and the state-of-the-art power densities in dc/dc converters will be discussed. Finally, section 2.3 gives an overview of the GaN technologies, presents some already existing applications of such devices and discusses the a drawback of this devices when operating at high frequencies, the switching loss.

2.1 DC/DC Power Converters

During the past few years, there is a general trend in the area of power conversion to higher power densities while maintaining high efficiencies, mainly driven by reduced weight/space in applications like automotive, aircrafts [12], and microprocessors [16]. However, in order to understand the procedure through which power density may be increased within a power converter, an understanding of the general principle behind the dc/dc voltage conversion and an explanation of the topology's operation, from which the topic of this thesis was born, are considered necessary.

DC/DC Conversion Methods

The first and oldest method of achieving dc/dc voltage conversion is by means of linear voltage regulators. They adjust a variable resistor in order to provide a constant output

voltage, dissipating the excess electric power in the form of heat. They are inexpensive, quite simple to use and provide a very low noise output, but they suffer from inefficiency when there is large difference between the input and the output voltage. However, when higher efficiency and smaller size or lighter weight are demanded, switched-mode conversion is used. Switching regulators utilize one or more switches in order to maintain an average output value. Magnetic field storage components (inductors) or electric field storage components (capacitors) are used to store the input energy temporarily and release it later in order to transform a dc voltage from one level to another. Nevertheless, complexity is increased and precautions must be taken in order to avoid the electromagnetic interference caused by the high frequency switching.

Switched-mode dc/dc converters are used to convert an unregulated dc input into a controlled dc output at a desired voltage level. There are many dc/dc converters topologies, but only two of them are considered the basic ones: the buck converter (also known as step-down converter because it steps the output voltage down) shown in figure 2.1a and the boost converter (also known as step-up converter because it steps the output voltage up) shown in figure 2.1b. The rest of the converters are either combination of the two (like buck-boost and *Ćuk* converters) or they are derived from either the buck converter (like half-bridge and full-bridge converters) or the boost converter (like the flyback converter). For a given input voltage, the output voltage is controlled by adjusting the on and off durations (t_{on} and t_{off} respectively) of the switch. One of the most common method for controlling the output voltage utilizes a constant switching frequency and, hence, a constant switching time period ($T_s = t_{on} + t_{off}$). In this method, known as pulse-width modulation (PWM) switching, the switch duty cycle, which is defined as the ratio of the on duration to the switching time period ($D = {}^{t_{on}}/_{T_s}$), is varied by changing the on duration of the switch and consequently the average output voltage is controlled. Other control methods with variable switching frequency exist too, but this variation in the switching frequency makes the filtering of the ripple components in the converter's input and output waveforms more difficult [17].

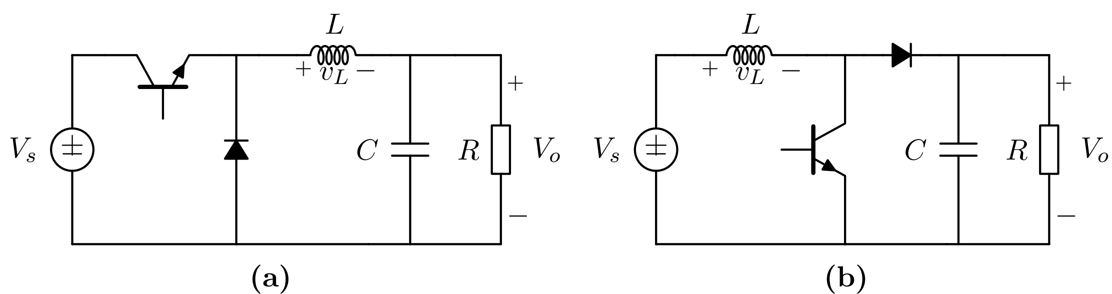


Figure 2.1: Basic dc/dc converter topologies. (a) Buck Converter & (b) Boost Converter

In many applications, it is considered desirable to incorporate a transformer into the switching converter. The main reason for this incorporation is to provide galvanic isolation between the input and the output of the converter. Adding a transformer into the switching converter not only offers isolation, but also the possibility to choose the value of the voltage and current in the secondary side by the proper choice of the turns ratio. This can eventually help minimizing the voltage and current stresses imposed on the transistors and diodes [18]. Moreover, multiple dc outputs can also be created, by simply adding multiple secondary windings and secondary-side circuits. There are several

ways of adding transformer isolation into a dc/dc converter and almost all the isolated converters are isolated versions of the non-isolated ones. For example, the full-bridge, half-bridge, forward, and push-pull converters are commonly used isolated versions of the buck converter. Similar isolated versions of the boost converter are also known (by inverting the source and load of the buck-derived isolated converters, transformer isolated boost converters can be derived). The flyback converter is an isolated version of the buck-boost converter and isolated versions of the SEPIC and $\acute{C}uk$ converter are also well known.

Non-isolated converters, are very common these days and widely used in computers, telecommunication systems, portable electronics and many other applications. They are usually built directly on the motherboard and very close to the load, hence they are also called point-of-load (POL) converters. They are usually constructed with discrete components and, thus, operate at a lower frequency around $100-600kHz$ to achieve a decent efficiency. In order to achieve higher power density in POL converters, significant increase in the switching frequency and level of integration need to be achieved. Therefore, there is currently a lot of research conducted in industry to develop a high-frequency integrated POL converter [19]. Isolated dc/dc converters are also widely used in many applications and depending on the power level of the application different topology is selected, i.e. flyback and forward are usually selected for low power applications while half-bridge and full-bridge are used for medium or high power applications.

These converters can also be categorized based on whether there is a direct path between the input and the output terminals during at least one switching state, known as direct converters, or there is no direct path between the terminals in any state, known as indirect converters [20]. It is quite noteworthy that the presence of transformers or additional filters does not reverse the above characteristic. Examples of direct topologies include the buck, boost, forward while examples of indirect topologies include the buck-boost, the $\acute{C}uk$, the flyback. The direct topology is preferred for high power density applications because the direct connection between the terminals allows part of the electrical energy that must be transferred from the input to the output, to be transferred without having to be stored first in the passive components.

Soft-Switching PWM converters

Integral part of the dc/dc converters are the semiconductor devices that are used as switches. These devices are followed by conduction and switching losses that usually dominate the other converter losses. Switching loss constitutes a significant source of inefficiency of the converters and they will be studied separately later on in this thesis. Although, the turn-on and turn-off transitions of the semiconductor devices, nowadays, are in the range of nanoseconds to microseconds, the instantaneous power loss that occurs in the semiconductor devices during these transitions can be very large (see figure 2.4).

The basic PWM converters are hard-switched. They transfer power across their terminals by means of abrupt switching between the turn-on and turn-off states of the semiconductor devices. This hard-switching operation, however, results in significant increase in the switching loss and stress upon the switches, especially at higher frequencies. Therefore, increasing the switching frequency in order to achieve higher power density and at the same time having high efficiency, is limited with these converters. Following the contin-

uously increasing demand for higher power density and higher efficiency, soft-switching PWM converters have developed. Soft-switching is realized by either zero voltage switching (ZVS) or zero current switching (ZCS), causing a notable reduction in the switching losses and stresses compared to the basic PWM converters. In order to achieve the ZVS or ZCS, additional energy needs to be stored in the topology [21], [22]. This energy usually comes from an auxiliary circuit or by operating the topology in such a way that the additional energy is stored in the already available passive components. In addition, the energy that is stored in the output capacitances of semiconductor devices and in the leakage and stray inductances of the circuit, can also be used to achieve the ZVS or ZCS.

The full-bridge PWM converter is one of the most widely used circuits in high-power applications and through the years different ZVS and ZCS techniques have been proposed in order to improve the performance of the converter [23–29]. The background of this thesis is a high power density, high efficiency application where a full-bridge converter with the phase-shift technique to achieve ZVS and control the output voltage at constant frequency with a current doubler rectifier (CDR) at the secondary side of the transformer to improve the performance of the converter, shown in figure 2.2, was developed.

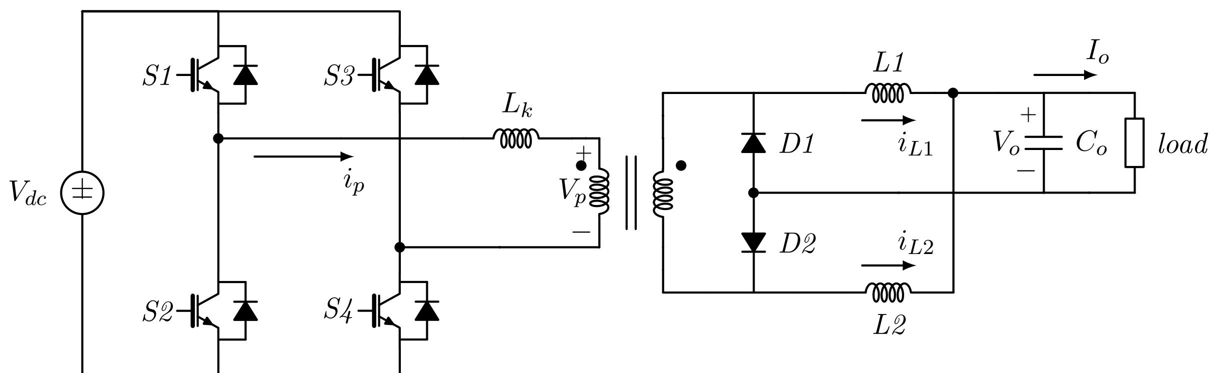


Figure 2.2: A full-bridge converter with a CDR at the transformer secondary side

The principle behind this operating mode of the full-bridge PWM converter is to utilize the circuit parasitics, which at higher frequencies become very important for the converters performance, in order to achieve ZVS for all the switching devices. More specifically, it utilizes the leakage inductance of the transformer and the output parasitic capacitance of the power switches to achieve zero volt turn-on switching transitions. As already mentioned above, it uses the phase-shift technique to achieve ZVS. In this technique, the switching transition of the switches in the leg $S1 - S2$ is delayed (phase-shifted) with respect the switching transition of the switches in the leg $S3 - S4$, instead of turning on the diagonally opposite switches in the bridge simultaneously, determining the duty cycle of the converter (in figure 2.3 this time shift occurs at intervals $t2$-$t3$ between $S1$, $S3$ and at $t8$-$t9$ between $S2$, $S4$).

Looking at figure 2.3, power switches $S1$ and $S4$ are turned on before time $t1$, when $S4$ is turned off. A dead time interval is then added between the $S4$ turn-off and $S3$ turn-on. During that interval, the output capacitance of $S4$ is charged from 0 to v_{dc}, while $S3$'s output capacitance is discharged from v_{dc} to 0. Thus, the $S3$ can be turned on under ZVS operations at time $t2$. Likewise, at time $t3$, power switch $S1$ is turned off and a dead time interval is added before $S2$ turn-on. During that interval, the output

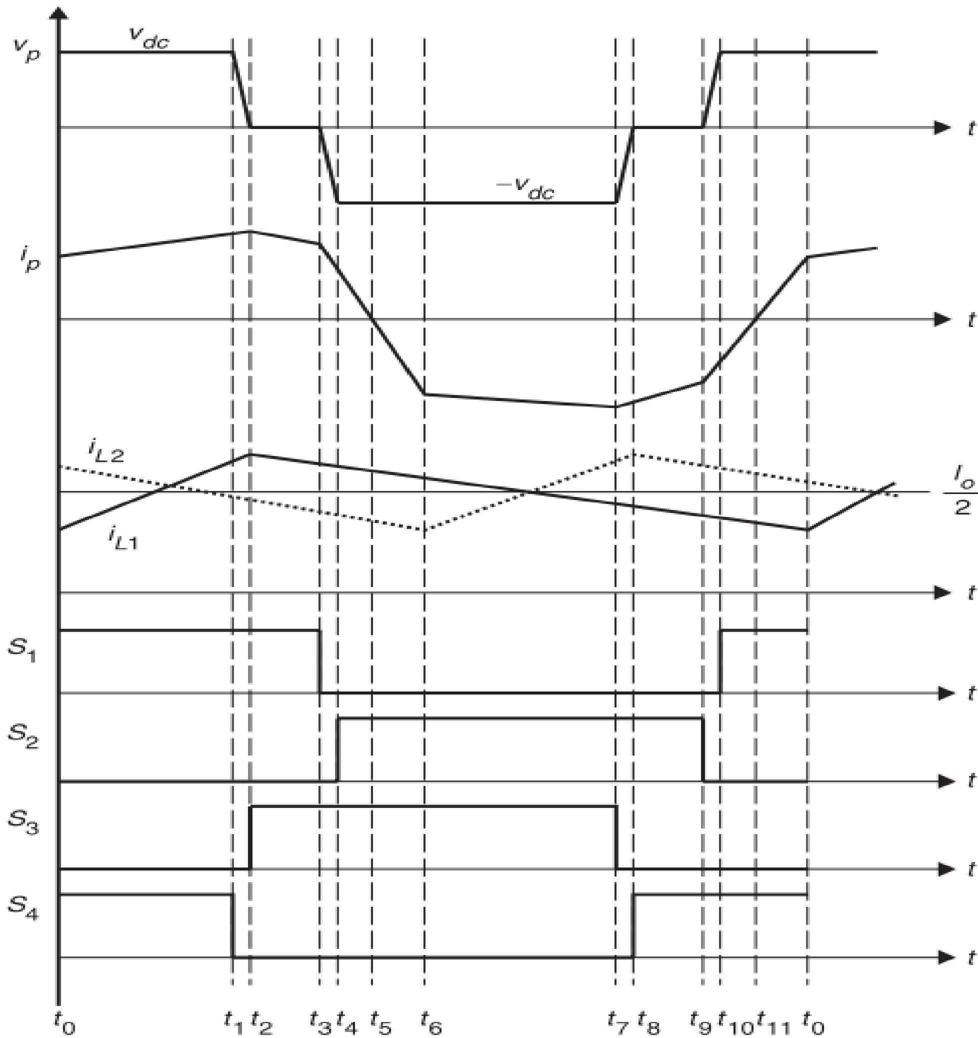


Figure 2.3: Key waveforms of the full-bridge dc/dc converter with CDR [30]

capacitance of $S1$ is charged from 0 to v_{dc}, while $S2$'s output capacitance is discharged from v_{dc} to 0, so the $S2$ can be turned on under ZVS operation. Consequently, in order to ensure the ZVS, the dead time intervals between the $S4$ turn-off and $S3$ turn-on, as well as between the $S1$ turn-off and $S2$ turn-on, must be enough for the charging/discharging procedure [23].

However, the procedure through which ZVS is achieved for both legs of the bridge is different. For the transistors $S3, S4$, the energy to charge and discharge the output capacitance of these switches, is provided by the leakage inductance of the transformer plus the output filter inductor. Consequently, the amount of the inductive energy available for ZVS is higher, which makes it easier to achieve ZVS for these switches. On the other hand, for the transistors $S1, S2$ the ZVS is provided by the resonance between the leakage inductance and the output capacitances of the switches, which causes one of the main drawbacks of this operating mode. In order to ensure the ZVS operation, the energy stored in the transformer's leakage inductance, which is used as the resonant inductance, must be greater than the energy stored in the the output capacitances of the switches, which are the resonant capacitance. Due to the small value of the leakage inductance, the current through it might not be enough to charge/discharge the output capacitance

of the switches during operation of reduced output power. This dependency of the load current might cause the converter to loss the soft-switching characteristic for light loads. In addition, for high switching frequency operation, the parasitic capacitance of the transformer's primary winding should be taken into consideration. This capacitance is added to the resonant capacitance, increasing the energy stored in it and eventually, higher energy required to be stored in the leakage inductance in order to ensure ZVS. A more detailed explanation of the converters operation and possible solutions to increase the ZVS range by utilizing the magnetizing inductance of the transformer are given in [23], [28], [30].

The full-bridge phase-shifted dc/dc converter is considered capable of achieving high efficiency while the ZVS allows operation with reduced switching losses and stresses on the devices, which allows the increase of the switching frequency for improved power density. It is characterized by relative simplicity and offers a constant frequency operation, along with other benefits such as low EMI and the integration of the parasitic components in the power circuit. However, it requires an optimized transformer design regarding the parasitic capacitance of the windings because it can affect the performance of the converter.

2.2 Power Density

High power density is considered, nowadays, a critical and favorable system feature for many applications, i.e. in telecommunicantion power supplies [31] and in industrial drives [32]. The increase in power density of power electronic systems was made feasible, so far, by developments in the semiconductors field, namely by semiconductors that can operate at higher switching frequencies and generate less power loss. However, before discussing further the increase in power density, the concept of power density itself must first be defined. The power density of a power converter is defined as the ratio of electrical power delivered from the converter to the total volume occupied by the converter. Mathematically is given by the equation below:

$$\rho = \frac{P_{out}}{V_{total}} \tag{2.1}$$

where, ρ is the power density measured in $[W/m^3]$, P_{out} is the rated or maximum electrical output power of the power converter in $[W]$ and V_{total} is the total volume of the power converter, including all the components and the coolant used in the converter in $[m^3]$.

Power density is a useful figure of merit (FOM) that connects the amount of power, which is being processed or converted in the given volume of the converter. Nevertheless, power density does not take into account the maximum base plate temperature of the converter. Therefore, when converters with base plate are examined, a more meaningful FOM would be considered the thermal density, which does make reference to the heat dissipation related to the base plate area of the module [33].

By the equation 2.1 given above, we can easily conclude that increasing the power density can be achieved by:

1. Increasing the power delivered by the module and/or

2. Reducing the volume of the module for a given power rating.

Increasing the converter's delivered power can be achieved by either increasing its efficiency for a fixed input power, or increasing the switching frequency for a given energy density of the passive components. An increase in the efficiency of the converter implies that the losses in both the active and passive components will be reduced, which can be achieved by utilizing appropriate converter topologies (like discussed in section **??**) and techniques that can improve the efficiency of the converter, like soft switching techniques [29], [34]. On the other hand, increasing the switching frequency in a power converter, as already mentioned above, has become possible due to the development of semiconductors but by looking at the equation 2.2 below:

$$P_{out} = E_{cycle} \cdot f_s \tag{2.2}$$

where, P_{out} is the output power in $[W]$, E_{cycle} is the energy delivered per switching cycle in $[J]$ and f_s is the switching frequency in $[Hz]$, we can observe that an increase in the switching frequency can indirectly affect the power density by both increasing the output power for a given energy density of the passive components and decreasing the volume of the power converter by reducing the energy delivered from the power converter per switching cycle.

The energy delivered from the power converter per switching cycle is determined by the volume of the passive components and the topology in which they are being used. These parameters define the energy density of the passive components and by keeping this energy density constant while increasing the switching frequency, the power delivered by the converter can be increased, according to equation 2.2. Alternatively, it can be considered that:

- A higher frequency, in principle, means that the circuit needs to process a proportionally smaller amount of energy during each cycle for a constant amount of output power, resulting in a reduced amount of energy stored in the passive components, and
- The volume of the passive components is mostly determined by the "place" required to store the electromagnetic energy (dielectric or magnetic material) and the space required to establish the electromagnetic fields (inductor windings and capacitor plates).

Therefore, since less amount of energy is to be stored, the sizes of energy storage and transfer components such as inductors, filters, resonant tanks, decoupling capacitors, power transformers, depending on the frequency operation, will eventually scale down as the frequency increases, and the total volume of the converter module will decrease. A more detailed explanation of how the power density can be increased is given by M. B. Gerber in [35].

Passive components are integral parts of most power converters, performing various functions, like energy storage, voltage and current filtering, and they usually occupy the largest volume in the converter module. So, it would be considered justifiable to push the switching frequency as high as possible to achieve a significant decrease in the power density of the converter. However, certain limitations occur at higher switching frequencies, since

an increase in the switching frequency will also increase the losses in the converter and the influence of the parasitic inductances and capacitances become more critical.

Assuming, for simplicity, the piecewise linear approximation for the switching waveforms of a semiconductor device [17] shown in figure 2.4, the average switching power losses due to turn-on and turn-off transitions can be derived by:

$$P_s = \frac{1}{2} V_d I_o f_s (t_{on} + t_{off}) \tag{2.3}$$

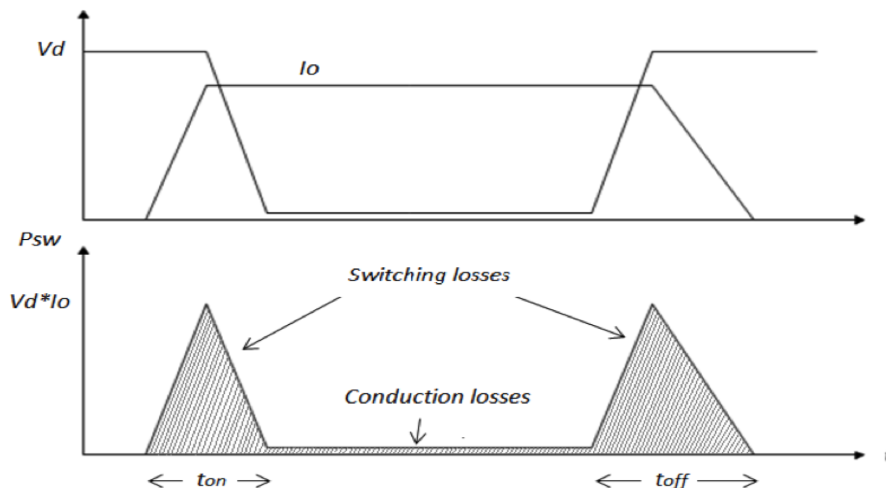


Figure 2.4: Piecewise linear approximation for switching waveforms of a semiconductor device [17]

From the equation 2.3 it is shown that the semiconductor device's switching losses are linearly proportional to the switching frequency. Additionally, at some frequency the losses in the magnetic components start to increase faster (passive component's losses tend to increase exponentially with switching frequency) than the value of the inductance decreases, requiring larger cores in order to reduce the losses, while skin and proximity effects will make the use of more spacious winding techniques necessary [36]. Both semiconductor and magnetic losses generate heat in the power converter, creating in that way the interaction between the electrical and thermal designs, since the heat has to be removed from the converter according to the thermal design.

Thermal Management

Power density improvement has mainly been driven by the development of semiconductors able to operate at higher switching frequencies and generate lower power loss, resulting in smaller size of heat sinks. Increasing the switching frequency of the semiconductors results in a reduced amount of energy stored in passive components, leading to smaller-size passives. Consequently, the converter volume and the surface areas available for the cooling of the components are reduced. However, this growing demand for higher power density has pushed the operating temperature of the components to increase at the point where the components approach their thermal limits and, for the given generation of semiconductors, the power electronics engineers have turned their focus on the component's spatial layout and thermal management for further increase in the power density [37].

Passive components, which are considered low heat density components, come from various manufacturers and in different shapes and sizes. Heat removal from such components is based on their separate heat management embedded in the component itself and on the existence of substantial amount of air around the components (convection heat removal). When these conventional pre-manufactured components are used on single PCBs like is usually done in commercial dc/dc converters, a significant percentage of the volume is occupied by air [33]. This results in an inefficient thermal design and will eventually prevent the increase in power density.

In order to achieve higher power densities while reducing the amount of air around the passive components, heat removal from the power converters has to be based on conduction heat transfer. In many applications, though, the common cooling techniques, such as heat sinks, will no longer be capable of meeting the thermal management demands and more advanced and efficient thermal techniques will be required to effectively remove the heat from the power converters. There are many technologies emerging but the most promising are considered to be the liquid cooling, refrigeration and spray cooling [38]. On the other hand, there are applications, like lighting, automotive, where using cooling fans are not preferred. In these cases the passive components are forced to operate close to their thermal limits and in order to prevent any failures, sacrifices regarding the system power density through allowing more air the components have to be made. Moreover, C. Xiao in [39] proved that pursuing higher frequency alone does not necessarily lead to higher power densities and efficiencies, but there are compromises that should be made depending on the application.

The low power densities of the commercial power electronic converters, caused by the: the poor 3D converter volume utilization and the non-optimized thermal management, has led the thermal management, three-dimension spatial layout and passive components integration technologies to become more and more important factors in reaching higher converter power density and longer converter lifetime. For this reason, a lot of research has been conducted in the past years on these fields, showing significant power density improvements [35], [40], [41], [42], [43] (see figure 2.5). However, the manufacturers of commercial power electronics are not willing to adopt these new technologies, mainly due to their complexity and high cost.

Finally, the converter application and the power level have a significant influence in the power density of the power electronic products. In general, lower power converters present a lower power density than converters designed for higher power applications. The reason for this is that the control circuit, measurements, auxiliary power supplies and semiconductor devices occupy a larger percentage of the overall volume in low power converters, while their size does not increase significantly with the power level. In example, circuitry within a switching control device, nowadays, is small and power dense, and while the semiconductor devices and their control constitute the primary electrical elements of a power converter module, power density isn't significantly affected by either. On the other hand, at higher power levels the thermal management elements occupy a smaller portion of total converter volume as the higher power converters are cooled by forced convection, which is more effective than the natural convection cooling typically used in the lower power converters.

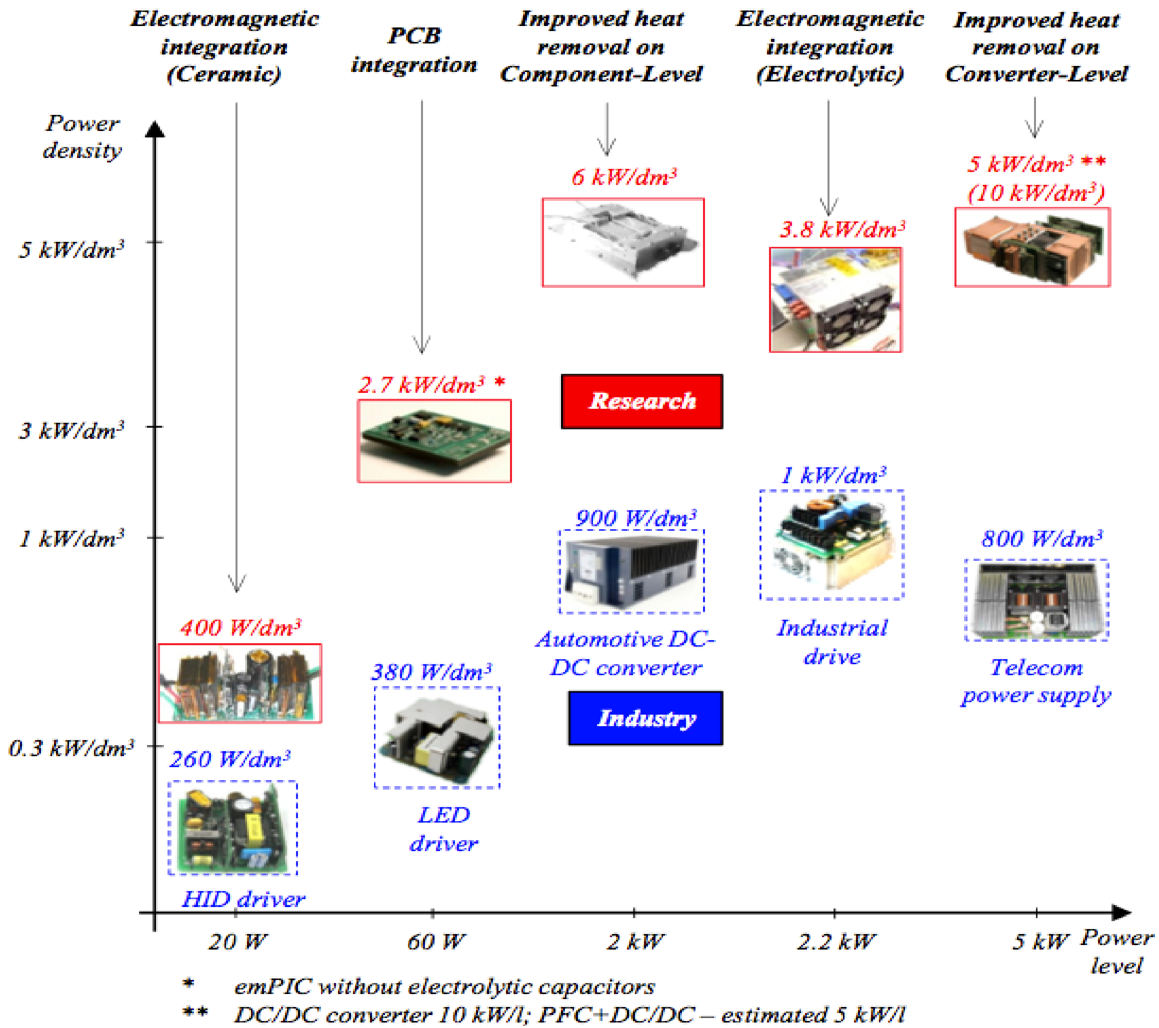


Figure 2.5: Power density of the converters versus power level in industry and research communities [42]

2.3 Semiconductors for High Frequency Applications

Evolution of Power Semiconductors

Achieving higher power densities and higher level of integration has been made possible so far by the improved semiconductors. Until now, silicon-based power devices have managed to monopolize the power electronics and power system applications, by offering multiple advantages to power electronics designers. Specifically in power electronics, there are numerous silicon-based devices that are widely used, such as diodes, thyristors, insulated-gate bipolar transistors (IGBTs) and metal-oxide-semiconductor field-effect transistors (MOSFETs). Power MOSFETs appeared in 1976 as alternatives to bipolar transistors and, within the past decades, they became very popular in power supplies community and in many other applications, due to their superior performance over the other devices. During these years, in order to improve the switching performance and to effectively serve in various applications, different silicon-based MOSFET structures (figure 2.6) have been introduced achieving great improvements in figures of merit (FOMs) [44].

However, although silicon MOSFETs are suitable for high switching frequency appli-

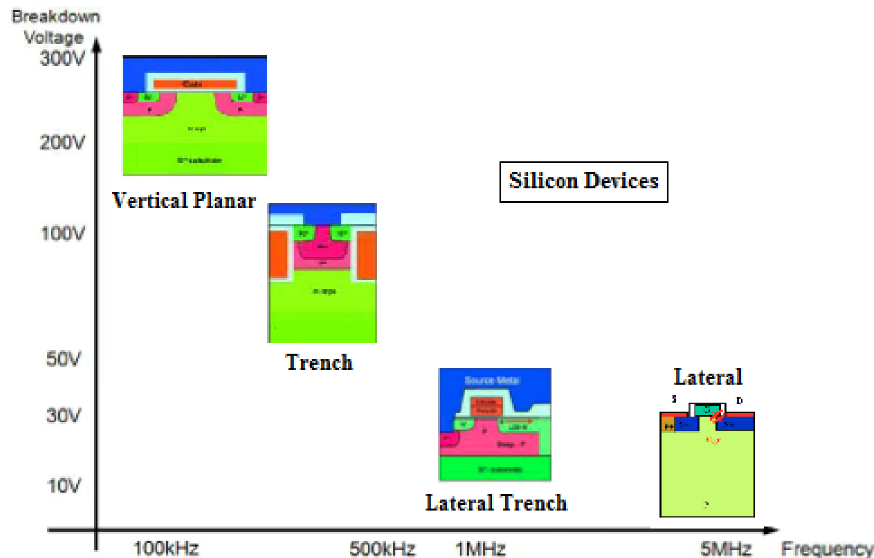


Figure 2.6: Semiconductor device structures [44]

cations, they are considered inadequate for high voltage applications. They suffer from high conduction losses due to their high on-state resistance ($R_{DS,on}$), which increases exponentially with the blocking voltage. As the need for devices with higher voltage and switching frequency capability is growing, silicon-based power devices suffer from limitations due to some inherent material properties, such as low bandgap energy, small critical electric field, low thermal conductivity, and switching frequency limitations [45]. Due to these limitations, the use of silicon-based devices is considered to start reaching a limit.

Wide-bandgap Power Semiconductors

On the contrary, wide-bandgap semiconductors, such as silicon carbide (SiC) and gallium nitride (GaN), are considered promising to solve these issues. Their advanced behavior is due to intrinsic material properties and can be seen from a comparison of these parameters [46]:

- *Energy bandgap*: wide-bandgap semiconductors have wider energy bandgaps ("wider" is usually defined as larger than 2eV) compared to silicon devices, resulting in a much lower leakage current and consequently in higher operating temperatures.
- *Critical electric field*: wide-bandgap semiconductors have higher critical electric field, which allows a significant reduction in the blocking layers thickness while containing higher doping concentrations, resulting in significantly lower on-resistance.
- *Electron saturation velocity*: wide-bandgap semiconductors have higher electron saturation velocity, which leads to higher operating frequencies.
- *Thermal conductivity*: indicates how easily the dissipated power can be extracted from the device. Especially SiC has high thermal conductivity, which leads to better heat spreading and allows operation in higher power densities.

For these reasons, the wide-bandgap devices have received much attention for the past several decades. Silicon carbide device technology has gone from research to commercial

Table 2.1: Summary of key semiconductor material properties

Parameter	*Si*	*4H-SiC*	*GaN*
Energy bandgap, E_g(eV)	1.12	3.2	3.4
Critical electric field, E_c(MV/cm)	0.25	2.2	3
Saturated drift velocity, V_{sat}(10^7 cm/s)	1.0	2.0	2.5
Thermal conductivity, λ (W/cm-K)	1.5	3.8	1.3
Electron mobility, μ (cm^2/Vs)	1350	950	1000
Permittivity, ε_r	11.9	10	9.5

production with the launch of Schottcky diode by Infineon [47] and Cree [48] since 2001. On the other hand, gallium nitride device technology has gone commercial quite recently, by EPC that provides devices with breakdown voltage up to 200V and by Transphorm with 600V devices. There are more companies working on their development, such as IR, MicorGaN, Panasonic and others. Table 2.1 summarizes the key material properties for SiC and GaN compared to Si [49].

The best way to convert these material parameters into a comparison of device performance is by calculating the best theoretical performance that could be achieved in each of these candidates. For that reason, different FOMs have been proposed over the years [44]. In example, the specific on-resistance ($R_{DS,on}$) is considered an important parameter since it indicates how much resistive loss the device generates in the conduction mode and is calculated from equation 2.4 given below:

$$R_{DS,on} = \frac{4V_B^2}{\varepsilon \mu_n E_c^3} \tag{2.4}$$

where, V_B is the breakdown voltage, ε is the permittivity, μ_n is the electron mobility and E_c is the critical electric field. It can be seen from the above equation that $R_{DS,on}$ is reversely proportional to critical electric field and since the E_c of SiC and GaN are 8-9 and 12 times higher than that of Si, respectively, one can easily understand the important advantage of using wide-bandgap semiconductors. Figure 2.7 shows a comparison of the specific on-resistance versus breakdown voltage for Si, SiC and GaN devices.
However, the specific on-resistance versus the breakdown voltage is considered adequate only in low frequencies where the device loss is dominated by its conduction loss. When investigating the use of a device in high frequencies, designers prefer to use another FOM that is the product of gate-drain charge (Q_{gd}) and on-resistance ($R_{DS,on}$).

Emergence of Gallium Nitride HEMTs

Gallium Nitride transistor has emerged as possible candidate to replace silicon and even silicon carbide devices in various power conversion applications. GaN devices offer potential benefits for high frequency power conversion, due to their material properties listed in table 2.1 above. Their operation is similar to the MOSFETs, as it is based on a conductive path formed by a channel of electrons between the drain and the source, which is controlled by the gate-source voltage. Currently, there are no available homoepitaxial GaN waffers yet, most technologies are based on a GaN epitaxy on either SiC, sapphire

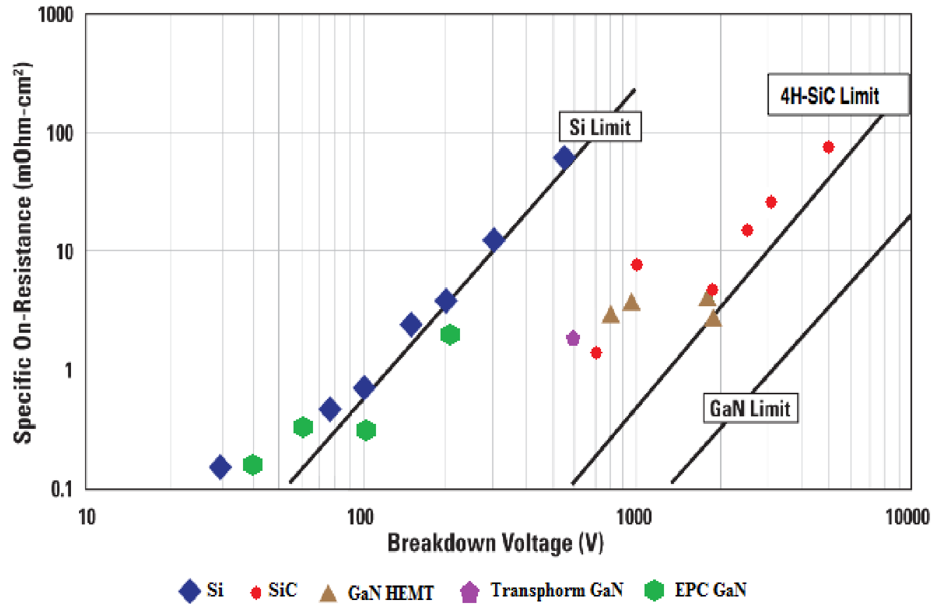


Figure 2.7: Comparison of Si, SiC and GaN specific on-resistances [50]

or silicon wafers, which basically constitutes an important disadvantage of GaN devices over SiC MOSFETs. Although, SiC substrates have much higher thermal conductivity than Si ones, the majority of GaN transistors intended for power electronics use are built on a Si substrate, in order to simplify fabrication and reduce cost. However, GaN-on-SiC HEFTs are also examined and a review can be found in [51].

A typical structure of a GaN device is shown in figure 2.8. An Aluminum Nitride (AlN) transition layer that isolates the GaN from the Si substrate, exists on top of the Si substrate. The next layer is the base of the GaN transistor, a thick layer of highly resistive un-doped GaN, and on top of that lies a thin layer of highly conductive AlGaN. The combination of the thin AlGaN layer on top of a high quality GaN surface creates a two-dimensional electron gas (2DEG) layer, which acts as the electron channel, and makes the GaN transistor a high electron mobility transistor. Drain and source electrodes form an ohmic contact with the underlying 2DEG, which creates a short circuit between them until the 2DEG layer is depleted by the gate electrode that is placed on top of the AlGaN layer.

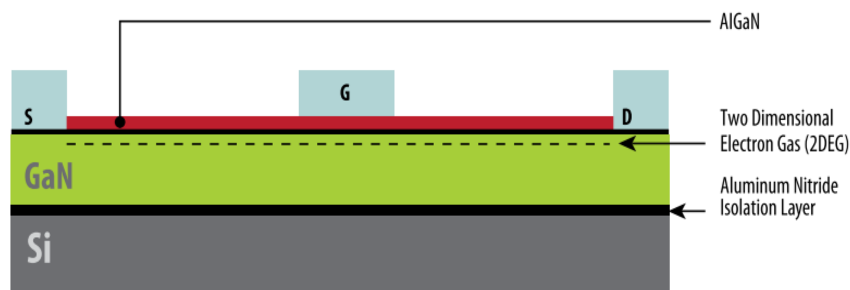


Figure 2.8: The basic GaN transistor structure [52]

Furthermore, at the heteroepitaxial devices the lattice mismatch and thermal coefficients of expansion mismatch between the substrate and the GaN layer can lead to stress of

the materials. In order to achieve material matching between the substrate and the GaN layer, the AlN layer is used. However, this layer makes the manufacturing of vertical devices not possible and, thus, the main device design of a GaN is a lateral FET structure. On the other hand, lateral structure requires large chip areas in order to achieve high breakdown voltages, which is translated into high costs and manufacturing difficulties, making them unsuitable for high voltage applications.

The GaN transistor can be categorized, depending on its physical structure, as operating in either enhancement mode or in depletion mode. The most notable difference between the two is that the enhancement mode GaN is a normally-off device that requires a positive voltage to turn-*on*, while the depletion mode GaN is a normally-on device that requires a negative voltage to turn-*off*. Their difference is that at the enhancement mode structure, the gate electrode is placed properly on top of the AlGaN layer so that a depletion region is formed underneath it, instead of the 2DEG layer. The requirement of negative voltage in order to turn-off is a significant disadvantage for the normally-on devices.

Currently, for low voltage applications, there are two types of GaN transistors available on the market: the depletion mode GaN transistors from International Rectifier (IR) [53] and the enhancement mode GaN transistors from Efficient Power Conversion Corporation (EPC) [54]. Until now, the application of the enhancement mode GaN transistor is limited due to critical driving issues as addressed in [55], [56]. The enhancement mode GaN transistor has gate voltage limits between -5V to 6V and it is designed to achieve maximum performance with a gate voltage between 4.5-5V. This leaves a very small margin for safe operation and a quite demanding gate driving design need to be considered. On the contrary, the depletion-mode GaN transistor is preferred due to simple and safe gate drive, since it has gate voltage limits between -10V to 6V and it is designed in such a way so that the device is driven on at 0V and driven off at -3.3V. However, this means that both positive and negative power supplies are needed for the driver.

A lot of research has been conducted the past years regarding the low voltage GaN transistors showing significant improvements for the point of load (POL) converters. D. Reusch presented a $12V$, $20A$, $2MHz$ converter with an efficiency of 83% and power density $750W/in^3$ doubling the power density of POL converters until that time [56]. S. Ji demonstrated three 12V to 1.2V POL modules in [55] achieving even higher power densities than before: a single phase $20A$, $900W/in^3$, $2MHz$ converter with enhancement mode GaN transistors, a single phase $10A$, $1100W/in^3$, $5MHz$, and a two-phase $20A$, $1100W/in^3$, $5MHz$ using depletion mode GaN transistors. Next, M. Acanski in [57] showed that enhancement mode GaN transistors used for a 12V to 48V boost converter, aimed for PV applications, achieved better performance compared to their Si counterparts for power values over $60W$ while operating at double the switching frequency. These results prove the significant contribution of GaN devices for low voltage high power density applications, as it combines better efficiency and smaller size components.

For higher voltage rating GaN HEMTs (600V), the depletion mode device technology is considered more mature and its performance has been studied by W. Saito in [58], where a $120W$, $1MHz$ boost converter with an efficiency of 94.2% and a peak voltage of 350V is demonstrated, and by Y. Wu, who presented a 175V to 350V, $300W$ boost

converter at $1MHz$ with an efficiency of 97.8% in [59]. However, the depletion mode device is a normally-on device, which means that the device is conducting in the absence of applied voltage. This requires the driving circuit to be operating before the input voltage is applied on the devices, otherwise a short circuit between the input and the output will happen. In order to use a high-voltage depletion mode GaN transistor in a circuit design, a low voltage Si MOSFET is used to drive the high voltage GaN transistor, which is well known as a cascode structure and helps to generate a normally-off condition from a normally-on device [60].

2.3.1 High Voltage GaN-HEMT in cascode configuration

In high voltage depletion mode GaN HEMTs, the driving circuit can operate in a voltage range between -30V to 2V and -5V is required to fully turn-on, which ensures a sufficient safety driving margin. To easily apply the depletion mode GaN HEMT in a circuit design, a cascode structure is used. In this configuration, only the low voltage Si MOSFET is actively controlled while its drain-source voltage acts as a control for the GaN HEMT. Specifically, the GaN HEMT's gate is connected to the Si MOSFET's source, causing its drain-source voltage to become the negative gate-source voltage of the GaN HEMT and provide the negative gate voltage required to pinch off its channel as shown in figure 2.9.

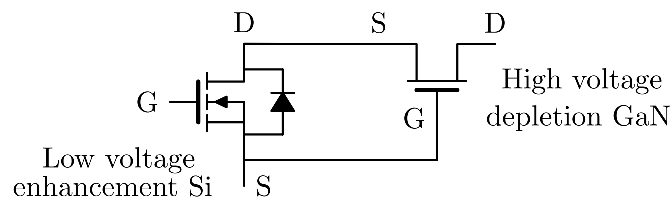


Figure 2.9: GaN HEMT in cascode configuration

The cascode GaN HEMT takes advantage of both Si MOSFET and GaN HEMT. The GaN HEMT blocks high voltage with high switching speed while the Si MOSFET provides more rugged gate-source voltage and more stable threshold. The principle of cascode GaN HEMT operation is quite straightforward. Basically, the on/off state of the high voltage GaN HEMT is being controlled by the on/off state of the low voltage Si MOSFET. During turn-on period, the low voltage Si MOSFET turns on first, and when the gate-source voltage exceeds the threshold, the drain-source voltage which is also the *source-gate* voltage of GaN HEMT will decrease. Consequently, the GaN HEMT will turn on when the gate-source voltage exceeds the threshold. Similarly, during turn-off period, the Si MOSFET turns off first, and the drain-source voltage increases. GaN HEMT will turn off when gate-source voltage drops below the threshold. Controlling the on/off state of the low voltage Si MOSFET in order to control the on/off state of the high voltage GaN HEMT makes the cascode GaN HEMT compatible with the commercial drivers.

In an inverter application, even if the transistor is turned off, reverse conductivity of the switch is required. In case of the cascode configuration, the reverse current flows through the body diode of the low voltage Si MOSFET and its drain-source voltage becomes the negative value of the diode's forward voltage. Thus, the GaN HEMT gate-source path becomes slightly positive biased resulting in a turn-on of its channel. As a consequence, if the Si MOSFET is turned off, reverse current flows through the MOSFET body diode and reverse direction of the GaN channel [61].

Cascode GaN HEMT Applications

The behavior of the high voltage cascode GaN HEMT has already been examined in few publications showing noteworthy results. However, its use still remains in research level. X.Huang in [13] compared the cascode GaN HEMT and a state of the art Si MOSFET while operating on a 380V to 200V, $500kHz$ hard-switching buck converter. He proved that the low reverse recovery charge and the relatively small output capacitance of the cascode GaN HEMT will lead to smaller transitions times and eventually to an improved efficiency of the buck converter. Moreover, a $1MHz$, $300W$, $400V/12V$ LLC resonant converter was used in the same publication to show the advantages of the GaN HEMT over the Si MOSFET. An LLC resonant converter was also used by W.Zhang in [62], in order to compare the performance of the topology when 600V Cascode GaN HEMT and state of the art Si CoolMOS are used. The results showed that the total device loss was improved by 42% with the GaN device, while the total efficiency was improved only by 0.5%. When a LLC resonant converter operates at the resonant frequency, ZVS for the primary switches and ZCS for the secondary switches can achieved. Thus, the GaN HEMT is considered more suitable due to its small output capacitance enabling both low magnetizing current and dead time, which will cause smaller conduction and switching losses. However, it was observed, and it will also be shown in this thesis project, that the turn-on switching loss of the GaN HEMT is quite high and soft-switching is required in high frequency operation.

Next, J. Everts presented in [63] a 76V to 142V boost converter with enhancement mode GaN transistor achieving efficiency of 96.1% at $106W$, $512.5kHz$,and 93.9% at $97.5W$, $845.2kHz$.

Measurement Challenges

Additionally, the measurements of the electrical quantities are becoming more challenging as the power converters are moving into higher frequency and smaller volume. In order to accurately determine the switching power losses of semiconductor devices, current and voltage measurements need to be taken during the turn-on and turn-off switching transients. However, they are characterized by very high current and voltage rates of change, making the gathering of accurate measurements of their switching behavior a challenge. Therefore, high performance voltage and current measurement equipment has to be used. For measuring high frequency signals, conventional measurement equipment are no longer suitable due to their limited bandwidth and dynamic frequency response limitations. The interferences from high dv/dt or di/dt signals and the intrusion of probes and oscilloscopes into the circuits result in measurement deviations. Consequently, accurate power loss measurements are becoming increasingly difficult as frequency is being pushed higher [39]. A discussion about the measurement equipment and techniques that can be used in higher frequencies will be given in chapter 4 of this thesis.

2.3.2 Switching Losses

The emergence of the wide-bandgap semiconductor devices has made it possible for the power electronics designers to push the switching frequency into much higher levels in order to achieve higher power density and the miniaturization of the power converters. However, increasing the switching frequency is strongly connected with higher switching

losses and thermal stresses on the switching devices that can significantly lower the power efficiency and the overall performance of the converter module.

In order to optimally design a high frequency switching power converter, an estimation of the power losses is considered mandatory before moving to the thermal design and the power device selection. Power devices have a maximum allowable junction temperature that ensures safe operation and in the same time constitutes a limiting factor whether a power device can be used into a specific application or not. However, a direct measurement of the junction temperature is not always possible and for this reason an accurate calculation of the conduction and switching losses of the switching device is required. The conduction losses can be estimated relatively easily, since they require values that are easy to compute or are already known, such as the on-resistance or voltage-drop over the device, rms current through the device and duty cycle. On the contrary, the switching losses are often hard to estimate or they require lots of time consuming measurements. Consequently, an accurate loss model is required in order to investigate the performance of a circuit.

There is an abundance of publications dealing with loss models, each achieving unique balance between accuracy and simulation time. As discussed in [64], the loss models can be distinguished in three main types: the physics-based model, the behavior model and the analytical model.

- Firstly, the physics-based models require the physical parameters of the device and the circuit in order to accurately calculate the device losses by utilizing finite element analysis (FEA) tools. However, it is time consuming and more important is the fact that the designers don't know the exact parameters of the device.

- Secondly, the behavior models use the device behavior model, provided by the vendors, for calculating the device losses by using Pspice or SABER simulation tools. Its simulation speed is faster than the physics-based model and it presents a sufficient balance between accuracy and simulation time [65].

- Finally, analytical models are math based and the loss expressions are derived by the equivalent circuits during each step of turn-on and turn-off transitions of the device. It is the fastest method and it is considered suitable for data processing, but they lack in accuracy.

Using loss models, many design parameters and components can be compared in order to achieve a design with the optimal combination of efficiency and cost. From the three categories previously described, analytical models are usually much preferable when designing a converter due to the simplicity, the suitability for parametric analysis, and the small simulation times.

The most simple analytical loss model uses piecewise linear waveforms for the switch turn-on and turn-off transitions (figure 2.4). However, as the switching frequency increases, parasitic inductances resulting from the Printed Circuit Board (PCB) layout and device package start to influence the switching performance more and more as they may oscillate with the parasitic capacitances of the switching device. Therefore, neglecting the influence of the parasitic elements is no longer tolerable, as they extend the switching times and the oscillations will induce excessive voltage and current stresses on the switch,

causing destructive results. In order to improve the accuracy of the analytical model, the parasitic elements of the device and the circuit need to be taken into consideration.

MOSFET Switching Characteristics and Influence of the Parasitic Elements

A power MOSFET is mostly used in the literature in order to investigate the influence of the parasitic elements and the nonlinearity of the device capacitances in the switching performance [64], [66–71]. However, the definitions for the switching characteristics are general and they can also be used for other switching devices. The switching behavior of the power MOSFET is tested under the condition of clamped inductive load and a typical example of such load is the double-pulse tester (DPT) (figure 2.10). At the end of the first pulse and beginning of the second pulse measurements of the gate-source voltage (V_{gs}), drain-source voltage (V_{ds}) and drain current (I_d) can be taken in order to characterize the device's switching transients. The main goal of this section is not to explain in detail the operation of the power MOSFET but to give a briefly description of the turn-on and turn-off transitions and the influence of the parasitic elements in each one of them.

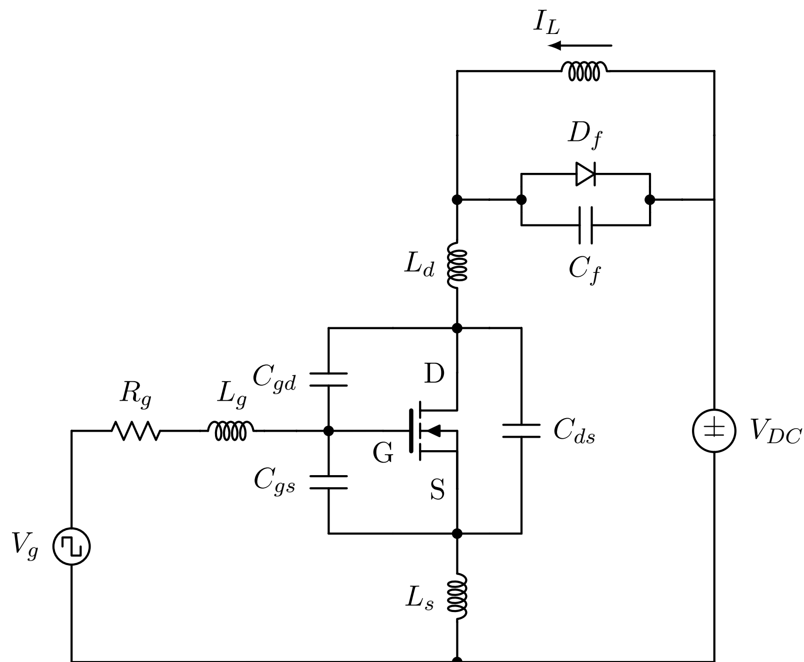


Figure 2.10: Double-pulse Tester schematic including the parasitic elements

Turn-on Switching Transient

The turn-on transition of the MOSFET is usually divided into four phases. In this section, the influence of the parasitic elements in each phase will be presented by a few equations. For more detailed reading, the reader is highly recommended to refer to the references mentioned above.

Phase 1: *turn-on delay time*
The gate voltage (V_{dr}) is applied to the gate and the input capacitance (C_{iss}) of the MOSFET is being charged. The input capacitance is a combination of the C_{gs} and C_{gd}

and along with the gate resistance (R_g) determine the time constant of the gate voltage's increase. Since the C_{gs} is the biggest part of the input capacitance, an increase in the C_{gs} will increase the delay time making the V_{gs} slower.

The parasitic inductance L_g is usually neglected from the analytical models, as it is minimized by placing the gate drive circuit as close as possible to the switch. However, it tends to resonate with input capacitance, causing oscillations to the V_{gs}, but without really influencing the V_{ds} and I_d. The C_{gd} doesn't play significant role in this phase because it is relatively small compared to C_{gs} and its value is dependent to the V_{ds}, which is constant during this phase. This phase ends when the V_{gs} reaches its threshold value.

Phase 2: *current rise period*

During this phase the V_{gs} increases beyond the threshold and the MOSFET starts to conduct current. The MOSFET usually operates in the saturation region [69] and both the I_d and the V_{ds} change. The change in the I_d will induce voltages on the L_d and L_s that will impact the switching performance.

More parasitic elements influence the switching during this phase and, thus, there are two cases that are usually discussed in the literature [64], [69]. The C_{gs} continues to influence the rate of change of the V_{gs}, which in saturation region, is proportional to the current slew rate. As the C_{gs} increases, the current slew rate decreases, having impact on the current stress and the V_{ds} drop. The rate of change of the V_{gs} is lower in this phase compared to the previous due to the negative feedback by the L_s, as the voltage induced across this inductance opposes the changing in the V_{gs}, thus slowing down the I_d. Therefore, an increase in the L_s, significantly increases the switching losses. The inductance L_d, like the L_s, slows down the I_d, but mainly affects the V_{ds} during this phase. A big value of L_d can cause a large drop in the V_{ds} and basically determines which case will be used during this phase. The C_{gd} is still small in this phase and it has a small impact on the V_{ds} slew rate.

Moreover, the junction capacitance of the diode (C_f) influence the switching in this phase. In order for the freewheeling diode to start blocking voltage, the C_f needs to be charged and this charging current is added to the I_d causing an overshoot. This increase in the current is reflected to the gate drive circuit causing also an overshoot in the V_{gs}. This phase ends when the I_d reaches its maximum value, together with the reverse peak current from the diode.

Phase 3: *voltage fall period*

During this stage the diode current returns to zero and the diode begins to block voltage, and the V_{ds} continues to decrease until it reaches the voltage V_{miller}. As the V_{ds} decreases, the C_{gd} significantly increases and during this phase it strongly influences the voltage slew rate. Additionally, the C_{ds} that is the biggest part of the output capacitance (C_{oss}) of the MOSFET, is being discharged as the V_{ds} decreases. As the discharging time increases, the voltage slew rate slightly reduces. During this phase, the L_d resonates with the C_f and C_{oss} causing ringing in the current.

Phase 4: *V_{gs} rise period*

The V_{ds} decreases to the $V_{ds(on)}$. The V_{gs}, in order to provide low enough channel resis-

tance, continues to increase with a time constant given by $R_g(C_{gd} + C_{gs})$. However, the value of the C_{gd} has increased a lot since the V_{ds} is almost zero.

Turn-off Switching Transient

Similar to turn-on, turn-off is also divided in four phases.

Phase 1: *turn-off delay time*
The V_{gs} starts to decrease and the C_{iss} is being discharged with a time constant determined by the gate resistance and the value of the C_{iss}, as in the phase 1 of the turn-on transition. Since the V_{ds} is close to zero the C_{gd} is much bigger compared to the phase 1 during turn-on and thus more time is required to discharge the C_{iss}. However, even though the C_{gd} is bigger, the C_{gs} dominates the C_{iss} and influences the time delay of the V_{gs}. This phase ends when the gate voltage drops to V_{miller}.

Phase 2: *voltage rise period*
During this phase the V_{gs} remains constant at the V_{miller} in order for the MOSFET to afford the load current. V_{ds} starts to increase with a slew rate given by the equation:

$$\frac{du_{ds}}{dt} = \frac{V_{miller}}{R_g C_{gd}} \tag{2.5}$$

It can be seen from equation 2.5 that the slew rate depends on the nonlinearity of the C_{gd}. As the voltage increases, the C_{gd} decreases and the slope of the V_{ds} will increase. Moreover, the voltage across the C_{oss} and C_f changes as the V_{ds} increases, and the current flowing thought cannot be neglected. The C_f is being discharged by drawing part of load current, causing a drop in the I_d even before the diode starts forward conducting. On the other hand, the C_{oss} is begin charged during this phase, drawing current from the load current, causing the channel current to be less than the measured I_d. Larger values of C_{oss} will slow down the voltage slew rate as more time is required for charging the capacitance. This phase ends when the voltage reaches the V_{DC} bus voltage and the freewheeling diode stops blocking voltage.

Phase 3: *current fall period*
During this phase the load current begins to fall, as it is transferred from the MOSFET to the diode. The V_{gs} continues to fall with the same time constants as in phase 1 of turn-on, with the difference that it starts falling from the V_{miller} value. The V_{ds} ideally would be considered constant at the V_{DC}, but as the current decreases there are voltages induced in the parasitic inductances L_d and L_s, reshaping the voltage. Especially, big values of L_d can cause a voltage overshoot inducing an extra stress on the device. This phase ends when the I_d reaches zero and V_{gs} reaches the threshold voltage.

Phase 4: *V_{gs} fall period*
During this phase the rest of the charge stored in the C_{iss} of the MOSFET is being discharged until the V_{gs} becomes zero. The voltage overshoot from the previous phase is being damped by the stray resistance of the circuit. However, since the drain voltage still changes, there is a current in the C_{oss} affecting the drain current. Moreover, the L_d tends to resonate with the C_{oss} during this phase causing ringing in the voltage and current waveforms.

Summary of the switching transitions

From the description of the turn-on/off transitions, it can be concluded that the switching waveforms will appear different from the piecewise linear waveforms. Parasitic elements, such as the junction capacitance of the freewheeling diode (C_f), the junction capacitance of the MOSFET (C_{ds}) and the switching loop inductance (L_d), will eventually deteriorate the switching transitions and causing them to appear like in figure 2.11.

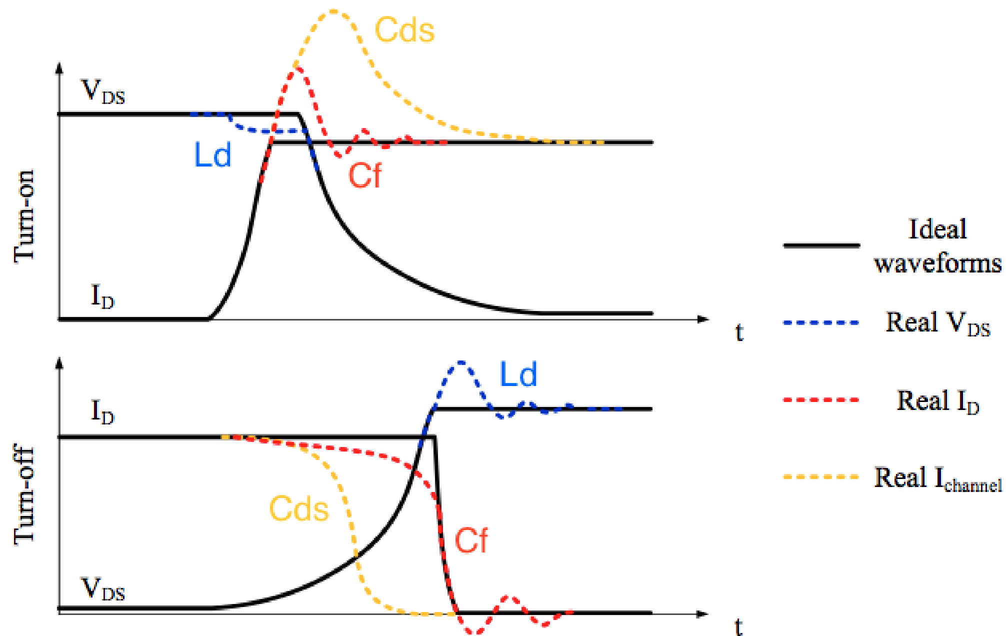


Figure 2.11: Effect of the parasitic elements on the switching transitions [71]

The diode's junction capacitance is getting charged and discharged during the turn-on and turn-off process, respectively. Thus, the capacitive current responsible for the charging and discharging process will influence the drain current measured outside the MOSFET by increasing it during the turn-on and causing to fall even before the diode starts forward conducting during the turn-off (red dashed line in figure 2.11). Next, the drain current flows through the switching loop inductance reshaping the dain-source voltage, it forms a notch during turn-on and a peak during turn-off. Also, the switching loop inductance tends to resonate with the device junction capacitance during the switching transients, resulting in high-frequency ringing in the waveforms.

The effect of the MOSFET's junction capacitance cannot be observed by the measuring equipment, but it does change the current distribution within the device. During MOSFET turn-on, the energy stored in this capacitance discharges through the MOSFET channel, causing the channel current to be bigger than what is measured, while during turn-off, this capacitance is charged by drawing some current from the load and causes the channel current to be smaller than the measured current (orange dashed line in figure 2.11).

2.4 Discussion

In this chapter, the theoretical background required during this thesis is discussed. The principles of the dc/dc conversion along with the different topologies of the switched-mode dc/dc power converters that are mostly used in the recent power electronics applications. Soft-switching PWM power converters are introduced and why they can contribute to the increase of the power density and efficiency of the converter is explained. Such a topology is the origin of this thesis project and its operation is presented here.

The concept of the power density in dc/dc power converters is explained along with ways of increasing it. Moreover, different limitations and considerations towards this increase are discussed. The emergence of the GaN devices and how the improved performance of these devices can contribute to the development of the power electronic applications is presented. Finally, a limitation of such devices is discussed, and its understanding is considered important, because it is used throughout the whole thesis.

Chapter 3

Analytical Loss Model of High Voltage GaN HEMT in cascode configuration

As discussed in chapter 2, the increase in power density of power electronic systems was made feasible, so far, by developments in the semiconductors field, namely by semiconductors that can operate at higher switching frequencies while not compromising the circuit's efficiency. Even though, the use of GaN HEMTs allows the increase of the switching frequency to the megahertz range, due to the lower transition times [13], the further increase in the frequency is limited by the switching loss, which, in hard-switching conditions, is the biggest percentage of the total power loss. Accordingly, there is a great desire in developing accurate loss models that can estimate the switching loss and eventually give an good prediction on the maximum temperature and the overall efficiency of the power converter.

Although analytical loss models are considered less accurate compared to the other loss models (see section 2.3.2), they are popular because they are fast and appropriate for data processing. The most popular and simplest analytical model is the piecewise linear model (figure 2.4). However, this model does not predict the switching loss accurately, especially for high frequency applications, because it does not take into consideration the parasitic inductances and the non-linearity of the junction capacitors of the device. More accurate analytical models have been developed during the years, for low voltage [64], [70] and high voltage [69] power MOSFETs, as well as for low voltage GaN HEMTs [72], [19]. Recently, an analytical model for high voltage GaN HEMT in cascode configuration has been proposed by Huang in [73]. This model is the basis for the model that was used during this thesis and it will be discussed and evaluated in this chapter.

3.1 Switching characteristics of the device

In this section the switching transition of the device under the conditions of clamped inductive load will be studied. The switching transition will be divided in stages and the switching loss will be calculated by solving the equivalent circuit for each stage. The afore-

mentioned model takes into consideration the parasitic inductors and the non-linearity of the junction capacitors of the device.

The cascode GaN transistor, manufactured by Transphorm Inc., comes in two different packages: the TO-220 package and the PQFN 8x8 package. In figure 3.1, the equivalent circuit of the high voltage GaN transistor in cascode configuration in a traditional TO-220 package, including its parasitics elements, is shown. Inductances L_g, L_d, and L_s represent the package lead frames, while L_{int1}, L_{int2}, and L_{int3} represent the interconnections between the GaN die, the Si die and the lead frames. Other packages and configurations can be modeled by neglecting the corresponding parasitic inductances. These inductances are in the nH range, but they influence the switching transition significantly when the switching frequency is pushed up to the megahertz range. Due to that fact, the design of the PCB layout becomes even more critical concerning the minimization of the parasitic inductances that induces. Thus, the package and PCB parasitic inductances will be taken into consideration in this model and their influence will be studied later on in this chapter.

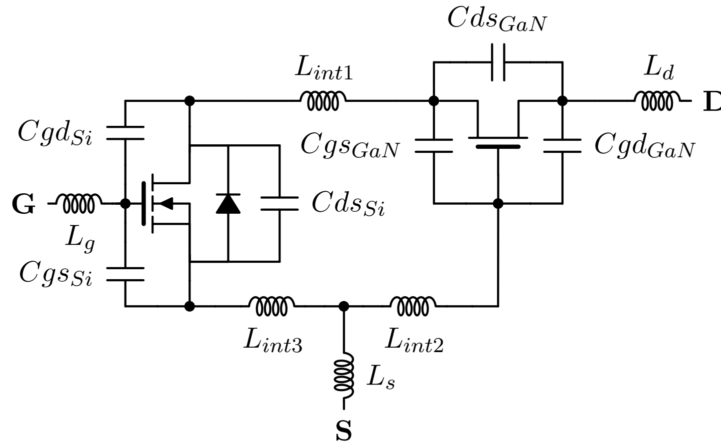


Figure 3.1: GaN HEMT in cascode configuration including parasitic inductors and capacitors

However, the values of these parasitic inductances are not easy to accurately calculate, since, based on the electromagnetic theory, parameters like the dimensions, the positions, and the current directions in the conductors, have significant effect on self-inductance and mutual-inductance [74]. They may be predicted, though, if the spatial configuration of the Si MOSFET die and GaN die in the package, and the bonding diagram of the device are known. Z. Liu in [74] extracted the package parasitic inductances by using Ansoft Q3D FEA simulation for the TO-220 package. They are given in table 3.1 below and these values will be used in this chapter.

Table 3.1: Package parasitic inductances [74]

L_{int1}	L_{int2}	L_{int3}	L_s	L_g	L_d
0.27nH	0.23nH	0.24nH	0.57nH	2.87nH	1.89nH

The junction capacitors of the GaN HEMT and Si MOSFET are also considered parasitic elements of the device and are presented in the figure 3.1. The capacitors shown in the above figure stand for the gate-source capacitance (C_{gs}), gate-drain capacitance (C_{gd}) and drain-source capacitance (C_{ds}) of each die. They are intrinsic capacitors and are formed due to the physical structure of the transistors. Gate-drain and drain-source

capacitances depend on the bias conditions and they change with the applied voltage, while the gate-source capacitance remains constant regardless the applied voltage. Their values are given in the device datasheet as input capacitance ($C_{iss} = C_{gs} + C_{gd}$), output capacitance ($C_{oss} = C_{ds} + C_{gd}$), and reverse transfer capacitance ($C_{rss} = C_{gd}$) and their relation with the applied voltage can be extracted from the C-V characteristic using curve fitting.

However, as can be seen from figure 3.1, the equivalent circuit of the package itself is very complicated and applying non-linear capacitances will further increase the complexity of the calculations. For this, an assumption taken in this model is that discrete values of the capacitances are used during each stage based on the voltage range. As it can be seen from the C-V characteristic of the device used (figure 3.2), the values of the junction capacitances show small changes in the 10-600 Volts range, except the value of the C_{ds}. In order to model this change, the stage that correspond to that voltage range is divided in substages and, thus, the assumption does not affect the accuracy of the model significantly.

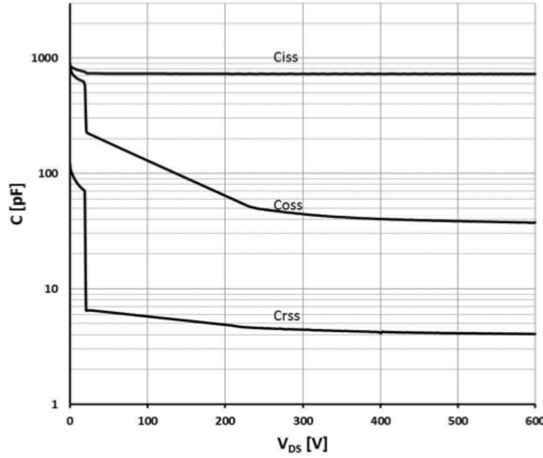


Figure 3.2: C-V characteristic of the GaN HEMT [75]

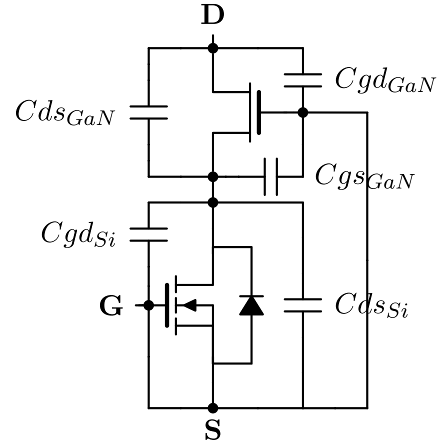


Figure 3.3: Cascode circuit with parasitic capacitances

For voltages lower than 10Volts the values of the capacitors jump abruptly to higher values and this can be explained by the unique structure of the cascode configuration that combines two devices. At the beginning of turn-off transition, the device increases its voltage through the charging process of its output capacitance [61]. Looking at figure 3.3, the output capacitance of the low voltage Si MOSFET must be charged first. Moreover, the gate-source capacitance of the GaN transistor is connected in parallel with the output capacitance of the MOSFET. As the drain-source voltage of the Si MOSFET is lower than the absolute value of the pinch-off voltage of the GaN transistor (approximately 10V), the GaN channel is conducting, connecting the gate-drain capacitance of the GaN in parallel with the capacitances mentioned above.

Consequently, for voltages lower than the pinch-off voltage of the GaN transistor, the output capacitance of the cascode structure is given by the sum: $Cgd_{Si} + Cds_{Si} + Cgs_{GaN} + Cgd_{GaN}$. When the drain-source voltage of the MOSFET reaches the pinch-off voltage of the GaN transistor, the further increasing voltage of the cascode structure is supported only by the GaN transistor and the output capacitance is given by the sum:

$Cds_{GaN} + Cgd_{GaN}$. The impact of this characteristic of the cascode GaN HEMT is significant in bridge configurations and will be studied later on.

3.2 Analysis of the switching transitions

The switching loss of the cascode GaN HEMT will be analyzed under the condition of clamped inductive load by using a DPT circuit. Two different cases can be studied with such a circuit based on the characteristics of the top switch: a switch (i.e. a SiC Schottky diode) with no reverse recovery charge can be used or an active switch (i.e. same switch as the DUT) with reverse recovery charge modeling a bridge configuration. An inductor is placed in parallel with the top switch and it is considered to have very small equivalent parallel capacitance (EPC). Nonetheless, this capacitance will be taken into consideration during this study, because it is considered a parasitic element that can influence the switching of the devices significantly. The inductor current is modeled as a current source during the switching transition and the parasitic inductances induced by the PCB will be denoted as Ldr_{loop} for the driving loop inductance and Lp_{loop} for the power loop inductance. The gate resistance Rg is the sum of the internal resistance of the low-voltage Si MOSFET, the gate driver output resistance and any external resistance added from the designer. The equivalent circuit that will be studied is shown in the figure 3.4 below:

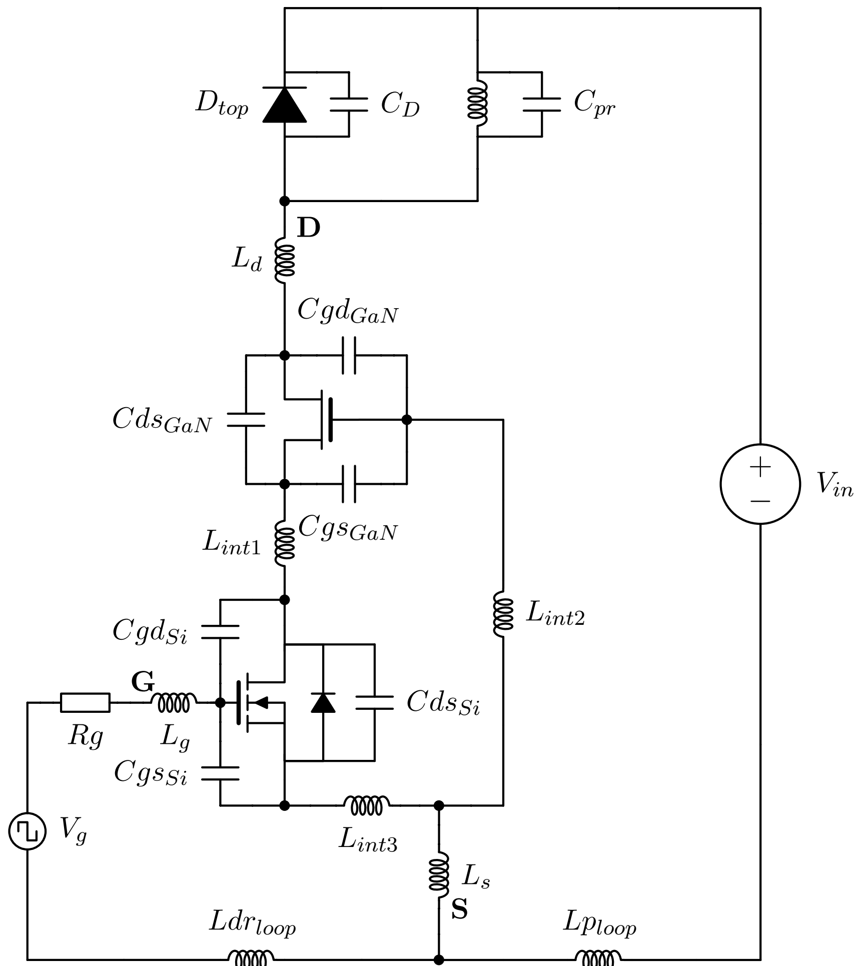


Figure 3.4: Equivalent circuit to analyze the switching loss of the cascode GaN HEMT

3.2.1 Turn-on transition

The turn-on transition will be studied first. The DUT is considered off and the current is freewheeling through the top diode. At the moment, the DUT is turned-on, the inductor current is at the desired value (I_L) and the applied voltage V_{in} is across the DUT. The turn-on transition can be divided into six or five staged, based on whether the top switch has reverse recovery charge (Q_{rr}) or not, respectively. Equivalent circuit and the corresponding equations will be shown for each stage.

***Stage I*: Si MOSFET turn-on delay period**

When the gate signal V_g is applied to the gate of the DUT, the C_{iss} of the Si MOSFET is charged through the R_g. However, the Cgs_{Si} is much larger than the Cgd_{Si} and it is assumed that all the gate current charges the Cgs_{Si} during this stage. The Si MOSFET will not leave the cut-off region until its gate-source voltage ($u_{gs_{Si}}$) reaches the threshold voltage Vth_{Si}. Likewise, the GaN is open circuit and there is no current flowing in the circuit. Consequently, the power stage doesn't change during this stage and the load current is still circulating through the freewheeling diode. The equations for this stage are derived from the equivalent circuit shown in the figure 3.5:

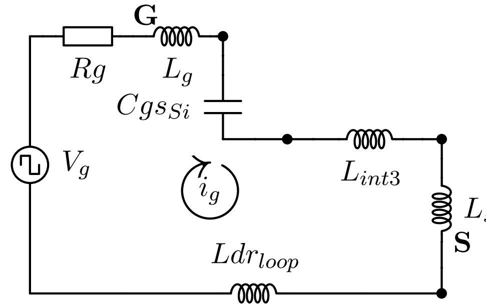


Figure 3.5: Equivalent circuit during stage I of turn-on transition

$$V_g = (Lg + L_{int3} + Ls + Ldr_{loop})\frac{di_g}{dt} + Rg \cdot i_g + u_{gs_{Si}} \tag{3.1}$$

$$i_g = Cgs_{Si}\frac{du_{gs_{Si}}}{dt} \tag{3.2}$$

The laplace and the inverse laplace transformation are performed in order to get the equation for the gate-source voltage. This stage ends when the $u_{gs_{Si}}$ reaches the threshold voltage Vth_{Si}.

***Stage II*: Si MOSFET drain-source voltage Falling period**

When the threshold voltage Vth_{Si} is reached, the Si MOSFET enters the saturation region and its channel starts conducting. The channel current discharges the Cds_{Si} and Cgd_{Si} and the drain-source voltage of the MOSFET ($u_{ds_{Si}}$) decreases. As can be seen from figure 3.1, the Cgs_{GaN} is connected in parallel with the Cds_{Si} and it is also discharged through the interconnection parasitic inductors L_{int1}, L_{int2}, and L_{int3}.

The GaN transistor is still an open circuit and there is no current flowing through the device. The purpose of the cascode structure, as explained in section 2.3.1, is to control the on/off state of the GaN by controlling the Si MOSFET. However, the induced voltages on these parasitic inductors, due to the high di/dt, slow down the increase of the gate-source voltage of the GaN ($u_{gs_{GaN}}$) compared to the decrease of the $u_{ds_{Si}}$ [76]. As these inductors only add a delay to the $u_{gs_{GaN}}$, they will be neglected in this study because they increase the complexity of the equations significantly. Thus, it is assumed that during this stage the $u_{gs_{GaN}}$ follows the fall of the $u_{ds_{Si}}$.

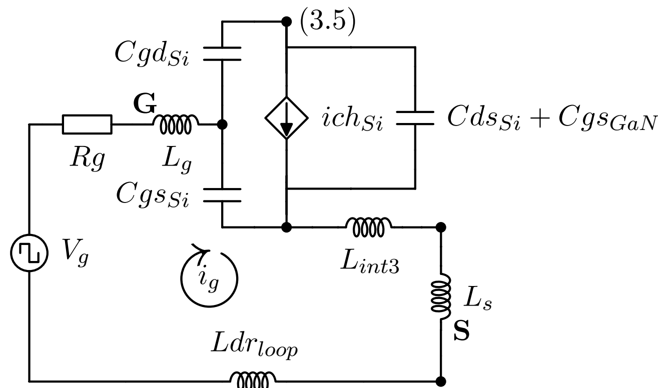


Figure 3.6: Equivalent circuit during stage II of turn-on transition

The interconnection parasitic inductors are neglected and the equivalent circuit for this stage is given in the figure 3.6. The equations derived from this circuit are shown below and by performing the laplace and the inverse laplace transformation, the gate-source and drain-source voltages of the Si MOSFET can be calculated.

$$V_g = (Lg + L_{int3} + Ls + Ldr_{loop})\frac{di_g}{dt} + Rg \cdot i_g + u_{gs_{Si}} \tag{3.3}$$

$$i_g = Cgs_{Si}\frac{du_{gs_{Si}}}{dt} + Cgd_{Si}\frac{d(u_{gs_{Si}} - u_{ds_{Si}})}{dt} \tag{3.4}$$

$$gm_{Si} \cdot (u_{gs_{Si}} - Vth_{Si}) = Cgd_{Si}\frac{d(u_{gs_{Si}} - u_{ds_{Si}})}{dt} - (Cds_{Si} + Cgs_{GaN})\frac{du_{ds_{Si}}}{dt} \tag{3.5}$$

The gate-source voltage of the GaN is given by the drain-source voltage of the MOSFET with a negative sign and this stage ends when it reaches the threshold voltage Vth_{GaN}.

Stage III: GaN channel current Rising period

When the threshold voltage Vth_{GaN} is reached, the GaN HEMT channel starts conducting and the channel current (ich_{GaN}) discharges the Cds_{GaN} and Cgd_{GaN}, causing the drain-source voltage of the GaN HEMT ($u_{ds_{GaN}}$) to decrease. Due to this fall in the $u_{ds_{GaN}}$, the current starts to transfer from the diode through the DUT, causing the drain current i_{Ld} to increase. Regarding the MOSFET, its $u_{gs_{Si}}$ continues to increase while the $u_{ds_{Si}}$ will drop to zero. Thus, the MOSFET can be considered as operating in the ohmic region during this stage and it will represented as a resistance (Rch_{Si}). As the MOSFET doesn't influence the switching process significantly, the GaN can be studied separately. At this point,

current is flowing trough the cascode structure and the parasitic inductance L_{int1} should be taken in consideration as it acts as source inductance for the GaN. The equivalent circuit during this stage is shown in figure 3.7, from which the following equations are derived:

$$u_{gs_{GaN}} + (L_{int1} + L_{int2} + L_{int3})\frac{dig_{GaN}}{dt} + (L_{int1} + L_{int3})\frac{di_{Ld}}{dt} + Rch_{Si}(ig_{GaN} + i_{Ld}) = 0 \quad (3.6)$$

$$ig_{GaN} = Cgs_{GaN}\frac{du_{gs_{GaN}}}{dt} + Cgd_{Si}\frac{d(u_{gs_{GaN}} - u_{ds_{GaN}})}{dt} \quad (3.7)$$

$$gm_{GaN}(u_{gs_{GaN}} - Vth_{GaN}) = Cgd_{GaN}\frac{d(u_{gs_{GaN}} - u_{ds_{GaN}})}{dt} - Cds_{GaN}\frac{du_{ds_{GaN}}}{dt} + i_{Ld} \quad (3.8)$$

$$(L_{int1} + L_{int3} + Ld + Ls + Lp_{loop})\frac{di_{Ld}}{dt} + (L_{int1} + L_{int3})\frac{dig_{GaN}}{dt} + Rch_{Si}(ig_{GaN} + i_{Ld}) + u_{ds}GaN = Vin \quad (3.9)$$

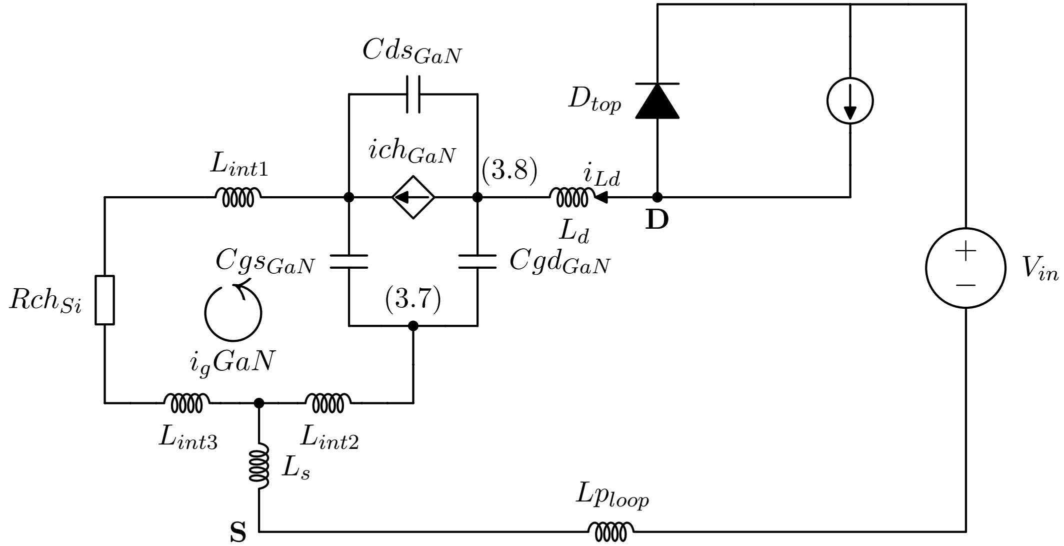


Figure 3.7: Equivalent circuit during stage III of turn-on transition

The expressions for the $u_{gs_{GaN}}$ and $u_{ds_{GaN}}$ can be obtained by replacing the ig_{GaN} and i_{Ld} from equations 3.7 and 3.8, respectively, into the equations 3.6 and 3.9. Again, the laplace and inverse laplace transformation are used to solve the system of the differential equations. Once the expressions for the $u_{gs_{GaN}}$ and $u_{ds_{GaN}}$ are known, the i_{Ld} is calculated by the equation 3.8. This stage ends when the inductor current I_L is reached.

***Stage IV*: Reverse recovery charge of the top switch**

During the turn-on transition of the DUT, the top switch should be able to block the voltage. The increase in the voltage across the top switch should start when the i_{Ld} reaches the I_L. However, when an active switch with reverse recovery charge (Q_{rr}) is used, this cannot happen until the reverse recovery charge of the top switch is removed. Consequently, when the i_{Ld} reaches the I_L, the reverse recovery process begins. This additional charge is translated as a further increase in the current through the DUT, as well as an increase in the transition time.

The equivalent circuit for this stage remains the same as in figure 3.7. Thus, the equations are also the same but they have different initial conditions. The increase in the i_{Ld} will continue until the reverse recovery process is complete. Calculating the Q_{rr} is not an easy task, since it is related to the inductor current I_L and the current slew rate at the moment when i_{Ld} equals the I_L, which is determined basically from the loop inductance. The Q_{rr} given in the device datasheet is calculated under specific conditions, which are usually not applicable due to small di/dt. Thus, the value of the current (I_{rr}) due to the reverse recovery will be calculated as follows:

$$Q_{rr} = \frac{Q_{rr,datasheet}}{I_{rr,datasheet}} \cdot I_L$$

$$I_{rr} = \sqrt{\frac{di_{Ld}}{dt} \cdot Q_{rr}}$$

This rapidly increased current will flow through the parasitic inductor L_{int1} inducing a voltage across it, which slows down the $u_{gs_{GaN}}$. This will cause the GaN HEMT channel to saturate during this stage and the $u_{ds_{GaN}}$ to increase rather continue decreasing. This stage ends when the i_{Ld} reaches the value $I_L + I_{rr}$. Finally, when the top device has no Q_{rr}, this stage is skipped, which is the case for this thesis project.

***Stage V*: GaN drain-source voltage Falling period**

When the reverse recovery process is complete, the top switch is able to block the voltage. The increase in the voltage stands for the charging process of the junction capacitance of the top switch (C_D). This is actually the reason, why switches with no Q_{rr} introduce a reverse-recovery-like current. The parasitic capacitor of the inductor (C_{pr}) is effectively in parallel with the junction capacitance of the top switch and thus it is also charged during this stage. As the voltage across the top switch increases, the $u_{ds_{GaN}}$ of the DUT can continue falling till it reaches zero, concluding the turn-on switching transition. The charging current of the C_D and C_{pr} is added to the I_L, increasing the overshoot of the current through the DUT. The equivalent circuit for this stage is shown in figure 3.8.

This stage is supposed to end when the $u_{ds_{GaN}}$ drops to zero. However, it is considered the most complicated since the voltage across the DUT decreases while at the same time the voltage across the top switch increases. The junction capacitances of these devices are voltage dependent and their value changes during this stage. Since the non-linearity of the capacitances is modeled by using discrete values based on the voltage range, this

stage will be divided into two sub-stages with the same equations but with different values for the capacitances.

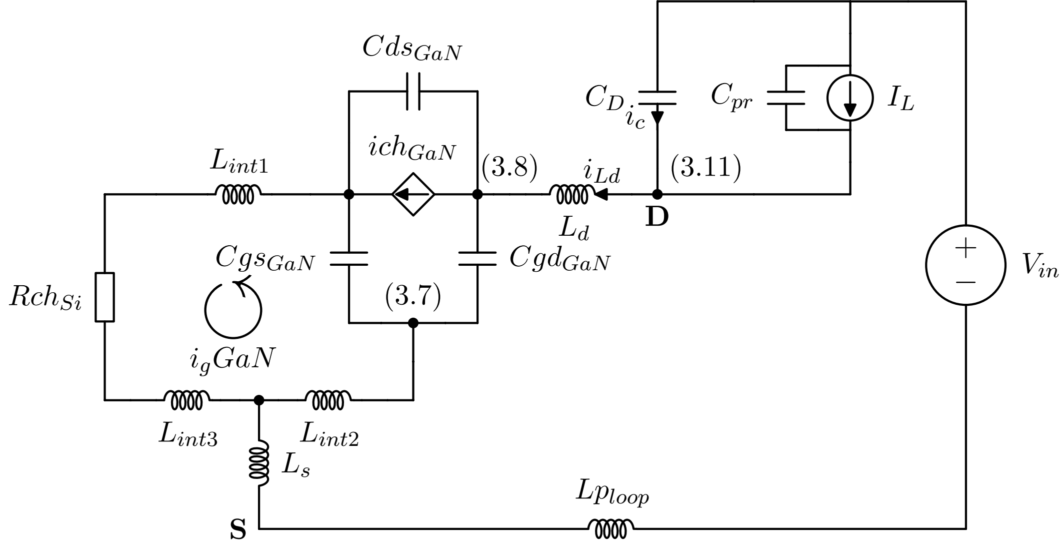


Figure 3.8: Equivalent circuit during stage V of turn-on transition

The equations 3.6, 3.7, and 3.8 are still valid for this stage, while equation 3.9 changes as indicated below, and equation 3.11 is added to them:

$$(L_{int1} + L_{int3} + Ld + Ls + Lp_{loop})\frac{di_{Ld}}{dt} + Rch_{Si}(ig_{GaN} + i_{Ld}) + (L_{int1} + L_{int3})\frac{dig_{GaN}}{dt} + u_{ds_{GaN}} + u_D = Vin \quad (3.10)$$

$$i_{Ld} = I_L + (C_D + C_{pr})\frac{du_D}{dt} \quad (3.11)$$

As stated above, the overshoot in the current, when there is no Q_{rr} in the top switch, is generated by the charging process of the junction capacitance of the top switch and the parasitic capacitance of the inductor. Thus, the first sub-stage of this model calculates the peak value of the current based on the total capacitive charge of the top switch given in the device's datasheet and a part of the charge from the externally added capacitance in parallel with the inductor. When the drain current i_{Ld} reaches this value, the first sub-stage ends. In the second sub-stage, the same equations are used, while the values of the junction capacitance Cds_{GaN} and C_D change. This sub-stage ends when $u_{ds_{GaN}}$ drops to zero and so does stage V. This assumption will introduce a discontinuity in the waveforms, but it is considered tolerable.

It is assumed at this point that since the $u_{ds_{GaN}}$ collapses to zero very fast, the parasitic capacitance of the inductor will not get fully charged on this small interval. This becomes more obvious as the value of this capacitance increases (see chapter 5). Thus, only part of the parasitic capacitance is considered to contribute to the current's overshoot and the rest will get charged in the next stage.

***Stage VI*: Current ringing period**

When the $u_{ds_{GaN}}$ reaches zero, the parasitic capacitances of the top switch and the inductor resonate with the parasitic inductances in the circuit and the current ringing period begins. The $u_{gs_{GaN}}$ increases to zero and the $u_{gs_{Si}}$ exponentially increases to the gate voltage V_g. Normally, the ringing will be damped long before the $u_{gs_{Si}}$ reaches the gate voltage, but, as it will be shown later on, the parasitic capacitance of the inductor has a significant impact during this stage. The equivalent circuit used during this stage is shown in figure 3.9, followed by the equation used for the current.

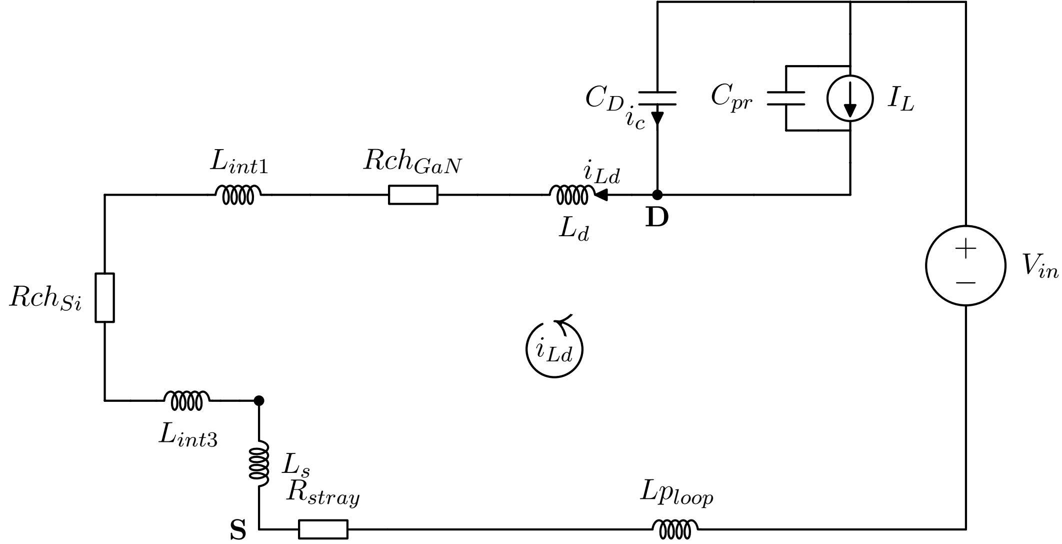


Figure 3.9: Equivalent circuit during the ringing period of turn-on transition

$$(L_{int1} + L_{int3} + Ld + Ls + Lp_{loop})\frac{di_{Ld}}{dt} + (Rch_{Si} + Rch_{GaN} + R_{stray})i_{Ld} + \frac{1}{(C_D + C_{pr})} \cdot \int (i_{Ld} - I_L)dt = V_{in} \quad (3.12)$$

This stage is considered to be valid as long as the gate voltage pulse is on. In reality, the inductor current will continue to increase till the next turn-off transition, but in this study it is considered to be equal to the desired I_L.

3.2.2 Turn-off transition

Before the turn-off transition occurs, the current is flowing through the DUT and the top switch is blocking the voltage. When the inductor current reaches the desired value, the DUT is turned off. The turn-off transition is divided in five stages. Equivalent circuit and the corresponding equations for each stage will be shown in this section.

***Stage I*: Si MOSFET tun-off delay period**

When the gate voltage drops to zero, the Si MOSFET still operates in the ohmic region. The C_{iss} of the Si MOSFET is being discharged through the R_g. The equivalent circuit for this stage is given in figure 3.10 followed by the equations derived from it.

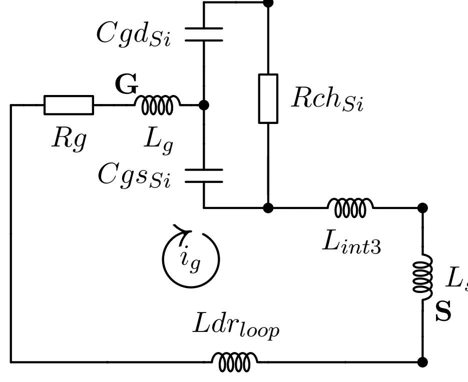


Figure 3.10: Equivalent circuit during stage I of turn-off transition

$$0 = (Lg + L_{int3} + Ls + Ldr_{loop})\frac{di_g}{dt} + Rg \cdot i_g + u_{gs_{Si}} \tag{3.13}$$

$$i_g = (Cgs_{Si} + Cgd_{Si})\frac{du_{gs_{Si}}}{dt} \tag{3.14}$$

The gate-source voltage of Si MOSFET is calculated through the laplace and inverse laplace transformations. This stage ends when the channel current reaches the inductor current and the $u_{gs_{Si}}$ reduces to V_{miller} according to the equation:

$$gm_{Si} \cdot (u_{gs_{Si}} - Vth_{Si}) = I_L \tag{3.15}$$

Normally, the $u_{ds_{Si}}$ voltage rises to the V_{miller} and the MOSFET begins to operate in the saturation region [69]. However, in this study, the MOSFET will enter the saturation region when this stage ends, while the drain source voltage is still zero.

Stage II: Si MOSFET drain-source Rising period

During this stage, the Si MOSFET operates in the saturation region and as the $u_{gs_{Si}}$ continues to decrease, the channel current reduces below the I_L value. On the other hand, the GaN transistor is still fully turned on and the whole inductor current is flowing through it. This difference between the ich_{Si} and the I_L will charge the Cds_{Si}. Similar to its turn-on counterpart (stage II), the Cgs_{GaN} will be charged as it is connected in parallel to the Cds_{Si} through the interconnection parasitic inductances. Again, these interconnection inductances will be neglected since they only introduce a phase delay to the $u_{gs_{GaN}}$. Thus, the $u_{gs_{GaN}}$ is assumed to follow the increase of the $u_{ds_{Si}}$.

The equivalent circuit is given in figure 3.11 and the equations for this stage are the following:

$$0 = (Lg + L_{int3} + Ls + Ldr_{loop})\frac{di_g}{dt} + Rg \cdot i_g + u_{gs_{Si}} \tag{3.16}$$

$$i_g = Cgs_{Si}\frac{du_{gs_{Si}}}{dt} + Cgd_{Si}\frac{d(u_{gs_{Si}} - u_{ds_{Si}})}{dt} \tag{3.17}$$

$$gm_{Si} \cdot (u_{gs_{Si}} - Vth_{Si}) = Cgd_{Si}\frac{d(u_{gs_{Si}} - u_{ds_{Si}})}{dt} - (Cds_{Si} + Cgs_{GaN})\frac{du_{ds_{Si}}}{dt} + I_L \quad (3.18)$$

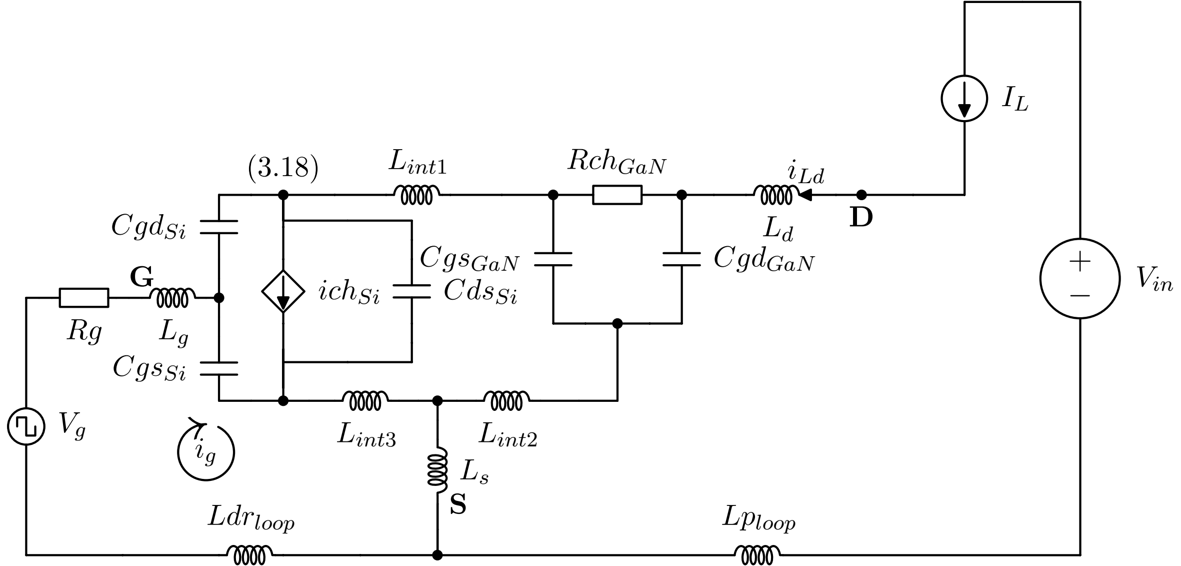


Figure 3.11: Equivalent circuit during stage II of turn-off transition

The expressions for the $u_{gs_{Si}}$ and $u_{ds_{Si}}$ are calculated by solving the system of the differential equations above, through the laplace and inverse laplace transforms. The expression for the $u_{gs_{GaN}}$ is given by the $u_{ds_{Si}}$ with a negative sign. This stage ends when the channel current of the GaN equals the I_L and the gate-source voltage of the GaN reaches the miller value, according to the equation:

$$gm_{GaN} \cdot (u_{gs_{GaN}} - Vth_{GaN}) = I_L \quad (3.19)$$

Stage III: GaN channel current Decreasing period

As the GaN transistor has entered the saturation region, the further decrease in the $u_{gs_{GaN}}$ will cause the channel current ich_{GaN} to become less than the I_L. This difference in the current will start charging the Cds_{GaN} and the $u_{ds_{GaN}}$ will eventually start increasing. Regarding the Si MOSFET, it is modeled as a non-linear capacitor in parallel with the Cgs_{GaN}, as the $u_{gs_{Si}}$ is very likely to drop below the threshold voltage during stage II. The $u_{gs_{Si}}$ continues to decrease during this stage until it drops to zero.

As the $u_{ds_{GaN}}$ increases, the voltage across the top switch start to decrease and its junction capacitance gets discharged. This additional current is added to the inductor current I_L. The total current (i_{Ld}) that flows through the cascode structure keeps charging the Cds_{Si}, Cgd_{Si} and discharging the Cgs_{GaN}. Thus, $u_{ds_{Si}}$ increases rapidly, and accordingly $u_{gs_{GaN}}$ decreases very quickly. The equivalent circuit during turn-off Stage III is shown in figure 3.12 and the corresponding equations are:

$$i_{Ld} = I_L + (C_D + C_{pr})\frac{du_D}{dt} \quad (3.20)$$

$$(Ld + Ls + L_{int3}Lp_{loop})\frac{di_{Ld}}{dt} + u_{ds_{GaN}} - u_{gs_{GaN}} + u_D = V_{in} \quad (3.21)$$

$$(Cgs_{GaN} + Cds_{Si} + Cgd_{Si})\frac{du_{gs_{GaN}}}{dt} + Cgd_{GaN}\frac{d(u_{gs_{GaN}} - u_{ds_{GaN}})}{dt} = -i_{Ld} \quad (3.22)$$

$$gm_{GaN}(u_{gs_{GaN}} - Vth_{GaN}) = Cgd_{GaN}\frac{d(u_{gs_{GaN}} - u_{ds_{GaN}})}{dt} - Cds_{GaN}\frac{du_{ds_{GaN}}}{dt} + i_{Ld} \quad (3.23)$$

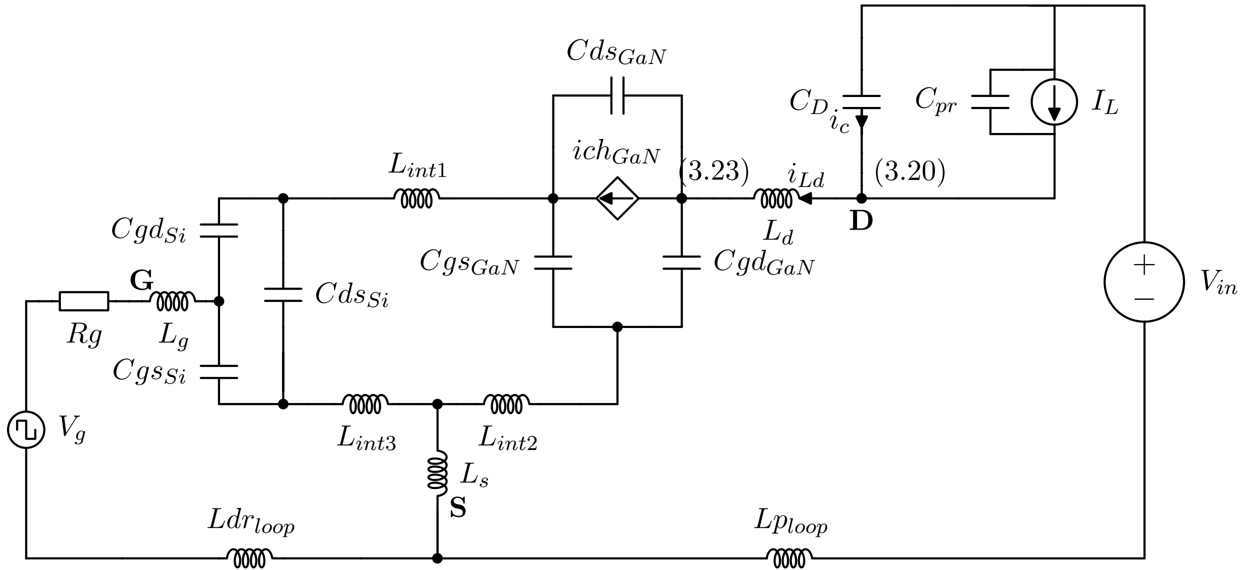


Figure 3.12: Equivalent circuit during stage III of turn-off transition

The expressions for the $u_{gs_{GaN}}$ and $u_{ds_{GaN}}$ are obtained by performing the laplace and inverse laplace transformations in the system of differential equations given above. This stage ends when the channel current ich_{GaN} drops to zero. This happens very quickly because the intrinsic current source driving mechanism shortens the GaN HEMT channel current falling time, which is unique to the cascode configuration.

***Stage IV*: GaN drain-source Rising period**

When the stage III ends, the GaN transistor channel is totally shut down, the remaining current keeps charging the junction capacitors of the cascode GaN transistor. Meanwhile, the voltage across the freewheeling diode decreases, and the inductor current transfers from the top switch to the bottom switch. The equivalent circuit during turn-off Stage IV is shown in figure 3.13. In fact, the voltage across the interconnection inductance has no significant impact during this stage, but it makes the circuit order too high for a mathematical solution. Therefore, the internal parasitic inductors are already removed from the figure below. The key equations different from stage III are shown as follows:

$$(Cgs_{GaN} + Cds_{Si} + Cgd_{Si})\frac{du_{gs_{GaN}}}{dt} = Cgd_{GaN}\frac{du_{ds_{GaN}}}{dt} \quad (3.24)$$

$$i_{Ld} = Cgd_{GaN}\frac{d(u_{gs_{GaN}} - u_{ds_{GaN}})}{dt} + Cds_{GaN}\frac{du_{ds_{GaN}}}{dt} \tag{3.25}$$

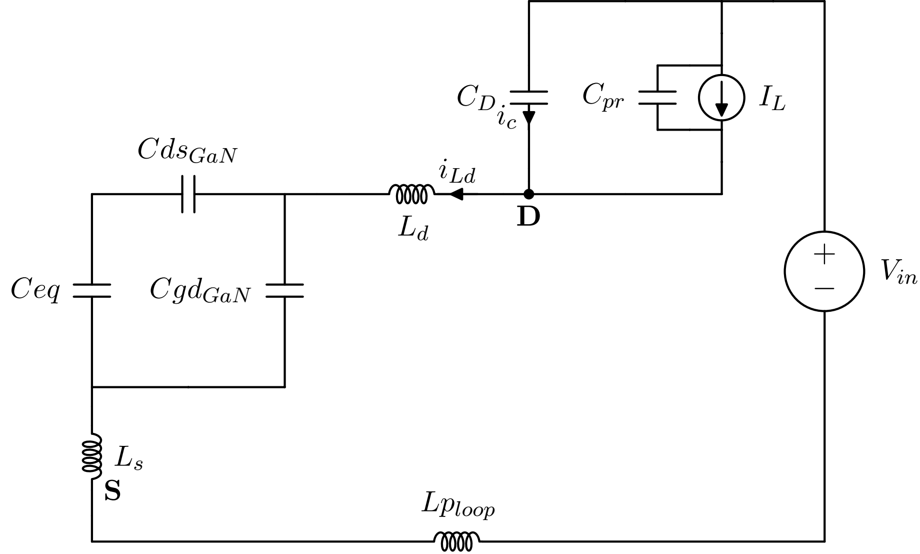


Figure 3.13: Equivalent circuit during stage IV of turn-off transition

, where C_{eq} equals $Cgs_{GaN} + Cds_{Si} + Cgd_{Si}$. The expressions for the $u_{ds_{GaN}}$ and i_{Ld} are obtained by performing the laplace and inverse laplace transformations in the system of differential equations given above. The stage ends when voltage across the top switch decreases to zero and the freewheeling diode is forward biased.

Stage V: Current and voltage ringing period

When voltage across the top switch decreases to zero and the freewheeling diode is forward biased the current ringing period begins. The value of the current i_{Ld} at the end of the previous stage determines the remaining energy of the parasitic inductors and, eventually, the overshoot of voltage across the cascode GaN transistor $u_{ds_{GaN}}$. The schematic remains the same as in the previous stage and the equation used is:

$$(Ld + Ls + Lp_{loop})\frac{di_{Ld}}{dt} + (Rch_{Si} + Rch_{GaN} + R_{stray})i_{Ld} + \frac{1}{C_{ringing}} \cdot \int (i_{Ld})dt = V_{in} \tag{3.26}$$

,where $C_{ringing}$ is the $Cds_{GaN} + Cds_{Si} + Cgd_{Si} + C_{pr}$.

3.2.3 Calculated results of the analytical model

For this thesis project, the analytical model assumes that the top switch has zero Q_{rr} and thus, the stage IV of the turn-on switching transition is skipped. Specifications of the SiC Schottky diode from CREE with part number C3D04060A were used and the 400V/5A conditions were chosen to be presented. The inductor's EPC does not influence the switching transitions at this point. The stages of switching transitions, as discussed above, are indicated in the waveforms of the drain-source voltage and drain current calculated by the proposed analytical model and shown below. In turn-off switching transition, the channel current (red waveform) is also used as it is responsible for the stage III of the turn-off transition.

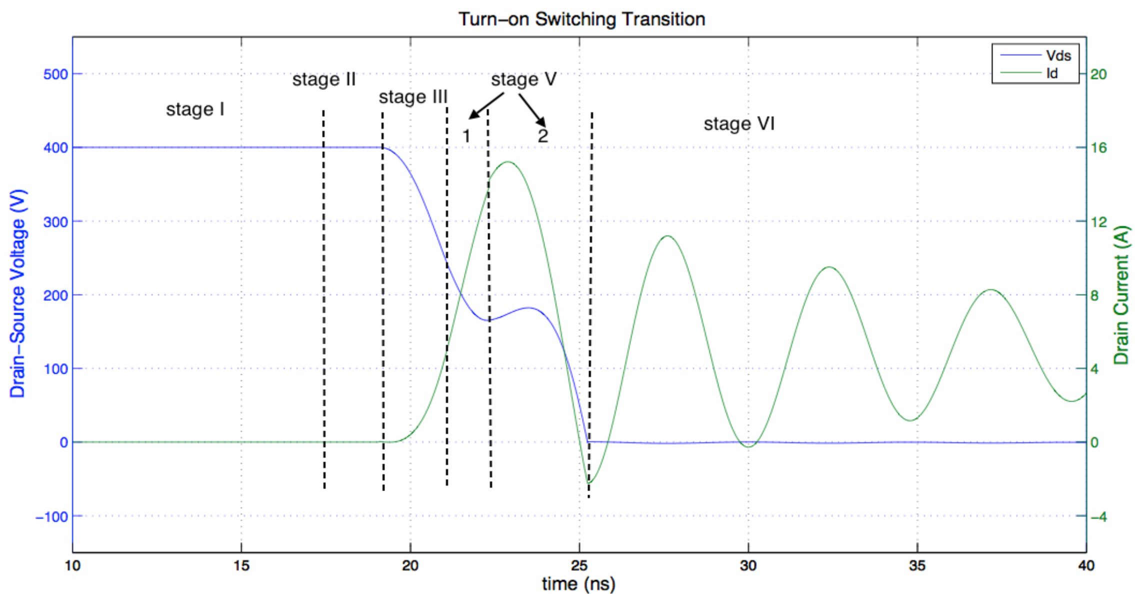


Figure 3.14: Stages during turn-on switching transition

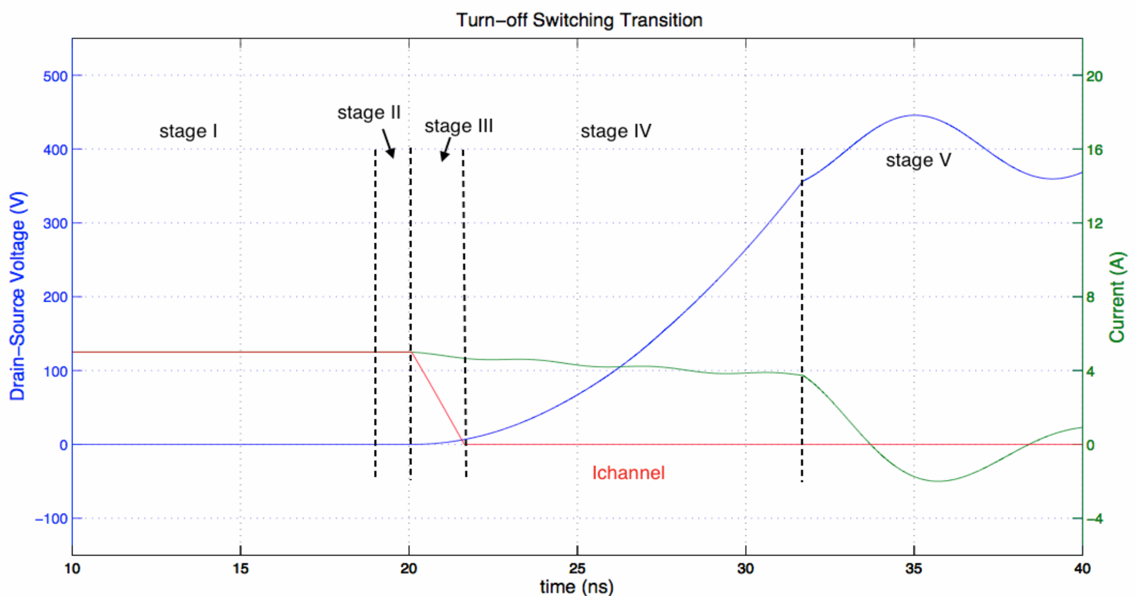


Figure 3.15: Stages during turn-off switching transition

The full waveforms of the drain-source voltage and drain current of the DUT calculated by the proposed analytical model during the turn-on and turn-off switching transitions as will be used in the next chapter for comparison with the experimental results are shown below:

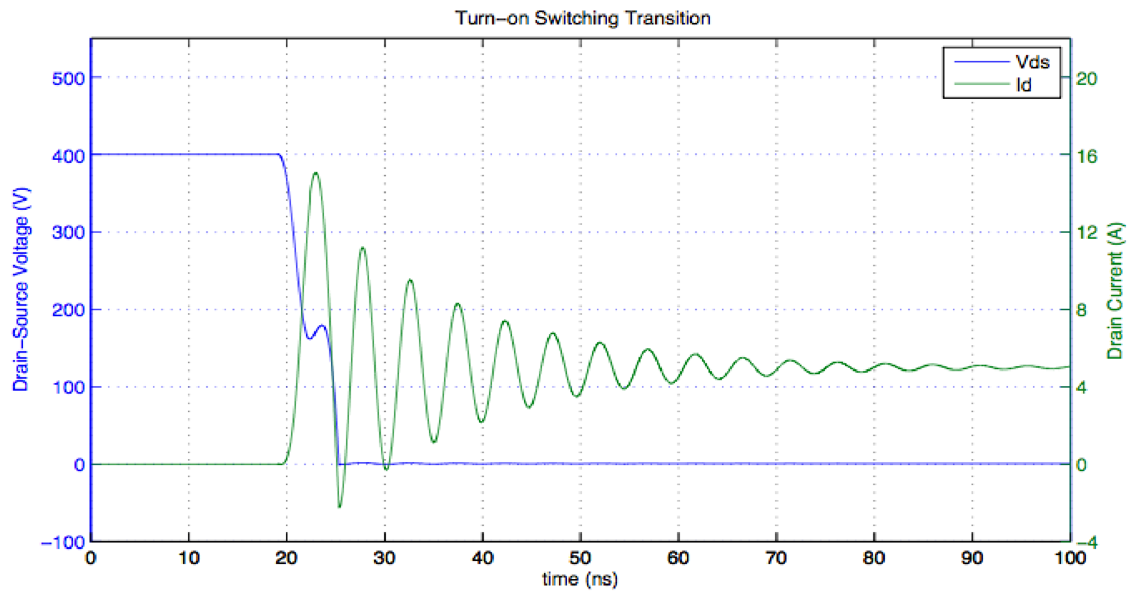


Figure 3.16: Turn-on switching transition at 5A

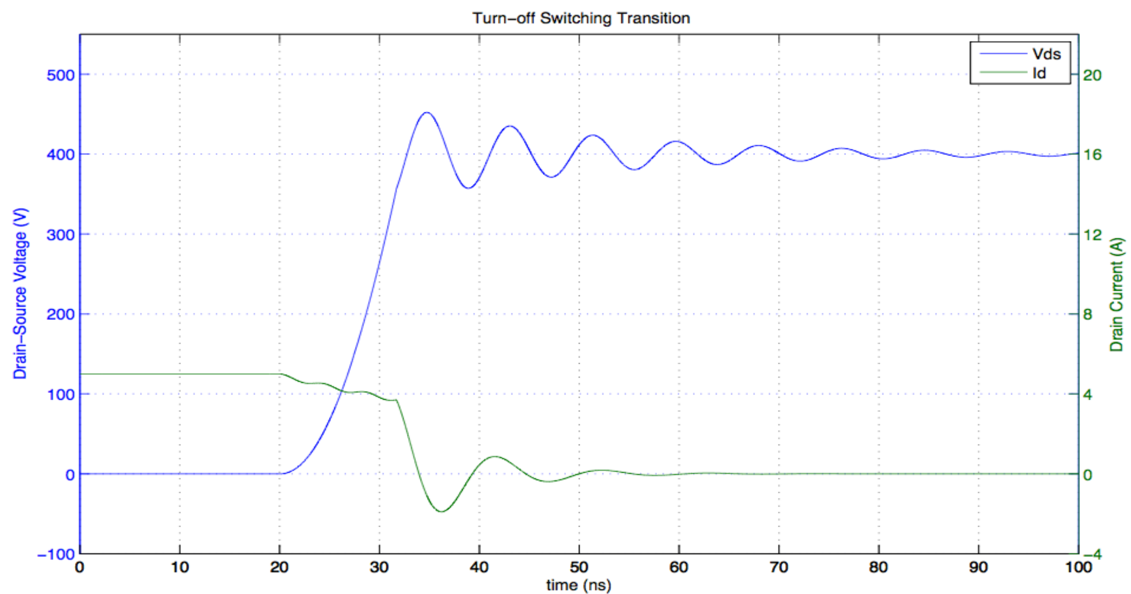


Figure 3.17: Turn-off switching transition at 5A

3.3 Investigation of package parasitic inductances influence

Due to intrinsic material properties of the GaN (see section 2.3), the cascode GaN HEMT shows advanced behavior and is able to switch with very high frequency. However, at higher frequencies, the parasitic inductances introduced by the package of the device (figure 3.1) will cause large switching losses and oscillations during the switching transitions.

The influence of the package's parasitics on the switching transitions of the Si MOSFET is being studied for many years showing that the common-source inductance (CSI), which is defined as the inductance shared by the driving and power loop, is of great importance [64], [69]. The CSI acts as negative feedback slowing down the driver of the device during the turn-on and turn-off switching transitions. This mechanism prolongs the voltage and current crossover time causing a significant increase in the switching loss. Recent studies on the package influence for the wide-bandgap devices, such as high-voltage SiC MOSFET [71] and low-voltage GaN HEMT [56], has led to similar conclusions, due to the fact that all these devices use a single-switch structure. Consequently, the CSI is proven to have the biggest impact on the device's switching loss. However, the unique structure of the cascode GaN HEMT makes the definition of the CSI complicated and the conclusions of the above publications are no more applicable.

Z. Liu in [74] investigated the influence of the cascode GaN HEMT's package parasitics by defining the CSI of the low-voltage Si MOSFET and the high-voltage GaN HEMT separately (see figure 3.18). Both devices share the same power loop (blue loop), while they have different driving loops, the red loop is the Si MOSFET's driving loop and the green loop is the GaN HEMT's driving loop. It can be seen that for the Si MOSFET, the CSI consists of the inductances L_{int3} and L_s, while from the prospective of the GaN HEMT, the CSI is formed by the L_{int3} and L_{int1}. Consequently, the L_{int3} is considered to be the most critical parasitic inductance as it is CSI for both the GaN HEMT and the Si MOSFET. Next, the L_{int1} is considered the second-most critical inductance as it is the CSI for the GaN HEMT. Finally, the L_s is considered as the third most important.

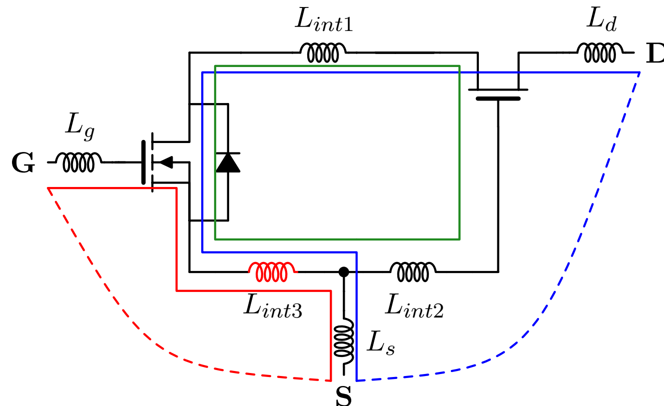
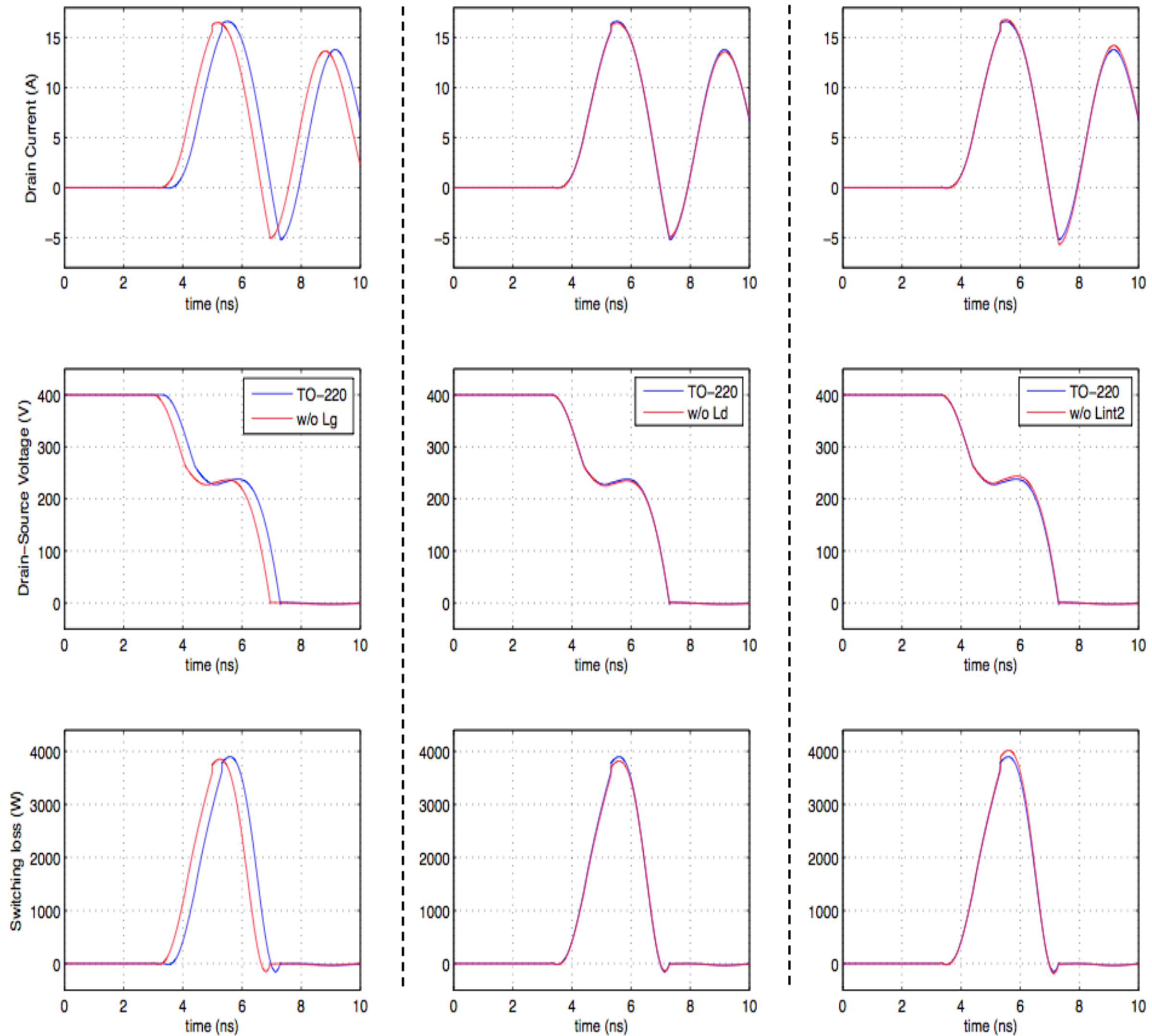


Figure 3.18: Identification of the critical parasitic inductances of the cascode GaN HEMT. The blue loop is the power loop, the red loop is the driving loop of the Si MOSFET and the green loop is the GaN HEMT driving loop

The proposed analytical model can be used to verify the above theoretical analysis. The DPT circuit will be used, where the GaN HEMT is working under hard-switching conditions. The turn-on switching loss is the dominant part of the switching loss during the hard-switching operation. Thus, the turn-on energy under 400V/5A conditions is chosen for comparison. In the figures below, the turn-on switching of the TO-220 package will be used as basis (blue waveform) and each one of the parasitic inductances will be removed in order to evaluate its impact on the switching loss (red waveform).

By comparing waveforms, we can observe the different influence of each parasitic inductance on the turn-on switching transition. Without the L_d, the waveforms are almost the same, while by removing the L_g, a forward phase shift for the current and voltage waveforms is observed, but no significant difference regarding the turn-on energy. The absence of L_{int2} causes a small increase in the turn-on energy, but it can be considered inaccurate because its influence is neglected through the stage II of the turn-on transition. On the other hand, without L_{int1} and L_{int3}, the I_{ds} has slightly higher peak value and the V_{ds} drops to zero faster causing smaller crossover time and consequently turn-on energies. Finally, setting the L_s equal to zero does not lead to the desired results, since a reduction in the turn-on loss was expected.



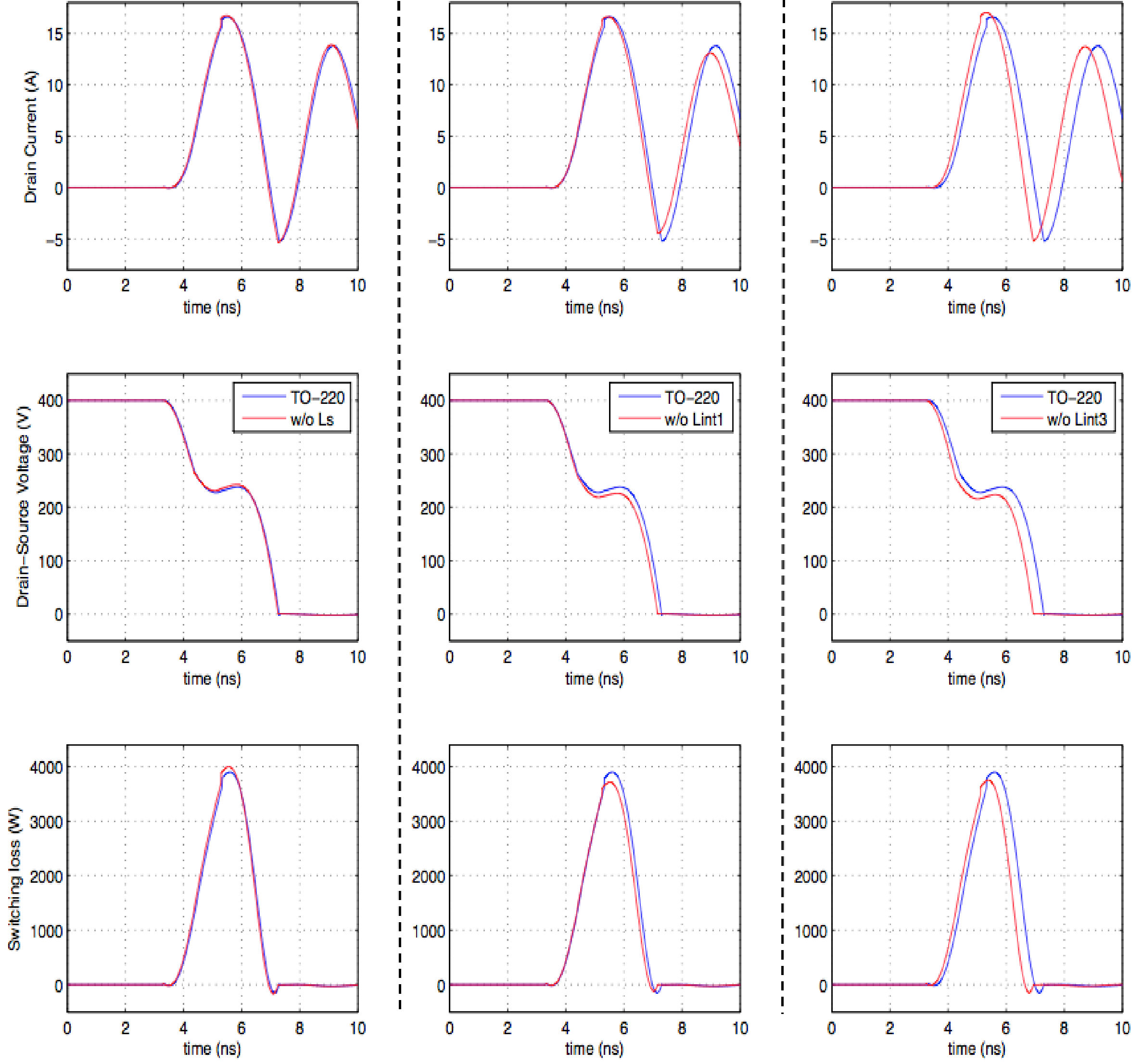


Figure 3.19: Impact of the package parasitic inductances on the turn-on switching energy under 400V/5A conditions

In order to better understand the influence of the package parasitic inductances on the turn-on switching loss, a comparison of the turn-on energy is shown in figure 3.20. The turn-on energy for the TO-220 package is $7\mu J$ under 400V/5A conditions. By setting the L_g and L_d equal to zero, the reduction of turn-on switching loss is 1.4% and 1.6% of the $7\mu J$, respectively, which can be considered negligible. On the other hand, when the parasitic inductance L_{int1} and L_{int3} are removed, the turn-on switching loss reduce significantly (7.1%, and 12.9% of $7\mu J$, respectively). Furthermore, considering that the values of these inductances are less than 1nH (see table 3.1), the percentage of the increase in the switching loss is considered significant. The impacts of the L_{int2} and L_s are not included in the comparison because their results can not be considered valid.

Consequently, it is observed that the results calculated by the proposed analytical model confirm the above discussion, and the parasitic inductance L_{int1} and L_{int3} are proven to be the most critical package parasitic inductances.

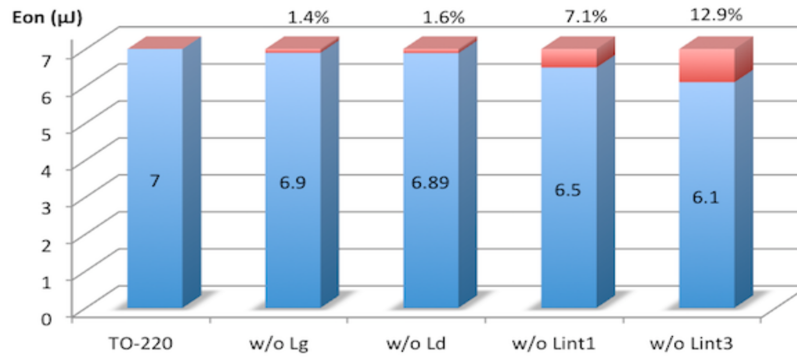


Figure 3.20: Comparison of the turn-on energy

3.4 Discussion

This chapter has focused on the characterization of the high-voltage GaN HEMT in cascode configuration and on the development of an analytical loss model in order to calculate the switching loss under the condition of clamped inductive load by means of a DPT circuit.

Section 3.1 analyzes of the GaN HEMT device, regarding its parasitic elements and, also, the basic assumption of this model is mentioned. Section 3.2 develops the equations that describe each stage of the switching transitions and presents the calculated voltage and current waveforms. Moreover, the influence of the inductor's parasitic capacitance is taken into consideration in the development of these equations, but the results will be presented in the next chapter in order to make the comparison clearer for the reader. Finally, section 3.3 uses the proposed analytical model to investigate the influence of the package parasitic inductances on the switching transitions of the device. The results confirmed the analysis made in the same section, regarding the importance of each one of the package parasitic inductances.

Chapter 4

Measurements in high frequency power electronics applications

In order to accurately determine the switching power losses of the power switches, current and voltage measurements need to be conducted during the turn-on and turn-off switching transients. However, power switches are characterized by very high current and voltage rates of change, making the gathering of accurate measurements during their switching transitions a challenge. Therefore, high performance voltage and current measurement equipment has to be used.

Due to the different oscilloscope measurement applications and needs, there is a broad variety of probes that can be used, as well as three issues that should be taken into consideration in order to properly select one: physical attachment, minimum impact on circuit operation and adequate signal fidelity. It is explained thoroughly in [77] how to deal with these issues and how to select the right probe depending on the measurement needs and the application. A short description of the measurement probes will be presented in sections 4.2 and 4.3. Moreover, it is proven that under conditions of very fast switching, the waveform seen in the oscilloscope can be very different from the actual electrical signal of the circuit under test. For this, some issues involved in collecting accurate measurements and limitations regarding the measurement system will be discussed in section 4.1.

4.1 Important Issues in Measurements

4.1.1 Bandwidth Considerations

Bandwidth is the range of frequencies that an oscilloscope or probe is designed for. It is also defined as the point on an amplitude vs frequency plot, where the response of the probe causes a decrease of 3dB to amplitude of the output. At frequencies beyond that point, the measurement results can be unreliable since the signal becomes extremely attenuated. Additionally, all the signals, except the DC and the pure sinusoidal ones, have content of multiple frequencies. The non-sinusoidal signals, such as square-waves and saw-tooth waves, contain high frequency components, which cannot be neglected since with

the fundamental component establish the shape of the rising and falling waveshape's transitions and the edges of the signal. For example, a square wave can be considered as the sum of an infinite Fourier series as shown in figure 4.1. For obtaining accurate measurements, including these high frequency components of the signal, the bandwidth of the oscilloscope should be five times greater than the frequency of the signal being measured [77].

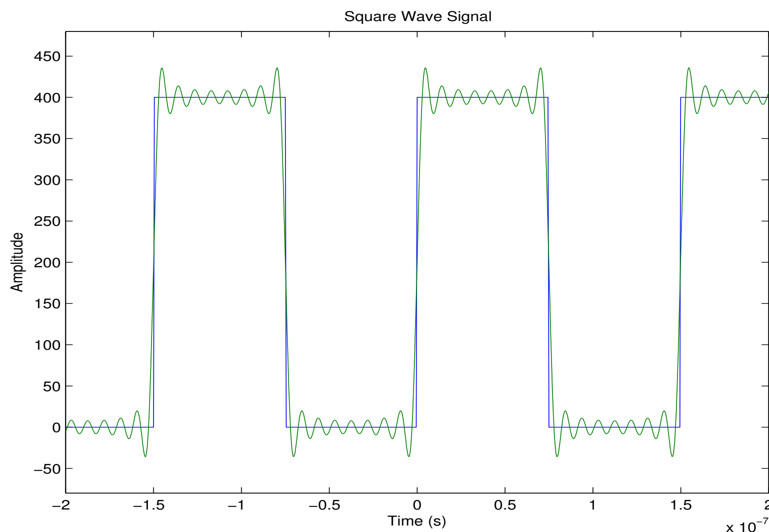


Figure 4.1: A square wave signal consists of many higher frequency components

Similarly, every probe should have an adequate bandwidth in order to be able to capture, with complete fidelity, the fast rise and fall edges during the switching transitions. According to the signal theory, the effective bandwidth of a slope signal with a rise time t_r or fall time t_f can be derived using the formula below [78]:

$$f_{BW} \approx \frac{0.35}{min(t_r, t_f)} \tag{4.1}$$

where, t_r is the time required for the measured signal to rise from 10% to 90% of its nominal value and t_f is the time required for the signal to fall from 90% to 10% of its nominal value. Therefore, the smaller time between the rise and the fall time will determine the bandwidth required for the measuring equipment. According to 4.1, a 5nsec rise time corresponds to 70MHz bandwidth and leaving a five times margin, as mentioned above, the bandwidth of the measuring equipment should be higher than 350MHZ.

Probes should be selected to match or exceed the oscilloscopes bandwidth. However, attaching a probe to an oscilloscope, results into a new system of bandwidth and rise time specifications. The relationship between system bandwidth and the individual scope and probe bandwidths and rise/fall times is complex. For acceptable accuracy in rise/fall time measurements, the bandwidth of the system (probe and scope together) should be three to five times higher than the maximum frequency of the signal measured (considering also the high-frequency content of the signal) [77]. An approximation of the system bandwidth is given by the following formula combining the scope and the probe rise

time [79]:

$$t^2_{r,system} \approx t^2_{r,probe} + t^2_{r,scope} \Rightarrow BW_{system} \approx \frac{1}{\sqrt{\frac{1}{BW^2_{probe}} + \frac{1}{BW^2_{scope}}}} \tag{4.2}$$

This overall bandwidth of the oscilloscope and probe together is, actually, the main limitation and this performance is what determines the measurement equipment's capabilities.

This can also be seen from the figure 4.2 below, where an example of measuring a current with 5nsec rise time while changing the scope's bandwidth is depicted. A coaxial shunt with a 2GHz bandwidth was used together with the Yokogawa DLM2000 mixed signal oscilloscope with a 350MHz bandwidth. As already mentioned above, measuring a signal with 5nsec rise time requires a measuring system with a minimum bandwidth of 350MHz, in order to capture it with adequate fidelity. Using a scope with less bandwidth than required will cause the measured signals to be different than the actual signals, as can be seen in figure 4.2. The waveforms shown by the green and blue arrows were captured with the bandwidth of the scope set at 250MHz and 100MHz, respectively. It can be seen that not only the rise time, but also the peak value of the current changes as the bandwidth reduces. There is also a delay introduced in the measured signal. A measuring system with inadequate bandwidth will lead to inaccurate measurements and the deviations in the captured signals from the actual signal will eventually lead to false calculations of the device's switching losses.

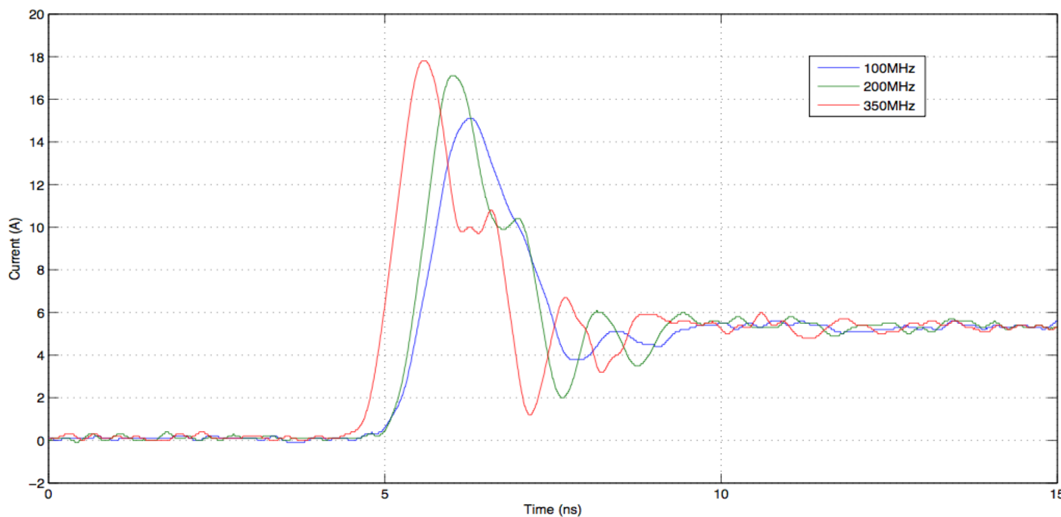


Figure 4.2: Influence of the system's bandwidth in the accuracy of the measurements

4.1.2 V-I Alignment

Another issue that has to be considered when making high frequency measurements is that every type of voltage and current probe, has its own propagation delay. Despite the fact that the difference in the delays between two probes, also known as skew, is in the range of nanoseconds, it can cause severe timing misalignment. When measuring high frequency transients, as in the case of wide-bandgap devices, the timing misalignment can lead to inaccurate calculations of the switching losses [80].

In order to avoid measuring errors, especially when measuring pulse rise and fall times, every probe needs to be calibrated before the measurement. The probes can be compensated by using the probe compensation output of the oscilloscope as a fixed square waveform signal source as explained in [71]. Another method, suggested in [81], is to remove the inductor in a DPT and replace the top device by a low inductance 100Ω resistor. The voltage across the resistor will be 100 times the current through with a negligible phase shift introduced by the small inductance to resistance ratio.

4.2 Voltage Measurement Techniques

The voltage measurements required for the switching characterization of a power switch are the gate-source voltage V_{gs} and the drain-source voltage V_{ds}. Voltage probes are used for these measurements and they can be either passive or active. Passive probes are rather simple, as they are built with wires and connectors, and/or resistors and capacitors, when needed for attenuation. They are economical, easy to use and thus the most widely used type of probes. On the other hand, active probes contain active components, such as transistors, and therefore, they require a power supply. They have a very low input capacitance, which leads to very small capacitive loading and eventually in high operating bandwidths [77]. However, they don't have the voltage range of the passive probes. There are three types of probes available for voltage measurements: differential probes, voltage divider probes and single-ended voltage passive probes [77].

4.2.1 Voltage Divider Probes

The voltage divider probes are considered as a special category of passive probes, which are used when much higher bandwidths are needed. A typical voltage divider probe, also known as Z_o probe, has a very low tip capacitance, which leads to bandwidth of several gigahertz and a rise time of 100 picoseconds or faster, whereas they can cause relatively high resistive loading. Bias-offset probes are a special type of voltage divider probe with the capability of providing a variable offset voltage at the probe tip. They are usually used in applications where resistive loading could upset the circuits operating point [77].

4.2.2 Differential Probes

Differential signals are usually referenced to each other instead of the earth ground. They can be probed by making two single-ended measurements and then use the scope to subtract one from the other. However, this method doesn't ensure an adequate common mode rejection ratio (CMRR). For this reason, in applications where the voltage must be measured across two points, neither of which is at the oscilloscope ground potential, differential probes are used in order to eliminate any signal interference caused by ground loops and currents. The main criteria for these probes are the CMRR and the bandwidth limitation. Their bandwidth is limited to around 100MHz because of the differential amplifiers slew rate [77]. Laimer in [82] tested 3 different differential probes reaching a bandwidth of 250MHz by using a differential voltage probe in conjunction with a high-performance differential amplifier, but still it is much lower than the single-ended probes. Moreover,

differential probes usually have long leads, causing a reduction to their bandwidth and introducing an inductance that might be sufficient to deteriorate the measurement.

4.2.3 Single-ended Passive Voltage Probes

Passive voltage probes, as discussed above, are the most widely used probes and they are available with different attenuation factors (1X, 10X and 100X), with the 10X probe being the most commonly used. The attenuation factor indicates the amount by which the probe reduces signal amplitude and thus extends the measurement range of the oscilloscope. These attenuation factors are achieved using resistive voltage divider techniques. This splits also the probe capacitance, effectively presenting lower probe tip capacitance for higher attenuation factors. Their bandwidth range is usually between 100MHz to 500MHz, which is higher than the bandwidth of the differential probes, and they have much lower resistive loading than the voltage divider probes [77]. Moreover, they allow the utilization of probe-tip adaptors (shown in figure 4.4), whenever the reduction of the measurement loop inductance is necessary.

Ground Lead Effects

All measurements can be considered as differential measurements. Even a measurement where the probe is attached to the signal point and the probe ground lead is attached to the circuit ground is actually a measurement between two signals, the ground signal line and the test signal line. However, differential measurement refers to the measurement of two signals, both of which are above ground. Making ground-referenced measurements, a ground return path is required in order to complete the measurement current path. For example, when the circuit under test and the oscilloscope are plugged into the same power circuit, the required ground return path is provided by the power grounds. However, this signal return path is lengthy and cannot be considered a low-inductive ground return. For this reason, most probe manufacturers supply with the probe a short ground lead that provides a ground return path.

Figure 4.3 represents the equivalent circuit of a typical passive voltage probe along with the probe's ground lead. The probe's ground lead is actually an inductance in series with the measurement, which increases with the length of the lead. This inductance forms a series LC resonant circuit with the capacitance of the probe, which might ring in the presence of a pulse. This ringing will cause deviations and possible errors in the measurement. Therefore, the probe ground lead should be kept as short as possible. Reducing the inductance will push the frequency of the ringing to values beyond the bandwidth limit of the probe-oscilloscope system, minimizing its effect on the measurements.

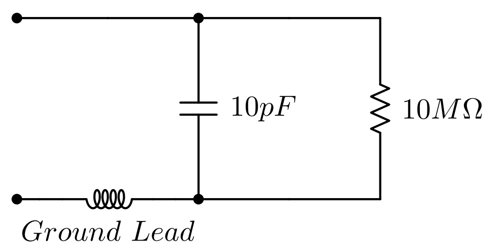
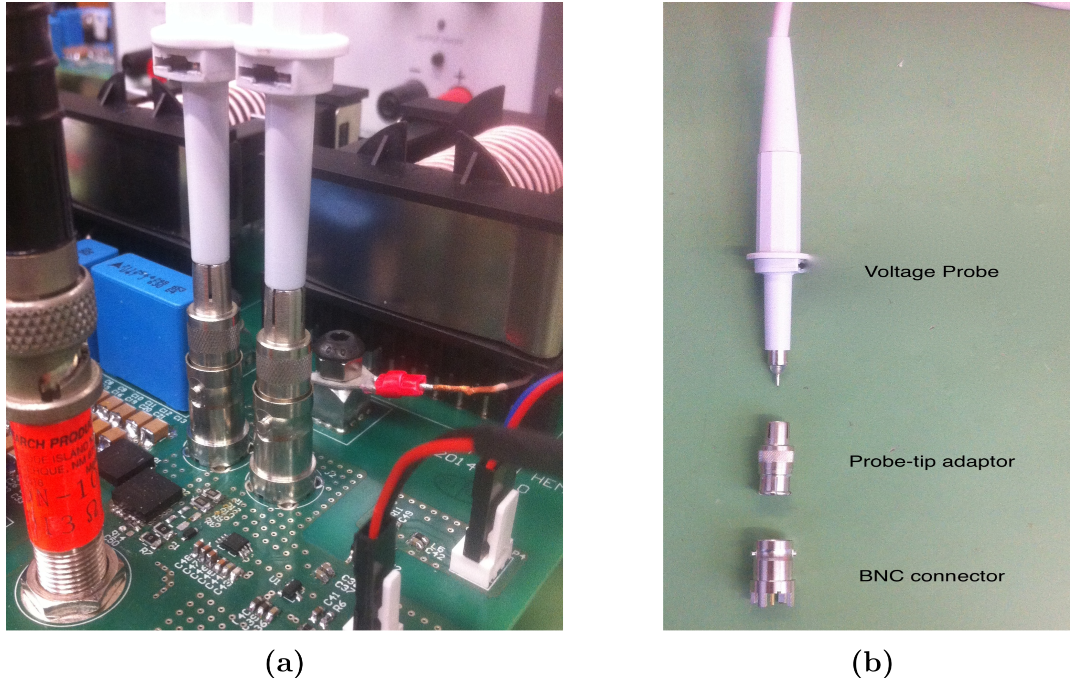


Figure 4.3: Equivalent circuit of a typical passive voltage probe

The best way of reducing measurement errors due to the ground path and also providing the best possible connection to the test point, is by using BNC connectors along with a probe-tip adaptors as shown in figure 4.4. The probe-tip adaptor is placed in the BNC connector and allows the probe tip to get connected directly into a test point, while the outer barrel of the adaptor makes a direct and short ground contact.



(a) (b)

Figure 4.4: Example of using a probe-tip adaptor to reduce the tip-to-ground loop

4.3 Current Measurement Techniques

Apart from the V_{ds} and V_{gs}, the drain current I_d is also required for the characterization of a power switch and there are several current measurement techniques that can be used in order to obtain it. Current sensors are very important in power electronics systems for purposes of protection and control. Therefore, extensive research work has been conducted on current sensing technology, including Rogowski coils, current transformers, Hall effect sensors, Magneto Impedance (MI) sensors, Giant Magneto Resistive (GMR) sensors and shunts. In principle when a current flow through a conductor, an electromagnetic flux field is formed around the conductor. The current measurement techniques are designed in such a way, as to sense the strength of this field and convert it to a voltage that can be measured by an oscilloscope. Each of them has its own advantages and disadvantages and a short description is given below.

4.3.1 Rogowski Coil

A Rogowski coil is an air-cored coil placed around the conductor to be measured. The principle of operation is based on the induced voltage in the coil by the magnetic field around the conductor. This voltage, which is proportional to the rate of change of the current, is integrated and produces an output proportional to the current, as shown in figure 4.5. The Rogowski coil is considered a relatively simple device and suitable for transient current measurements.

A Rogowski coil has the following features [83], [84]: *a*) high bandwidth which allows the measurement of switching transients; *b*) capability of measuring by using the same coil a wide range of currents by selecting appropriate values for the integrator components; *c*) there are no saturation effects, which makes the Rogowski coil suitable for protection applications; *d*) provides galvanic isolation *e*) it is inexpensive, easy to use, compact and light weight; and *f*) they are linear.

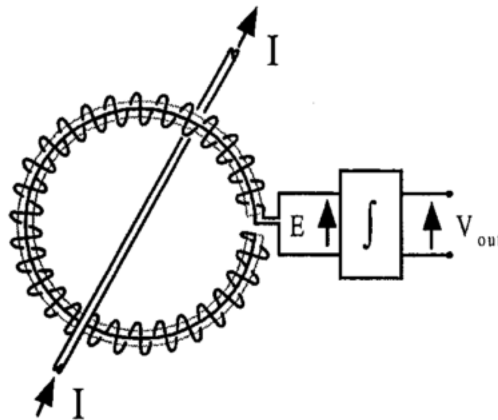


Figure 4.5: Basic configuration of a Rogowski current trasducer [83]

One of the limitations when a wide bandwidth is desired, is the contradictory coil constraints for operation at very low or very high frequencies. A combination of active integrators for the lower frequencies and passive integration for the higher frequencies can be used to solve this problem and achieve a bandwidth up to 10 MHz [83], [85], [86], [87].

A PCB-based Rogowski coil is presented in [88] combined with a Hall sensor. With this technique, called HOKA [89], DC current as well as transient current with several kA/s can be measured. A new Rogowski coil design is presented in [90], which can achieve bandwidth up to 40MHz and allows the measurement of high current gradients close to high voltage gradients without interferences. A planar embedded Rogowski coil is proposed in [91], which can be used in the integrated power electronics modules.

4.3.2 Current Transformer

This measuring technique measures the current in a conductor, which is passed through a toroid magnetic material. Once an alternating current flows through the single-turn primary, a voltage is induced in the secondary winding. The secondary winding of n turns, which should always remain shorted, carries the current that is 1/n times the measured current. The secondary current is in phase with the primary current and is usually used as an input to a power measuring device. DC current can not be measured and presence of DC current affects low frequencies performance. Current Transformers (CTs) have been extensively used for AC current sensing with a bandwidth up to tens of MHz. Measuring with CTs provides galvanic isolation and consumes little power [92].

Depending on the core material used in the CT, the designer should take into consideration the saturation, as well as the hysteresis of core material, which can affect the

measurement accuracy. Moreover, when measuring with a CT, a possible offset can cause saturation affecting the information obtained from the measurement. CTs are usually used for measurement of low frequency power. Radio frequency current in transmitting antennas can also be measured by using suitable core material, and PWM current in switching power supplies can be measured by using ferrite cores with appropriate compensation.

The saturation issue of the CTs can be solved by introducing a gap in the magnetic path. Because the magnetic flux density is always small in a CT with air gap, the heating effect of eddy currents is less important than in the CT. These sensors are known as Gapped Inductive Sensors [93].

CT can be integrated in the power electronics modules in the form of a planar transformer. However, when a very low profile with a high enough saturation flux density is required, its application is limited in the integrated power electronics modules. Regarding the paracitics, a CT introduces additional inductance to the conductor being measured compromising its high frequency performance [94].

Split core current probe

A particular current probe that uses the CT technique, is referred to as a split core probe and utilizes a U shaped core that is completed with a ferrite slide closing the top of the U (figure 4.6). This type of probe offers the advantage that the ferrite slide can be retracted, so the probe can be easily clipped onto the conductor whose current is to be measured, and when the measurement is completed the slide can be retracted again in order to be moved to another conductor. Split-core current probes are by far the most common type and they offer a frequency bandwidth of DC to 150MHz. These are available in both AC and AC/DC versions, and there are various current-per-division display ranges [77].

Figure 4.6: A split core AC current probe

Furthermore, transformer basics can be taken advantage of to increase probe sensitivity by looping the conductor through the probe multiple times. Two loops doubles the sensitivity, and three loops triples the sensitivity, but this also increases the impedance insertion by the square of the added turns. A split core current probe was used during this thesis work to measure the inductor's current.

4.3.3 Hall Effect Sensor

The Hall effect sensor is based on the Hall effect. This phenomenon requires the simultaneous presence of an electric current and magnetic field on a conducting material. Usually, a Hall device comes with a structure of a plate with four contacts. When a current is

detected between the two contacts and a perpendicular magnetic field is applied to the device, a voltage appears between the sense contacts. This voltage is proportional to the vector cross product of the magnetic field and the current. Because this voltage is in the range of millivolts, an amplifier stage is usually required with low noise, high input impedance and moderate gain. A differential amplifier with these characteristics can be integrated with the Hall element using conventional CMOS technology [95]. Next, as the Hall voltage is a function of the input current, a regulator that will maintain a constant current is required. Finally, temperature compensation is also easily integrated. Many low-power applications like current sensing and position detection use this kind of sensors. A schematic of the hall effect sensor is given below:

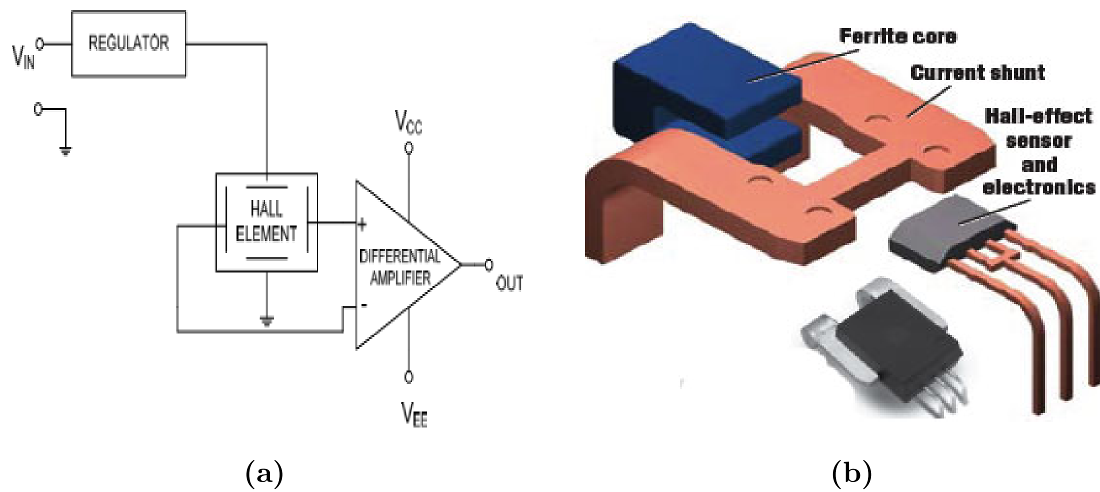


Figure 4.7: Hall effect sensor examples (a) Schematic of basic hall effect sensor (b) Commercial Hall effect current sensor (graphic courtesy Allegro Microsystems Inc., Worcester, MA)

They are characterized by a limited peak current due to core saturation and they have low bandwidth (<1MHz) including the DC current. For improved accuracy and wider dynamic range, the Hall effect sensors operate in closed loop modes with a frequency response up to hundreds of kHz [93]. Hall sensors performance evaluation is strongly connected to the sensitivity, offset and its temperature drift. Additionally, there is a strong connection between the geometry and the performance of the Hall effect sensors as is shown in [96].

The offset, which can be caused by imperfections in the device manufacturing process, is one of the major concerns in these sensors and it should be always minimized. Although microelectronics technology is used to fabricate a Hall device with lower offset voltage [97], the offset voltage is not stable and may vary with temperature and time. Due to the simple structure and its compatibility with the microelectronic devices, a Hall sensor can be monolithically used into a fully integrated magnetic sensor [98].

4.3.4 Giant Magnetoresistive Current Sensor

Giant Magnetoresistive (GMR) current sensors are based on the Giant Magnetoresistive effect. The trajectory of an electron moving through a magnetic field changes due to the presence of that field, causing the resistance of the metal to vary with the direction of the applied magnetic field. The resistance is highest when the applied magnetic field is

parallel to the current and lowest when it is perpendicular to the current. This difference in the resistance for a current parallel to the applied field and for a current perpendicular to the applied field is the classical magnetoresistive effect [99].

The GMR effect observed strongly in ultra thin multilayer films and a GMR current sensor consists of alternating ferromagnetic and non-ferromagnetic thin layers, each a few atomic layers thick. However, there are two conditions for the GMR effect to occur [99]: *a*) the relative orientations of the applied magnetic film in adjacent magnetic metal layers must change, and *b*) the thickness of the films must be a fraction of the mean free path of an electron in the multilayer array.

Due to the high sensitivity to the magnetic field, the GMR sensors can be adequately used to measure the current by sensing the magnetic field induced by the current. GMR sensors are typically deposited and etched into a Wheatstone bridge pattern to improve the sensitivity and minimize the temperature dependent effects [100]

4.3.5 Giant Magnetoimpedance Current Sensor

The principles of magnetoinductance were discovered by Hans Cristian Orsted, who observed that when a current flows through a wire and varies with time, not only a magnetic field is induced around a wire, but the magnetic flux in the conductor varies as well and induces eventually, an electromotive force between the ends of the conductor. This force is superimposed on the ohmic voltage.

However, the magnetoinductive effect has been under more intense investigation since the development of the amorphous wires with soft magnetic properties and it is considered as a new principle for magnetic field sensors. It was found that the impedance $Z(\omega) = R + jX$ of amorphous ferromagnetic wires, such as FeCoSiB and CoSiB, changes significantly with the applied magnetic field in the range of frequencies over 10MHz [101]. This effect is called Magneto Impedance (MI) effect and can be explained by the skin effect and the fact that the effective permeability of the ferromagnetic materials depends on the frequency, the amplitude of the ac magnetic field, the magnitude and orientation of a bias dc magnetic field [102]. By measuring the variation in the impedance, the magnetic field produced by the current can be calculated in order to find the value of the current. This effect is expected to be promising showing high sensitivity, quick response and small dimensions.

The MI effect has been investigated first in wires and ribbons. However, such forms result in installation's difficulties and, also, they are characterized by poor repeatability of their magnetic properties since they are influenced by the stress generated in wires. In order to eliminate these problems, thin film magnetic field sensors based on the Magneto Impedance effect have beed developed [101].

MI sensor is more field sensitive than GMR sensor. Although the Giant Magneto Impedance sensors are still improving, they are already considered suitable candidates in replacing the existing current sensors, due to their low cost, high flexibility, small size, high sensitivity and wide bandwidth.

4.3.6 Coaxial Shunt

Shunts are very cost effective sensing element, since it is simply a resistance placed in the main current path, in order to amplify the voltage drop to an adequate level. The resistance is usually in the range of few milliohms, in order to keep the dissipated power to a minimum, and Kelvin terminals are utilized to increase accuracy. They are suitable for measuring DC, AC and impulse currents, but they don't offer galvanic isolation.

Their design should be done with care, since they must have a low resistance and at the same time a low inductance in order to achieve a wide bandwidth along with a high accuracy. Their principle of operation is based on the ohmic voltage drop and due to the low resistance, the magnitude of the output voltage is typically very small. Measuring this voltage requires wires to be attached at each terminal forming eventually a loop with the sensing resistor and measurement circuit. Moreover, practical shunts have intrinsic inductance.

According to Faraday's law, the magnitude of the induced voltage in this loop due to the rapidly changing magnetic fields may become comparable to the resistive voltage drop, adding noise to the measured voltage. On the other hand, minimizing the impedance by using a thick conductor for the connections, will influence the response of the shunt due to the electromagnetic skin effect, which will cause the impedance to change, especially in high frequency operation. To minimize these effects, wide-bandwidth resistive shunts are usually coaxial in design, as shown in figure 4.8, including two resistive tubes each carrying current in opposite directions [103].

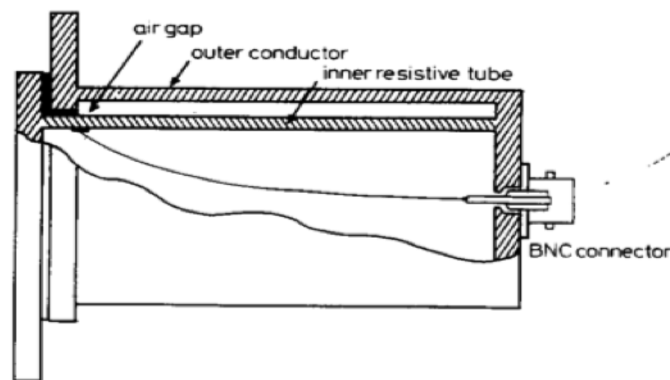


Figure 4.8: Structure of a coaxial shunt [103]

Coaxial shunt is a bulky device and is usually used when wide-bandwidth resistive shunts are required in order to measure with high accuracy high DC, AC and impulse currents. A coaxial design comprise a thin tube of resistive material and a closely attached, concentric current return path made with a highly conductive material. The advantage of this design is that the current through the shunt does not produce significant amount of magnetic flux inside the cylinder, where the measuring circuit is. This means that the circuit is inductively decoupled with the shunt current and the output voltage contains no inductive component [103]. Moreover, the outer conductor provides protection from external noise sources and internal fields of the current traveling through the sense wires ensuring an accurate measurement.

The principle of operation is elaborated in [103]. According to [103], when a step current is applied to the current shunt, the electromagnetic field will be firstly restrained in the air gap between the two conducting cylinders and then it will be diffused into the conductors, at a rate determined by the shunts characteristics, until a uniform current density is reached. Since it is claimed that there is no magnetic field inside the inner tube, the measured voltage will be due to the electric field on the inside surface of the shunt alone. However, the magnetic field in the air gap will introduce an inductance to the shunt, which will eventually cause an increased amplitude peak along with a phase lead to the measured signal [79]. This can also be seen from the equation 4.3, which can also be used to estimate the bandwidth of the coaxial shunt [104].

$$f = \frac{1}{2\pi}\frac{R}{L} \tag{4.3}$$

It can be seen from the equation above that the resistance to inductance ratio of the coaxial shunt should be as high as possible. In addition, the bandwidth of the coaxial shunt is influenced by the skin effect of the resistive material and the distributed capacitance of the shunt [103]. However, despite these limitations, coaxial shunts have higher bandwidth compared to CTs and Rogowski coils.

Throughout the experimental part of this thesis, a 0.1Ω shunt resistor (SSDN-10) manufactured by T&M Research with an equivalent bandwidth of 2GHz was used. An equivalent circuit of this shunt resistor was presented by Chen in [71] and it is illustrated in figure 4.9. He proved that although the main current flows through the inner and outer resistance tubes without creating a magnetic field within the shunt resistor, an inductance is caused by the loop that the current forms within the resistor. This inductance (2.2nH as shown in the figure below) is in series with the resistance, but its voltage drop is not shown by the measurement port.

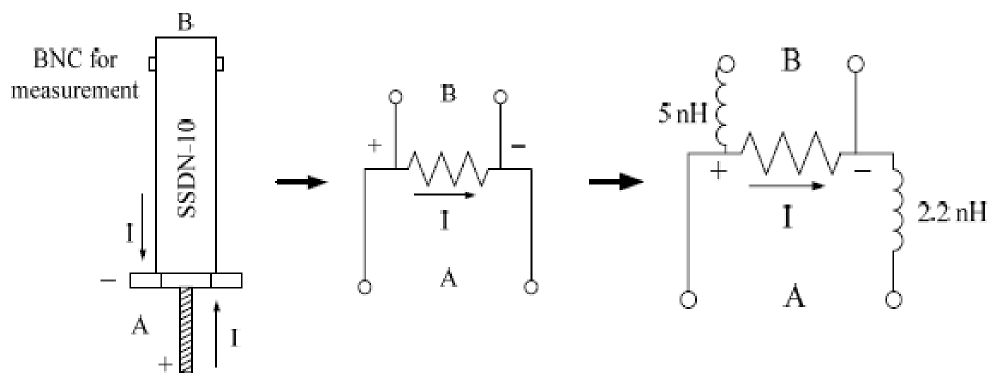


Figure 4.9: A coaxial shunt resistor with the equivalent circuit [71]

4.3.7 Summary of the discussed current measurement techniques

The comparison of the performance and characteristics of the current sensors described above is summarized in the following table 4.1. These characteristics are considered of most importance for the selection of a current probe.

Table 4.1: Comparison of current sensors technologies [91]

	Bandwidth	*Saturation*	*Linearity*	*Material Technology*
Rogowski	$0.1 \sim 100MHz$	No	Very good	simple
CT	$0.1Hz \sim 100MHz$	Yes	Fair	simple
Hall	$< 1MHz$	Yes	Poor	complicated
GMR	$DC \sim 5MHz$	Yes	Fair	Very complicated
GMI	$DC \sim 30GHz$	No	Fair	Very complicated
Shunt	$DC \sim 10MHz$	No	Very good	simple
Coaxial Shunt	$DC \sim 2GHz$	No	Very good	simple

4.4 Discussion

This chapter focuses on issues and limitations that need to be taken into consideration when high frequency measurements are required, in order to ensure the fidelity and the accuracy of the results. Moreover, different voltage and current measuring techniques are presented.

As already mentioned above, all the probes should have enough bandwidth so as to be able to capture the fast rise and fall time of the switching waveforms. However, different probes possess different propagation delays and the probes need to be compensated after connected to the oscilloscope, otherwise there could be timing misalignments between the captured waveforms, eventually leading to measurement errors and wrong calculations in switching losses.

Chapter 5

Investigation of the influence of the inductor's parasitic capacitance

Nowadays, the widely accepted method to assess the switching performance of power devices is the double-pulse tester (DPT). Two pulses are launched to the device under test (DUT) in a clamped inductive load circuit. Switching under this load condition is the same commutation mode for the power devices as switching in a PWM, hard-switching type converter under any desired voltage and current ratings. During this thesis project, one circuit was designed and two PCBs were built having different device as top switch in order to observe the behavior of the DUT under different conditions. However, when designing the actual circuit, several layout limitations are to be taken into consideration.

Power devices are implemented in topologies where a transformer or an inductor is usually needed. Apart from the circuit and device's package characteristics, the equivalent parallel capacitance (EPC) introduced by the transformer or inductor influence the switching transitions of the power switch. Experimental analysis of the impact of this EPC on a power device's switching transitions and verification of the analytical model will be the goal of this chapter. For this, an inductor with very low EPC was constructed and used during this work.

In this chapter, the operation of a DPT will be explained in detail in section 5.1. Next, the design of the PCB used in this study will be discussed in section 5.2.1. In section 5.2.2, the methods used for the high frequency measurements will be discussed. The design and construction of the inductor will be given in section 5.2.3. Finally, the results of the experiments will be discussed and comparison with the analytical model calculations will be made.

5.1 The Double-Pulse Tester

Apart from the model (simulation, analytical etc) used from the designer to investigate the switching transitions of the DUT, sets of experiments are also conducted in order to examine the behavior of the DUT on an actual circuit and, mainly, to verify the accuracy

of the model. Furthermore, the test results can also provide a basis for the power converters' design, regarding the switching frequency selection, dead time setting, thermal management, and efficiency estimation [71], [79], [105], [106]. Therefore, there have been a lot of publications explaining the operation of power devices under the clamped inductive load, as already discussed in section 2.3.2.

An inductive load double-pulse tester has been designed for this thesis, using the software Altium Designer, in order to investigate the switching behavior of the high voltage GaN HEMT in cascode configuration. The circuit is, basically, a buck converter and a basic schematic is shown in figure 5.1. The complete schematic of the DPT used during this thesis project can be found in Appendix . Two setups were built with the only difference that different devices where used as the top switch in order to investigate how the reverse recovery charge of the top switch influences the switching transition of the DUT.

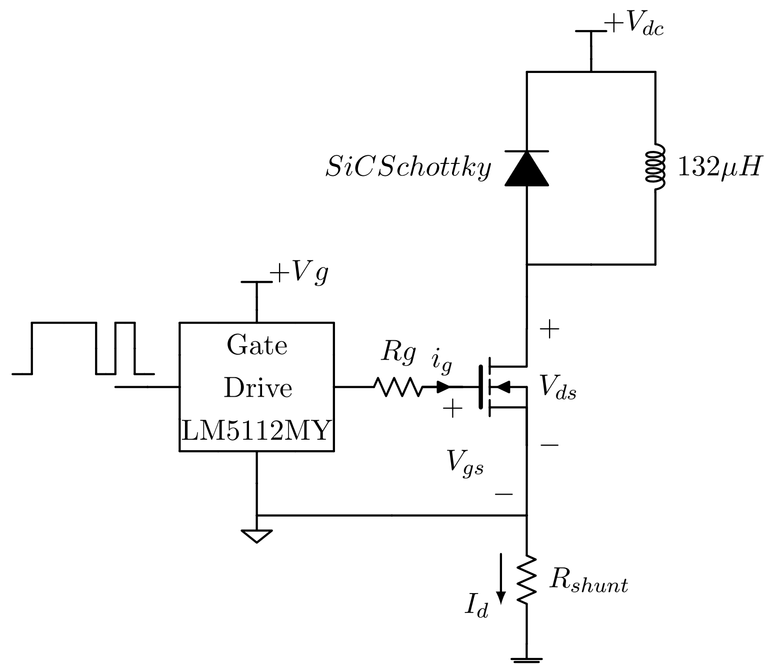


Figure 5.1: Double-pulse Tester schematic for the high voltage GaN HEMT

First, a SiC Schottky diode from CREE (C3D04060A) with very small reverse recovery charge was used, simulating a unidirectional buck converter, while in the second setup another high voltage GaN HEMT with low reverse recovery charge was applied to examine the case of a bidirectional buck converter. The DUT is driven in both setups by the same high-speed, high-current gate driver LM5112MY from Texas Instruments, with gate voltage from 0V to 10V. The circuit's operation is controlled by a digital signal processor (DSP) (TMS320F28069 Piccolo Microcontroller from Texas Instruments) providing a double-pulse signal to the gate driver as shown in figure 5.1. Measurements of the gate voltage (V_{gs}), drain voltage (V_{ds}) and drain current (I_d) are taken as shown in figure 5.1 and the waveforms captured under the double-pulse operation are shown in figure 5.2.

At time t_0, the first pulse is sent from the signal generator to the gate driver and the device is turned on. The width of the first pulse determines the current value, thus the switch stays on until I_d reaches the desired current level. At time t_1, the first pulse ends and the gate is forced low. The turn-off switching transition of the DUT is obtained

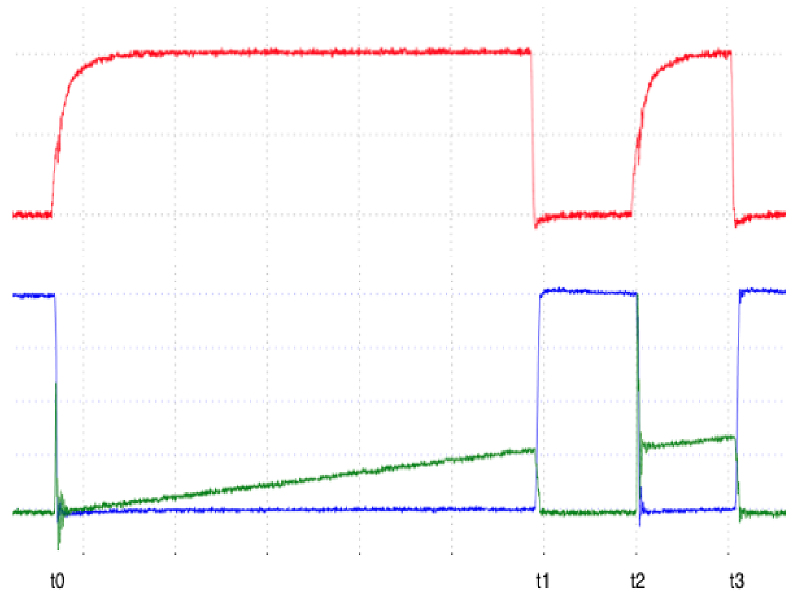


Figure 5.2: Double-pulse test waveforms. Blue waveform is the drain-source voltage, the green is the drain current and red is the gate-source voltage

through the measuring equipment. During the t_1 to t_2 interval, the device is off and the inductor current freewheels through the top switch (diode or GaN HEMT). This time interval is usually long enough so any ringing in the drain voltage and current is damped before the second pulse is sent. At time t_2, the second pulse is sent to the gate driver and the device is turned on again.

Under clamped inductive load condition, the inductance value is chosen so as to maintain the load current constant during the previous interval. Hence, the turn-on switching transition is captured at t_2 under almost the same conditions as the turn-off transition. The interval from t_2 to t_3 is chosen so as any ringing in the drain voltage and current is damped and the increase in the drain current does not exceed the device limitations. Finally at time t_3, the gate is forced low again and the device is turned off and stays off.

The time intervals t_1 to t_2 and t_2 to t_3 are set to be equal in this study. By doing so, the interval from t_1 to t_3 is considered to be a period (T) of operation with 50% duty cycle. Thus, the switching transients captured at the end of the first pulse and the beginning of the second, can be assumed to be the same as if the DUT was operating in a buck converter with a frequency equal to 1/T. However, the DUT is switched only twice and the device junction temperature rise due to the switching loss cannot be taken into consideration. In order the examine the switching transitions of the DUT while taking into consideration its temperature-dependent switching characteristics, like the on-resistance of the device, the junction temperature can be controlled externally by a heating device.

5.2 The DPT hardware Setup

The DPT hardware setup is shown in figure 5.3. The setup is divided into two stages, the control and the power stage. For the control stage, a DSP, which is controlled by a

PC, sends the double-pulse signal with adjustable pulse widths to the DPT board. The switching waveforms are captured through the measuring probes by a digital oscilloscope, and the data are transferred to the PC. Thus, the PC is responsible for programming the double-pulse signal, collecting switching waveforms, and post-processing the measured data. For the power stage, a DPT board is designed featuring the gate driver circuit, power devices, and interfaces to connect with dc voltage source, load inductor, auxiliary power supply, and the DSP. Considering that the GaN HEMT devices are characterized by high switching-speed capability, the challenges for switching characterization of the DUT primarily lies on the layout design of DPT board and precision measuring of the switching waveforms.

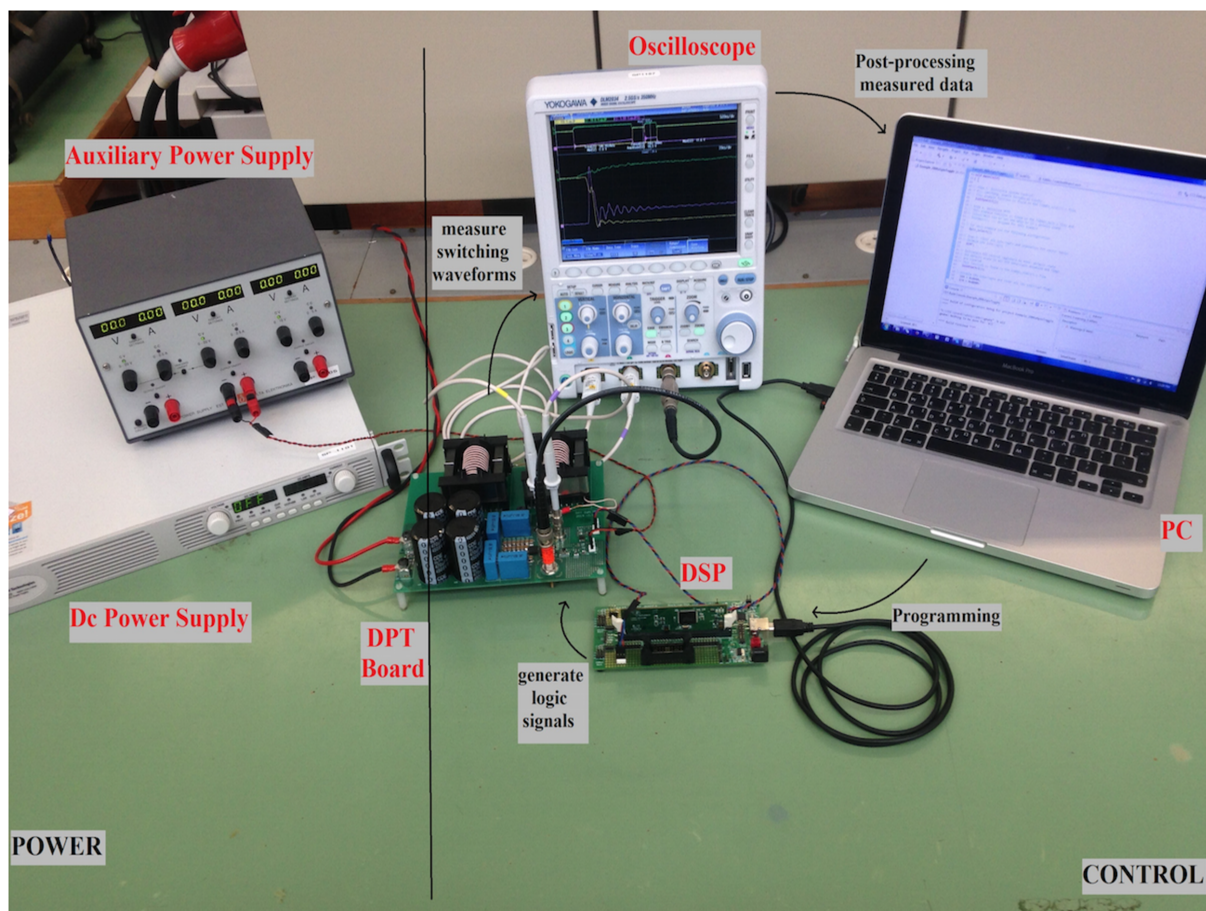


Figure 5.3: Double pulse tester hardware setup

5.2.1 Printed Circuit Board design

Although the schematic shown in figure 5.1 is quite simple, there are several key layout constraints to consider in order to minimize the influence of the external parameters on the switching transitions when building the actual circuit. For this thesis project the tester was constructed on a four layer PCB, integrating the dc bus, the switching phase leg, the gate drive circuit, the dc bus bulk aluminum electrolytic capacitors (AECs), the film and the ceramic capacitors, the GaN HEMT and the top switch, the measuring probes (coaxial current shunt and the single-ended passive voltage probes), and the inductor into a single board (see figure 5.4). All these components were placed in such a way as to

minimize the switching power loop inductance, the gate driving loop inductance and the common source inductance [71].

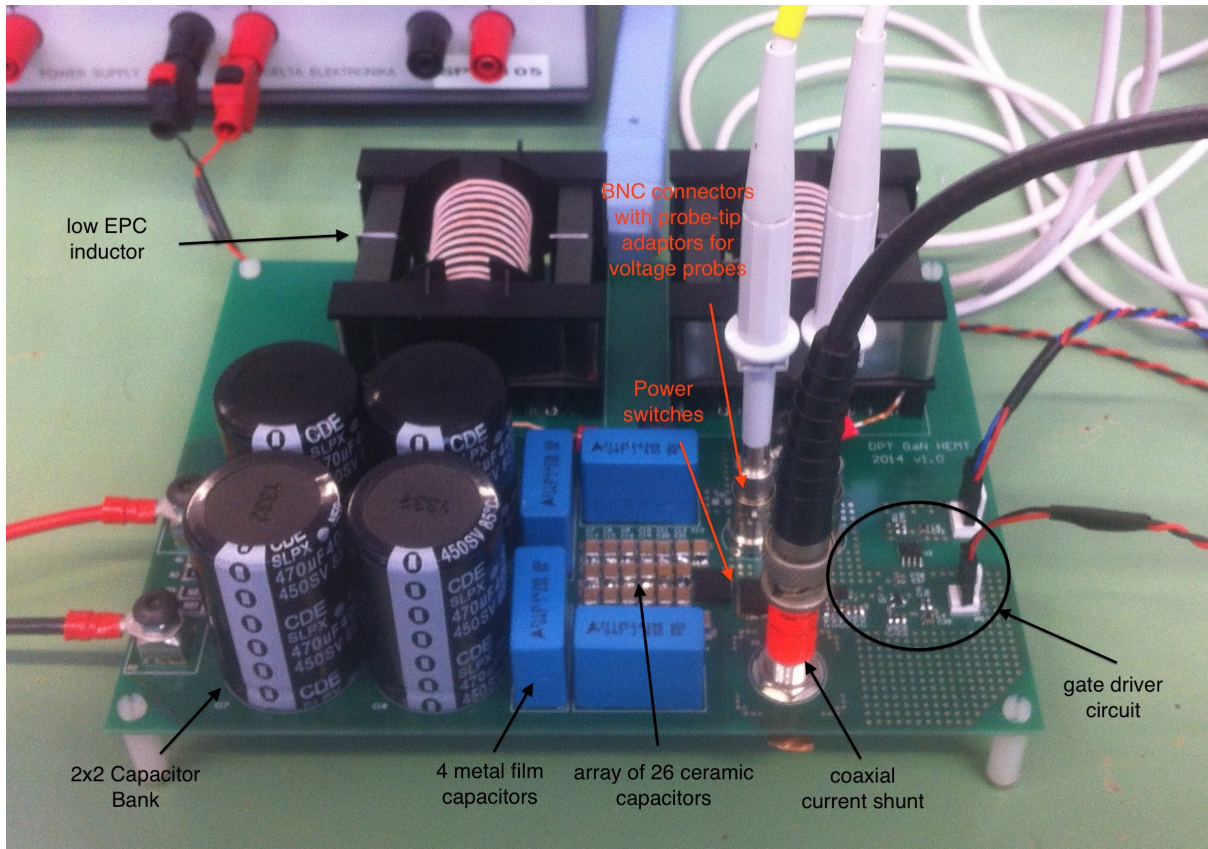


Figure 5.4: Photo of the PCB constructed during this thesis project

The switching power loop inductance consists mainly of the dc bus, the top freewheeling diode or top device, the bottom DUT, and the inductance introduced from the coaxial current shunt. The dc bus is formed by all four layers. The top layer and the middle-layer 1 form the positive dc bus plane, while the middle-layer 2 and the bottom layer the negative dc bus plane. The four layers are almost perfectly overlapped, except that the negative dc bus plane is extended in order to include the current shunt. The two inner layers of the PCB are shown in figure 5.5, where the dc bus planes are pointed with the red dashed lines. Furthermore, the dc bus power loop is built using a planar bus structure and features a 2x2 bank of $470\mu F$ - 400V AECs, to act as a bulk capacitance for power storage, four $470nF$ - 630V metal film capacitors in parallel, to decouple the AECs and the dc source, and an array of twenty six $100nF$ - 630V ceramic capacitors, to provide a high frequency decoupling layer of the remaining dc bus stray inductance.

The film and ceramic capacitors usually have low values of equivalent series resistance (ESR) and inductance (ESL) and they are used because the bulk capacitance will not be able to provide quickly sufficient amount of energy. More than one of these capacitors were used connected in parallel, in order to minimize the contribution of their ESL to the switching loop inductance. The film and ceramic capacitors were placed as close as possible to the two devices (top switch and DUT) with their negative pins connected closest to the DUT, minimizing the drain-source loop parasitic inductance. The arrangement of the capacitors and devices can be observed in the figure 5.4 and 5.5.

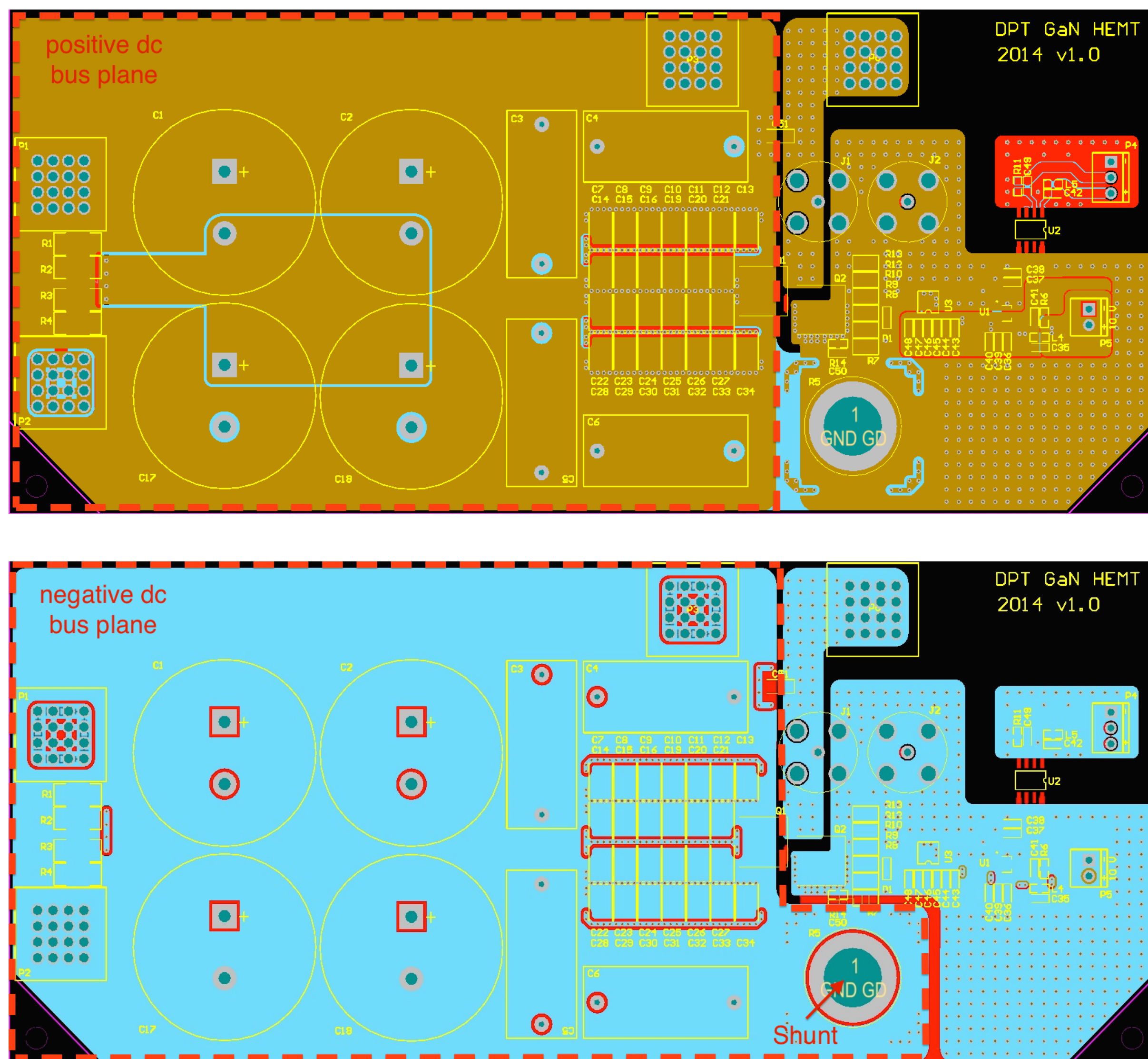


Figure 5.5: Middle layers of the PCB forming the dc bus. Brown layer is the +Vdc and cyan layer is the -Vdc

In order to further minimize the drain-source loop parasitic inductance, the two devices were placed so as the drain of the DUT would be in maximum proximity to the anode or source of the top device. The connection between these two terminals (indicated as mid-point in figure 5.6) designed as to have no overlap with the positive dc bus plane, avoiding in this way to add any parasitic capacitance across the freewheeling diode, and, eventually, to cause a bigger current overshoot during the turn-on of the DUT.

Next, the common source inductance, which is the inductance shared by the gate driving loop and switching power loop, is critical for the performance of the DUT (see section 2.3.2) and, thus, it should be minimized in order to achieve the maximum switching performance. This inductance is shown in figure 5.6 as the top-layer red plane surrounding the DUT, the gate driver circuit, and the shunt. Its planar structure helps towards the minimization of this parasitic loop inductance. Moreover, the gate driving loop's inductance was minimized by placing the gate driver as close as possible to the DUT's gate. An array of SMD gate resistors (Rg array) was used in order to further minimize this loop inductance, placed in maximum proximity to the DUT. All four PCB layers can be

found in Appendix .

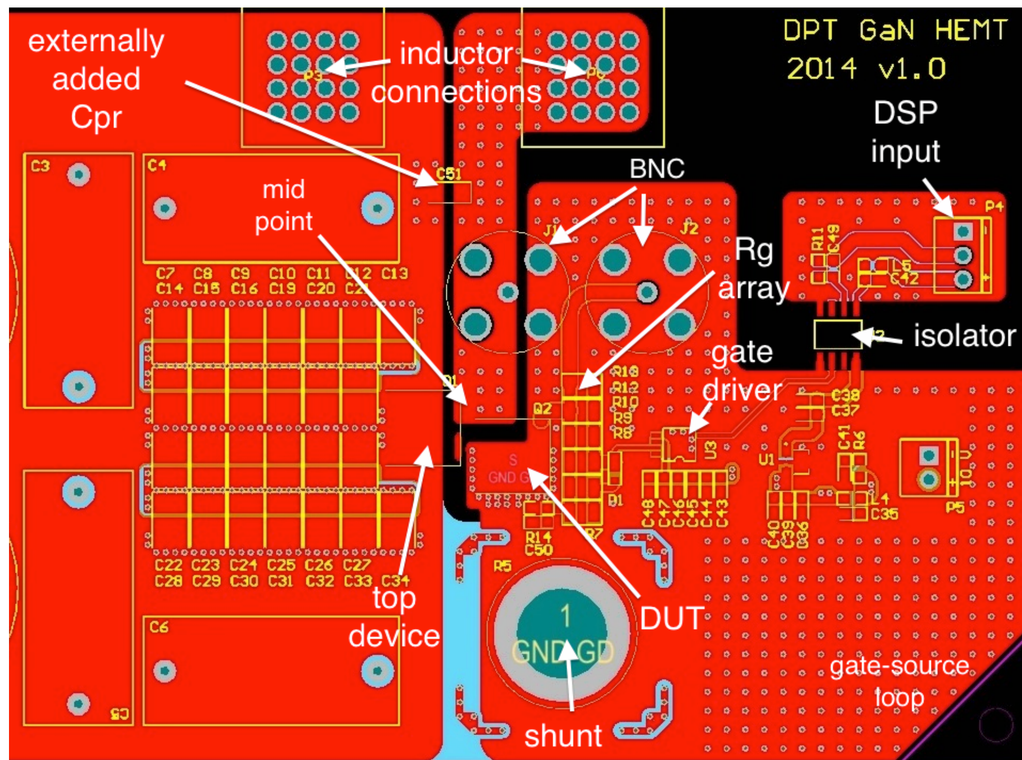


Figure 5.6: Top layer view of the gate drive area

5.2.2 Measurement Techniques

In order to fully characterize the switching transition of a power device, measurements of the gate voltage (V_{gs}), drain voltage (V_{ds}) and drain current (I_d) are needed. However, making high frequency measurements require special attention (see chapter 4). The I_d is measured with a 0.1Ω shunt resistor (SSDN-10) manufactured by T&M Research with an equivalent bandwidth of 2GHz, while the V_{gs} and V_{ds} are measured with the Yokogawa 701939 600V, 500MHz, 10x passive probes supplied standard with the Yokogawa mixed signal oscilloscope DLM2000 350MHz used during this work. Single-ended passive probes can be used in this work because the DUT is on the low side of the configuration. As it will be shown later on in this chapter, the rise/fall time of the GaN HEMT V_{ds} and I_d can reach a time of 6nsec. According to section 4.1.1, such a transition time corresponds to a bandwidth of 350MHz. Consequently, all the measurements equipment meet the bandwidth requirements. The shunt and the voltage probes can be seen in figure 5.4.

As shown in figure 5.1, all three measurements share the common point of the DUT source terminal. This point is used as ground for the voltage probes and, hence, for the oscilloscope. In order not to short-circuit the setup and eventually destroy the oscilloscope, the current shunt needs to be connected with its negative pin to that point and then flip the waveform in the oscilloscope to get the correct waveform. The current shunt is connected with a 50Ω coaxial cable to the scope. A 50Ω terminator resistance is placed at the end of the cable, designed to match AC impedance and hence minimize signal reflections. Electrical termination of a signal stands for providing a terminator at the end of a wire or cable to prevent a high-frequency signal from being reflected back, causing interference.

Using different types of probes means different propagation delays (see section 4.1.2). These delays are usually in the range of nanoseconds, and yet, if not compensated properly, they will lead to serious timing misalignment and eventually to wrong loss calculations. In this work, the 701939 passive probe was used as the basis and compared to this, the coaxial cable has minus 2.5ns delay.

5.2.3 Low EPC inductor design

The load inductor is of great importance for this thesis, because of its equivalent parallel capacitance (EPC). The EPC is considered a parasitic element of the circuit with a high impact on the DUT's switching transitions and especially on the turn-on process. It will be shown later on that the energy stored in the EPC, will eventually contribute to the DUT's current overshoot during the turn-on transition increasing the turn-on switching losses [105], [15]. Apart from that, the parasitic capacitance together with the value of the inductance determine the self-resonance frequency (SRF) of the inductor. Converters operating at frequencies close to the range of the SRF may present resonances, due to the fact that the oscillations in the inductor would not have been damped before the next switching occurs.

The EPC of an inductor is usually modeled as a lumped capacitance C_{pr} in parallel with an inductance L, which can reproduce the first resonant frequency of the inductor (see figure 5.7). This modeling approach is satisfying in most cases, but it neglects the factors that affect the EPC value.

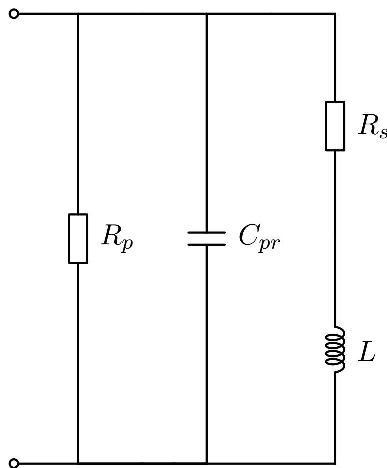


Figure 5.7: Equivalent simplified model of an inductor

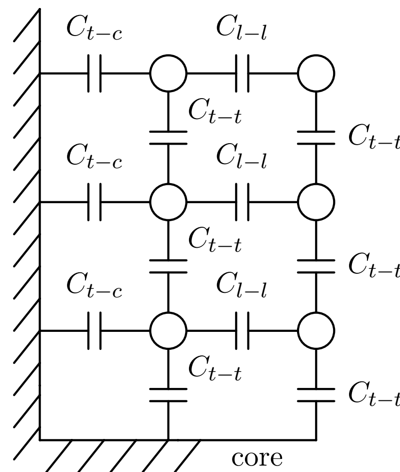


Figure 5.8: Cross section of a 2-layer inductor

For a more comprehensive analysis, the parasitic capacitance should be considered as being distributed and that it consists of turn-to-core (C_{t-c}), turn-to-turn (C_{t-t}) and layer-to-layer (C_{l-l}) capacitances (see figure 5.8) [15]. A bobbin is usually used that provides adequate distance between the core and the winding, reducing the C_{t-c}. However, when the winding consists of many turns, the equivalent C_{t-c} can be a mayor contributor to the EPC since all the turn-to-core capacitances are in parallel. In regards to the capacitances contributed by the coil itself, the turn-to-turn capacitances on a given layer are connected

in series and thus the equivalent C_{t-t} is small, while the parasitic capacitances formed between the turns of adjacent layers appear in parallel, making the equivalent C_{l-l} a big contributor to the total EPC.

When the inductor is used in a high-frequency converter, the EPC of the inductor is not a negligible parameter any more and thus, it must be minimized. The most effective way to reduce the EPC is by using one layer of windings, which is not always feasible because more space is required. Another way to reduce the EPC is by increasing the distance between the layers of the inductor, when two or more layers are required. For this, different kinds of spacers can be used between the layers. Typical insulation materials used for this purpose have relative permittivity (ε_r) 3 or more. In order to further minimize the EPC, the material of the spacer used between the layer can be chosen to have small relative permittivity. The best insulator is considered to be the air, which has $\varepsilon_r \approx 1$.

Finally, it was considered more convenient to build an inductor with very low EPC and to add capacitances of different values externally in parallel with the inductor at later stage. Since the physical size of the PCB and of the inductor itself is not an issue, two single-layer 12 turns $66\mu H$ inductors on a ferrite magnetic core ETD 54 with an air gap between the turns were built and connected in series achieving a total equivalent parasitic capacitance of $2pF$, as shown in figure 5.9. Ceramic capacitors of $22pF$, $56pF$, $78pF$, and $100pF$ were soldered close to the inductor in order to model inductors with bigger values of equivalent parasitic capacitance (see figure 5.6).

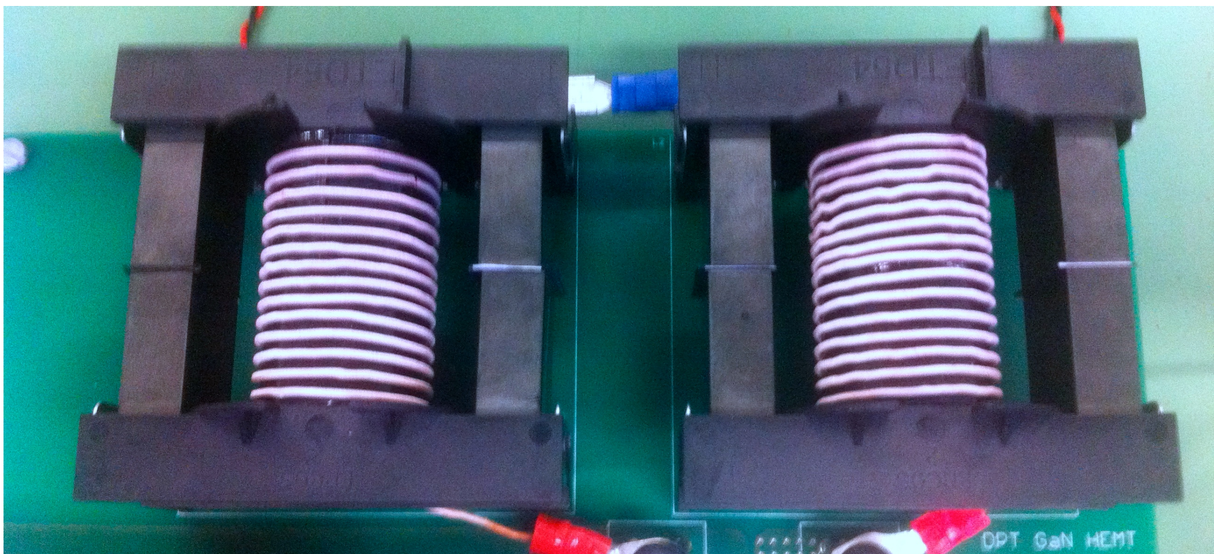


Figure 5.9: Photo of the inductor built during this work

5.3 Verification of the analytical loss model

In order to verify the analytical loss model developed in chapter 3, this section is divided into two parts: firstly, the switching behavior of the GaN HEMT with no additional capacitance in parallel with the low EPC inductor was examined. The PCB is considered to be optimally designed so as to minimize the parasitic inductances, which leaves only the device characteristics (parasitic capacitances and package parasitic inductances) to determine the switching process of the GaN HEMT. Secondly, ceramic capacitors of $22pF$, $56pF$, $78pF$, and $100pF$ were soldered close to the inductor modeling inductors with bigger parasitic capacitance, in order to investigate the influence of the inductor's EPC on the GaN HEMT's switching behavior.

The analytical loss model assumes that the top device has no reverse recovery charge, thus the PCB with the SiC Schottky diode will be used in this section..

5.3.1 Investigation of the GaN HEMT's switching behavior

The DUT was subjected at switching conditions of 400V drain-source voltage and different values of inductor's current I_L (2A, 5A and 10A). The drain-source voltage and the drain current were recorded to compare with the calculated results from the analytical model. Comparison of the switching transitions for the three different values of the inductor's current are shown in figures 5.10, 5.11, and 5.12. The waveforms are recorded for a period of 100ns, which is long enough to capture the switching transition and for the ringing to settle down before the next switching occurs. The gate resistance for this set of experiments is set at 7.5Ω for turn-on and 0Ω for the turn-off process.

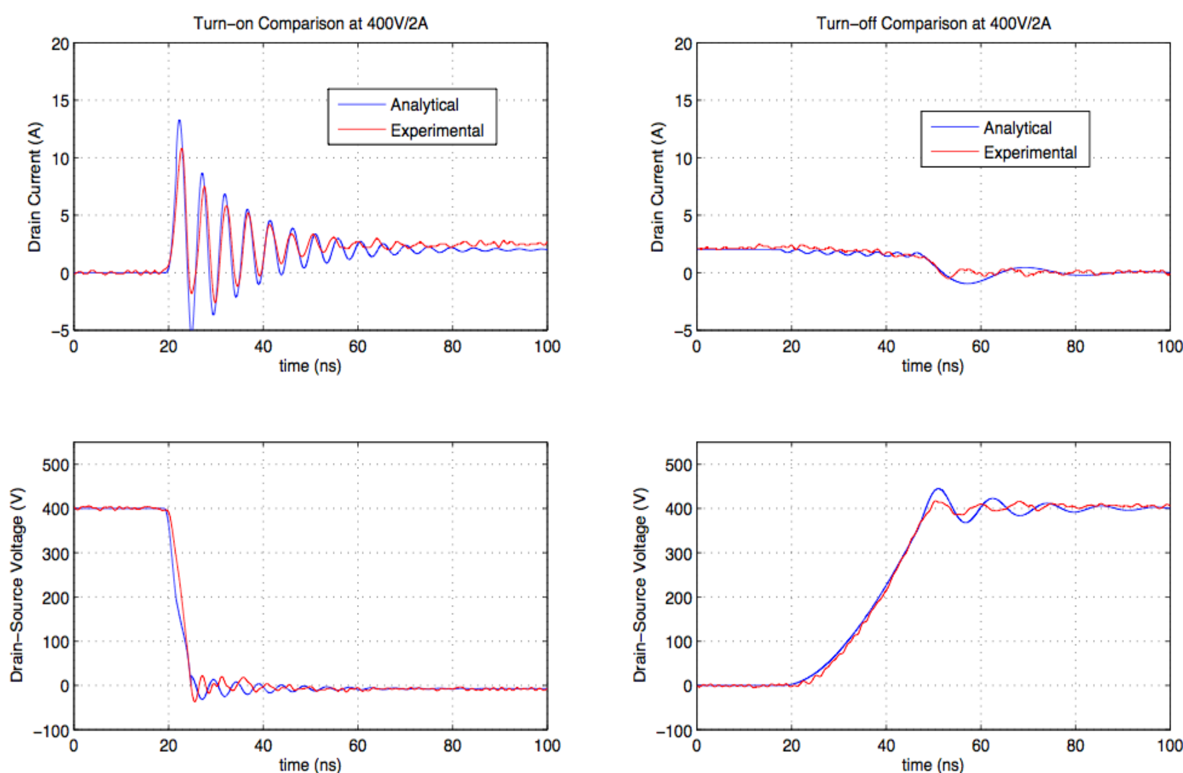


Figure 5.10: Comparison of the turn-on & turn-off switching transitions at 400V/2A

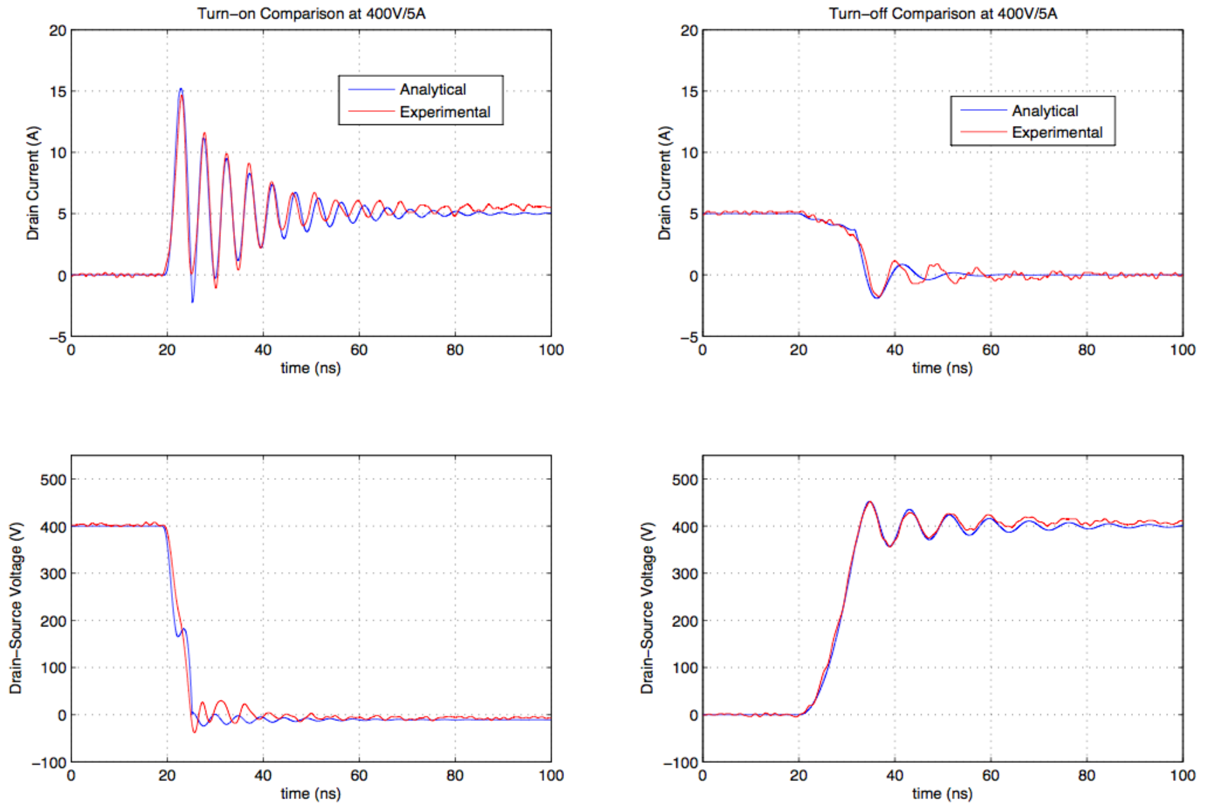


Figure 5.11: Comparison of the turn-on & turn-off switching transitions at 400V/5A

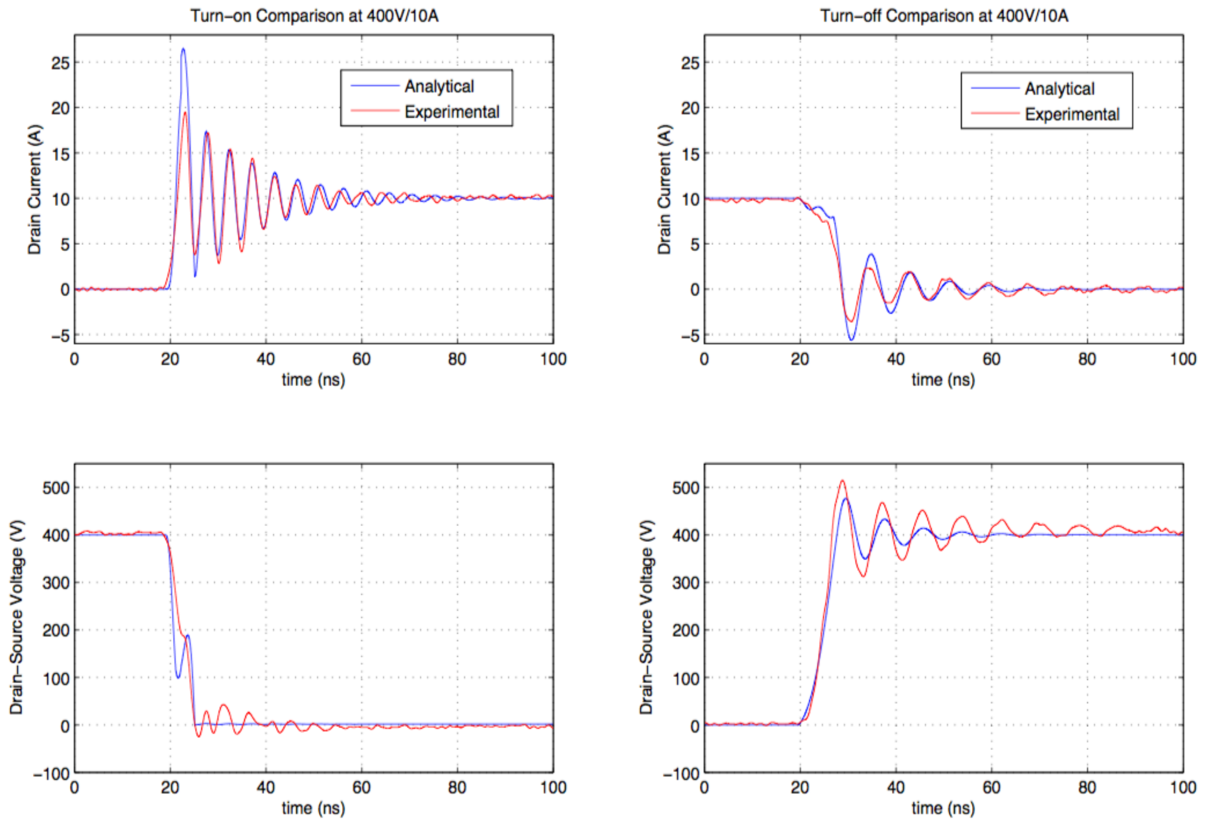


Figure 5.12: Comparison of the turn-on & turn-off switching transitions at 400V/10A

Analysis of the comparison

The figures above show the waveform comparisons between the double-pulse test and the calculated results of the proposed analytical model during the switching transitions. It can be seen that the analytical model is able to match the experiments on the voltage and current slope rate, especially during turn-off, and the main transition time. However, during the turn-on process, the drain-source voltage drops faster in the beginning and increases again to match the falling of the experimental waveform. This is caused due to the discrete values of the parasitic capacitances used in every stage of the transition modeling the non-linearity of these capacitances. For the same reason, the current overshoot during the turn-on transition is not accurately predicted. Next, the oscillation frequencies and damping effects have been predicted reasonably well, but they present differences due to inaccurate high-frequency parasitic inductance and stray resistance of the circuit.

Additionally, the energy dissipation during the turn-on and turn-off switching transitions is calculated and compared in figure 5.13. Based on the experiment and analytical model waveforms, the energy dissipation is calculated by integrating the product of the drain-source voltage and the drain current. However, it is important to note that integrating the drain-source voltage and the drain current does not represent the real turn-on and turn-off loss. During turn-on process, the output capacitance (C_{oss}) of the device is discharged through the channel of the device, causing the channel current to deviate from the drain current measured on the device terminals. During the turn-off process, the C_{oss} is charged by drawing part of the load current, making the channel current smaller than the drain current. Thus, in a double-pulse test, the turn-on loss derived from the waveforms is underestimated while the turn-off loss is overestimated. On the other hand, the sum of the turn-on and turn-off energy can be used to predict the switching loss in one switching cycle [71]. Finally, the switching energy calculated with the analytical model seems to match well the experimental results, expect the case at 10A where the current overshoot in the analytical model is bigger.

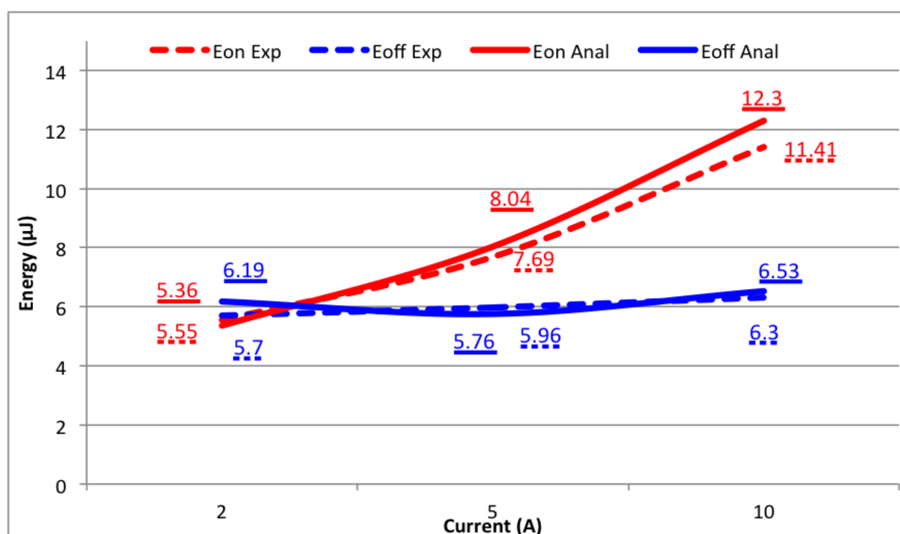


Figure 5.13: Switching energy comparison between the experimental & the analytical results

Analysis of the switching behavior

The first thing to observe from the graphs is that the turn-on process present more severe spikes and higher frequency oscillations compared to the turn-off process. It is worth noting that, even though the SiC Schottky diode has no reverse recovery charge, a reverse-recovery-like overshoot is observed in the current during the turn-on process. This overshoot is created by two capacitive current contributions. The first one is the capacitive current necessary for charging the junction capacitance of the SiC Schottky diode and the other one is originated from the inductor's parasitic capacitance (see chapter **??**).

Since the low EPC inductor with no additional external capacitance was used, this overshoot is considered to be contributed only by the charging process of the junction capacitance of the diode. Although the capacitive charge required for the junction capacitance of the diode is considered constant for different voltages [107] and can be calculated by integrating the area under the current curve that is bigger than the inductor current, a small increase in the value of the overshoot is observed as the inductor's current increases. This is caused by the increased current slew rate (di/dt) at the moment that the drain current reaches the desired value of the inductor's current (for $I_L = 2A$ the di/dt is about $877A/\mu s$ while for $I_L = 10A$ is $di/dt = 3170A/\mu s$).

As the value of the inductor's current increases, the switching transition of the turn-on process becomes longer. The time required for the drain-source voltage to drop to zero increases from 5nsec when switching at 2A to 7nsec at 10A, which is translated to a 40% increase on the switching time. This increase is also due to the high di/dt across the L_{int1}, which, as discussed in chapter 3, acts as the source inductance for the GaN die slowing down its turn-on process. Combined with the bigger overshoot, this increase in the transition time will have significant impact on the turn-on switching energy.

When the charging process of the junction capacitance is complete, the drain current returns to the inductor's current with a high di/dt, triggering oscillations to the circuit. Since the DUT is already on, this ringing current is caused by the switching power loop inductance resonating with the junction capacitance of the diode [71]. The frequency of the oscillation ($f = 215MHz$) remains the same in all cases verifying that the oscillation is determined by the circuit's parasitics and not by the inductor's current value.

On contrary, the turn-off switching process is getting shorter as the inductor's current increases. The turn-off process is basically determined by the GaN transistor's channel current, which can not be captured by the measurement equipment. As explained in section 3.2.2, the GaN HEMT features a unique intrinsic current source mechanism, which depends on the value of the inductor's current, and effectively decreases the falling time of the channel current. When the channel is totally shut down, the junction capacitance of the DUT is getting charged by drawing part of the inductor's load and the drain-source voltage increases. In the meanwhile, the junction capacitance of the SiC Schottky diode is discharged by also drawing part of the inductor's current and the voltage across it drops to zero [71]. Consequently, the value of the inductor's current influence significantly the turn-off process. This can be verified by the figures 5.10 and 5.12, where the drain current drops to zero in 31nsec when switching at 2A while when switching at 10A it requires only 8.5nsec.

Looking at the turn-off current waveforms, a change in the slew rate is observed a few nanoseconds before the drain-source voltage reaches the dc bus voltage. This change is related to the moment that the voltage across the top diode drops to zero. As the value of the diode's junction capacitance is smaller than the DUT's one, it is expected to discharge faster and the voltage across the diode to drop to zero before the drain-source voltage of the GaN HEMT increase to the dc bus voltage. At this moment, the value of the transistor's current will determine the remaining energy of the parasitic inductors [73]. When the current has dropped close to zero, as in the case of switching at 2A, the remaining energy is small and the overshoot of the DUT's drain-source voltage is also small. As the value of the inductor's current increases, so does the remaining energy in the parasitic inductors causing a higher overshoot of the voltage (see case of switching at 5A & 10A), which eventually will trigger oscillation to the circuit.

When the GaN HEMT starts blocking the full voltage, the diode's junction capacitance is effectively bypassed by the diode and thus, the ringing current is caused by the switching power loop inductance resonating with the junction capacitance of the GaN HEMT. As the junction capacitance of the GaN HEMT is bigger that the diode's one, the frequency of the oscillation ($f = 117MHz$) will be smaller compared to the one during turn-on.

Summarizing the analysis of the switching behavior, we can conclude that:

- during the turn-on transition, the charging process of the junction capacitance of the diode will increase the current overshoot. As the inductor's current increases, the current overshoot and the switching transition of the turn-on process increase. The combination of these two makes the turn-on energy a strong function of the inductor's current.
- the turn-off switching process is getting shorter as the inductor's current increases, due to the unique intrinsic current source mechanism of the GaN HEMT. However, the turn-off energy stays almost constant under different values of the inductor's current.
- the frequency of oscillations during the turn-on process is higher than during the turn-off, because the switching power loop inductance resonates with the junction capacitance of the diode, which is smaller compared to the junction capacitance of the GaN HEMT

5.3.2 Parametric Study of the inductor's EPC on the switching behavior of the GaN HEMT

As discussed in chapter 3 the equivalent parasitic capacitance of the inductor is effectively in parallel with the top switch's junction capacitance. Thus, it is expected to have the same effect on the switching behavior of the DUT. The DUT was switching at 400V/5A and the drain-source voltage and the drain current were recorded for a period of $200ns$ to compare with the calculated results from the analytical model. It can be seen that the EPC not only impact the main switching transition, but the voltage and current ringing as well.

Comparison of the switching transitions for the different values of the inductor's EPC are shown in figures 5.14, 5.15, 5.16, and 5.17:

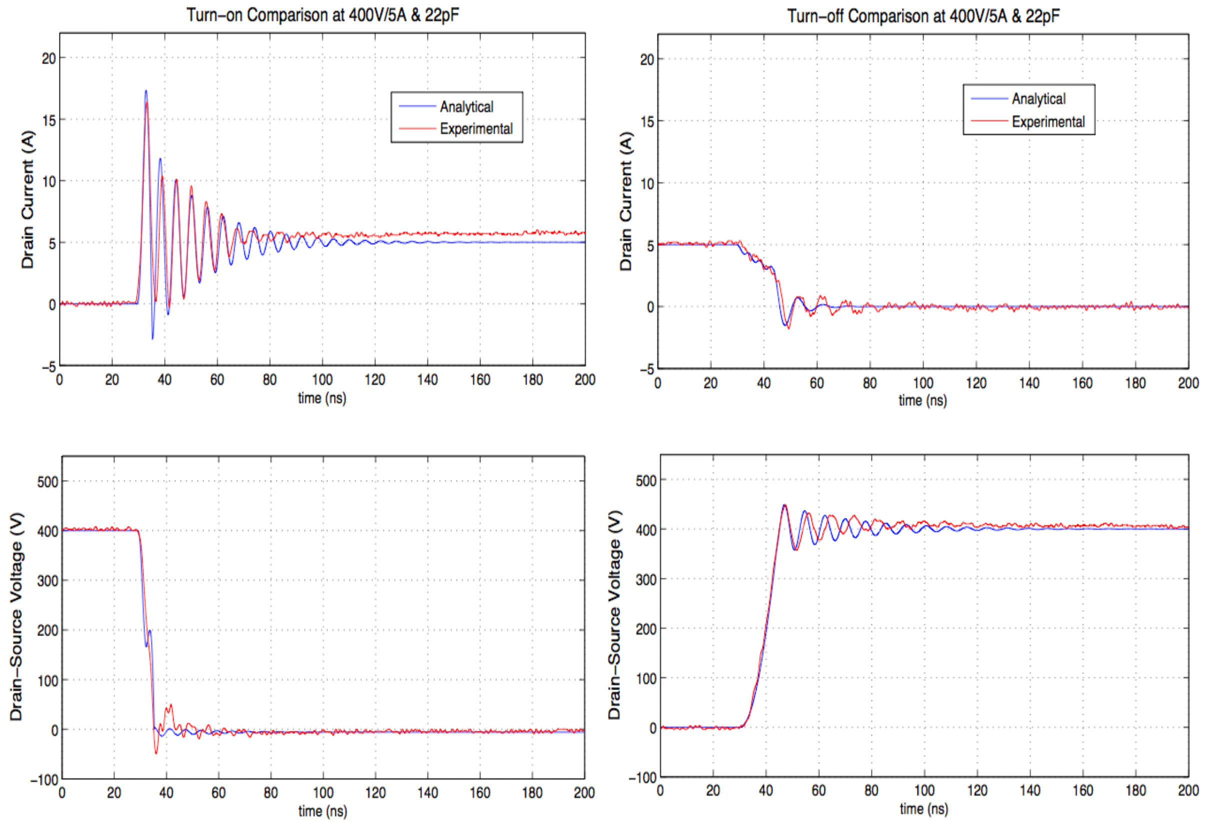


Figure 5.14: Comparison of the turn-on & turn-off switching transitions at 400V/5A & 22pF

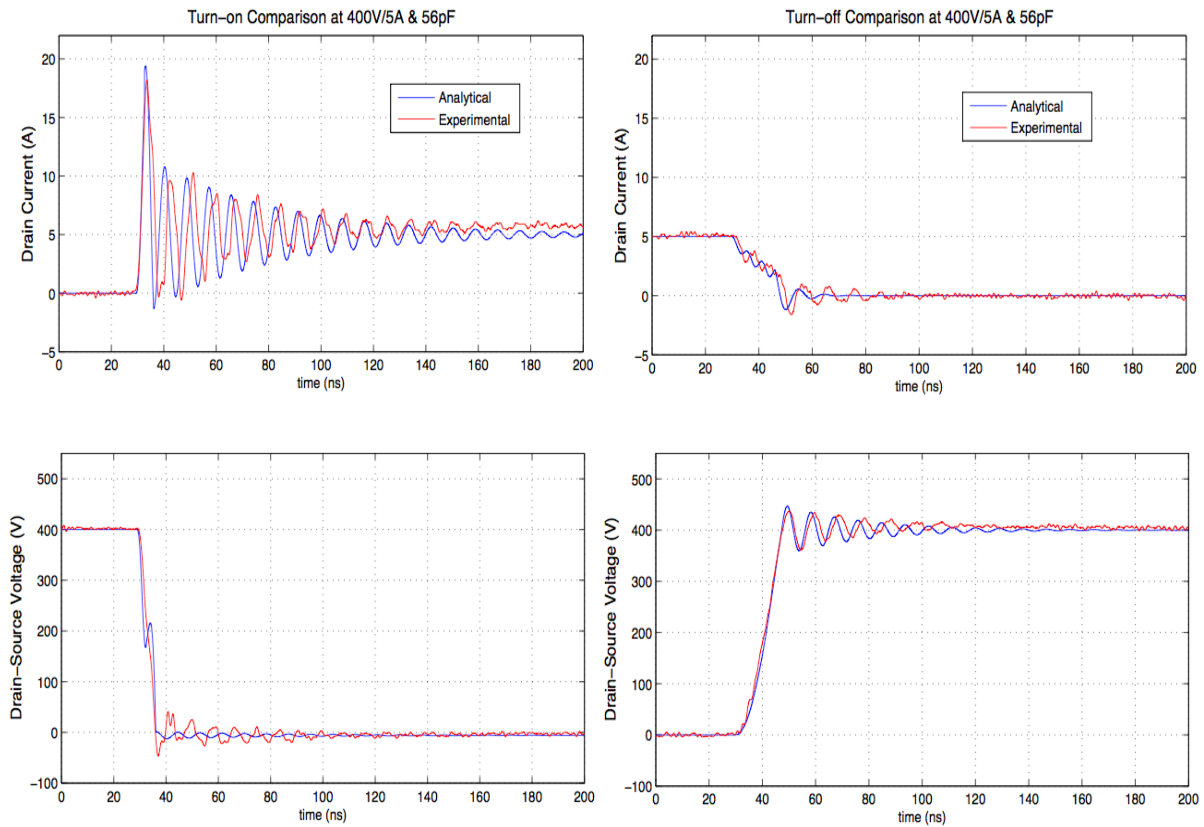


Figure 5.15: Comparison of the turn-on & turn-off switching transitions at 400V/5A & 56pF

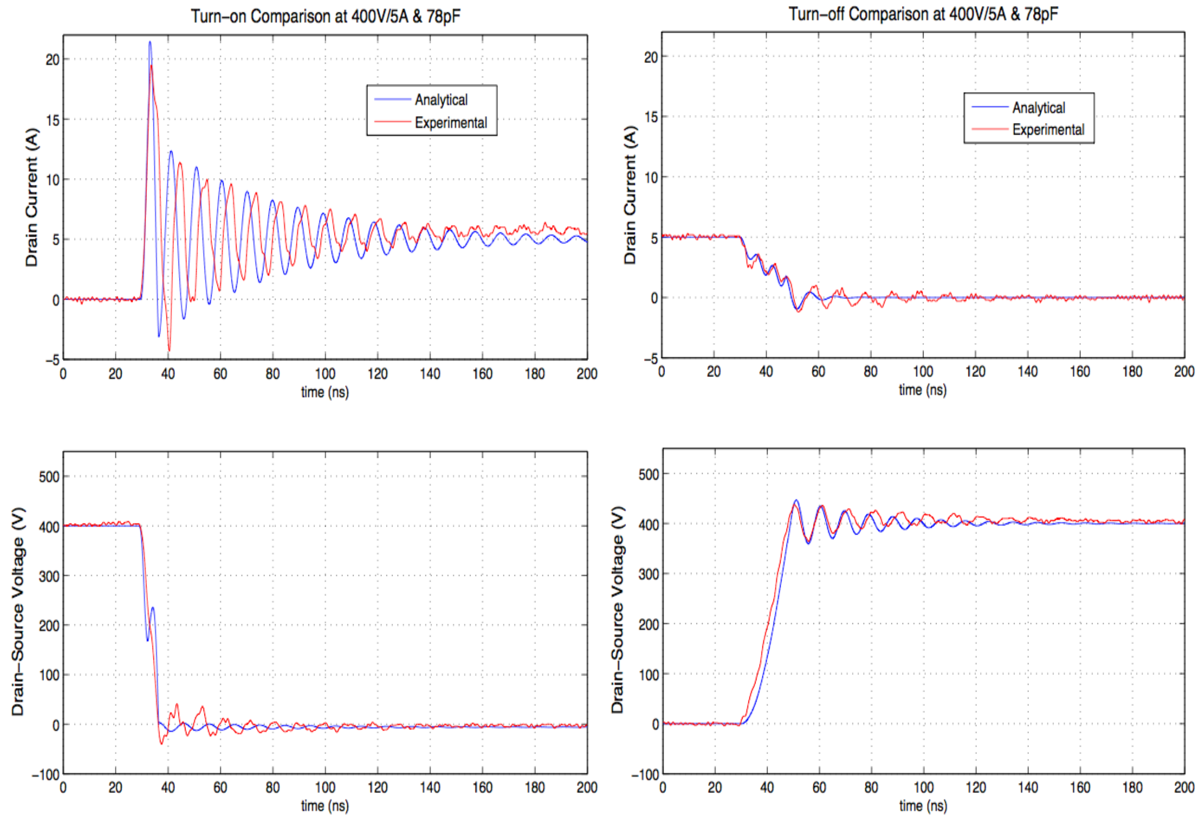


Figure 5.16: Comparison of the turn-on & turn-off switching transitions at 400V/5A & 78pF

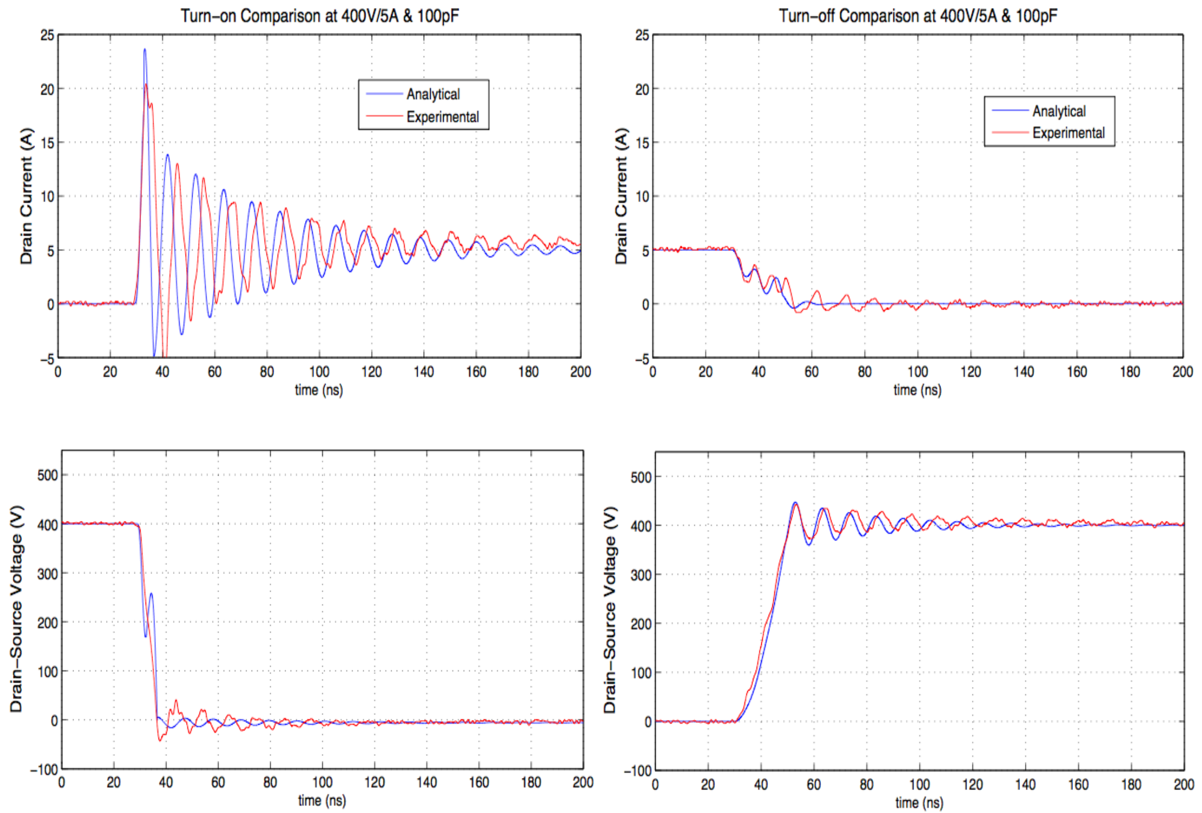


Figure 5.17: Comparison of the turn-on & turn-off switching transitions at 400V/5A & 100pF

Analysis of the comparison between the experimental and analytical results

The figures above show the waveform comparisons between the double-pulse test and the calculated results of the proposed analytical model during the switching transitions, while the inductor's EPC increases. It can be seen that the analytical model is able to match the experiments on the voltage and current slope rate, especially during turn-off. However, as already mentioned above, an increase of the voltage during the turn-on process, due to the discrete values of the parasitic capacitances used in the model, is observed. This increase is getting bigger as the EPC increases, since the EPC is effectively added to the junction capacitance of the top switch. Although this increase gets bigger with the EPC, the voltage still manages to match the falling time of the experimentally measured drain-source voltage.

On the contrary, the drain current during the turn-on transition is not accurately predicted. Although the increase slop rate is matched perfectly, the current reaches a higher peak value and then drops faster to zero triggering oscillations to the circuit. This is caused due to the fact that in the analytical model, the total capacitive charge of the top switch is used in order to find the peak value of the current and on the assumption that only part of the EPC is getting charged during the main switching transition. Thus, only part of the additional EPC's charge contributes to the current overshoot, while the rest is in parallel to the top switch's junction capacitance and gets charged by resonating with the circuit's parasitic inductance.

Finally, the oscillation frequencies and damping effects can been considered reasonably well predicted, but they present differences due to inaccurate high-frequency parasitic inductance and stray resistance of the circuit. Despite the inaccuracies and the assumptions of the model, the switching energy calculated with seems to match well the experimental results, as it is shown in the following graph:

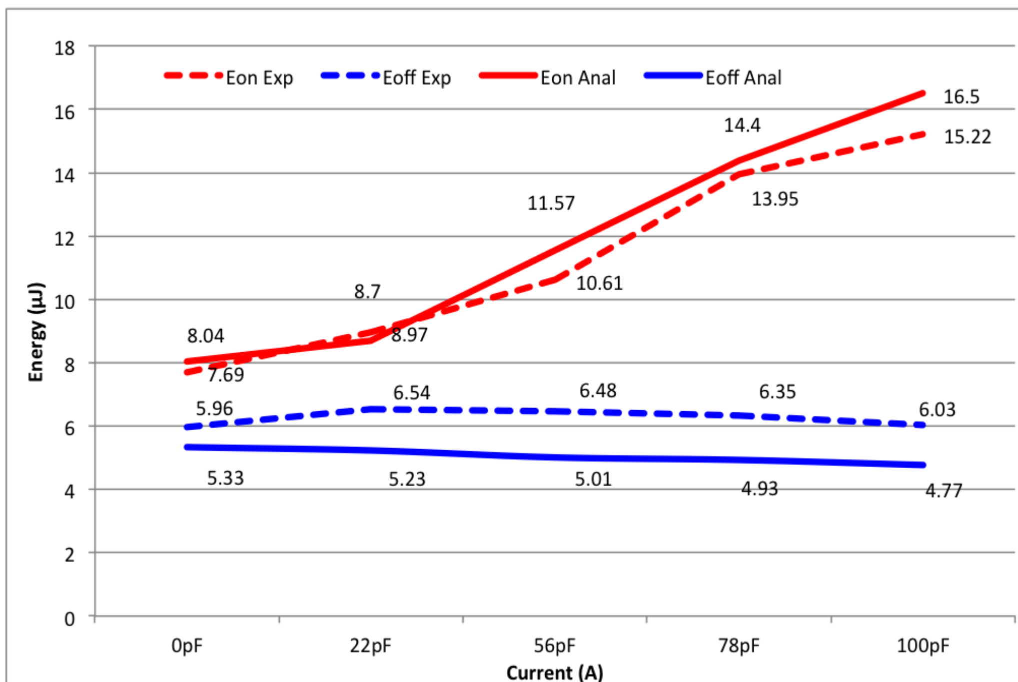


Figure 5.18: Switching energy comparison between the experimental & the analytical results

Analysis of the EPC's impact on the switching behavior

When a top switch with no Q_{rr} is used, the overshoot in the current during the turn-on process is created by two capacitive current contributions. The first one is the capacitive current necessary for charging the junction capacitance of the SiC Schottky diode and the other one is originated from the inductor's parasitic capacitance.

As the value of the EPC increases, so does its contribution to the DUT's drain current overshoot. This statement can also be verified by the comparison of the measured current waveforms as shown in figure 5.19. This figure also helps to understand that the contribution of the EPC does not only translated into a higher peak value of the drain current, but also to a wider area under the drain current. Moreover, it can be seen that the time required for drain-source voltage to drop to zero is increased from about 5nsec to 7nsec. This increase is actually caused by the higher overshoot and the higher di/dt across the L_{int1}, which acts as the source inductance for the GaN transistor slowing down its turn-on process.

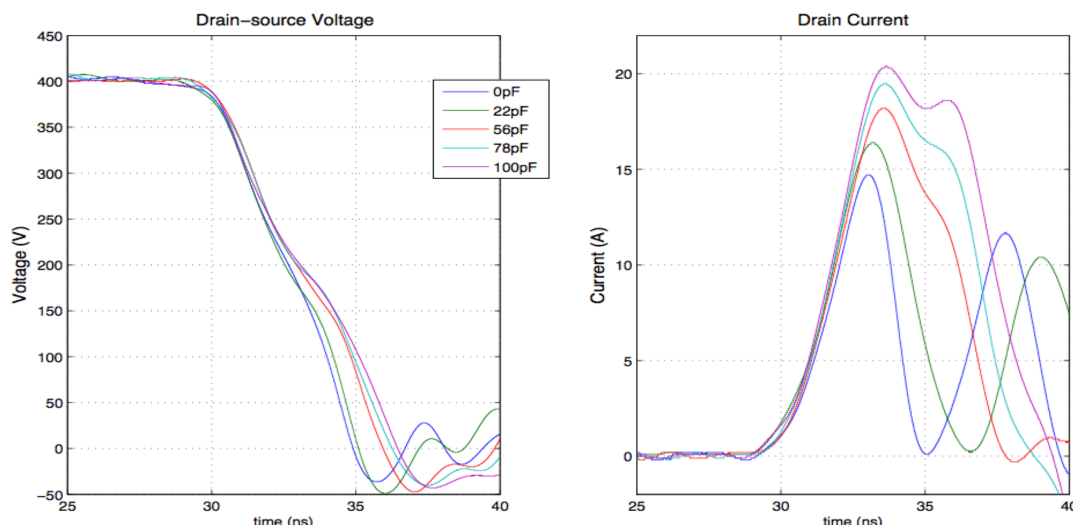


Figure 5.19: The influence of the inductor's EPC increase on the drain-source voltage (left) and the drain-source current (right) during the turn-on process with a SiC Schottky diode

When the charging process of the junction capacitance and the inductor's EPC is complete, the drain current returns to the inductor's current with a high di/dt triggering oscillations to the circuit. The higher the overshoot, the higher the di/dt that will trigger the oscillation and the envelop of the oscillation increases as the EPC increases. Since the drain-source voltage drops to zero very fast and the DUT is already on, the ringing current will be caused by the switching power loop inductance resonating with the junction capacitance of the diode (Cj_d) in parallel with the inductor's EPC. Therefore, as the EPC added in parallel with the junction capacitance of the diode increases, the frequency of the oscillation is expected to decrease according to the equation:

$$f = \frac{1}{2\pi\sqrt{Lp_{loop} \cdot (Cj_d + C_{EPC})}}$$

Additionally, from this equation can be verified that the switching loop inductance is the one that resonates with the junction capacitance of the diode and the EPC, since the

inductance calculated with every value of EPC and its corresponding frequency of oscillation remains almost the same.

As regards to the turn-off process, there is no significant change observed in the waveforms beside a small increase in the time required for the drain-source voltage to reach the dc bus voltage and for the current to drop to zero. As we discussed in section **??** above, during the turn-off process the junction capacitance of the top switch is getting discharged by drawing part of the inductor's current. Since the additional EPC is effectively in parallel with this capacitance, bigger part of the inductor's current will be drawn in order to discharge both capacitances. This is actually what causes the drain-source voltage to increase slower.

Moreover, with the increase of the EPC, there is an oscillation appears in the current before the drain-source voltage reaches the dc bus voltage. This is probably caused by the EPC resonating with the parasitic inductances formed by the inductor interconnection. When the GaN HEMT starts blocking the full voltage and the diode's junction capacitance and the EPC are effectively bypassed by the diode, the frequency of the current's and voltage's oscillation is due to the power loop inductance resonating with the junction capacitance of the DUT.

Summarizing the analysis of the influence of the inductor's EPC on the switching behavior, we can conclude that:

- during the turn-on transition, the inductor's EPC constitutes another capacitive contribution to the drain current's overshoot. As the inductor's EPC increases, so the does the current's overshoot and the switching transition. The combination of these two causes the turn-on switching energy to increase with the increase of the EPC.

- during the turn-off switching process, the inductor's EPC is in parallel with the junction capacitance of the top switch and they are both getting discharged by drawing part of the inductor's current. Thus, the drain-source voltage increases slower, as the EPC increases.

- the current oscillation during the turn-on process is caused by the switching power loop inductance resonating with the junction capacitance of the diode (Cj_d) in parallel with the inductor's EPC. Consequently, as the EPC increases the frequency of oscillations decreases. However, the envelope of the oscillation increases with the EPC, due to the higher di/dt that triggers the oscillation and the bigger capacitance that needs to be charged during the turn-on process.

5.4 Investigation of the GaN HEMT's switching behavior with an active top switch

Although the analytical model can not model the case of a top switch with reverse-recovery charge, the influence of top device with Q_{rr} on the DUT's switching behavior was examined experimentally. Again, the DUT was subjected at 400V drain-source voltage and different values of inductor's current (2A, 5A and 7.5A). Measurements of the switching transitions for 2A, 5A and 7.5A value of the inductor's current are shown in the graphs in figure 5.20. The waveforms are recorded for a period of 100$nsec$, which again is long enough for the ringing to settle down before the next switching takes place. The gate resistance for this set of experiments is set at 14Ω for turn-on and 0Ω for the turn-off process.

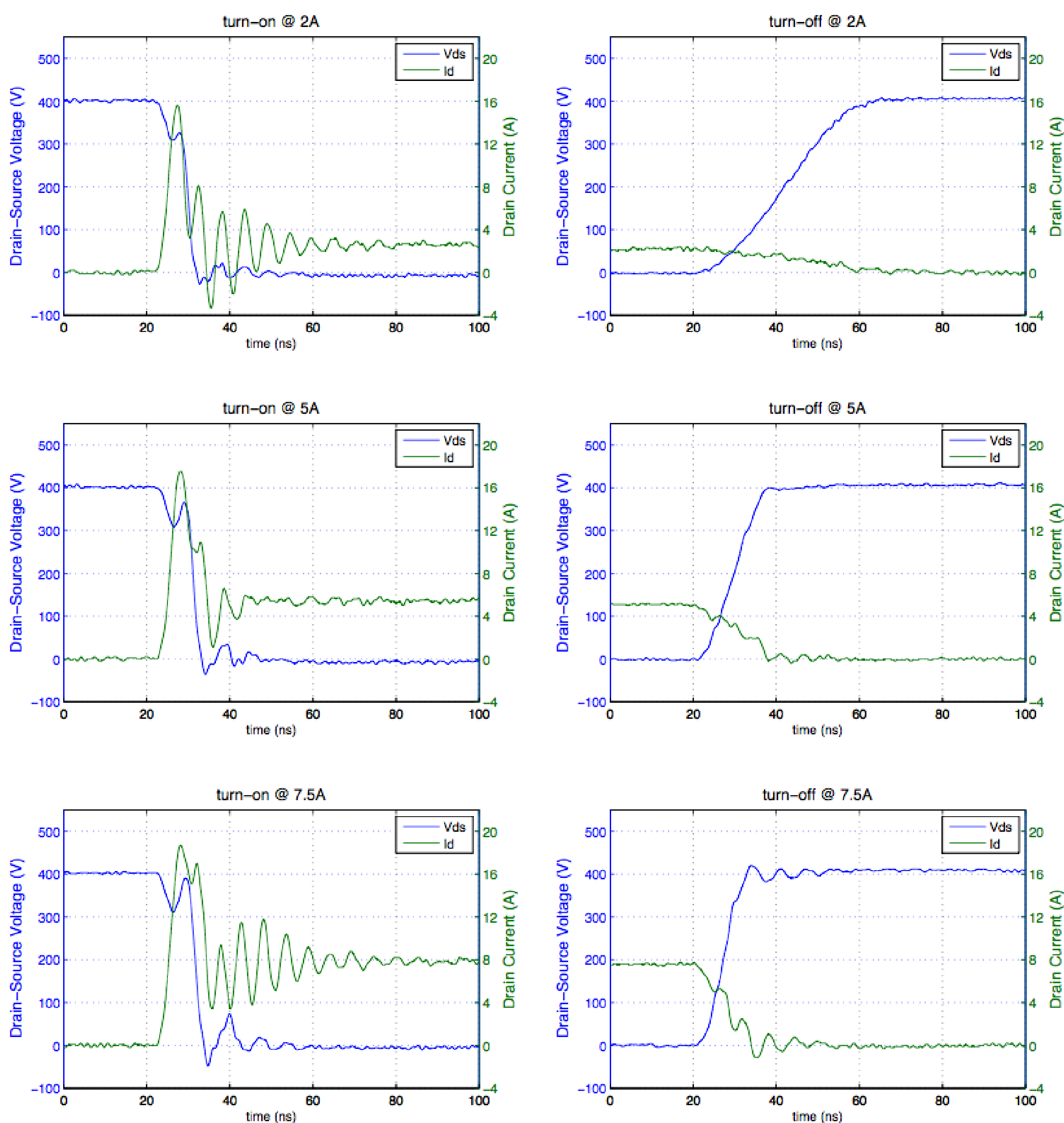


Figure 5.20: Turn-on & turn-off transitions with a GaN HEMT as top switch. Blue waveform is the drain-source voltage and the green is the drain current in all graphs

The turn-on process again presents more oscillations and severe spikes compared to the turn-off process, which in this case is smoother. Even though a bigger gate resistance is used in this set of experiments slowing down the DUT's switching transition, the current overshoot during the turn-on process is larger than in the case with the SiC Schottky diode. This is caused by two different characteristics of the GaN HEMT, used as the top switch: *a*) the reverse recovery charge (Q_{rr}) due to the body diode of the low voltage Si MOSFET, and *b*) the larger junction capacitance compared to the SiC Schottky diode. These characteristics, and especially the Q_{rr} will cause the switching transition of the turn-on process to be longer compared to the turn-on transition where a SiC Schottky diode was used.

In order for a device with Q_{rr} to attain its blocking capability, the stored charge in its junction needs to be extracted or neutralized [108]. This excess current will be eventually added to the inductor's current becoming one more contribution to its overshoot. As there is no external capacitance added in parallel with the inductor, the overshoot observed in the current waveforms constitutes only by the reverse recovery effect and the charging process of the junction capacitance of the top switch ($Q_{rr} + Q_{Ctop}$). The charging process of the junction capacitance of the top switch starts when the reverse recovery effect is complete. However, there is no physical indication when the Q_{rr} recombination process is complete and it is difficult to distinguish which portion of the area is due to the Q_{rr} and which due to the Q_{Ctop}. Moreover, calculating the current due to the reverse recovery effect becomes more complicated, since it is related to the value of the inductor's current and the di/dt at the moment when drain current equals the inductor current, which is determined basically from the loop inductance.

Although it is quite complicated to accurately distinguish the stages of the turn-on process, we can assume that the current and voltage waveforms follow a specific pattern by looking at figure 5.20. The first peak of the current is assumed to be mostly contributed by the Q_{rr}. This can be verified by the fact that the drain-source voltage of the DUT starts to increase rather than continue decreasing a few nanoseconds before the current reaches its peak value. This is caused by the high di/dt across the L_{int1}, which slows down the increase of the GaN transistor's gate-source voltage and eventually saturates the channel as the reverse recovery process is not complete yet and the GaN HEMT is not fully turned on [73].

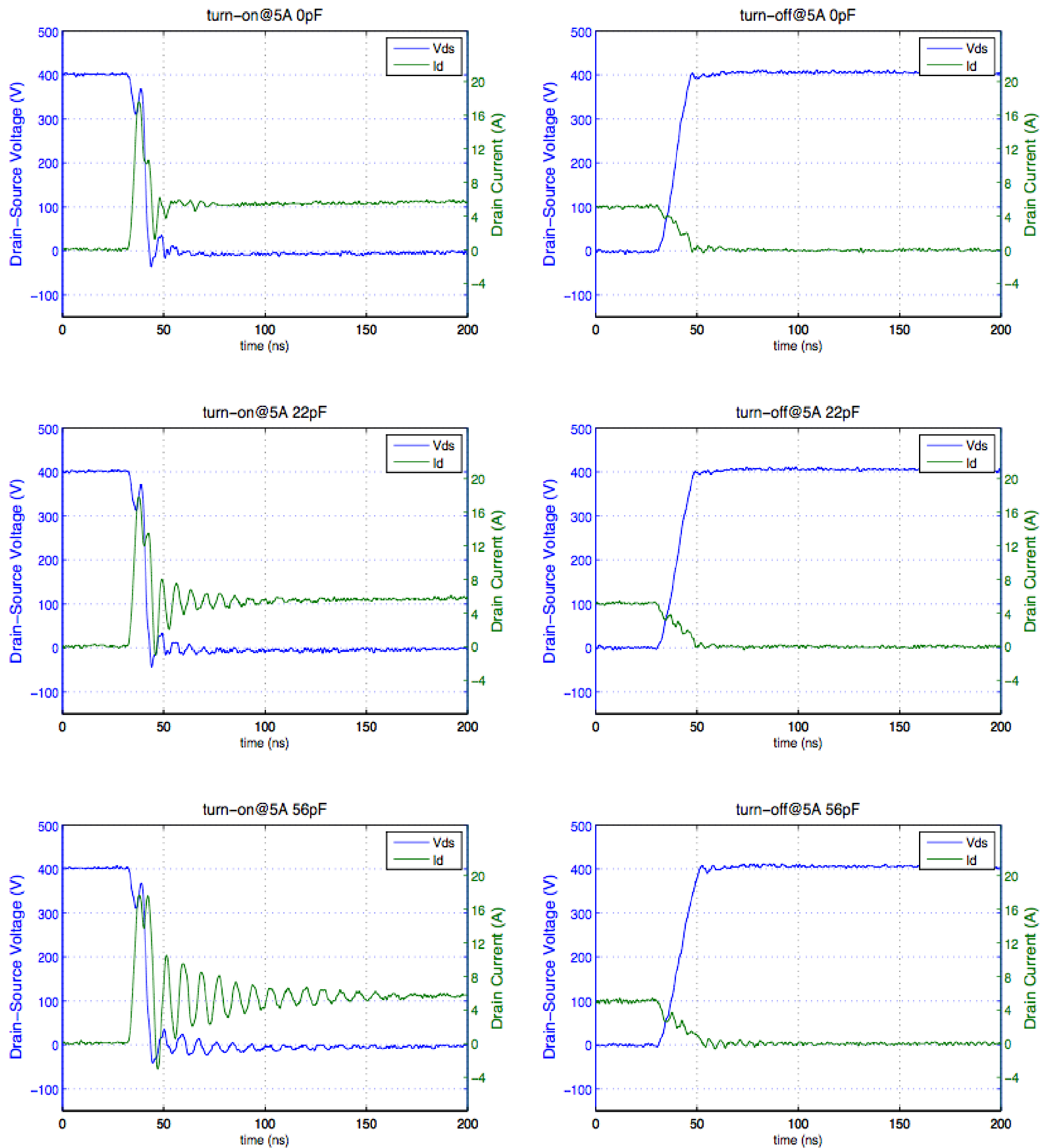
As shown in the figure 5.20, the turn-on switching transition increases as the inductor's current increases. The time required for the drain-source voltage to drop to zero increases from 9.5nsec when switching at 2A to 11.5nsec at 7.5A. When the charging process of the junction capacitance is complete, the drain current returns to the inductor's current with a high di/dt triggering oscillations to the circuit. The DUT is already on and this ringing current is caused by the switching power loop inductance resonating with the junction capacitance of the top GaN HEMT. The junction capacitance of the GaN HEMT is bigger than SiC Schottky diode's one causing the frequency of the oscillation to be smaller ($f = 185MHz$). Once again, the frequency of oscillation remains the same regardless the inductor's current value verifying the initial statement.

As regards to the turn-off process, it is getting shorter as the inductor's current increases for the same reasons explained in section 5.3.1. However, there is a small increase in the

time required for the current to drop to zero, due to the fact that the junction capacitance of the top switch is bigger and more time is required for its discharge. The discharge process of the top switch's junction capacitance starts slightly before the charging process of the bottom's one and this might be the reason for the small oscillation observed in the drain-source voltage during switching at 7.5A.

5.4.1 Parametric Study of the inductor's EPC on the switching behavior of the GaN HEMT with an active top switch

The SiC Schottky diode was replaced by a GaN HEMT and the same experiments as in the section 5.3.2 were conducted again. The waveforms captured are shown in figure 5.21.



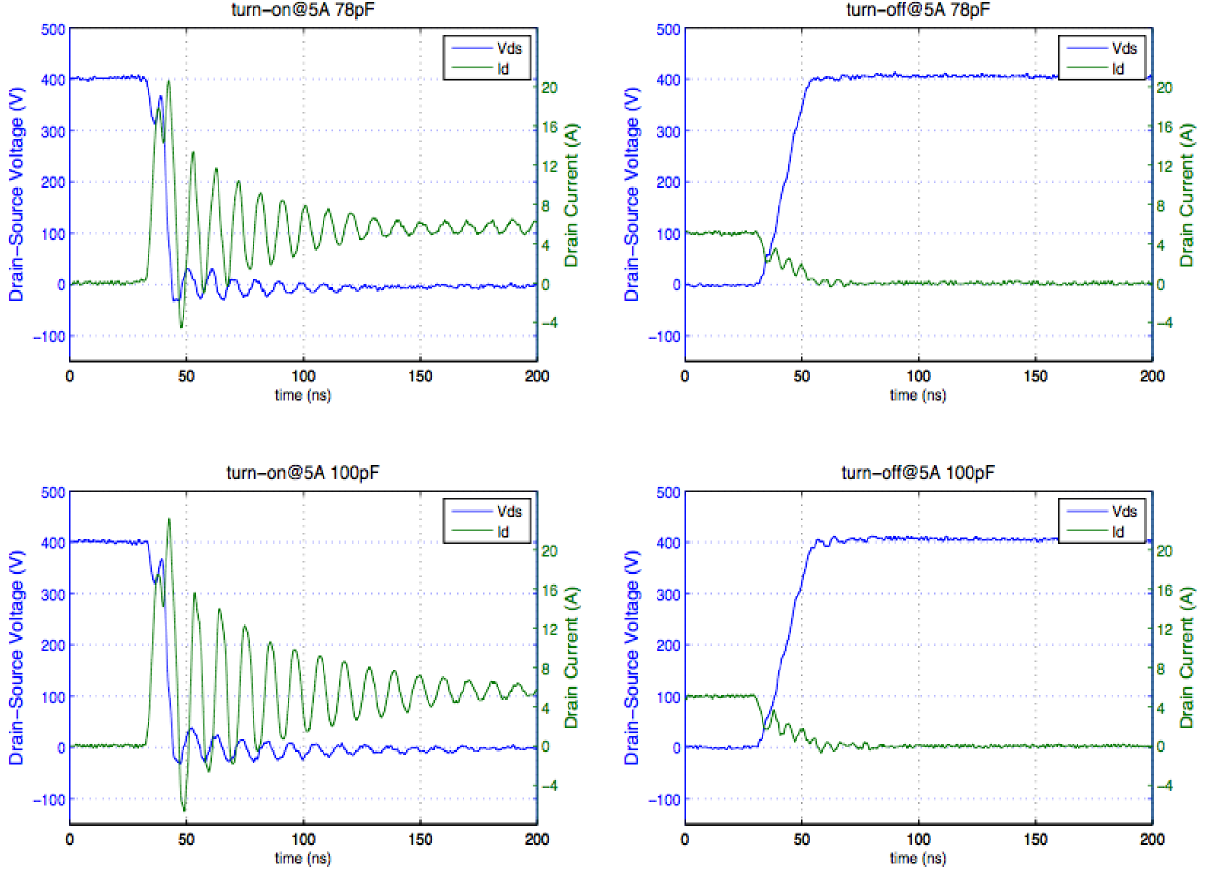


Figure 5.21: Turn-on/off transitions with a GaN HEMT as the top switch and increasing EPC. Blue waveform is the drain-source voltage, the green is the drain current in all graphs

As already discussed in the previous section, applying a top switch with Q_{rr} influences significantly the turn-on switching transition by increasing the current overshoot and the voltage falling time. As the impact of the inductor's EPC is basically added to the one of the top switch's junction capacitance, the overshoot of the turn-on current will be caused by the reverse recovery effect, the charging process of the top switch's junction capacitance and the current originated from the inductor's EPC.

However, the top switch's junction capacitance along with the inductor's EPC will start getting charged after the reverse recovery process is complete. From the waveforms captured during the experiments with no additional capacitance in parallel with the inductor (figure 5.20), we assumed that the first peak in the current's overshoot is mostly caused by the reverese recovery charge. This assumption can be verified again from the current and voltage waveforms shown in figure 5.22, as the first peak of the current's overshoot and the first part of the voltage's falling transition are exactly the same for all values of the inductor's EPC.

When the reverse recovery process is complete, the current overshoot consists of the capacitive current necessary for charging the junction capacitance of the top GaN HEMT and the inductor's parasitic capacitance. It can be seen that as the value of the inductor's EPC increases, so does the value of the current's second peak. Moreover, this second increases of the current will induce a voltage across the L_{int1} causing a small delay on

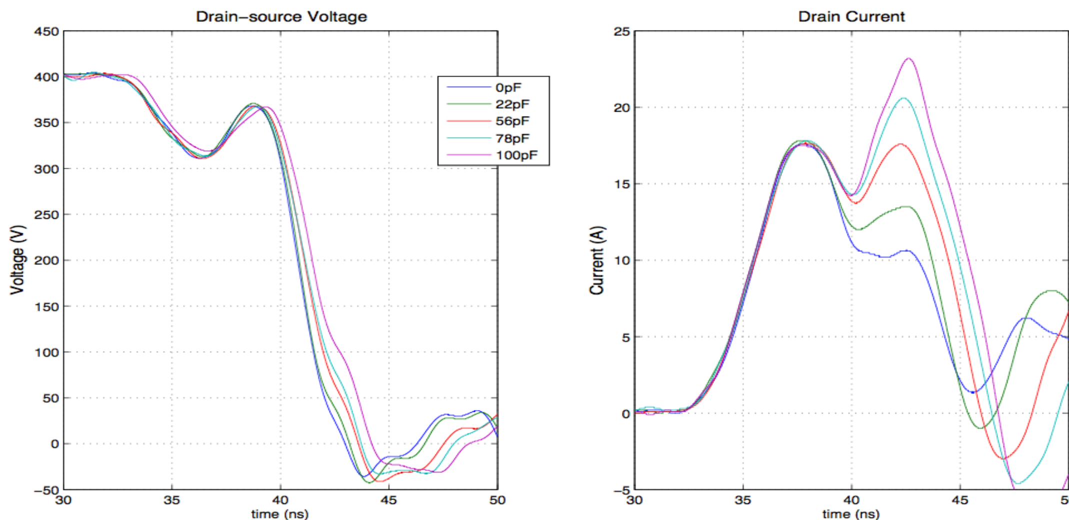


Figure 5.22: The influence of the inductor's EPC increase on the drain-source voltage (left) and the drain-source current (right) during the turn-on process with a GaN HEMT

the voltage's falling time. Finally, the charging of these capacitances is complete and the current will return to the inductor's current value. After this point, the behavior is the same as explained in the previous case. The envelope of the oscillation triggered in the circuit depends on the value of the current's overshoot and di/dt, and the frequency decreases as the value of the EPC increases.

The turn-off process behaves like in the case with the SiC Schottky diode. There is no significant changes in the waveforms beside a small increase in drain-source voltage's rising time and current's falling time. Moreover, with the increase of the EPC, an oscillation appears again in the current while the drain-source voltage rises to the dc bus voltage. This is probably caused by the EPC resonating with the parasitic inductances formed by the inductor interconnection, until the voltage across the top switch collapses to zero and this capacitance is effectively bypassed by the body diode of the GaN HEMT.

5.4.2 Influence of the gate resistance on the switching behavior of the GaN HEMT with an active top switch and additional EPC

As already discussed above, the Q_{rr} is influenced also by the di/dt of the current at the moment that it reaches the inductor's current. In order to change this slew rate of the current, different values of the gate resistance were used. The case of an inductor's EPC equal of 56pF was used and the gate resistance changes from 10Ω to 21.5Ω. The measured waveforms are shown in the following graphs.

It can be seen that as the gate resistance increases and based on the analysis above, the first peak of the current, which is caused due to the Q_{rr} as explained above, decreases, but the second peak, which is caused by the charging process of the top switch's junction capacitance and the inductor's EPC, increases. This verifies that the reverse-recovery process is complicated and not easy to identify which portion of the area is due to the Q_{rr}, which due to the Q_{Ctop}, and which due to the inductor's EPC. However, the oscillation frequency remains almost the same in the three cases.

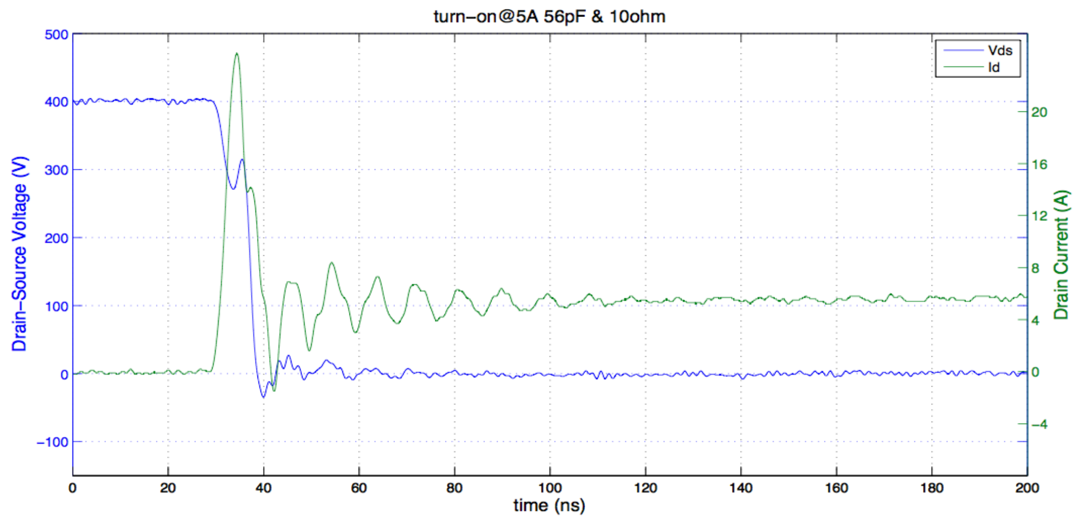


Figure 5.23: Turn-on switching transition with $R_g = 10ohm$

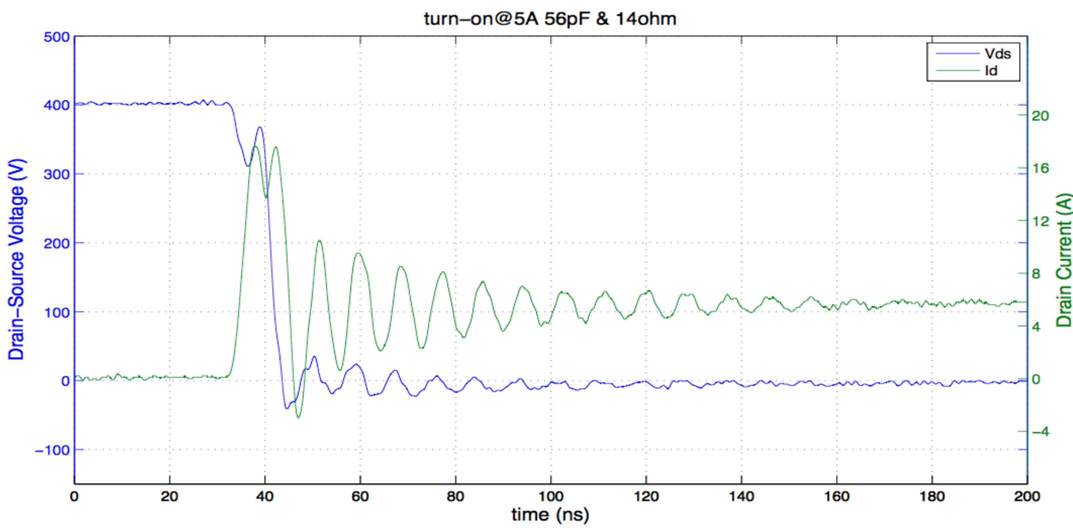


Figure 5.24: Turn-on switching transition with $R_g = 14ohm$

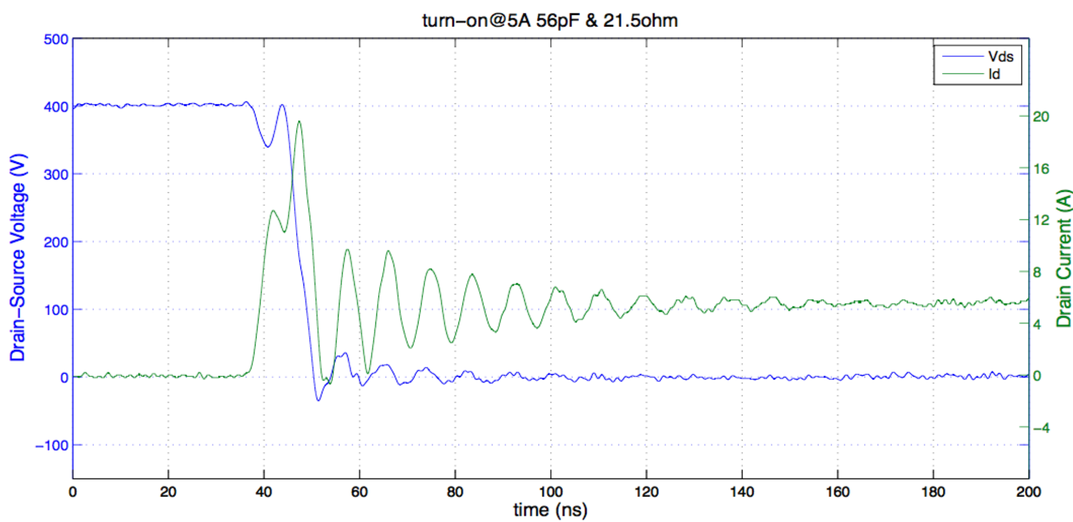


Figure 5.25: Turn-on switching transition with $R_g = 21.5ohm$

5.5 Comparison of the two examined cases

In order to compare the influence of the top switch on the DUT's switching behavior, a comparison of the turn-on/off switching energy will be made. The dissipated energy during the switching transitions is calculated by integrating the area where the crossover of the drain-source voltage and the drain-source current occurs. In figure 5.26 the calculation of the turn-on switching loss for both cases while switching at 5A is shown.

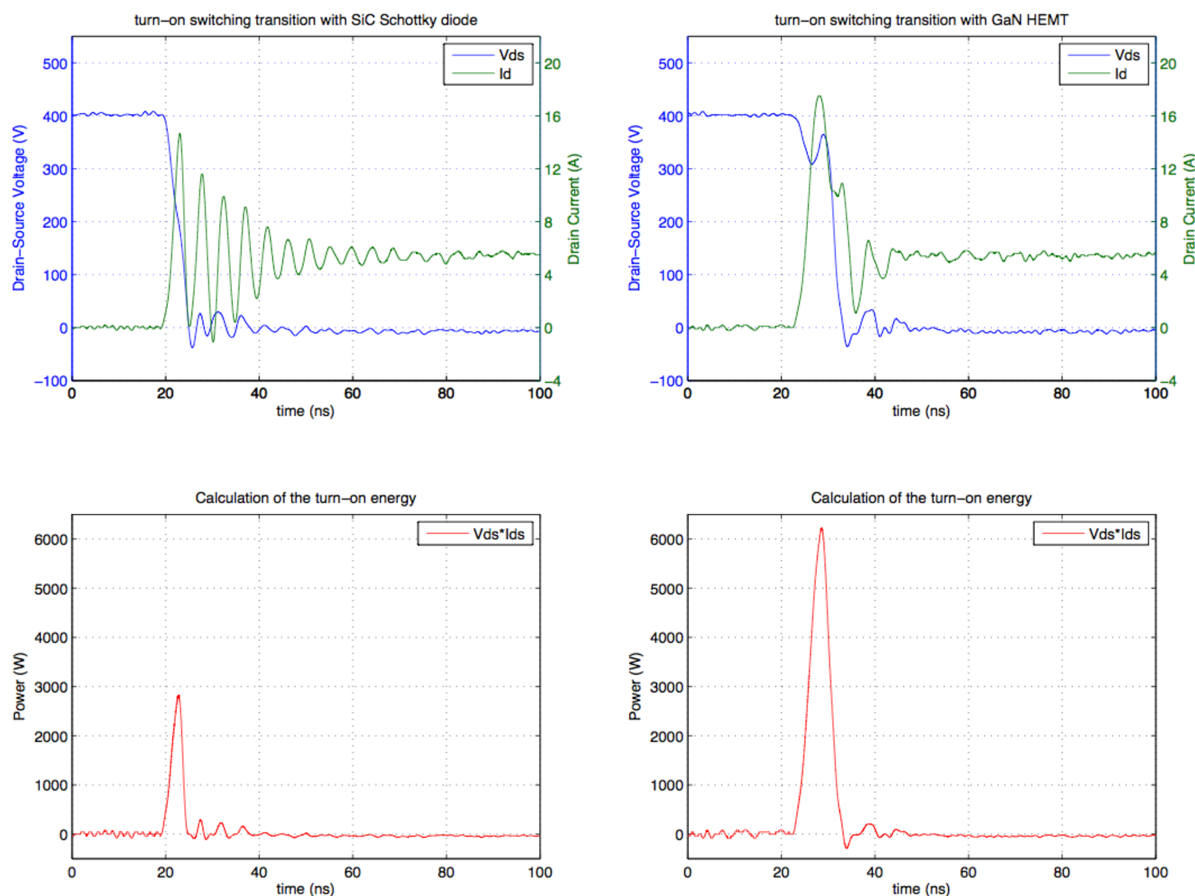


Figure 5.26: Calculation of the turn-on/off energy. Blue waveform is the drain-source voltage, the green is the drain current and the red is the power loss

From the figures 5.10, 5.11, 5.12 and 5.20 shown above, it is observed that the turn-on switching transition increases as the inductor's current increases, while the turn-off switching transition decreases. This increase in the turn-on switching time combined with the higher value of the current overshoot will significanlty increase the turn-on switching loss. The calculation of the dissipated energy during the turn-on/off process for the different values of the inductor's current is shown in figure 5.27. As we can see from the charts, the turn-on energy is strong function of the inductor's current, whereas the turn-off energy is small and remains almost constant for both cases.

Next, the influence of the inductor's equivalent parasitic capacitor on the GaN HEMT's switching behavior for both cases (SiC Schottky diode and GaN HEMT) was investigated in the section 5.3.2 and 5.4.1. It was shown that the turn-off transition stays essentially the same, since the inductor's EPC is bypassed by the freewheeling diode, while the tran-

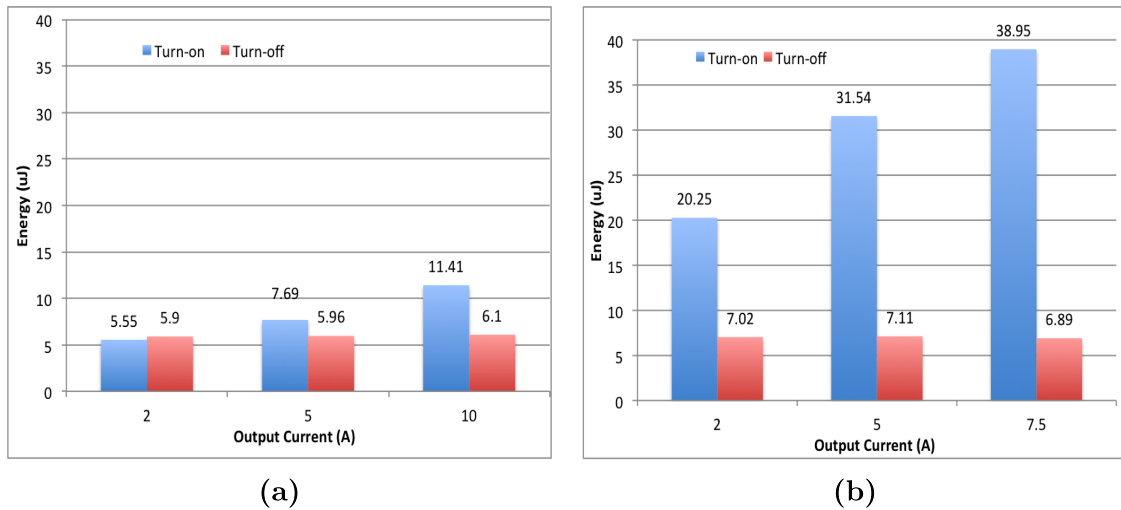


Figure 5.27: Calculation of the dissipated turn-on/off energy for a (a) SiC Schottky diode as top switch and (b) GaN HEMT as top switch

sistor's current during the turn-on transition presents remarkable changes as the value of the inductor's EPC increases. The inductor's EPC is in parallel with the junction capacitance of the top switch and, thus, it contributes to the current's overshoot increasing eventually the turn-on switching loss. The energy dissipated during the turn-on/off transitions is calculated for both examined cases while different values of the inductor's EPC are used and the results are summarized in the charts shown in the figure 5.28 below.

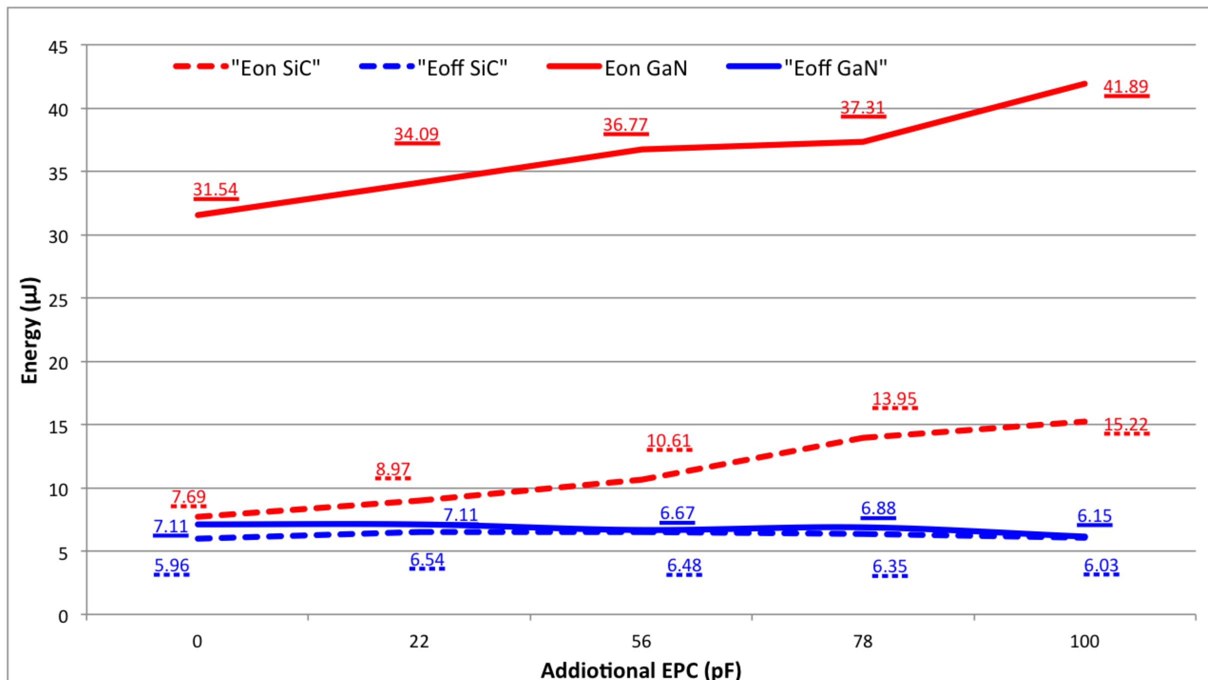


Figure 5.28: Calculation of the conduction losses for differenet values of the inductor's EPC

Summarizing the influence of the top device on the switching behavior of the GaN HEMT, we can conclude that:

- applying an active switch with reverse recovery charge and bigger junction capacitance will deteriorate the switching transition and significantly increase the turn-on

switching loss. As shown in charts in figure 5.27, an increase of about 300% in the energy dissipated during turn-on process is observed when the SiC Schottky diode is replaced by a GaN HEMT.

- the increased value of the inductor's EPC, not only will increase of the turn-on switching loss, but it will also cause the transistor's current to oscillate after the DUT is fully on. This will lead to more conduction losses of the DUT. The calculation of the conduction losses is shown in the figure below.

- although the conduction losses are small compared to the switching losses, the high oscillations in the transistor's current might cause further issues. For further increase in the switching frequency, this oscillation might not get completely damped causing problems in transistor's operation.

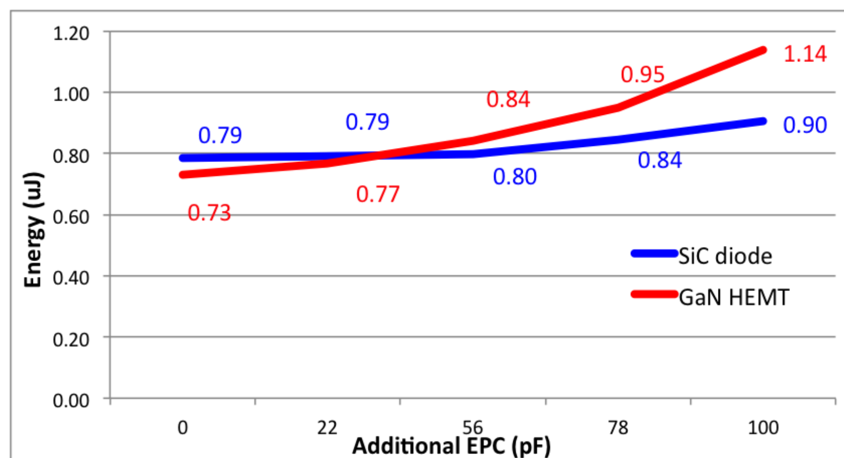


Figure 5.29: Calculation of the conduction losses for differenet values of the inductor's EPC

5.6 Discussion

In this chapter the operation of a DPT was thoroughly explained and typical waveforms of the gate-source voltage, drain-source voltage, and drain current were presented in figure 5.2. Considerations regarding the design of the PCB and how to reduce its impact on the switching performance of the DUT are discussed. Moreover, the measuring equipment was selected so as to meet the requirements of the circuit and capture the aforementioned waveforms with adequate accuracy and fidelity.

The inductor design was of great importance for this thesis project, since the influence of one of its parasitic elements (equivalent parasitic capacitance) was chosen to be investigated. For this, a low EPC inductor was needed and ways of how to design one are discussed in section 5.2.3. Additional capacitors were placed in parallel with the indcutor in order to model bigger values of EPC. This modeling approach was verified by building another inductor with bigger value of EPC and comparing the switching waveforms of the DUT. These waveforms matched well enough the ones when the initial inductor with the same value of capacitor placed in parallel were used.

Next, the analytical loss model developed in chapter 3 was verified by investigating the

the switching behavior of the high-voltage cascode GaN HEMT with a Sic Schottky diode as top switch and the influence of the inductor's EPC on that switching behavior. It was shown that the waveforms calculated with the analytical model were able to match the experimentally captured waveforms, despite the inaccuracies and the assumptions used in the model.

Finally, the influence of an active switch as the top switch of the DPT on the switching behavior of the high-voltage cascode GaN HEMT was examined experimentally. It was proven that applying an active switch with reverse recovery charge and bigger junction capacitance will deteriorate the switching transition and significantly increase the turn-on switching loss. Additionally, it was proven that the inductor's EPC not only contributes to the turn-on switching loss but also causes the transistor's current to oscillate, which might cause the transistor's operation to fail in higher frequencies.

Chapter 6

Conclusion

6.1 Conclusions

The main objective of this thesis project was to investigate the influence of the magnetic component's parasitic capacitance on the switching behavior of the high voltage GaN HEMT in cascode configuration. Many steps have been made towards that goal including the development of an analytical loss model for the high-voltage cascode GaN HEMT and the implementation of the inductor's parasitic capacitance impact in it. The construction of an inductor with low equivalent parasitic capacitance for the experimental part of the thesis. The design and manufacture of a double-pulse tester in order to experimentally verify the developed analytical loss model and investigate the switching behavior of the GaN HEMT under different conditions. Based on the discussions and results presented in this thesis project, the most important points are summarized here:

- An analytical loss model of the high-voltage cascode GaN HEMT was developed during this thesis project that includes the package parasitic inductances, the non-linearity of the junction capacitances of the low voltage Si MOSFET, but uses discrete values for the parasitic capacitances of the GaN HEMT and the top device, based on the voltage level of every transition stage. Moreover, it takes into consideration the impact of the inductor's EPC.

    - By using the proposed analytical model, the influence of the package parasitic inductances on the switching transitions of the device was investigated. From these results, the theoretical analysis was confirmed, indicating that the parasitic inductances L_{int1} and L_{int3} are the most critical for the switching transitions.
    - The verification of the model is shown in chapter 5, where the waveforms calculated with the analytical model match adequately the experimental results. The assumptions used in the model in order to implement the inductor's EPC cause discontinuities in the waveforms, but the switching energy dissipated during the turn-on and turn-off transitions calculated with the analytical model and with the experimental results are close enough. Finally, the oscillation frequencies and damping effects are predicted reasonably well.

- In order to characterize the device and eventually verify the analytical loss model, current and voltage measurements need to be taken during the turn-on and turn-off switching transitions. As the GaN HEMT is capable of switching are very high speed, there are issues and limitations that need to be taken into consideration in order to ensure the fidelity and the accuracy of these high frequency measurements. Thus, the voltage and current measuring techniques that will be used should meet the bandwidth requirements in order to capture the fast rise and fall time of the switching waveforms. Moreover, different probes possess different propagation delays and the probes need to be compensated after connected to the oscilloscope, otherwise there could be timing misalignments between the captured waveforms, eventually leading to measurement errors and wrong calculations of switching loss.

- A double-pulse tester was designed and manufactured during this thesis project in order to experimentally verify the developed analytical loss model and investigate the switching behavior of the GaN HEMT under different conditions. Apart from the investigation of the inductor's EPC influence on the switching behavior of the GaN HEMT, which was the main goal of the thesis, the influence of the reverse recovery of the top device of the DPT was also examined. Based on the comparison in section 5.5, we can conclude that:

    - applying an active switch with reverse recovery charge and bigger junction capacitance will eventually deteriorate the switching transition and significantly increase the turn-on switching loss. As shown in charts in figure 5.27, an increase of about 300% in the energy dissipated during turn-on process is observed when the SiC Schottky diode is replaced by a GaN HEMT.

    - the increased value of the inductor's EPC, not only will increase of the turn-on switching loss by 97.92% for the case of SiC Schottky diode and by 32.82% for the case of the GaN HEMT, but it will also cause the transistor's current to oscillate after the DUT is fully on. This will lead to an 14% and 56.16% increase in the conduction losses of the DUT, respectively.

    - although the conduction losses are small compared to the switching losses, the high oscillations in the transistor's current might cause further issues. For further increase in the switching frequency, this oscillation might not get completely damped causing problems in transistor's operation.

- Last but not least, during the thesis project, the advanced performance of the high voltage cascode GaN HEMT was observed. Its cascode configuration, where a low voltage Si MOSFET is used to drive the high voltage GaN transistor, makes the device compatible with most of the commercial drivers. The cascode GaN HEMT features a very low reverse recovery charge and a relatively small output capacitance, which is where the energy for dissipation at hard-switching conditions is stored. Thus, the cascode GaN HEMT can be considered superior to the Si MOSFET, but due to considerable package and layout parasitic inductors and capacitors, soft-switching is still required in order to operate at higher frequencies.

6.2 Suggestions for future work

Over the course of this thesis project, a number of possible ideas for further investigation have been considered.

- The analytical loss model developed during this thesis can be further optimized. Implementation of the non-linearity of the parasitic capacitances, instead of using discrete values in every stage of the switching transition, and an extension, so as to be able to model the reverse recovery of the top switch, will increase the accuracy of the model significantly and make the model more complete.

- It would be interesting to design and build a buck converter in order to make comparison of the efficiency between the experimental results and the analytical model. Moreover, the influence of the temperature rise of the device can be examined with the help of a buck converter. Eventually, a full bridge converter can be designed and built utilizing high voltage GaN HEMTs.

- Investigate the topic from the prospective of the magnetic component. How can a more complicated magnetic component be optimally designed in to reduce the impact of its parasitic capacitance on the behavior of the power switches.

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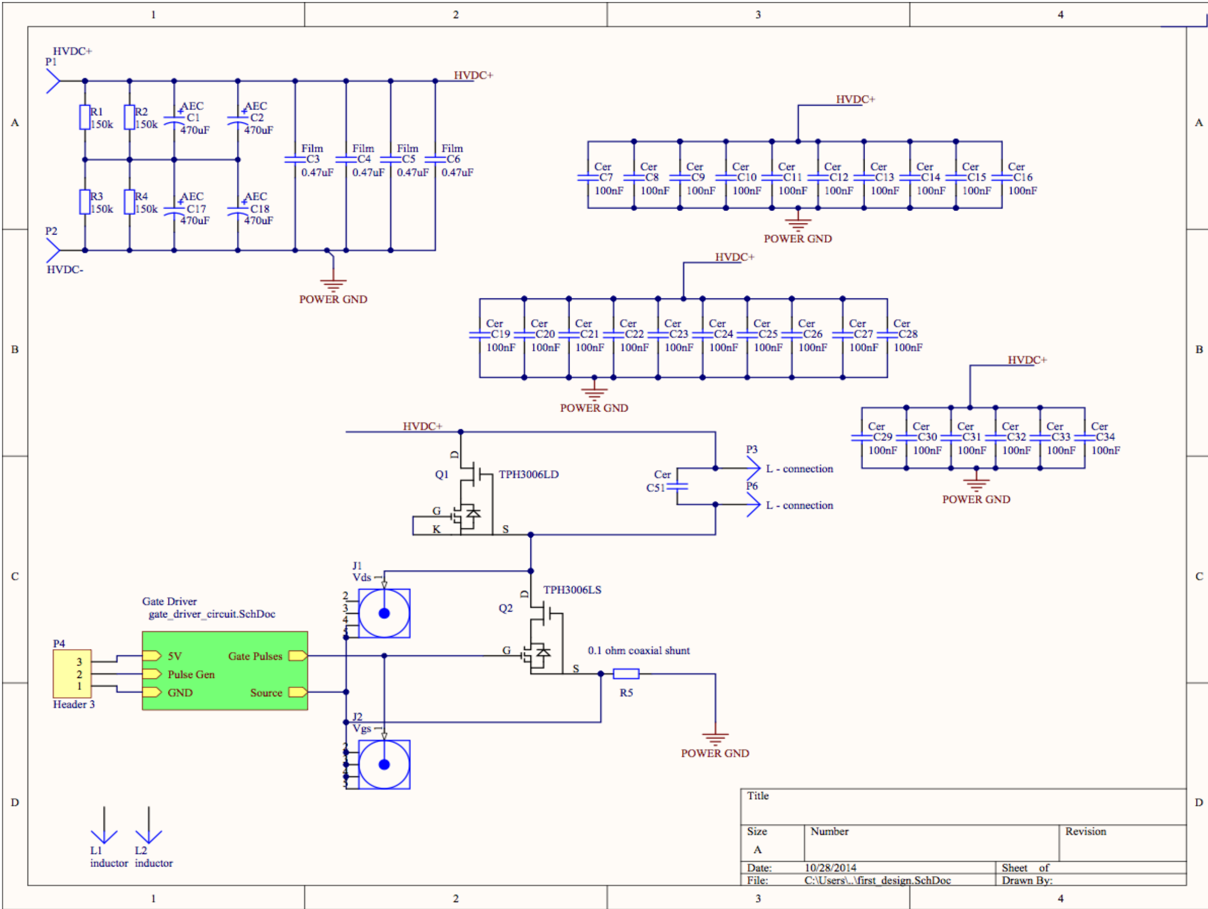
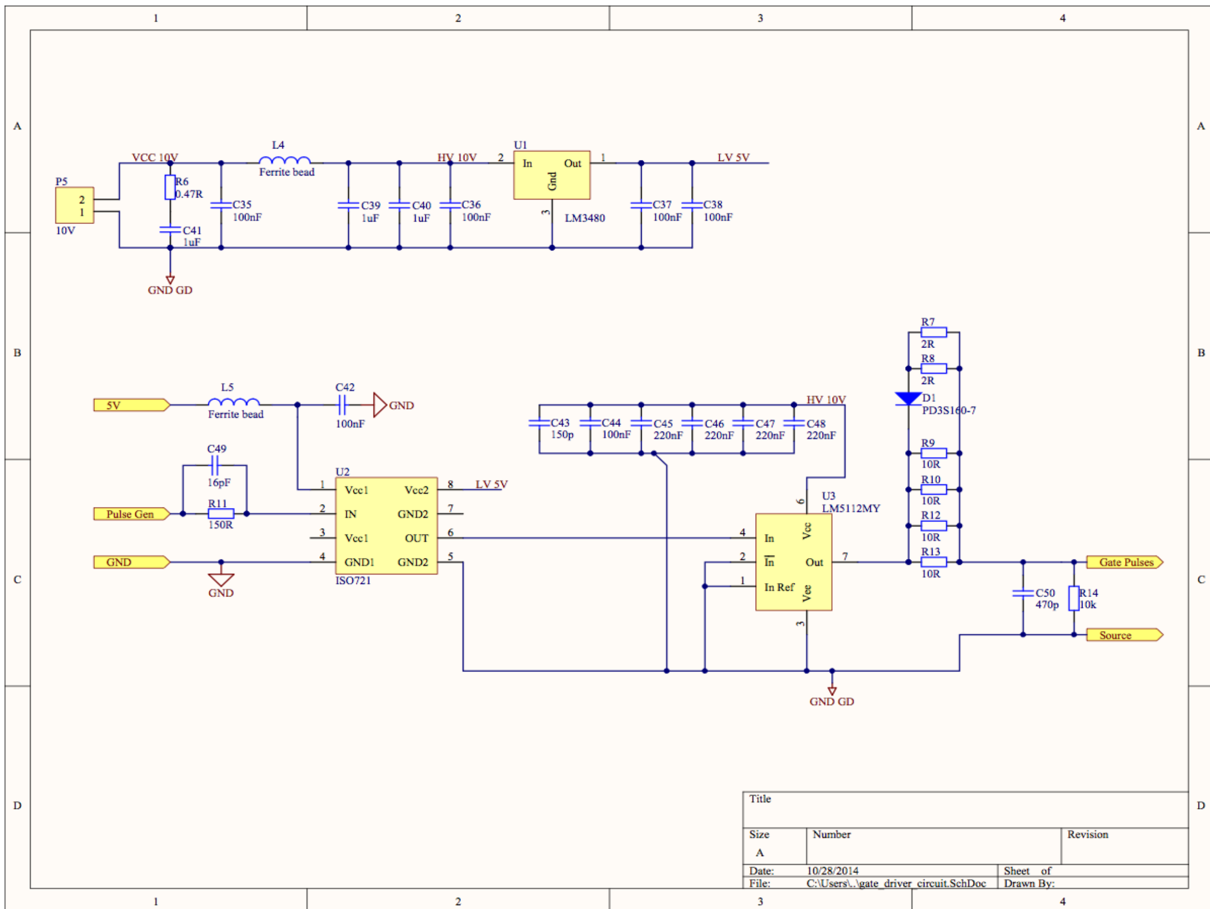
Appendices

Appendix A

DPT schematic and PCB layouts

The detailed schematic of the double-pulse tester and the four layers of the PCB designed by the software Altium Designer are given below:





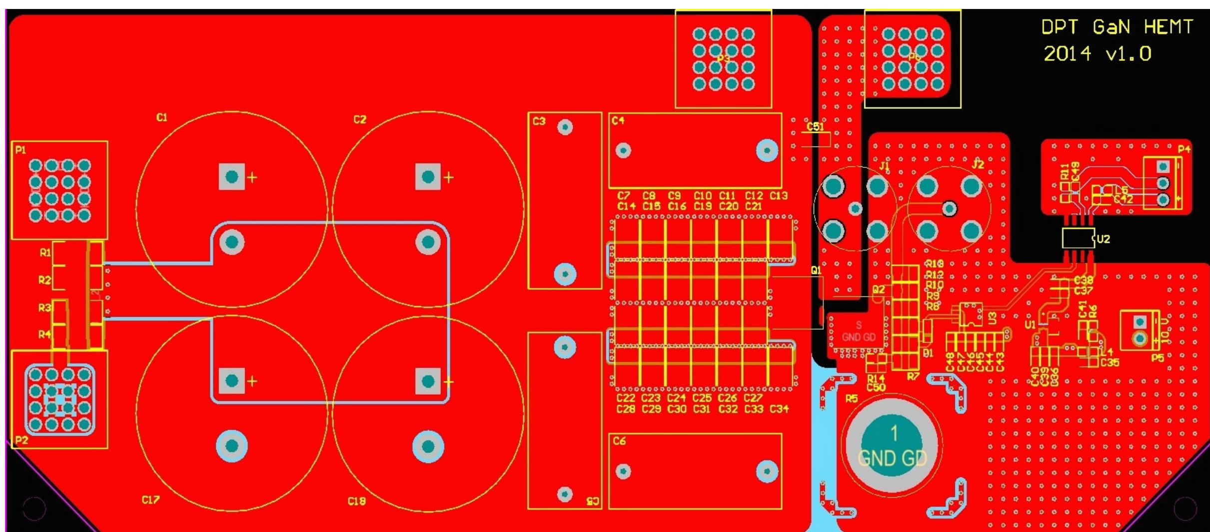


Figure A.1: Top-layer of the PCB

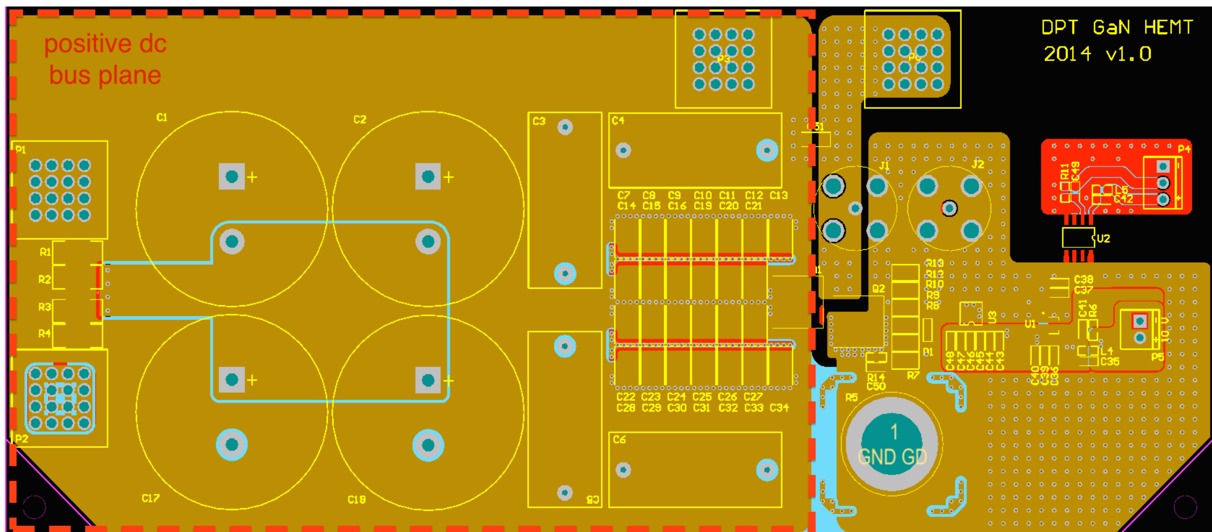


Figure A.2: Middle-layer 1 of the PCB

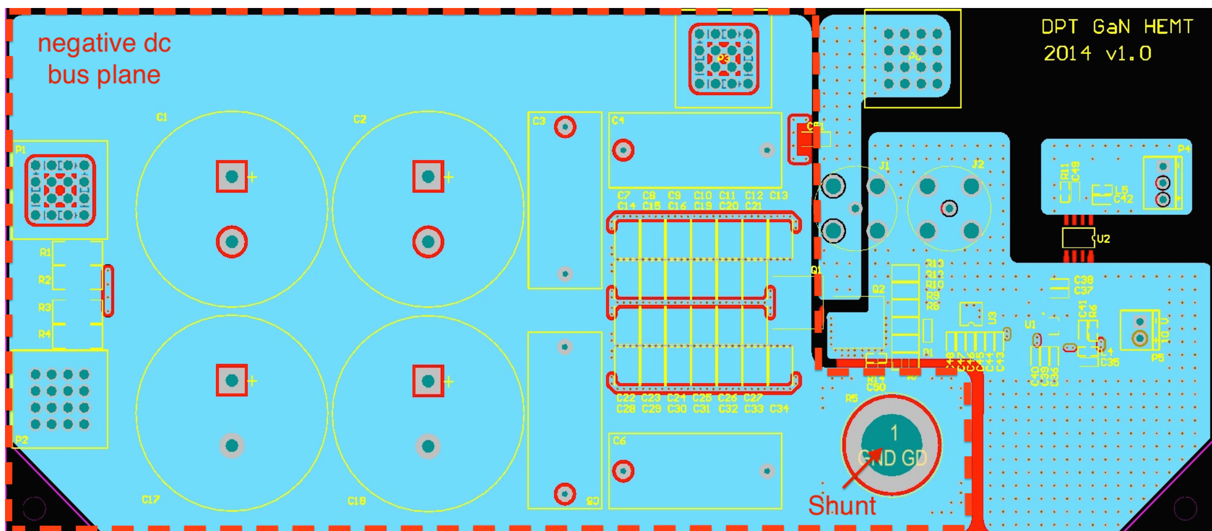


Figure A.3: Middle-layer 2 of the PCB

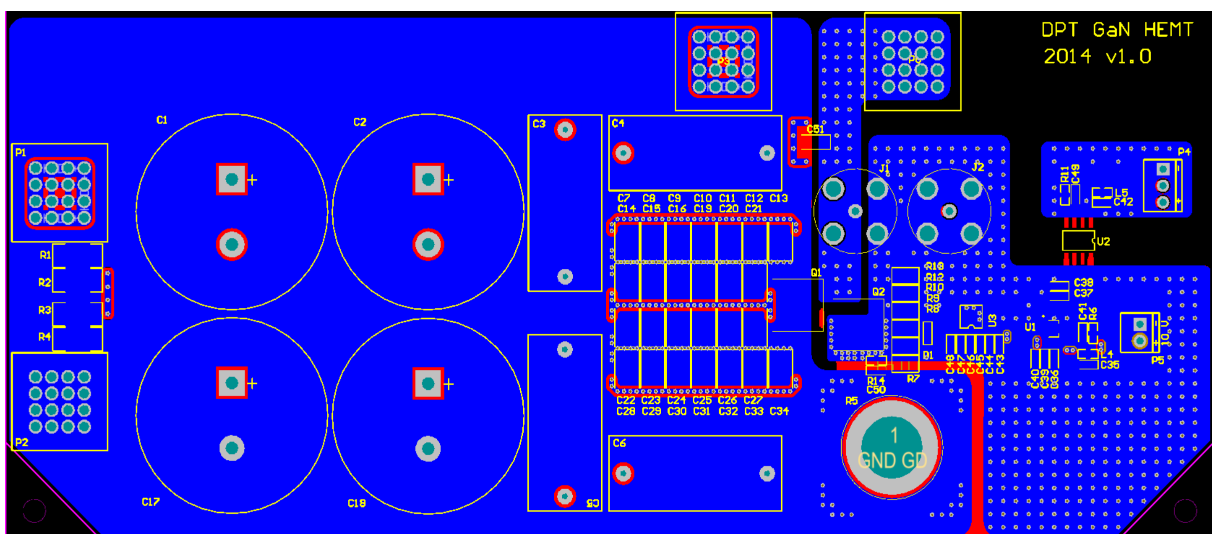


Figure A.4: Bottom-layer of the PCB