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Si and SiGe Epitaxy in Perspective

W. B. de Boer

Delft Institute of Microsystems and Nanoelectronics (DIMES)
Delft University of Technology, Feldmannweg 17, 2628CT Delft, The Netherlands

Fifty years of Si and SiGe epitaxy in the semiconductor industry and twenty-five since the conception of the present generation of industrial epi reactors suffice to justify a review of the evolution and the status of the technology. Although there has been very little change in the reactor design, the epi process progressed significantly. The strengths and weaknesses of the current technology are discussed with an emphasis on possible improvements.

Introduction

CVD silicon epitaxy is an old technique in the semiconductor industry. The technique remained almost unchanged for some fifty years. Originally it was used in the bipolar technology to grow a high-resistivity layer on top of a surface with buried layers to enable the combination of a high breakdown voltage and a low collector resistance of the transistor. The low oxygen and carbon content of the epi layer results in a crystal quality better than the substrate. The process is mature and difficulties like auto doping, pattern wash out and slip are well known and taken for granted.

In spite of the additional costs, the epi process was also introduced in MOS processing. For small feature sizes adding an epi layer as the active layer in which the MOS transistors are made, has several advantages, offsetting the costs of an extra layer. Latch-up suppression and reduction of 'soft' errors in memory cells are the most important benefits. Better crystal quality, resulting in better quality gate oxides, is in MOS transistors more important than in bipolar processing.

Low temperature epi, the latest addition to the technology, deviates considerably from the conventional epi process. Low temperature epi, with deposition temperatures so low that diffusion of dopants does not play a role any more, is done in a different growth regime where many of the old rules do not apply. With diffusion ruled out, doping control is possible with monolayer accuracy. Not only does this allow the growth of very complicated doping profiles, which are very different from the single epi layer in conventional processing, but the low temperature also enables the growth of SiGe mixed crystals. HBT's (Heterojunction Bipolar Transistors) are an important application of this technology. The SiGe base, including the required doping profile, is deposited rather than implanted. In MOS processing a SiGe epi layer is used to modify the mobility of the charge carriers. Elevated source and drain is another MOS application of this new technology.

The low temperature process does not replace conventional (high temperature) epi. It has cut out its own application area, led to new designs and is not fully explored yet. As modern epi reactors are quite capable in dealing with high and low temperature processes, there is not much need for special epi reactors that are dedicated to low temperature processing.

Process Development

CVD in General

Atmospheric pressure CVD used to be the common way to deposit oxide, nitride, polysilicon and monosilicon layers in the early days of the semiconductor industry. Driven by economical and technological requirements there was a continuous search for lower deposition temperatures and more efficient processing. In the mid-seventies of the last century, this resulted in Low Pressure CVD (LPCVD), a huge improvement over processing at atmospheric pressure. The transport of the active chemical species towards the wafer surface improved as the mean free path increased. The result was a much better on-wafer and wafer-to-wafer uniformity. The carrier gas consumption was reduced by two orders of magnitude, thanks to the change from the transport limited growth regime to the kinetically controlled mode. Gas depletion leading to a lower deposition rate at the downstream end of the reactor, was largely overcome by lowering the growth rate. The reactor design changed from cold wall (wafers parallel to the gas flow) to hot wall (wafers closely stacked perpendicular to the gas flow) (fig.1). The long deposition time was compensated by the increased wafer capacity. Apart from the more uniform layers, LPCVD reduced the processing cost per wafer enormously and made atmospheric pressure CVD obsolete.

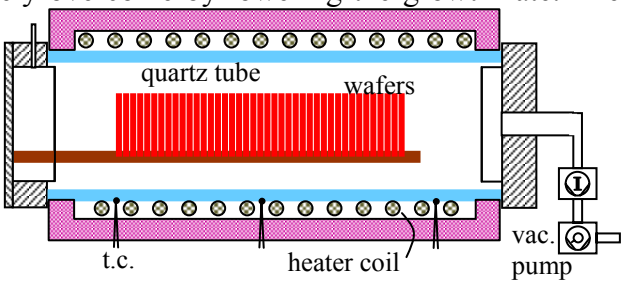

Figure 1. Cross section of an LPCVD system sketching the general set up and the high packing density of the wafers.

There was one thing in which LPCVD was less successful, namely the reduction of the temperature budget. A new technology, PECVD (Plasma Enhanced CVD), took care of this shortly after the introduction of LPCVD. The deposition reactions became plasma driven and were no longer entirely thermally activated. Oxide, nitride and polysilicon layers could be deposited at temperatures around and below 400°C, which was several hundreds of degrees lower than before.

Conventional Epitaxy

The common epi process was and still is characterized by very high processing temperatures (1100-1200°C), which results in interdiffusion of dopants between substrate and epi layer. Consequently the transition region is very wide. This is the interface region between the original substrate and the epi layer in which the doping level changes to a different level. It ranges from several microns to a quarter micron, depending on the process conditions and the doping species. The situation is further complicated by doping atoms that are released from the surface or the backside of the wafer. These tend to get into the gas stream and are redeposited in the epi layer. The overall phenomenon, the widening of the transition region, is called auto doping.

The improvements in the CVD technology had no influence on the way epi was performed. It remained a CVD process in a cold wall reactor with a relatively high growth rate that is transport limited. The LPCVD approach was tried for epi as well, but the low growth rate that is inherent to an LPCVD process, together with the high deposition temperature, caused too much outdiffusion of the dopants. Serious efforts have

been undertaken to develop plasma epi as well. Again to no avail: the incorporation of contaminants into the epi layer probably was the showstopper here.

Although there were no basic changes in the epi process, a few improvements did see the light. In the late seventies the reactor became optionally equipped with a vacuum pump to lower the deposition pressure. The effect was a huge improvement in the auto doping behavior of n-type dopants. Reduced pressure (50-100 Torr) became the standard for bipolar epi processes with As buried layers.

The in situ pre-epi surface cleaning also improved. It used to be a high temperature HCl etch, removing a few tenth of a micron Si from the surface, a remnant from the old bipolar days. The requirements for MOS in terms of cleanliness were much more severe, which has led to cleaner processing and better suppression of metal contamination. The HCl etch process, that had in the old bipolar days been so successful in removing metals from the surface of the wafer, now had an opposite effect. In many cases it caused a metal contamination. The HCl etch was replaced by a hydrogen bake. Exposing the wafer to a high temperature in hydrogen was sufficient to remove the native oxide and to prepare the surface for the epi deposition.

Low Temperature Epi

A revolutionary change came in the eighties. The high deposition temperatures of the conventional epi process had always been reason for concern and numerous researchers have tried to lower the deposition temperature. Plasma epi was only one example. Other examples were the use of different precursors and carrier gases other than hydrogen, like Ar or even He. The problem with lower temperatures was and is the crystallographic quality of the layer. Every attempt to lower the deposition temperature has failed because the defect levels increased unacceptably.

The potential of SiGe HBT's renewed the interest in low temperature epi and this time the approach was more scientific. Meyerson (IBM) believed that oxide on the surface of the wafer was the limiting factor in growing good quality epi layers. His thoughts were based on extrapolated data about the chemical equilibrium between Si-O and Si-H_2O as a function of the temperature and pressure. In order to keep the Si surface from oxidizing he proposed a UHV growth environment. The native oxide was removed ex situ and the wafers were loaded in the UHV system, heated and deposited. Good quality epi layers were obtained at temperatures below 500°C, till then new in CVD.

Around the same time two more sets of publications drew attention. They described growing epi at low temperatures while obviously not fulfilling the criteria that made UHVCVD epi work. At Stanford University a special technique was used, called Limited Reaction Processing (LRP). The wafer was heated very rapidly, in seconds, and the temperature was used to turn on the growth, rather than switching the reactive gases on and off. This way the dangerous temperature area, too low to grow but high enough to quickly oxidize the wafer, is bridged without creating too many oxide clusters. In spite of this somewhat obscure method and in spite of the high oxygen content in some of the early layers, the Si and SiGe epi layers were good enough to be used for HBT's. Stanford demonstrated the first HBT's based on CVD epi.

Even more surprising were the results obtained within IBM by Meyerson's colleague Sedgwick. He reported good quality Si epi at atmospheric pressure and at temperatures around 700°C. The processing was conventional, including the hydrogen bake step to remove any native oxide.

Finally an experiment to grow Si and SiGe epi in a commercially available epi reactor turned out to be a complete success. At deposition temperatures of 600-700°C and

atmospheric pressure, Si and SiGe epi layers of excellent crystallographic quality were deposited. Excellent here meaning device quality, good enough to be used in a high yielding production line. The installation of state-of-the-art gas purifiers (10ppb rating for oxygen and moisture) in the main gas lines, was all that was needed to reach a result that exceeded all expectations. The surface preparation of the wafers was performed as usual, with a high temperature hydrogen bake. Whereas the epi layer quality never was an issue in this process, it took quite some effort to lower the temperature of the bake step to a level compatible with the processing of patterned wafers. A combined HF dip to remove the oxide and Marangoni drying rendered good results and limits the temperature of the bake step to 800°C.

The discrepancy between the extremely low oxygen and moisture partial pressures needed for UHVCVD epi on one hand, and the relaxed requirements for low temperature epi in common production reactors on the other hand, needs further explanation. The Si-O_2 and Si-H_2O equilibrium data had previously been obtained in a hydrogen free ambient. The extrapolation of the data to low temperatures may well be correct and valid for UHVCVD, however, in conventional epi reactors the hydrogen partial pressure is high due to the presence of the carrier gas. The result of this is that the hydrogen coverage of the surface stays intact up to temperatures at which low temperature epi is performed. This protects the surface and allows growth of high quality layers.

Low temperature epi does not replace conventional epi, because the growth rate is too low. It is used for new applications. The capability to control the doping profile to the monolayer level is not used to its full extent and deserves more attention.

Some of the problems of conventional epi do not exist in low temperature epi. Slip generation is no issue at low temperatures. B auto doping has disappeared, proving that it is diffusion driven. B profiles can be grown steeper than SIMS can resolve, possibly atomically sharp. The same is true for Ge. But phosphorus doping is more difficult to control at low temperatures and As doping profiles become uncontrollable. Pattern wash out also gets increasingly worse at lower temperatures. But as the layers are thin this is usually no issue.

Carbon (C) is a contaminant in conventional epi. A high surface concentration of C before the start of the deposition causes SiC crystallites at the interface, generating epi defects. However, C can be introduced and is substitutionally incorporated in the Si lattice when the temperature is low. It suppresses the diffusion of B and is used to maintain the block shaped doping profiles during subsequent high temperature processing steps.

Tool Development

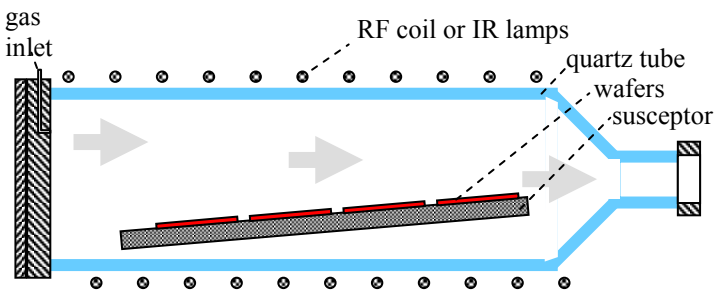

Figure 2. The typical horizontal CVD reactor

The horizontal reactor running at atmospheric pressure, sketched in fig. 2, was the reactor of choice for CVD processes during the early years of the semiconductor industry. The wafers are placed on a graphite

susceptor and the gases are passed through a quartz reactor chamber. RF heating is possible by wrapping a coil around the quartz tube. Lamp heating can be done by high intensity lamps that are aimed at the susceptor and radiate through the quartz. For some applications even a resistive heater inside the susceptor was applied. The walls of the tube are cooled to keep them from collecting deposits, usually by air, sometimes by water in a double-walled tube. In the more sophisticated designs the susceptor is tilted at the exhaust end to increase the gas velocity in order to counteract gas depletion.

While the deposition processes changed from atmospheric CVD to LPCVD and PECVD, the reactors evolved as well. The reactors we use now are very different from those we used in the past and much more efficient, with one exception: epitaxy. The epi technique for conventional epi did not change. We have seen variations on the horizontal reactor such as the barrel reactor. The susceptor is turned vertically and becomes pyramid-shaped, contained in a quartz bell jar. It has a higher wafer capacity and, thanks to the rotating susceptor, better uniformity than the horizontal reactor, but the gas flow still is parallel to the wafer surface (fig. 3). Contrary to a horizontal reactor, which would collapse immediately, the bell jar can be used at reduced pressure. Although originally it was not very clear what good it would do, the barrel reactor was equipped with a vacuum pump and depositions could be done in the 50-100 Torr pressure range. After reduced pressure processing turned out to be beneficial in suppressing n-type auto doping, RP epi became the standard for bipolar epi and the lamp-heated barrel reactor became the workhorse of the industry.

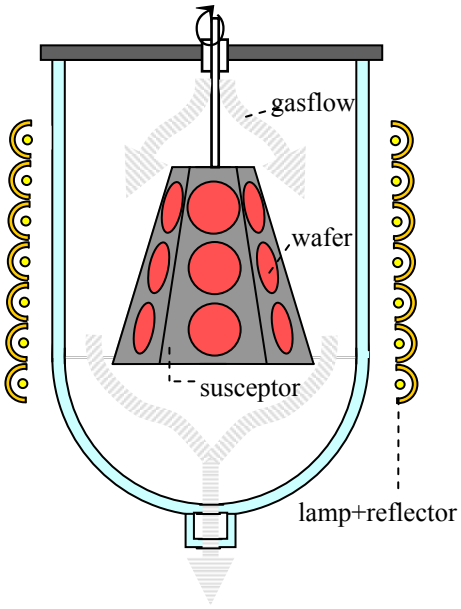

Figure 3. A barrel reactor, the long time workhorse of the epi industry.

Another reactor popular in production was the pancake reactor. It consisted of a round, rotating horizontal susceptor with the RF coil underneath, contained in a bell jar. The gas was injected and recirculated in the bell jar, which was good for the uniformity but not so good for the memory effects. The biggest draw back of this type of reactor is the way the wafers are heated. When the susceptor heats the wafers, the wafers have a tendency to curl up at the edges as the edge of the wafer runs cooler than the center. When they loose contact with the susceptor the edges cool even more, which leads to stress and finally slip. This is a basic problem with any RF heating system and becomes more severe when the wafer diameter increases.

Finally, in the eighties, it looked like the LPCVD approach would be applied to epi as it had been applied to other CVD processes. Applicable only to thin layers at low temperatures and, due to the special requirements for epi, much more complicated than common LPCVD, it opened the gate to new applications. It was called UHVCVD, indicating that the reactor had to be UHV compatible to guarantee a sufficient level of cleanliness.

Simultaneously, also during the eighties, the manufacturers of industrial epi reactors started to develop the next generation of epi equipment. It was foreseen that MOS would

need an epi layer in future generations and everybody saw the reactor sales multiply. The market was for conventional epi, p on p+ several microns thick. Low temperature epi was ignored because there was no market. The results of these developments that were completed by the second half of that decade, were large, high capacity reactors. Not very different from the reactors they were supposed to replace, only bigger. A huge RF heated barrel reactor was produced for only a short while, and a carousel with a mixture of RF and lamp heating did not even make it to production. The only successful reactor, developed during that same time frame, deviated in the sense that it seemingly was a step back. It closely resembled the old lamp heated horizontal reactor sketched in fig. 2, with some important improvements. Its characteristics are single wafer processing with wafer rotation to compensate for gas depletion and to create superior uniformity. Lamp heating was combined with a low thermal mass susceptor to get an acceptable wafer throughput and load-locked wafer entry was added to improve the cleanliness (fig. 4). Better than the batch reactors in terms of layer uniformity and crystal quality, it became competitive in cost per wafer at a wafer diameter of 150mm and was a clear winner for larger diameters. Developed for the MOS market, p on p+ epi, it did not have reduced pressure capability. The characteristics were also appealing to the bipolar world and RP capability was added at a later point in time. Fig. 4 shows a sketch of the heart of the reactor.

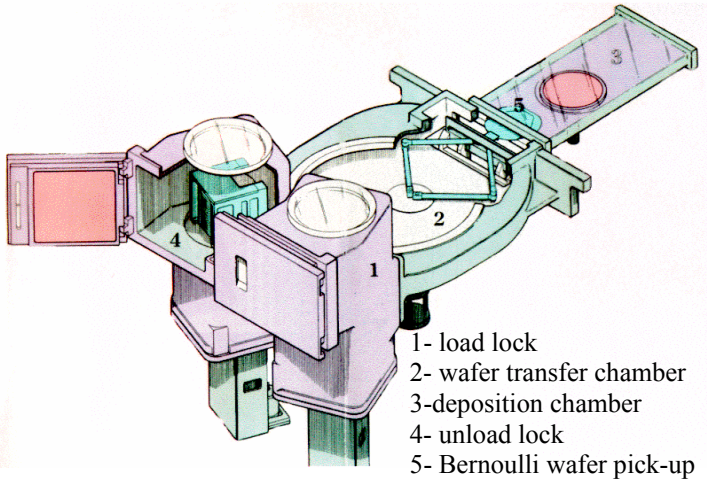

Figure 4. Example of a modern epi reactor: the Epsilon.

Ironically, while the research community was looking for a way to grow Si and SiGe epi at low temperatures at an industrial scale, the reactor that could do it all existed already. The new single wafer reactor had been on the market for several years before it was tried on low temperature epi for the first time. It was straightforward and it was a complete success, even before the RP capability was added. The result is two competing technologies, both fit for low temperature epi: UHVCVD, a batch process in a dedicated reactor, and low temperature epi in a standard production reactor, designed for and ready to grow conventional (thick) epi layers as well. From a production point of view it does not seem very difficult to choose between the technologies, especially not when the flexibility of the single wafer reactor is also taken into account.

An intriguing question remains open. Why was an experiment suddenly successful that must have been performed by everybody in the epi business over the last fifty years, an experiment that failed time after time and again? The experiment we are talking about is the growth of an epi layer at a lower temperature than usual in commercially available reactors. A part of the answer is the improvement in the quality of the process gases and the availability of gas purifiers with ratings in the 10ppb range. However, this cannot be the full explanation. Pd purifiers with similar or even better ratings have been around for

a long time. The reactor design probably has a lot to do with it, in particular the presence of a load lock. For the first time in the epi reactor history the inside of the reactor is not exposed to ambient air during the load and unload procedures and does not come into contact with high levels of oxygen and moisture for weeks in a row. This causes a very low level of adsorbed moisture on the inside walls and flanges of the reactor, resulting in low levels of desorbed moisture during the process. It is more than likely that this improvement, compared to earlier reactors, is responsible for the enhanced performance at low temperatures.

Process Improvements

Conventional Epitaxy

In conventional epi only limited progress can be made. The knowledge that device quality epi can be grown at lower temperatures than used in the past, can be applied to further suppress slip. Slip is a crystallographic defect caused by uneven heating of the wafer. Temperature differences between the center and the edge of the wafer cause stress and when the yield limit is exceeded, dislocations occur. The dislocations run through the entire wafer and leave slip lines behind. As the yield stress increases with decreasing temperatures, a lower deposition temperature is less likely to generate slip.

Also, B diffusion will benefit from lower deposition and baking temperatures. However, slip is hardly a problem any more in modern reactors and B diffusion is usually not a big concern. In bipolar technology As auto doping still is a concern, as is pattern wash out. Pattern wash out is the change of the shape of geometrical features on the surface of the wafer due to the epi process. More specifically, this refers to the lithographic process when the wafer stepper fails to recognize the alignment markers. This occurs because the epi growth rate is different on surfaces with a different crystallographic orientation. On the sidewalls of the alignment markers different crystallographic orientations are exposed, growing at different rates and building facets. These facets obliterate the geometry. When epi is grown on a (111) surface, the same growth rate differences lead to pattern shift. The impact of both phenomena, As auto doping and pattern wash out, is less at higher temperatures, which makes it unlikely that a shift towards lower processing temperatures will happen.

It is not to be expected that in a mature and established technology like conventional epi process improvements can be found easily. Nevertheless, the processing is also based on old habits and low temperature epi offers new insights. The most important one is that the quality of the epi layer does not need to suffer from lower deposition and bake temperatures. The almost automatic reaction to increase the temperature when the surface quality deteriorates, is a wrong one and it hides the cause of the problem.

Low Temperature Epitaxy

Low temperature epi has its own set of problems. The low growth rates are not a problem, at least not when the layers that have to be deposited are thin. The extreme temperature sensitivity of the growth rate and the dopant incorporation also is not a problem. This sensitivity is a logical consequence of working in a kinetically controlled growth regime. Fortunately, the wafer temperature in single wafer reactors can be controlled well enough and locally enough to overcome the increased sensitivity. The problems lie in areas where they are least expected. A few important difficulties and, when known, remedies are indicated below.

n-Type Doping. Ge, B and C profiles can be controlled to a monolayer level or better, allowing the growth of box-shaped profiles with unparalleled control of the transition regions.

This is no longer the case when As or P doped layers are deposited. An attempt to grow a P or As doped layer with an undoped Si capping layer at reduced pressure is illustrated in fig. 5. When the As flow is turned on, the doping level in the growing layer increases slowly. When the doping gas flow is turned off, the doping level in the epi layer decreases slowly. It resembles in no way the B and Ge profiles obtained at low temperature. Apparently, the wafer is doped from an adsorbed surface layer. At the onset of the growth of the doped layer, it takes a while before the equilibrium is reached. When the dope supply is turned off, the wafer continues to be doped until the adsorbed layer is consumed. The described behavior makes it impossible to control the growth of As-doped layers.

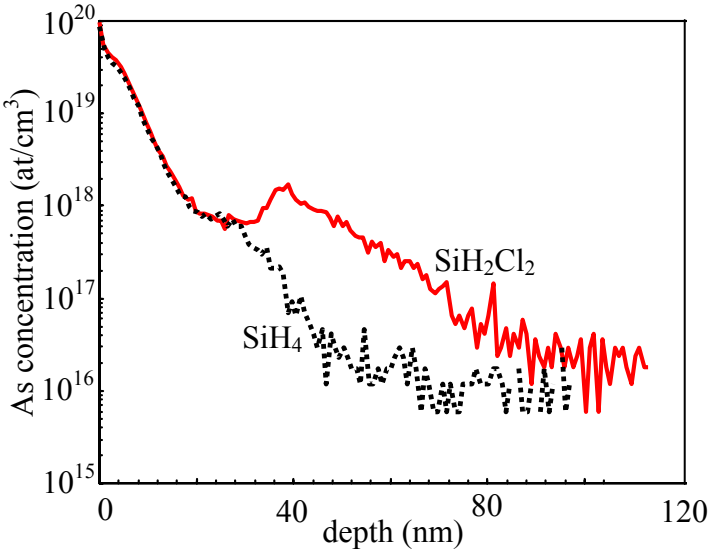

Figure 5. An attempt to grow block shaped As profiles. The SIMS plot shows that neither the beginning nor the end of the doped section is well defined. A different Si precursor does not make much difference. As segregates at the surface.

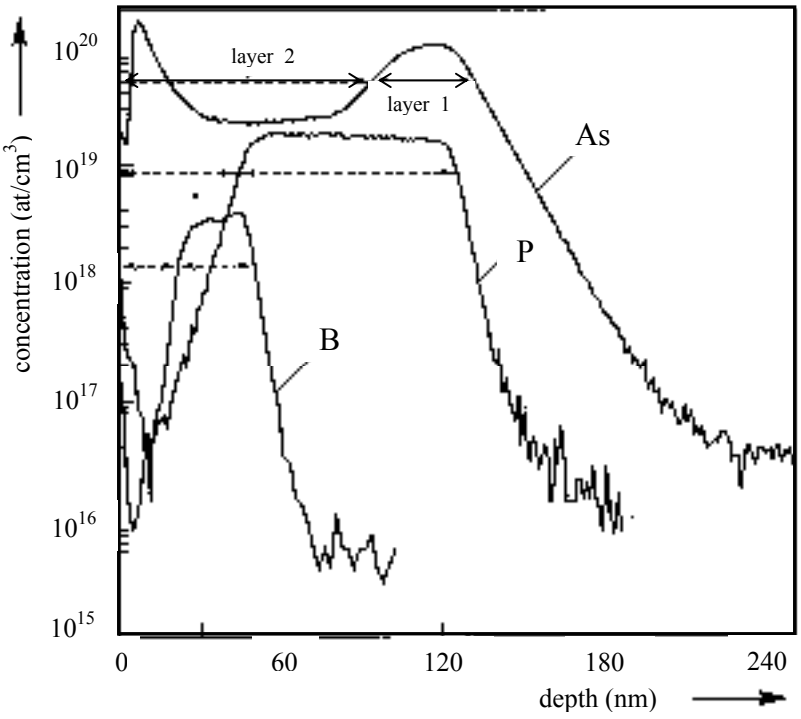

Figure 6. When the growth is done at atmospheric pressure, the P doping profile can be controlled, albeit that the transition region is not as good as for B. The As profile remains out of control, the profile is similar to the profile obtained at reduced pressure, in contrast to P.

Nevertheless, P doped layers can be controlled. The control is not as good as for B and Ge doped layers, but sufficient, provided the growth is done at atmospheric pressure. Fig. 6 shows the SIMS profiles of a B-, a P- and an As-doped layer, each capped with an unintentionally doped layer. The layers have been deposited at atmospheric pressure, 625°C and with SiH_2Cl_2 as the Si precursor. The B profile is abrupt, the leading and the trailing edge are SIMS determined. The leading P edge (leading from a SIMS perspective, not from a grower's perspective) is not as steep, clearly no longer SIMS determined, but acceptable. The As profile remains uncontrollable and does not show much improvement compared to the growth at reduced pressure. This shows the importance of the H_2 partial pressure and the competition between P and H for adsorption sites. For some applications switching to atmospheric pressure and using PH_3 as the doping gas may solve n-type dope control problems. However, it is not the panacea one hoped it to be. Growth on patterned wafers at atmospheric pressure increases the loading effects. The growth becomes dependent on the local environment and factors like the pattern density come into play. Even at atmospheric pressure and P as n-type dopant, there are still signs of surface segregation. For instance, when a B-doped capping layer is deposited on top of a P-doped layer, both dopants P and B show a peak at the interface, before returning to the expected levels. There is no interference if it is done the other way around: a P-doped capping layer on top of a B-doped layer. At reduced pressure these effects are much more severe.

For an application like an in situ As-doped (mono)emitter in HBT's, the leading edge is not important. There is a pile up of As at the surface, but it will be removed in consecutive wet cleaning cycles. The slope of the trailing edge is important, as it influences the emitter resistance. A trick to get a steeper slope is to expose the surface to the doping gas AsH_3 before the Si source (usually SiH_4 or SiH_2Cl_2) is turned on. A more elegant way to achieve a steep leading edge is to co-dope the emitter layer with Ge during the first few seconds of the deposition. A fraction of a monolayer of Ge at the interface has a strong effect on the trailing slope of the As profile, as can be seen in figures 7 and 8. The slope increases with an increasing Ge content of the spike. In fig. 9 the steepness of

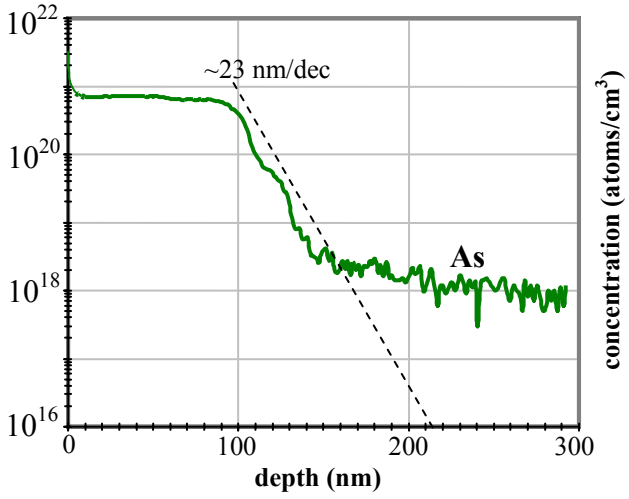

Figure 7. A SIMS plot of an in situ doped As emitter illustrates the slow rise of the As signal after the doping flow has been turned on, typical for n-type doping.

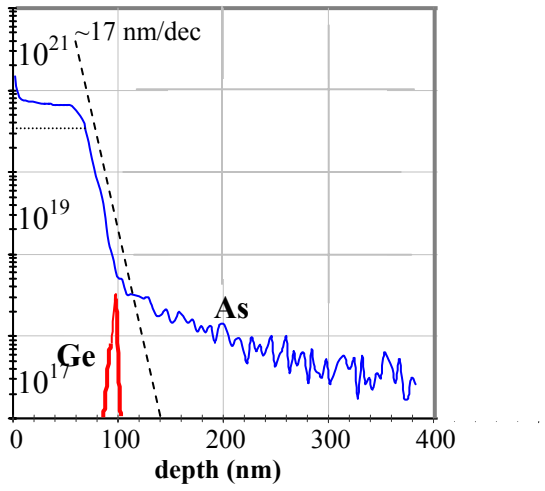

Figure 8. A small amount of Ge at the interface improves the trailing slope of the As profile considerably.

the slope is already beyond the SIMS resolution and the measured value of 4 nm/decade is SIMS determined. The total amount of Ge at the interface in this case is between 10% and 20% of a monolayer.

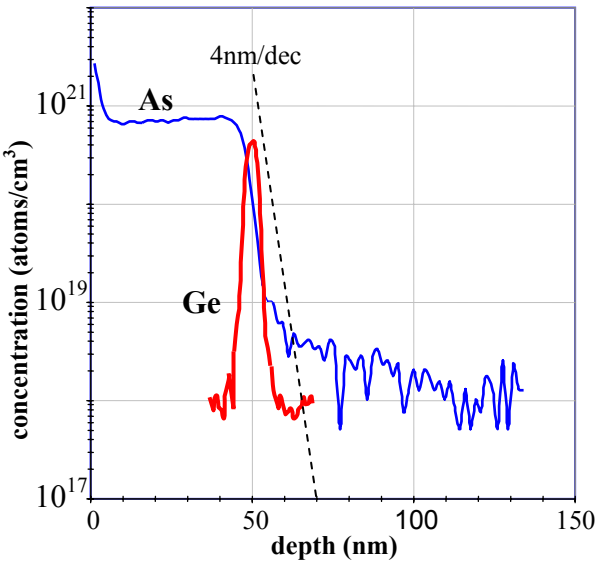

Figure 9. The steepness of the trailing edge of the As profile increases with an increasing amount of Ge at the interface. Here the slope is already SIMS determined.

Temperature Inconsistencies. In spite of the fact that the temperature is measured with a thermocouple, the wafer temperature depends on its emissivity. The cause of this is that the susceptor temperature is measured, not the wafer temperature. As there is a considerable thermal resistance, the temperature difference between wafer and susceptor depends on the heat flux and can easily be 50°C or more (see below). Especially at reduced pressure, when the efficiency of the heat conducting hydrogen film between wafer and susceptor deteriorates, large differences are possible. The difference itself is not the problem. The reactor is stable and reproduces very well. It becomes a problem when wafers with different patterns (and different emissivities!) are run with the same recipe in order to get the same layer. A large difference between these wafers can occur in terms of layer thickness and dope incorporation.

Even worse is that on a patterned wafer polysilicon will deposit on the field oxide (or nitride) when a blanket deposition is done. The polysilicon with the underlying oxide or nitride layer forms an interference filter, changing the wafer emissivity and subsequently the temperature during the growth of the layer. The effects are a varying growth rate and varying dope concentrations.

Although this is more a reactor deficiency than a process problem, it is best to deal with it in the process. It does not look like this problem will be solved in the design of the reactor any time soon. In practice it is not often perceived as a problem. The stability and reproducibility of the reactor guarantee the same output if the input is the same. One will notice that the growth rate does not increase linearly with the deposit time or that the doping level is not constant. These are small inconveniences, solved with an additional calibration run. In an R&D kind of operation, with different patterns and different layer thicknesses, the situation is more serious and the costs to analyze test wafers (SIMS !) can rise exceptionally. Until something is done to measure and control the wafer temperature rather than the susceptor temperature, the situation will not improve.

Another side to this problem is that large areas on the wafer (> ~1cm2) that have an average emissivity different from the surrounding area, will have a different temperature. This time the reactor cannot be blamed and the solution has to come from mixing the patterns as much as possible, making sure the patterns stretch out all the way to the wafer edge (no ragged edges), etc.

Reactor Improvements

Several improvements are possible, separated in categories such as: indispensable for the process, driving the costs per wafer down or demonstrating technological superiority. Below are three examples, one in each category, referring to the single wafer reactor.

Wafer Temperature Measurement

The measurement of the wafer temperature was never very accurate in epi reactors. It is either done by a thermocouple inside the susceptor or by pyrometry. As the emissivity of the wafers is not constant, especially not when the wafers are patterned, a pyrometer usually is aimed at the susceptor, also measuring the susceptor temperature. In conventional epi measuring and controlling the susceptor temperature is sufficiently accurate. The growth rate and dope incorporation are only moderately temperature dependent in a diffusion limited CVD process. An additional beneficial factor is, that at the high temperatures used in conventional epi, the heat transfer is primarily by radiation. The conduction through a gas film between wafer and susceptor is less important. The result is that the wafer and the susceptor temperature are not very far apart. The wafer temperature is constant when the susceptor temperature is kept constant.

As explained in the preceding section, this is all different in RP low temperature epi. It is not sufficient to measure the susceptor temperature to control the wafer temperature. Temperature differences of 30-50°C between wafer and susceptor are not uncommon and the wafer temperature of patterned wafers can cycle during the growth from 0 to more than 50°C below the susceptor temperature.

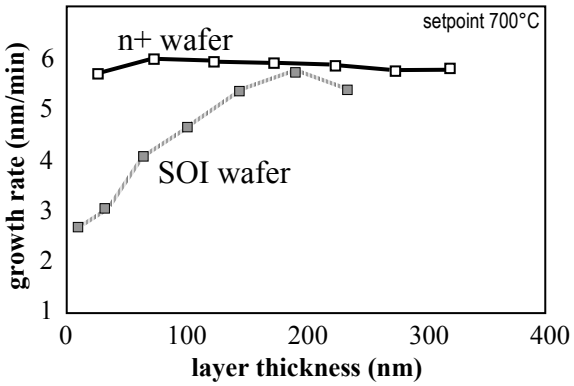

Figure 10. The comparison of the growth rate vs. layer thickness for a standard wafer and an SOI wafer, clearly shows that the SOI wafer is going through large growth rate variations.

This is easily demonstrated by an experiment: B spikes are grown into an epi layer at fixed time intervals in order to determine the growth rate between two B spikes. The process conditions are those commonly used for low temperature epi, 20 Torr pressure and 700°C. Identical runs are made on two wafers, one standard, unpatterned (100) wafer and the other an SOI wafer. The top layer of the SOI wafer should have the same crystallographic orientation: (100). As the SOI wafer is optically active, it changes its emissivity during the growth of the layer. In fig. 10 the growth rates of the wafers are compared. Whereas the growth rate on the standard wafer is constant, the SOI wafer goes through large growth rate variations. When the epi layer is thick enough to absorb the radiation like the standard wafer does, its growth rate returns to normal.

We are saved here by the extremely good reproducibility of the modern reactor, but the situation is far from ideal. After every change, such as a different pattern or a different layer thickness of one in the layers in the stack, the growth parameters have to be checked and adjusted. As SIMS is applied to determine the layer thickness and the dope concentration, the analysis costs easily get out of hand.

Measuring and controlling the true wafer temperature is not a new problem in this industry. In RTP (Rapid thermal Processing), the temperature measurement has been problematic for as long as this discipline existed and numerous methods have been suggested to alleviate the difficulties, so far with only limited success. RTP, by definition, does not use a susceptor, which complicates the matters. Although in epi the susceptor is a part of the problem, it also could be part of the solution. Our aim is not so much to know the real temperature, but to keep the wafer temperature constant during the process and from wafer to wafer. Thermocouples in the susceptor are insufficient to reach this goal. Pyrometry does not work, because the emissivity of the wafers varies from wafer to wafer. However, with a combination of thermocouple measurement and pyrometry we may be able to reach our goal.

By adding pyrometry aimed at the backside of the wafer, we should be able to detect and correct any deviation from the starting condition. The wafer backside does not change the emissivity during the run. The starting condition is the deposition temperature at atmospheric pressure. This provides a calibration for the pyrometer, because under these conditions the wafer temperature is close to the susceptor temperature as read by the thermocouple. During the remainder of the process, evacuation and deposition, the reading of the pyrometer needs to be kept constant. Additionally pyrometer readings preferably should be taken at the center and the edge of the wafer to suppress any center to edge variation.

The difficulty of the method suggested here is of course the optical temperature measurement of the backside of the wafer. The view is obstructed by the susceptor. A solution with optical fibers, possibly embedded in the susceptor, may not be an easy one but seems doable and would significantly improve the low temperature performance of the present generation epi reactors

Throughput

In single wafer reactors, throughput always is an area of concern. Any improvement in cycle time reduces the cost per wafer proportionally. An easy option for reducing the cycle time is reduction of the heating and cooling time. Especially in conventional epi the heating and cooling can consume 50% of the wafer cycle time. With respect to this it is amazing that so little effort had been undertaken to improve the heating and cooling times. Without a susceptor the wafer heats up in seconds rather than minutes. The step towards susceptorless epi may be big, but the rewards will be such that development efforts into this direction can easily be justified. The difficulty here again is the measurement of the wafer temperature. It has to be a multi point measurement to guarantee uniform and slip free heating and cooling of the wafer.

Power Consumption

The installed power to heat a wafer in a modern epi reactor is well over 100kW. The full power is not used at steady state but during the heating phase of the cycle. Depending on the temperature, 50% or even more power is used at steady state. This exorbitant energy consumption is caused by the design. In a cold wall reactor a large fraction of the energy put into the system disappears into the cooling air and into the cooling water. At a temperature of 1150°C the radiation loss of a 150mm wafer is typically an order of magnitude less than the energy put into the heating lamps.

After having built epi reactors the same way for almost fifty years, it is time for a change. A design that saves energy would be more than appropriate. Is there a way to

build a cold wall epi reactor with similar or better specifications than the industry standard of today that consumes only a fraction of the energy? There may be, but it will be challenging technology, to say the least.

The first thing to get rid of is the quartz reactor wall. Quartz is an ideal material for the reactor chamber, it is clean, compatible with Si and transparent for the radiation from the heating lamps. However, it absorbs a large fraction of the long wavelength radiation emitted by the wafer. In order to conserve energy the emitted radiation has to be reflected by the walls of the reactor, as in a radiation cavity. The cavity will be far from ideal, but the energy that needs to be supplied to heat a wafer and to maintain the temperature will be considerably less than in the present reactors. The crucial factor here is the design of the reactor walls. A surface reflecting long wavelength infrared, compatible with epi technology and cleanable, will not be easy to find. A metal chamber with an impervious optically active coating comes to mind. The wall is not the only technological challenge. How to supply energy to the wafer, how to keep deposits away from the reactor walls and how to measure the temperature are all areas waiting for innovative design.

Concluding Remarks

The epi industry has too long relied on a reactor design that is almost half a century old. The process improved over the years, but the reactor design did not keep pace. These days the R&D capacity in the industry is no longer used to prepare the next increase in wafer diameter, the resources are available to improve the reactors. The incentive, if nothing else, is to get an edge on the competition, important in a maturing industry. However, the toolmakers do not demonstrate a real urge to improve the reactor technology. Existing problems are ignored rather than attacked. The customers are part of the problem: in many cases they do not realize that the difficulties they have are inherent to the design of the reactor. One would think that it makes a lot of sense to get rid of some reactor flaws, improve the design and outsmart the competition technologically. Instead the efforts and money are spent on legal fights and hostile takeovers. This may be logical from a business point of view, but it is not good for the industry.

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