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2-output Spin Wave Programmable Logic Gate

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This paper presents a 2-output Spin-Wave Programmable Logic Gate structure able to simultaneously evaluate any pair of AND, NAND, OR, NOR, XOR, and XNOR Boolean functions. Our proposal provides the means for fanout achievement within the Spin Wave computation domain and energy and area savings as two different functions can be simultaneously evaluated on the same input data. We validate our proposal by means of Object Oriented Micromagnetic Framework (OOMMF) simulations and demonstrate that by phase and magnetization threshold output sensing {AND, OR, NAND, NOR} and {XOR and XNOR} functionalities can be achieved, respectively. To get inside into the potential practical implications of our approach we use the proposed gate to implement a 3-input Majority gate, which we evaluate and compare with state of the art equivalent implementations in terms of area, delay, and energy consumptions. Our estimations indicate that the proposed gate provides 33% and 16% energy and area reduction, respectively, when compared with spin-wave counterpart and 42% energy reduction while consuming 12x less area when compared to a 15 nm CMOS implementation.

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I. INTRODUCTION

During the past decades, the human society experienced an information technology revolution that resulted in a huge increase of easy available raw data, which processing requires efficient computing platforms ranging from high-performance clusters to simple Internet of Things (IoT) nodes[1,2]. However, CMOS downscaling that provided the means to meet the data processing energy and performance requirements[3] became more and more difficult due to various technological hurdles indicating that Moore's Law will soon come to its end mainly because of: (i) leakage wall[4,5], (ii) reliability wall[6], and (iii) cost wall[4,6]. Therefore, to keep the pace with "exploding" market needs, novel alternative technologies are under investigation[3]. Among them Spin-Wave (SW) stands apart as one of the most promising avenue[3,7,8] because it has: (i) ultra low power consumption potential - SW based calculations are performed by means of SW interactions and do not require charge movements, (ii) acceptable delay, and (iii) high scalability - SW wavelengths can reach into the nm-range. Therefore, novel Spin Wave technology circuit design methodologies are of great interest.

Up to date different SW logic gates have been introduced, e.g.,[9–17]. The current controlled Mach-Zehnder interferometer was employed to construct a NOT gate, which is considered to be the first experimental work to implement logic gates using spin-waves[9]. Afterwards, XNOR, NAND and NOR gates were implemented using Mach-Zehnder as well[10,11,18]. Furthermore, a magnon transistor has been utilized to build an XOR gate by embedding two transistors in the Mach-Zehnder interferometer arms[12]. Moreover, research was conducted to implement voltage controlled XNOR and NAND using two parallel re-configurable nano-channel magnonic devices[13]. Information encoding in SW phase rather than in SW amplitude also proposed[14] and buffer, inverter, AND, NAND, OR, NOR and XOR gate designs introduced[14]. Furthermore, a 3-input majority gate design, which can perform 2-input AND and OR by assigning one of its inputs to 0 or to 1, respectively, was presented[14] . In addition, OR and NOR were implemented using the cross structure[15]. Furthermore, two experimental prototypes for majority gates were presented[16] and[17]. However, due to SW interaction way of operation, all of the reported logic gate designs cannot provide fan-out support, which is an essential gate feature for the effective implementation of larger circuits. Hence, if a SW gate output should serve as input for multiple following gates in the circuit it has to be replicated, leading not only to area overhead, but also to higher energy consumption.

This paper solves the above limitation and proposes a 2-output Programmable Logic Gate (PLG). Depending on the design of the structure, the 2 outputs can produce the same or different functions simultaneously. The main contributions of this work are:

- Design of 2-input 2-output PLG: Two logic functions (including AND, NAND, OR, NOR, XOR and XNOR) can be implemented using a single 2-output structure. For example, assuming that the gate inputs are x and y it can simultaneously provide both AND(x, y) and XOR(x, y).

- Validation of gate functionality: Object Oriented Micromagnetic Framework (OOMMF) software is used to successfully validate the proposed gate behaviour for all considered Boolean functions and input cases.

- Demonstration of the superiority: The evaluations indicate that the proposed 2-output gate saves 33% of energy and 16% of area without incurring any delay penalty when compared with functionally equivalent designs based on state-of-the-art spin-wave gates. Moreover, the proposed design outperforms 15 nm CMOS in terms of energy and area by providing an energy reduction of 42% while consuming 12x less area.

The rest of the paper is organized as follows. Section II provides basic spin-wave technology background. Section III describes the proposed Programmable Logic Gate design. Section IV introduces the OOMMF simulation setup and results while in Section V we evaluate the proposed design, compare it with the state of the art, and discuss issues like scalability, variability, and thermal noise effects. Section VI concludes the paper.

II. SW TECHNOLOGY BACKGROUND

A Spin Wave (SW) is the collective spin excitation in a magnetic system[19] and this precessional motion of the magnetization is described by the Landau-Lifshitz-Gilbert equation[2021] as:

$$\frac{d\vec{m}}{dt} = -|\gamma|\mu_0 \left(\vec{m} \times \vec{H}_{eff}\right) + \frac{\alpha}{M_s}\left(\vec{m} \times \frac{d\vec{m}}{dt}\right), \tag{1}$$

FIG. 1. Generic Spin Wave Device

where α is the damping factor, γ the gyromagnetic ratio, M_s the saturation magnetization, $\vec{m}$ the magnetization and H_{eff} the effective magnetic field given by

$$H_{eff} = H_{ext} + H_{ex} + H_{demag} + H_{ani} + H_{ani}^{sh}, \tag{2}$$

where H_{ext} is the external field, H_{ex} the exchange field, H_{demag} the demagnetizing field, H_{ani} the magneto-crystalline field and H_{ani}^{sh} the shape field.

The main interactions which give rise to spin waves are the exchange and dipolar interaction for respectively short and long wavelength spin waves[19]. Depending on SW propagation direction relative to the orientation of the magnetization and effective magnetic field, different SW types can be excited and each has its own characterstics. Three main spin-wave regimes exist depending on the wavelength: exchange spin-waves, exchange-dipole spin-waves, and dipole (magnetostatic) spin-waves. There is a single dispersion relation, which represents the SW frequency as a function of the wavevector k[22]. While all three regimes are captured by a single relation this is not a linear function as the curvature can change depending on the dipolar/exchange contribution. Additionally, depending on the relative orientation between the wave propagation direction and the magnetization different spin wave types exist, namely Magnetostatic Surface spin-wave (MSSW), Backward Volume Magnetostatic spin-wave (BVMSW), and Forward Volume Magnetostatic spin-wave (FVMSW) each

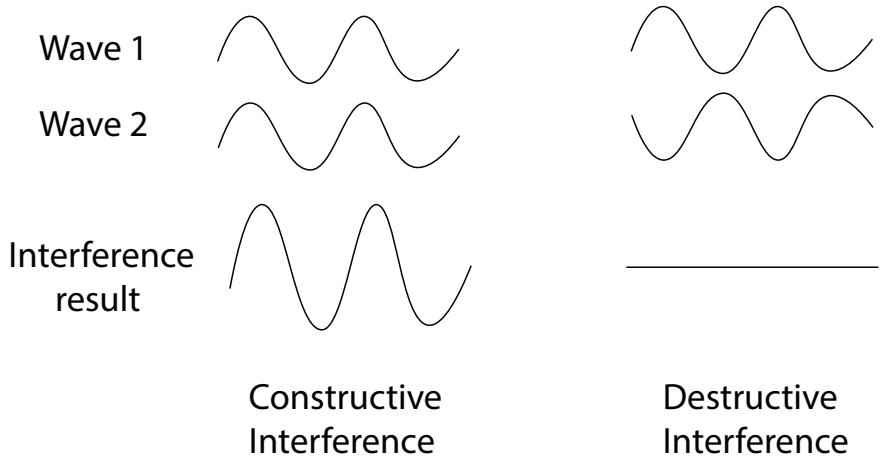

FIG. 2. SW Constructive and Destructive Interference

one characterised with its own dispersion relation[23]. We note that FVMSW in-plane propagation is isotropic and as a result the same wave number is excited in all directions, which is not the case for other types. In view of this FVMSWs are the most promising from the circuit design prospective[23] and are utilized in this paper.

As depicted in Figure 1, a spin wave device consists of 4 regions: excitation region I (where SWs are excited), waveguide B (where SW propagate), functional region FR (where SWs can be manipulated), and detection stage O (where tha output SW is detected). During the excitation stage, information can be encoded into the amplitude (A) and phase (ϕ) of spin-waves at different frequencies (f)[25,26]. This makes it possible to use spin-waves as data carriers and their interaction as data processing mechanism to enable parallelism in SW circuits. If multiple waves co-exist in the same waveguide, their interactions is based on the interference and superposition principles. When SWs interfere in the waveguide, their interaction can be constructive or destructive depending on their phase difference. Figure 2 illustrates these two cases. Two spin waves having the same wavelength (λ) constructively interference if they have the same phase ($\Delta\phi = 0$) and destructively if they are out of phase ($\Delta\phi = \pi$). If more than two waves coexist in the waveguide, then their interference results is based on a majority decision. By assuming that input SWs can have phases $\phi = 0$ or $\phi = \pi$ their interference results in a SW with $\phi = 0$ if the majority of inputs have $\phi = 0$, and in a SW with $\phi = \pi$ otherwise. This implies that SW interaction provides natural support for, e.g., single gate 3-input majority function implementation, which in a CMOS technology based Boolean logic based implementation requires 18 transistors[14,27].

III. 2-INPUT 2-OUTPUT PROGRAMMABLE LOGIC GATE

This section describes the proposed gate structure and discusses different logic gate embodiments.

A. Proposed Programmable Logic Gate Structure

Figure 3 graphically depicts the topology of the proposed programmable logic gate that has a ladder shape structure. It has 2 inputs (I_1 and I_2) placed on the stair's steps and two control signals C_1 and C_2 located at the ladder top that control the way the input

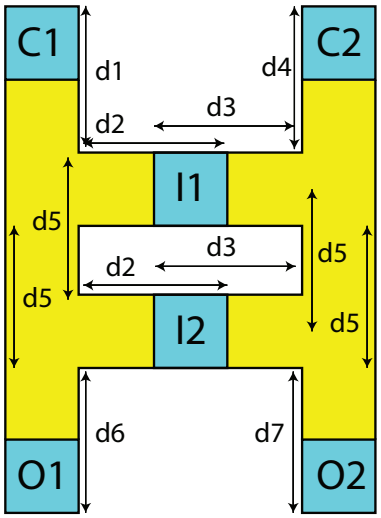

FIG. 3. 2-input 2-output SW Programable Logic Gate

spin-waves are interacting. Further, the outputs O_1 and O_2 are obtained at the end of both columns. Both input SWs generation and output SWs detection are performed by means of magnetoelectric (ME) cells or other transducers[19] able to transform voltage (current) encoded logic values into SWs and the other way around. To obtain the correct expected output results the distances between SW interference points must be accurately determined as multiples of the SW wavelength λ. In particular, if $d_i = n\lambda$ (where $i \in \{1, 2, 3, 4, 5\}$, and $n = 0, 1, 2, \ldots$), the SWs are constructively interfering if they have the same phase ($\Delta\phi = 0$) and destructively if they are out of phase ($\Delta\phi = \pi$). On the other hand, when $d_i = (n + \frac{1}{2})\lambda$, SWs are destructively interfering if $\Delta\phi = 0$ and constructively if $\Delta\phi = \pi$. To correctly read the outputs, the distance d_6 and d_7 must be multiples of λ. The multiplicity factor determines whether the direct or inverted output value is made available. Reading a non-inverted output at O_1 and O_2 requires $d_6 = d_7 = n\lambda$, while if the output complement is of interest, O_1 and O_2 should be positioned at $d_6 = d_7 = (n + \frac{1}{2})\lambda$. In addition, there are two ways to detect the output: (i) Detection based on the phase, and (ii) Detection based on the threshold[14]. Phase detection method is based on a predefined phase reading, i.e., if the detected spin wave has a phase of π, then the result is logic 1, and a logic 0 if the detected spin wave has a phase of 0. However, threshold detection method is based on a predefined threshold, i.e., if the output magnetization is greater than or equal to a certain threshold, then the gate output is 0 and 1 otherwise.

B. Logic Function Programming

The logic function performed by the structure in Figure 3 depends on the detection mechanism as follows: (i) If phase detection is utilized the gate can evaluate (N)AND and (N)OR operators and (ii) if threshold detection is in place the structure implements X(N)OR.

To explain the programmable 2-input gate operation based on phase detection, we consider the structure in Figure 3 under the assumption that the control signals are $C_1 = 0$ and $C_2 = 1$. If a logic 0 is applied on both I_1 and I_2, spin-waves with the same frequency, wavelength, and phase are excited in both horizontal waveguides. In the first stage, SW generated at I_1 constructively interferes with the one generated at C_1. The resulting SW continues the propagation downwards in the waveguide and eventually constructively interferes with the spin wave emitted by I_2, which results in a logic 0 at the output cell O_1 because the interference results in a SW with phase of 0. If $I_1 = 0$ and $I_2 = 1$, the waves (from C_1 and I_1) interfere constructively and the resulted SW propagates downwards to destructively interfere with the wave from I_2, which results in a logic 0 at the output cell O_1 because the interference results in a SW with phase of 0. When $I_1 = 1$ and $I_2 = 0$, the waves from the I_1 and C_1 interfere destructively, which diminishes the resulted SW energy to a minimum if not make it vanish completely. Thus, the wave emitted by I_2 is the only one still present in the waveguide and propagates to the output resulting in a logic 0 at O_1 because the interference results in a SW with phase of 0. Finally, when $I_1 = 1$ and $I_2 = 1$, the same interference as in the previous case happens but since I_2 is now logic 1, the output is logic 1 at O_1 because the interference results in a SW with phase of π. Thus, the left side of the structure behaves as an AND gate. Following the same line of reasoning, one can easily demonstrate that the right side behaves as an OR gate. By changing the control signals values to $C_1 = 0$ and $C_2 = 0$, $C_1 = 1$ and $C_2 = 0$, and $C_1 = 1$ and $C_2 = 1$ the gate functionality is changed to (AND, AND), (OR,AND), and (OR,OR), respectively. Thus the gate can provide fanout of 2 OR/AND behaviour but also the parallel evaluation of both AND and OR over the same input values. Furthermore, the gate can also produce NOR and NAND if the outputs are read at distances d_6 and d_7 equal to $(n + \frac{1}{2})\lambda$. Thus the gate is capable to evaluate a rich set of function combinations, e.g., (NAND, NAND), (NOR,NAND), (NOR,NOR), (NAND, AND), (NOR,AND), (NOR,OR).

If thresholding-based output detection is utilized, the performed functions change into

TABLE I. Parameters

Parameters	Values
Magnetic saturation M_s	1.1×10^6 A/m
Perpendicular anisotropy constant k_{ani}	8.3177×10^5 J/m^3
damping constant α	0.004
Waveguide thickness t	1 nm
Exchange stiffness A_{exch}	18.5 pJ/m

XOR and XNOR. This relates to the fact that in this case the output SW phase is ignored and the output logic value is asserted based on the SW energy level or Magnetization Spinning Angle (MSA) which can be calculated as:

$$MSA = \arctan\left(\frac{\sqrt{(\overline{m_x})^2 + (\overline{m_y})^2}}{M_s}\right), \tag{3}$$

where $\overline{m_x}$ and $\overline{m_y}$ are the x and y magnetization components, respectively.

We also note that, as output detection methods are not mutually exclusive, one output can be read in phase and the other one by thresholding, which enables the parallel evaluation of mixed function pairs, e.g., (AND,XOR), (OR,XOR).

IV. SIMULATION SETUP AND EXPERIMENTS

To validate the behaviour of the proposed SW programable gate we make use of an Object Oriented MicroMagnetic Framework (OOMMF)[28] based simulation platform.

During the OOMMF simulations we made use of the parameters summarized in Table I[29] and to automate the simulation process we developed a Tckl/Tk script. To demonstrate the functionality of the proposed structure, we considered $Fe_{60}Co_{20}B_{20}$ magnetic waveguides of 50 nm width, with a perpendicular magnetic anisotropy field greater than the magnetic saturation, thus no external magnetic field is required[29]. (N)AND/(N)OR and X(N)OR gates for waveguide width $w = 50$ nm are instantiated based on the proposed structure. To determine the SW frequency, we have chosen a SW wavelength $\lambda = 110$ nm, which means that $d_1 = d_2 = d_3 = d_4 = d_5 = d_6 = d_7 = 110$ nm, and from the dispersion relation calculated based on the parameters in Table I and wavelength, the SW frequency is determined as $f = 9$ GHz at a spin wave number $k = 2\pi/\lambda = 57$ rad/μm.

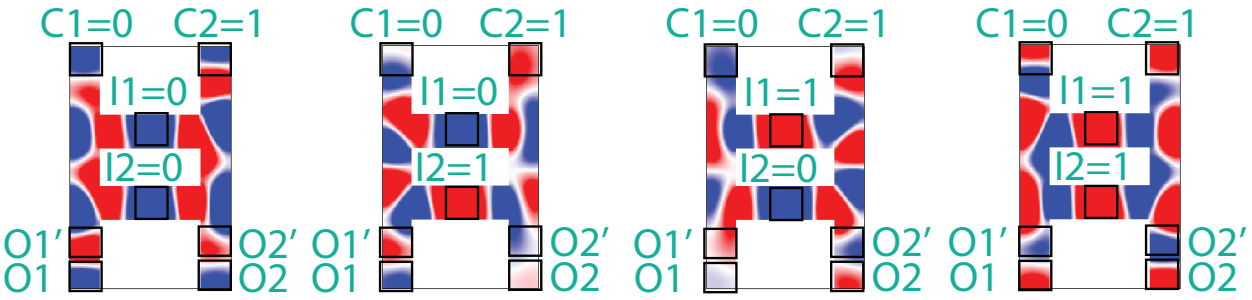

FIG. 4. Fan-in of 2 AND/OR Gate OOMMF Simulation

A. Phase Detection based AND/OR gate

Figure 4 presents the simulation results for a 2-input gate with $C_1 = 0$ and $C_2 = 1$. The color code in the figure is: Red (dark) represents logic 1 and Blue (light) represents logic 0. The visual inspection of Figure 4 reveals that the structure simultaneously produces AND and OR over the two inputs. O_1 provides the AND function, i.e., $O_1 = 0$ for the input combinations ($I_1I_2 = 00$, $I_1I_2 = 01$, $I_1I_2 = 10$), and $O_1 = 1$ for $I_1I_2 = 11$. Similarly, O_2 produces the OR function, i.e., $O_2 = 1$ for the input combinations ($I_1I_2 = 01$, $I_1I_2 = 10$, $I_1I_2 = 11$), and $O_1 = 0$ for $I_1I_2 = 00$. Note that O_1 and O_2 are placed at $d_6 = d_7 = 110$nm ($n = 1$) such that direct functions are obtained. The Figure also indicate that NAND and NOR functions are obtained at outputs O_1' and O_2' by just shifting the output reading points by $\lambda/2$ such that $d_6 = d_7 = 55$nm ($n = 0$). Hence, Figure 4 demonstrates the correct behaviour of the proposed 2-input 2-output logic gates. However, as one can observe in the Figure input value depended output signal strengths are obtained. For example, O_2 is weaker than O_1 when the inputs are $(0, 0)$ because in the left column two constructive interferences take place (resulting in a strong output), while in the right column one destructive and one constructive interference occur (resulting in a weaker output). Thus, the output detection mechanism must be able to deal with such variability phenomena.

B. Threshold Detection based XOR/XNOR gate

Table II presents the normalized Magnetization Spinning Angles (MSA) values at O_1 and O_2 for $C_1 = C_2 = 0$ and all possible I_1 and I_2 input values. The MSA values in the Table are computed based on Equation (3) and normalized with respect to the highest MSA, which in this case is obtained when $I_1I_2 = 00$. Note that the results for the other possible control

TABLE II. 2-input 2-output Gate Normalized Output MSAs

Cases			O_1/I_1	O_2/I_1
$C_1 = C_2$	I_2	I_1		
0	0	0	1	1
0	0	1	0.28	0.28
0	1	0	0.37	0.37
0	1	1	0.45	0.45

input combinations, i.e., C_1C_2=01, C_1C_2=10, and C_1C_2=11, are similar to those obtained for $C_1C_2 = 00$.

The basic idea behind the threshold based output value interpretation is to define an appropriate MSA value MSA_{th} and, e.g., classify the gate output as 0 if its MSA value is larger than MSA_{th} and 1 otherwise. By applying this principle on the Table II values and choosing $MSA_{th} = 0.41$ the gate outputs will be both 0 if $I_1I_2 = 00$ and $I_1I_2 = 11$ and 1 otherwise, which means that the gate provides the XOR functionality. If the detection rule is changed such that logic 1 is reported when the normalized MSA value is larger than MSA_{th} and logic 0 otherwise, the proposed structure evaluates an XNOR function. Thus, in this case the output reading location is not relevant as the inverted version of the output is obtained by switching the thresholding rule.

V. PERFORMANCE EVALUATION AND DISCUSSION

To asses the implications of our proposal, we make use of the proposed gate to implement a fanout of 2 3-input majority (MAJ3) gate, evaluate its area, delay, and energy consumption and compared it with the state of the art SW[30], and 15 nm CMOS based counterparts.

To this end we instantiated a MAJ3 gate design with a waveguide width of 48 nm and $\lambda = 96$ nm and validated it by means of OOMMF simulations as presented in Figure 5. For a fair comparison with the MAJ3 implementation in[30], we made use of the same assumptions: (i) ME cells are utilized for SW excitation and detection, (ii) ME cell parameters are: Area = 48 nm × 48 nm area, Energy=$i \times C_{ME} \times V_{ME}^2$, where i is the number of excitation cells, $C_{ME} = 1$ fF, $V_{ME} = 119$ mV), and Switching Delay = 0.42 ns , (iii) We moved the output locations of our design and placed them immediately after the interference points,

i.e., $d_6 = d_7 = 0$, (iv) MAJ3 gate outputs are directly driving the following SW gates, thus no delay and energy overhead is accounted for the ME cells at the gate output, and (v) The spin-wave through the waveguide propagation delay is negligible. Note that due to the SW technology early stage of development some of these assumptions might not accurately reflect the physical reality, but their discussion is out of the scope of this paper.

In addition, in order to compare with CMOS, we evaluated a 3-input Majority gate implemented with two NAND gates and one OR-AND-Invert (OAI) gate in 15 nm technology at $V_{dd} = 0.8$ V, 25°C, and an output load capacitance of 20 fF.

Table III presents our evaluation results, it indicates that while the proposed SW gate is 14x slower than the CMOS counterpart it provides a 42% energy consumption reduction while requiring 12x smaller area. The Table also indicate that the Majority gate in[30] is slightly more energy efficient. However, the design in[30] can only provide a single output, which means that if multi-output is desired replication is required which result in area and energy overhead. For example, if 2 outputs are required when using the design in[30], the structure must be replicated twice, which is doubling the energy consumption and area to 86.6 aJ and 0.0691 μm^2, respectively. Given that our design consumes 56.6 aJ, and requires 0.0576 μm^2, it provides 33%, 16% energy and area reduction, respectively, without any

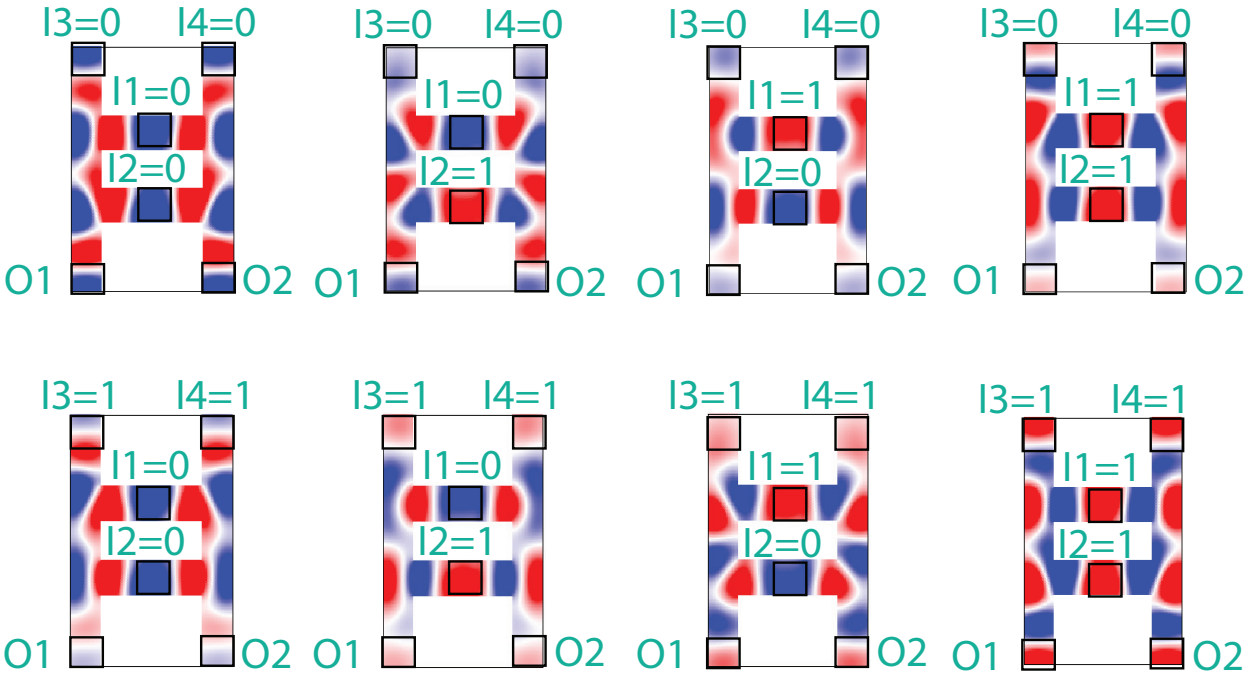

FIG. 5. 3-input Majority Gate

TABLE III. Performance Comparison

	CMOS	SW[30]	SW
Technology	15 nm CMOS	SW	SW
Implemented function	2-output MAJ3	1-output MAJ3	2-output MAJ3
Number of used cell	16 transistors	4 ME cells	6 ME cells
Fanout capability	>2	1	2
Delay (ns)	0.031	0.42	0.42
Energy (aJ)	98	43.3	56.6
Area (μm^2)	0.688	0.0346	0.0576

delay overhead.

In the remainder of this section we briefly discuss issues related to the scalability of our proposal and some practical implementation aspects.

Logic Scalability: The proposed structure is certainly scalable in terms of inputs and outputs. Additional inputs can be added by increasing the number of ladder steps. However, as the number of inputs increases, the inputs nearer to the outputs must be excited at lower energy to compensate for the potential degradation due to the damping effect in the waveguides of the SW inputs traveling from more faraway inputs. If the SW propagation delay is neglected the gate delay is number of inputs independent, while the energy increases linearly as the it is proportional to the number of inputs. In addition, the area of the proposed structure increases linearly with the number of inputs as the structure length increases by $w + \lambda$ when an input is added to the structure and the structure width is constant. In term of outputs, the scalability is limited by the number of columns. However, because SW propagates in all directions the two columns can be vertically extended such that outputs (up to 4) can be read both at the top and bottom of each column. Thus the number of inputs and outputs of the proposed structure can be increased as depicted in Figure 6, but the detailed design of such a structure is out of the scope of this paper.

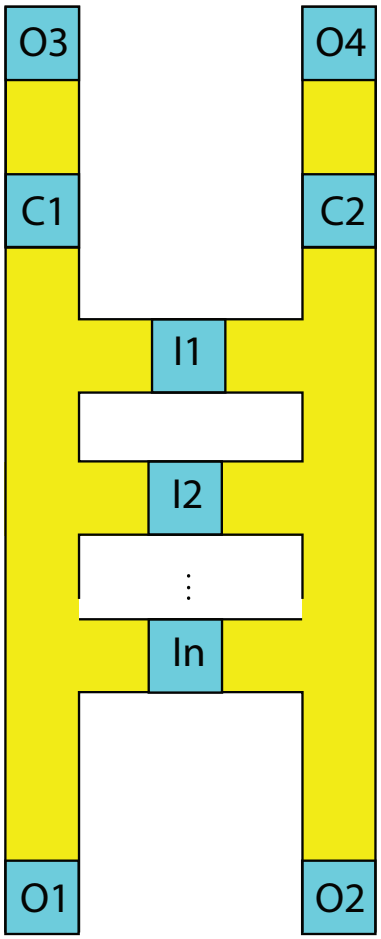

FIG. 6. Multi-input Multi-output Programmable Logic Gate

Geometrical Scaling: To examine the effect of the waveguide width scaling on the functionality of the proposed structures, two additional designs with waveguide widths of 30 nm and 75 nm were instantiated and validated by means of OOMMF simulations. We noticed that the width scaling does not detrimentally affects the functionality of the proposed structures and that when the waveguide width increases, the output MSA values increase as larger ME cells can excite stronger spin-waves.

Balanced Spin Wave Strength: It was noticed that the controls and data inputs contribute differently to the outputs. This is related to the fact that the control inputs have a larger contribution to the outputs than the data inputs as they have a direct straight path to the output, while the data inputs have bent region at the edges. Therefore, C_1 and C_2 must be excited at lower energy than I_1 and I_2 to balance the spin waves strength, and guarantee that the gate functions correctly. Furthermore, it was observed that all inputs

C_1, C_2, I_1 and I_2 affect both outputs O_1 and O_2. Thus, C_1 has an effect on O_2, and C_2 has an effect on O_1, which might create a problem when different gates are captured at both outputs O_1 and O_2. Therefore, to guarantee a proper gate functioning correctly, it must be ensured that C_1, I_1 and I_2 contribute more on output O_1 compared to C_2, and that the contribution of C_2, I_1 and I_2 on output O_2 is more than the contribution of C_1.

Variability: The main purpose of this paper has been to propose the concept and validate it by means of micromagnetic simulations under ideal conditions even if it is obvious that waveguide dimension variations, edge roughness, and spin wave strength variation might affect the gate functionality. However, given the actual development of the SW technology such aspects cannot be investigated for the time being but we certainly consider them as future work when relevant technology data became available.

Thermal Noise: Generally speaking the thermal noise is a circuit design crucial issue. However, for spin wave technology, the Curie temperature, which is the temperature at which the magnetic properties of the material are changing, is high for the ferromagnetic materials, e.g., Curie temperature for CoFeB=1000 K[19]). So, it is expected that limited temperature variations over the room temperature do not fundamentally affect the gate behaviour. However, further investigations on the thermal impact are part of planned future work.

VI. CONCLUSIONS

We introduced and evaluated by means of Object Oriented Micromagnetic Framework (OOMMF) simulations a novel 2-input 2-output Spin Wave based Programmable Logic Gate with a ladder shape structure capable to evaluate any pair of AND, NAND, OR, NOR, XOR, and XNOR Boolean functions. To get inside into the potential practical implications of our proposal we made use of such a gate to instantiate a 3-input Majority gate, which we evaluated and compared with state of the art equivalent implementations in terms of area, delay, and energy consumptions. Our estimates indicated that the proposed gate provides 33% and 16% energy and area reduction, respectively, when compared with spin-wave counterpart and 42% energy reduction while consuming 12x less area when compared

to a 15 nm CMOS implementation.

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