MOSFET-C Filter with Low Excess Noise and Accurate Automatic Tuning

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Abstract—**Continuous-time integrated filters having a maximum dynamic range at the audio-frequency range are obtained using MOSFET-C filters. In combination with a careful design of the applied symmetrical amplifiers in a BiCMOS technology, the detrimental influence of $1/f$ noise can be minimized. A 98-dB dynamic range (THD < 0.3%) is obtained in a realized fifth-order Butterworth low-pass filter, while the overall $1/f$ noise corner frequency is limited to 250 Hz. Automatic adjustment of the filter cutoff frequency is performed using a novel all-silicon automatic tuning system that, compared with traditional automatic tuning systems, demands reduced overhead circuitry.**

I. Introduction

THE achievement of a sufficiently high dynamic range in combination with a high linearity, a minimum chip area, and minimum power consumption is generally the main objective for continuous-time integrated filters. An important figure of merit that combines noise performance with linearity is the intermodulation-free dynamic range (IMFDR). The IMFDR is defined as the ratio between that level of two sine waves with equal amplitude for which the level of the intermodulation products is equal to the noise floor and the noise floor itself.

A major limitation of integrated technology is the absence of usable inductors, while only small capacitors are available as reactive elements. Consequently, the requirement of a filter transfer with complex poles can only be met using active filters. A basic building block of continuous-time active filters is an active integrator. Maximization of the (intermodulation-free) dynamic range of the entire filter implies both optimization of a single integrator and optimization of the filter structure [1]. The implementation of active integrators having a maximum (intermodulation-free) dynamic range for audio frequencies for a given chip area and power consumption is dealt with in Section II. Subsequently, Section III describes the design of a symmetrical amplifier applied in MOSFET-C filters.

The transfer of a filter in the frequency domain can be normalized with respect to a certain cutoff frequency (or central frequency). In integrated active filters, the (dimensionless) coefficients of the normalized filter transfer can be established as ratios of on-chip component values, which are generally well matched. The cutoff frequency, however, is determined by absolute component values. The large absolute tolerance generally makes tuning of this cutoff frequency necessary. Section IV presents a novel automatic tuning system that, compared with traditional tuning systems, requires a reduced amount of overhead circuitry.

As an application example, Section V presents a prototype continuous-time filter, implemented in a BiCMOS technology. The application of this filter as an output filter of a synchronous detector for an AM shortwave upconversion receiver [2], [3] requires a fifth-order Butterworth low-pass filter with a 3.3-kHz cutoff frequency, having a dynamic range of at least 90 dB (THD < 0.3%) and a second- and third-order IMFDR of at least 70 and 77 dB, respectively. The applied calculation model for MOS transistors is outlined in the Appendix.

II. Integrator Implementations

An active integrator is realized around a resistive voltage-to-current transfer and a capacitor as a current-to-voltage integrator. In order to facilitate automatic tuning, the integration time constant has to be electrically adjustable. Since (fixed) oxide capacitors are largely preferred because of the excellent linearity and matching, this facility requires electrically adjustable resistive voltage-to-current transfers.

Electrically adjustable resistive transfers are commonly realized using MOS transistors as transconductance elements or as gate-controlled resistors. Balanced integrator structures are applied in order to cancel even-order nonlinearity emerging from the quadratic behavior of MOS transistors. For low-frequency applications (< 100 kHz), special attention must be paid to the detrimental influence of $1/f$ noise (also called excess noise or flicker noise) upon the dynamic range.

Fig. 1 shows an elementary integrator architecture, built up around a source-coupled pair as a transconductance element. Using the square-law drain-current model in the saturation region, given in the Appendix, the small-signal integrator transfer is calculated as

$$\frac{V_o(s)}{V_i(s)} = \frac{1}{s\tau} = \frac{\sqrt{\beta I_T}}{2sC} = \frac{g_m}{2sC}. \quad (1)$$

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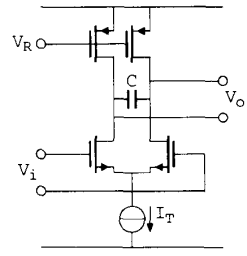

Fig. 1. Elementary integrator architecture.

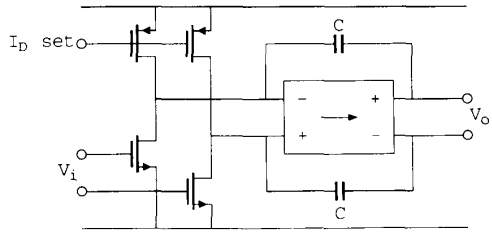

Fig. 2. Alternative transconductance integrator.

The small-signal transconductance g_m and hence the integration time constant τ are adjusted by the tail current I_T.

From the Appendix (equation (A6)), it follows that the equivalent input noise voltage in a frequency range Δf can be calculated as

$$V_{ni}^2 = \frac{8kT\tau}{3C}\int_{\Delta f}\left[1+\frac{f_{ln}}{f}+\frac{g_{mp}}{g_{mn}}\left(1+\frac{f_{lp}}{f}\right)\right]df \qquad (2)$$

where the indexes n and p indicate the NMOS and PMOS transistor, respectively. The frequency f_l expresses the noise corner frequency for which the $1/f$ noise level equals the thermal noise level. For drain currents of about 10 μA, f_{ln} is in the order of magnitude of 300 kHz and f_{lp} is in the order of magnitude of 10 kHz in the applied process. Comparable results are obtained for a PMOS source-coupled pair using NMOS current sources.

An alternative transconductance integrator, depicted in Fig. 2, uses NMOST's biased in the triode region. According to the Appendix, a constant drain–source voltage results in a linear transfer from the gate–source voltage to the drain current. With V_{DS} the drain–source bias voltage, the integrator transfer is equal to

$$\frac{V_o(s)}{V_i(s)} = \frac{1}{s\tau} = \frac{\beta V_{DS}}{sC} = \frac{g_m}{sC}. \qquad (3)$$

This drain–source bias voltage and hence the integration time constant is adjusted by the PMOS current sources.

In analogy with the saturated transconductance integrator, the equivalent input noise voltage in a frequency range Δf is calculated as

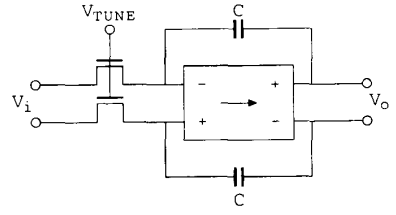

Fig. 3. Principle of MOSFET-C integrator using gate-controlled MOS resistors.

$$V_{ni}^2 = \frac{8kT\tau}{C}\int_{\Delta f}\left[\frac{V_G}{V_{DS}}\left(1+\frac{f_{l'n}}{f}\right)+\frac{2g_{mp}}{3g_{mn}}\left(1+\frac{f_{lp}}{f}\right)\right]df. \qquad (4)$$

The $1/f$ noise corner frequency $f_{l'}$ in the triode region is much smaller than the corner frequency in the saturation region. In the applied process, this corner frequency is in the order of magnitude of 50 kHz for NMOST's using $I_D \approx 10$ μA. If the amplifier is optimally designed, its noise contribution can be kept lower than that of the triode transconductance transistors.

Fig. 3 shows the principle of a MOSFET-C integrator that uses gate-controlled MOS resistors. According to the Appendix, the equivalent resistance of a gate-controlled MOS resistor with zero bias current is calculated as

$$R_m = \left.\frac{dV_{DS}}{dI_D}\right|_{V_{DS}=0} = \frac{1}{\beta V_G} \qquad (5)$$

which results in the integrator transfer

$$\frac{V_o(s)}{V_i(s)} = \frac{1}{s\tau} = \frac{1}{sR_mC}. \qquad (6)$$

The thermal noise of a MOS resistor with zero bias current corresponds to that of its ohmic equivalent, while the $1/f$ noise is totally absent. Provided that the symmetrical amplifier is well designed, the equivalent input noise voltage of this integrator is completely determined by the thermal noise of the MOS resistors:

$$V_{ni}^2 = 8kTR_m\Delta f = \frac{8kT\tau\Delta f}{C}. \qquad (7)$$

If we compare the equivalent input noise voltages of the given integrator implementations for equal values of the time constant τ and the capacitance C, the MOSFET-C integrator has the lowest noise level, especially for low frequencies. The signal handling capability of these integrators does not significantly differ, since they are bounded by the available supply voltage. Consequently, MOSFET-C filters provide the highest dynamic range for audio-frequency applications.

Calculation of the distortion of MOSFET-C filters is based upon the drain current model given in the Appendix. From (A4), the differential-mode input current as a function of the differential-mode input voltage of the

MOSFET-C integrator is derived as

$$i_{d1} - i_{d2} = \beta\left\{V_G v_i - \frac{\epsilon}{2} v_i^2 + \frac{\gamma}{96} V_B^{-3/2} v_i^3\right\}. \quad (8)$$

In this equation, ϵ denotes a small imbalance in transistor parameters. Measurements of the applied MOS resistors show that the effect of mobility degradation can practically be ignored in this specific case. As a result, the second- and third-order IMFDR's are calculated as

$$\text{IMFDR}_2 = \sqrt[4]{\frac{V_G^2 C}{4\epsilon^2 kT\tau\Delta f}} \quad (9)$$

$$\text{IMFDR}_3 = \sqrt[3]{\frac{8V_B^{3/2} V_G C}{\gamma kT\tau\Delta f}}. \quad (10)$$

The maximum input voltage for which the MOS transistors remain in the triode region is almost equal to $2V_G$, which results in a dynamic range:

$$\text{DR} = \sqrt{\frac{V_G^2 C}{4kT\tau\Delta f}}. \quad (11)$$

Additional odd-order nonlinearity cancellation by the double-MOSFET method is not applied, since this method increases the thermal noise level and does not compensate for the residual even-order nonlinearity due to component mismatches [5].

III. Design of a Symmetrical Amplifier

A MOSFET-C integrator requires a fully balanced amplifier with a sufficiently high differential-mode voltage gain and an accurate output common-mode voltage. The limited value of on-chip capacitances combined with a low cutoff frequency requires large MOS resistors R_m in the order of magnitude of 100 kΩ to 1 MΩ. The equivalent input noise voltage of the amplifier must not exceed the noise voltage of these resistors.

Optimum noise matching with the MOS resistors in combination with a maximum gain and a high common-mode rejection is obtained using a PMOS source-coupled pair as input stage. The transfer and noise behavior of a similar source-coupled pair was already dealt with in Section II. As mentioned before, the $1/f$ noise corner frequency of PMOS transistors is much lower than that of NMOS transistors. The common-mode rejection is important in order to prevent common-mode instability by parasitic common-mode loops within the filter.

The current sinks of the input stage are commonly implemented using NMOS transistors. At low frequencies, the $1/f$ noise of these NMOS transistors dominates over the noise of the PMOS input stage and even over the thermal noise of the MOS resistors. If these current sinks are replaced by ordinary resistors, the resulting loss of amplifier gain is generally unacceptable, unless a bipolar second stage is applied. Current sinks using bipolar transistors are not considered as a useful alternative because of the high level of the collector-current shot noise.

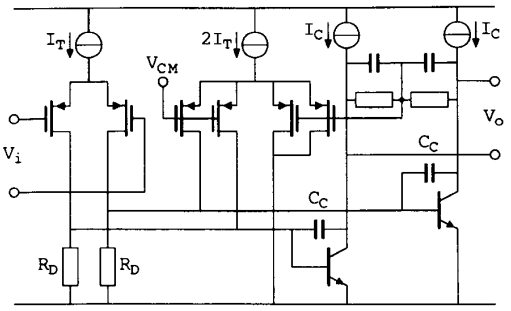

Fig. 4. Two-stage BiCMOS amplifier with common-mode feedback.

A two-stage BiCMOS amplifier, using a bipolar common-emitter stage as second stage, is depicted in Fig. 4. The output voltage swing of this bipolar output stage is nearly rail to rail. Accurate common-mode sensing is performed using two diffused resistors and the double source-coupled pair provides for a maximum common-mode accuracy [3], [4]. The capacitors C_C are added for phase compensation.

The small-signal low-frequency differential-mode voltage gain of the amplifier according to Fig. 4 is calculated as

$$G_{dm} = g_{mp} \frac{R_D}{R_D + r_\pi} \beta_f R_L \quad (12)$$

where $g_{mp} = \sqrt{\beta_p I_T}$ is the transconductance of the PMOS input transistor and β_f is the current gain of the n-p-n transistors. The common-mode sense resistors are part of the effective load resistance R_L, calculated from each output to ground. The input impedance r_π of the bipolar output stage is equal to

$$r_\pi = \frac{\beta_f V_T}{I_C} \quad (13)$$

in which V_T is the thermal voltage. With $R_D = V_{BE}/I_T$, (12) can be written as

$$G_{dm} = \sqrt{\beta_p I_T} \frac{V_{BE}}{V_{BE} + \beta_f V_T I_T / I_C} \beta_f R_L. \quad (14)$$

If the base current is ignored, a maximum voltage gain for a given collector current I_C is found if

$$I_T = \frac{V_{BE} I_C}{\beta_f V_T} \quad (15)$$

and consequently, $R_D = r_\pi$. This maximum voltage gain is equal to

$$G_{dm} = \frac{1}{2} g_{mp} \beta_f R_L. \quad (16)$$

The equivalent input noise voltage of the amplifier for $R_D \approx r_\pi$ is completely determined by that of the input

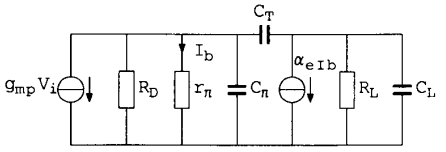

Fig. 5. Single-ended amplifier model for calculation of high-frequency behavior.

source-coupled pair:

$$S(v_{ni}) = \frac{16kT}{3g_{mp}}\left(1+\frac{f_{lp}}{f}\right). \tag{17}$$

With a low bias current I_T of some tens of microamperes, the $1/f$ noise corner frequency f_{lp} of the PMOS transistors is limited to 10 kHz or even lower. The $1/f$ noise can be neglected in the weighed audio spectrum if the overall corner frequency of the integrator does not exceed 500 Hz, which results in the condition

$$g_{mp} > \frac{40}{3R_m}. \tag{18}$$

In this case, the filter noise is determined by the noise of the integration resistors only.

For high frequencies ($f \gg 1/\tau$), the integration capacitors can be regarded as a unity feedback. A single-ended amplifier model for the calculation of the high-frequency behavior is depicted in Fig. 5. In this figure, C_π is the bipolar transistor base–emitter capacitance, while the collector–base capacitance is incorporated in the compensation capacitance C_T. The input capacitance of the PMOS input stage and the parasitic substrate capacitance of the filter capacitors are part of the total load capacitance C_L. The drain resistor R_D is assumed to be equal to r_π.

If we assume $\beta_f \gg 1$ and $\beta_f R_L \gg r_\pi$, the poles in the amplifier transfer can be calculated as

$$p_1 \approx -\frac{1}{R_L(C_L+\beta_f C_T/2)} \tag{19}$$

$$p_2 \approx -\frac{2+\beta_f C_T/C_L}{r_\pi(C_T+C_\pi)} \tag{20}$$

in which p_1 is the most dominant one ($p_1 \ll p_2$). The resulting unity-gain angular frequency ω_t is equal to

$$\omega_t = -G_{dm}p_1 = \frac{g_{mp}}{C_T+2C_L/\beta_f}. \tag{21}$$

Since the most dominant pole p_1 gives a phase lag of 90° at ω_t, the phase margin ϕ_m is calculated as

$$\phi_m = 90° - \arctan\left(\frac{G_{dm}p_1}{p_2}\right) \tag{22}$$

in which

$$\frac{G_{dm}p_1}{p_2} = \frac{g_{mp}}{g_{mn}}\frac{(C_T+C_\pi)C_L}{(C_T+2C_L/\beta_f)^2}. \tag{23}$$

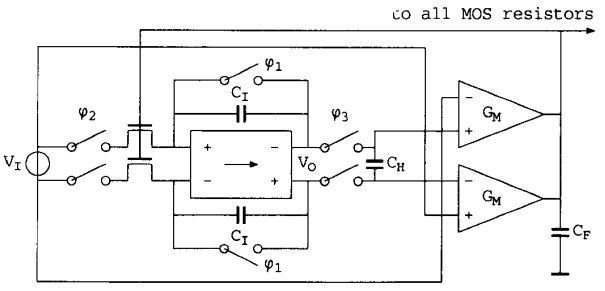

Fig. 6. Novel elegant tuning technique.

In this equation, $g_{mn} = I_C/V_T$ is the transconductance of the bipolar output transistors. A minimum required phase margin of 45° results in the relation

$$\frac{g_{mn}}{g_{mp}} \geq \frac{(C_T+C_\pi)C_L}{(C_T+2C_L/\beta_f)^2}. \tag{24}$$

The small-signal behavior of the common-mode feedback loop is similar to the unity-feedback differential-mode behavior. The common-mode loop gain, however, is approximately half the differential-mode gain G_{dm}. Since the phase lag of the common-mode sense resistors is compensated by two bypass capacitors (see Fig. 4), differential-mode stability also implies common-mode stability.

In an implementation of a fifth-order MOSFET-C filter, described in Section V, the symmetrical amplifier is dimensioned using a 0.1-mA collector current for the bipolar output transistors. With $V_{BE} = 0.7$ V, $\beta_f \approx 190$ $\mu A/V^2$, and $\beta_p = 250$ $\mu A/V^2$, a maximum voltage gain is obtained if $R_D = r_\pi = 48$ kΩ and $I_T = 15$ μA. The transconductance of the input transistor $g_{mp} = 61$ $\mu A/V$. The maximum voltage gain is 49 dB for an effective load resistance $R_L = 50$ kΩ. Using a 1-pF compensation capacitance, the calculated unity-gain bandwidth is 6.4 MHz with a 57° phase margin. The output capacitance in this case is 50 pF for each output to ground. The measured transfer does not significantly differ from the calculated one ($G_{dm} = 52$ dB, GBW = 6 MHz, and $\phi_m = 55°$).

IV. Automatic Tuning

In continuous-time integrated filters, tuning of the cutoff frequency is usually performed automatically by means of indirect tuning techniques. The integration time constants of one or more additional integrators, implemented on the same chip as the filter itself, are related to a reference frequency. If *all* integrators are simultaneously tuned, the value of the cutoff frequency is related to the reference frequency as well. The accuracy of such tuning techniques is determined by the matching of on-chip component values.

Traditional indirect automatic tuning concepts use two active integrators configured as a two-integrator oscillator in a PLL or as a frequency discriminator in a frequency control loop [5]. Fig. 6 shows a novel elegant tuning technique, in which the integration time constant of only

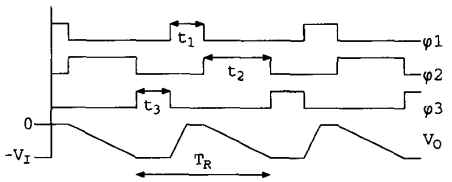

Fig. 7. Timing diagram.

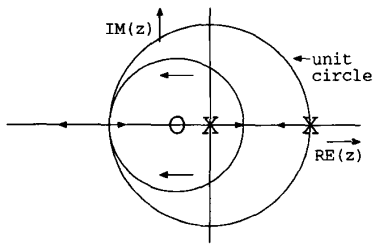

Fig. 8. Root locus of sampled feedback system as a function of k.

one additional integrator is compared with a time reference. The timing and control is performed directly with switches, which are driven by the reference timing signals φ_1, φ_2, and φ_3. This technique is called the direct sample tuning technique.

The timing diagram is shown in Fig. 7. During the time φ_1 is active, the integration capacitors are short circuited, forcing the output differential-mode voltage to zero. During the time interval t_2, in which φ_2 is active, a fixed differential input voltage is connected to the integrator input, which results in a ramp voltage at the integrator output. Finally, when φ_3 gets active, the integrated voltage is sampled into the capacitor C_H. This sampled voltage passes through the low-pass filter, consisting of two transconductances G_M and a capacitor C_F, to the gates of all MOS resistors.

In the stationary state, the final sampled voltage V_O is equal to the reference voltage V_I, which is also the integrator input voltage. Consequently, the integration time constant τ_I is tuned to the time interval t_2, which is derived from a reference frequency. The sampled and filtered tuning voltage, applied to all MOS resistors, remains constant with no ripple. Now all absolute values of all time constants, and hence the cutoff frequency, are related to the reference time t_2.

The stability of the sample control loop would pose no problems if the time constant C_F/G_M is made much larger than the autotuning cycle time T_R. However, if all capacitors including C_F have to be implemented on chip, only a limited time constant C_F/G_M can be realized. Because the autotuning circuitry inherently produces no ripple on the resistor tuning voltage in the stationary state, the minimum C_F/G_M mainly depends on the loop stability. Using the z transform [3], the poles of the sample control loop are found with the root-locus equation:

$$\frac{-1}{k} = \frac{3z+1}{8z^2-8z}. \tag{25}$$

The time interval t_2 is assumed to be half the tuning cycle time T_R, while the root-locus factor k is equal to

$$k = \frac{2\beta V_I G_M T_R^2}{C_I C_F}. \tag{26}$$

In this equation β is the proportionality factor of the MOS resistors. The root locus of this sampled feedback system as a function of k is drawn in Fig. 8.

The breakaway point in the root locus at the real axis occurs for $k = 8/9$ at $z = 1/3$ and for $k = 8$ at $z = -1$. For a stable autotuning system without complex poles, we have to choose $k \leqslant 8/9$. However, a smaller value of k is preferred for minimum noise and interference on the tuning voltage. In a prototype integrated filter, described in Section V, $\beta = 1\ \mu A/V^2$, $V_I = 1$ V, $T_R = 32\ \mu s$, and $C_I = 33$ pF. A value of $k = 0.4$ is obtained taking $G_M = 1.25\ \mu A/V$ and $C_F = 200$ pF. Both C_I and C_F are implemented on-chip.

V. Application Example

This section presents a prototype fifth-order Butterworth filter, designed as an output filter of a synchronous detector for an AM shortwave upconversion receiver. For HF interference suppression purposes, this filter has to be implemented as a fourth-order active filter preceded by a first-order passive RC filter [2], [3]. Fig. 9 shows a photomicrograph of the evaluation chip, on which the fourth-order MOSFET-C filter part (Fig. 11) including a first-order MOSFET-C test section (Fig. 10) and the automatic tuning circuitry (see Section IV) have been integrated.

A maximum signal-handling capability for signals within the filter passband requires a unity transfer from the filter input to the output of the integrators for frequencies below the cutoff frequency. For this reason, all integration resistors of one integrator section have the same value.

In order to obtain a Butterworth transfer:

$$|H(s)|^2 = \frac{|V_o|^2}{|V_i|^2} = \frac{1}{1+(\omega/\omega_c)^{10}} \tag{27}$$

the integration time constants have to fulfill the relations:

$$a_1 = \omega_c \tau_1 = 1 \tag{28}$$

$$a_2 = \omega_c \tau_2 = 0.5\sqrt{5} \tag{29}$$

$$a_3 = \omega_c \tau_3 = 0.8\sqrt{5} \tag{30}$$

$$a_4 = \omega_c \tau_4 = 0.5\sqrt{5} \tag{31}$$

$$a_5 = \omega_c \tau_5 = 0.2\sqrt{5}. \tag{32}$$

The angular cutoff frequency is equal to

$$\omega_c = \frac{1}{\sqrt[5]{\tau_1\tau_2\tau_3\tau_4\tau_5}}. \tag{33}$$

The dimensionless normalized filter coefficients a_i are in

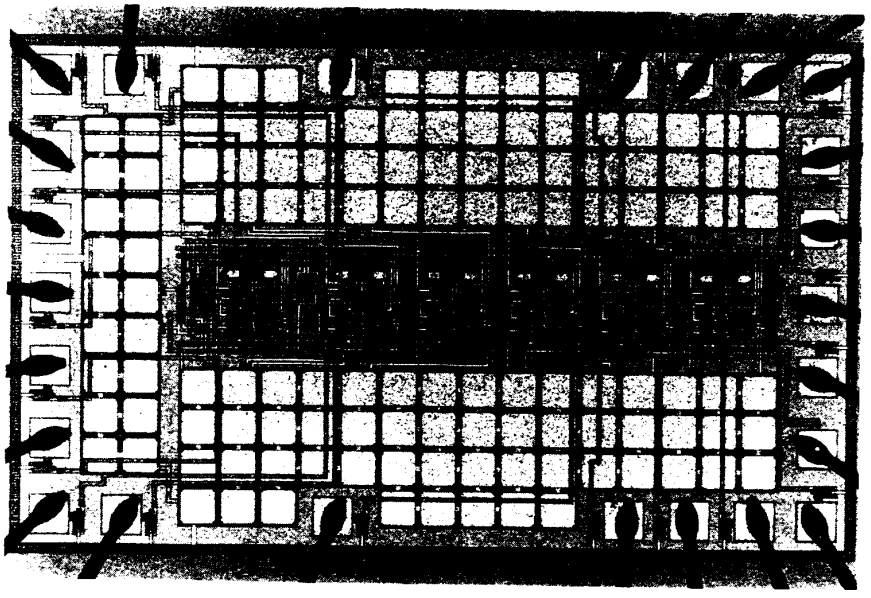

Fig. 9. Photomicrograph of evaluation chip.

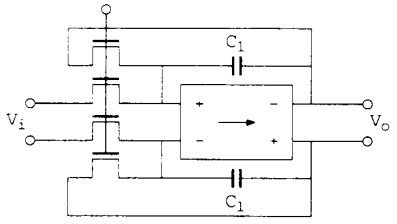

Fig. 10. First-order MOSFET-C test section.

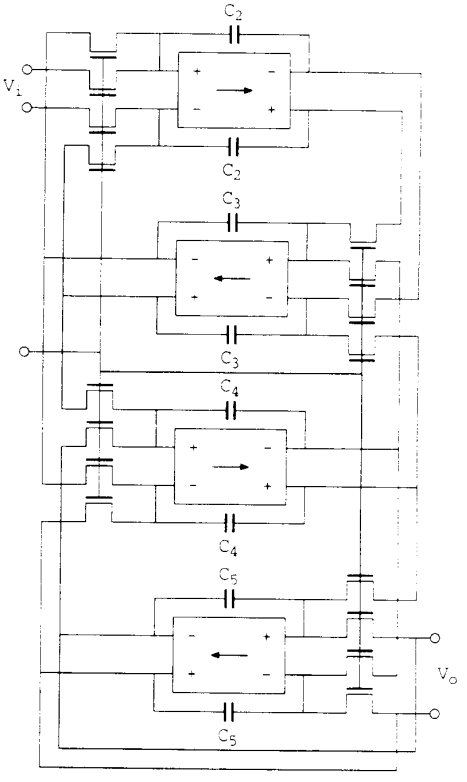

Fig. 11. Fourth-order MOSFET-C filter part.

fact ratios of component values. If all time constants are tuned with the same scale factor, the cutoff frequency can be adjusted without affecting the normalized coefficients and hence shape of the filter transfer. For MOSFET-C filters, this factor depends on the gate control voltage of the MOS resistors (see Section II), which is generated by the automatic tuning system.

The equivalent output noise voltage of the first-order section is calculated as

$$V_{no1}^2 = \frac{16kTR_{m1}}{2\pi}\int_0^\infty \frac{d\omega}{1+\omega^2\tau_1^2} = \frac{4kT}{C_1} \qquad (34)$$

which is, independent of the integration resistance, inversely proportional with the available capacitance. In analogy with this first-order section, the equivalent output noise of the fourth-order section is calculated as

$$V_{no4}^2 = 4kT\sum_{i=2}^{5}\frac{1}{C_i} \qquad (35)$$

and the equivalent output noise voltage of the complete filter is equal to

$$V_{no}^2 = 4kT\sum_{i=1}^{5}\frac{1}{C_i}. \qquad (36)$$

If all MOS resistors are equal and the ratios of the time constants are established as ratios of the capacitor values, the output noise as a function of the total capacitance C_T is expressed by

$$V_{no}^2 = \frac{8kT}{C_T} \sum_{i=1}^{5} \frac{1}{a_i} \sum_{j=1}^{5} a_j \approx \frac{244kT}{C_T}. \quad (37)$$

However, if all capacitor values are equal and the ratios of the time constants are established as ratios of the MOS resistor values of each integrator section, the output noise as a function of the total capacitance C_T is expressed by

$$V_{no}^2 = \frac{200kT}{C_T} \quad (38)$$

which is only 1 dB lower. For a maximum tracking accuracy of the MOS resistors, all MOS resistors are taken as equal and a 1-dB higher noise floor is accepted.

In a silicon prototype, all MOS resistors R_m have the nominal value of 500 kΩ, which results in the capacitor values:

$$C_1 = 99 \text{ pF}$$
$$C_2 = 110 \text{ pF}$$
$$C_3 = 176 \text{ pF}$$
$$C_4 = 110 \text{ pF}$$
$$D_5 = 44 \text{ pF}.$$

With a total capacitance $C_T = 1.078$ nF, the calculated equivalent output noise voltage is 31 μV. Within the filter passband, the calculated noise density of the output voltage corresponds to that of a 10-MΩ resistor ($S(V_{no}^2) = 80\ kTR_m$).

Fig. 12 shows the measured filter transfers from the filter input to the integrator outputs. Within the passband of the filter, all integrators have to handle the same signal level. With a maximum 2-dB overshoot around the cutoff frequency, the signal-handling capability of the complete filter is almost equal to that of a single integrator. The measured filter output noise corresponds to the calculated output noise within 1 dB, while the measured overall $1/f$ noise corner frequency does not exceed 250 Hz.

Using a nominal gate voltage $V_G = 2.2$ V, the measured maximum input signal level for which the total harmonic distortion of one sine wave does not exceed 0.3% is 3.5 V_p (2.5 V rms). In combination with an output noise voltage $V_{no} = 31$ μV, the dynamic range is 98 dB. If we consider two interfering signals in the stopband, the intermodulation distortion is determined by the first MOS resistor pair. In this case, the IMFDR is calculated as

$$\text{IMFDR}_2 = \sqrt[4]{\frac{2V_G^2}{\epsilon^2 V_{no}^2}} \quad (39)$$

$$\text{IMFDR}_3 = \sqrt[3]{\frac{64V_B^{3/2}V_G}{\gamma V_{no}^2}}. \quad (40)$$

With $\epsilon = 1\%$, $V_B = 3.5$ V, and $\gamma = 0.28$, the calculated second- and third-order IMFDR's are 70 and 83 dB, respectively. The measured second- and third-order IMFDR's are 73 and 82 dB, respectively, which is very close to the calculated ones.

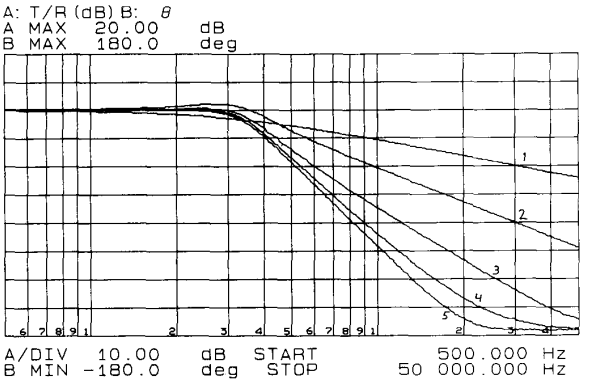

Fig. 12. Measured filter transfers from filter input to integrator outputs.

VI. Conclusions

In conclusion, we can state that for continuous-time integrated filters in the audio-frequency range, MOSFET-C filters are preferred over transconductance implementations. Using MOSFET-C filters in combination with a well-designed BiCMOS amplifier, the detrimental influence of $1/f$ noise can practically be eliminated and the filter noise is completely determined by the unavoidable thermal noise of the filter resistors.

The novel direct sample tuning system proposed in Section IV provides for an all-silicon tuning system with minimum overhead circuitry.

Appendix
Applied MOS Model

The applied MOS drain current formula in the triode region is derived from the Ihantola and Moll model, which can be found in [6, p. 120]:

$$I_D = \beta\Big((V_{GS} - V_{FB} - \phi_B)V_{DS} - \frac{1}{2}V_{DS}^2 + \frac{2}{3}\gamma(V_{SB} + \phi_B)^{3/2} - \frac{2}{3}\gamma(V_{SB} + V_{DS} + \phi_B)^{3/2}\Big). \quad (A1)$$

In this equation, V_{SB} denotes the source–bulk voltage, V_{FB} denotes the flat-band voltage, ϕ_B denotes the surface Fermi potential, and γ denotes the body coefficient.

A simplified expression with a minimum loss of accuracy can be obtained using a Taylor-series expansion up to the third order:

$$I_D = \beta\Big((V_{GS} - V_{TH})V_{DS} - \Big(\frac{1}{2} + \frac{\gamma}{4}V_B^{-1/2}\Big)V_{DS}^2 + \frac{\gamma}{24}V_B^{-3/2}V_{DS}^3\Big). \quad (A2)$$

In this equation, $V_{SB} + \phi_B$ is written as V_B for short, while the threshold voltage V_{TH} is equal to

$$V_{TH} = V_{FB} + \phi_B + \gamma\sqrt{V_B}. \quad \text{(A3)}$$

For (Bi)CMOS processes with lightly doped substrates, the body factor γ is small ($0.3\ \sqrt{\text{V}}$) and the drain current formula can be further simplified to

$$I_D = \beta\left(V_G V_{DS} - \frac{1}{2}V_{DS}^2 + \frac{\gamma}{24}V_B^{-3/2}V_{DS}^3\right). \quad \text{(A4)}$$

The term $V_{GS} - V_{TH}$ is written as V_G for short. This equation is valid for $V_G > V_{DS}$. In the saturation region, for which $V_G < V_{DS}$, the drain current is modeled according to the square law:

$$I_D = \frac{\beta}{2}V_G^2. \quad \text{(A5)}$$

The drain-current spectral noise density of a MOS transistor is given by

$$S(I_{dn}) = 4kT\beta V_G\frac{2}{3}\frac{1+\alpha+\alpha^2}{1+\alpha} + \frac{K_F I_D^{A_F}}{WLC_{ox}}\frac{1}{f}. \quad \text{(A6)}$$

The left-hand term expresses the thermal noise according to [6], where k is the Boltzman constant and T is the absolute temperature. In the triode region, the factor α is equal to:

$$\alpha = 1 - \frac{V_{DS}}{V_G} \quad \text{(A7)}$$

while in the saturation region, $\alpha = 0$. The right-hand part of (A6) expresses the $1/f$ noise according to [7], where K_F and A_F are technology-dependent constants, W is the transistor length, L is the transistor width, and C_{ox} is the oxide capacitance per unit area.

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References

[1] G. Groenewold, "Design of high dynamic range continuous-time integrable bandpass filters," to be published in *IEEE Trans. Circuits Syst.*, vol. 38, 1991.

[2] J. van der Plas and E. H. Nordholt, "A novel extended dynamic range synchronous detector for AM shortwave upconversion receiver," *IEEE Trans. Consumer Electron.*, vol. 35, no. 3, pp. 390–396, Aug. 1989.

[3] J. van der Plas, "Synchronous detection in monolithically integrated AM upconversion receivers," Ph.D. dissertation, Delft Univ. of Technology, Delft, The Netherlands, Nov. 1990.

[4] M. Banu, J. M. Khoury, and Y. Tsividis, "Fully differential operational amplifiers with accurate output balancing," *IEEE J. Solid-State Circuits*, vol. 23, no. 6, pp. 1410–1417, Dec. 1988.

[5] Y. Tsividis, B. Banu, and J. Khoury, "Continuous-time MOSFET-C filters in VLSI," *IEEE Trans. Circuits Syst.*, vol. CAS-33, no. 2, pp. 125–139, Feb. 1986.

[6] Y. P. Tsividis, *Operation and Modeling of the MOS Transistor*. New York: McGraw-Hill, 1987.

[7] A. Vladimirescu and S. Liu, "The simulation of MOS integrated circuits using Spice2," College of Engineering, Univ. of Calif., Berkeley, Memo. UCB/ERL M80/7, Feb. 1980.

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