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A Charge Detection ROIC with Sub-6ppm Error Rate and 200µW Power Consumption in Scanning Electron Microscopy

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***Abstract*— Imaging nanoscopic features with Scanning Electron Microscopes (SEMs) requires rapid specimen scanning with a low-energy electron beam. The electron detector is highly pixelated. Each pixel is interfaced with a high-precision, wide-bandwidth, low-noise readout integrated circuit (ROIC), to enable single-electron counting operation. This paper introduces an innovative power-efficient pixel readout frontend architecture, achieving a time resolution of $2.5\,\text{ns}$. The fabricated prototype in 40 nm CMOS process demonstrates better than 6ppm electron detection precision. It consumes only $200\,\mu\text{W}$, with an area of $150\mu\text{m} \times 100\mu\text{m}$.**

Keywords*— *single electron detection, readout frontend, high-precision, low-offset, comparator

I. Introduction

To produce a high-resolution image that reveals nanoscopic details within a reasonable timeframe, modern scanning electron microscopes (SEMs) utilize a beam of low-energy electrons that rapidly scans the specimen [1] – [3]. As a result, only a limited number of low-energy backscattered and secondary electrons are detected within nanosecond time frames using a pixelated PIN detector, which consists of thousands of individual pixels [3]. Each pixel is coupled with a high-precision, wide-bandwidth, power-efficient readout frontend specifically designed to detect weak charge signals with high accuracy [3]. The objective is to enhance the detection capabilities for signals generated by external electrons impacting the detector at random intervals, achieving both high sensitivity and efficient power consumption.

There are two main readout modes for the PIN detector: short-circuit and open-circuit, as shown in Fig. 1 [4], [5]. The detector can be modeled as a current source (I_{Signal}) in parallel with a capacitor (C_D), representing the generated charge and junction capacitance. In short-circuit mode, the detector is connected to a near-zero impedance load ($Z_L \approx 0$), ensuring that I_{Signal} is promptly transferred rather than stored on C_D. This enables real-time, continuous readout. In practice, a preamplifier creates a virtual ground to approximate this low-impedance path, allowing fast charge extraction. However, it also introduces challenges as the main noise source, limiting bandwidth and increasing power consumption [5].

In open-circuit mode, the detector is connected to a load with infinite impedance ($Z_L = \infty$), causing I_{Signal} to accumulate in C_D rather than flowing into the load. This configuration results in a high-impedance node, where the accumulated charge is converted into a voltage signal directly within the diode itself. The voltage signal is then directly fed to a threshold discriminator, which compares it with a reference threshold level to detect the presence of an incoming signal [3], [5].

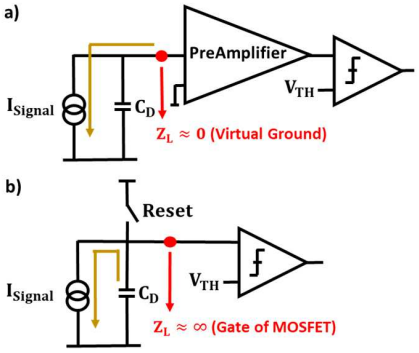

Fig. 1. Two primary modes of reading out the signal generated by the PIN detector: (a) short circuit mode and (b) open circuit mode.

Operating in open-circuit mode presents several challenges, with charge pileup being among the most critical [3]. Charge pileup occurs when multiple electron impacts cause the voltage across C_D to approach the diode's threshold voltage, leading to signal gain compression—where additional incoming charge results in diminishing changes to the output voltage. This non-linearity reduces measurement accuracy, making it difficult to precisely detect and quantify incoming signals. Reliable detection also hinges on the discriminator's precision and speed: high precision enables weak signal detection, while fast response avoids missed events during rapid bursts [6]. Techniques like auto-zeroing and dynamic thresholding enhance both aspects [5], improving detection accuracy and overall system reliability.

In the targeted application of this paper, the ultimate goal is to detect input charge signals (Q_{in}) as small as $200\,\text{aC}$ (equivalent to 1250 electrons) with a time resolution of $2.5\,\text{ns}$ at the moment of occurrence. This level of precision allows for an event rate of up to $400\,\text{MEvents/s}$. Another critical challenge is minimizing power consumption, which must remain below $500\,\mu\text{W}$ [7] – [9].

State-of-the-art readout integrated circuits (ROICs) predominantly operate in short-circuit mode, using low-input-impedance preamplifiers for current-to-voltage conversion [10] – [14]. These preamplifiers dominate noise performance, limit bandwidth, and increase power usage. Achieving high time resolution and detection accuracy is essential for ROICs handling fast and low-energy charge signals. However, optimizing these parameters often conflicts with the goal of

minimizing power consumption, as noted in [5], [15]. While energy-efficient ROICs excel at reducing power dissipation, their detection accuracy tends to degrade, particularly under high-input-flux conditions, as discussed in [16]. This underscores the need for innovative readout frontends that strike a balance between high time resolution, detection accuracy, and acceptable power consumption in low-energy particle detection.

This paper presents a high-precision, high-time-resolution ROIC that operates the PIN detector in open-circuit mode, using the detector itself for charge-to-voltage conversion. By eliminating the preamplifier, this architecture significantly improves power efficiency. Instead, a high-input-impedance comparator is directly connected to the detector, as shown in Fig. 1(b). The trade-off lies in the increased performance requirements of the comparator and the need for periodic reset, due to the intrinsic memory effect of the detector (C_D retains the voltage signal until reset). However, this memory also enables power savings, as the comparator activates only once per time frame—sufficient since only one event is expected per frame.

II. ROIC Architecture

The proposed ROIC block diagram is shown in Fig. 2. The comparator's inverting input connects to the detector and reset switch S_1. The detector is modeled as a pulsed current source I_S in parallel with a capacitance C_D ranging from 30 fF to 50 fF. Input charges Q_{in} between 140 aC and 200 aC are generated by 1.8 ns-wide pulses. To mitigate charge injection from S_1 and comparator kickback noise, the non-inverting input is symmetrically connected to a second reset switch S_2 and a programmable dummy capacitor C_{dummy}.

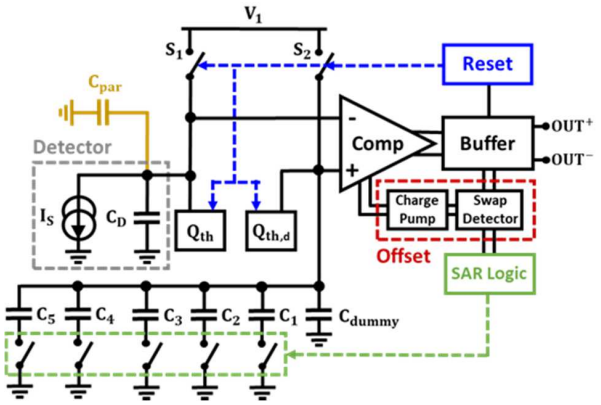

Fig. 2. Block diagram of the proposed readout frontend for detectors operating in the open-circuit (voltage-output) mode.

The comparison of the input signal with a reference signal is done in charge domain using the detector's junction capacitance C_D. Figure 3 depicts the circuit pre-charging the detector with a reference charge of opposite polarity. Both the threshold and the detector charge signals are converted to voltage by C_D ensuring a consistent threshold-to-signal ratio, independent of variations in C_D. Capacitor C_{dec} is implemented by a MOS capacitor (MOSCAP) due to its accuracy at a fixed applied voltage.

The charge generation network generates a reference charge $Q_{th} = V_{step} \times C_{dec}$, if $C_{dec} \ll C_D$. The V_{step} is generated through a capacitive divider, enabling precise step size adjustments by tuning V_{step2}. During the reset phase, switches S_1 and S_3 bias Cdec to a fixed voltage. When the threshold generation is enabled, after the reset phase, V_{step} is raised according to the ratio C_{step1}/C_{step2}, thereby adding the threshold charge Q_{th} to C_D. The implemented threshold generator achieves an average standard deviation of 1.4% and exhibits a temperature dependency of 270 ppm/°C.

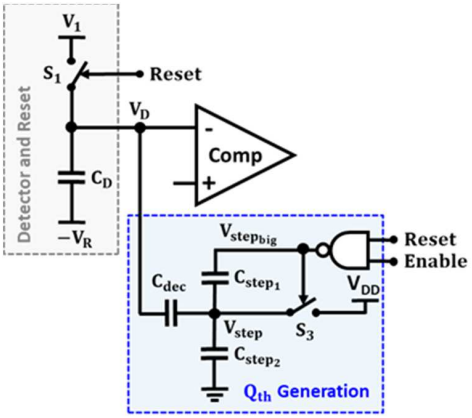

Fig. 3. The charge generation network.

A dynamic matching mechanism is employed to closely match C_{dummy} to C_D. It includes a replica of the threshold circuit ($Q_{th,d}$) in parallel with C_{dummy}, consisting of a 16 fF static capacitor and programmable elements from 2 fF to 16 fF. During matching, a fixed charge is applied to both C_D (plus the parasitics C_{par}) and the C_{dummy} network. A comparator detects the voltage difference, while SAR logic iteratively tunes C_{dummy} until balance is achieved. This calibration runs during the startup phase of the readout frontend and completes within 350 ns.

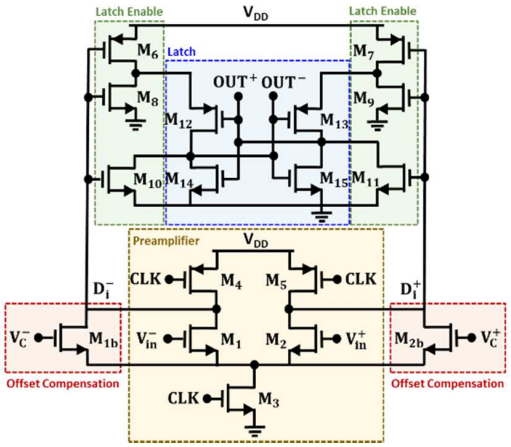

Fig. 4. Schematic of the high-speed, power-efficient dynamic comparator based on Miyahara's design [17], operating at 800 MHz.

Figure 4 illustrates the schematic of the high-speed, power-efficient dynamic comparator based on Miyahara's design [17], operating at 800 MHz. The input transistors' size and biasing point are optimized to meet noise requirements. A two-sided active offset compensation mechanism is employed, which incorporates auxiliary input pairs (M_{1b} and M_{2b}) and storage capacitors (C_C^+ and C_C^-). Two charge pumps dynamically adjust the voltage across C_C^+ and C_C^- based on the comparator output status, reducing the step size each time the output polarity swaps, as illustrated in Fig. 5. The residual offset after the compensation is 172 µV.

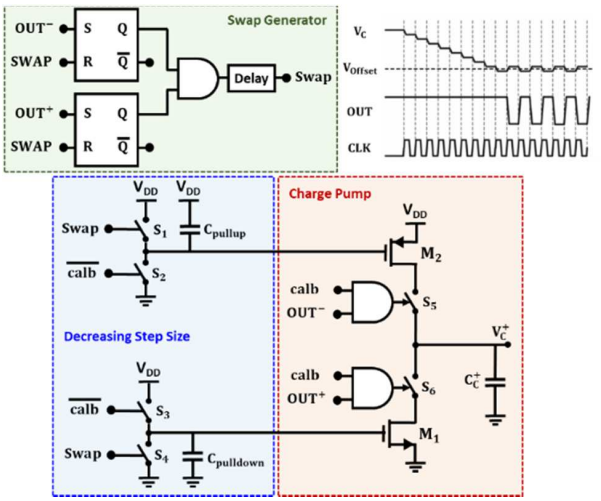

Fig. 5. Dynamically amplitude adjustable charge pump for offset compensation. Signal 'clab' activates the offset compensation.

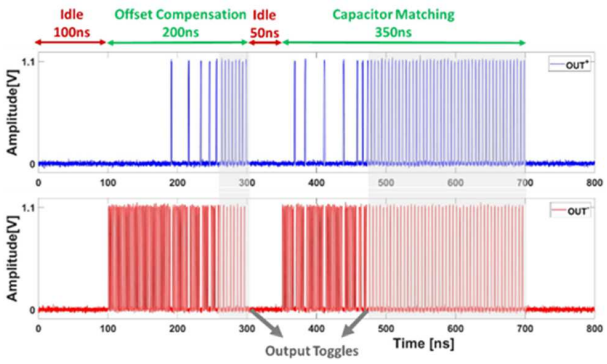

Fig. 6. Illustration of the output signals of the comparator during the offset compensation and the capacitor matching phases.

The offset compensation is completed within a 200 ns time frame and must be repeated every 1ms to maintain accuracy. During the offset compensation phase, the readout frontend is temporarily disengaged from the detector, resulting in a periodic deadtime that is directly tied to the detection accuracy. However, in specific SEM applications, periodic intermediate breaks in the scanning process can be strategically utilized for the offset compensation [3], thereby enhancing performance without sacrificing detection precision. Figure 6 illustrates the output signals of the comparator during the offset compensation and the capacitor matching phases.

III. Experimental Results

Fig. 7 shows the micrograph of the chip. The readout frontend error rate was evaluated with 10^8 Poisson-distributed input events over 10^{10} time frames, excluding the offset compensation periods. Figure 8 shows the average and 3-sigma error rates for $Q_{in} = 160$ aC and $C_D = 30$ fF at 20^oC, after repeating the test 100 times. The optimal performance at $Q_{th} = 88$ aC with a 3-sigma error rate of 1.72 ppm. Fig. 9 highlights the dependency of the detection error rate on temperature, revealing significant increases at extreme ends of Q_{th}. This behavior is attributed to elevated leakage currents at higher temperatures, which introduce additional noise charges comparable to the signal and threshold charges.

Figures 10 and 11 present the 3-sigma error rates as functions of Q_{th} across various Q_{in} and C_D values, demonstrating the high precision and robustness in performance. The power consumption is 200 µW per pixel.

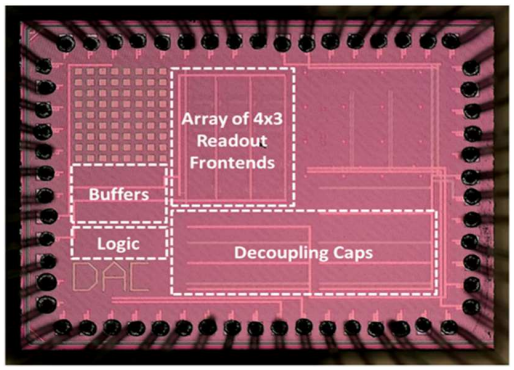

Fig. 7. Chip micrograph.

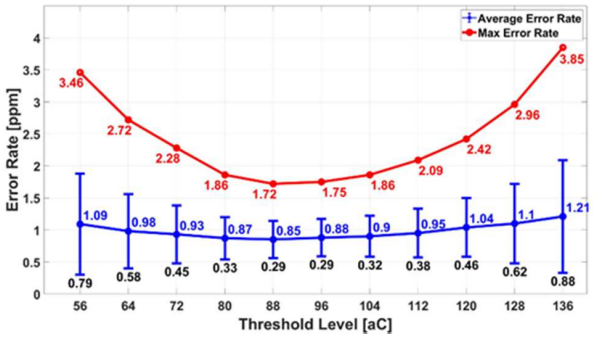

Fig. 8. Average error rate along with the corresponding standard deviation and the 3-sigma error rate as a function of the threshold level for Q_{in} = 160 aC at 20^oC.

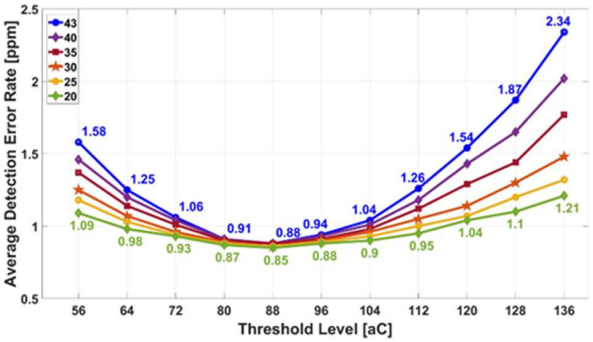

Fig. 9. Average error rate as a function of the threshold level for Q_{in} = 160 aC in a temperature range of 20^oC to 43^oC.

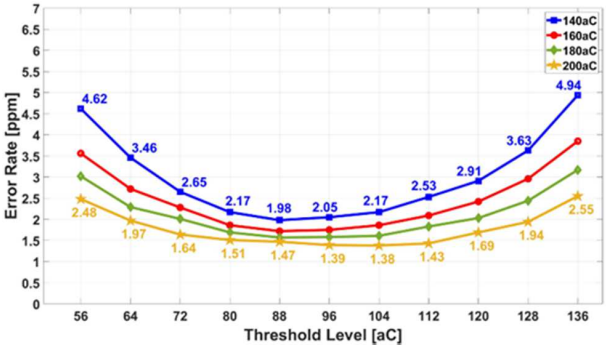

Fig. 10. The 3-sigma error rate as a function of the threshold level for various detector charge signals from Q_{in} = 140 aC to Q_{in} = 200 aC at 20^oC.

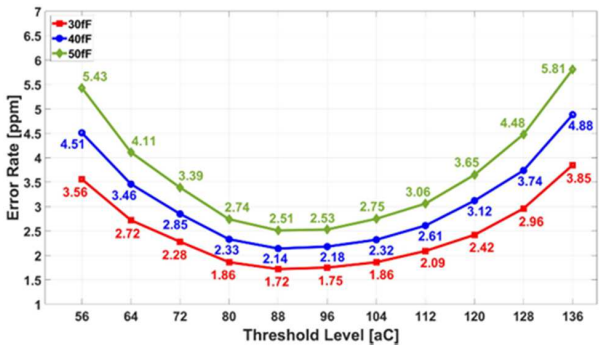

Fig. 11. The 3-sigma error rate as a function of the threshold level for a fixed input charge signal of $Q_{in} = 160$ aC , with C_D values from 30 fF to 50 fF.

Table I presents and compares the key parameters of the state-of-the-art ROICs in similar applications with a focus on their effectiveness in detecting fast and low-energy charge signals. The noise performance of each frontend is quantified using the Equivalent Noise Charge (ENC) metric, which measures noise levels in units of electron charge, ensuring consistency across different architectures. To facilitate a fair and comprehensive comparison of the readout frontends, a figure of merit (FOM) is introduced. The FOM is defined as the product of the ENC, time resolution, and power consumption, providing an aggregate performance measure. A lower FOM value indicates superior performance, representing an optimal balance of noise, timing precision, and energy efficiency.

The presented design is the first experimentally validated architecture tailored for detectors operating in the open-circuit (voltage-output) mode. It offers exceptional time resolution, high precision, and efficient power consumption, setting a new benchmark for SEM readout frontends.

TABLE I. COMPARISON OF THE STATE-OF-THE-ART CHARGE DETECTION ROICS WITH THE PROPOSED SOLUTION

	TCASII 2023 [10]	TCASI 2023 [11]	JSSC 2018 [12]	TNS 2018 [13]	TNS 2024 [14]	This Work
Process [nm]	40	130	40	110	65	**40**
Pixel Area [µm²]	50×50	75×75	100×100	75×75	35×35	**150×100**
Input Charge [aC]	65.5 – 133	380	350	140 – 720	160 – 360	**140 – 200**
ENC [e^-_{rms}]	188	44	212	89 – 150	20	**27**
Time Resolution [ns]	34	1666	81	100	10000	**2.5**
Power/Pixel [µW]	26	42	45	8 – 55	180	**200**
Pileup Correction	Yes	Yes	No	Yes	No	**Yes**
#Threshold Bins	1 – 3	2	1	2	2	**1**
FOM [e^-_{rms} × µs × µW]	166.2	3078.7	772.7	71.2 – 825	36000	**13.5**

IV. CONCLUSIONS

This work presents the design and characterization of a high-precision, energy-efficient ROIC tailored to a pixelated PIN detector for SEM applications. This paper proposed a novel high-precision, high-time-resolution ROIC that leverages the PIN detector itself for charge-to-voltage conversion, operating it in open-circuit mode. This approach significantly enhances power efficiency through a direct connection of the high-input-impedance precision comparator to the detector.

The architecture integrates dynamic offset compensation, programmable threshold generation, and high-speed charge-domain processing to achieve a time resolution of 2.5 ns while maintaining a detection error rate below 6 ppm. It has an ENC of 27 electrons and a power consumption of 200 µW per pixel. The error rate analysis highlights the impact of temperature variations, revealing the need for precise control of leakage currents to maintain low detection errors at elevated temperatures. Comparative benchmarking against state-of-the-art charge detection ROICs underscores the superior performance of the proposed design, achieving the lowest reported figure of merit among similar solutions.

REFERENCES

[1] J. I. Goldstein, D. E. Newbury, J. R. Michael, N. W. M. Ritchie, J. H. J. Scott, and D. C. Joy, Scanning Electron Microscopy and X-Ray Microanalysis. New York, NY: Springer New York, 2018.

[2] A. J. Schwartz, M. Kumar, B. L. Adams, and D. P. Field, Eds., Electron Backscatter Diffraction in Materials Science. Boston, MA: Springer US, 2009.

[3] Y. Wang, Z. Dong, R.-L. Lai, and K. Kanai, "Semiconductor charged particle detector for microscopy," WO2019233991A1, Dec. 12, 2019.

[4] H. Spieler, Semiconductor Detector Systems. Oxford University Press, 2005.

[5] M. Nakhostin, "Pulses from Ionization Detectors," in Signal Processing for Radiation Detectors, New York: John Wiley & Sons, 2017.

[6] L. Bouman, "High-Speed Readout Circuit for PIN Single Electron Detector in Voltage Mode," M.S. thesis, Dept. Microelectronics, TU Delft, Delft, the Netherlands, 2023.

[7] M. Al Disi, A. Mohammad Zaki, Q. Fan, and S. Nihtianov, "High-Count Rate, Low Power and Low Noise Single Electron Readout ASIC in 65nm CMOS Technology," in 2021 XXX International Scientific Conference Electronics (ET), Sozopol, Bulgaria, Sep. 2021, pp. 1–5.

[8] A. Mohammad Zaki and S. Nihtianov, "High Time Resolution, Low-Noise, Power-Efficient, Charge-Sensitive Amplifier in 40 nm Technology," in 2022 XXXI International Scientific Conference Electronics (ET), Sozopol, Bulgaria, Sep. 2022, pp. 1–6.

[9] A. Mohammad Zaki and S. Nihtianov, "Experimental Qualification of a Low-Noise Charge-Sensitive ROIC with Very High Time Resolution," in 2023 IEEE 32nd International Symposium on Industrial Electronics (ISIE), Helsinki, Finland, Jun. 2023, pp. 1–6.

[10] P. Grybos et al., "SPHIRD–Single Photon Counting Pixel Readout ASIC With Pulse Pile-Up Compensation Methods," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 70, no. 9, pp. 3248–3252, Sep. 2023.

[11] R. Kleczek, P. Kmon, P. Maj, R. Szczygiel, M. Zoladz, and P. Grybos, "Single Photon Counting Readout IC With 44 e− rms ENC and 5.5 e− rms Offset Spread With Charge Sensitive Amplifier Active Feedback Discharge," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 70, no. 5, pp. 1882–1892, May 2023.

[12] R. Kleczek, P. Grybos, R. Szczygiel and P. Maj, "Single Photon-Counting Pixel Readout Chip Operating Up to 1.2 Gcps/mm2 for Digital X-Ray Imaging Systems," in IEEE Journal of Solid-State Circuits, vol. 53, no. 9, pp. 2651-2662, Sept. 2018.

[13] M. Bochenek et al., "IBEX: Versatile Readout ASIC With Spectral Imaging Capability and High Count Rate Capability," IEEE Transactions on Nuclear Science, vol. 65, no. 6, pp. 1285–1291, Jun. 2018.

[14] E. Fabbrica et al., "MIRA: A Low-Noise ASIC With 35-µm Pixel Pitch for the Readout of Microchannel Plates," IEEE Transactions on Nuclear Science, vol. 71, no. 6, pp. 1339–1347, Jun. 2024.

[15] A. Rivetti, CMOS: Front-End Electronics for Radiation Sensors. Boca Raton: CRC Press, 2018.

[16] R. Ballabriga et al., "Review of hybrid pixel detector readout ASICs for spectroscopic X-ray imaging," Journal of Instrumentation, vol. 11, Jan. 2016.

[17] M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, "A low-noise self-calibrating dynamic comparator for high-speed ADCs," in 2008 IEEE Asian Solid-State Circuits Conference, Nov. 2008, pp. 269–272.