A 23.8–30.4-GHz Vector-Modulated Phase Shifter With Two-Stage Current-Reused Variable-Gain Amplifiers Achieving 0.23° Minimum RMS Phase Error

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A 23.8–30.4-GHz Vector-Modulated Phase Shifter With Two-Stage Current-Reused Variable-Gain Amplifiers Achieving 0.23° Minimum RMS Phase Error

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***Abstract*—This letter presents a millimeter-wave (mm-wave) vector-modulated phase shifter (VMPS) for phased-array applications. To improve the phase-shift accuracy without drastically increasing design complexity, the proposed VMPS structure employs variable-gain amplifiers (VGAs) that offer 2× better resolution at their low-gain states compared to their high-gain states. A two-stage current-reused structure is also proposed to implement the desired VGAs with minimal layout complexity, negligible gain penalty, and no extra power. Moreover, the proposed VMPS can maintain its phase-shift accuracy even at lower voltage gains. Fabricated in 40-nm CMOS, the prototype core consumes 11 mW from a 1.1-V supply and occupies a core area of 0.19 mm^2. At 28 GHz, with a phase resolution of 0.61°, the measured RMS phase error is 0.23° at the maximum gain and remains <0.5° at 9-dB gain back-off. With a fixed set of VGA's codewords, the RMS phase error and gain variation error are, respectively, lower than 1° and 0.24-dB over a bandwidth of 23.8–30.4 GHz.**

***Index Terms*—Active phase shifter, millimeter-wave (mm-wave), phased-array systems, two-step variable gain amplifier, vector-modulator.**

I. Introduction

Phased-array transceivers are widely exploited in the emerging millimeter-wave (mm-wave) systems to improve the communication range and channel capacity. A phase shifter is one of the critical elements in those systems, as its phase resolution and accuracy directly affect the beam's directivity, steering resolution, and pointing accuracy. Compared to passive phase shifters, the vector-modulator-based active ones are more attractive due to their superior performance in terms of chip area, insertion loss, and phase accuracy. Besides, they can accurately control the signal magnitude to realize spatial interference nulling [1]. Fig. 1 shows a simplified diagram of a vector-modulated phase shifter (VMPS). It consists of a network to generate the required in-phase (I) and quadrature (Q) signals, two variable-gain amplifiers (VGAs) with weights of G_I and G_Q, and a current-domain combiner to synthesize the desired phase shift, $\theta = (180/\pi)\arctan(G_Q/G_I)$. Each VGA is usually realized by n-bit current-steering cells [2] to enable linear gain control. As a result, due to the quantization noise, the worst-case phase error of a digitally controlled VMPS may be estimated by half of its phase resolution,

$$\theta_{e,q} = (180/\pi)\arctan(1/N)/2 \approx 90/(\pi N) = 90/\left(\pi 2^n\right). \quad (1)$$

The design of a VMPS also comes with several challenges. First, as indicated in (1), $\theta_{e,q}$ can only be improved by increasing the number of VGA cells, $N = 2^n$, in the conventional VMPSs. However, at mm-wave frequencies, since this approach dramatically adds the layout complexity, the phase error related to layout mismatch or routing parasitics grows significantly, which in turn counteracts the effect of the added cells. Second, by increasing n by 1 bit, not only the number of cells is doubled, but also the area of VGA's unit cell must be largened by 2× to keep the differential nonlinearity (DNL) of the VMPS constant if the binary control is applied. As a result, the VMPS's output parasitic capacitance increases by 4×, thus lowering its voltage gain dramatically if the power consumption is kept constant. In addition, the conventional VMPS exhibits larger phase errors at lower gain states due to the reduced effective gain resolution of the VGAs. This would degrade the rejection provided by interference nulling in a phased-array system.

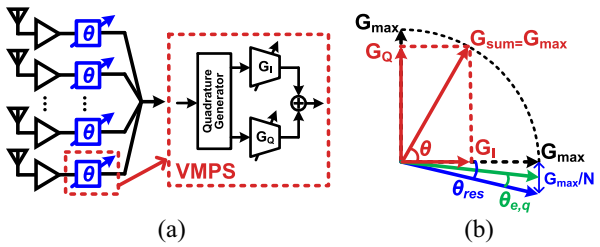

Fig. 1. (a) Block diagram. (b) Basic operation of a VMPS.

To address these issues, this letter introduces a VMPS structure using a novel two-stage current-reused VGA. With a negligible increase in the number of current-steering cells and output capacitance, the proposed VGA offers 2× better resolution at low-gain states, thus enabling the VMPS to improve its phase resolution considerably without compromising the gain and power consumption. This letter is organized as follows. Our system-level solution for improving the VMPS phase accuracy is discussed in Section II. Section III reveals and analyzes the circuit details of the proposed VMPS and VGA. The measurement results are shown in Section IV, followed by conclusions in Section V.

II. Phase Shifter System Design

To gain more insight and improve the phase-shift accuracy, the phase error of an ideal VMPS with unsigned 5-bit VGAs (i.e., each consisting of 32 unit cells) is simulated, and the corresponding results of the first quadrant are shown in Fig. 2. Given a ∼0.3 dB gain variation for different phase settings, the largest phase-shifting errors occur near 0° and 90°, where either G_I or G_Q is small. Hence, by improving the VGAs' gain resolution merely at the lower gain settings, the phase error around 0° and 90° can greatly be reduced.

Fig. 3 compares the constellation diagrams of the conventional and proposed VMPS in the first quadrant. The conventional one uses unsigned 5-bit VGAs with a gain range from 0 to 32 and a step size of one. However, the proposed VMPS employs VGAs that offer 2× better gain resolution (i.e., 0.5 instead of 1) at lower gain states (i.e., from 0 to 16). Consequently, the phase error of the

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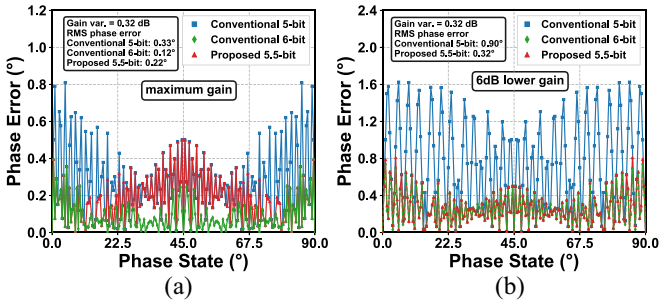

Fig. 2. Comparison between the phase error of the conventional VMPSs using unsigned 5-bit and 6-bit one-stage VGAs, and the proposed VMPS using unsigned 5.5-bit two-stage VGAs at their (a) maximum gain and (b) 6-dB lower gain.

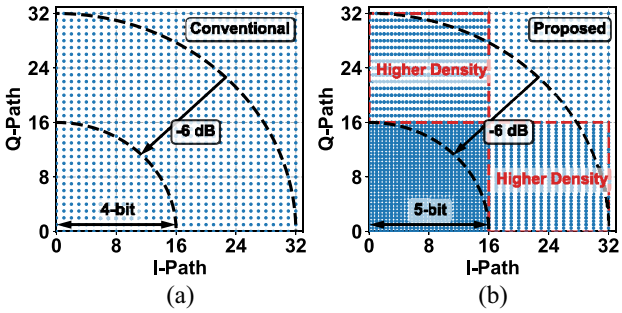

Fig. 3. First-quadrant constellation diagram of (a) conventional VMPS using unsigned 5-bit one-stage VGAs and (b) proposed VMPS using unsigned 5.5-bit two-stage VGAs.

proposed VMPS improves near 0° and 90°, as its constellation diagram shows a higher density in the vicinity of those angles. Thanks to this technique, the RMS phase error decreases from 0.33° to 0.22°, and the maximum phase error reduces to half, as shown in Fig. 2 (a). Although the phase error of the VMPS with 6-bit VGAs can be further improved, its voltage gain is lowered dramatically due to the largened output capacitance. Besides, considering the layout-related errors, the improvement of the phase-shift error would not be achieved as expected in practice.

As can be gathered from Figs. 2 (b) and 3, when the VMPS voltage gain is scaled down by 6 dB, the RMS phase error of the conventional VMPS worsens to 0.9° due to the 1-bit decrease in the effective gain resolution of the VGAs. In contrast, the proposed VMPS can maintain its phase-shift accuracy up to a 6-dB lower voltage gain since the VGA's resolution remains almost the same. The phase-shift accuracy can alternatively be maintained if an attenuator/VGA follows the conventional VMPS. However, compared with the proposed solution, it demands a larger power consumption and chip area.

Note that the abovementioned improvements could be achieved by increasing the current-steering cells to 48 instead of doubling them (i.e., using 64 cells). Nevertheless, the output capacitance still increases by ~50%, lowering the VGA's gain. Consequently, to further simplify the layout complexity and reduce gain penalty, the next section introduces a *two-stage* VGA structure that realizes the desired characteristics using only 36 current-steering cells. Among these cells, four are placed in the first stage and the rest in the second one, resembling the conventional 5-bit VGA. Thus, the increase of the output capacitance is negligible, and the gain will not be degraded.

III. Phase Shifter Circuit Design

The block diagram of the proposed mm-wave phase shifter is shown in Fig. 4. A quadrature all-pass filter (QAF) [3] first generates the quadrature signals. The proposed two-stage current-reused phase-invariant VGAs then apply the desired gains to the I and Q signals. As the output buffer, a common-source differential amplifier is designed to drive the 50-Ω load and facilitate the measurements.

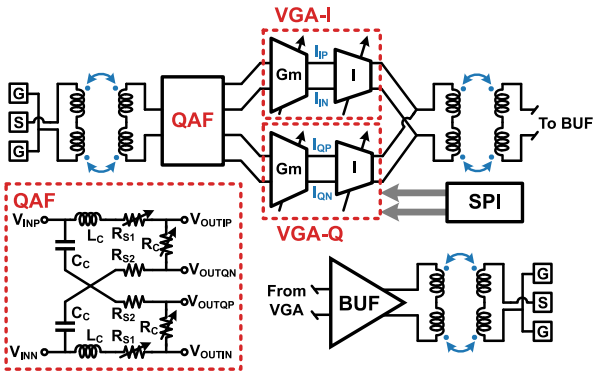

Fig. 4. Block diagram of the proposed phase shifter.

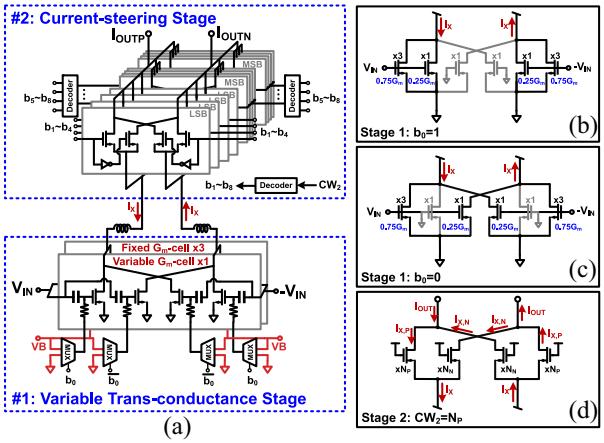

Fig. 5. (a) VGA schematic; Simplified schematics of the first stage when (b) $b_1 = 1$ and (c) $b_1 = 0$. (d) Second stage when $CW_2 = N_P$.

Compared with poly phase filters, as a second-order network [3], the QAF structure can generate quadrature signals with larger bandwidth, lower voltage loss, and smaller form factor. However, its IQ mismatch would worsen at mm-wave frequencies since the load capacitance (i.e., the parasitic capacitance of the next stage) becomes non-negligible compared to the QAF coupling capacitance (i.e., C_C in Fig. 4). To alleviate this issue, series resistors R_{S1} and R_{S2} are inserted into the L_C and C_C branches in the filter to make the QAF less sensitive to its load capacitance [3]. However, based on simulation results, the voltage gain of the QAF reduces by ~4 dB in this work. To deal with the PVT variations, the resistors R_{S1} and R_C are tunable with a range of ±10% to limit the maximum I/Q phase and magnitude mismatch to about ±° and 0.5 dB, respectively.

A. Proposed Two-Stage VGA

Fig. 5 (a) shows the schematic of the proposed current-reused two-stage phase-invariant VGA. The first stage consists of three fixed and one switchable trans-conductance (gm) cells with an identical size and a total trans-conductance gain of G_m (i.e., each cell $G_m/4$). As shown in Fig. 5 (b) and (c), according to the control bit of the first stage ($b_0 = 0$ or 1), the current of the switchable gm cell is added constructively or destructively to the current of the fixed cells. Hence, the output current of the first stage can be calculated by

$$I_X = 0.5G_m(1 + b_0) \times V_{IN} \quad (2)$$

where V_{IN} is the input voltage. According to (2), I_X can have only two different values, $0.5G_mV_{IN}$ and G_mV_{IN}.

The second stage employs a *signed* 5-bit (i.e., 2 × 32 cells in total) current-steering structure such that the entire constellation diagram and 0° to 360° phase shift can be covered by the VMPS. Each cell consists of four identical transistors that steer its differential input current to the output branches either positively (i.e., I_X to the left

branch and $-I_X$ to the right one) or negatively (i.e., I_X to the right branch and $-I_X$ to the left one). As illustrated in Fig. 5 (d), assuming that N_P and N_N cells, respectively, steer the current positively and negatively, the output current is calculated by

$$I_{OUT} = I_{X,P} - I_{X,N} = I_X\left[N_P/N - N_N/N\right] \tag{3}$$

where $N = 64$ is the total number of cells. To minimize the output phase variation over the gain states and cover larger bandwidth, the dc current and the input and output impedance of the current-steering structure should not change across all gain settings. Consequently, the total number of the ON-state (and OFF-state) transistors at each output node must be constant regardless of the gain state, leading to $N = N_P + N_N$ and simplifying (3) to

$$I_{OUT} = I_X(2CW_2/N - 1) \tag{4}$$

where CW_2 is the second stage codeword equal to N_P and can be changed from 0 to 64 with a step size of 1. Hence, I_{OUT} has 65 states from $-I_X$ to I_X with a step of $I_X/32$. By exploiting (2) and (4), the total trans-conductance gain of the proposed VGA may be estimated as

$$G_{VGA} = I_{OUT}/V_{IN} = G_m(1 + b_0)(CW_2/N - 0.5). \tag{5}$$

To gain more insight, G_{VGA} is then normalized to G_m/N

$$G_{VGA,N} = (1 + b_0) \times (CW_2 - 0.5N). \tag{6}$$

According to (6), the $G_{VGA,N}$ range is -32–32 with a step size of 0.5 and 1 when $|G_{VGA,N}|$ is 0–16 and 17–32, respectively. Therefore, by adding only one switchable gm cell in the first stage, the proposed VGA improves the gain resolution at low-gain states while keeping the number of current-steering cells in the second stage constant (i.e., using 2×32 cells instead of 2×48). This simplifies the layout complexity and reduces the input/output parasitic capacitance. Moreover, since the dc current is reused between the variable trans-conductance and current-steering stages, no extra power consumption is needed. Note that G_{VGA} is PVT sensitive as it is proportional to G_m. However, the phase shift of the VMPS is defined by $\arctan(G_Q/G_I)$. With the digitally controlled two-stage VGA structure, the ratio of G_Q to G_I of the proposed VMPS is determined by the number of the positive and negative cells in the Q and I VGAs. Hence, the VMPS phase-shift accuracy can be largely maintained over PVT variations.

The sizes of VGA's transistors are determined based on the linearity and gain requirements. Note that the VGA's transfer function should be monotonic and without any missing codes to maintain the VMPS phase accuracy and resolution. Hence, the DNL of the VGAs is considered to determine the unit cells' size. In this work, a segmented thermometer-coded technique is also exploited in the current-steering stage to optimize the tradeoff between the VGA's DNL and layout complexity. As shown in Fig. 5 (a), the 64 unit cells are divided into four least-significant-bit (LSB) cells and 15 most-significant-bit (MSB) cells to enable the segmented thermometer-coded control. Each LSB cell consists of one unit, while each MSB cell contains four units (i.e., $N_{seg} = 4$). By applying the method in [4], and considering matching constraints, the active area ($W \times L$) of each unit transistor in the current steering cells can be calculated by

$$W \times L = \frac{N_{seg}\left[A_{VTH}^2\left(g_m/I_D\right)^2 + A_\beta^2\right]}{DNL_{max}^2} \tag{7}$$

where $A_{VTH} = 3\ \text{mV} \cdot \mu\text{m}$, and $A_\beta = 0.6\%{\cdot}\mu\text{m}$ are, respectively, the threshold-voltage and current-factor proportionality parameters in the 40-nm CMOS technology. By considering $g_m/I_D = 5$ to optimize the device's maximum oscillation frequency (f_{max}) and using a minimum length transistor to reduce the output parasitic capacitance, W should be wider than 0.4 µm to achieve a maximum DNL DNL_{max} of <0.25 LSB. On the other hand, by considering the desired voltage gain and the effective load resistance of the VMPS, the required G_m and size of the gm-cells' transistors can also be estimated.

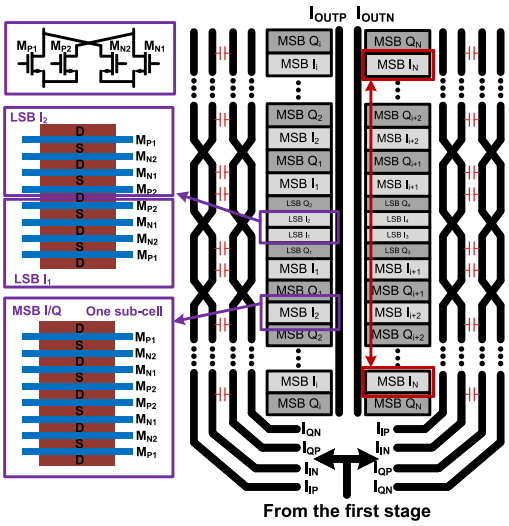

Fig. 6. Layout floor-plan of the current-steering stage.

B. Layout Design of the VGA

A conventional VMPS typically uses two physically separated I and Q VGAs. However, due to gradients in the gate-oxide thickness and substrate doping, this approach results in a severe mismatch between the I and Q VGAs, thus degrading the phase-shift accuracy. Hence, as shown in Fig. 6, the I and Q current-steering cells are interleaved in the layout to alleviate this issue. Besides, the input feeding lines of I and Q current-steering cells are twisted to balance their parasitic capacitances. This alleviates the IQ gain imbalance caused by the mismatch between the load impedances of the gm stages of the I- and Q-VGAs. Each MSB cell is also divided into two subcells and placed symmetrically (see Fig. 6) to compensate for the phase shift along the input and output lines. Finally, the four transistors within one unit cell share their source and drain areas to reduce parasitic capacitance.

IV. Implementation and Measurement

The proposed phase shifter is fabricated in 40-nm CMOS with a core area of 0.19 mm^2, as shown in Fig. 7 (a). The on-chip S-parameter measurement is done with Keysight vector network analyzer E8361A. The DC supplies and SPI control signals are wire-bonded to a printed circuit board (PCB). The core circuit of the phase shifter consumes 11 mW under a 1.1-V supply voltage in all states, and the power consumption of the output buffer is 12 mW.

Before measuring the phase states, the R_{S1} and R_C are swept, and the corresponding IQ magnitude and phase mismatch of the QAF over operating frequency band are measured and shown in Fig. 7 (b). By choosing the optimum R_{S1} and R_C settings, the calibrated IQ magnitude and phase mismatch reach below 0.5 dB and 1.2° from 22 to 31.5 GHz. Note that the selected R_{S1} and R_C settings are fixed in all the following measurements.

Fig. 7 (c) shows the measured constellation diagram of the proposed VMPS at 28 GHz, resulting from sweeping all codewords of the I and Q VGAs. As expected, it shows a higher density at <6 dB gain back-off and also in the vicinity of 0°, 90°, 180°, and 270° rotation angles. Based on the measured constellation diagram, the RMS phase error of the proposed VMPS at different gain states is reported in Fig. 7 (d). The RMS phase error is 0.23° at the maximum gain and remains <0.5° even at a 9-dB gain back-off. In contrast, the RMS phase error of a conventional VMPS degrades drastically as its gain drops. Therefore, the reduced phase error of the proposed VMPS at lower gains improves the beam nulling in phased-array systems and thus increases the interference rejection by ~9 dB, according to [5].

Fig. 7 (e) shows the measured RMS phase and gain errors versus frequency in two different scenarios. In the first case, to minimize phase error and keep the gain error <0.24 dB, the VGAs settings

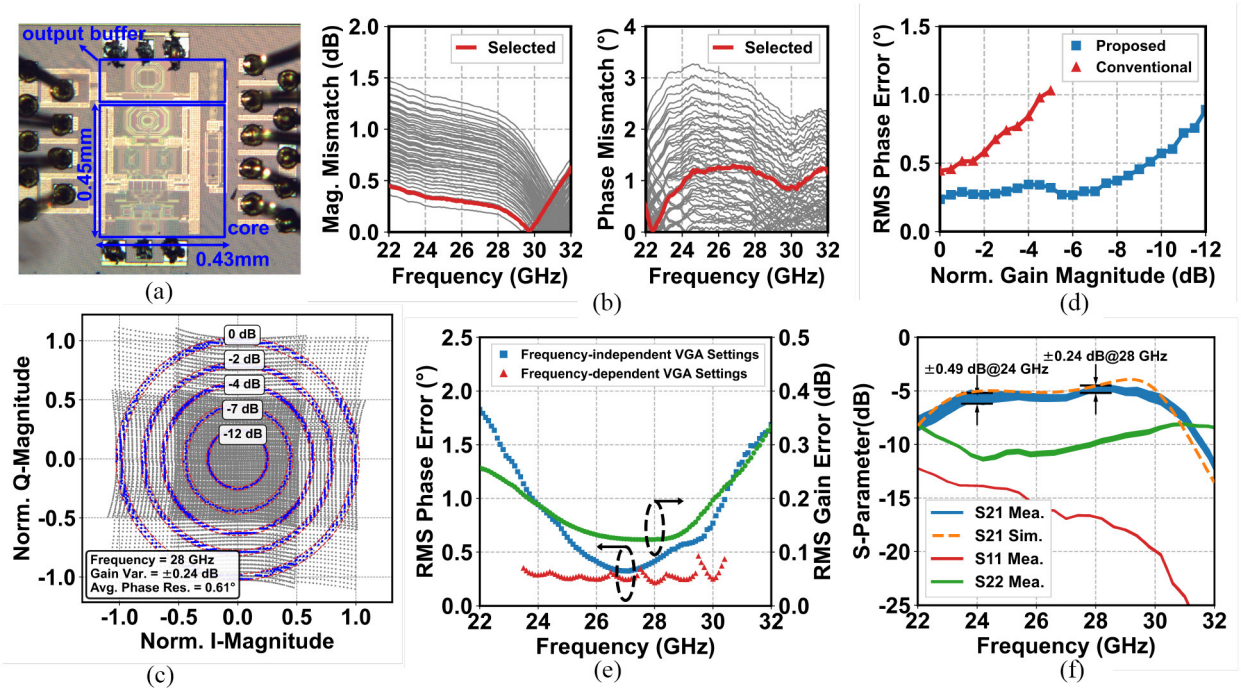

Fig. 7. (a) Chip micrograph; measured (b) IQ magnitude and phase mismatch for different R_{S1} and R_C settings. (c) Constellation diagram at 28 GHz. (d) RMS phase error versus the VMPS normalized gain. (e) RMS phase and gain errors. (f) S-parameters for all phase states.

TABLE I
COMPARISON OF STATE-OF-ART ACTIVE VMPSS

	This Work	[2] TMTT 20	[6] TCAS2 19	[7] TMTT 22	[8] TCAS2 22
Tech. (nm)	40	65	45 (SOI)	65	65
Freq. (GHz)	23.8~30.4	51~66.3	27~33	55~65	24~28
Phase res. (°)	0.61	11.25	5	11.25	5.625
RMS phase error (°)	0.23~0.5* 0.32~1	3~7	0.5~0.8	1.09	1.4
RMS gain error (dB)	0.13* 0.12~0.24	0.25~ 0.72	0.1	0.12	0.25
Gain (dB)	-4.9 (-2.3$)	-3.8	-5.8	6.2 (-7.9$)	-6.1
Core area (mm²)	0.19	0.3	0.27	0.38	0.27
P_{DC} (mW)	23 (11#)	5	25	25.2 (10.6#)	31.9
FoM_1	911 (1228$)	380.9	703.8	465.1	214.6$
FoM_2	39.6 (111$)	76.18	28.15	18.46	6.72$

* Frequency-dependent control, # excluding the buffer, $ VMPS only, simulated gain used.

$$FoM_1 = \frac{f_0(GHz) \times BW(GHz) \times Gain_{PS}(\text{lin.}) \times n_{PS}(bits)}{\theta_{error,RMS}(^\circ) \times A_{error,RMS}(\text{lin.})} \quad FoM_2 = \frac{f_0(GHz) \times BW(GHz) \times Gain_{PS}(\text{lin.}) \times n_{PS}(bits)}{\theta_{error,RMS}(^\circ) \times A_{error,RMS}(\text{lin.}) \times P_{DC}(mW)}$$

$$n_{PS}(bits) = log_2[360/\theta_{res}(^\circ)]$$

for each phase-shift state are optimized in every 1-GHz band from 23.5–30.5 GHz. The minimum and maximum RMS phase errors (red curve) are 0.23°, and 0.5° over the operational bandwidth. Then, the VGAs settings for each phase-shift state are kept fixed over the bandwidth. In this case, the RMS phase/gain errors (blue and green curves) are, respectively, lower than 1°/0.24 dB over a bandwidth of 23.8–30.4 GHz, according to which the VMPS's bandwidth is defined. The minimum RMS phase error is 0.32° at ∼27 GHz. The measured S-parameters of the corresponding 585 phase states are also shown in Fig. 7 (f). The measured peak gain of the VMPS is −4.9 dB at 28 GHz, while the simulated gains of the VMPS core and the output buffer are −2.3 and −1.5 dB, respectively. In addition, the measured input P1dB of the VMPS is 1 dBm at 28 GHz. Compared with the prior art in Table I, our work demonstrates the best phase resolution and lowest RMS phase error.

V. CONCLUSION

It is proved that the phase-shift error of a conventional VMPS is higher in the vicinity of 0° and 90° rotation angles. To tackle this issue, a VMPS structure with a two-stage current-reused VGA is introduced. With a negligible increase in the number of gm and current-steering cells, the proposed VGA offers 2× better resolution at low-gain states, thus improving the VMPS phase resolution considerably without compromising the gain and power consumption. Moreover, the proposed VMPS maintains its phase-shift accuracy even up to 9-dB gain back-off. Fabricated in 40-nm CMOS, the prototype demonstrates an RMS phase/gain error of 1°/0.24 dB over a bandwidth of 23.8–30.4 GHz while the core consumes 11 mW.

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