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DOI
10.1109/iscas.2017.8050951

Publication date
2017

Document Version
Final published version

Published in
Conference Proceedings - IEEE International Symposium on Circuits and Systems, ISCAS 2017

Chopping in Continuous-Time Sigma-Delta Modulators

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***Abstract*— This paper discusses the use of chopping in continuous-time sigma-delta modulators where 1/*f* noise and offset need to be suppressed by continuous-time methods. An intuitive analysis of the artifacts related to chopping is presented. Aliasing of quantization noise is found to be the main problem, especially for chopping frequencies lower than the modulator's sampling frequency (f_s). Correctly timed return-to-zero and switched-capacitor DACs are proposed as a solution to the aliasing problem. In both cases, the key idea is to synchronize DAC transitions with moments when the quantization noise at the input of the first integrator is low. Circuit level simulations are presented to validate the proposed techniques.**

Keywords—chopping; chopping artifacts; continuous time; sigma delta; precision ADC; 1/f noise; offset

I. INTRODUCTION

Continuous-time sigma-delta modulators (CTΣΔMs) are attractive for precision applications due to their greater energy efficiency and explicit anti-aliasing behavior compared to their discrete-time counterparts. In such applications, the offset and 1/*f* noise contributed by the modulator's first stage is critical, however, such errors cannot be efficiently mitigated by discrete-time techniques such as auto-zeroing. Chopping, which is a continuous-time technique, then becomes the only viable way to reduce such errors in CTΣΔMs.

Although chopping has been successfully implemented in instrumentation amplifiers and discrete-time ΣΔMs (DTΣΔMs) [1,2], it is known to cause undesirable artifacts when used in CTΣΔMs [3-5], namely fold-back of quantization noise to the signal band. In this work, this problem is analyzed and two solutions based on return-to-zero (RZ) and switched-capacitor (SC) DACs are proposed. Since such DACs are often used in CTΣΔMs for their superior robustness to inter-signal-interference (ISI) and jitter, respectively, the proposed solutions can be integrated into current designs without introducing significant overhead.

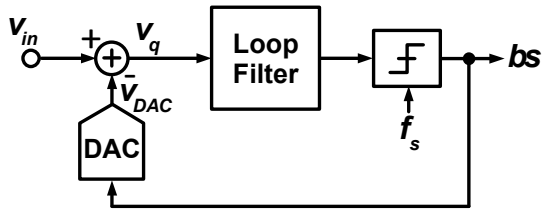

Fig. 1. Block diagram of a 1-bit CTΣΔM

This paper is organized as follows. In Section II, an analysis of chopping-related errors in CTΣΔMs is made, and previous solutions from literature are discussed. In Section III two novel chopping methods based on DAC pulse shape (return-to-zero, and exponentially decaying) are proposed. Simulation results showing the effectiveness of the proposed methods are given in Section IV. Conclusions are drawn in Section V.

II. CHOPPER STABILIZATION IN CTΣΔMS

Fig. 1 depicts the block diagram of a 1-bit CTΣΔM. The input signal v_{in} is assumed to be band-limited, and the signal bandwidth is assumed to be much lower than the sampling frequency (f_s). The DAC signal v_{DAC} is a discrete-time signal sampled at f_s with an arbitrary pulse shape. For our analysis, a rectangular (zero-order-hold) pulse shape will be assumed.

The performance degradation caused by chopping can be attributed to the parasitic sampling of quantization noise (v_q) content at the input of the loop-filter [3, 4]. If this occurs at a frequency which causes aliasing ($|f| < |f_s|$), high frequency quantization noise may fold-back into the signal band as will be explained next. Fig. 2 shows the simplified schematic of a CTΣΔM with a chopped first integrator, and a 1-bit resistive DAC, with the timing diagram. Two choppers are placed at the virtual ground and at the output of the OTA to up-modulate its offset and 1/*f* noise. In a practical OTA-RC integrator however, the virtual ground node *(a)* will have a signal swing given by:

$$v_a \cong \frac{v_q}{1 + g_m \cdot R} \tag{1}$$

where R is the value of the parallel combination of the input and DAC resistors, and g_m is the transconductance of the OTA. As shown in Fig.2, *bs* (= ±1) is the digital bit-stream. v_b is the chopped version of the v_a such that

$$v_b = v_a \cdot \Phi_{ch} \tag{2}$$

where Φ_{ch} (= ±1) is a square wave chopper state signal with a period of T_{ch} and 50% duty cycle. When Φ_{ch} changes state at its half periods (1 → -1 or 1 → -1), v_b changes its polarity, causing a current spike due to the charging of the parasitic capacitors C_{p1} at the input of the OTA (Fig. 2). This differential current i_b (= $i_{bp} - i_{bn}$) is mostly provided by the OTA via the integration caps, assuming $g_m \gg 1/R$. However, the feedback current i_a (= i_{ap} - i_{an}) is modulated again by Φ_{ch}, making it independent of Φ_{ch} edge direction. i_a is then integrated on the integration capacitors (C_{int}), resulting in a sampled input-referred error voltage v_{err} given by:

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$$v_{err}[n] = \frac{2 \cdot C_{p1} \cdot v_q[n\frac{T_{ch}}{2}]}{C_{int}(1 + g_m \cdot R)} \quad (3)$$

This means that the quantization noise is sampled at $2{\cdot}f_{ch}$. For $f_{ch} = f_s$ and $f_{ch} = f_s/2$, v_{err} is a sampled and scaled down version of v_q without any aliasing (or fold-back) [2]. However, any mismatch of the parasitic or integration capacitors will result in sampling of quantization noise also at f_{ch}. Although the mismatch-induced f_{ch} sampled error is usually orders of magnitude smaller than that sampled at $2{\cdot}f_{ch}$, for $f_{ch} = f_s/2$ it causes fold-back of quantization noise around $f_s/2$ (where it has its highest noise power) to DC and thus may significantly degrade the modulator's performance.

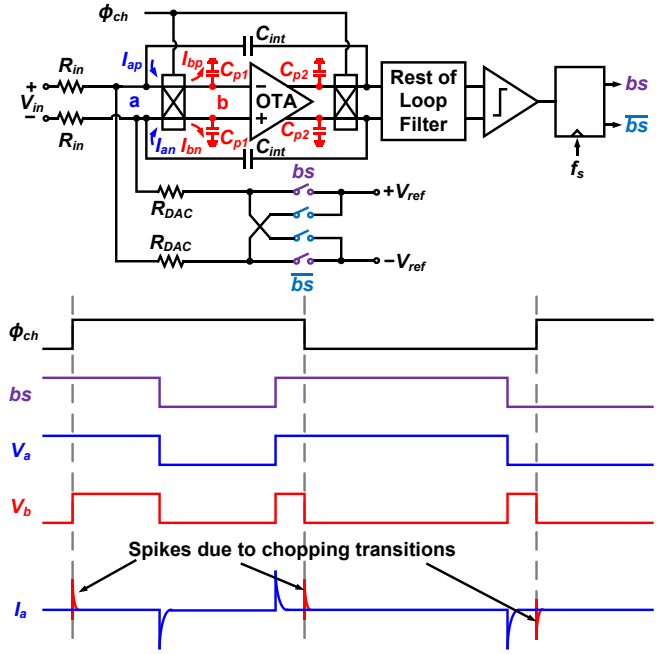

Fig. 2. A second-order CTΣΔM, with chopping with a resistive NRZ DAC.

The output parasitic capacitors C_{p2} also cause a similar sampling of the integrator output voltage. However, when the error is referred back to the input it is first-order high pass shaped. This makes the output sampling error negligible in most practical cases, provided that the integrator's DC gain is high. However, it should be noted that the switched-capacitor resistor due to the switching of C_{p2} may degrade the impedance of the OTA and reduce its DC gain.

Although chopping at f_s and its integer multiples ($f_{ch} = K{\cdot}f_s$) causes no quantization noise fold-back [2,5], there are secondary effects proportional to f_{ch} such as reduced input impedance, increased input current noise, increased offset ripple, and reduced output impedance of the OTA [4]. Thus, chopping at lower frequencies is preferable, provided that the chosen f_{ch} is above the $1/f$ corner and well within the stop-band of the digital decimation filter.

As can be seen from (1) and (3), chopping artifacts can be reduced if the swing at the virtual ground of the OTA is reduced. This can be achieved by increasing its g_m or by adding a low-impedance output stage. Both increase its power consumption, and hence reduce energy efficiency. Observing that the only fold-back prone signal is the output of the DAC (v_{DAC}), previous work has suggested the use of a finite-impulse-response (FIR) DAC to suppress quantization noise around the error-sampling-frequency $2{\cdot}f_{ch}$ [3,4]. Although this is quite effective, the FIR filter should be designed to have notches around $2{\cdot}f_{ch}$ and its harmonics, which may require a large number of taps especially for CTΣΔMs with high OSR. This results in more excess loop delay which needs to be compensated by additional loops, and an area overhead that is proportional to the number of FIR taps, and so increases design complexity. Thus, a simpler method of implementing low frequency chopping is still needed.

III. Proposed Methods

The previous analysis addresses the problem in the frequency domain, resulting in a frequency domain filtering solution. An alternative approach can be found in the time domain. For a non-return-to-zero (NRZ) DAC v_{dac} is a zero-order-held version of *bs*. In practice, the DAC shape can be chosen arbitrarily as far as the total error feedback charge integrated on C_{int} is kept the same over T_s. If the DAC pulse shape includes a *bs-free* time window, the sampled error can be reduced if the chopping transition occurs during this time window. The same observation holds for DAC pulse shapes which decay to zero. We propose to use a RZ or SC DAC in the modulator's feedback loop so as to have a *bs-free* or a *reduced-bs* time window for the chopping transitions, respectively. This approach can be extended to other DAC pulse shapes with similar properties.

A. Chopping with RZ-DAC

As shown in Fig. 3, when Φ_{RZ} is low, the DAC is connected to the virtual ground of the OTA and the DAC output current is proportional to *bs*. When Φ_{RZ} is high, the DAC is in its RZ phase and its output is zero. This indicates that during the RZ phase no quantization noise from the DAC will appear at the virtual ground node of the OTA. In this case, the virtual ground node signal will be given by:

$$v_a \cong \begin{cases} \dfrac{v_q}{1 + g_m \cdot R}, & \Phi_{RZ} = 0 \\ \dfrac{v_{in}}{1 + g_m \cdot R}, & \Phi_{RZ} = 1 \end{cases} \quad (4)$$

As it is clear from (4), if Φ_{ch} changes its state during RZ phase ($\Phi_{RZ} = 1$) i_a and i_b would be only v_{in} dependent. Thus, the sampled error caused by chopping transitions will not contain the *bs* related part (v_{dac}). Hence, Signal-to-Quantization-Noise Ratio(SQNR) will not be degraded by the aliased quantization noise.

Since RZ-DACs are often used in CTΣΔMs to avoid inter-symbol interference (ISI) due to the finite rise and fall times of its output signal, the proposed method will not increase the complexity for the most designs. Moreover, it allows the modulator's first integrator to be chopped at frequencies much lower than the sampling frequency. In this way, the input current and noise associated with the charge injection of the chopper switches can be reduced. Furthermore, the degradation of the first OTA's gain due to the loading of the switching parasitic capacitors at the output (C_{p2}) will be less pronounced.

In turn, this not only helps to suppress the offset and $1/f$ noise of the following stages of the loop filter, but also improves the CTΣΔM's SQNR performance.

B. Chopping with SC-DAC

SC-DACs are commonly used in CTΣΔM to reduce their jitter sensitivity while also reducing ISI [6]. Chopping artifacts can also be reduced by selecting the right chopping moment as shown in Fig. 4. The DAC capacitor C_{DAC} is charged to $\pm v_{ref}$ during Φ_{SMP} and its polarity is determined by bs. During Φ_{DAC} the sampled charge is integrated on C_{int}. The virtual ground voltage during this phase has a decaying shape.

$$v_a \cong \begin{cases} \dfrac{v_{in}}{1+g_m \cdot R} - \dfrac{v_{ref} \cdot g_m}{g_m \cdot R_{dac}+1} e^{-\frac{t}{\tau}} & , \phi_{DAC} = 1 \\ \dfrac{v_{in}}{1+g_m \cdot R} & , \phi_{SMP} = 1 \end{cases} \quad (5)$$

where R_{DAC} is the series resistance of the DAC, τ is the SC DAC settling time constant given by

$$\tau = \frac{(g_m \cdot R_{dac}+1) \cdot \left(\dfrac{C_{int} \cdot C_{DAC}}{C_{int}+C_{DAC}}\right)}{g_m} \quad (6)$$

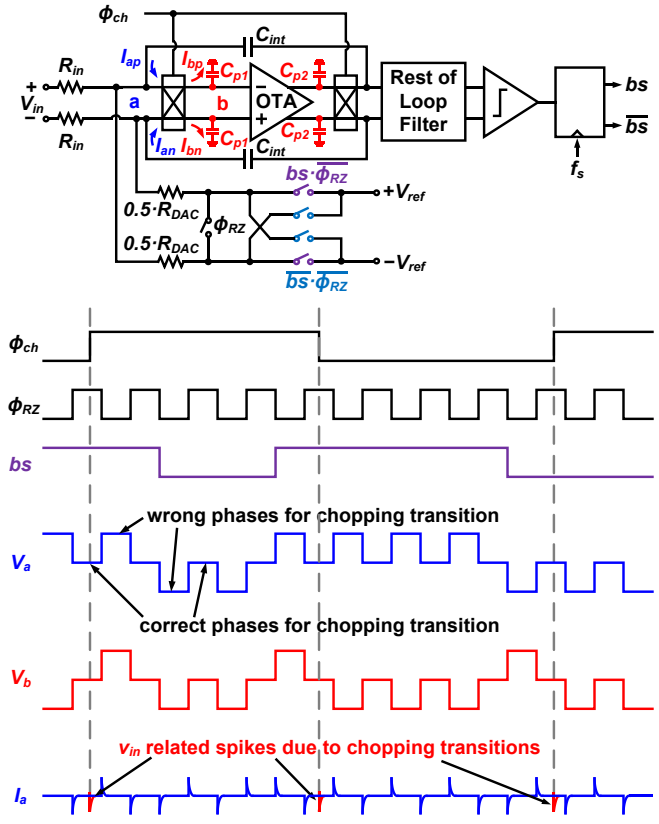

Fig. 3. A second-order CTΣΔM, with chopping with a resistive RZ DAC.

It is evident from (5) that a SC-DAC offers a time window for chopping transition moments, such as during the whole of Φ_{SMP} or at the end of Φ_{DAC} when the bs related virtual ground components have decayed. The attenuation of the bs components depends on the ratio $0.5 \cdot T_s/\tau$, which is typically very high for a CTΣΔM.

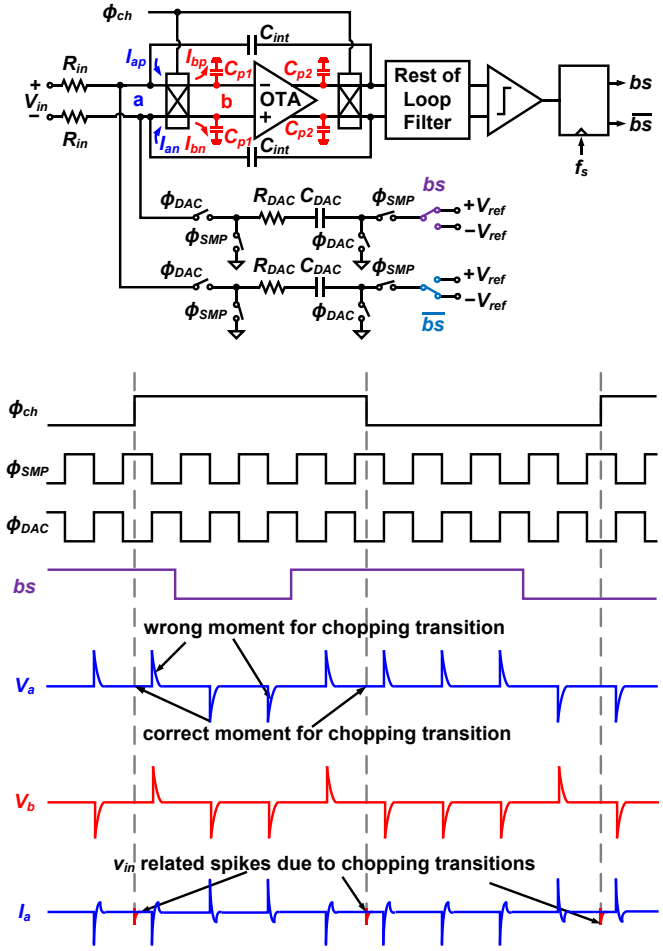

Fig. 4. A second-order CTΣΔM, with chopping with an SC DAC.

IV. Simulation Results

To further verify the effectiveness of the proposed techniques, two second-order feed-forward CTΣΔMs have been implemented, one with a resistive RZ-DAC and one with a SC-DAC. The input signal frequency is 500 Hz, the sampling frequency is 2 MHz, and C_{int} is 35 pF for both CTΣΔMs. The OTA in the first integrator has 80 dB DC gain and 1 mS transconductance. The virtual ground parasitic C_{p1} is 1 pF and the output parasitic C_{p2} is 100 fF.

When chopped at 20kHz, a comparison of the output spectra of the modulator with the RZ-DAC is shown in Fig. 5 for the correct and incorrect chopping phases, i.e. at $\Phi_{RZ} = 1$ and $\Phi_{RZ} = 0$ respectively. Chopping during the $\Phi_{RZ} = 0$ phase significantly increases the noise floor due to quantization noise fold-back. This is similar to what occurs in NRZ-DACs. Chopping during the $\Phi_{RZ} = 1$ phase, however, practically eliminates the effect of quantization noise fold-back.

For further validation, 3 mV offset and 100 fF parasitic capacitance (C_{p1}) mismatch were added to the OTA used in the first integrator. The offset is converted to ripple at $2 \cdot f_{ch}$, and the ripple power is proportional to the f_{ch} [1]. In order to show the SQNR degradation due to high frequency chopping f_{ch} =

$f_s/100$ = 20 kHz, and $f_{ch} = f_s$ = 2 MHz are chosen with RZ chopping. As shown in Fig. 6, the low-frequency noise PSD for f_{ch} = 2 MHz is worse than for f_{ch} = 20 kHz, even when chopping at Φ_{RZ}. The residual offset also improves by 40dB for f_{ch} = 20 kHz, due to the reduced chopper ripple.

Fig. 7 shows the output spectra for the CTΣΔM with the SC-DAC when it is chopped at the correct and at the wrong moments indicated in Fig. 3. Although the output of a SC-DAC decays exponentially, the initial amplitude of the *bs*-related virtual ground signal will be larger than that of a RZ-DAC. Thus, the sampled quantization noise power is dependent on the exact chopping moment. As a result, the simulated PSD corresponding to the wrong chopping moment (Fig. 7) has a higher noise floor than that obtained with a RZ-DAC (Fig. 5).

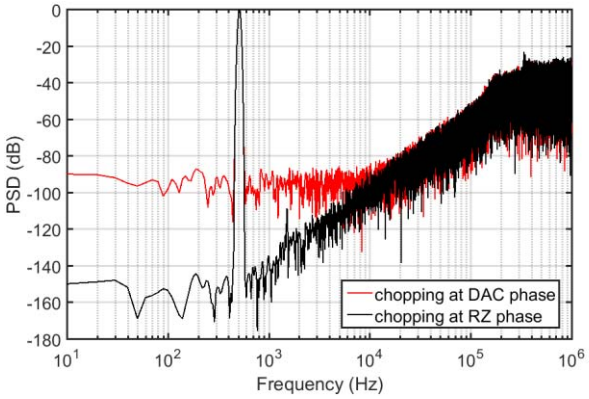

Fig. 5. Bitstream spectrum of a second-order CTΣΔM with resistive RZ DAC, with chopping at DAC phase (red) at first integrator, and with chopping at RZ phase (black) at first integrator. (2×10^5 samples, Kaiser window.)

V. Conclusion

This paper describes the theory and implementation problems associated with the use of chopping to reduce offset and 1/*f* noise in CTΣΔMs. It is shown that chopping can significantly degrade the noise floor of such modulators due to the aliasing of high-frequency quantization noise.

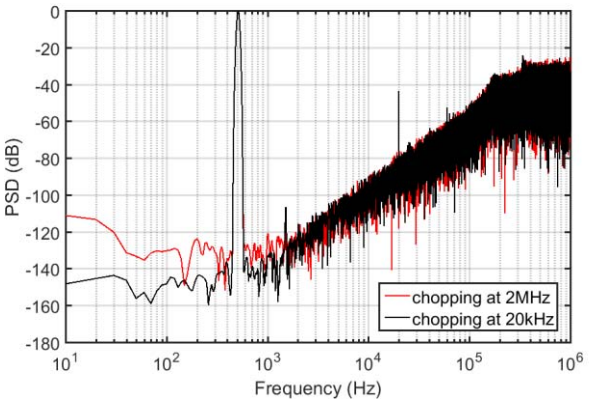

Fig. 6. Bitstream spectrum of a second-order CTΣΔM with resistive RZ DAC, with 2MHz chopping frequency (red) at first integrator, and with 20kHz chopping frequency (black) at first integrator. (2×10^5 samples, Kaiser window.)

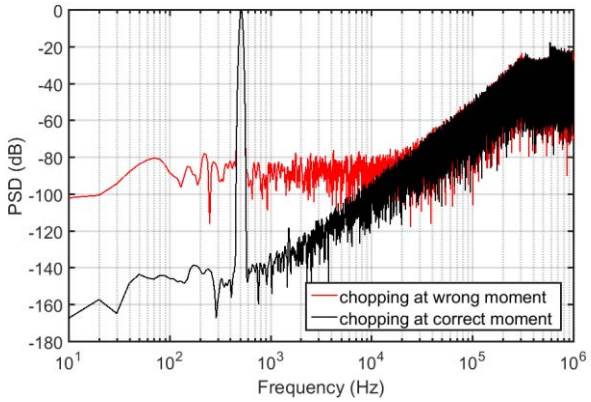

Fig. 7. Bitstream spectrum of a second-order CTΣΔM with SC DAC, with chopping at the wrong moment (red) at first integrator, and with chopping at the right moment (black) at first integrator. (2×10^5 samples, Kaiser window.)

In this work, two methods are proposed to mitigate quantization-noise aliasing for modulator's with RZ-DAC and SC-DACs. Both are based on the DAC pulse shape and the choice of appropriate chopping moments. Analysis and simulations show that these techniques can almost completely eliminate quantization noise fold-back. The proposed methods thus allow the chopping frequency to be flexibly chosen. This is especially valuable in the design of high OSR 1-bit CTΣΔMs where low-frequency chopping is desired to avoid the increased offset and input current associated with high-frequency chopping, e.g. the traditional technique of chopping at the sampling frequency. The proposed methods can be further extended to any DAC shape that exhibits moments when it is zero, open, or decaying.

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