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DOI
10.1109/ISCAS56072.2025.11043648

Publication date
2025

Document Version
Final published version

Published in
Proceedings of the 2025 IEEE International Symposium on Circuits and Systems (ISCAS)

An SSHI Rectifier with Energy-Investing Technique for Piezoelectric Energy Harvesting

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2025 IEEE International Symposium on Circuits and Systems (ISCAS) | 979-8-3503-5683-0/25/$31.00 ©2025 IEEE | DOI: 10.1109/ISCAS56072.2025.11043648

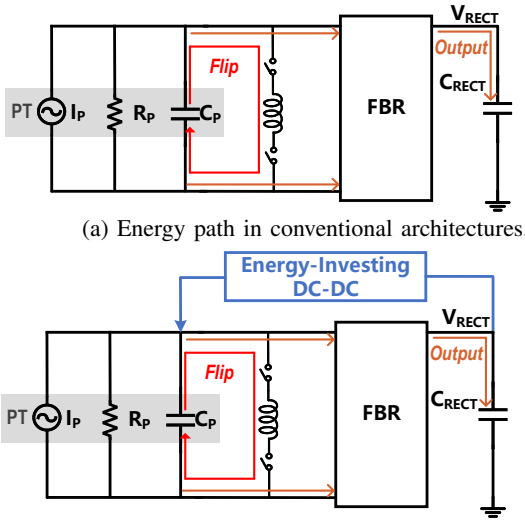
***Abstract*—With the rapid development of the Internet of Things (IoT), piezoelectric energy harvesting has emerged as a highly promising power solution for autonomous IoT devices. To increase the extracted energy from the harvesters, various rectifiers have been developed. Bias-flip rectifiers, one of the most widely used rectifiers, utilize extra components to periodically flip the voltage across the harvester to achieve higher output power. This work proposes a bias-flip rectifier with an energy investment technique to boost the total harvesting power. By optimizing the energy invested from the load to the harvester and the loading conditions, the circuit can achieve higher FoM compared to conventional SSHI rectifiers under the same configurations. The proposed circuit was designed in a 180-nm BCD process, the simulation results show a $5.97\,\mathrm{X}$ energy enhancement compared to a full bridge rectifier (FBR) and a $1.2\,\mathrm{X}$ enhancement compared to conventional synchronized switch harvesting on inductor (SSHI) rectifiers.**

***Index Terms*—Energy harvesting, piezoelectric transducer, energy investment, bias-flip rectifiers, DC-DC.**

I. Introduction

With the dramatically rising number of Internet of Things (IoT) devices, the demand for low-power sensor networks and self-powered systems is increasing. Piezoelectric energy harvesting (PEH) converts ambient kinetic energy into electrical energy, providing a fully sustainable power solution for edge IoT devices without using batteries.

A piezoelectric transducer (PT) can be modeled as an AC current source I_P in parallel with a capacitor C_P and resistor R_P when it is excited at resonance [1]. To rectify AC energy, many passive architectures are developed [2–4]. However, a significant amount of charge is wasted in charging and discharging the C_P, severely limiting the output power performance. To address this issue, many active architectures have been developed, among which the bias-flip, or synchronized switch harvesting on inductor (SSHI), rectifiers synchronously flip the polarity of the charge on C_P [1, 5–8]. These rectifiers greatly increase the extracted energy from the mechanical domain and have superior power improvement compared to other extraction techniques [9–11]. As shown in Fig. 1a, the energy-transferring path in a conventional SSHI rectifier consists of the flipping path and output path, and no energy is transferred from the load back to the harvester. However, the output power is highly related to the output voltage and the output charge. This characteristic implies that a small energy investment from the load to the PT can push the load voltage higher and increase the amount of output charge, eventually leading to a net output power promotion. Previous energy-investing works implement one-time collection, unable to take advantage of the bias-flip rectifier's high extraction efficiency to achieve better performance [10, 12].



(a) Energy path in conventional architectures.

(b) Energy path in proposed architectures.

Fig. 1: Energy path analysis.

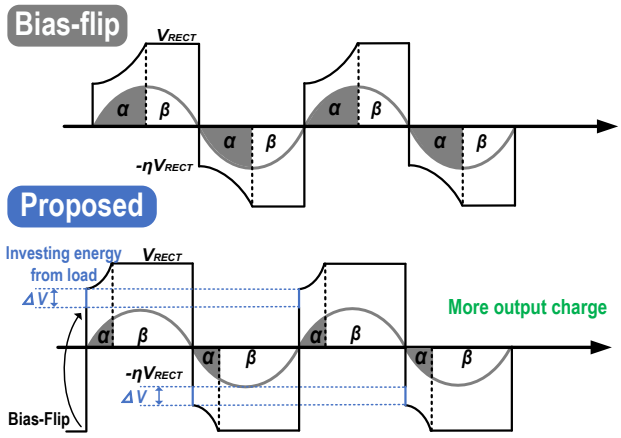
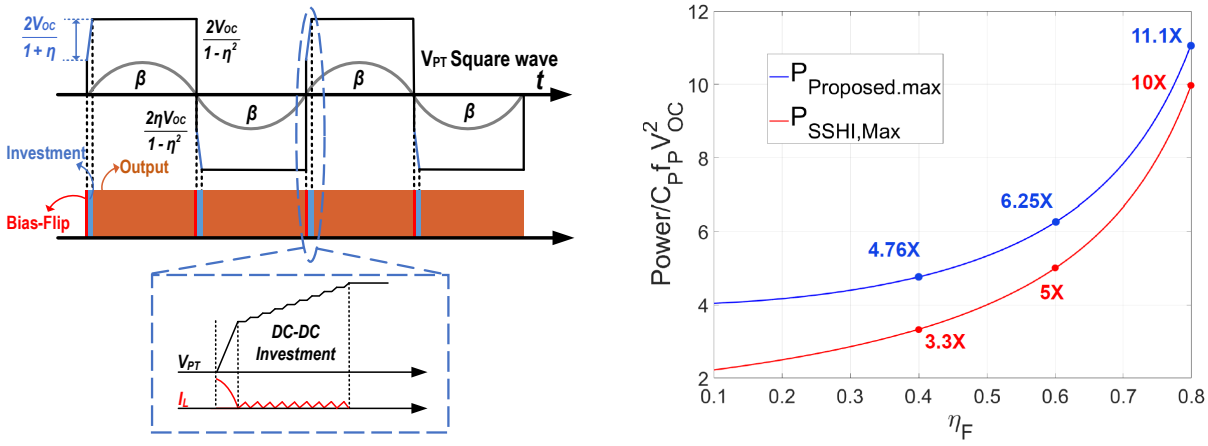


Fig. 2: Waveform of conventional and proposed rectifiers.

In this work, a bias-flip rectifier with an energy-investing technique is proposed, illustrated in Fig. 1b. The proposed circuit will be displayed and analyzed in section II. The simulation results and the conclusion are shown in section III and IV, respectively.



(a) Waveform under the optimum working state.

(b) Theoretical Output power under different flipping efficiency.

Fig. 3: Theoretical optimum investing point and improvement power.

II. Proposed Bias-Flip with Investment Rectifier

The waveform of a conventional bias-flip circuit and the proposed bias-flip with energy investment (BFEI) rectifier are shown in Fig. 2. Conventionally, the V_{PT} are built up during phase α and output energy during β. When the current I_P crosses zero, the voltage is flipped. In the proposed circuit, some energy from the load C_{RECT} is invested in boosting V_{PT} by ΔV after the bias-flip, then it builds up in α and remains during phase β. The detailed analysis will be given as follows.

A. Optimized investment analysis

For a conventional bias-flip rectifier, the output power can be expressed as:

$$P_{SSHI} = 2C_P V_{RECT} f_P (2V_{OC} - V_{RECT}(1-\eta_F)) \tag{1}$$

where f_P is the vibration frequency, V_{OC} is the PT open-circuit voltage amplitude, V_{RECT} is the output voltage, and η_F is the voltage-flipping efficiency. The peak power is:

$$P_{BF,Max} = \frac{2C_P f_P V_{OC}^2}{1-\eta_F} \quad (\text{when } V_{OC} = \frac{V_{OC}}{1-\eta_F}) \tag{2}$$

For the proposed circuit, setting the invested voltage as ΔV, the charge extracted from I_P during phase α is $aC_P V_{OC}$, the charge during phase β is $bC_P V_{OC}$. The related equation can be expressed as:

$$Q_{Total,\frac{T}{2}} = aC_P V_{OC} + bC_P V_{OC} = 2C_P V_{OC} \tag{3}$$

Considering a relative stable V_{RECT}, it's related to both ΔV and a:

$$V_{RECT}\eta_F + \Delta V + aV_{OC} = V_{RECT} \tag{4}$$

$$V_{RECT} = \frac{\Delta V + aV_{OC}}{1-\eta_F} \tag{5}$$

The output power can be expressed as:

$$P_{Out} = 2f_P V_{OUT} Q_{OUT} = 2f_P V_{RECT} bC_P V_{OC} \tag{6}$$

Considering the investment loss from the load:

$$P_{Loss} = f_P C_P ((V_{RECT}\eta_F + \Delta V)^2 - (V_{RECT}\eta_F)^2) \tag{7}$$

The boosted power P_{Gain} can be expressed as:

$$P_{Gain} = P_{Out} - P_{Loss} - P_{SSHI,Max} \tag{8}$$

To obtain the optimum investment point:

$$\frac{\partial P_{Gain}}{\partial \Delta V} = 0, \Delta V = V_{OC}(\frac{2}{1+\eta} - a) \tag{9}$$

$$\frac{\partial P_{Gain}}{\partial a} = 0, a = 0 \tag{10}$$

Therefore, for a given circuit with fixed f_P, C_P, V_{OC}, and η_F, the maximum net gain power can be achieved when all the charge is used for output, and V_{PT} becomes close to a square wave shown in Fig. 3a. Optimum V_{RECT} and output power can be expressed as:

$$V_{Opt} = \frac{2V_{OC}}{1-\eta_F^2} \tag{11}$$

$$P_{Opt} = \frac{4C_P f_P V_{OC}^2}{1-\eta_F^2} = \frac{2}{1+\eta_F} P_{SSHI,Max} \tag{12}$$

The simulated output power of the proposed circuit is illustrated in Fig. 3b. The proposed circuit can always achieve higher output power compared to a conventional SSHI rectifier.

B. Power stage operation

Fig. 4 shows the 3-phase operations. During the output phase, the DC-DC module is not activated, and a negative voltage converter (NVC) with an active diode limits V_{PT} to V_{RECT}. The circuit enters the bias-flip phase when the current I_P crosses zero, and the switches S_{BF} are closed to flip the V_{PT}. After the bias-flipping, the DC-DC conversion is activated in the investment phase to transfer energy from C_{RECT} to C_P in two sub-phases. These two sub-phases repeat until V_{PT} reaches V_{RECT}. After that, the system immediately enters again the output phase.

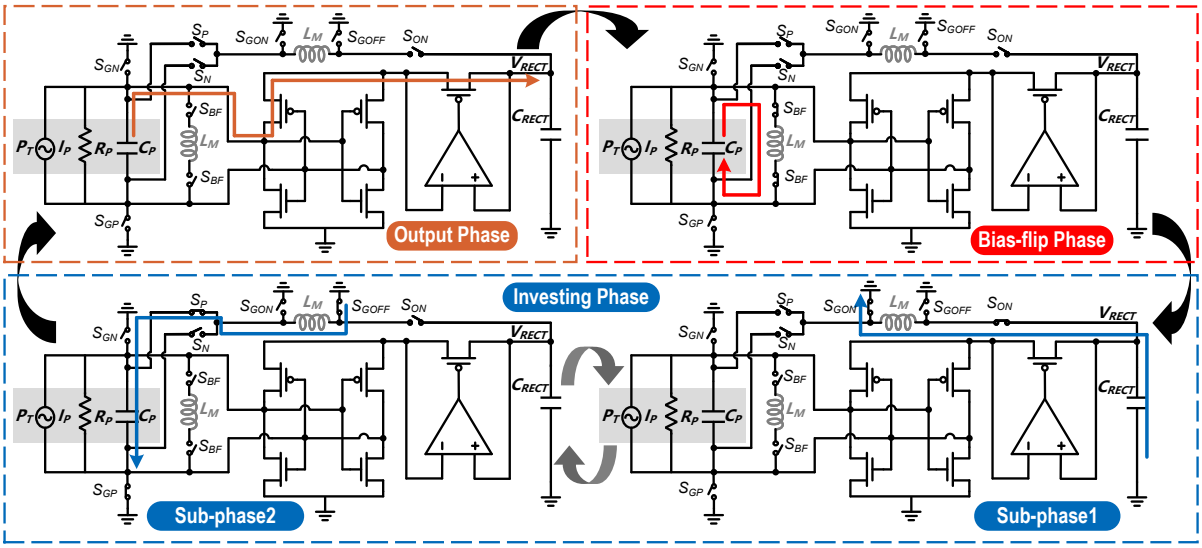


Fig. 4: Power stage operation of the proposed circuit.

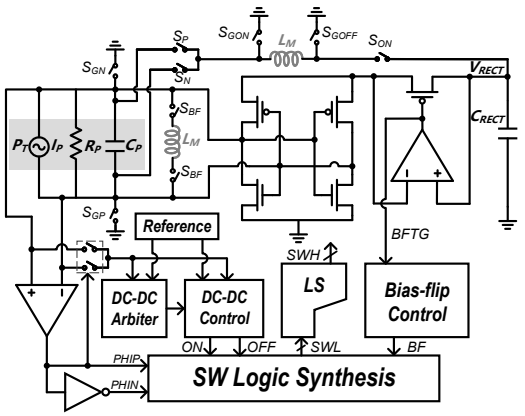


Fig. 5: Architecture of the proposed circuit

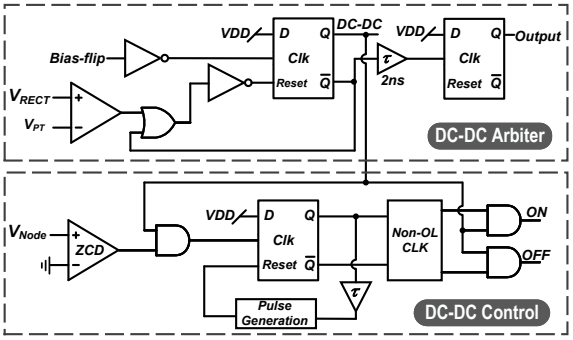


Fig. 6: Diagram of the DC-DC block.

C. System architecture

Fig. 5 shows the architecture of the proposed circuit. Only the inductor L_M and output capacitor C_{RECT} are off-chip components. A comparator is connected across C_P to detect the V_{PT} polarity. Signals $PHIP$ and $PHIN$ are generated

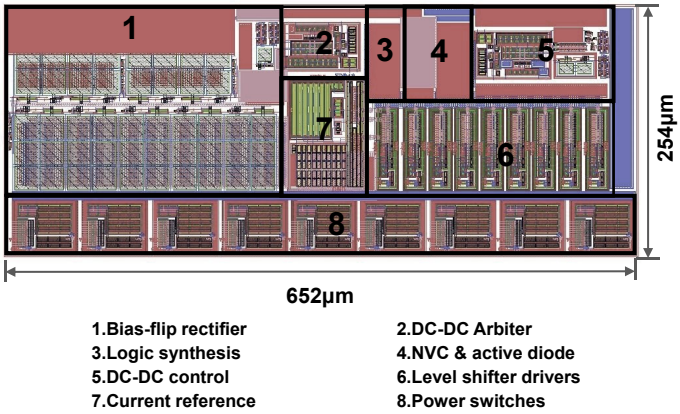
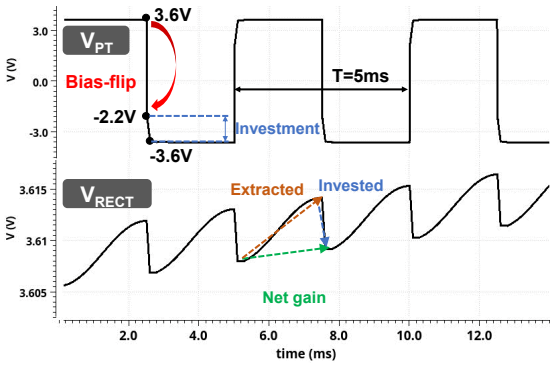


Fig. 7: Circuit layout.

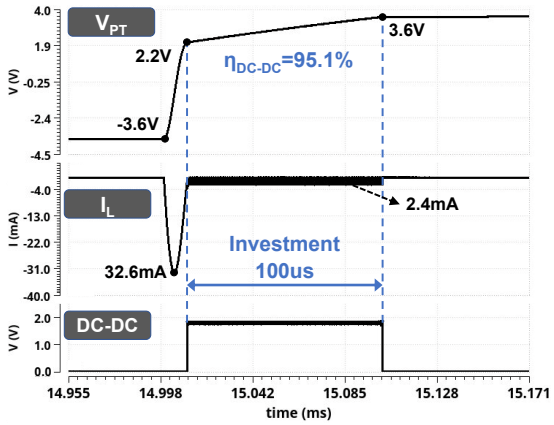
to control the switch. The switch tracks the value of V_{PT}, which is then sent to the DC-DC arbiter block, determining when the energy investment should be activated. Then the DC-DC Control block controls the investment process. The driving signal of the active diode is used to trigger the Bias-flip Control block. Finally, all the signals are synthesized in the SW Logic Synthesis module to produce driving signals, which go through level shifters (LSs) and switch drivers to drive power switches.

D. DC-DC implementation

As shown in Fig. 6, the DC-DC module consists of DC-DC Arbiter and DC-DC control blocks. In the DC-DC Arbiter, a comparator compares V_{PT} and V_{RECT} to determine the length of the investment phase. In the logic part, signals of the output phase and investing phase are produced. The DC-DC signal is utilized to trigger the first sub-phase, whose length T_{ON} relies on the setting of the delay cell. The second sub-phase starts after the first sub-phase and ends with the signal from the zero-current detection (ZCD) comparator, resulting in a boundary conduction mode (BCM) DC-DC operation.



(a) Waveform of the SSHI with investment.



(b) Zoom-in waveform of investment.

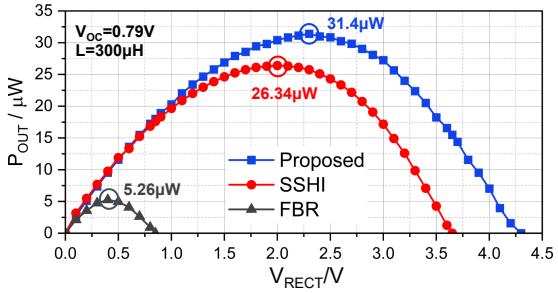
Fig. 8: Working waveform of the circuit

III. Simulation Results

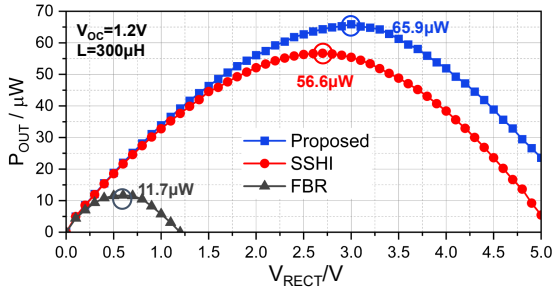
The proposed rectifier was designed with a 180-nm BCD process with an active chip area of $0.166\,\mathrm{mm}^2$. The layout is shown in Fig. 7. Except for the inductor, all the control blocks and power switches are designed on-chip.

Fig. 8a shows the waveform of the V_{PT} and V_{RECT}. The PT vibration frequency is $200\,\mathrm{Hz}$ and the C_P is $40\,\mathrm{nF}$. The V_{PT} is periodically flipped and invested from the V_{RECT}. In the bottom part, The V_{RECT} experiences a drop and a rise every half-cycle due to the investment loss and output charge. Hence, the net gain is the real harvesting energy. The zoom-in figure of the investment process is shown in Fig. 8b With a 95.1% DC-DC conversion efficiency during the investment phase, the V_{PT} is charged from $2.2\,\mathrm{V}$ to $3.6\,\mathrm{V}$ within $100\,\mu\mathrm{s}$, during which the charge from I_P can be neglected because the investment phase time is negligible compared to vibration period as well as the small current amplitude around the zero-current moment. The peak current on the inductor is $32.6\,\mathrm{mA}$ and $2.4\,\mathrm{mA}$ during bias-flip and investment, respectively, under the given situation.

Fig. 9 shows the output power curve when the V_{OC} is $0.79\,\mathrm{V}$ and $1.2\,\mathrm{V}$, respectively. A higher peak output power can be achieved by adding the investment phase. In Fig. 9a, the proposed circuit archives a $31.4\,\mu\mathrm{w}$ output power with a 597% improvement compared to the FBR rectifier and a 120% boost



(a) Output power with different load condition under a $0.79\,\mathrm{V}$ V_{OC}.



(b) Output power with different load condition under a $1.2\,\mathrm{V}$ V_{OC}.

Fig. 9: Simulating output power under different V_{OC}

TABLE I: Comparison table with prior arts.

Parameters	**This work**	JSSC'10[1]	JSSC'14[10]	ISSCC'16[5]	ISSCC'23[8]
Rectifier Type	**BFEI**	SSHI	EI	SSHI	SSHI
Technology	**180nm**	N/R	350nm	350nm	180nm
Piezoelectric capacitance	**40nF**	18nF	15nF	26/20/9nF	42nF
Resonant Frequency	**200Hz**	225Hz	143Hz	134.6-229.2Hz	230Hz
Off Chip Component	**300μH (L)**	820μH (L)	330μH (L)	3.3mH (L)	N/R
η_F	**0.6**	*0.5	N/R	0.89	0.82
Power Improvement	**597%(Investment) 500%(SSHI)**	*400%	360%	681%	738%
$P_{Proposed}/P_{BF}$	**1.2**	1	N/R	1	1

N/R : Not Reported * : Estimated

compared to the SSHI circuit. In Fig. 9b, the proposed circuit archives a $65.9\,\mu\mathrm{w}$ output power with a 563% improvement compared to the FBR rectifier and a 116% boost compared to the SSHI circuit. The power boost ratio is slightly decreased with a higher V_{OC} due to the higher DC-DC loss.

TABLE. I compares the proposed BFEI rectifier with state-of-the-art works. This work achieves a high energy extraction enhancement by employing a small inductor. Most importantly, the investment technique achieves an output power boost compared to bias-flip rectifiers.

IV. Conclusion

A bias-flip with energy investment (BFEI) rectifier is proposed in this paper. The proposed circuit reaches a 597% power improvement compared to a passive full-bridge rectifier and a 120% improvement compared to a traditional SSHI circuit with the same size of inductor.

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