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Carrier-Based Modulated Model Predictive Control Strategy for Three-Phase Two-Level VSIs

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Abstract—The implementation of finite-control-set model predictive control (FCS-MPC) in voltage source inverters (VSIs) can make the system suffer from poor current harmonics performance, which may complicate the design of the required AC filter. To overcome this shortcoming, a carrier-based modulated model predictive control (CB-MMPC) strategy is proposed in this paper. This method enables the utilization of existing PWM modulation techniques with FCS-MPC, where a modulation waveform with zero-sequence signal injection is generated and compared to a triangular carrier wave, while optimizing the selection of the switching states. As it is shown, the studied CB-MMPC strategy not only considerably improves the current total harmonic distortion (THD) but also attains the performance of fast current dynamic response and robustness as the traditional FCS-MPC. Herein, the detailed implementation of the CB-MMPC control strategy is given, while considering its application to the current feedback control loop of a three-phase three-wire two-level VSI modulated at constant switching frequency. Finally, PLECS circuit simulation and a 3-kW VSI prototype are used to verify the superiority and the effectiveness of the presented CB-MMPC strategy. This is also benchmarked to the FCS-MPC and dead-beat based controllers.

Index Terms—Finite-control-set model predictive control (FCS-MPC), carrier-based modulated MPC (CB-MMPC), pulse width modulation (PWM), voltage source inverters (VSIs).

I. INTRODUCTION

THREE-PHASE two-level voltage source inverters (VSIs) have been widely used in many industrial applications such as traction of electric vehicles, grid-tied photovoltaic systems, and other renewable energy generations [1], [2]. In recent years, with the development of high performance microprocessors [3],

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the finite-control-set model predictive control (FCS-MPC) has gained attention. FCS-MPC utilizes the analytical model of the system to predict its future behavior over a time horizon. This control technique applied to the current control of a VSI provides exciting features such as easy implementation and fast dynamic response without the necessity of designing the controlling parameters of an alternative linear control logic such as the ones used in a proportional-integral (PI) or proportional-resonator (PR)-controllers [4]. However, since FCS-MPC utilizes only one switching state for the whole sampling interval, the controller will generate an output waveform with a variable switching frequency, which can negatively affect the voltage/current waveform harmonic spectrum generated by the VSI, making the design of harmonic filters more challenging [5]. Moreover, though a shorter sampling period will improve the waveform quality, it is still a challenge for the commercially available micro-controller unit (MCU) to achieve an ultra-high sampling frequency by compressing the total required computation to an extremely short time [6].

Several advanced strategies have been proposed to address the main drawbacks of the conventional FCS-MPC and to improve the output current quality of two-level VSIs [7]–[10]. In [7], the prediction horizon of the FCS-MPC is increased to improve the control performance, however, due to the higher numbers of possible converter states required to be calculated, a larger computational time can not be avoided in the MCUs. Discrete space vector modulation (DSVM) integrated FCS-MPC is proposed in [8], [9]. This strategy can achieve a high performance of the VSI output current waveform in both static and dynamic operations, but it needs to calculate a large number of virtual voltage vectors which reduces its effectiveness due to data processing limitation of today's commercial MCUs. The modulated MPC (MMPC) studied in [10] applies multiple vectors, and it can achieve improved performance at a constant switching frequency, thereby addressing the major issue of the FCS-MPC, i.e. it mitigates the drawbacks associated to the variable frequency operation. Such a method, which combines MPC and the principle of PWM modulation strategies while retaining all the advantages of the FCS-MPC, is being a current focus of interest in MPC studies [5], [10]–[16].

Conventional MMPC adopting the space-vector modulation scheme was initially presented for a cascaded H-bridge back-to-back converter in [11], and then extended to a three-phase active rectifier in [10] and a shunt active filter in [12]. Based

on these MMPC studies, a finite-set MPC strategy with fixed switching frequency is developed in the grid-tied application [5] while the balance of the partial DC capacitor voltages is realized by utilizing the available redundant voltage vectors. According to the arm-voltage-regulating algorithm, a novel MMPC strategy especially suited for modular multilevel converters (MMC) is proposed in [13] with the aim to enhance the steady-state performance of the system under unbalanced grid conditions. In [14], the error between the measured currents and the current references is used to calculate the times of the three vectors to be used within a switching period, i.e. two active vectors and a zero vector, resulting in a zero tracking error. Considering the over-modulation region of the two-level VSI, a new MMPC with optimized over-modulation is proposed in [15] that guarantees a spectrum switching frequency in the linear modulation range and extends its optimized response to the over-modulation region. A modified MMPC technique is presented in [16] to improve the steady-state and transient performance of the conventional MMPC scheme, which determines the optimal vectors to be applied by evaluating the cost function values of all admissible voltage vectors.

Most of the aforementioned MMPC strategies are based on the space-vector modulation scheme, which needs to calculate the time lengths of the inverter switching states and then to program the voltage pulses directly after obtaining the operation time of the selected vectors. Another modulation technique for VSIs is named carrier-based implementation [17], where a modulation wave is compared with a triangular carrier wave and the intersections define the switching instants for the associated VSI bridge leg switches. The carrier- and space-vector based pulse width modulation (PWM) methods have equivalent performances [18]. Furthermore, the implementation of carrier-based modulations is simpler than the space-vector modulation approach as the involved computation burden is generally reduced. It is noted that so far very limited publications exist using the carrier-based PWM approach to realize the MMPC strategy.

To fill this gap, a new carrier-based MMPC (CB-MMPC) strategy for the three-phase three-wire two-level VSI is proposed. Different from the traditional MMPC in [5], [10], the error between the reference duty cycle and the duty cycle to be executed in the next period is applied in the cost function, and the modulation waveform is derived directly based on the pairs of switching states which minimizes the optimization loop of the cost function. Unlike the recently published carrier-based PWM methods for motor drives and grid-connected applications in [19]–[21], the main current control scheme used in this paper is based on the concept of MPC, not on the PI-controller, and thus it is not necessary to design the controlling parameters. It is noted that PI-controller is well suited for achieving zero steady-state error but often at the cost of degraded transient performances [22], [23]. Compared with the model-based dead-beat controllers (DBC) [24], [25], the proposed strategy will select the optimal vector pairs based on the cost function minimization, which will be more robust if there is a large mismatching in the circuit model parameters and in the control loop. Presented through carrier-based PWM approach [17], the CB-MMPC method can be of simple implementation with a digital signal

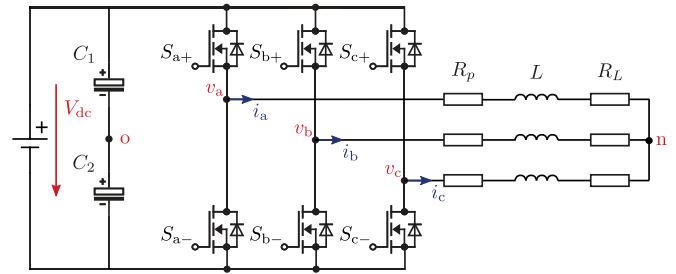


Fig. 1. Three-phase three-wire two-level VSI.

processor (DSP); meanwhile, instead of continuous PWM methods, e.g., SVPWM and SPWM, different discontinuous PWM (DPWM) methods with zero-sequence signals injection can be realized with the concept of the CB-MMPC without compromising the performance of fast current dynamic response and robustness. The contributions of this paper are listed as follows:

- 1) The idea of carrier-based PWM implementation is combined with the concept of model predictive control to realize the MMPC method.
- 2) Both the carrier-based continuous and discontinuous PWM methods are implemented.
- 3) The cost function based on the duty cycle is derived, where the error of the zero vector and zero-sequence signals injection can be introduced.
- 4) Benchmarking of classic FCS-MPC, DBC based PWM methods, and studied CB-MMPC methods are presented in experiments.

The rest of the paper is divided as follows. In Section II, the analytical model of the three-phase three-wire two-level VSI is derived. In Section III, the detailed implementations of the carrier-based PWM approach, the classic FCS-MPC, and the DBC based PWM method are given. In Section IV, the principle of the CB-MMPC method is illustrated in detail, where the CB-MMPC SVPWM and CB-MMPC DPWM1 are selected as examples. Finally, in Section IV, a PLECS simulation and a 3-kW VSI prototype are used to verify the superiority and the effectiveness of the presented CB-MMPC strategy in comparison with the traditional FCS-MPC and DBC PWM based methods.

II. MODELING OF TWO-LEVEL VSIS

A three-phase three-wire two-level VSI circuit is shown in Fig. 1. The basic converter is composed of 6 active switches, two series-connected DC capacitors C_1 and C_2 , and a Y-connected three-phase $R - L$ load. Note that in Fig. 1, i_a , i_b and i_c represent the output currents of the inverter, while v_a , v_b and v_c are the converter phase voltages; L refers to the value of the inductor and R_p is the equivalent parasitic resistance of the inductor; and R_L is the value of the series resistor modeling the active power of the load. The switching states and the corresponding converter terminal voltages are summarized in Table I. Assuming that each capacitor voltage is equal to half of the DC-link voltage, then these three switching states ($x = a, b, c$) generate an output terminal voltage of $v_{x0} \in \{-V_{dc}/2, V_{dc}/2\}$, i.e. voltage of terminal $x = a, b, c$ with respect to the terminal o as shown in

TABLE I
 SWITCHING STATES ($x = a, b, c$)

Switching State	Converter output	Gate signal
S_x	v_{xo}	(S_{x+}, S_{x-})
1	$V_{dc}/2$	(1,0)
0	$-V_{dc}/2$	(0,1)

Fig. 1. According to the current flow direction in Fig. 1, the current dynamics can be represented in the α - β coordinates as:

$$\begin{cases} L \frac{di_\alpha}{dt} = v_\alpha - R_p i_\alpha - R_L i_\alpha = v_\alpha - R_p i_\alpha - v_{\alpha L} \\ L \frac{di_\beta}{dt} = v_\beta - R_p i_\beta - R_L i_\beta = v_\beta - R_p i_\beta - v_{\beta L} \end{cases} \quad (1)$$

where $v_{\alpha L} = R_L i_\alpha$ and $v_{\beta L} = R_L i_\beta$ represent the α - β coordinates of the voltage across the load, and in a grid-connected application, e.g. in a photovoltaic inverter, it could represent the grid voltage or the voltage measured across the capacitor of a multi-order harmonic filter, i.e. LCL filter. In the reminder of this paper a resistive load will be considered for simplification purpose so $v_{\alpha L}$ and $v_{\beta L}$ are calculated directly from the modeled load R_L and i_α and i_β , however all the analysis can be extended to grid-connected application by using the $v_{\alpha L}$ and $v_{\beta L}$ as measured quantities in the control loop computations.

In order to be implemented in a digital controller, the model of the inverter must be defined in a discrete-time domain [4]. The derivative of the AC line currents in the continuous-time model can be approximated based on the forward Euler for the approximation sampling period of T_s as:

$$\begin{cases} \frac{di_\alpha}{dt} \approx \frac{i_\alpha(k+1) - i_\alpha(k)}{T_s} \\ \frac{di_\beta}{dt} \approx \frac{i_\beta(k+1) - i_\beta(k)}{T_s} \end{cases} \quad (2)$$

Accordingly, the expression (1) can be re-written as:

$$\begin{cases} i_\alpha(k+1) = \frac{L - R_p T_s}{L} i_\alpha(k) + \frac{T_s}{L} (v_\alpha(k) - v_{\alpha L}(k)) \\ i_\beta(k+1) = \frac{L - R_p T_s}{L} i_\beta(k) + \frac{T_s}{L} (v_\beta(k) - v_{\beta L}(k)) \end{cases} \quad (3)$$

III. STATE OF THE ART

A. Carrier-Based PWM Approach

For the three-wire VSI depicted in Fig. 1 the carrier-based PWM approach provides the freedom in the choice of the zero-sequence signal [17]. Firstly, the zero-sequence signals are obtained based on the original modulation signals v_a^* , v_b^* , v_c^* . Secondly, the carrier waves of the different phases are used to generate the PWM pulse. The generalized block diagram of the carrier-based PWM approach with zero-sequence signal injection principle is illustrated in Fig. 2. The modulation waveforms of SVPWM and the DPWM1 are shown in Fig. 3. The zero-sequence signal of the SVPWM is generated by (4), where the reference signal with the lowest magnitude is defined as v_j^* . For example, if $|v_a^*| \leq |v_b^*| \leq |v_c^*|$, then $v_0 = 0.5v_a^*$. For DPWM1, the zero-sequence signal is given in (5), where the phase signal which has the largest in magnitude is defined as v_j^* . For example, if $|v_a^*| \geq |v_b^*| \geq |v_c^*|$, then $v_0 = \text{sign}(v_a^*)V_{dc}/2 - v_a^*$. More details regarding the zero sequence component of the modulation

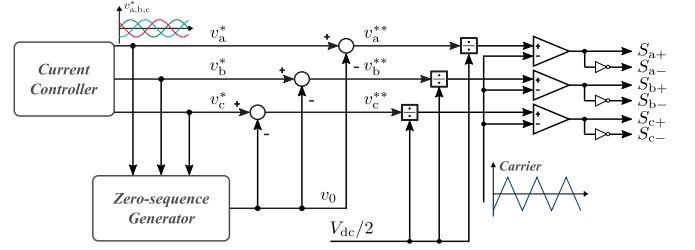


Fig. 2. Block diagram of the carrier-based PWM modulator.

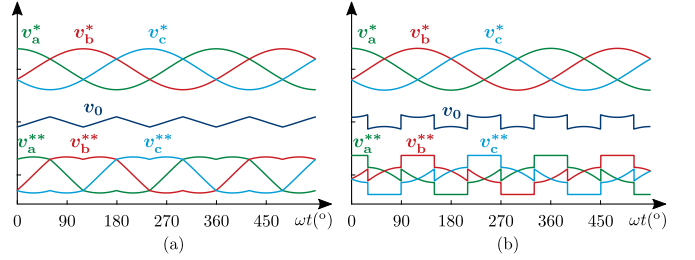


Fig. 3. Modulation waveforms of (a) SVPWM, (b) DPWM1.

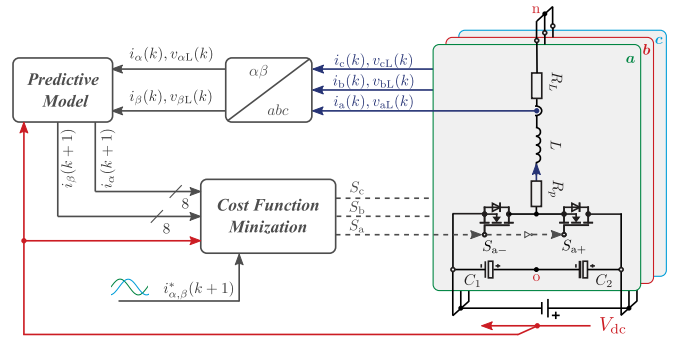


Fig. 4. Block diagram of the conventional FCS-MPC.

waveforms can be found in [26].

$$v_0 = 0.5v_j^* \quad i \in \{a, b, c\} \quad (4)$$

$$v_0 = \text{sign}(v_j^*) \cdot V_{dc}/2 - v_j^* \quad j \in \{a, b, c\} \quad (5)$$

B. Finite-Control-Set Model Predictive Control or FCS-MPC

The feedback current control based on the FCS-MPC technique is known for utilizing only a finite number of possible switching states that can be generated by the power converter during the optimization routines. This method can predict well the behavior of the modeled system variables and specific performance indexes for each analyzed switching state [3]. Herein, each current $i_{\alpha,\beta}$ prediction is evaluated with respect to its references $i_{\alpha,\beta}^*$ in a cost function, and the switching state S_a , S_b , and S_c , that generates the minimum deviation value is selected to be applied in the next sampling period.

The block diagram of this control strategy for the three-phase three-wire two-level VSI is shown in Fig. 4. The main control objective is the regulation of the AC line currents in the α - β coordinates, i.e. $i_{\alpha,\beta}$. The FCS-MPC method uses the

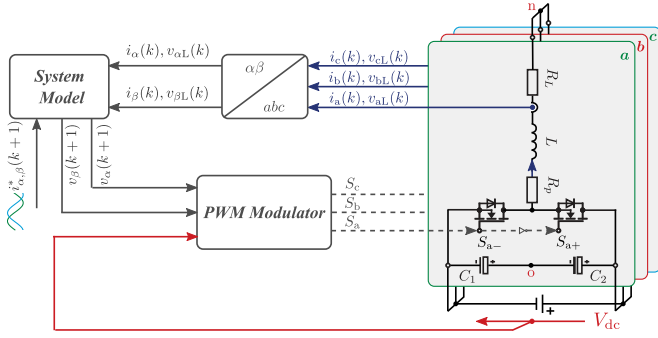


Fig. 5. Block diagram of the conventional DBC.

discrete-models of the system developed in Section II, i.e. the AC currents analytical models, and all the 8 possible switching states to predict the future behavior of the controlled variables. The defined cost function G objective is to minimize the quadratic error between the predicted load currents $i_{\alpha\beta}(k+1)$ and their references $i_{\alpha\beta}^*(k+1)$, as represented:

$$G = |i_{\alpha}^*(k+1) - i_{\alpha}(k+1)|^2 + |i_{\beta}^*(k+1) - i_{\beta}(k+1)|^2 \quad (6)$$

In practice, two steps of prediction are used as the delay compensation for the conventional MPC. While computing the new values of $i_{\alpha,\beta}$, The values of the switching states calculated during the previous sampling interval are utilized and then applied to the converter. The new calculated values of $i_{\alpha,\beta}$ are used in the cost function minimization [3], [4].

C. Dead-Beat Controller or DBC

DBC utilizes the system model in (3) to select the best voltage vector that improves the reference tracking of the control logic in the next sampling period [24], [25]. The output of the DBC is a continuous value, and it is chosen by attempting to attain a current response at the next sampling instant which is equal to the desired reference value. After that, the voltage vector in the next sampling period is determined, and the carrier-based PWM modulator with any practicable zero-sequence injections can be realized. The block diagram of this control strategy for the three-phase three-wire two-level VSI is shown in Fig. 5.

IV. CARRIER-BASED MMPC

A. Voltage Based FCS-MPC

Considering that the current feedback control operates appropriately by applying the optimized voltage vectors, it is possible to assume that the load dynamic in (3) can be expressed by the inverse analytical model as [27], [28]:

$$\begin{cases} v_{\alpha}^*(k) = \frac{L}{T_s} i_{\alpha}^*(k+1) + \frac{R_p T_s - L}{T_s} i_{\alpha}(k) + v_{\alpha L}(k) \\ v_{\beta}^*(k) = \frac{L}{T_s} i_{\beta}^*(k+1) + \frac{R_p T_s - L}{T_s} i_{\beta}(k) + v_{\beta L}(k). \end{cases} \quad (7)$$

The space distribution of the reference vector $v^*(k)$ along with the eight synthesizable voltage vectors are shown in Fig. 6.

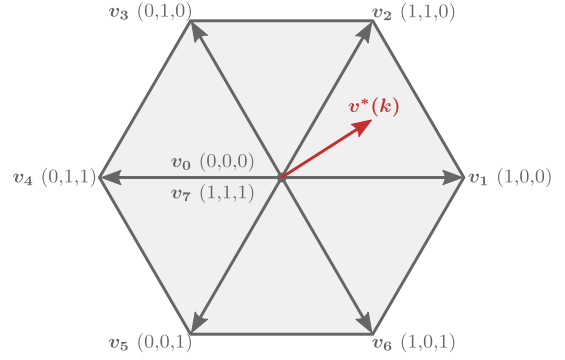


Fig. 6. Voltage space vectors of the three-phase two-level VSI.

Above all, the voltage based FCS-MPC works towards identifying the voltage vector to be applied by the VSI which best suits the minimization of the following quadratic cost function:

$$G = |v_{\alpha}^*(k) - v_{\alpha}(k)|^2 + |v_{\beta}^*(k) - v_{\beta}(k)|^2 \quad (8)$$

Based on the inverse analytical model in (3) and (7), the expression (8) can be evolved as:

$$\begin{aligned} G &= \left| \frac{L}{T_s} i_{\alpha}^*(k+1) + \frac{R_p T_s - L}{T_s} i_{\alpha}(k) + v_{\alpha L}(k) - v_{\alpha}(k) \right|^2 \\ &\quad + \left| \frac{L}{T_s} i_{\beta}^*(k+1) + \frac{R_p T_s - L}{T_s} i_{\beta}(k) + v_{\beta L}(k) - v_{\beta}(k) \right|^2 \\ &= \left(\frac{L}{T_s} \right)^2 |i_{\alpha}^*(k+1) + \frac{R_p T_s - L}{L} i_{\alpha}(k) + \frac{T_s}{L} (v_{\alpha L}(k) - v_{\alpha}(k))|^2 \\ &\quad + \left(\frac{L}{T_s} \right)^2 |i_{\beta}^*(k+1) + \frac{R_p T_s - L}{L} i_{\beta}(k) + \frac{T_s}{L} (v_{\beta L}(k) - v_{\beta}(k))|^2 \\ &= \left(\frac{L}{T_s} \right)^2 |i_{\alpha}^*(k+1) - i_{\alpha}(k+1)|^2 \\ &\quad + \left(\frac{L}{T_s} \right)^2 |i_{\beta}^*(k+1) - i_{\beta}(k+1)|^2 \end{aligned} \quad (9)$$

It is clearly seen that due to the absolute value the cost function shown in (8) is equivalent to the cost function described in (6) of the conventional MPC. This proves that using voltage vector FCS-MPC is essentially the same as prior MPC methods in terms of cost function [29].

B. Delay Time Compensation

In order to eliminate the control delay due to the digital implementation, the voltage vectors need to be determined at the $(k+1)$ th instant. By time shifting (7) one step forward and assuming $v_{\alpha L}(k+1) \approx v_{\alpha L}(k)$, $v_{\beta L}(k+1) \approx v_{\beta L}(k)$ in such a short sampling interval [30], [31], the predictive voltage model can be obtained as:

$$\begin{cases} v_{\alpha}^*(k+1) = \frac{L}{T_s} i_{\alpha}^*(k+2) + \frac{R_p T_s - L}{T_s} i_{\alpha}(k+1) + v_{\alpha L}(k) \\ v_{\beta}^*(k+1) = \frac{L}{T_s} i_{\beta}^*(k+2) + \frac{R_p T_s - L}{T_s} i_{\beta}(k+1) + v_{\beta L}(k). \end{cases} \quad (10)$$

Combining (3) and (10), the following derivation arises:

$$\begin{aligned} v_\alpha^*(k+1) &= \frac{L}{T_s} i_\alpha^*(k+2) - \frac{(L-R_p T_s)^2}{L T_s} i_\alpha(k) \\ &\quad + \left(\frac{R_p T_s}{L} - 1\right) v_\alpha(k) + \left(2 - \frac{R_p T_s}{L}\right) v_{\alpha L}(k) \\ v_\beta^*(k+1) &= \frac{L}{T_s} i_\beta^*(k+2) - \frac{(L-R_p T_s)^2}{L T_s} i_\beta(k) \\ &\quad + \left(\frac{R_p T_s}{L} - 1\right) v_\beta(k) + \left(2 - \frac{R_p T_s}{L}\right) v_{\beta L}(k). \end{aligned} \quad (11)$$

where $i_\alpha^*(k+2)$ and $i_\beta^*(k+2)$ are the two step future current reference in $\alpha\beta$ frame, and $v_\alpha(k)$ and $v_\beta(k)$ are the selected voltage vectors at the previous computational routine. According to the Lagrange extrapolation in [4], the one-step future current reference can be calculated by using the present and the two past reference values as:

$$\begin{cases} i_\alpha^*(k+1) = 3i_\alpha^*(k) - 3i_\alpha^*(k-1) + i_\alpha^*(k-2) \\ i_\beta^*(k+1) = 3i_\beta^*(k) - 3i_\beta^*(k-1) + i_\beta^*(k-2). \end{cases} \quad (12)$$

Similarly, the two-step future current reference required in (11) can be obtained by shifting one-step forward of the future current reference in (12) as:

$$\begin{cases} i_\alpha^*(k+2) = 3i_\alpha^*(k+1) - 3i_\alpha^*(k) + i_\alpha^*(k-1) \\ i_\beta^*(k+2) = 3i_\beta^*(k+1) - 3i_\beta^*(k) + i_\beta^*(k-1). \end{cases} \quad (13)$$

C. Reference Duty Cycle Calculations

The original sinusoidal modulation signals (v_a^* , v_b^* , and v_c^*) can be calculated from the reference voltage vector in (11):

$$\begin{cases} v_a^*(k+1) = v_\alpha^*(k+1) \\ v_b^*(k+1) = -\frac{1}{2}v_\alpha^*(k+1) + \frac{\sqrt{3}}{2}v_\beta^*(k+1) \\ v_c^*(k+1) = -\frac{1}{2}v_\alpha^*(k+1) - \frac{\sqrt{3}}{2}v_\beta^*(k+1). \end{cases} \quad (14)$$

As shown in Fig. 2, the modulation waveforms v_a^* , v_b^* , and v_c^* of the carrier-based PWM method are given as:

$$\begin{cases} v_a^{**}(k+1) = v_a^*(k+1) + v_0(k+1) \\ v_b^{**}(k+1) = v_b^*(k+1) + v_0(k+1) \\ v_c^{**}(k+1) = v_c^*(k+1) + v_0(k+1) \end{cases} \quad (15)$$

where v_0 is the zero-sequence voltage derived as shown in Fig. 2.

Taking the condition that the reference voltage vector v^* is located in the first sector S_1 as an example, the two active voltage vectors to synthesize v^* will be v_1 (100), and v_2 (110), as shown in Fig. 7. The three-phase duty cycles (d_a , d_b , and d_c) can be calculated from their modulation signals as [26]:

$$\begin{cases} d_a^*(k+1) = 0.5[v_a^{**}(k+1)/(V_{dc}/2) + 1] \\ d_b^*(k+1) = 0.5[v_b^{**}(k+1)/(V_{dc}/2) + 1] \\ d_c^*(k+1) = 0.5[v_c^{**}(k+1)/(V_{dc}/2) + 1]. \end{cases} \quad (16)$$

The variables d_a , d_b , and d_c can also be expressed as:

$$\begin{aligned} \begin{bmatrix} d_a^* \\ d_b^* \\ d_c^* \end{bmatrix} &= \begin{bmatrix} 1 & 1 & 1 & 0 \\ 1 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} T_7/T_s \\ T_2/T_s \\ T_1/T_s \\ T_0/T_s \end{bmatrix} \\ &= \begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 0 \\ 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} d_7^* \\ d_2^* \\ d_1^* \end{bmatrix} \end{aligned} \quad (17)$$

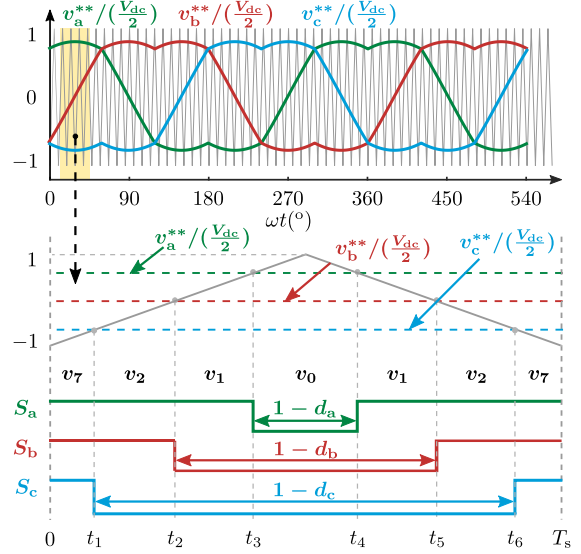


Fig. 7. Voltage space vectors of the three-phase two-level VSI in Sector I.

where, T_7 , T_2 , T_1 , and T_0 are the duration time of v_7 , v_2 , v_1 , and v_0 , respectively. For each one of the two active vectors v_i and v_j [$(i, j) \in \{(1, 2), (2, 3), (3, 4), (4, 5), (5, 6), (6, 1)\}$] the three-phase duty cycles can be determined as given in Appendix-A. Accordingly, the generalized expression of the three-phase duty cycles with any pair of active vectors $v_i(S_a^i, S_b^i, S_c^i)$ and $v_j(S_a^j, S_b^j, S_c^j)$ can be summarized as:

$$\begin{cases} d_a^* = d_i^* S_a^i + d_j^* S_a^j + d_7^* S_a^7 \\ d_b^* = d_i^* S_b^i + d_j^* S_b^j + d_7^* S_b^7 \\ d_c^* = d_i^* S_c^i + d_j^* S_c^j + d_7^* S_c^7 \end{cases} \quad (18)$$

Thereafter, by solving the three-dimensional cubic equations in (18), it is possible to calculate the duty cycles for each pair of active vectors and v_7 as:

$$\begin{aligned} d_i^* &= \frac{(-d_b^* + d_c^*) S_a^j + (d_a^* - d_c^*) S_b^j - (d_a^* - d_b^*) S_c^j}{S_a^i S_b^j - S_a^j S_b^i - S_a^i S_c^j + S_a^j S_c^i + S_b^i S_c^j - S_b^j S_c^i} \\ d_j^* &= \frac{(d_b^* - d_c^*) S_a^i - (d_a^* - d_c^*) S_b^i + (d_a^* - d_b^*) S_c^i}{S_a^i S_b^j - S_a^j S_b^i - S_a^i S_c^j + S_a^j S_c^i + S_b^i S_c^j - S_b^j S_c^i} \\ d_7^* &= \frac{(S_a^i S_c^j - S_a^j S_c^i) d_a^* + (S_a^j S_c^i - S_a^i S_c^j) d_b^*}{S_a^i S_b^j - S_a^j S_b^i - S_a^i S_c^j + S_a^j S_c^i + S_b^i S_c^j - S_b^j S_c^i} \\ &\quad + \frac{(S_a^i S_b^j - S_a^j S_b^i) d_c^*}{S_a^i S_b^j - S_a^j S_b^i - S_a^i S_c^j + S_a^j S_c^i + S_b^i S_c^j - S_b^j S_c^i} \end{aligned} \quad (19)$$

D. Optimal Vectors and Modulation Waveforms Generation

The reference voltage calculation and the time interval calculations are executed in parallel, and for each pair of vectors, a cost function future voltage reference is calculated as follows:

$$\begin{cases} G^i = (v_a^{**} - v_a^i)^2 + (v_b^{**} - v_b^i)^2 + (v_c^{**} - v_c^i)^2 \\ G^j = (v_a^{**} - v_a^j)^2 + (v_b^{**} - v_b^j)^2 + (v_c^{**} - v_c^j)^2 \\ G^z = (v_a^{**} - v_a^z)^2 + (v_b^{**} - v_b^z)^2 + (v_c^{**} - v_c^z)^2 \end{cases} \quad (20)$$

where $v_x^{(i,j)} \in \{\pm V_{dc}/3, \pm 2V_{dc}/3\}$, $x \in \{a, b, c\}$, and $v_x^z = 0$. The valid eight switching states and the corresponding VSI voltage states are listed in Table II. Thereafter, based on the Lagrange optimization theory [5], the duty cycles is simplified

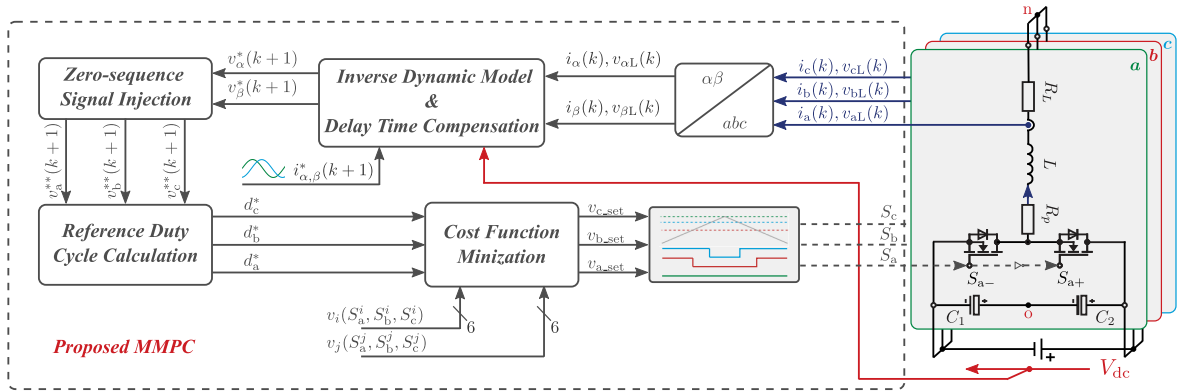


Fig. 8. Overall block diagram of the carrier-based MMPC.

TABLE II
VALID SWITCHING STATES AND CORRESPONDING PHASE VOLTAGE

Voltage state	Switching state	v_a	v_b	v_c
v_1	(1, 0, 0)	$2V_{dc}/3$	$-V_{dc}/3$	$-V_{dc}/3$
v_2	(1, 1, 0)	$V_{dc}/3$	$V_{dc}/3$	$-2V_{dc}/3$
v_3	(0, 1, 0)	$-V_{dc}/3$	$2V_{dc}/3$	$-V_{dc}/3$
v_4	(0, 1, 1)	$-2V_{dc}/3$	$V_{dc}/3$	$V_{dc}/3$
v_5	(0, 0, 1)	$-V_{dc}/3$	$-V_{dc}/3$	$2V_{dc}/3$
v_6	(1, 0, 1)	$V_{dc}/3$	$-2V_{dc}/3$	$V_{dc}/3$

as:

$$\begin{cases} d_i = \frac{\frac{1}{G^i}}{\frac{1}{G^i} + \frac{1}{G^j} + \frac{1}{G^z}} \\ d_j = \frac{\frac{1}{G^j}}{\frac{1}{G^i} + \frac{1}{G^j} + \frac{1}{G^z}} \\ d_z = \frac{\frac{1}{G^z}}{\frac{1}{G^i} + \frac{1}{G^j} + \frac{1}{G^z}} \end{cases} \quad (21)$$

Where $d_z = d_0 + d_7$ is the duty cycle for the zero vectors. d_7 can be defined as $d_7 = kd_z$, where $k = 0.5$ for SVPWM, and $k = (\text{sign}(v_0) + 1)/2$ for DPWM1. The cost function for each region is calculated as:

$$G = |d_i - d_i^*|^2 + |d_j - d_j^*|^2 + |d_7 - d_7^*|^2 \quad (22)$$

The optimal pair of vectors with the minimum value of G , named (S_a^i, S_b^i, S_c^i) and (S_a^j, S_b^j, S_c^j) is selected to be applied to the associated duty cycles d_{a_set} , d_{b_set} , and d_{c_set} .

$$\begin{cases} d_{a_set} = d_i S_a^i + d_j S_a^j + d_7 \\ d_{b_set} = d_i S_b^i + d_j S_b^j + d_7 \\ d_{c_set} = d_i S_c^i + d_j S_c^j + d_7 \end{cases} \quad (23)$$

Then, the modulation waveforms v_{a_set} , v_{b_set} , and v_{c_set} that are set to be compared to the triangular carrier are obtained.

$$\begin{cases} v_{a_set} = 2d_{a_set} - 1 \\ v_{b_set} = 2d_{b_set} - 1 \\ v_{c_set} = 2d_{c_set} - 1 \end{cases} \quad (24)$$

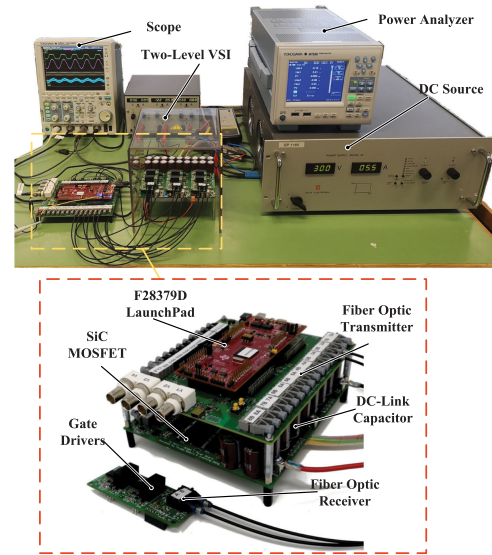


Fig. 9. Experimental setup.

The overall block diagram of the studied carrier-based MMPC method is shown in Fig. 8.

V. SIMULATION AND EXPERIMENTAL VERIFICATION

To validate the effectiveness of the studied MMPC method, simulations and experimental tests are conducted. Firstly, a PLECS based simulation is carried out. Then, the control methods are implemented and run on the experimental setup of a three-wire two-level 3-kW VSI controlled with the Texas Instruments TMS320F28379D as shown in Fig. 9. Compared with the commonly-used DSP TMS320F28335 in power electronic converters, the TMS320F28379D has an improved calculation speed with a comparable cost (\$11.836/1 ku) [32]. The SiC MOSFET from Wolfspeed C3M0120090 J is selected for the VSI switches. The simulation and experiment parameters are shown in Table III. The value of R_p will be intentionally changed in the tests during the benchmarking of control methods. The current references i_α^* and i_β^* in both simulation and experiment are set artificially. The sampling and switching frequency of

TABLE III
SIMULATION AND EXPERIMENTAL PARAMETERS

Variables	Parameters	Value
V_{dc}	DC voltage	300 V
C_1, C_2	DC capacitance	738 μ F
f_0	Output frequency	50 Hz
R_L	Load resistor	10 Ω
R_p	Parasitic resistor	0.5 Ω
L	Inductive filter	3 mH

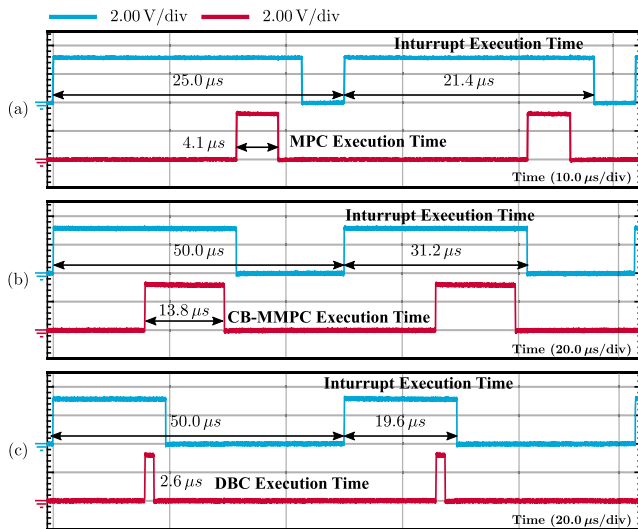


Fig. 10. Measured code execution times for (a) FCS-MPC, (b) CB-MMPC methods, and (c) DBC PWM methods.

the CB-MMPC and DBC based methods are set to be 20 kHz. In order to have a reasonable comparison between the studied control methods, a higher sampling rate of $f_s = 40$ kHz is considered for the classical FCS-MPC, which is the double of the modulated methods, i.e. CB-MMPC and DBC PWM methods, and it is commonly adopted by the literature [5], [10], [13], [15]. It is noted that in the experimental tests, due to the lack of AC voltage measurements, $v_{\alpha L} = R_L i_{\alpha}$ and $v_{\beta L} = R_L i_{\beta}$ are used in the system model (1).

A. MCU Computational Time and Switching Signal Frequency Spectra

Fig. 10 shows the execution time achieved in the MCU of the prototype for the implemented FCS-MPC, the CB-MMPC and DBC PWM methods. It can be seen that the traditional FCS-MPC program needs a total of 21.4 μ s to be executed in the control interrupt loop, of which 4.1 μ s is required to perform the calculations of the MPC algorithm. Meanwhile, the total execution time of the CB-MMPC is 31.2 μ s in the control interrupt loop, where 13.8 μ s is used to process the CB-MMPC algorithm. For the DBC PWM method, the execution time of the control interrupt loop is 19.6 μ s in total, where only 2.6 μ s is used for the DBC algorithm. As shown in Fig. 10, all methods can finish the algorithm within one sampling period. The DBC PWM

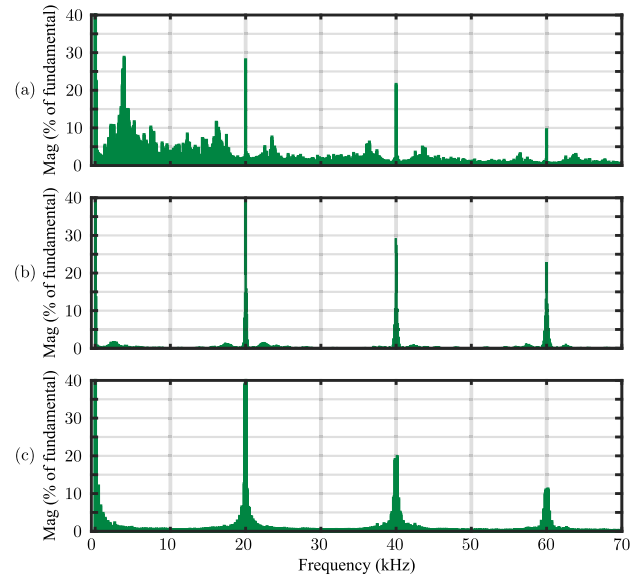


Fig. 11. Experimental switching signal frequency spectrum for: (a) conventional FCS-MPC, (b) CB-MMPC SVPWM, and (c) CB-MMPC DPWM1.

method requires the least computation time, because it does not need to calculate the value of the cost function repeatedly to find the minimum value. Although the implementation of the studied CB-MMPC methods has a higher computational burden, it is still able to accomplish the calculations within about 60% of the available time.

The frequency spectrum of the experimental switching signal for FCS-MPC and CB-MMPC methods is given in Fig. 11 with the current magnitude set as 12 A. It can be seen that the dominant high-frequency components of all methods are around the integer frequencies of 20 kHz. Therefore, a fair comparison with FCS-MPC and the proposed CB-MMPC method can be conducted.

B. Steady-State Response

The steady-state waveforms for the three-phase output currents (i_a, i_b, i_c), the switching signal (S_a^+), the modulation waveform (v_a^{**}), the phase voltage (v_{an}), and the line-to-line voltage (v_{ab}) obtained with the conventional FCS-MPC, DBC, and the CB-MMPC methods are shown in Fig. 12, where the magnitude of the reference current is set as 12 A. By analyzing the results one can observe that the shape of the output current of the FCS-MPC can be considerably improved by the CB-MMPC strategies, which is similar to the results obtained with the DBC PWM methods. The modulation waveform (v_a^{**}) of the DBC PWM methods are smoother than the ones for the CB-MMPC methods which leads to a better current THD in Table IV, because it does not need to determine the voltage vectors via cost function optimization. Additionally, the current ripple for the CB-MMPC SVPWM is found slightly lower than for the CB-MMPC DPWM1. As expected this occurs because the DPWM1 modulation strategy has each phase of the VSI stopping switching during one third of the fundamental time.

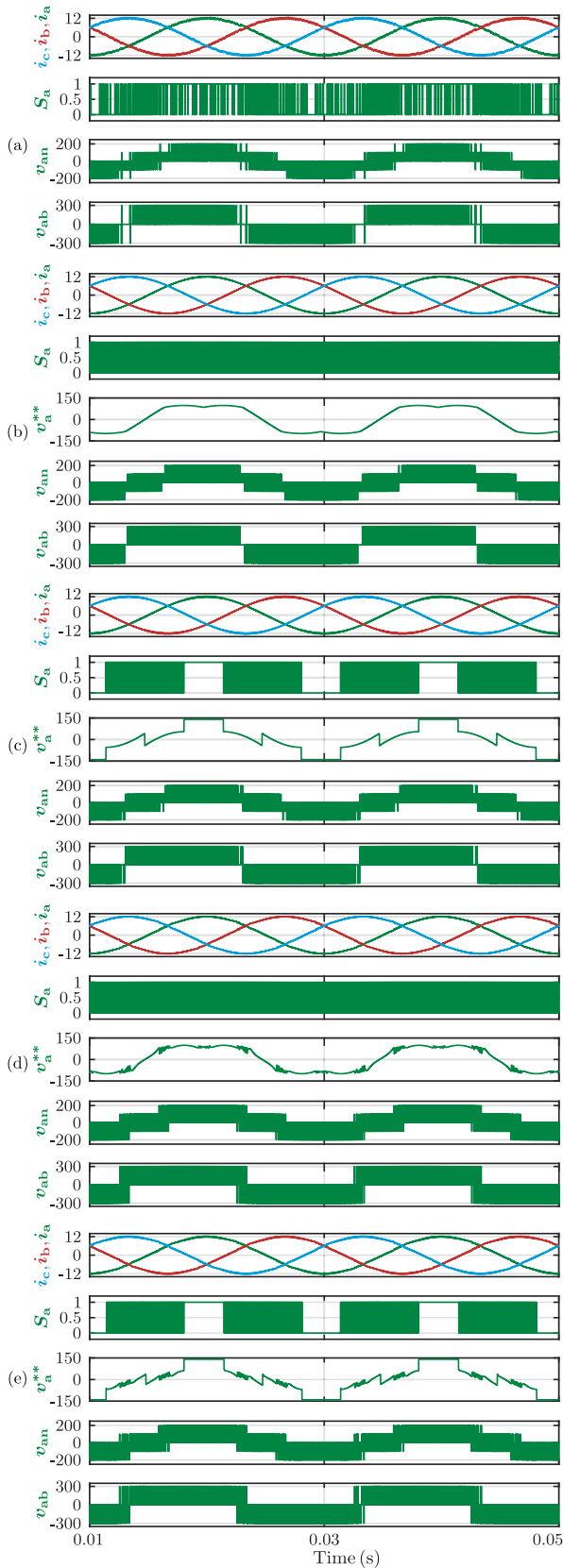


Fig. 12. Steady-state simulation waveforms for the three-phase output currents (i_a , i_b , i_c), the switching signal (S_a^+), the modulation waveform (v_a^{**}), the phase voltage (v_{an}), and the line-to-line voltage (v_{ab}), for: (a) conventional FCS-MPC, (b) DBC SVPWM, (c) DBC DPWM1, (d) CB-MMPC SVPWM, and (e) CB-MMPC DPWM1.

TABLE IV
CURRENT THD WITH A VARIATION IN L AND R_p

	Methods	L			
		$L'=0.5L$	$L'=L$	$L'=1.5L$	$L'=2L$
L	FCS-MPC	8.51%	6.68%	7.92%	10.02%
	DBC-SVPWM	1.94%	1.89%	1.95%	-
	DBC-DPWM1	2.13%	2.04%	2.31%	-
	CB-SVPWM	2.42%	2.21%	2.38%	4.98%
	CB-DPWM1	2.77%	2.46%	2.61%	5.39%
	Methods	R_p			
		$R'_p=0R_p$	$R'_p=R_p$	$R'_p=2R_p$	$R'_p=4R_p$
R_p	FCS-MPC	6.95%	6.68%	6.66%	6.68%
	DBC-SVPWM	1.90%	1.89%	1.86%	1.86%
	DBC-DPWM1	2.05%	2.04%	1.99%	1.98%
	CB-SVPWM	2.24%	2.21%	2.20%	2.20%
	CB-DPWM1	2.52%	2.46%	2.46%	2.51%

Fig. 13 presents the main experimental waveforms obtained during the steady state operation for the implemented FCS-MPC, DBC and the CB-MMPC PWM methods. As it can be noted that the experimental results have good correspondence with the PLECS simulation results depicted in Fig. 12. The output currents obtained by the CB-MMPC methods are similar as the results from the DBC PWM methods, and above all are better than the conventional FCS-MPC even though the sampling frequency is lower. Based on these results one can verify the effectiveness of the tested CB-MMPC methods.

C. Dynamic Response

To demonstrate the performance of the studied MPC techniques in terms of dynamic response, a transient test is carried out. Fig. 14(a) and Fig. 14(b) show the experimental waveforms for the output current (i_a), the switching signals (S_a^+), the modulation reference (v_a^{**}), and the converter voltage (v_{an}) when the magnitude of the reference currents is increased from 6 A to 12 A. The experimental results of the reference current with a step change in the frequency command from 50 Hz to 25 Hz are presented in Fig. 14(c) and Fig. 14(d). Since v_{an} is the switching waveform which is the potential difference from the phase leg, a , to the load star point, n , due to the resistive load used, the step change of output voltage represents a modulation index change and this can be observed via v_a^{**} and i_a . It can be found that the phase currents and phase voltage controlled by the proposed method follow the reference change with fast dynamics under both step changes.

The fast dynamic performance of the CB-MMPC can be clearly seen in Fig. 15. Both CB-MMPC SVPWM and CB-MMPC DPWM1 have similar results to the FCS-MPC and DBC PWM methods during the transient time, meanwhile the FCS-MPC is found to be slightly faster than the modulated strategies, because its sampling frequency is higher. Furthermore, the experimental result in Fig. 16 shows that the transient time for both CB-MMPC SVPWM and CB-MMPC DPWM1 is about 740 μ s, which is almost the same as the time obtained by the DBC PWM methods and nearly twice that of the FCS-MPC. Therefore, it is proved that the CB-MMPC strategy can improve

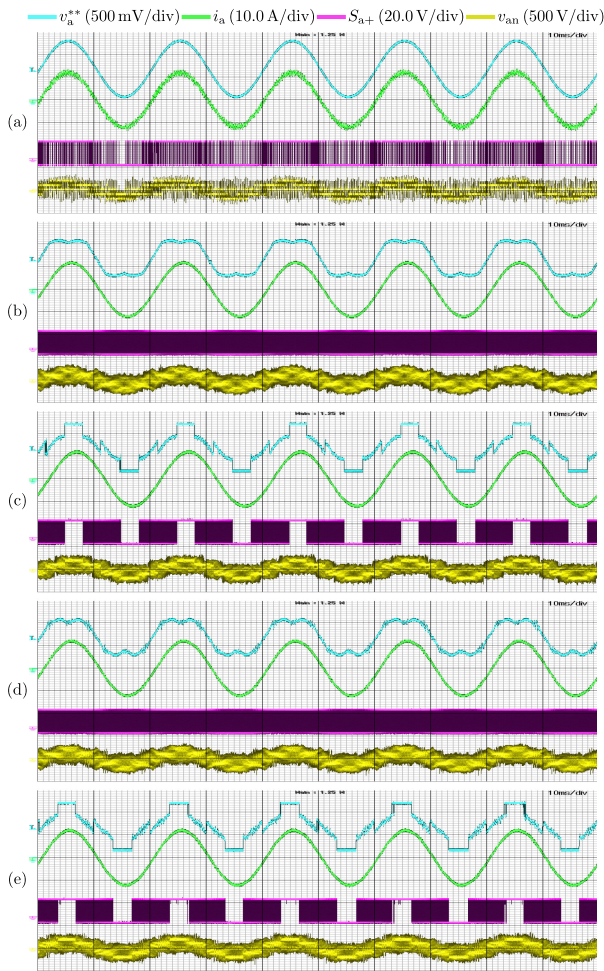


Fig. 13. Steady-state experimental waveforms for the output current (i_a), the switching signals (S_a^+), the modulation reference v_a^{**} , and the converter voltage v_{an} for: (a) conventional FCS-MPC, (b) DBC SVPWM, (c) DBC DPWM1, (d) CB-MMPC SVPWM, and (e) CB-MMPC DPWM1.

current distortion without compromising the performance of fast dynamic response.

Simulation results of the three-phase output currents (i_a , i_b , i_c), the switching signal (S_a^+), the modulation waveform (v_a^{**}), the phase voltage (v_{an}), and the line-to-line voltage (v_{ab}) obtained with the CB-MMPC methods when a load resistance step change from 10Ω to 5Ω happens are shown in Fig. 17, where the magnitude of the reference current is set as 12 A. Both methods can adapt the step-change in load well. Since the prototype does not implement AC voltage measurements, it is not possible to use the system with an AC voltage source, and carry out the experiments of a load step change with the fixed modulation index.

D. Control System Performance Considering Various Modulation Indexes and Output Frequency

In practice, a wider range of modulation index (m_i) is expected. Therefore, in this section, simulation results considering a ramp change of AC current magnitude and frequency is implemented and the corresponding results are shown in Fig. 18.

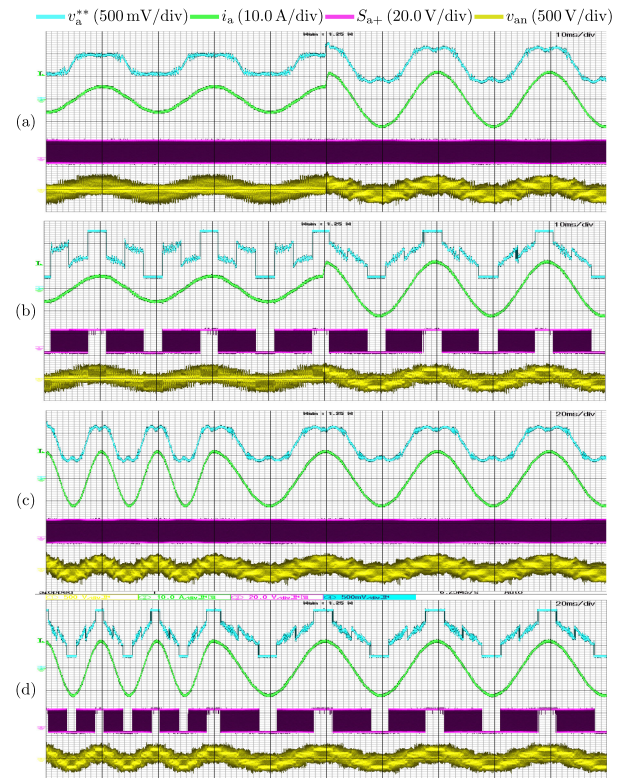


Fig. 14. Dynamic-state experimental waveforms for the output current (i_a), the switching signals (S_a^+), the modulation reference v_a^{**} , and the converter voltage v_{an} : (a) current reference step change with the CB-MMPC SVPWM, (b) current reference step with the CB-MMPC DPWM1, (c) frequency step change with the CB-MMPC SVPWM, and (d) frequency step change with the CB-MMPC DPWM1.

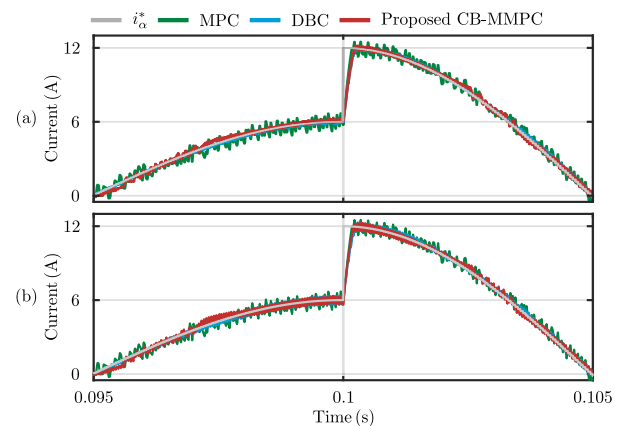


Fig. 15. Dynamic-state simulation waveforms comparison between the conventional FCS-MPC, the DBC methods, and the CB-MMPC methods. (a) FCS-MPC with DBC SVPWM and CB-MMPC SVPWM, (b) FCS-MPC with DBC DPWM1 and CB-MMPC DPWM1.

In Fig. 18(a), when the current reference is varying from 0 A to 16 A at the fixed fundamental frequency, i.e. f_o set to 50 Hz, the three-phase output currents controlled by the CB-MMPC can effectively follow the reference change. At $I_{ref} = 16$, m_i is 1.125 ($m_i = I_{ref} \sqrt{(R_p + R_L)^2 + \omega^2 L^2} / (V_{dc}/2)$), it can be found in Fig. 18(a), there is no significant current distortion

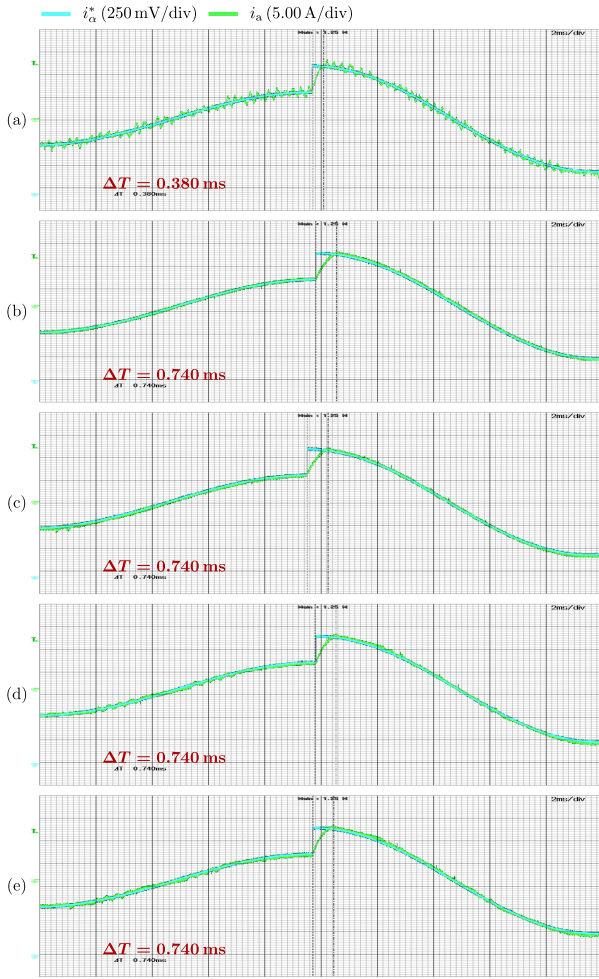


Fig. 16. Dynamic-state experimental waveforms comparison: (a) conventional FCS-MPC, (b) DBC SVPWM, (c) DBC DPWM1, (d) CB-MMPC SVPWM, and (e) CB-MMPC DPWM1.

in the high m_i range. The tracking error, i.e., the difference between the reference current and the measured current of the proposed method is compared with other methods when the current reference is increasing from 0 A to 16 A at 50 Hz fundamental frequency in Fig. 19. It can be seen the tracking error of the proposed CB-MMPC methods does not worsen much with the increase of m_i . It is higher than the DBC based methods but it is still better than the traditional FCS-MPC.

In Fig. 18(b), when f_o is set to change from 20 Hz to 100 Hz at the fixed current reference set of 12 A, the three-phase output currents controlled by the CB-MMPC can also efficiently follow the change in frequency. Accordingly, the CB-MMPC can adapt well to the change in both current reference magnitude and output frequency.

E. Parameter Sensitivity

In this section the effects of variations in the control parameters of the CB-MMPC method is analyzed and compared to the parameter sensitivity of the conventional FCS-MPC and the DBC PWM methods, where the magnitude of the current

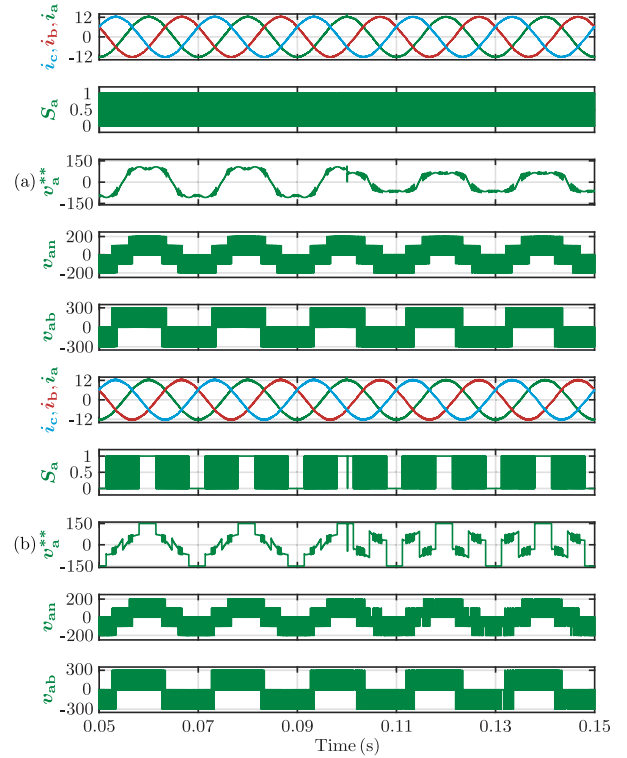


Fig. 17. Dynamic-state simulation waveforms for the three-phase output currents (i_a, i_b, i_c), the switching signal (S_a^+), the modulation waveform (v_a^{**}), the phase voltage (v_{an}), and the line-to-line voltage (v_{ab}) with load resistance step change from 10Ω to 5Ω, for: (a) CB-MMPC SVPWM, (b) CB-MMPC DPWM1.

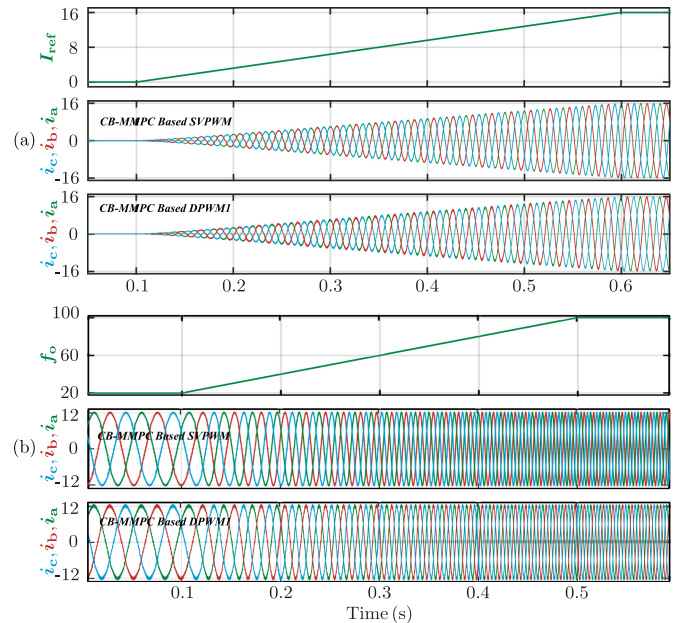


Fig. 18. Simulation waveforms for the CB-MMPC methods with current magnitudes and output frequency variations, (a) current reference varying from 0 A to 16 A at $f_o = 50$ Hz, (b) f_o varying from 20 Hz to 100 Hz at $I_{ref} = 12$ A.

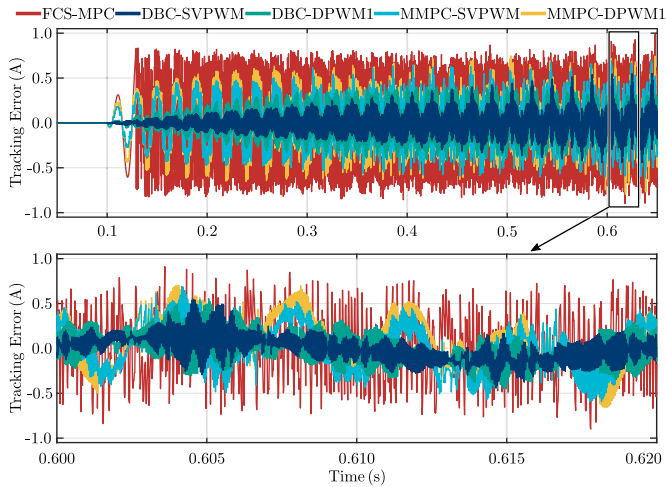


Fig. 19. Comparison of tracking error with different methods when current reference increases from 0 A to 16 A at $f_o = 50$ Hz and the zoomed results in one fundamental period.

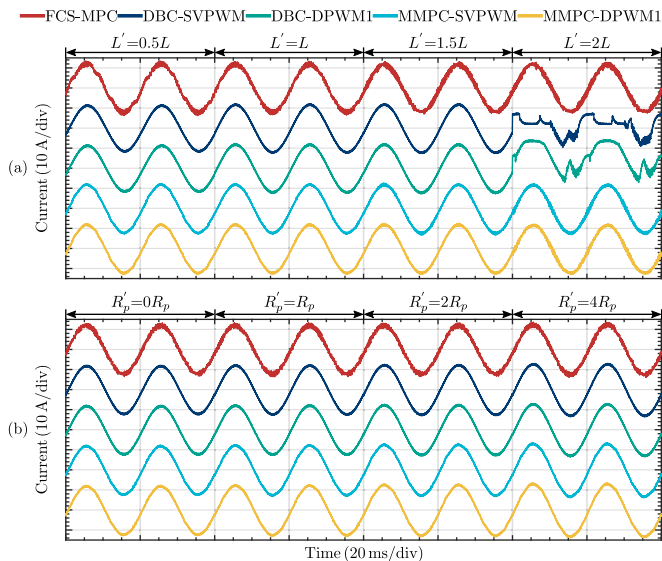


Fig. 20. Experimental results of output current with a variation in L and R_p , (a) variation in L , (b) variation in R_p .

reference is set as 12 A. The current THD for different variations of L and R_p are shown in Table IV, where L' and R_p' are the control parameters programmed in the code of the algorithm. The corresponding experimental waveforms of the output current obtained by the FCS-MPC, the DBC PWM methods, and the CB-MMPC methods are presented in Fig. 20.

It can be concluded that the effects of the variations of R_p in the controller do not have a substantial impact on the stability, tracking error and current THD for all methods. Conversely, a significant effect in the control performance is produced when the inductance L is misidentified by the control system. As expected, the worst performance is obtained with the conventional FCS-MPC when there is a $\pm 50\%$ variation in L . On the other hand, for the CB-MMPC and DBC methods, the change

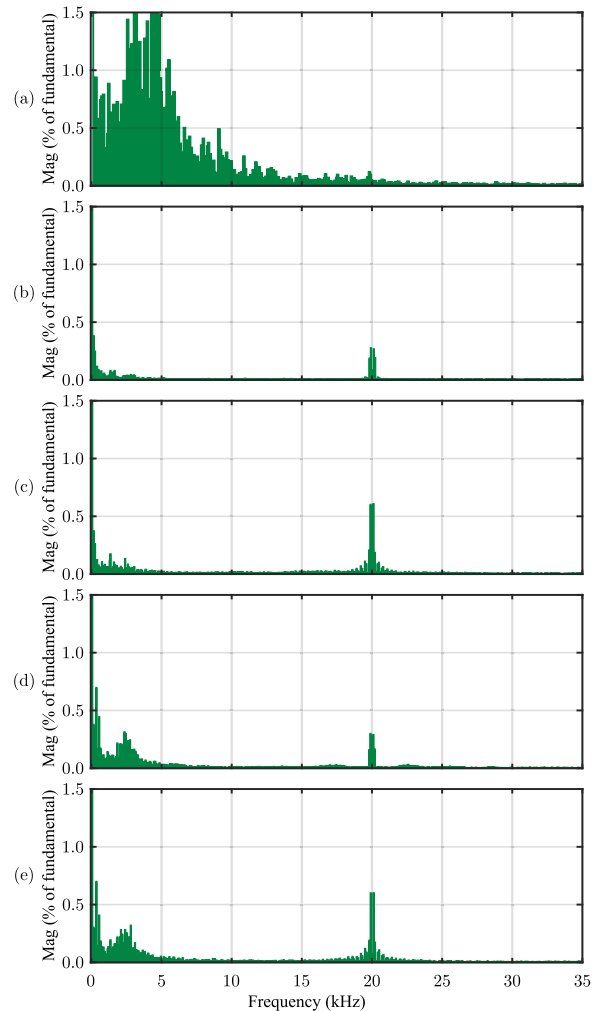


Fig. 21. Experimental frequency spectrum of the output current for: (a) conventional FCS-MPC, (b) DBC SVPWM, (c) DBC DPWM1, (d) CB-MMPC SVPWM, and (e) CB-MMPC DPWM1.

in current THD is much lower than that obtained by the conventional FCS-MPC. However, with further increment of L' , the output current achieved by the DBC based controller becomes unstable at $L' = 2L$; meanwhile, the results with FCS-MPC and the CB-MMPC methods can still keep the system stable, even though the quality of the current waveform deteriorates. Consequently, the CB-MMPC methods not only have a better performance than the FCS-MPC when L is misidentified by the control system but also are more robust performance than the DBC PWM methods.

F. Output Current Frequency Spectra

The output current frequency spectrum for the FCS-MPC, the DBC PWM and CB-MMPC methods obtained in the experimental setup are shown in Fig. 21, respectively, for the steady-state operation (current reference is set to 12 A and $f_o = 50$ Hz). From the current spectrum analysis, one can observe that the DBC PWM and the CB-MMPC methods produce a current with clustered harmonics multiplied by the fundamental switching

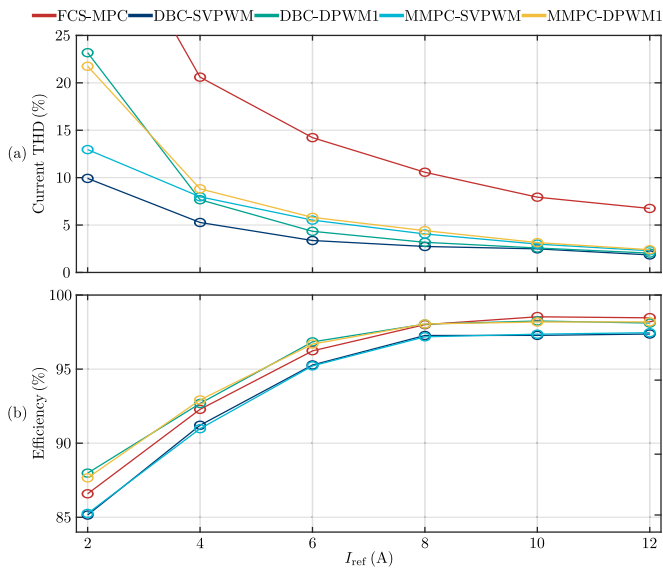


Fig. 22. Current THD and VSI power efficiency comparison at $f_o = 50$ Hz with different current reference, I_{ref} .

frequency of 20 kHz, while the FCS-MPC control has a variable switching frequency, which is mostly lower than 20 kHz. It can also be seen that the studied CB-MMPC methods contain more low frequency harmonic components than the DBC PWM methods, because the presented CB-MMPC methods will select the optimal vector pairs based on the cost function minimization, which will cause some distortions in the modulation waveforms as seen in Fig. 12 and Fig. 13, especially at the moment of sector change.

G. Current THD and Power Efficiency Comparison

The comparison results of the current THD and VSI power efficiency tested by a power analyzer YOKOGAWA WT500 for the FCS-MPC, the implemented DBC PWM and the CB-MMPC methods with different current reference and different output frequency are presented in Fig. 22 and Fig. 23. As expected, the current THD performance for the studied DBC and CB-MMPC methods are superior to that of the FCS-MPC. The performance of the CB-MMPC methods are similar to the DBC PWM methods. Moreover, CB-MMPC SVPWM generates lower current THD than the CB-MMPC DPWM1. Since the harmonic component within the low frequency can be significantly suppressed by using the CB-MMPC, it brings convenience in grid-connected applications compared to the FCS-MPC because it simplifies the selection of the typically used *LCL* filter and further reduce the current THD [33]. Fig. 22(b) shows the VSI power efficiency comparison between the CB-MMPC methods and the other studied methods. With DPWM methods, the power efficiency of the VSI is higher than the SVPWM methods. The power efficiency of FCS-MPC is lower than that of the DPWM methods when the current command is low, but it is slightly higher than that of the DPWM methods at the high current range, because the switching frequency of the FCS-MPC is not always fixed at 20 kHz, and one switching state can be the optimal selection

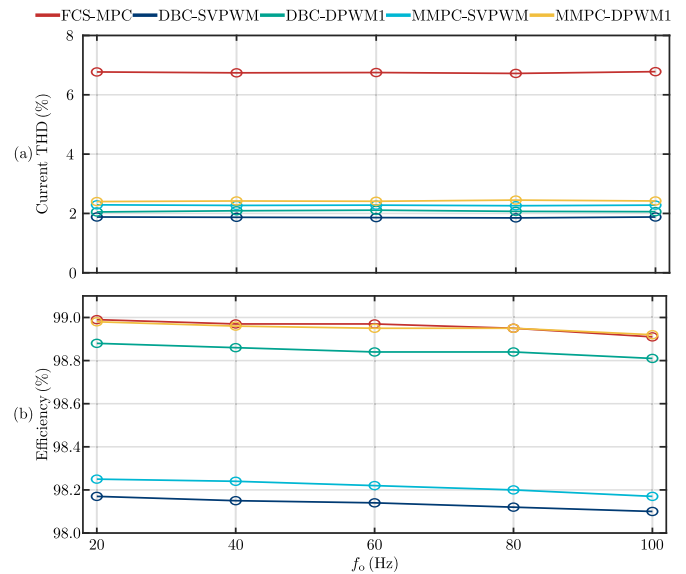


Fig. 23. Current THD and VSI power efficiency comparison at $I_{ref} = 12$ A with different output frequency, f_o .

for two or more sampling periods [3]. As shown in Fig. 23, with different output frequency, the current THD for different methods are similar, because the current references are the same and the modulation index does not change much; meanwhile, there is a slight decrease in the power efficiency for different methods, because the losses on the filter inductors increases with higher output frequency.

All in all, the presented simulation and experimental cases have shown that a remarkable improvement on current THD can be achieved with the CB-MMPC methods compared to the conventional FCS-MPC. The proposed CB-MMPC methods can adapt well to the change in wide modulation index and output frequency range. Additionally, the presented CB-MMPC method is more robust than the DBC PWM methods when there is a large mismatching in the converter's model parameters. These not only confirm the effectiveness of the studied method, but also show its comprehensive features when compared to other traditional strategies. Therefore, the validity and advantages of the CB-MMPC method are verified.

VI. CONCLUSION

This paper has proposed a carrier-based modulated model predictive control or CB-MMPC for the three-phase three-wire two-level VSI. This method, which has been illustrated through carrier-based PWM, is simple to implement in a commercial available DSP. Based on the different modulation waveforms, two different CB-MMPC methods have been studied in the paper, named CB-MMPC SVPWM and CB-MMPC DPWM1. Compared with the classic FCS-MPC and dead-beat control or DBC PWM methods, the implemented CB-MMPC solve the problem of wide spectrum of voltage/current harmonic content of the FCS-MPC without degrading the control performance in terms of fast dynamic response, and improve the robustness of the system to circuit model parametric mismatching when

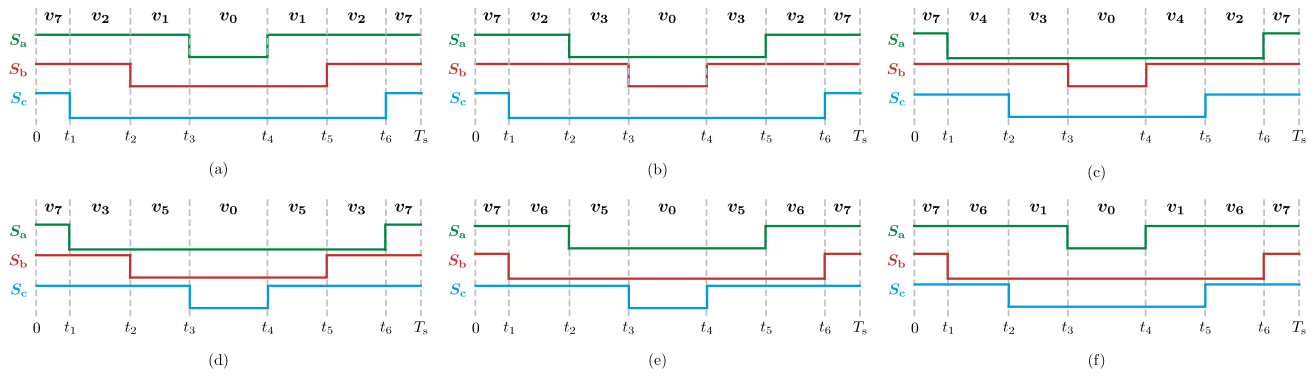


Fig. 24. Switching sequence in different Sectors. (a) Sector I, (a) Sector I, (b) Sector II, (c) Sector III, (d) Sector IV, (e) Sector V, and (f) Sector VI.

 TABLE V
 EXPRESSION OF d_a , d_b , AND d_c IN DIFFERENT SECTORS

Sector	Active vectors	(d_a, d_b, d_c)
I	$v_1(1, 0, 0), v_2(1, 1, 0)$	$\begin{bmatrix} 1 & 1 & 1 \\ d_7 \end{bmatrix}$
		$\begin{bmatrix} 1 & 1 & 0 \\ d_2 \end{bmatrix}$
		$\begin{bmatrix} 1 & 0 & 0 \\ d_1 \end{bmatrix}$
II	$v_2(1, 1, 0), v_3(0, 1, 0)$	$\begin{bmatrix} 1 & 1 & 0 \\ d_7 \end{bmatrix}$
		$\begin{bmatrix} 1 & 1 & 1 \\ d_2 \end{bmatrix}$
		$\begin{bmatrix} 1 & 0 & 0 \\ d_3 \end{bmatrix}$
III	$v_3(0, 1, 0), v_4(0, 1, 1)$	$\begin{bmatrix} 1 & 0 & 0 \\ d_7 \end{bmatrix}$
		$\begin{bmatrix} 1 & 1 & 1 \\ d_4 \end{bmatrix}$
		$\begin{bmatrix} 1 & 1 & 0 \\ d_3 \end{bmatrix}$
IV	$v_4(0, 1, 1), v_5(0, 0, 1)$	$\begin{bmatrix} 1 & 0 & 0 \\ d_7 \end{bmatrix}$
		$\begin{bmatrix} 1 & 1 & 0 \\ d_4 \end{bmatrix}$
		$\begin{bmatrix} 1 & 1 & 1 \\ d_5 \end{bmatrix}$
V	$v_5(0, 0, 1), v_6(1, 0, 1)$	$\begin{bmatrix} 1 & 1 & 0 \\ d_7 \end{bmatrix}$
		$\begin{bmatrix} 1 & 0 & 0 \\ d_6 \end{bmatrix}$
		$\begin{bmatrix} 1 & 1 & 1 \\ d_5 \end{bmatrix}$
VI	$v_6(1, 0, 1), v_1(1, 0, 0)$	$\begin{bmatrix} 1 & 1 & 1 \\ d_7 \end{bmatrix}$
		$\begin{bmatrix} 1 & 0 & 0 \\ d_6 \end{bmatrix}$
		$\begin{bmatrix} 1 & 1 & 0 \\ d_1 \end{bmatrix}$

compared to the DBC PWM methods. PLECS based simulations and a 3-kW VSI prototype have verified the effectiveness and superiority of the presented CB-MMPC method.

APPENDIX A DERIVATION OF THE THREE-PHASE DUTY CYCLES WITH ANY PAIR OF ACTIVE VECTORS

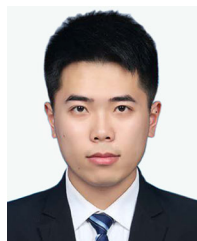
The switching sequence in every sector are presented in Fig. 24, and the duty cycles of each phase (d_a^n , d_b^n , and d_c^n) in sector n ($n \in \{1, 2, 3, \dots, 6\}$) are listed in Table V.

Therefore, for each one of the two active vectors v_i and v_j , the generalized expression of the three-phase duty cycles is summarized in (18).

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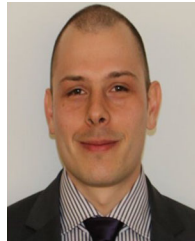
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