MSc thesis in Electrical Engineering

A Hybrid Step-Up DC-DC Converter and A VCSEL Driver

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Abstract

In today's highly information-based society, portable smart devices are helping everyone all the time. At the same time, a majority of them need corresponding power management modules to provide them with stable power from the Li-ion battery. Since different functional modules require different voltage levels, a special DC-DC converter or driver must be designed to meet the requirements. In this thesis, one design is proposed to fulfill the requirement of high efficiency, and another one achieves fully integrated.

This thesis proposes a hybrid DC-DC step-up converter with a new architecture by merging a traditional inductor-based (IB) boost converter with a switched-capacitor (SC) converter to boost $3-4.2$-V input to $20-30$-V output. By serially connecting an IB boost converter and a 1:6 Dickson SC converter, the capacitors take over most of the output voltage stress. As a result, the voltage stress over each switch is limited to 5 V, which makes it possible to implement all the power switches with only on-chip 5-V devices. Thanks to the 5-V devices, the overall power conversion efficiency is improved in various aspects. The switching frequency of the SC stage is decreased by the soft charging technique, which helps further improve the efficiency. The proposed converter is designed and simulated in TSMC 0.18 μm BCD process. An efficiency of 93.08 % is achieved under 3.7-V input and 29-V output voltage with a 25-mA current load.

A fully integrated VCSEL driver with adjustable pulse width is also proposed in this thesis. By combining two separate control signals, the VCSEL driver is able to overcome challenges posed by PVT and technology process limitations to achieve the narrowest pulse width of around 300-ps. The proposed converter is designed and simulated in SMIC 55 BCD process.

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1 Introduction

1.1 Background

In today's highly information-based society, smart devices are helping everyone all the time. At the same time, all related devices need corresponding power management modules to provide them the stable energy. Figure 1.1 shows the trends of Internet of Things(IoT) devices, which reflects the power modules of consumer electronics need to fulfill the new requirements with the development. In order to implement more and more functions in the tiny devices, all the modules within the device are preferred to be fully integrated. Meanwhile, the climate change problem asks power modules to be more efficient to save energy and protect the fragile climate[12]. Based on huge market holdings, a small improvement in efficiency helps to save total power consumption and reduces carbon emissions.

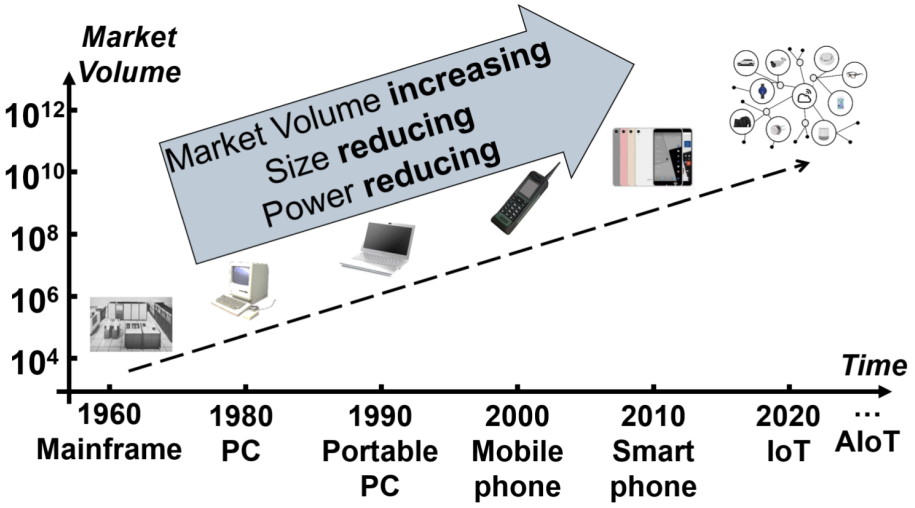

Figure 1.1: IoT device development will continue to follow the below trends, witnessing a continuous reduction in device size, reduction in power consumption, and expansion in market volume [1].

Since the majority part of IoT devices is powered by batteries, which only supply one voltage level within a certain range, the DC-DC converters are widely used in this scenario to fulfill the different voltage level requirements. The basic categorization of DC-DC converters is shown in Figure 1.2. Firstly, DC-DC converters are separated by switching. The linear regulator, represented by the low-dropout regulator (LDO), adjusts inner resistance with the changing

of input voltage and output resistance to maintain a stable output voltage. With the help of switching capability, another part of DC-DC converters storage or release electrical energy in capacitance or inductance in different time slots within the switching period to maintain a stable output voltage.

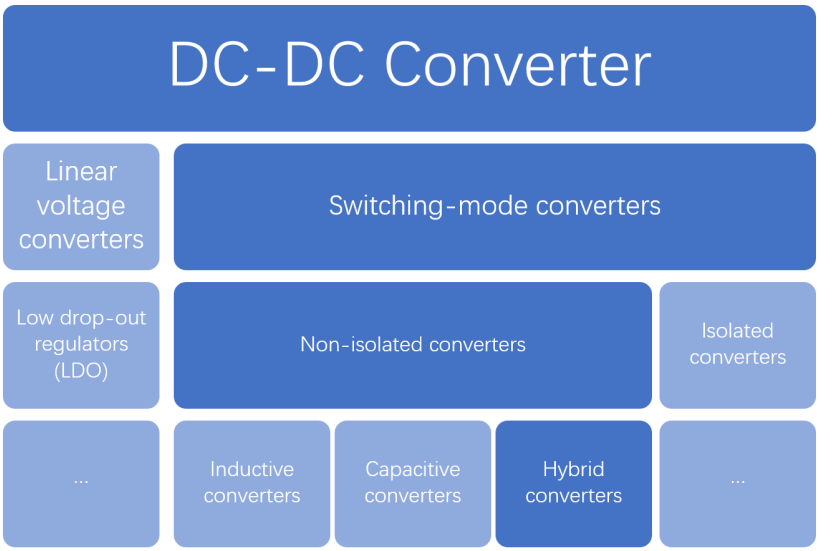

Figure 1.2: The basic categorization of DC-DC converters.

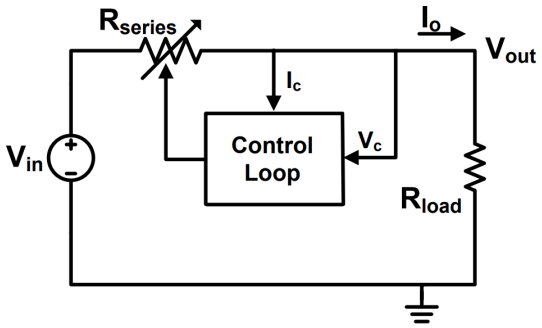

Figure 1.3: Schematic of a basic linear voltage converter[2].

The basic working principle of LDO is as shown in Figure 1.3. The stable output voltage level is achieved by an active resistive divider including a variable resistance (R_{series}) and the load resistance (R_{load}). Variable resistance is adjusted by the active control loop continually. The relationship between input and output voltage is as equation below.

$$\frac{V_{out}}{V_{in}} = \frac{R_{load}}{R_{load} + R_{series}} \tag{1.1}$$

The first drawback of LDO is reflected in Equation 1.1, in which only lower output voltage can be achieved. Therefore, the application scenario of this technique is limited by the principle and

only for step-down situations. Another drawback of this technique is the efficiency problem. The conversion efficiency of LDO in Figure 1.3 is calculated based on Equation 1.2.

$$\eta = \frac{V_{out} \cdot I_o}{V_{in} \cdot (I_c + I_o)} = VCR \cdot \frac{I_o}{I_o + I_c} \tag{1.2}$$

According to Equation 1.2, the voltage conversion ratio (VCR) is directly related to the efficiency of LDO. In order to keep converter efficiency within an acceptable range, the output voltage must be close to the input voltage. As a result, LDO is not only performing as a step-down converter but also hard to achieve high efficiency within a wide step-down VCR range.

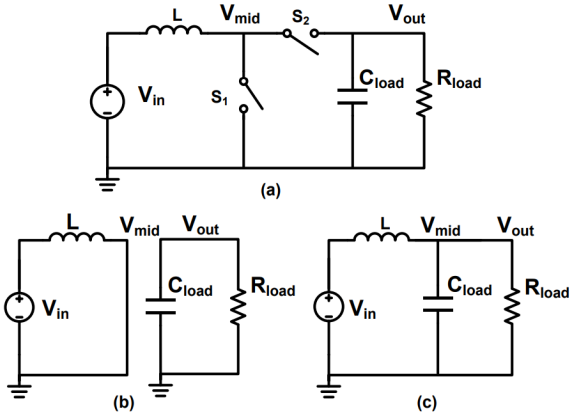

Figure 1.4: Schematic of an inductor-based step up DC-DC converter[2].

Figure 1.4 shows the basic structure of an inductor-cased step-up DC-DC converter. The first working phase shown in Figure 1.4 (b), in which the inductor L is been charged by the input voltage source when the low side switch S_1 is on and S_2 is off. In the second working stage, the energy stored in the inductor builds a forward voltage between the two sides of it and the output voltage is the sum result of input voltage and voltage built by the inductor. In the general step-up application scenarios, an inductor-based converter has a high conversion efficiency advantage, which will be discussed in the next chapter. However, the problem is the inductor is hard to integrate within chips, because of its large volume compared to integrated circuits. As a result, a tremendous amount of IoT decides to select the third way, the switched-capacitance technique, as their DC-DC converters.
Figure 1.5 shows the basic structure of a switched-capacitance step-up DC-DC converter. Rather than store energy in an inductor, the switched-capacitance technique stores energy in capacitance as shown in Figure 1.5 (b). After this charging phase, the switches control the capacitance in the right direction and build the output voltage. Compared to the inductor, capacitance is easier to integrate between the different layers of the chips. Especially for IoT devices, the power consumption is really low, which only requires relatively small capacitance. Even though the area of capacitance is also increasing the cost, no extra off-chip components like inductors achieve better volume and lower system cost. However, based on the design principle which will be discussed later, the converter is designed towards a certain VCR and achieve high efficiency at that working point. Therefore, the drawback of this kind of method is hard to maintain

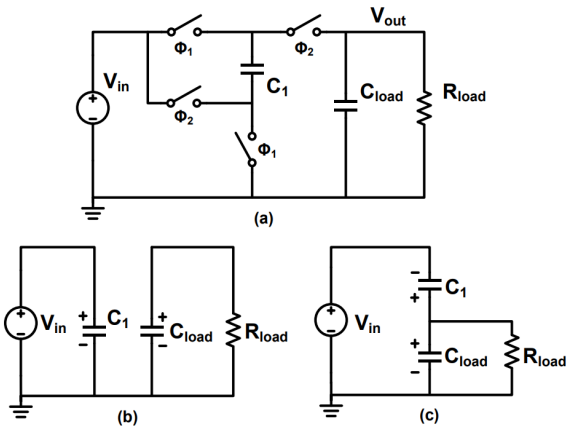

Figure 1.5: Schematic of a switched-capacitance DC-DC converter[2].

high efficiency in the wide VCR range. Input voltage level change leads to poor efficiency of the converter.

1.2 Motivation

Based on the above simple analyses of three main kinds of the DC-DC converter, it can be seen that each one has its own advantages and also some drawbacks. In order to achieve better performance, people are trying to combine them to overcome their own drawbacks and gain a better performance as a whole system. As a result, the hybrid structure of DC-DC converters is more popular and gained lots of attention in recent years. Meanwhile, there are some modules in the IoT devices that need voltage levels different from the input voltage level during part of their working period. In other words, that kind of module needs converters to generate a new voltage level but does not require converters to maintain it all the time. For this kind of need, DC-DC converters are wasted to implement to generate a new voltage level, since typical DC-DC converters have a large output capacitor to keep a stable output voltage all the time. A special driver with voltage conversion ability is more suitable. In this thesis, two suitable power module designs are proposed to meet the needs of two application scenarios.

1.2.1 High Voltage Conversion Ratio DC-DC Step-Up Converter

Display modules are widely used in different electric devices to provide information exchangeability. Take mobile phones as an example, which need LED panels to display information and support entertainment functions like video games. In a general application situation, only the Li-ion battery can be the power supply. Compared with the 3.7-V standard output voltage level of the Li-ion battery, the LED panel needs a much higher voltage to forward bias the LED panels[13]. As shown in Figure 1.6, a high voltage conversion ratio(VCR) DC-DC converter must be used to drive the LED panel. At the same time, compared to other parts of a smartphone, the LED panel consumes a large part of the total power. As a result, this scenario asks

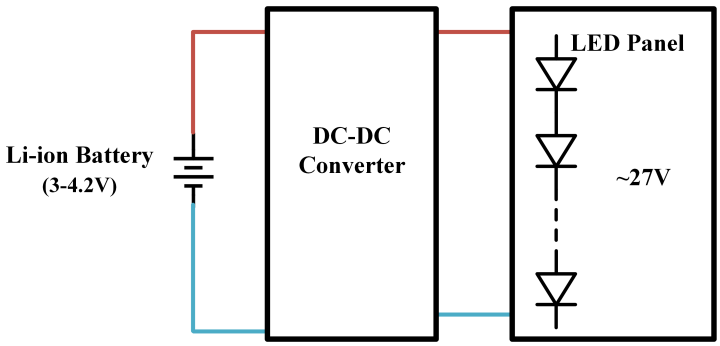

Figure 1.6: The importance of DC-DC converter in IoT device with LED panel.

for the high-efficiency step-up converter to save power as much as possible and improve the usage quality since nobody wants to charge the device very frequently. Meanwhile, the output voltage of the Li-ion battery is fluctuating during charging or discharging. The unstable input voltage problem and high-efficiency requirement ask for to design of a more suitable high VCR step-up DC-DC converter.

1.2.2 Fully Integrated VCSEL Diode Driver

Besides the traditional functions, IoT devices also begin to support more functions with the help of new modules to meet the requirements of augmented reality (AR), virtual reality (VR), and other application scenarios. Apple has implemented the light detection and ranging (LiDAR) technique in the IPad and IPhone products. With the help of the LiDAR, people can place furniture virtually with IPad in their room and check whether it is suitable and grateful. In order to realize this function, the IoT devices must have the ability to perceive distance in reality. Even though it can be calculated with a powerful algorithm based on the flat photo, the precision is not good enough for AR applications. Nowadays, additional function modules are used for this special application, and the direct time of flight system (DTOF) is one of the representatives.
The basic idea of the DTOF system is to send a pulse towards a target, receive the reflection of the pulse from the target, and then calculate the time difference between them to get the distance between the module and the target. As shown in Figure 1.7, there are two main functional parts, the transmission module and receiving module. In the apple LiDAR system, a vertical-cavity surface-emitting laser (VCSEL) diode is used as the laser generator. The VCSEL diode has several advantages as the pulse generator here, low cost, wavelength stability, manufacturability, and scalability [14]. However, as a current depended component, the VCSEL diode needs a driver to provide enough current to turn on it within the desired pulse width, which can also be found in the Figure 1.7. As for the receiver part, there is a light sensor with enough area to capture the reflection.
Since the DTOF module is integrated as small as possible to save space within the IoT devices, all parts of this module should be as small as possible and integrated components like on-chip capacitance are preferred. Meanwhile, the shorter width of the laser pulse is preferred. Since this module sends not only several but numerous pulses during one measure, the short width

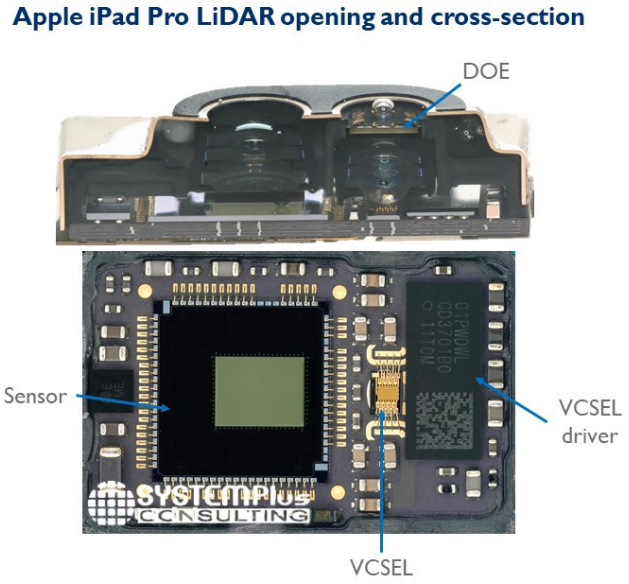

Figure 1.7: Apple's promotion of DTOF[3].

of the laser pulse saves total working time to get the average result based on the same number of pulses. In other words, a short-width laser pulse saves the working time of the system and saves power at the same time. However, owing to the parasite of the VCSEL, the VCSEL diode driver should be designed carefully to turn on or turn off the diode precisely. Meanwhile, the VCSEL diode needs a high voltage to turn on it, which means the VCSEL driver should have the ability of a voltage level converter. In summary, the VCSEL driver support pulse width as short as possible and is able to converter voltage level needed in this module.

1.3 Thesis Outline

In this thesis, the content is organized as follows. Two designs are proposed to fulfill the requirements mentioned in the motivation. The first one is a high VCR hybrid step-up DC-DC converter with high inefficiency. The second one is a fully integrated VCSEL diode driver with voltage level changeability and adjustable pulse width ability. The basic principle analyses and preliminary design are discussed in Chapter 2. It contains a basic analysis of the step-up DC-DC converter and the advantages of the proposed structure. The basic idea of the proposed VCSEL diode driver is also mentioned in Chapter 2. Since the proposed structure is especially for the VCSEL diode, the design choices are also discussed based on the VCSEL diode. Chapter 3 illustrates the basic control theory of the step-up converter and the control way for the hybrid structure. The adjustable high-speed pulse width module is the control part of the VCSEL diode driver, which is analyzed in the same Chapter. The transistor-level implementations of the two proposed designs are discussed in Chapter 4. Chapter 5 shows the layout arrangement and the

post-simulation results. The advantage of proposed designs is verified within the chapter. In the last Chapter 6, the summary of the two designs is given. The conclusions and possible future works are also mentioned.

2 Basic Principle Analyses and Preliminary Design

2.1 High-Efficiency Hybrid Step-Up DC-DC converter

2.1.1 Basic Working Principle of the Step-Up DC-DC Converter

Inductor Based Boost Converter

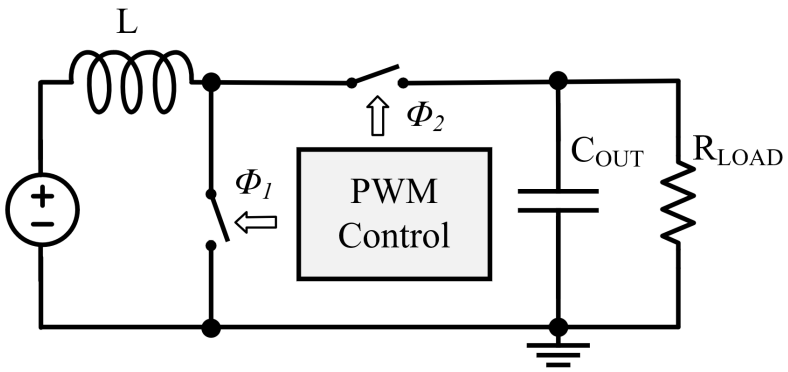

Figure 2.1: Inductor-based boost converter.

The basic structure of an inductor-based boost DC-DC converter is shown in Figure 2.1, which consists of two switches to control the inductor charging and releasing, and one inductor for energy storage. In order to analyze the principle, the small-ripple approximation method is used, which has been discussed in Erickson's book[11]. There are four assumptions:
(1) The converter already operates in the steady state. This assumption supposes the start-up stage has passed and the DC-DC converter works in the steady stage. As a result, the load current, input voltage, and output voltage can be recognized as constant values.
(2) The ripple voltage at the output point is very small compared to the steady output voltage value, which is calculated by averaging and becomes a DC value. The output voltage can be recognized as DC voltage to analyze the steady working principle of the DC-DC converter. The assumption can be written as:

$$\left|u_{ripple}\right|_{MAX} \ll U_o \tag{2.1}$$

(3) All the components of the converter obey ideal electrical characteristics and are lossless. It means all the components in the converter are modeled as ideal electrical models. All the parasitic capacitance and resistance within the power switches and inductors are ignored.
(4) The voltage and the current between the two terminals of the inductor and the capacitor follow the ideal first-order relationship. In other words, the current flowing out of the capacitor and the voltage across the inductor always obey the ideal basic equations:

$$V_L = L \cdot \frac{\mathrm{d}i_L}{\mathrm{d}t} \tag{2.2}$$

$$I_C = C \cdot \frac{\mathrm{d}v_C}{\mathrm{d}t} \tag{2.3}$$

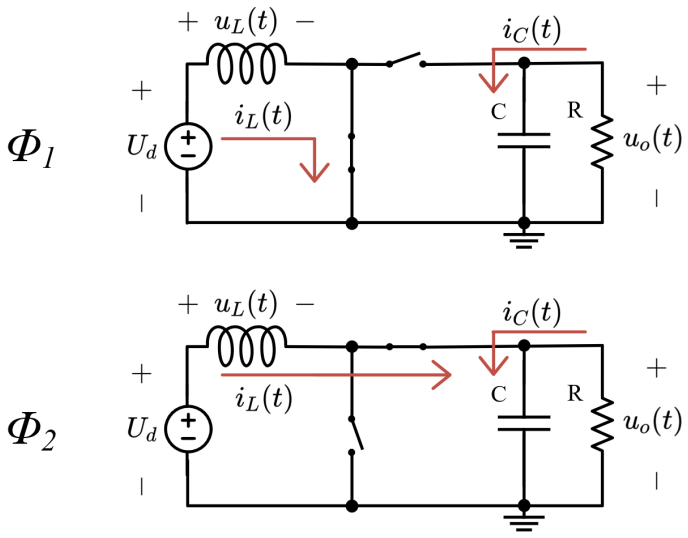

Figure 2.2: Two working phases of inductor-based boost converter.

As shown in Figure 2.2, there are two working phases. During phase one, the lower side power switch is on and another one is off. At this moment, the inductor is been charging with the input voltage U_d. the relationship between the voltage and the current can be written as:

$$u_L = U_d \tag{2.4}$$

$$i_C = -\frac{u_o}{R} \tag{2.5}$$

According to the assumption (2),$u_o \approx U_o$, the equation 2.5 can be written as:

$$i_C = -\frac{U_o}{R} \tag{2.6}$$

In the next working phase, the lower switch is off and the right terminal of the inductor is connected with the output voltage point. During this working phase, the relationship between voltage and current of the inductor can be written as:

$$u_L = U_d - u_o \tag{2.7}$$

$$i_C = I - \frac{U_o}{R} \tag{2.8}$$

According to the assumption (2),$u_o \approx U_o$ and $i_L \approx I$, the equation 2.5 can be written as:

$$u_L = U_d - U_o \tag{2.9}$$

$$i_C = I - \frac{U_o}{R} \tag{2.10}$$

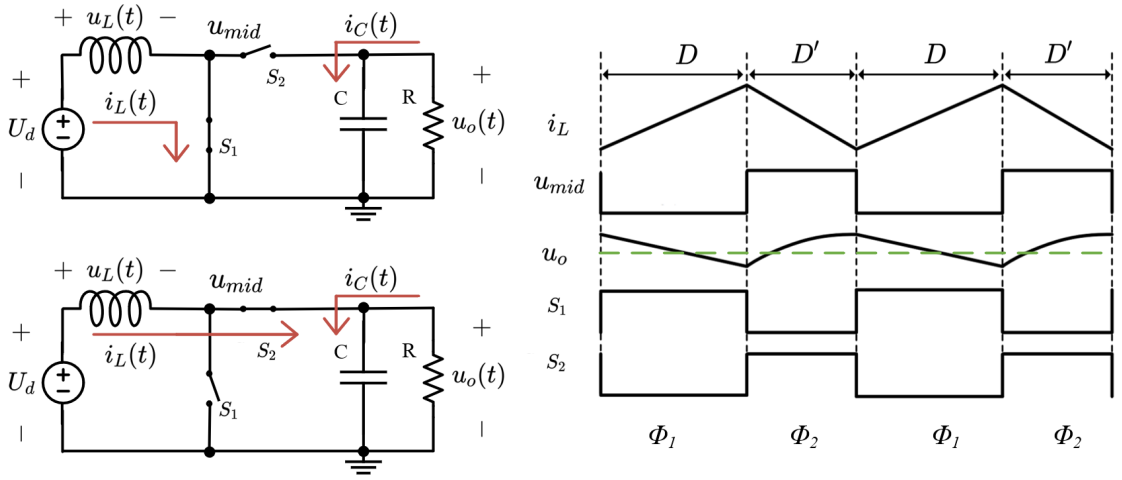

Figure 2.3: Timing diagram of main signals in the whole period.

In a complete two-phase period, T_S, the first charging phase occupies $D \cdot T_S$. The inductor releasing phase takes $D' \cdot T_S$. Since in the charging phase, the voltage across the inductor is positive and the current within the inductor is linear rising as shown in Equation 2.2. In order to maintain the balance of the energy stored in the inductor, the voltage across the inductor must be opposite to the charging phase, which means the $U_d - U_o$ is a minus value. The change of i_L is shown in the Figure 2.3 Based on the above analyses, the total voltage changing across the inductor can be written as:

$$\int_0^{T_S} u_L(t)\,\mathrm{d}t = (U_d)\,DT_s + (U_d - U_o)\,D'T_s \tag{2.11}$$

According to the steady assumption, the left side of the Equation 2.11 should be 0, and becomes as:

$$U_d \cdot \left(D + D'\right) - U_o D' = 0 \tag{2.12}$$

And with relationship between two phases, $D + D' = 1$, the equation becomes:

$$U_o = \frac{U_d}{D'} \tag{2.13}$$

The voltage conversion ratio of inductor-based boost converter can be written as:

$$M(D) = \frac{U_o}{U_d} = \frac{1}{D'} = \frac{1}{1-D} \tag{2.14}$$

According to Equation 2.14, the output voltage of the boost converter becomes input voltage when D equals to 0. The reason for this is obvious when D equals to 0, the lower switch S_1 is always off and the two terminals of the inductor are connecting to the input and output points. Meanwhile, when D closes to 1, the voltage conversion ratio will become infinitely large from the equation view. However, this is only possible if all the assumptions are achieved. In the real design, the losses will be the majority part of total input energy when D closes to 1. In other words, the infinite large output voltage can't be achieved in the real design.
After the discussion of DC voltage within the inductor, the DC current part will be illustrated. In the first charging phase, the output current will be provided by the output capacitor C_{LOAD}. In the inductor releasing phase, the current flows from the inductor providing the output current and charging the output capacitor at the same time. Therefore, the overall charge change within the whole switching period can be written as:

$$\int_0^{T_S} i_C(t)\,\mathrm{d}t = \left(-\frac{U_o}{R}\right) DT_S + \left(I - \frac{U_o}{R}\right) D'T_S \tag{2.15}$$

Use the steady assumption again, the right side of the Equation 2.15 equals 0 and can be simplified as:

$$-\frac{U_o}{R} \cdot \left(D + D'\right) + ID' = 0 \tag{2.16}$$

And use $D + D' = 1$ again, the DC current of the inductor can be calculated as:

$$I = \frac{U_o}{D'R} \tag{2.17}$$

Using Equation 2.13, the U_o can be replaced with U_d:

$$I = \frac{U_d}{D'^2 R} \tag{2.18}$$

When D' goes to 0, not only the output voltage increases dramatically, but also the current. Besides the two important DC values, the ripple current of the inductor is also worth illustrating. Based on the Equation 2.2, the slope of the inductor current in the charging phase is:

$$\frac{\mathrm{d}i_L(t)}{\mathrm{d}t} = \frac{u_L(t)}{L} = \frac{U_d}{L} \tag{2.19}$$

In the releasing phase, the slope is:

$$\frac{\mathrm{d}i_L(t)}{\mathrm{d}t} = \frac{u_L(t)}{L} = \frac{U_d - U_o}{L} \tag{2.20}$$

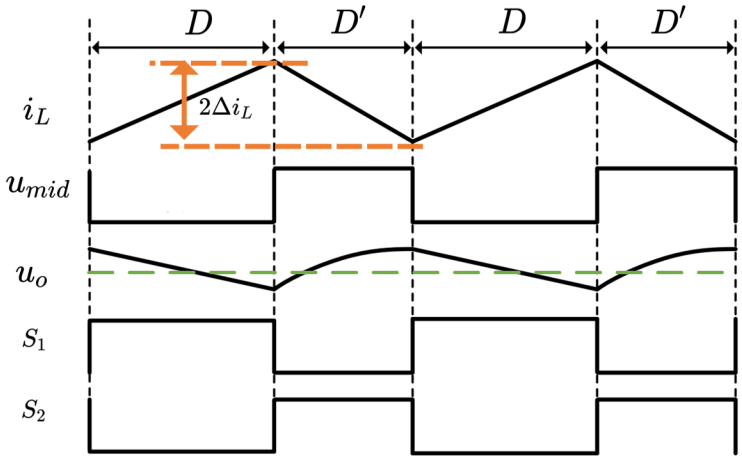

Figure 2.4: Current ripple within the inductor.

At the beginning of the charging phase, the current is the minimum value during the whole period. The total variance of the ripple current is $2\Delta i_L$ as shown in the Figure 2.4. Its specific value of it can be calculated as:

$$2\Delta i_L = \frac{U_d}{L} D T_S \tag{2.21}$$

$$\Delta i_L = \frac{U_d}{2L} D T_S \tag{2.22}$$

In the same way, the output voltage ripple can be calculated. the voltage slope of the capacitor in the first phase:

$$\frac{\mathrm{d}u_C(t)}{\mathrm{d}t} = \frac{i_C(t)}{C} = \frac{-U_o}{RC} \tag{2.23}$$

In the second phase, the voltage slope is:

$$\frac{\mathrm{d}u_C(t)}{\mathrm{d}t} = \frac{i_C(t)}{C} = \frac{I}{C} - \frac{-U_o}{RC} \tag{2.24}$$

In the first switching phase, the total voltage change across the capacitor $-2\Delta u_o$ can be written as:

$$-2\Delta u_o = -\frac{U_o}{RC} D T_S \tag{2.25}$$

$$\Delta u_o = \frac{U_o}{2RC} D T_S \tag{2.26}$$

The ripple current of the inductor helps to choose the value of the inductor and the ripple voltage of the capacitor helps to select the right value of the capacitor.

Switched-Capacitor Step-Up Converter

Unlike the inductor-based boost converter, the switched-capacitor step-up converter stores the charge in the capacitor and builds the voltage across the capacitor. With the help of switching, the voltage across the capacitor can be added between the input voltage and the output voltage, which results in the step-up behavior. The basic schematic of a series-parallel switched-capacitor DC-DC converter is as shown in Figure 2.5.

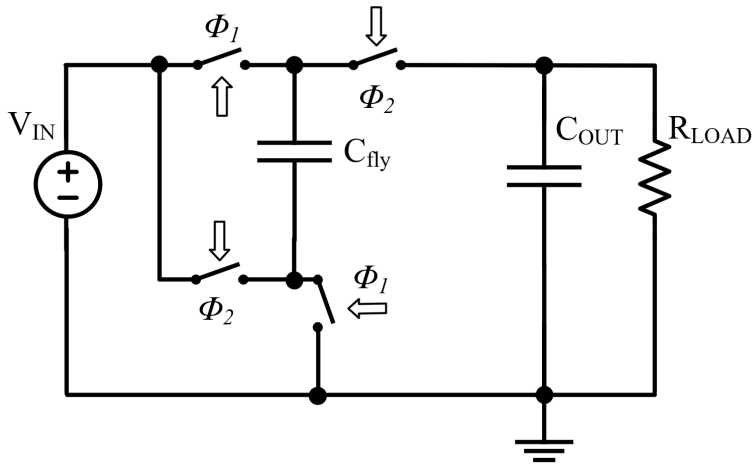

Figure 2.5: Basic step-up switched-capacitor DC-DC converter.

The two working phases are shown in Figure 2.6. In phase 1, the C_{fly} is directly connecting with the input voltage and the ground. In the ideal situation, when the converter works in the steady state, the voltage across the C_{fly} will be the input voltage V_{IN}, which shows in Equation 2.27. At this moment, the output current is provided with the output capacitor C_{OUT}. The current flows are marked in Figure 2.6.

$$U_{C_{fly}} = U_{IN} \tag{2.27}$$

In the second phase, the C_{fly} is connecting between the input voltage and the output voltage. In other words, the C_{fly} is series with the input voltage now. Using the steady assumption again, the output voltage can be written as:

$$U_o = U_{IN} + U_{C_{fly}} = 2U_{IN} \tag{2.28}$$

Therefore, the ideal voltage conversion ratio will be 2. Meanwhile, unlike the inductor-based boost converter, the topology of the switched-capacitor DC-DC converter not only has a single kind. Moreover, as shown in the above analyses, the ideal VCR of the converter fully depends on the topology. The analyses must be based on the specific topology and get the corresponding results. In the development history of the switched-capacitor converter, there are several outstanding and representative structures, series-parallel [15], the Dickson[7],the Fibonacci[16] and the successive approximation register (SAR) converter [17]. Different topology has their own advantages and some drawbacks. Since the characteristics brought by topology are mainly related to losses mechanism, it will be analyzed in the next section.

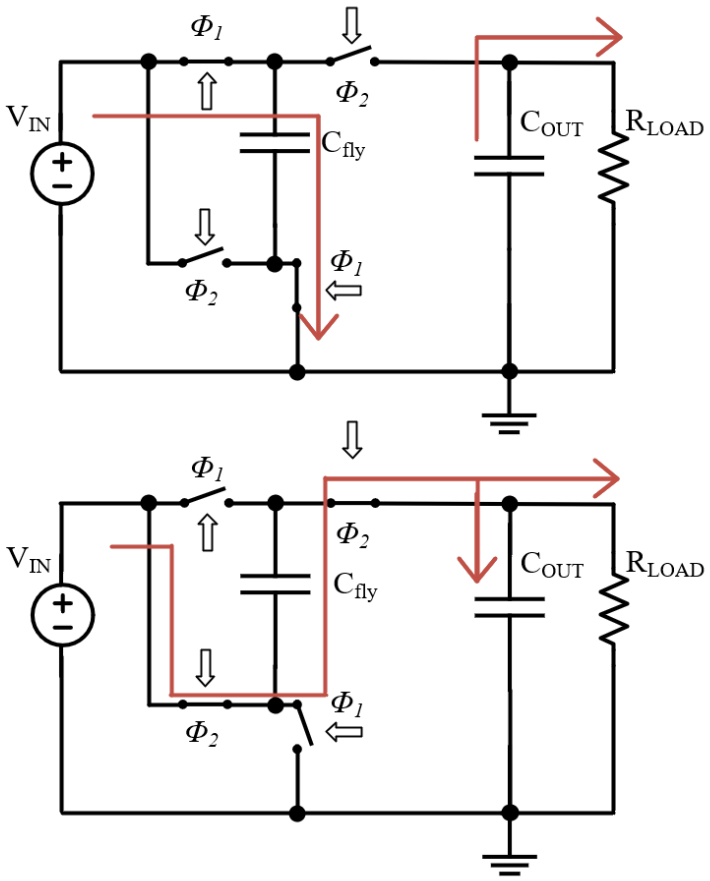

Figure 2.6: Two working phases of the series-parallel switched-capacitor DC-DC converter.

2.1.2 Power Loss Mechanism and Efficiency

Firstly, the losses mechanism of the inductor-based boost converter is been analyzed. The power losses in an inductor-based boost converter mainly consist of two parts, conduction losses P_{cond} and switching losses $P_{switching}$. Both of them are closely related to the sizes of switch devices. The P_{cond} is determined by the following equation [11]:

$$P_{cond} = i_{IND,RMS}^2 \cdot (R_{IND} + D \cdot R_{LS} + (1-D) \cdot R_{HS}) \tag{2.29}$$

where $i_{IND,RMS}$ is the RMS current value of the inductor, R_{IND} is the DC resistance of the inductor, R_{LS} and R_{HS} are the conducting resistances of two switches, and D is the duty of the low side switch.

The $P_{switching}$ mainly consists of three parts, transition losses P_{trans}, gate losses P_{gate} and inductor's magnetic losses P_{core} [18]. P_{trans} is the power losses during the stage change between on and off. The losses can be modeled as the following equation:

$$P_{trans} = 0.5 \cdot F_{SW} \cdot V_{OUT} \cdot I_L(t_1 + t_2) \tag{2.30}$$

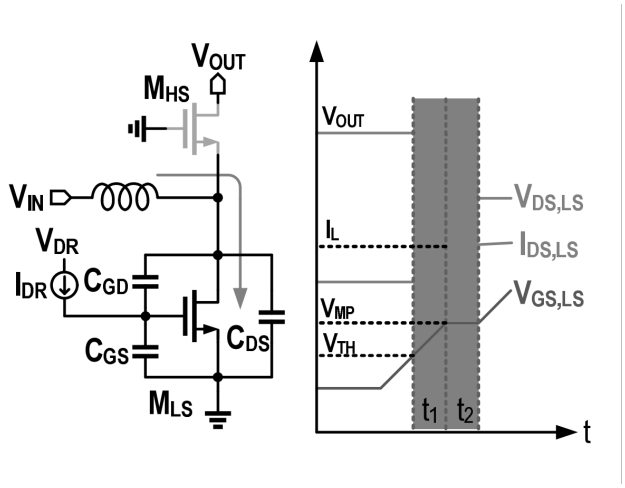

Figure 2.7: Transition loss modeling for turn-on event of low-side switch[4].

where F_{SW} is the switching frequency and V_{OUT} is the output voltage of the converter. t_1 and t_2 are determined by the gate charging current I_{DR}, C_{GS} and C_{GD} mentioned in [19].
The P_{gate} is the power loss when charging or releasing the gate capacitor of the power switches, which is mainly related to the size of the power switches. Therefore, it can be modeled as the following equation:

$$P_{gate} = C_{gate} \cdot V_{IN}^2 \cdot F_{SW} \tag{2.31}$$

The last part of the switching power losses is coming from the magnetic losses of the inductor, P_{core}. The core losses relate to the structure of the inductor and usually increase with the lower height of the inductor. According to the Steinmetz expression [20], the P_{core} can be modeled as:

$$P_{gate} = K_{FIT} \cdot F_{SW}^{\alpha} \cdot (\Delta I_{IND})^{\beta} \tag{2.32}$$

In the equation, K_{FIT}, α, and β are fitting parameters, which are influenced by the structure of the inductor and the values provided by the manufacturers. Therefore, only two parts of the boost converter will influence the P_{core}, switching frequency F_{SW} and the ripple current within the inductor ΔI_{IND}. Interestingly, with other design parameters fixed, in order to decrease the ΔI_{IND}, larger F_{SW} must be used, which will counter the improvement of the P_{core}. The balance between them must be taken into consideration.
Even though there are also other losses such as the losses during the dead time, the dominating power losses are all mentioned above. From the basic analysis, some intuitions can be gotten in the design flow. In order to improve the efficiency of a DC-DC converter, the sum of the P_{cond} and $P_{switching}$ must be decreased. However, for the power devices with the same voltage stress tolerance, the sum of the P_{cond} and $P_{switching}$ can not be reduced further, because the P_{cond} is always increasing while reducing the $P_{switching}$, since smaller width of power devices results in larger conducting resistance. Therefore, power switches with lower voltage-stress tolerance are preferred in high-efficiency designs to reduce the sum of the P_{cond} and $P_{switching}$. However, if the design is made toward a high VCR requirement, only large voltage-stress tolerance power

switches could be used, which will reduce the efficiency performance of the boost converter. The conclusion can also be shown in Figure 2.8.

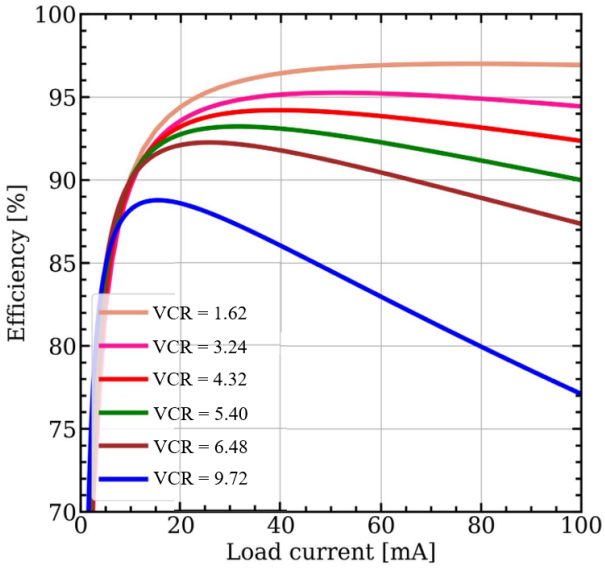

Figure 2.8: LED-driver efficiency versus load current for different VCR and fixed V_{IN} = 3.7 V.[4].

The switched-capacitor DC-DC converter also faces switching losses which have the same losses mechanism mentioned above. However, unlike the losses in the inductor can be analyzed as the conduction losses, the losses within the switched-capacitor DC-DC converter are called charge-sharing Losses. Its basic idea of it can be analyzed from the energy view. Suppose there is a capacitor C that has the voltage V_C across it as the initial condition just as shown in Figure 2.9. When the ideal switch is turned on, the voltage across the capacitor C becomes $V_C + \Delta V$. Therefore, the energy change of the capacitor ΔE is:

$$\Delta E = C\frac{(V_C + \Delta V)^2 - V_C^2}{2} \tag{2.33}$$

Meanwhile, the energy provided from the supply E_{supply} is:

$$E_{supply} = C\Delta V\,(V_C + \Delta V) \tag{2.34}$$

Now compare the E_{supply} with theΔE, it can be found there is power losses, and the specific value of it is:

$$E_{CS} = C\frac{\Delta V^2}{2} \tag{2.35}$$

Since the loss E_{CS} appears during the capacitor charging, it is typically referred to as a charge-sharing loss. Therefore, in order to achieve high efficiency, the ripple voltage across the capacitor must be as small as possible.

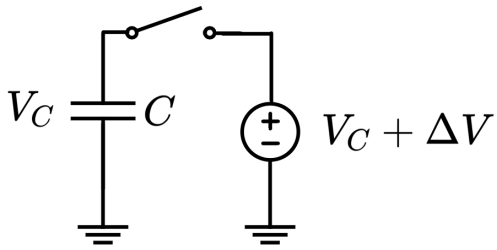

Figure 2.9: Charge-sharing losses example.

As mentioned in the last subsection, the topology of the switched-capacitor DC-DC converter varies and has some outstanding representative kinds. Unlike the flexible VCR range of the inductor-based boost converter, for a fixed topology switched-capacitor, the ideal VCR is also fixed. The ideal VCR is determined by the number of capacitors and phases in a topology. Under the general two-phase controlled switched-capacitor converters, the ideal VCR can be marked as:

$$idealVCR = \frac{P}{Q} \tag{2.36}$$

Both the P and Q are strictly positive integers. Moreover, they are coprime. The Q and P obey the following equation:

$$P, Q \leq F_{k+2} \tag{2.37}$$

where the F_i is the ith Fibonacci number and k is the number of capacitors[21]. If more working phases are involved, the possible values of P and Q are:

$$P, Q \leq F_{k+2}^{(p)} \tag{2.38}$$

The basic relationship between the components of the converter and the topology has been illustrated above. There is a gap between the ideal VCR and the true VCR. Therefore, there is an output impedance is used as modeling[21].
As shown in Figure 2.10, the Switched-capacitor converter consists of two parts. The first part is an ideal transformer, which converts the V_{IN} to the $V_{IN} \cdot idealVCR$. Meanwhile output impedance R_{OUT} is connecting the output terminal of the converter and the ideal transformer. There will be a voltage drop when I_{OUT} flows through the R_{OUT}. After including the R_{OUT}, the V_{OUT} can be written as:

$$V_{OUT} = idealVCR \cdot V_{IN} - I_{OUT} R_{OUT} \tag{2.39}$$

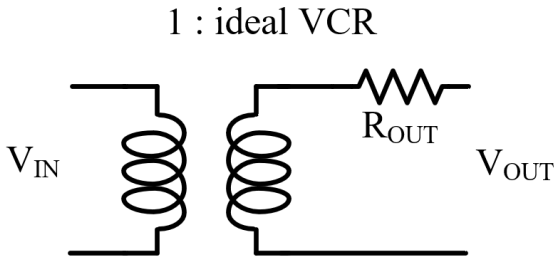

Figure 2.10: Switched-capacitor converter output impedance model.

The model of R_{OUT} is necessary to complete the analyses of the VCR including the output impedance. Since the impedance of the capacitor is related to the frequency, which is the switching frequency in the converter scenario, they are two fixed boundaries are defined, slow-switching limit (SSL) and fast-switching limit (FSL)[22]. The R_{OUT} can be modeled with the help of SSL and FSL as shown in Figure 2.11.

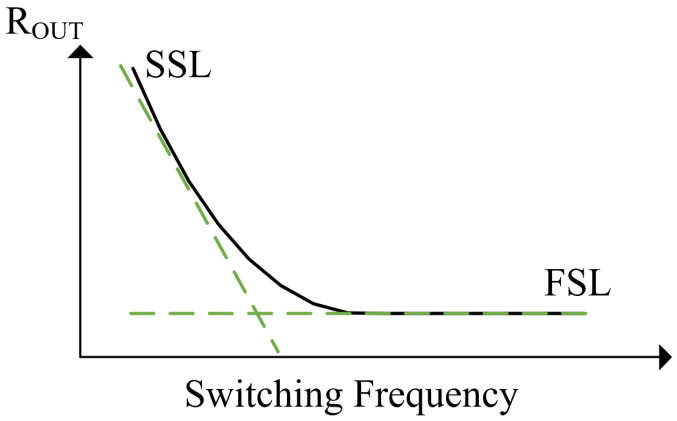

Figure 2.11: Output impedance versus switching frequency.

In the SSL situation, all the capacitors within the converter are charged or released fully. The time constant of each capacitor charging or releasing phase are ignorable compared to the phase duration time.
To quantitatively analyze the output impedance under SSL $R_{OUT,SSL}$, the charge-share losses of all the capacitors should be determined firstly[22].

$$P_{SSL} = \frac{F_{SW} q_{out}^2}{2} \sum_{caps,i} \sum_{phases,j} \frac{a_{c,ij}^2}{C_i} \tag{2.40}$$

Where C_i is the ith capacitor and q_{out} is the total charge transferred to the output in a whole switching period. Meanwhile, since the charge flows in the different topologies are different, $a_{c,ij}$ are used to include the topology information and it is:

$$a_{c,ij} = \frac{q_{c,ij}}{q_{out}} \tag{2.41}$$

Where $q_{c,ij}$ represents the charge change of the ith capacitor in the phase j. Meanwhile, the P_{SSL} can be written as:

$$P_{SSL} = R_{OUT_{SSL}} I_{OUT}^2 \tag{2.42}$$

Where I_{OUT} is:

$$I_{OUT} = F_{SW} \cdot q_{out} \tag{2.43}$$

Therefore, the Equation 2.40 becomes:

$$R_{OUT_{SSL}} = \sum_{caps,i} \sum_{phases,j} \frac{a_{c,ij}^2}{2F_{SW}C_i} \tag{2.44}$$

In a general two-phase converter, since the charge change of the capacitor during the whole period should be zero, the $R_{OUT_{SSL}}$ is:

$$R_{OUT_{SSL}} = \sum_{caps,i} \frac{a_{c,i}^2}{F_{SW}C_i} \tag{2.45}$$

In the Equation 2.45 topology information in both parts of $a_{c,i}$ and C_i. In order to directly reflect the topology influence, the topological factor K_C is used.

$$K_C = \sum_{caps,i} \sum_{phases,j} \frac{a_{c,ij}^2 C_{tot}}{2C_i} \tag{2.46}$$

Now the Equation 2.45 becomes:

$$R_{OUT_{SSL}} = \frac{K_C}{F_{SW}C_{tot}} \tag{2.47}$$

When the switching frequency is high enough, the current flows can be regarded as constant. As a result, the main power loss is determined by the conductance of the power switches.

$$P_{FSL} = D_j I_{R,ij}^2 R_i \tag{2.48}$$

Where D_j is the duty cycle of the phase j. In the common two-phase converter, the D_j equals to 0.5. R_i is the resistance of the ith power switch. The current flow across the ith switch during the jth phase is represented by $I_{R,ij}$. Just as the $a_{c,ij}$ mentioned in the Equation 2.40, the$a_{R,ij}$ can also be used here and get:

$$a_{R,ij} = \frac{q_{R,ij}}{q_{out}} \tag{2.49}$$

Where, $q_{R,ij}$ is the charge flows across the ith switch during the jth phase. Then we have the relationship between the charge and current:

$$F_{SW} q_{R,ij} = D_j I_{R,ij} \tag{2.50}$$

Therefore, the output impedance of the converter under FSL limit is[22]:

$$R_{FSL} = \sum_{switches,i} \sum_{phases,j} \frac{a_{R,ij}^2 R_i}{D_j} \tag{2.51}$$

The simplified result when two-phase is used is:

$$R_{FSL} = \sum_{switches,i} 2a_{R,ij}^2 R_i \tag{2.52}$$

With the same idea to use one parameter to reflect the topology information, parameter K_S is used:

$$K_S = \sum_{switches,i} \sum_{phases,j} \frac{a_{R,ij}^2 R_i}{D_j R_{tot}} \tag{2.53}$$

And the simplified result is:

$$R_{FSL} = K_S R_{tot} \tag{2.54}$$

The most common method to model the output impedance of the switched-capacitor converter is the Euclidean norm.

$$R_{OUT} \approx \sqrt{R_{SSL}^2 + R_{FSL}^2} \tag{2.55}$$

The result of the output impedance versus the switching frequency is shown in Figure 2.11.

2.1.3 Hybrid DC-DC Converter

After illustrating the basic ideas of the inductor-based converter and the switched-capacitor converter we can find some intuitions about them. The four important characteristics have been listed in Table 2.1.

In order to drive the LCD panel, the current flows from the battery is around hundreds of mA. Therefore, the value of the inductor must large enough to control the ripple current within it, which is around μH. The inductor of this size level is impossible to fully integrate on-chip With normally integrated circuit technology. As a result, it becomes a drawback of the inductor-based converter. On the contrary, it's easy to integrate capacitors on the chip, which becomes the advantage of the switched-capacitor converter.

In terms of efficiency under high VCR, the inductor-based boost converter also has problems. Just like what has been mentioned in Figure 2.8, in order to realize high VCR, the power switches must have the ability to face high voltage stress around output voltage. As a result

Table 2.1: Inductor-based converter versus switched-capacitor converter.

	Inductor based DC-DC converter	Switched-capacitor DC-DC converter
Fully integrated on chip	×	√
High efficiency with fixed large VCR	×	√
No charge sharing loss	√	×
High efficiency with different input voltage	√	×

the $P_{switching}$ gradually becomes the dominating loss and reduces the total efficiency. Owning to the flexible topology strategy, the switched-capacitor can arrange the whole voltage gap between the input and output to different parts of the converter. Therefore, high efficiency is also possible to be achieved under high VCR.

In the principle analyses, it can be found that power-sharing loss plays an important part in the switched-capacitor efficiency, especially under SSL. Even though there are also losses generated from other parts of the inductor-based converter besides the power switches, they are not the dominating part. In order to minimize the charge sharing loss, people have done a lot of work and used many methods. However, owing to the working principle, it can only be reduced rather than eliminated. In this aspect, the inductor-based converter has its own advantage with the intrinsic working principle.

Since the working principle of the inductor-based converter has D in its VCR, It has the ability to adjust VCR by modifying D without changing the topology and the components. In other words, within the suitable VCR range, the inductor-based converter keeps relatively stable high efficiency. This characteristic is hard to achieve with a switched-capacitor converter. As mentioned above, one topology determines one ideal VCR, which is also the best working point. Then, the pulse width modulation is not possible to help the switched-capacitor converter to change VCR. There are generally several ways to control the switched-capacitor converter to realize different VCR, which will be discussed later. However, whatever the methods are used to change the VCR, the converter will work away from the best efficiency point. In other words, the cost is the power. Therefore, the switched-capacitor converter has bad performance when the VCR is changing during the working.

It is quite reasonable that people want to combine them to have more advantages and fewer drawbacks. People have already done a lot of work based on using them together. The basic idea is to use a switched-capacitor converter facing a large but fixed VCR and use an inductor-based converter facing a small but changing VCR. Based on this simple idea, both the step-up and step-down can be designed in the hybrid mode.

For the step-down scenarios, the switched-capacitor converter parts are usually the first stage, and the inductor-based stage is the second stage. As shown in Figure 2.12, the author proposes a hybrid structure to achieve a step-down converter with high VCR and high efficiency of around

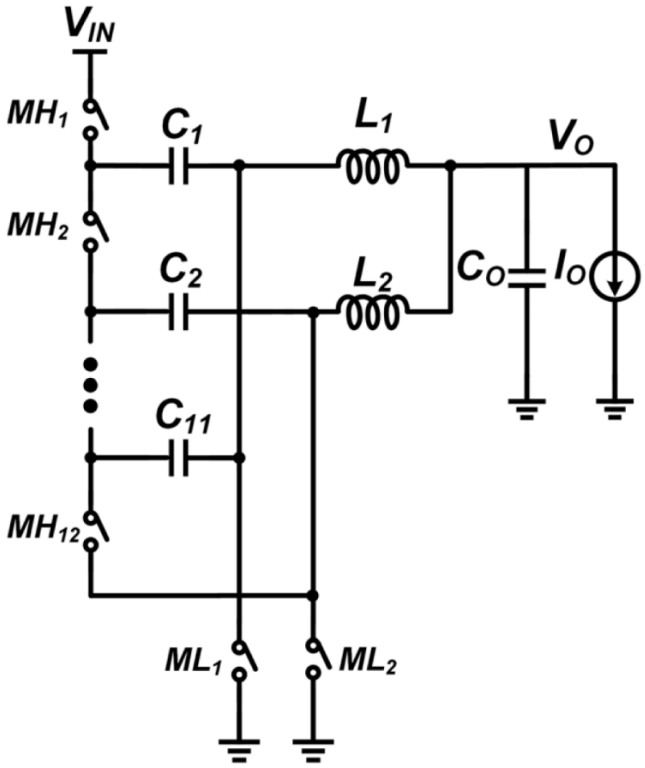

Figure 2.12: A 12-level series-capacitor 48-1 V DC-DC converter with on-chip switch and GaN hybrid power conversion[5].

90%. It is worth noting that the 12-level series-capacitor part converts input voltage from $48V$ to $4V$, which means the majority of VCR has been achieved in this stage. And then two inductors convert the $4V$ voltage to the target $1V$ under complex phase control.
Since the first series-capacitor stage is always facing a stable input voltage, it is easy to keep the switched-capacitor stage working on the best performance point. Meanwhile, when the load current is changing, the current flows out from the switched-capacitor stage is also changing. As a result, the output voltage of that stage will decrease with increasing load current. The advantage of the second inductor-based stage perfectly works there. Only pulse width modulation needs to be used in the second stage and get a stable $1V$ output voltage. Since the VCR change in the second stage will not influence its efficiency dramatically, this hybrid structure successfully separates the high VCR part and adjustable VCR part and achieves high-efficiency performance.
In terms of the step-up scenarios, the two stages are often placed in the opposite direction as the step-down structure. Huang proposes a Hybrid converter with cross-connected C_F[6] as shown in the figure 2.13. Even though the connection between the inductor-based stage and the switched-capacitor stage is unusual in the cross-connected method, the basic idea is the same. The input voltage is boosted with two inductors working in different phases, which will help to limit the ripple with only one inductor and increase the efficiency performance. Then the

voltage after boosting will be stored in the flying capacitors and added to the middle voltage at output phases to get the final output voltage. Since the middle voltage is generated by the inductor-based stage, the input voltage of the switched-capacitor stage is relatively stable, which helps to keep it at the best performance point. With the help of the flying capacitors, the stress voltage faced by the power switching in the first stage is decreased, which helps to improve the performance of the first stage with low-stress-voltage power switches.

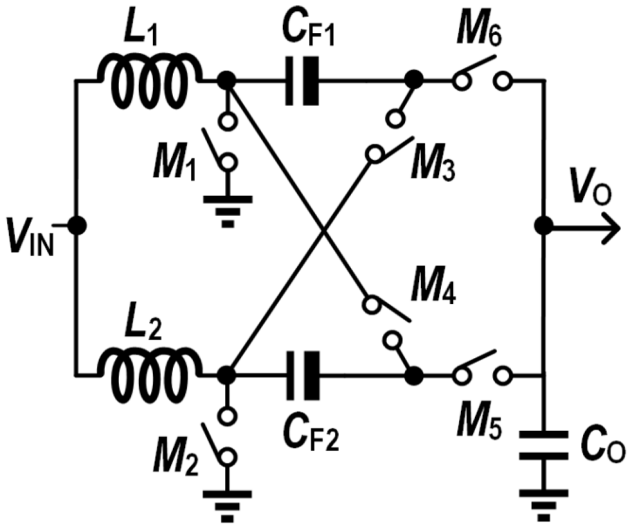

Figure 2.13: Hybrid converter with cross-connected C_F [6].

Besides macro principle perspective analysis, there is one key advantage within the hybrid structure, soft-charging. In order to illustrate it more intuitively, two ideal capacitors and one ideal inductor are used as shown in Figure 2.14. Suppose both of the capacitors have the initial voltage across them and the left one is larger. When the ideal switch is closed, the loop is closed and there is current flow since the potential difference. Based on the ideal relationship between the voltage and current of inductor and capacitor:

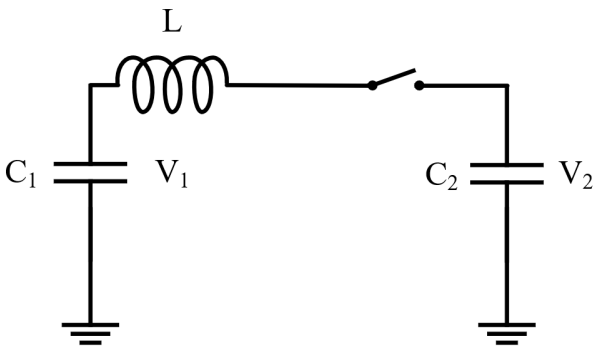

Figure 2.14: Soft charging illustration.

$$V_L(t) = L\frac{\mathrm{d}i_L(t)}{\mathrm{d}t} \tag{2.56}$$

Where i_L is the current that flows from the left capacitor to the right capacitor.

$$C\frac{\mathrm{d}v_1(t)}{\mathrm{d}t} = -i_L(t) \tag{2.57}$$

$$C\frac{\mathrm{d}v_2(t)}{\mathrm{d}t} = i_L(t) \tag{2.58}$$

And using the KVL law, the equation can be get from the closed loop:

$$V_L = v_1(t) - v_2(t) \tag{2.59}$$

In order to get the equation to describe the voltage and current, the Laplace transform is used here.

$$C[sV_1(s) - V_1] - C[sV_2(s) - V_2] = -2I_L(s) \tag{2.60}$$

$$V_1(s) - V_2(s) = sL \cdot I_L(s) \tag{2.61}$$

In order to use a simple calculation to show the basic principle, the initial value of V_1 is 1, and V_2 is 0. Then we can get:

$$I_L(s) = \frac{1}{s^2LC + 2} \tag{2.62}$$

After using the inverse Laplace transform:

$$i_L(t) = \frac{1}{\omega L}\sin\omega t \tag{2.63}$$

Where ω is the resonant frequency, the value is:

$$\omega = \sqrt{\frac{2}{LC}} \tag{2.64}$$

The voltage across the capacitors is:

$$V_1(t) = \frac{1}{2}(1 + \cos\omega t) \tag{2.65}$$

$$V_2(t) = \frac{1}{2}(1 - \cos\omega t) \tag{2.66}$$

Suppose C to be $1F$ and L to be $1H$, the voltage within the capacitors and the current within the inductor are as shown in Figure 2.15.
The total energy at all the moments within the loop is:

$$E_{tot} = \frac{1}{2}C(V_1(t))^2 + \frac{1}{2}C(V_2(t))^2 + \frac{1}{2}L(I_L(t))^2 \tag{2.67}$$

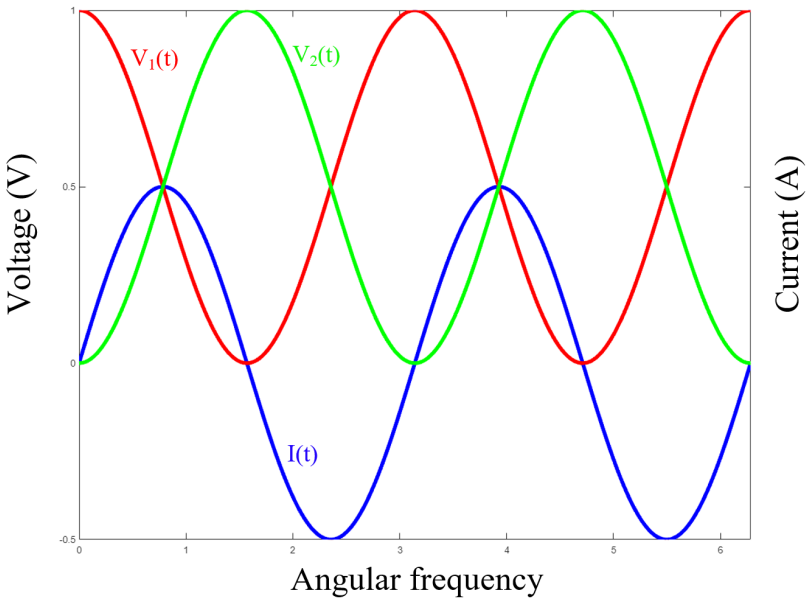

Figure 2.15: Relationship between the voltage and current within the resonant loop.

The above equation shows, that under an ideal situation, the charge share between capacitors is lossless. Since the inductor prevents the instance charge change within the loop, the charge is stored in the inductor firstly and then flows to the low potential point. Usually, this kind of charge re-balance is referred to as soft charging, which compares with hard-charging without the inductor in the loop.

Therefore, in the hybrid structure, the appearance of the inductor is helping to reduce the charge share loss. Since the charge share loss dominates the SSL range, it can also be regarded as reducing the R_{SSL}. Usually, the switching frequency F_{SW} of the switched-capacitor converter is designed to be near the balance point where R_{SSL} equals R_{FSL}. There is already a detailed analysis done in the publications on the output impedance change of the switch-capacitor converter with an inductor in the loop.

In Pal's paper[4], the total output impedance is calculated with the average output power and the average load current. As shown in Figure 2.16, after including an inductor within the loop, the output impedance shows a much more fast decrease with the increase of the switching frequency. As a result, a lower switching frequency can be used to put the switched-capacitor converter at the balance point. The calculated result is also matching the principle mentioned in soft charging which the inductor reduces the charge share loss and reduces the R_{SSL} at the same switching frequency.

Meanwhile, there are lots of peaks shown in Figure 2.16. From the intuitive perspective, it is also caused by the resonant loop. As shown in Figure 2.15, unlike the two capacitors achieving stable balance after the charge sharing, the charge sharing within the resonant loop will keep going in the ideal situation. If the switching frequency is chosen unwisely, the charge will go back to the initial capacitor and there is no charge flowing into the next stage. Under this kind of bad switching frequencies, the R_{SSL} will be larger rather than lower. Therefore, it is very

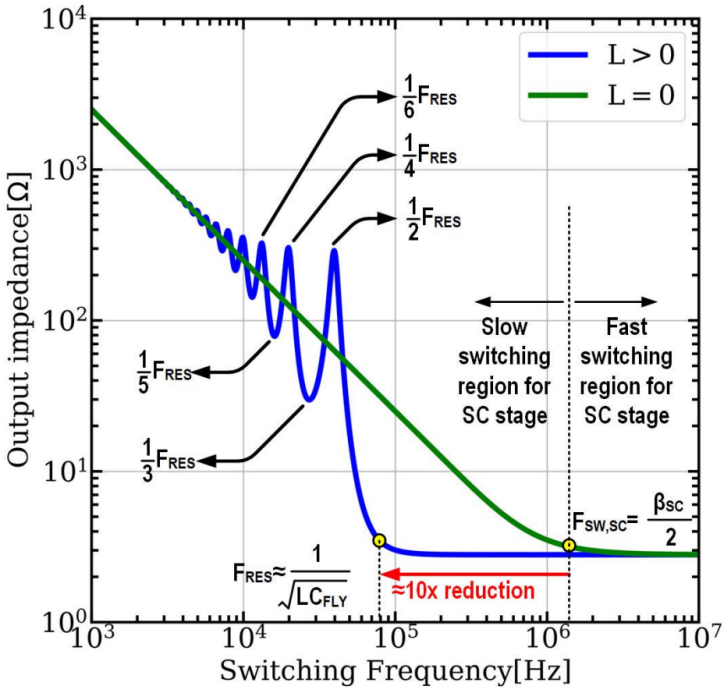

Figure 2.16: Comparison of output impedance of basic hybrid converter with that of the traditional SC converter[4].

important to choose the right switching frequency in the hybrid DC-DC converter.
In summary, the hybrid DC-DC converter is able to overcome drawbacks within the traditional inductor-based converter and the switched-capacitor converter. Meanwhile, with the resonant loop in the charging of realizing phases, the charge share loss will be reduced with the phenomenon often referred to as soft charging. However, compared with the traditional DC-DC converter, there is no complete and unified mathematical model to model all the parameters within the different hybrid structures. Therefore, the analyses must be based on each different hybrid structure, which brings difficulties to the designers. At the same time, small functional modules assist the converter and also play an important role in efficiency improving. A creative functional module designed toward a kind of hybrid converter is popular in recent years' publications.

2.1.4 Preliminary Design of the Hybrid Step-Up DC-DC Converter

As mentioned in the introduction, a high VCR DC-DC converter is needed to convert the voltage of the Li-ion battery to around $30V$ to forward bias all the diodes in the LED panel. Meanwhile, the efficiency of the converter is as high as possible to enlarge the endurance of the devices. A hybrid step-up DC-DC converter with all 5-V switches is proposed in this thesis.
The specifications of the proposed hybrid step-up DC-DC converter are shown in Table 2.2.

Table 2.2: The specifications of the hybrid DC-DC converter.

	Typical value	Range
Input voltage	3.7V	3-4.2V
Output voltage	29V	18-30V
Load current	25mA	0-100mA
VCR	7.8	6-10
Area	As small as possible	
Efficiency	As high as possible	

Since the design is for portable devices, the input voltage will be the working voltage of a lithium-ion battery. Therefore, the specification of the input voltage is based on the lithium-ion battery. Portable devices like smartphones operate between $3.0V$ and $4.2V$. When the operating voltage is lower than $2.4V$, the metal plates of the battery will be eroded, which may cause higher impedance blocking the charge flows and lower capacity. Meanwhile, when the operating voltage is larger than $4.3V$, the cycle life and capacity of the battery will be hurt. The higher voltage also causes lithium crystal growth, which may eventually result in an internal short circuit and even an explosion[23]. As mentioned in the introduction, in order to drive the LED panel, a high voltage of around $27V$ is needed. Such a high voltage generated in the portable devices can also be used to bias the Single-photon avalanche diode (SPAD), which usually appears in the receiver of the DTOF system. Based on the typical current operating range of LED panel, the typical load current is $25mA$ and support up to $100mA$. The typical VCR is 7.8 when the input voltage and the output voltage are both the typical values. The maxim VCR is gotten with the lowest input voltage $3V$ and the highest output voltage $30V$. As for the area and efficiency, the converter is designed to be as good as possible.

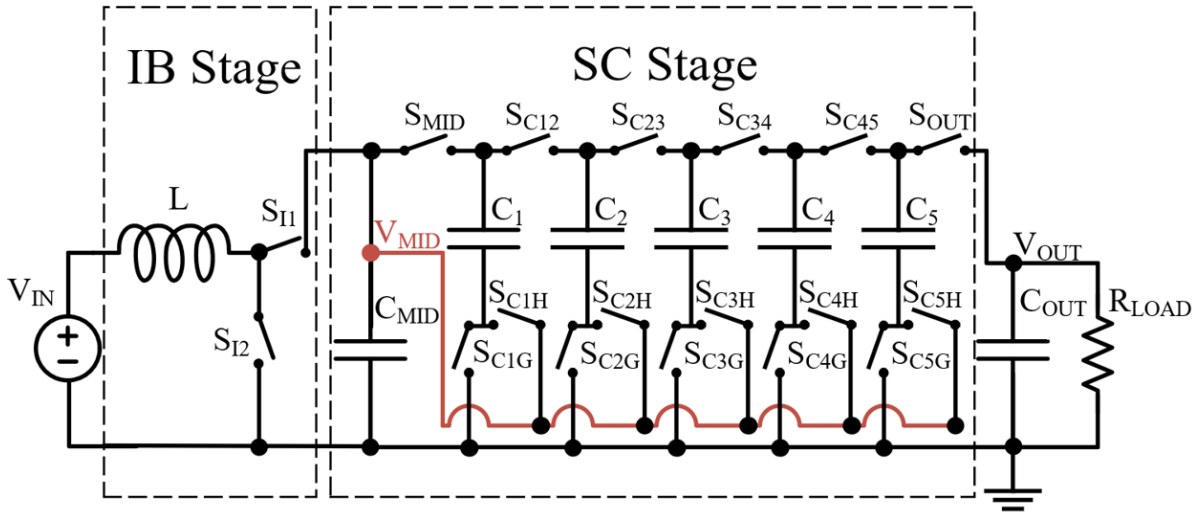

Figure 2.17: Proposed hybrid step-up DC-DC converter.

The proposed hybrid step-up DC-DC converter is as shown in Figure 2.17, which consists of

two parts. The first part is the inductor based and the second part is the switched-capacitor based on Dickson topology. Under the typical working condition, the first stage will converter input voltage from $3.7V$ to the $5V$ at the V_{MID}. Then the $5V$ voltage will be converted with 6x to near $30V$ by the second stage.
In order to achieve high efficiency as high as possible, two main methods are used in this design. The first one is the soft charging technique and the second one is full with 5-V switches. The soft charging is realized with suitable phase control. As shown in Figure 2.18, the switching frequency of the switched-capacitor part is designed to be half of the switching frequency of the inductor-based boost stage. The key idea here is to put switching moments of the switched-capacitor stage during the inductor realizing phases, which are the Φ_2 and Φ_3 shown in Figure 2.18. As mentioned in the soft charging principle, the inductor can have energy during the sudden charge balance process. Making sure the inductor is in the charging loop during the switching moments of the switched-capacitor stage will reduce the charge charging loss and reduce the R_{SSL} in the second stage. As a result, a lower switching frequency can be used in the second stage to achieve the same output impedance.

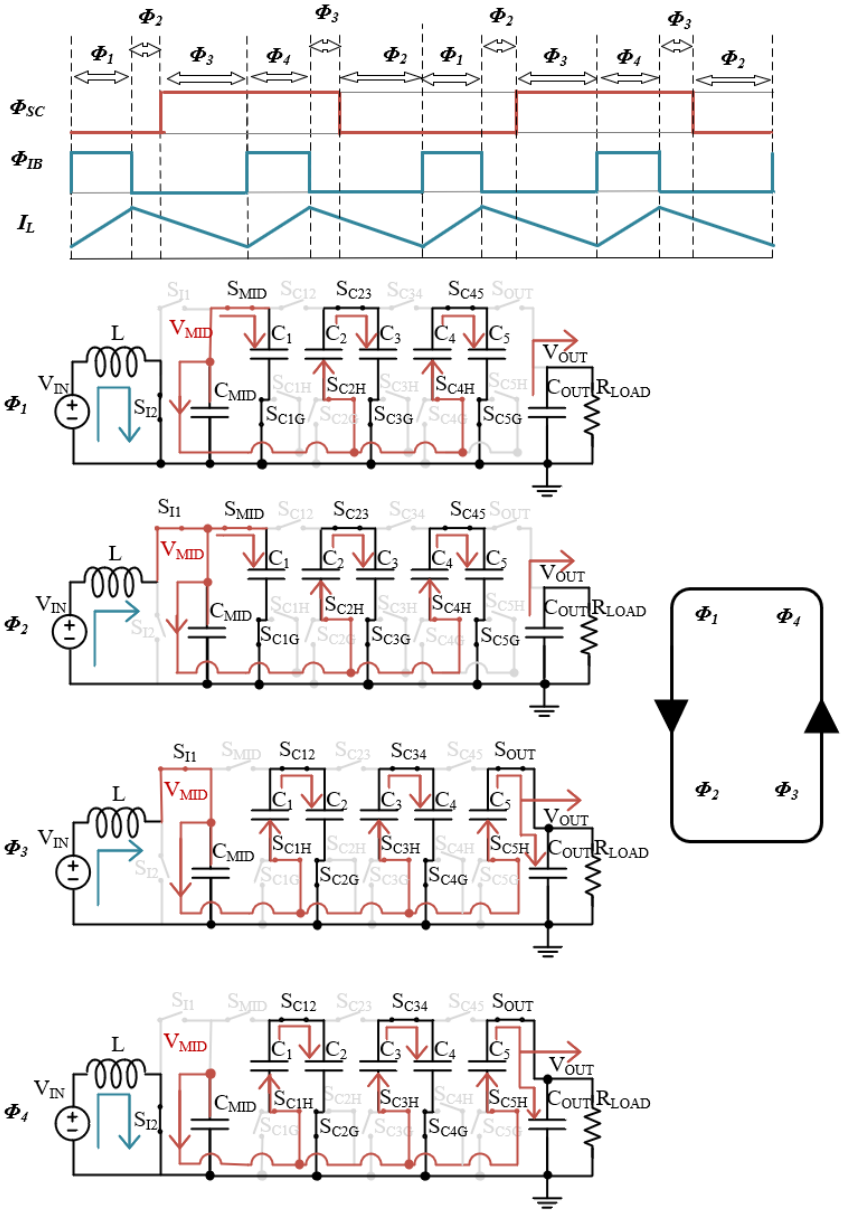

Figure 2.18: Operation principle of the proposed hybrid converter.

Another efficiency improvement came from the small power switches. Take the example under TSMC 180BCD technology. In order to achieve the same on resistance R_{on}, the relationship between gate capacitor C_{gg} of n-channel power devices with $36-V$ voltage stress and $5-V$ stress voltage is:

$$C_{gg_{36V}} = 5.3 \cdot C_{gg_{5V}} \tag{2.68}$$

According to the Equation 2.31, with other parameters in the same condition, the P_{gate}:

$$P_{gate_{36V}} = 5.3 \cdot P_{gate_{5V}} \tag{2.69}$$

At the same time, not only the gate capacitor C_{gg} is dramatically increasing with the stress ability, but the C_{GS} and C_{GD} will also increase. The larger parasitic capacitors lead t_1 and t_2 increasing in the Equation 2.30 and results a larger transition losses. Therefore, in this design, only $5-V$ devices are used to achieve such a high VCR can lead to better efficient performance. In order to separate the whole output voltage into $5V$ pieces which can be handled by $5-V$ devices, the Dickson topology is implemented as the second stage.
As shown in Figure 2.19, the original Dickson topology only consists of a diode and capacitor within the core part[7]. Under an ideal working process, the bottom plates of the capacitors are controlled to have the same high or low voltage with Φ_1 or Φ_2. When Φ_1 goes low, the capacitors with Φ_1 as their bottom voltage will be charged. The first capacitor from left to right is charged by the input voltage but the later capacitors with Φ_1 as their bottom voltage will be charged by their front capacitor with Φ_2 as their bottom voltage. During the next phases, the charging and releasing logic is reversed. As a result, the capacitors will be charged to 1x V_{IN}, 2x V_{IN}, 3x V_{IN} and 4x V_{IN}. The final output voltage will be 5xV_{IN}. Meanwhile, the stress voltage faced by all the diodes is equal to 2xV_{IN}, even though connecting more stages to get a higher output voltage.

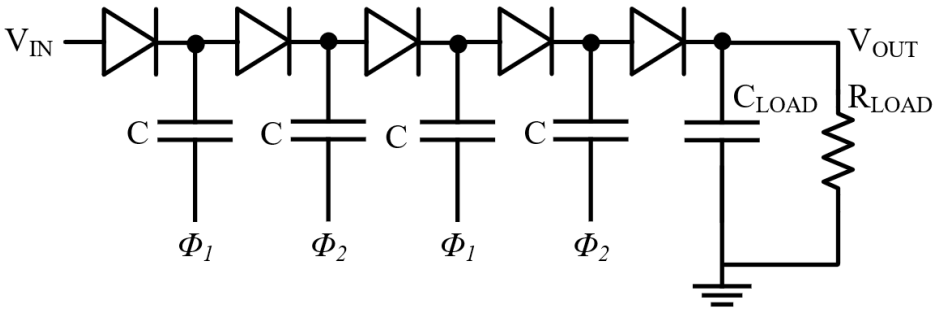

Figure 2.19: Original structure of Dickson topology[7].

In the original design, the drawback is also apparent. There is no diode that can be found in reality to have a 0 forward bias voltage drop. As a result, the voltage stored in the capacitor is less than the ideal analysis. In order to solve this problem, the MOSFET with a driving circuit is implemented to turn on the switches on the right phase with adjustable resistance and reduce

the voltage drop. In the proposed design the NMOS switches are used as power switches to replacing the diodes in the Dickson topology.
Focus on the switched-capacitor part, the two working phases are as shown in Figure 2.20. Based on the same working principle, the stress voltages faced by each switch are listed in Table 2.2. As shown in the table, with the help of the Dickson topology, the whole voltage conversion range is averaged to each switch equally. There are only four switches facing stress voltage large than $5V$. The power switch stacking technique is used in this design to use two $5-V$ devices in series to endure $10V$ stress voltage, which will be discussed in the transistor-level implementations chapter. With the stacking technique, all the power switches are facing $5V$ stress voltage, which leads to only $5V$ power switches being used in the proposed hybrid structure.

Table 2.3: Stress voltage across the switches in the Switched-capacitor stage.

Under ideal scenario		Phase 1	Phase 2	Stress voltage
S_{C1H} S_{C3H} S_{C5H}	Top or right terminal	$5V$	$0V$	$5V$
	Bottom or left terminal	$5V$	$5V$	
S_{C1G} S_{C3G} S_{C5G}	Top or right terminal	$5V$	$0V$	$5V$
	Bottom or left terminal	$0V$	$0V$	
S_{C2H} S_{C4H} S_{MID}	Top or right terminal	$5V$	$5V$	$5V$
	Bottom or left terminal	$10V$	$5V$	
S_{C2G} S_{C4G}	Top or right terminal	$0V$	$5V$	$5V$
	Bottom or left terminal	$0V$	$0V$	
S_{C12}	Top or right terminal	$10V$	$10V$	$10V$
	Bottom or left terminal	$5V$	$15V$	
S_{C23}	Top or right terminal	$10V$	$20V$	$10V$
	Bottom or left terminal	$15V$	$15V$	
S_{C34}	Top or right terminal	$20V$	$20V$	$10V$
	Bottom or left terminal	$15V$	$25V$	
S_{C45}	Top or right terminal	$20V$	$30V$	$10V$
	Bottom or left terminal	$25V$	$25V$	
S_{OUT}	Top or right terminal	$30V$	$30V$	$5V$
	Bottom or left terminal	$25V$	$30V$	

Since the second stage is designed to work the fast switching limit range, the output impedance R_{FSL} is the key part of the design parameter. Based on the charge flows analyses on the working principle shown in the Figure 2.20, during the first phase:

$$q_{C1H} = q_{C12} = q_{C2G} = q_{C3H} = q_{C34} = q_{C4G} = q_{C5H} = q_{OUT} = \frac{1}{2}q_{OUT} + q_{C_{OUT}} \tag{2.70}$$

Where q_{C1H} is the charge flows through S_{C1H} during this phase. The q_{out} is the charge flows out and q_{out} is the charge stored in the C_{OUT}. With the same method:

$$q_{MID} = q_{C1G} = q_{C2H} = q_{C23} = q_{C3G} = q_{C4H} = q_{C45} = q_{C5G} \tag{2.71}$$

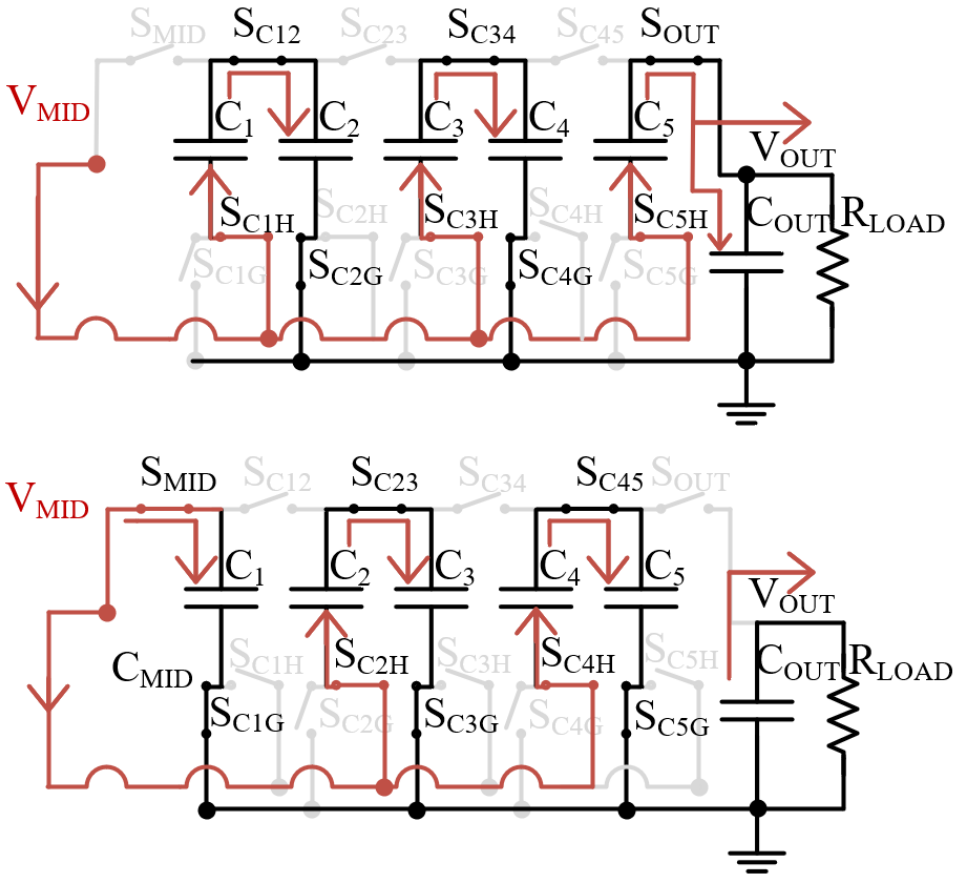

Figure 2.20: Working phases of the second stage of proposed hybrid converter.

$$\frac{1}{2}q_{OUT} = q_{C_{OUT}} \tag{2.72}$$

Therefore, we can find the same number of charges through all the power switches in the Dickson topology. And the relationship between charge through all the switches $q_{Switch,SC}$ the switches and the output charge q_{OUT} is:

$$q_{Switch,SC} = 2 \cdot q_{C_{OUT}} \tag{2.73}$$

Therefore, the a_R mentioned in Equation 2.49, will be 2 for all the second-stage switches. According to the Equation 2.52,R_{FSL} is:

$$R_{FSL} = 8 \cdot \sum_{switches,i} R_{switches,i} \tag{2.74}$$

In order to balance all the resistances equally, all the switch-on resistances in the second stage are designed to be the same value, R_{SC}. And the R_{FSL} is:

$$R_{FSL} = 80 \cdot R_{SC} \tag{2.75}$$

Take the design specifications into concerned:

$$V_{OUT} = V_{OUT_{firststage}} \cdot idealVCR_{secondstage} - I_{LOAD} \cdot R_{FSL} \tag{2.76}$$

Under typical condition, R_{FSL} is around 40Ω. Therefore, the on-resistance of each power switch in the second stage is designed to be 0.5Ω to fulfill the design specifications.
The general R_{SSL} is determined by the charge share loss as mentioned above. The R_{SSL} of the second stage of the proposed hybrid converter must consider the soft charge implemented by the inductor. As shown in Figure 2.18, there are four working stages. During the first stage, the inductor is charged with the input voltage and the second stage is been charged at the last stage. The output charges come from the output capacitor in this stage so this is no charge share within this phase and charge share loss doesn't exist. In the next Φ_2 stage, capacitor C_1, C_3, C_5 and C_{MID} is been charged with the current flows out from the inductor. As a result, there is no charge share loss. The C_{MID} is a protect buffer at the output of the inductor stage to keep the voltage under $5.5V$, which is the safe maxim stress voltage for the $5-V$ devices in the TSMC 180BCD technology. On the Φ_3 stage, the capacitor C_2, C_4, C_{OUT}, and C_{MID} are been charged with the inductor in the loop. Therefore, the charge share loss doesn't exist. Due to the protect capacitor C_{MID}, the charge shares without an inductor in the loop, which leads to charge share loss. Therefore, the R_{SSL} is determined by the charge share loss in the Φ_4.
The lasting time of Φ4 stage $T_{\Phi 4}$is:

$$T_{\Phi 4} = \left(1 - \frac{V_{IN}}{V_{OUT,firststage}}\right) T_{firststage} \tag{2.77}$$

Where $T_{firststage}$ is the switching period of the inductor-based stage. Under typical scenario, $T_{\Phi 4}$ is around $0.25T_{firststage}$. Since the switching frequency of the inductor-based stage is designed to be $2x$ of the switched capacitor stage, the charge change within Φ4 is:

$$q_{\Phi 4} = \frac{T_{\Phi 4}}{2 \cdot T firststage} q_{Switch,SC} \tag{2.78}$$

$$q_{\Phi 4} = \frac{1}{4} q_{OUT} \tag{2.79}$$

Therefore, parameter a mentioned in the equation 2.41 is 0.25. Based on the Equation 2.44, the second stage $R_{OUT_{SSL}}$ of the proposed converter is:

$$R_{OUT_{SSL}} = \sum_{i,capacitor} \frac{a^2}{2F_{SW,SC}C_i} \tag{2.80}$$

Within the Dickson topology, the charge changes of all the capacitors are equal, the C_1 to C_5 should have the same value C_{SW} to get the lowest R_{SSL} with the same total value of capacitors. Meanwhile, in order to design the parameters the C_{MID} is marked as:

$$C_{MID} = \alpha C_{SW} \tag{2.81}$$

Now, the Equation 2.80 becomes:

$$R_{OUT_{SSL}} = \frac{(5+\alpha)\,a^2}{2F_{SW,SC}C_{SW}} \tag{2.82}$$

According to Equation 2.26, the parameters $F_{SW,IB}$, I_L, and C_i are related to the ripple voltage at the output point of the first stage. Based on the design specifications, the rough design parameters can be chosen according to the working principle. The average current flows through the inductor is:

$$I_L = I_{LOAD} \cdot idealVCR \tag{2.83}$$

Where ideal VCR is 8.1 in the proposed design. If the typical value of load current is used, the current within the inductor is around $200mA$. Under the fixed duty cycle of the switching, both the value of the inductor and the switching frequency of the boost stage will influence the ripple voltage at the output of the first stage as mentioned in the analyses part. Based on the Equation 2.26, Δv is:

$$\Delta v = \frac{I_L}{2C_{tot}} DT_{SW,IB} \tag{2.84}$$

Where C_{tot} is the equivalent capacitance at the output of the first stage. As shown in Figure 2.18, the equivalent capacitance has a little bit difference between $\Phi 2$ and $\Phi 3$.

$$C_{tot_{\Phi 2}} = C_{MID} + C_1 + C_2 \backslash\backslash C_3 + C_4 \backslash\backslash C_5 = (2+\alpha)\,C_{SW} \tag{2.85}$$

$$C_{tot_{\Phi 3}} = C_{MID} + C_1 \backslash\backslash C_2 + C_3 \backslash\backslash C_4 + C_5 \backslash\backslash C_{OUT} \tag{2.86}$$

$$C_{tot_{\Phi 3}} = \left(1.5 + \alpha + \frac{C_{OUT}C_5}{C_{OUT}+C_5}\right) C_{SW} \tag{2.87}$$

Since the C_{OUT} is usually much greater than C_{SW}, the C_{tot} can be regards as $(2+\alpha)\,C_{SW}$. With $D = 0.25$, $I_L = 0.2A$ and $T_{SW,IB} = 0.5T_{SW,SC}$, the Equation 2.84 becomes:

$$\Delta v = \frac{1}{80\,(2+\alpha)\,C_{SW}} DT_{SW,SC} \tag{2.88}$$

Based on the Equation 2.82 and Equation 2.88, the $T_{SW,SC}$ is designed to be $20\mu s$ and C_{SW} to be $4\mu F$ to realize $R_{SSL} \ll R_{FSL}$ and Δv within safe range for $5-V$ devices. Meanwhile, $T_{SW,IB}$ is also determined to be $10\mu s$ with topology requirement.
Towards this current level, an inductor around μH is a reasonable choice. In order to get better performance with lower DCR of the inductor and lower switching frequency, a 504015 casing $(5.0mm \times 4.0mm \times 1.5mm)$ $10\mu H$ inductor with DCR equals to $140m\Omega$ is used in the first stage.

The power switches in the first stage are designed to be $70m\Omega$, which is the optimal value when conduction losses are equal to switching losses.
Meanwhile, the resonant frequency of the RC loop within the charging phase should be checked with the converter switching frequency. The resonant period is:

$$T_{LC} = 2\pi\sqrt{LC} \approx 55\mu s \tag{2.89}$$

Since half of T_{LC} is much larger than the charging period, which means the initial lower potential capacitors are only been charging. The designed switching frequency of the hybrid converter could work with a soft charge.

2.2 VCSEL Diode Driver with Adjustable Pulse Width

2.2.1 VCSEL Diode Basic Analysis

As mentioned in the introduction, more and more IoT devices become to support Spatial distance sensing functions. With the advantage of small area and cheap cost, the DTOF system with VCSEL diodes is popular in the last ten years. The basic structure of the VCSEL diode is shown in Figure 2.21.

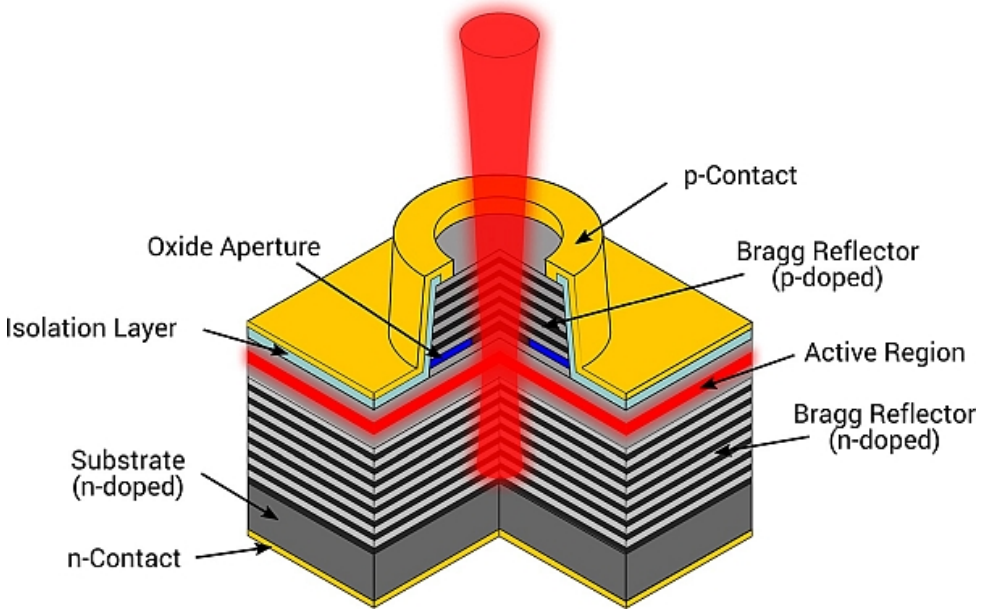

Figure 2.21: The basic structure of VCSEL [8].

VCSEL is directed perpendicular to the semiconductor surface. Two distributed Bragg mirrors make up the vertical cavity. The thicknesses of the Bragg mirrors are approximately equal to a quarter of the laser wavelength, which is built with alternating layers of high- and low-refractive-index material. Electrically pumped quantum wells or quantum dots provide gain, which is located in the active region between the monolithically grown semiconductor mirror,

resulting in a single-longitudinal mode operation. Oxide apertures influence both current and optical field, which enables operation in single-transverse mode, and finally makes the VCSEL become a compact and efficient source of laser emission[8].
In order to drive the VCSEL diode to generate the desired pulse for the measure, the electrical model of the VCSEL diode must be obtained. Since the pulse of the laser is as short as possible to obtain a better system performance, all the parasitic components should be taken into consideration. Meanwhile, the relationship between the electrical model and physical model is also important to estimate the width of the real laser pulse.
Usually, the electrical model is divided into two parts, the VCSEL diode part and the interconnect part[10; 24]. The VCSEL diode part consists main diode and all the modeled parasitic components within the VCSEL diode. The key point is to describe the relationship between the current and voltage of the diode. As shown in the Figure 2.22. With the influence of the overall package structure of the VCSEL diode, the parasitic inductor L_D, parasitic resistor R_D and parasitic capacitor C_D are connecting with VCSEL diode D between the anode and cathode of the packaged VCSEL diode. The parasitic information will be provided by the manufacturers. The static parameters of the VCSEL diode are modeled by the $I-V$ curve fitting in forwarding bias, which is the well-known Shockley equation as shown in Equation 2.90.

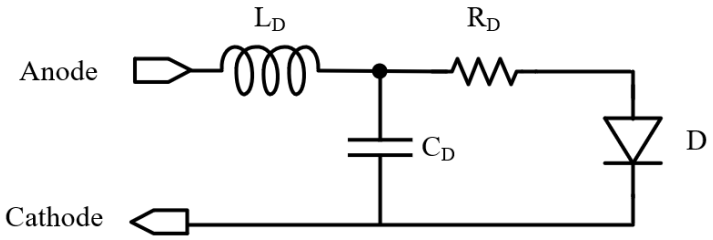

Figure 2.22: The basic parasitic structure of VCSEL.

$$V = R_D I + nV_T ln\left(\frac{I}{I_S}+1\right) \tag{2.90}$$

Where V and I are the diode D voltage and current.
The relationship between the current flowing through and the rate of the VCSEL diode is described as[25]:

$$\frac{\mathrm{d}S}{\mathrm{d}t} = \Gamma g_0 \frac{N(t)-N_0}{1+\varepsilon S(t)} - \frac{S(t)}{\tau_p} + \Gamma\beta\frac{N(t)}{\tau_n} \tag{2.91}$$

$$\frac{\mathrm{d}N}{\mathrm{d}t} = \frac{I(t)}{eV_a} - g_0\frac{N(t)-N_0}{1+\varepsilon S(t)}S(t) - \frac{N(t)}{\tau_n} \tag{2.92}$$

Where $S(t)$ is the photon density and $N(t)$ is the carrier density. N_0 represents the carrier density at transparency. The optical confinement factor is marked as Γ. g_0 is the gain slope. ε is the gain saturation parameter. τ_p and τ_n are the lifetimes of photon and carrier. e is the electron charge and v_a is the volume of the active region.

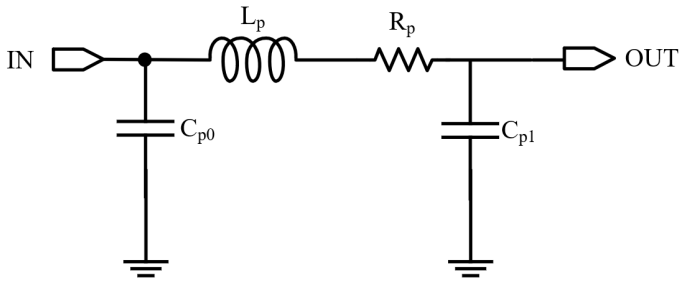

Figure 2.23: Electrical Π model for the interconnect equivalent circuit.

The model of interconnecting equivalent circuit is:
Since the bonding wires have parasitic parameters that influence the transient response of the VCSEL diode, the bonding wire must be considered during the driver design. The Electrical Π model is easy to measure and simulate, which makes it a good choice here.

2.2.2 Basic Working Principle of the VCSEL Diode Driver

In order to drive the VCSEL diode to generate a short-width pulse, the high voltage across the VCSEL diode must be on or off quickly. As mentioned in the above subsection, there are parasitic components within the bonding wires and packaged VCSEL diode. All of them will bring difficult to turn on or turn off the VCSEL diode quickly. The rising speed of the current in the loop is determined by the value of across voltage and the inductor within the loop as:

$$\frac{\mathrm{d}I_L}{\mathrm{d}t} = \frac{V_L}{L_S} \tag{2.93}$$

Where I_L is the current flow through total series inductor L_S and V_L is the cross voltage. Even though the VCSEL diode is able to work under low voltage conditions, in which the voltage level can come from the outside power supply directly, the rising speed of the pulse is slow which limits the pulse width of the laser. According to Equation 2.93, there are two possible solutions to improve the current rising speed, reducing the series inductor L_S or increasing the across voltage V_L. However, the parasitic inductor is hard to eliminate within the circuit design, the more suitable method is to increase the across voltage V_L.
In order to power the VCSEL diode with a high voltage level, the first step is to have the high voltage level. In terms of IoT devices, the output voltage of the Li-ion battery is not enough and a voltage step-up must be implemented. Generally, a DC-DC converter will be implemented to provide a voltage large enough to turn on the VCSEL diode quickly.
As shown in the Figure 2.24, Laszlo proposed a VCSEL driver with both V_{DDH} and V_{DD}[10]. Meanwhile, the floating isolated well and level shifter are used to convert signals between two different voltage levels. Since the whole DTOF system should be as tiny as possible to meet the compact volume requirement, such a design with an extra DC-DC converter to provide V_{DDH} is not suitable for compact IoT devices. There is another kind of design idea as shown

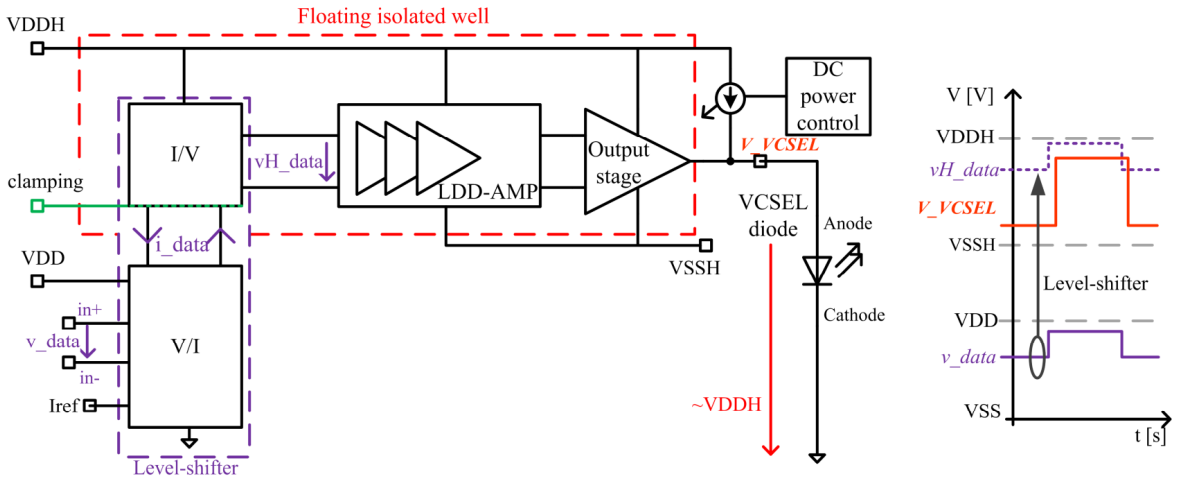

Figure 2.24: System diagram and waveforms of the floating-well VCSEL driver[9].

in Figure 2.25. Compared with the design mentioned in Figure 2.24, Samuel's design is able to drive the VCSEL diode with $2\times$ V_{DD} with only V_{DD} as the input voltage level. The basic working principle is charging the flying capacitor during Φ_1 and stacking the capacitor on the VDD during the Φ_2. The rising time of the pulse becomes:

$$t_{rise} \approx \frac{L_S I_D}{2V_{DD} - V_D} \tag{2.94}$$

Where I_D and V_D are the current and voltage of the VCSEL diode. Therefore, the main advantage of this topology is obvious, the t_{rise} is reduced with only one low voltage level which leads to shorter pulse ability.
Since the on-resistance of the power switches causes voltage drops when the current flows through, the voltage across the VCSEL diode during the on phase will be lower than ideal$2V_{DD}$. The V_{ac} is:

$$V_{ac} = 2V_{DD} - I_D\left(R_{M_0} + R_{M_4}\right) \tag{2.95}$$

And the value of the flying capacitor C_{fly} should be large enough to supply enough charge during the whole on phase. The rough voltage drop $V_{drop}$is:

$$V_{drop} = \frac{W_{pulse} I_D}{C_{fly}} \tag{2.96}$$

Meanwhile, charge re-balance between C_{fly} and C_D occurs on the turn-on moment which leads to the voltage drop of C_{fly}. The small drop voltage $V_{drop,re-balance}$ is:

$$V_{drop,re-balance} = V_{DD}\left(1 - \frac{C_{fly}}{C_{fly} + C_D}\right) \tag{2.97}$$

Based on the above two equations, the C_{fly} could be sized according to design specifications.

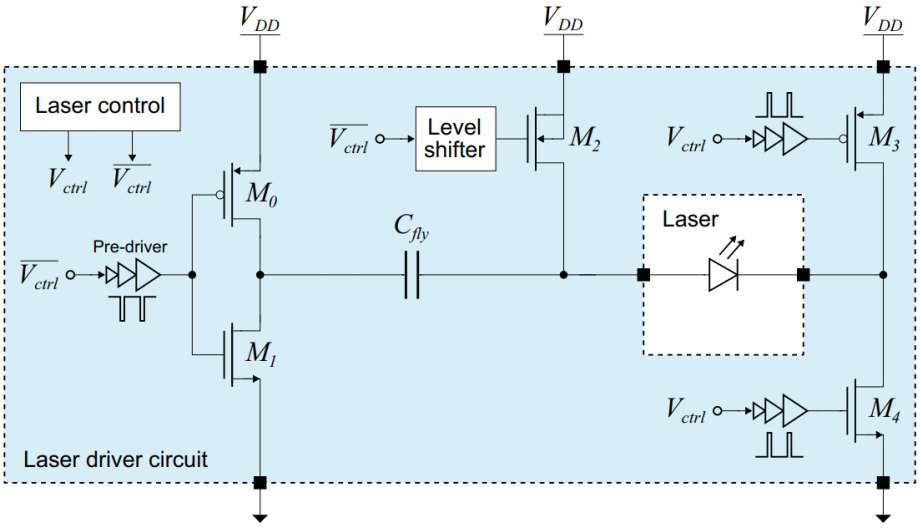

Figure 2.25: Block diagram of the laser driver circuit[10].

2.2.3 Preliminary Design of the VCSEL Diode Driver with Adjustable Pulse Width

The design specifications of the proposed VCSEL driver are shown in Table 2.4, and the design is based on the SMIC 55BCD process.

Table 2.4: The specifications of the VCSEL driver.

Input voltage	Logic part: $1.2V$
	Power part $3.0V$
Load current	$250mA$
Output voltage	$\approx 6V$
Pulse width	$300ps - 1600ps$
Pulse frequency	$16MHz$
Area	$< 0.33mm^2$ and as small as possible

Based on the similar idea shown in the [24], the proposed VCSEL driver shown in Figure 2.26 has two working phases. The whole system consists of a control part and a driver part. The control part will be discussed in the next chapter. The core part of the driver only consists of 5 power switches. The proposed VCSEL driver needs two separate control signals SW_{fixed} and $SW_{adjustable}$ with colored lines shown in the diagram. This design is to achieve pulse width as shorter as possible. Owning to the large size of the M_{p1} and PVT influence, pulse width shorter than $600ps$ is hard to pass the $buffer_1$ and appear at the gate of M_{p1}. Therefore, SW_{fixed} are implemented for the M_{p1} M_{n2}. M_{n3} is driven by $buffer_2$, which supports $SW_{adjustable}$ with pulse width of $200ps$ in majority PVT situations. Therefore, the lower pulse width is supported in this design. However, different buffer sizes result in different delays in the two control signal paths. The control part also takes this into account.

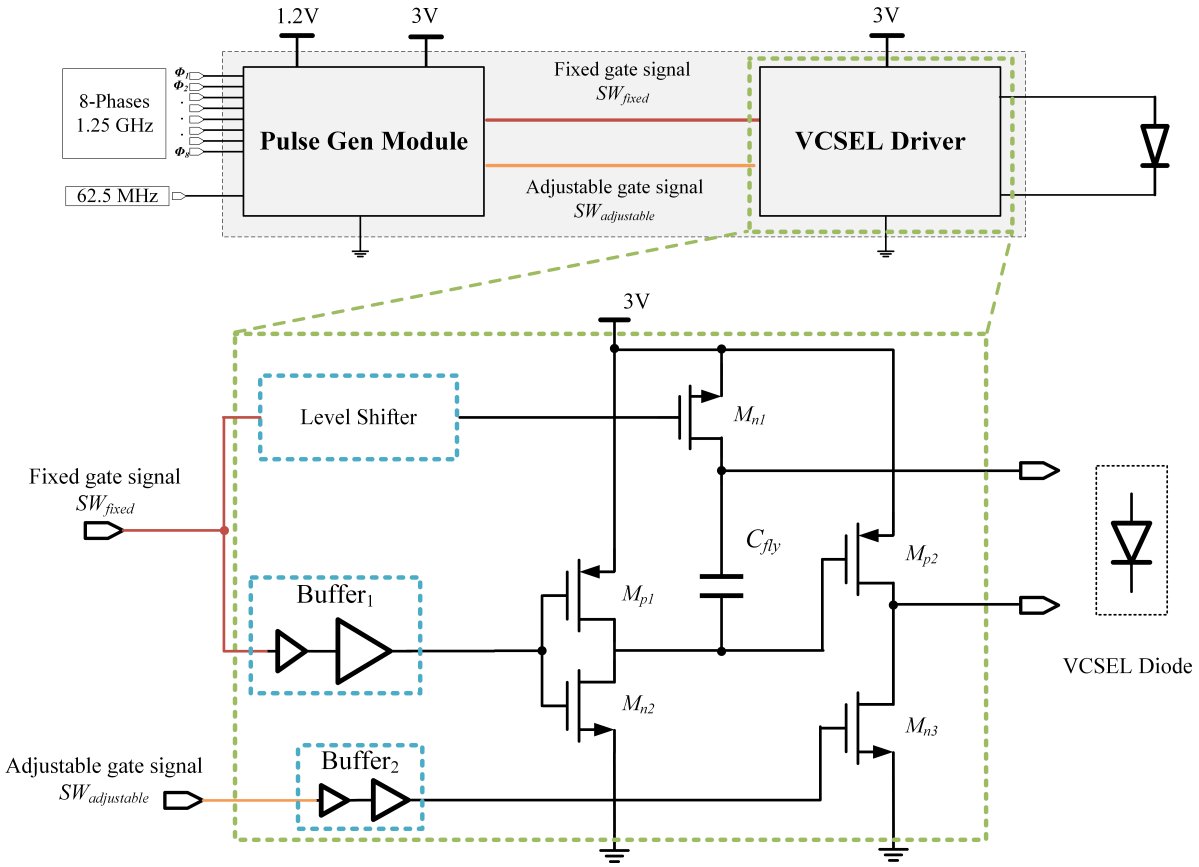

Figure 2.26: Proposed VCSEL diode driver.

During the Φ_1, the M_{n1} and M_{n2} are turned on to charge the C_{fly} to the input voltage of power part $3V$ and the anode of the VCSEL diode is connected to $3V$. Meanwhile, the M_{p2} is also turned on to connect the cathode of the VCSEL diode to $3V$. Therefore, the voltage across the VCSEL diode will be 0 in Φ_1.
During the Φ_2, the M_{p1} is turned on to charge the bottom plate of C_{fly} to $3V$. Therefore, the voltage on the top plate of C_{fly} is around $2 \times 3V$, which is also the voltage of the anode of the VCSEL diode. At the same time. the M_{n3} is on to drop the cathode voltage of VCSEL to the ground. Therefore, the voltage across the VCSEL diode will be $2 \times 3V$ in the Φ_2.
All the analyses above are towards the working principle of the core part of the VCSEL driver marked by the green dash line in Figure 2.26. Based on the Equation 2.95 and the VCSEL diode model, the on resistances of M_{p1} and M_{n3} are sized to be around 4Ω. Based on RC loop charging as shown in the Equation 2.98, the C_{fly} and on resistances of M_{n2} and M_{n1} can be designed to charge the C_{fly} to $3V$ during the Φ_2 which lasting more than $14.4ns$. Therefore, the C_{fly} is designed to be $220pF$ and values of M_{n2} and M_{n1} on resistances are around 41Ω.

$$V(t) = V_{discharged} + \left(V_{VDD} - V_{discharged}\right)\left(1 - e^{-\frac{t}{\tau}}\right) \tag{2.98}$$

The on-resistance of M_{p2} influences the off transient behavior of the VCSEL diode, which is

larger on resistance increasing the settling time. The damping factor ξ during the off process is:

$$\xi \approx \frac{R_{on,Mp2}}{2}\sqrt{\frac{C_{tot}}{L_{tot}}} \tag{2.99}$$

Where C_{tot} is the total parasitic capacitor at the cathode of the VCSEL diode and L_{tot} is the total inductor in the loop, which mainly comes from the interconnect part shown in the Figure 2.23. The $R_{on,Mp2}$ is designed to be 8Ω for a faster off process.

3 Control System

3.1 Hybrid Converter Control System

3.1.1 General Control System for Boost Converter

In order to control the inductor-based boost converter, the control loop must be implemented to achieve a closed loop system.

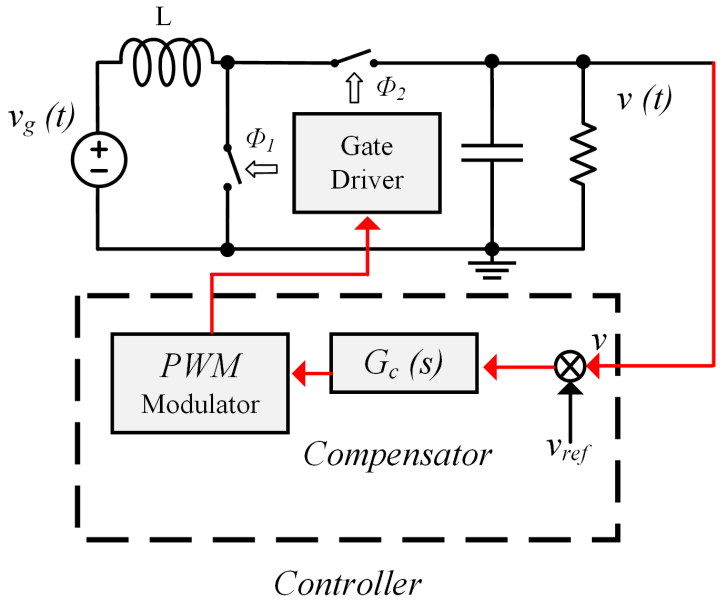

Figure 3.1: A simple DC-DC boost converter regulator system.

A simple closed loop system for boost converter is as shown in the Figure 3.1, output voltage v will be operated with reference voltage v_{ref} to get the error message. Then the compensator is implemented to make sure the stability of the closed loop system. The following PWM modulator generates a switching pulse according to the error information. Finally, the changed switching signal controls the power switches by the gate driver and gradually close to the target output voltage.
The AC model of the boost converter is necessary to analyze the stability of the control loop. Since there are a large number of analyses have been done, the results are referred to here. Since the boost converter changes the electric components within the loop in two different phases, the

boost converter is not a linear circuit. The averaged small-signal AC model of boost converter as shown in the Figure 3.2 is discussed in the [11].

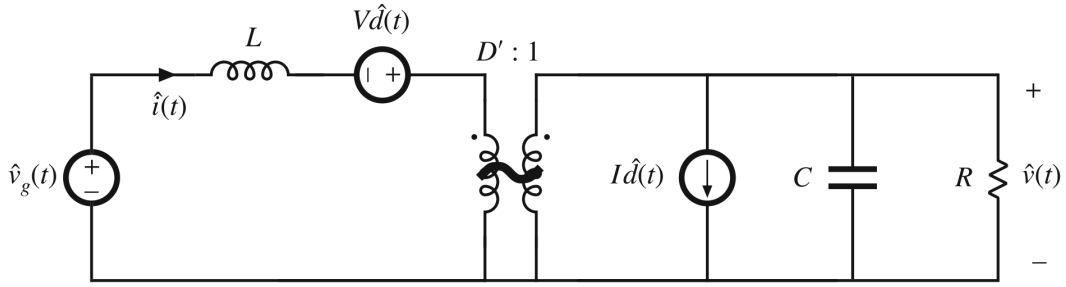

Figure 3.2: Averaged small-signal AC model for boost converter[11].

Where $\hat{d}(t)$ is the small AC variations of Duty cycle D and $\hat{v_g}(t)$ is the small ac variations of input voltage V. And based on the averaged small-signal ac model, the small signal model towards the relationship between the small AC variations of output voltage $\hat{v}(t)$ and $\hat{d}(t)$ can be written as[11]:

$$G_{vd(s)}\mid_{v_g(s)=0} = \frac{\hat{v}(t)}{\hat{d}(t)} = \frac{D'V\left(1-\frac{sL}{D'^2R}\right)}{LCs^2+s\frac{L}{R}+D'^2} \tag{3.1}$$

Meanwhile, the PWM modulator in the closed loop also needs the small signal model for loop analyses. The output waveform $\delta(t)$ is generated by comparing control voltage $v_c(t)$ and saw-tooth wave $v_{saw}(t)$ with V_M as peak voltage. The basic structure and the waveform are shown in Figure 3.3.

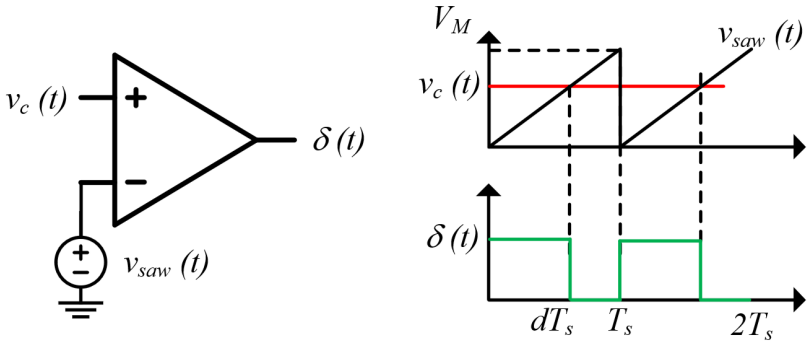

Figure 3.3: PWM modulator and waveform.

With the help of average model analyses, the AC small signal model of the PWM modulator is:

$$G_m(t) = \frac{\hat{d}(s)}{\hat{v}_c(s)} = \frac{1}{V_M} \tag{3.2}$$

With all the small models within the loop, the stability of the system can be analyzed and design suitable compensator.

3.1.2 General Control System for Switched-Capacitor Converter

Since the duty cycle D of the switched-capacitor converter is fixed during the design flow, the general way to control the converter is pulse frequency modulation (PFM). The first method is continuous frequency modulation as shown in Figure 3.4.

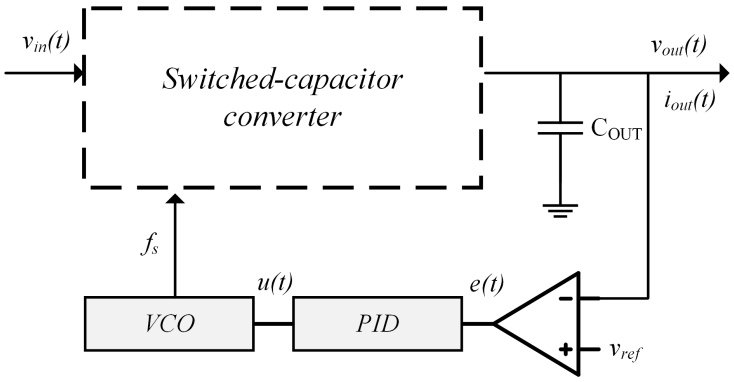

Figure 3.4: Continuous frequency modulation.

The basic idea of continuous frequency modulation is to modulate the switching frequency f_s and change the output impedance. As shown in Figure2.11, the lower switching frequency changes the converter from the FSL range to the SSL range. Therefore, this control way makes the switched-capacitor converter work just like an LDO circuit. Compared with the two other methods mentioned later, this control method is power consuming and complex owning to the stability problem.

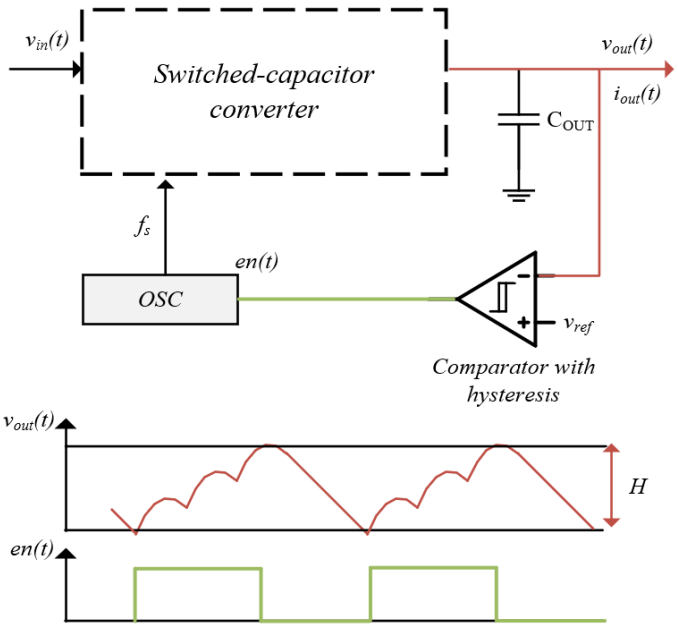

Figure 3.5: Hysteretic control of f_s.

Hysteretic control of f_s is also able to control the converter as shown in the Figure 3.5. The compactor with hysteresis will limit the output voltage ripple within the threshold value H by generating enable signal for the OSC. The advantage of this method is unconditionally stable and saves power during the disabled period. However, since the ripple voltage at the output is now proportionate with the H, the efficiency is reduced. Meanwhile, the delay in the control loop will result in more output ripple voltage, which should be limited in the design.
Pulse-skipping control as shown in Figure 3.6 is another common control method. As shown in the Figure, the clock signal pulses will be neglected when the output voltage is higher than the reference voltage. As a result, this working principle is changing the effective frequency of the switching signal. Compared with the first method using VCO, this method is able to simplify the control loop design and avoid stability problems.

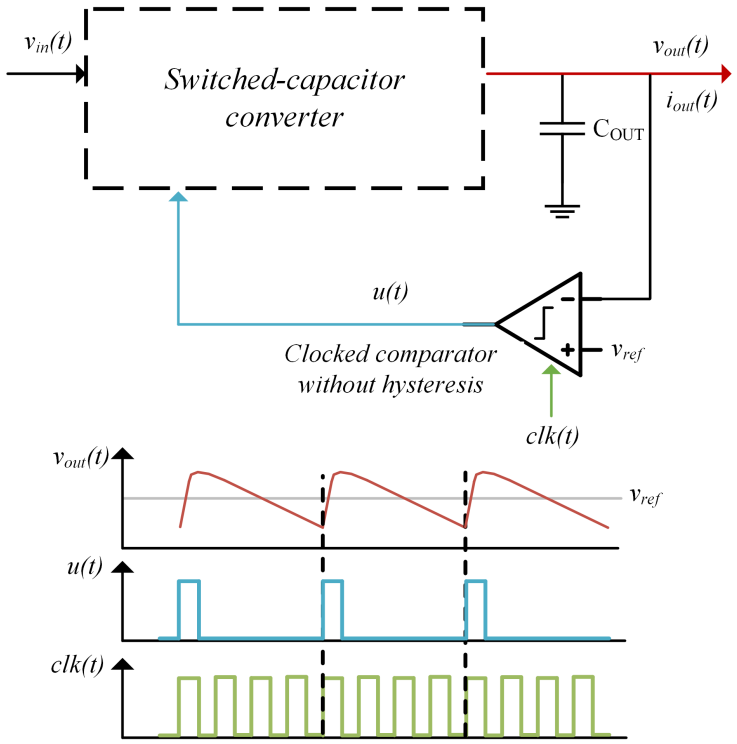

Figure 3.6: Pulse-skipping control.

3.1.3 Control System for Proposed Hybrid Converter

The whole system diagram of the proposed hybrid DC-DC converter is shown in Figure 3.7. With the help of the inductor-based stage, the proposed converter can be controlled with a simple voltage-based PWM control method. As shown in the diagram, the output voltage V_{OUT} will be divided by the R_{FB1} and R_{FB2} to make sure the amplitude of V_c is small enough processed by the control module. A $g_m - C$ is used in the control module to integrate the difference between the converter output voltage and the reference voltage and generates a control voltage. The loop bandwidth is designed around $1KHz$ Then the control voltage will be compared with the off-chip signal $100KHz$ saw-tooth wave V_{saw} to generate a $100KHz$ PWM signal. The $100KHz$ PWM signal will directly operate by the non-overlapping circuit and generate control signals for two power switches in the inductor-based stage. The $100KHz$ PWM signal will also be used to generate a $50KHz$ signal with a 50% duty cycle. The $50KHz$ signal is also operated by the non-overlapping circuit and generates two phase signals for controlling the switched capacitor converter.

The AC small-signal model for the proposed hybrid structure has been derived based on the methods mentioned in [11] and is shown in Figure 3.8. Based on the model, the duty cycle to output voltage transfer function is given by the Equation 3.3:

$$G_{vd} = \frac{V_{OUT}}{6D'} \frac{1 - s\frac{36L}{D'^2 R_L}}{1 + s\left(\frac{36L}{D'^2 R_L} + \frac{36C_{OUT}R_{eq}}{D'^2}\right) + s^2 \frac{36LC_{OUT}}{D'^2}} \tag{3.3}$$

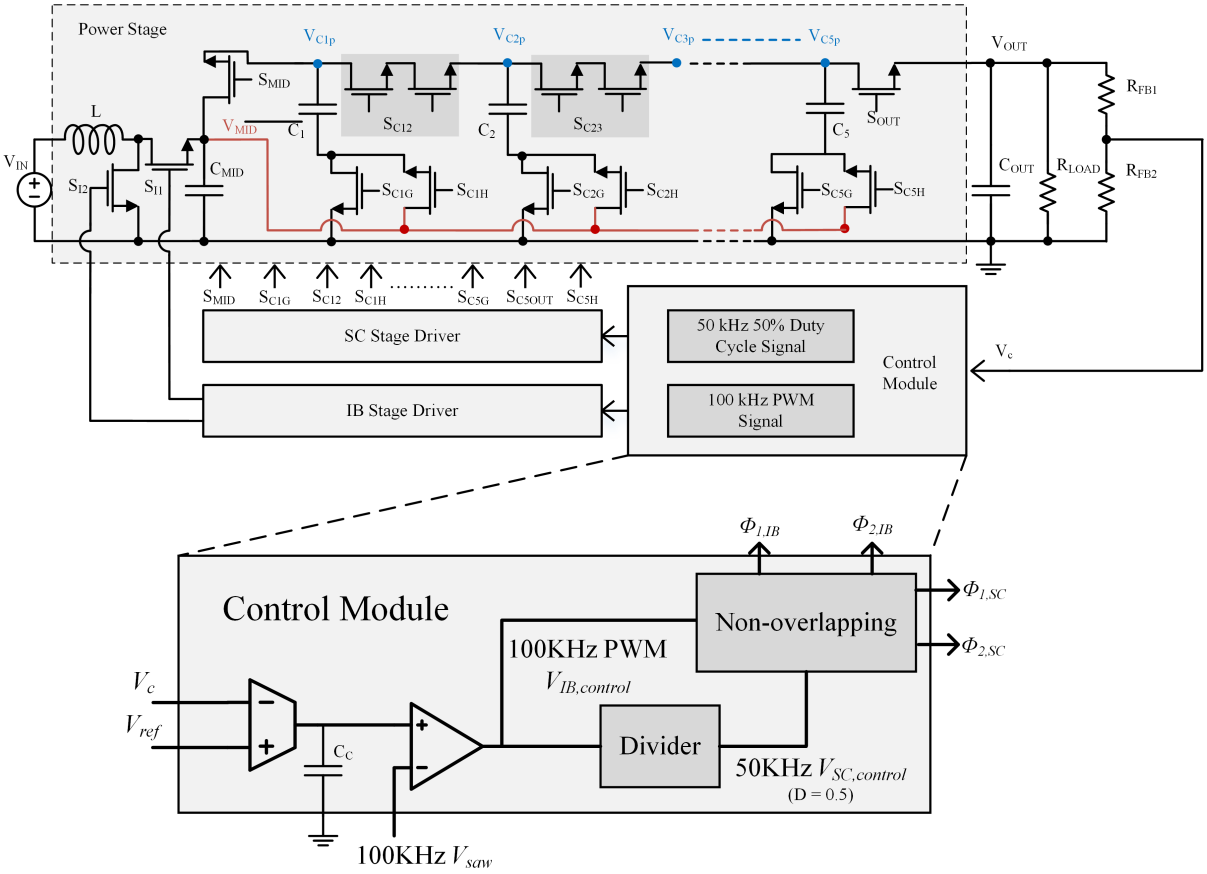

Figure 3.7: System architecture of the proposed converter.

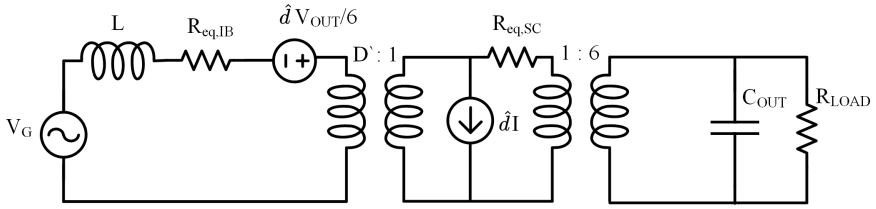

Figure 3.8: AC small-signal model for the proposed hybrid structure.

3.2 VCSEL Driver Control System

As mentioned in the preliminary design of the VCSEL driver, there are two signal pulses needed to control the driver with different pulse widths.
As shown in Figure 3.9, there are 8 phases of 1.25GHz clock signals to generate adjustable width signal and one 62.5MHz signal to determine the period of the short width pulse. Meanwhile, The two target pulses are shown below the diagram. In order to generate those two

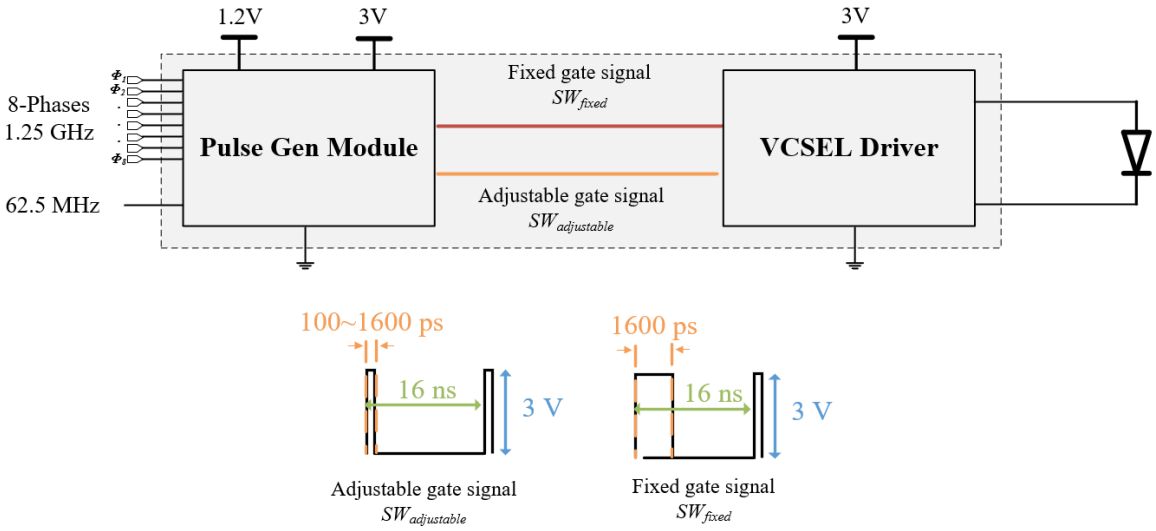

Figure 3.9: Control block diagram of the VCSEL driver.

pulses, there are several steps including synchronization, pulse selection, level shift, and signal operation.

Using the different phase $1.25GHz$ signals, the different pulses could be generated with a simple operation like AND logic. However, the output signal after the simple operation is still with $1.25GHz$ as its clock. In order to get an adjustable short pulse with $62.5MHz$ as its clock, the synchronization logic must be implemented at the beginning.

The signal synchronization block is as shown in Figure 3.10. The main function of this logic block is to get the select window signal with $62.5MHz$. The main function is achieved by the D flip-flop with a $62.5MHz$ signal on the DATA terminal and a high-speed signal on the clock terminal. In order to limit the risk of metastability during the synchronization, there are a series of delay flip-flops used to delay the data stream long enough for metastability failures to occur at a negligible rate. Therefore, there are four D flip-flops used in the core part and the outputs of the third and the fourth flip-flops are used to operate and get the select window signal. The MUX block at the beginning of the synchronization block is to select the $1.25GHz$ with the right phase by the programmable bits. Meanwhile, in order to reduce the leakage at off mode, the enable signal $en\_withsyn$ provides the block function within the MUX to prohibit the high-speed signals from flowing into the logic part.

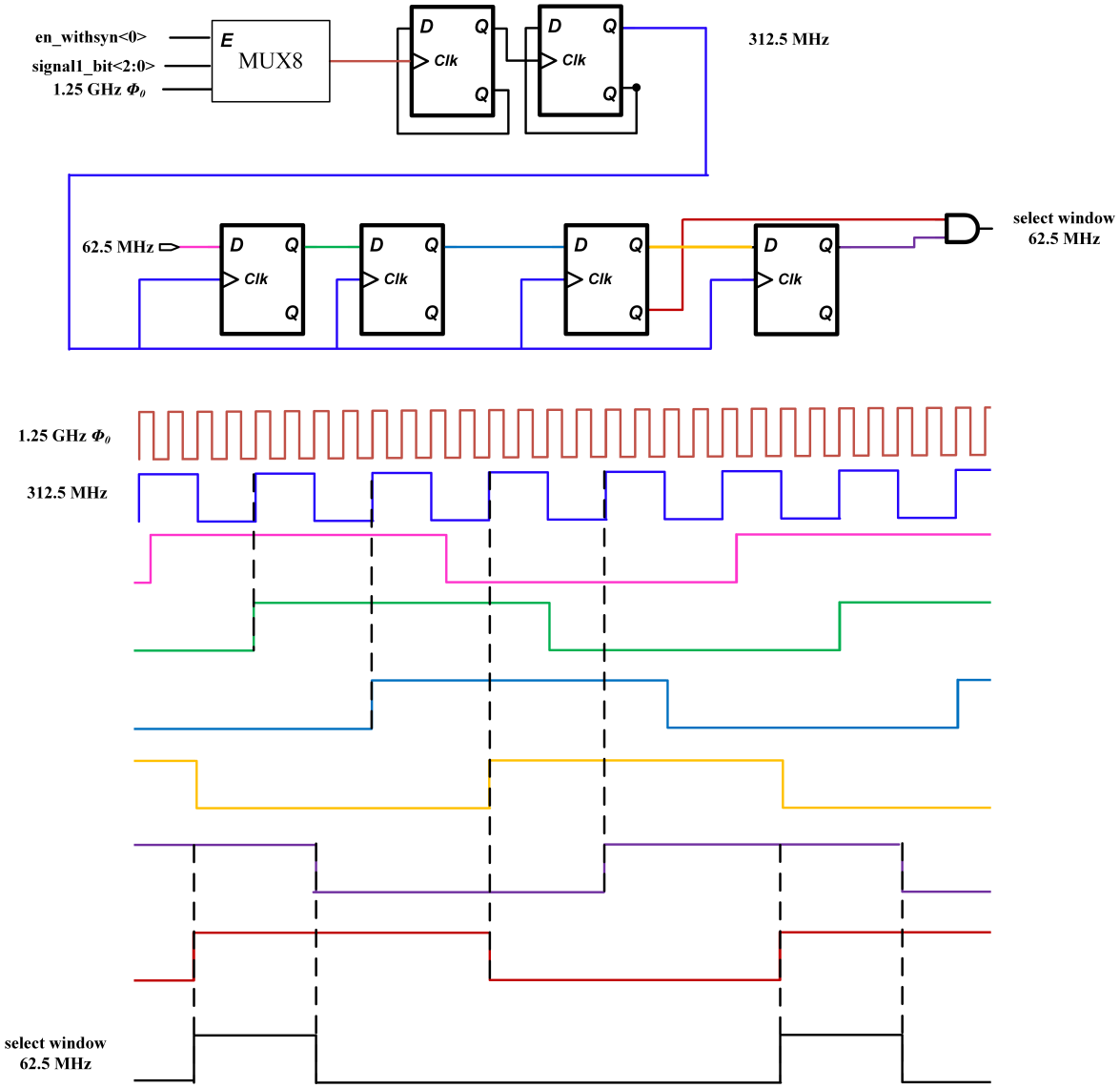

Figure 3.10: Signal synchronization block.

There are two more D flip-flops are used after the *MUX* to divide $1.25GHz$ signal by 4 and gain a $312.5MHz$ signal. The reason to lower the high-speed signal in the low-frequency range is to get a wide adjustable range of pulse width. In order to generate a pulse width range up to $1.6ns$, the two original signals must have $800ps$ as pulse width. however, if both *AND* and *OR* logic are used to operate two $800ps$ pulse width signals with different phases will bring difficulties to the circuit design, since PVT and mismatch effects of two functional logic can't be matched very well. Therefore, two signals with $1.6ns$ pulse width are used with *AND* logic to generate adjustable pulse width signals.

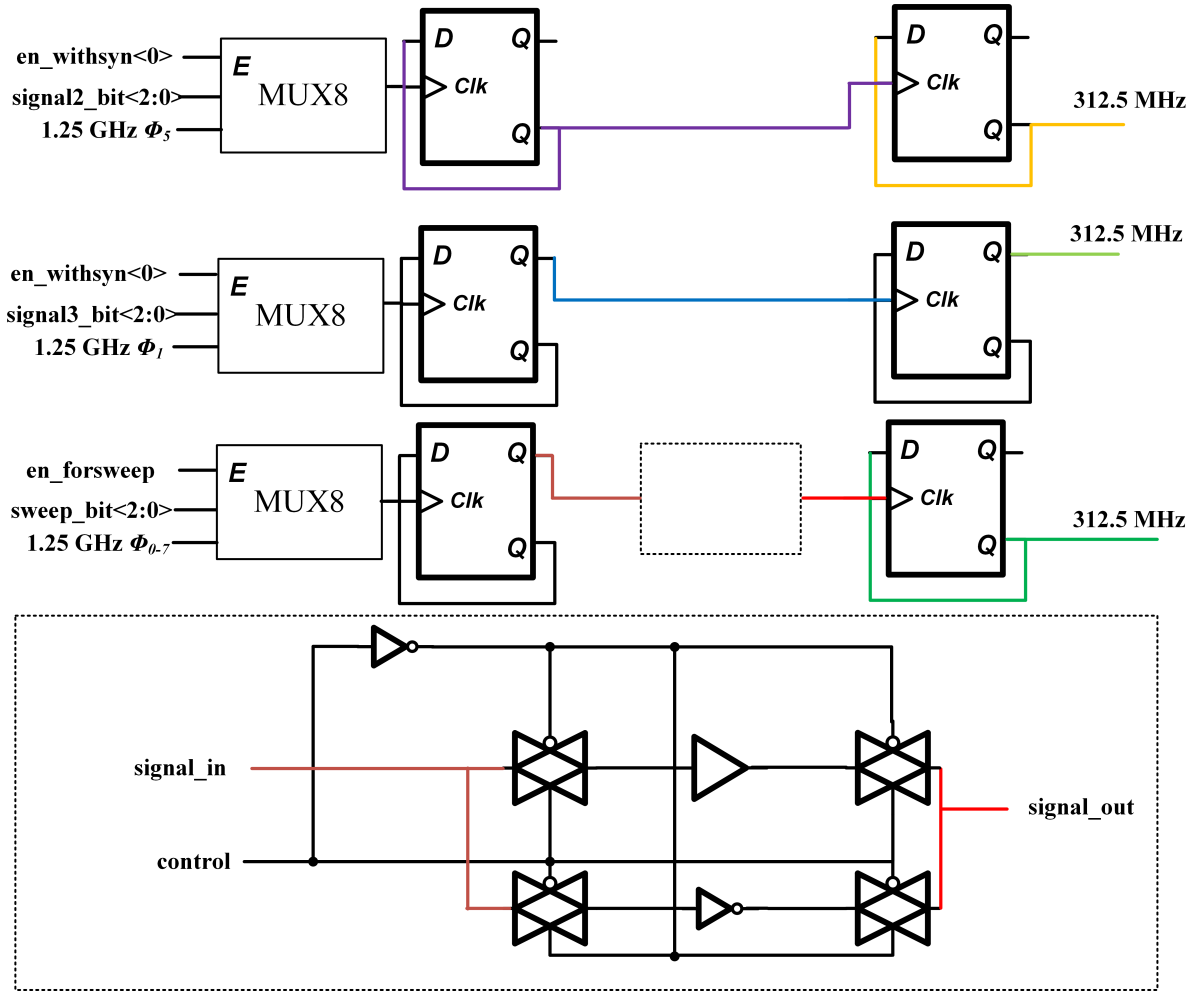

Figure 3.11: Adjustable pulse width block.

The main control logic part to generate two different phase pulses with $1.6ns$ pulse width is shown in Figure 3.11. In order to show the working principle directly, the waveform of important signals is shown in Figure 3.12, where the colors of the waveform have matched the paths in Figure 3.11. According to the same reason, *MUX* with enable signal is the beginning of each signal path to reduce the leakage during the off mode. The two kinds of green color waves signal 3 and signal 4 are the two different phase pulses with $1.6ns$ pulse width. With the

help of the two D flip-flops, the frequency of the signals is divided to be $312.5MHz$. The phase control consists of two-part. The first part is the bottom MUX, which is able to add delay up to $700ps$ in the phase by selecting 8 phase $1.25GHz$ signals. And the second part of the control logic between the two D flip-flops is shown in Figure 3.11. By inverse, the input signal of the second D flip-flop, a fixed $800ps$ phase delay can be added. Therefore, the phase delay range meets the requirement.
As shown in Figure 3.12, by operating signal 3 and 4 with AND logic, the adjustable pulse width signal is generated. By operating the select window signal gained from the synchronization block and signal $2-4$ signals with AND logic, all of them will appear with the period of $62.5MHz$ and meet the design requirements. Meanwhile, the yellow wave signal 2 is also important, since it has a fixed pulse width and its rising edge is ahead of signal 3's rising edge around $400ps$ to make up for the delay mismatch caused by the different buffer sizes which will be discussed in the next chapter.
It is worth noting that enable signal is added to all the input gates where high-frequency signals appear. And the later adjustable pulse width block is sensitive with the first rising edge after the enable signal is on since the relative phase relationship of all 8 phases $1.25GHz$ signals should keep the original order. Therefore, the enable signal must synchronize with the $1.25GHz$ signal. As shown in the Figure 3.13, the enable signal is synchronized with $1.25GHz$ Φ_6 signal firstly and synchronized with $1.25GHz$ Φ_2 signal later. The first synchronized enable signal $en\_withsyn<0>$ is used to enable the front four phases and $en\_withsyn<1>$ is used to enable the later four phases. This design also includes the D flip-flop delay influence as shown in the waveform.

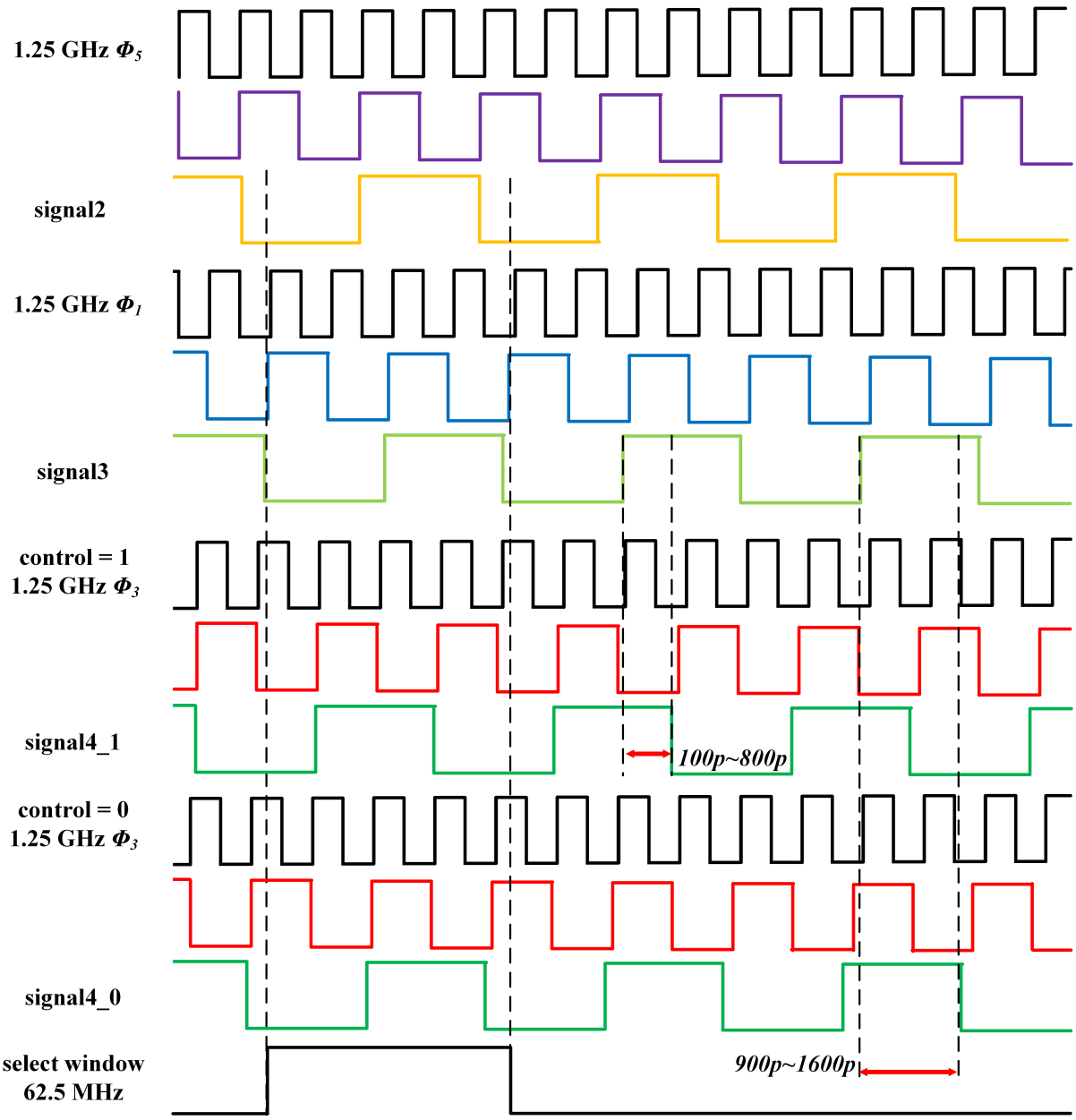

Figure 3.12: Adjustable pulse width waveform.

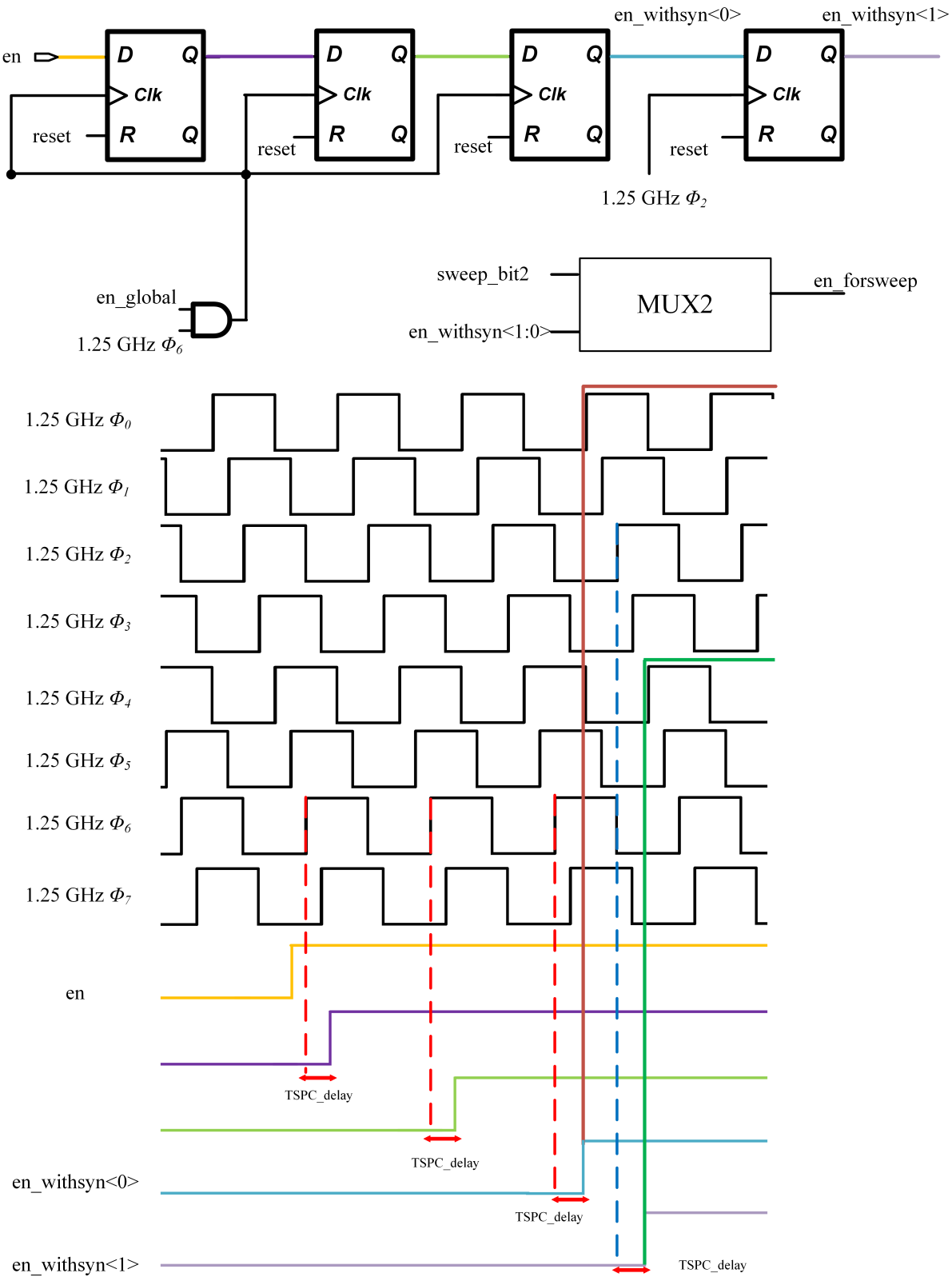

Figure 3.13: Enable signal synchronization block and waveform.

4 Circuit Implementation

In this chapter, the circuit implementations of key modules within the two designs will be discussed.

4.1 Hybrid DC-DC Converter Part

Since only $5-V$ devices are used in the power stage to improve the efficiency performance, the key part during the circuit implementation is to make sure all the devices are within the safe voltage range. The following two modules are designed from this basic idea.

4.1.1 Stacking Low-Voltage Switch

As shown in Table 2.3, the power switches between the two top plates of capacitors within the second stage face stress voltage around $10V$. This stress voltage is divided into two parts with a cascaded switch consisting of two $5-V$ devices as shown in Figure 4.1. The lower side switch

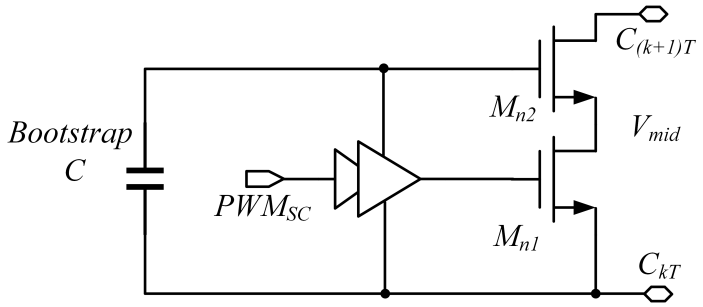

Figure 4.1: Stacking power switch.

M_{n1} is able to control the status of the stacking switch since the bottom voltage level of PWM_{SC} signal is the same as the source terminal of the lower side switch. The gate terminal of the upper switch M_{n2} and the top voltage level of the control signal buffer are around $5V$ higher than the source terminal of M_{n1}, which is stored in the bootstrap capacitor. When the control signal PWM_{SC} is low to turn off the switch, the V_{mid} is protected to lower than $5V$. Therefore, this stacking switch is able to resist $10V$ stress voltage. Meanwhile, owning to the series structure, the width of two switches should be $2\times$ larger to maintain the original on-resistance.
The advantages of stacking low-voltage devices are roughly shown by the output capacitance related to FOM[5]:

$$FOM_{stack-10V} \approx N \times R_{dson}\frac{C_{oss}}{M} = FOM_{5V} < FOM_{10V} \tag{4.1}$$

Where $FOM_{stack-10V}$, FOM_{5V} and FOM_{10V} are the equivalent FOM of the stacking devices, $5-V$ devices, and $10-V$ devices. The Equation shows the stacking results on resistance increasing and out output capacitance decreasing with the same proportion. Therefore, the stacking method shows better performance compared with $10-V$ devices, which usually helps to save area and power. The conclusion is also reported in [26].

4.1.2 Dynamically Controlled Level Shifter

Since all the power switches within the proposed hybrid converter are implemented with $5-V$ devices, the stress voltage requirements should be given special attention, which is important to keep all the power switches in safe working conditions. The stacking technique mentioned above helps to maintain safe voltage between the drain and source and the dynamically controlled level shifter (DCLS) [27] is used to maintain safe voltage between the gate and source.
The implemented dynamically controlled level shifter is shown in Figure 4.2. The original voltage level of control signal PWM_{SC} is between the ground and the logic power voltage level $VDDL$ as shown in the waveform. In order to keep V_{GS} of M_{n1} within a safe voltage range, the bootstrap method is implemented here to let the highest voltage on the gate following source voltage V_{float} is around $V_{float}+V_{BOOT}$. The DCLS firstly generates a pulse on the rising edge and falling edge of the PWM_{SC} with the help of the pulse generator. Then the two pulse are used to turn on the isolated NLDMOS M_{NLD} shortly and drop the drain voltage from $V_{float}+V_{BOOT}$ to $V_{float}-V_D$, where V_D is the voltage drop across the diode. A simple flip-flop is used to recover the PWM_{SC} from the two pulses. As a result, shown in the waveform, the control signal is converted to the targeted voltage level range.
Within the whole DCLS, only two swathes face stress voltage larger than $5V$. Therefore, the performance of speed and efficiency is better than the traditional methods. The conclusion is also reported in [27] with a detailed analysis.

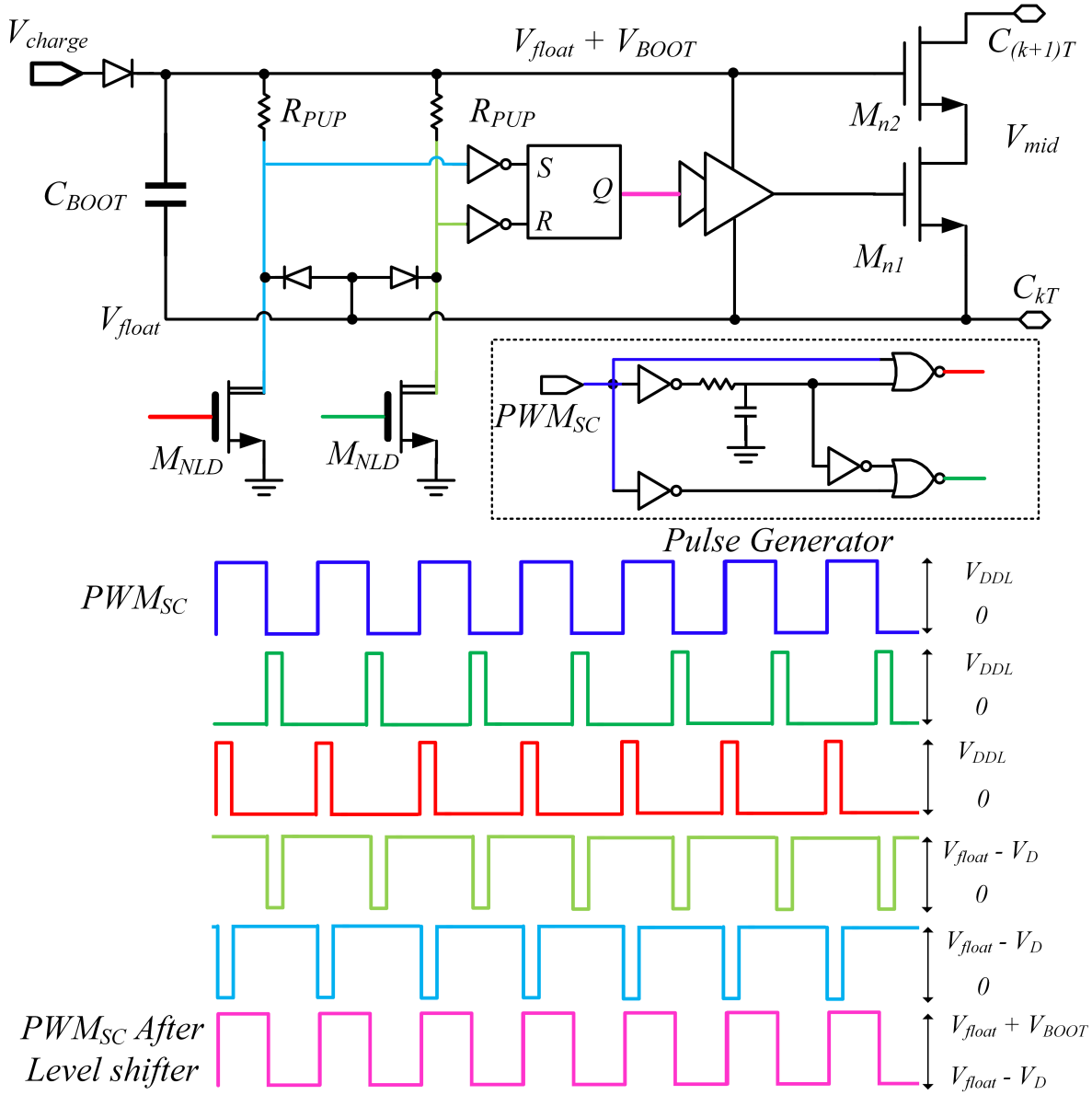

Figure 4.2: Dynamically controlled level shifter and waveform.

4.2 VCSEL Driver Part

The difficulties during the circuit implementation of the VCSEL Diver Part mainly consist of two parts: only $1.2-V$ and $5-V$ devices are possible to use and the PVT influence of the circuit should be considered. In order to increase the speed of the logic part, a true single-phase clock consisting of low threshold devices is used in the enable signal synchronization block as shown in Figure 3.13. Meanwhile, converting a signal from a $1.2-V$ domain to a $5-V$ domain without the help of middle $3-V$ devices requires a level shifter with speed enhanced. The level shifter is also needed for the M_{n1} shown in Figure 2.26, which is an NMOS with burried N well.

4.2.1 True Single-Phase Clock

The circuit implementation of a true single-phase clock is as shown in Figure 4.3. The inner signal paths have been marked with green lines. M_{p5} is used to set the Q to be logic low when the *reset* signal is logic high. The sizes of each transistor are shown in Table 4.1.

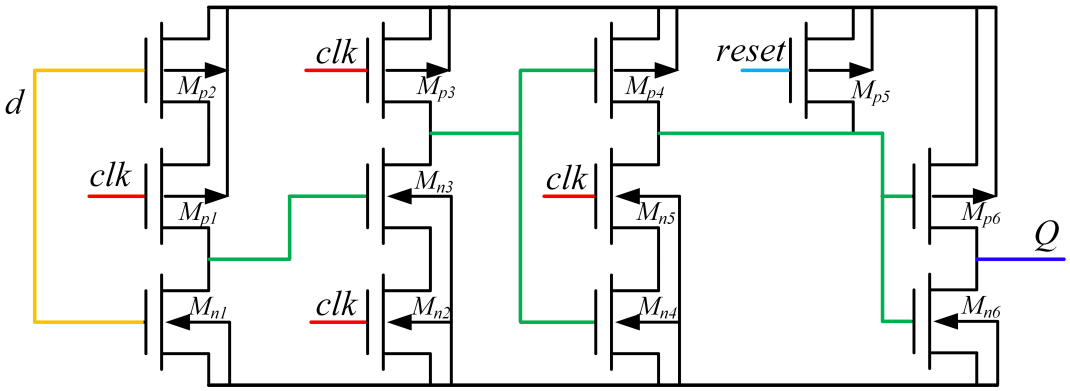

Figure 4.3: True single-phase clock (TSPC).

The reset transistor M_{p5} is designed with a normal threshold voltage rather than a low threshold voltage to reduce the leakage.

Table 4.1: Sizes of each transistor in TSPC.

	Length	Width	MOS type		Length	Width	MOS type
M_{n1}	60n	480n	LVT	M_{p1}	60n	960n	LVT
M_{n2}	60n	960n	LVT	M_{p2}	60n	960n	LVT
M_{n3}	60n	960n	LVT	M_{p3}	60n	960n	LVT
M_{n4}	60n	960n	LVT	M_{p4}	60n	960n	LVT
M_{n5}	60n	960n	LVT	M_{p5}	60n	120n	NM
M_{n6}	60n	960n	LVT	M_{p6}	60n	1.92n	LVT

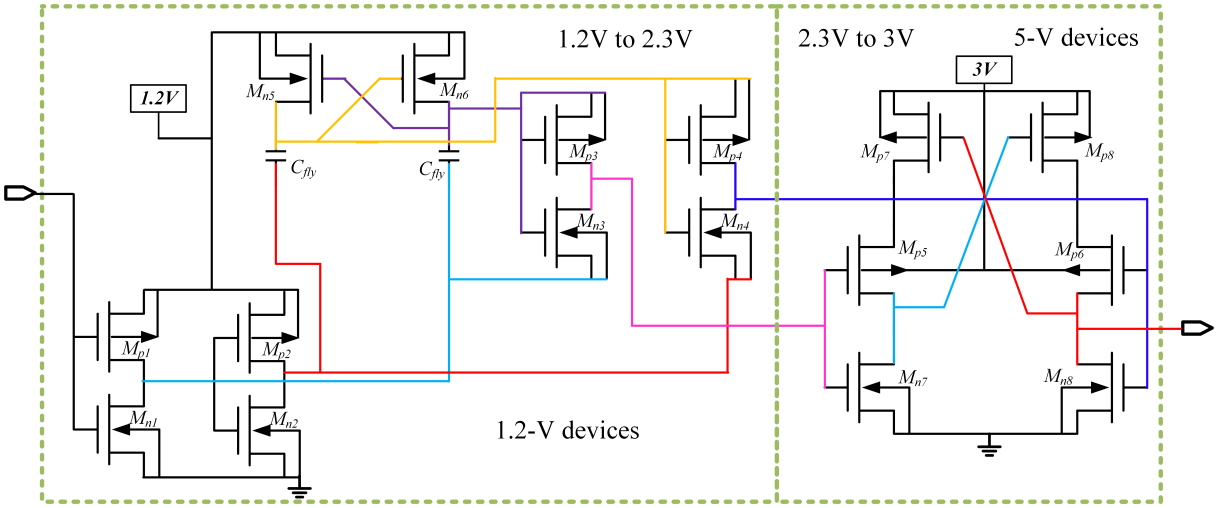

Figure 4.4: Level shifter with speed enhanced.

4.2.2 Level Shifter With Speed Enhanced

In order to speed up the level shifter process, the $1.2V$ signal will be converted to $2.3V$ firstly by $1.2V$ devices and then shift the $2.3V$ signal to $3V$ within the $5V$ device block. As shown in the left part of Figure 4.4, two flying capacitors are used to store $1.2V$, and then add it on the logic high. Two NMOS with deep N well on the top of the flying capacitors to control the charging process. On the output stage, the inverters have float logic low and make sure all the voltages across $1.2-V$ devices are within the safe range. Thanks to the higher logic high voltage provided by the first step, the normal level shifter can be implemented and generate a $3V$ signal pulse as wished.

4.2.3 Capacitively Coupled Level Shifter

In order to drive the M_{n1} in the VCSEL diode driver, the capacitively coupled Level shifter shown in [27] is implemented in the design. Since the charge within the capacitor will re-balance after the bottom plate of the capacitor becomes $3V$, the capacitor should be large enough. In this design, the value is around $10\times$ the gate capacitor of M_{n1}. Meanwhile, since there are power losses if two NMOS on top of flying capacitors is on at the same moment, the non-overlapping circuit is also implemented here to prohibit it. Since the large size of the flying capacitor, which is connecting with M_{n1} increases the time constant of the charging loop, the corresponding buffer is designed to make sure rising and falling times with a reasonable range. The important points' waveforms are also shown in the Figure.

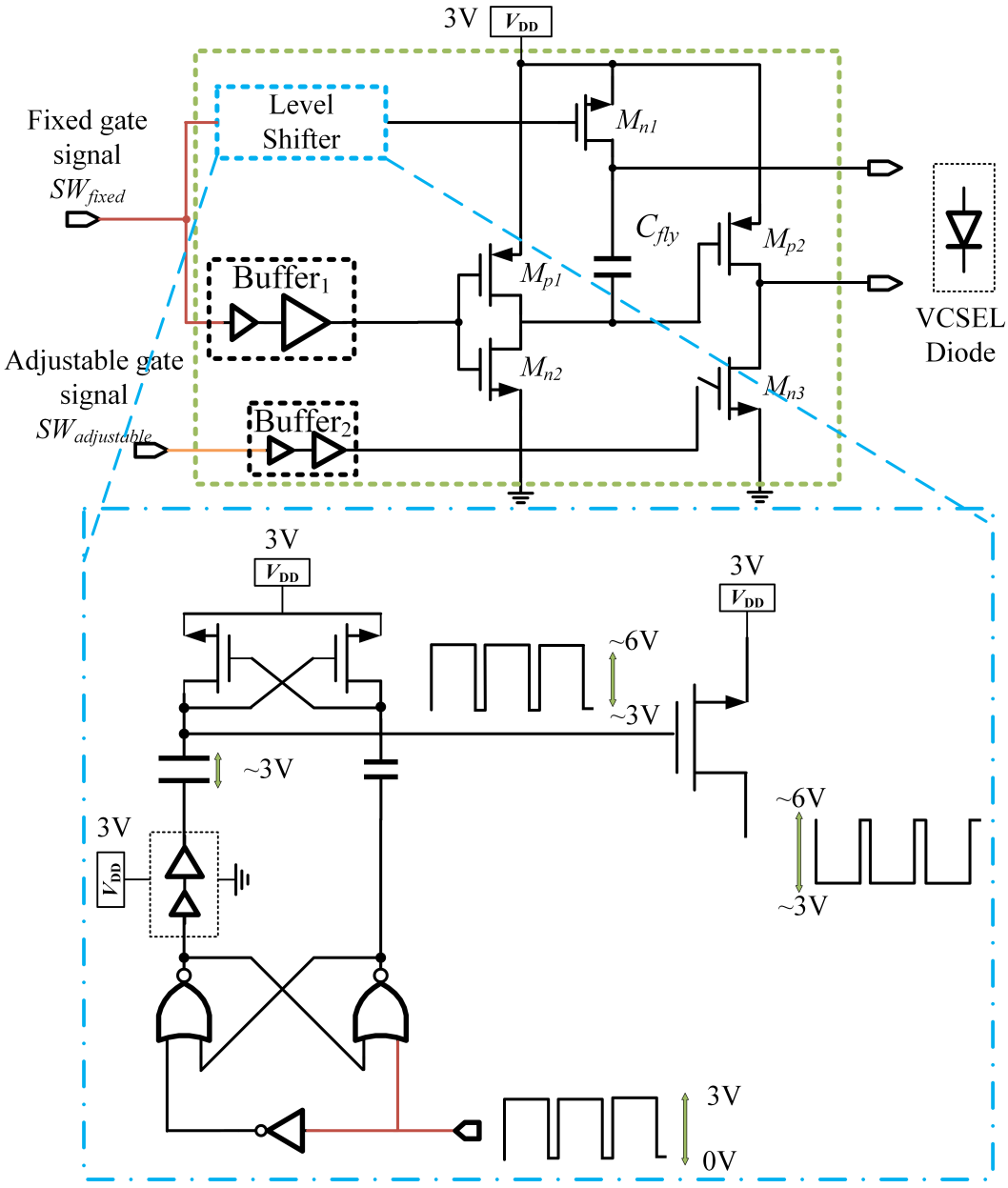

Figure 4.5: Capacitively coupled level shifter.

5 Simulation Results

5.1 Hybrid DC-DC Converter Part

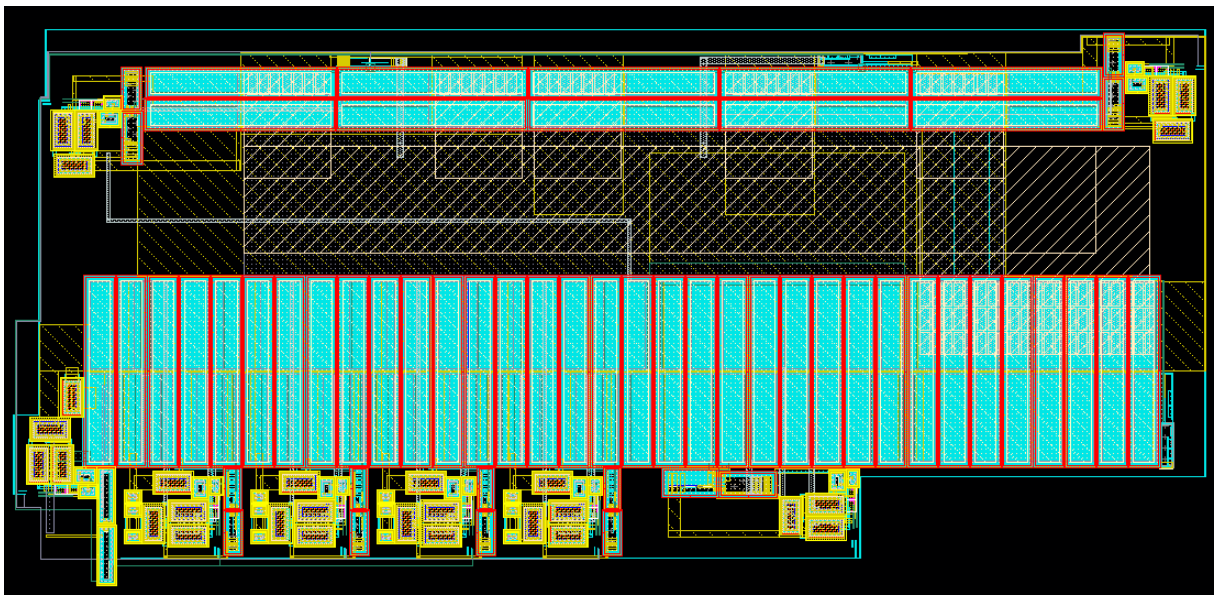

Figure 5.1: Layout of the proposed hybrid DC-DC converter.

The layout design of the proposed hybrid DC-DC converter is as shown in Figure 5.1, with TSMC 180*BCD* process. The active area is around $2mm^2$ and most of it is occupied by the power switches. Since the inductor and all the capacitors are off-chip components, only power switches, and gate drivers are included.
The start-up behavior of the converter is as shown in Figure 5.2. with the help of the boost stage, all the stress voltage within the converter could be limited to the safe range for $5-V$ devices.

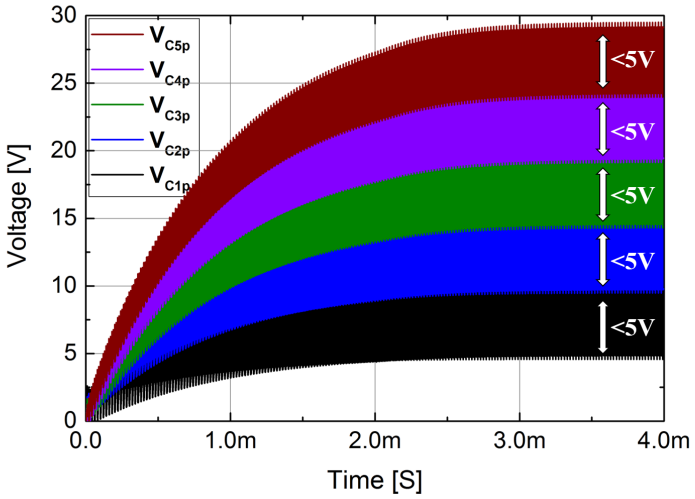

Figure 5.2: Start-up behavior of proposed hybrid DC-DC converter.

When the hybrid converter works in the stability status, the waveform of top plate voltages of capacitors in the switched-capacitor stage are shown in Figure 5.3. With the help of the stacking technique, all the $5-V$ devices are only facing voltage lower than $5V$. And the final output voltage is around $29V$.

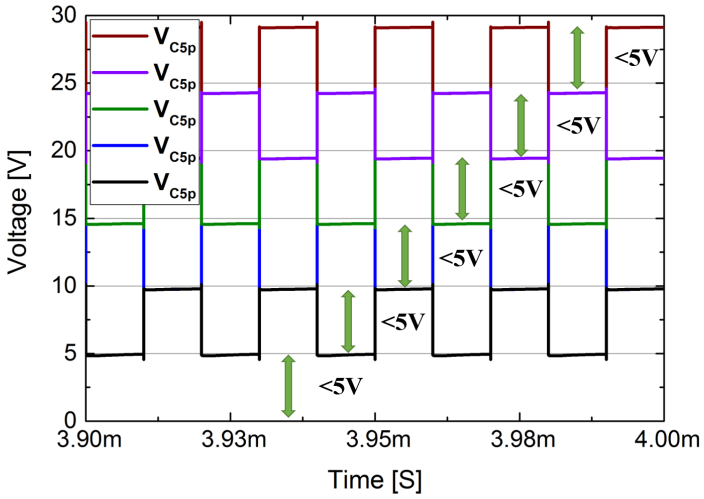

Figure 5.3: Stable behavior of proposed hybrid DC-DC converter.

The efficiency performance of the proposed hybrid converter is shown in Figure 5.4. The 93.08% peak efficiency is achieved when the input voltage is $3.7V$, the output voltage is $29V$, and the load current is $25mA$. Meanwhile, the high-efficiency range of the proposed hybrid converter is wider compared with a single boost converter or switched-capacitor converter.

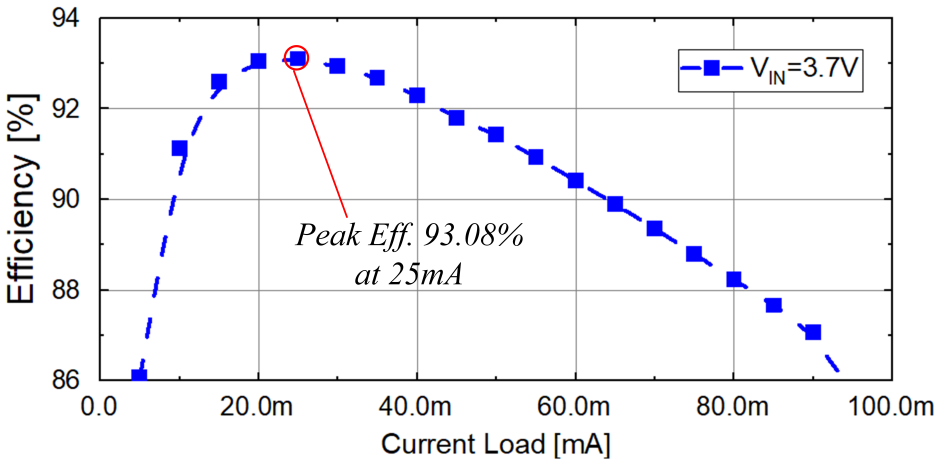

Figure 5.4: Post-simulation efficiency performance.

The comparisons are made in Table 5.1. Thanks to the smaller size power switches, the proposed design has competitive efficiency and area cost when achieves high VCR.

Table 5.1: Specifications and comparison table.

	This work	JSSC '21 [4]	JSSC '21 [6]
Technology	**180nm BCD**	180nm BCD	350nm CMOS
Input Volt. [V]	**3-4.2**	2.3-5	2-4.4
Max Output Volt. [V]	**30**	35	20
Load Range [mA]	**0-100**	0-100	10-250
Conversion Ratio	**6/(1-D)**	2/(1-D)	2/(1-D)
Switching Freq. [Hz]	**100k/50k**	1M/100k	2M
Output Capacitor [uF]	**10**	20	10
Inductor [uH]	**10**	10	2×3.3
DCR [mΩ]	**140**	140	-
Efficiency [%]	**93.08**	91.15	93.5
Load @ peak eff. [mA]	**25**	25	100
CR @ peak eff.	**7.8**	8.1	4.5
Power Switches	**5-V devices**	20-V devices	20-V devices
Active area [mm^2]	**2**	2.76	0.86

5.2 VCSEL Driver Part

The layout design of the proposed VCSEL driver with adjustable width is as shown in Figure 5.5, with SMIC 55*BCD* Technology. The active area is around $0.24mm^2$ and most of it is occupied by the on-chip mom capacitors and the power switches.
The width sweep results of the control signal pulse are shown in Figure 5.6. The corner and temperature influence is included in the Figure represented by different lines. The pulse widths are overall widening when under *SS* corner and $125°C$ and overall narrowing when under FF corner and $-40°C$. Meanwhile, the variances of the pulse widths are in the acceptable range.

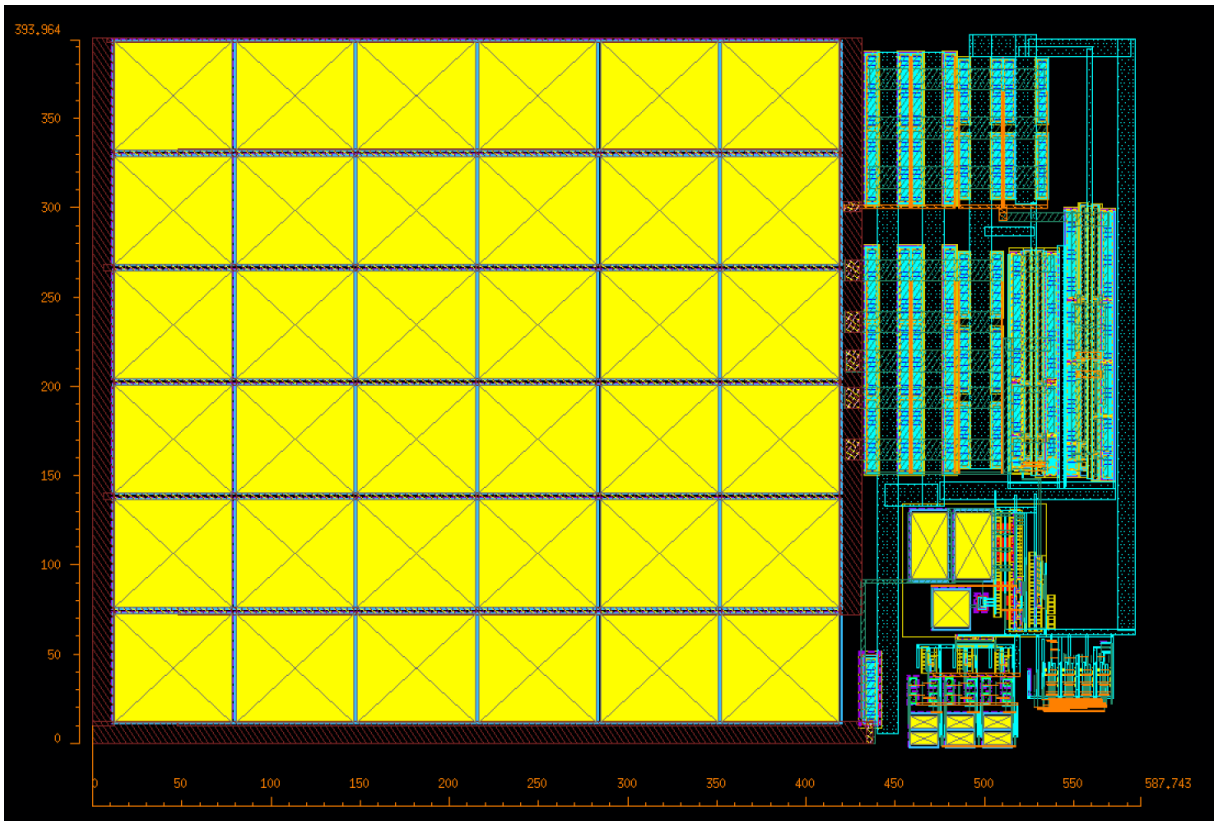

Figure 5.5: Layout of proposed VCSEL driver.

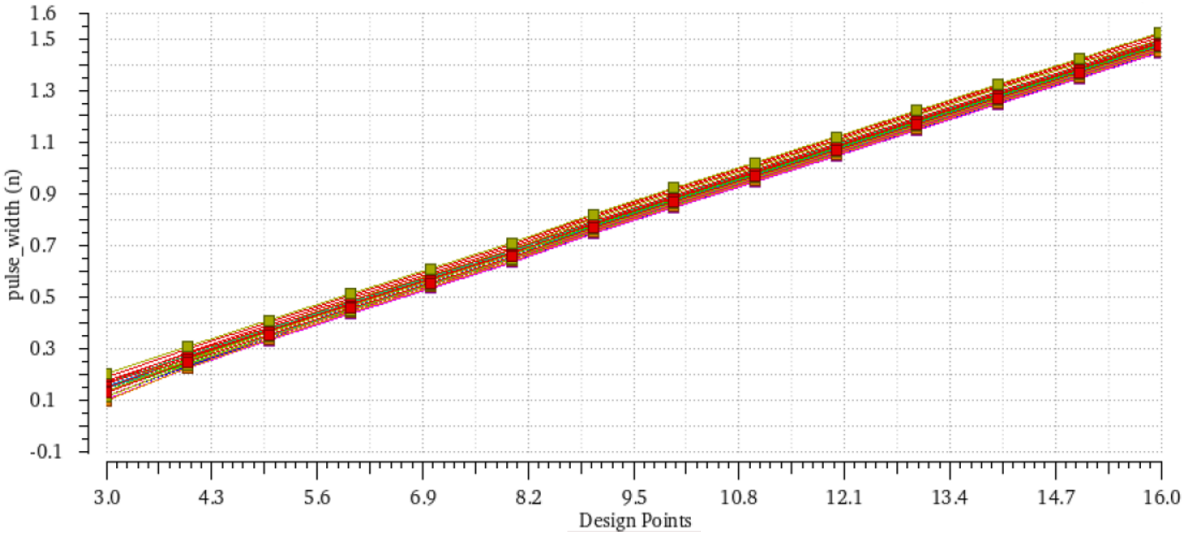

Figure 5.6: Width sweep results of control signal pulse.

The output voltage under different widths of the control pulse is shown in Figure 5.7. The results match the design specifications and achieve high output voltage width from 300ps to 1.6ns. The damping effect at the turning-off moment is reduced with the help of M_{p2} in Figure 2.26.

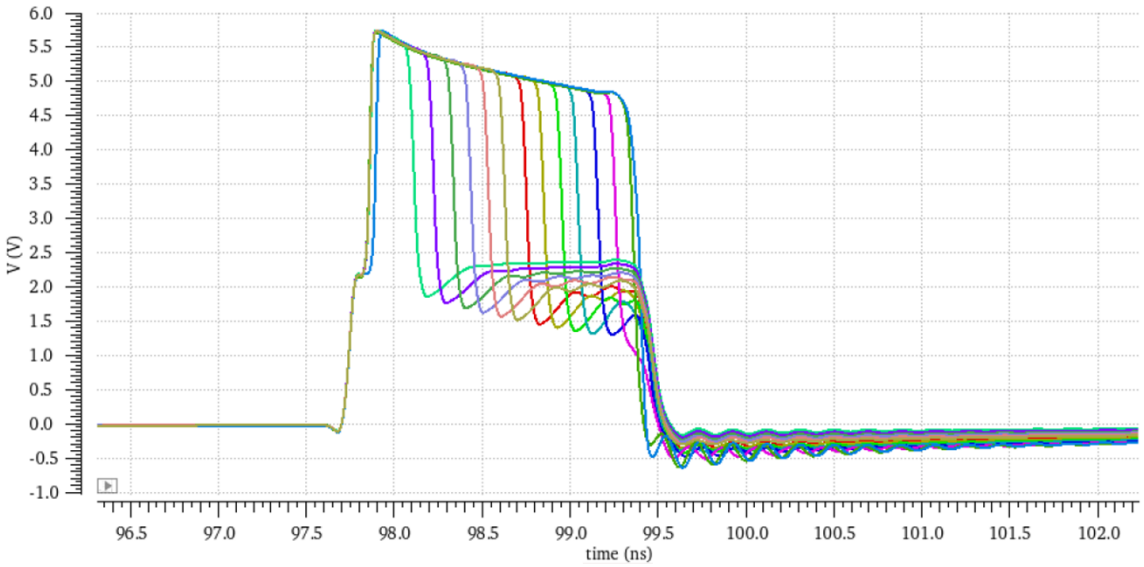

Figure 5.7: Output voltage with width sweep of the control pulse.

6 Conclusions

6.1 Summary of Main Contributions

A hybrid boost converter structure is proposed in this thesis. By merging the inductor-based boost converter with a 1:6 Dickson SC converter, all the power switches are employed with only on-chip $5-V$ devices. Meanwhile, thanks to the soft charging technique brought by the hybrid structure, the lower switching frequency is used in the switched-capacitor stage. The converter achieves a high power conversion efficiency of 93.08% under $3.7V$ input and $25mA$ current load. In addition, it keeps good efficiency within a wide load current range.
A pulse width adjustable VCSEL driver is designed in this thesis. High-speed TSPC is used in the logic part to overcome the influence of PVT and make sure all the clock signals enter the system with the original phase relationship. Level shifter with speed enhanced and capacitively coupled level shifter are used to meet the requirements of the design. The VCSEL driver is able to generate a pulse with a width of $300ps-1.6ns$.

6.2 Future Work

6.2.1 Interleaved Switched-Capacitor Stage

The second stage of the proposed hybrid converter is a general two-phase control stage. Usually, the interleaved switched-capacitor stage is able to replace the original second stage and reduce the ripple voltage at the output. However, in order to implement interleaved stage, the control clock also needs to be interleaved. As a result, the control signal generation block needs a higher frequency base clock to generate interleaved control clock.

6.2.2 Control System for Switched-Capacitor Stage

The proposed hybrid converter only has a control system for the inductor-based stage and used a fixed switching frequency for the switched-capacitor stage. Therefore, the VCR range of the proposed hybrid converter is been limited. If a hybrid control block with different control modes can be implemented, which controls two stages separately, the equivalent VCR range will be enlarged, especially towards the lower VCR direction. However, achieving a wide VCR range with high efficiency is very challenging, which means the control system should be designed carefully and controls the hybrid converter in the right working status for different VCRs.

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