Saddle Add-On Metallization for RF-IC Technology

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***Abstract*—A cost-effective add-on process module for reducing ohmic losses of radio-frequency (RF) inductors and interconnects in RF/BiCMOS and RF/CMOS technologies built on CMOS logic processes is proposed. The module is based on the local thickening of the top metal layer of the thin CMOS interconnects through copper (Cu) electroplating in selected areas. The combination of dense Cu-interconnects in the CMOS logic sections, of thick Cu top-level wiring through local Cu electroplating in the RF sections, and of aluminum (Al) capping of the bond pads provides an optimum tradeoff between packaging requirements, quality of passive components and interconnects, and cost. A special wet-etch process sequence for removal of the Cu-seed and adhesion films from the exposed top metal layer is described. A record quality factor of ~ 13 for a 10-nH inductor on a conventional 5-Ω-cm silicon substrate is demonstrated.**

***Index Terms*—BiCMOS integrated circuits, CMOS integrated circuits, conductivity, conductors, copper, electromagnetic induction, inductors, integrated circuits, losses, magnetic fields, microwave devices, passive circuits, scattering parameters measurements, silicon.**

I. Introduction

IT HAS BECOME common practice in the development of high-performance RF/BiCMOS and RF/CMOS to migrate an existing CMOS logic process along with the associated ASIC libraries to radio-frequency (RF) process development and to adopt the interconnect scheme unaltered from CMOS [1], [2]. Such interconnects are designed for a minimum pitch (width + space) for the particular metal layer thickness to achieve maximum integration density. An optimized layout of an integrated spiral inductor, however, is based on a rather large metal pitch in order to minimize the ohmic losses in the spiral coil [3]. The straightforward migration of the CMOS interconnect scheme to the RF process [Fig. 1(a)] leads to a comparably low quality factor (Q) of spiral inductors. This situation worsens with CMOS downscaling [4], which is surprising at first since the number of metal layers increases as the CMOS is advanced [5]. With downscaling, however, the thicknesses of metal and dielectric layers are reduced. It can be seen from the simplified sketch of three technology generations in Fig. 2, that the distance between the top metal layer and the silicon substrate remains at first order constant. The thickness of the upper metal layers, at which usually the spiral coil of the inductor is built, however, is reduced with downscaling. That means, that for a given inductor area the oxide capacitance to the substrate stays constant and the coil resistance increases

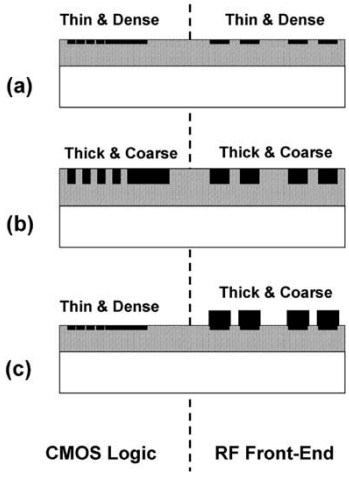

Fig. 1. Illustration of three multilevel interconnect technologies migrated from CMOS logic to RF/BiCMOS or RF/CMOS. (a) Unaltered interconnect scheme with a thin top metal layer that is insufficient for integration of RF passive components. (b) Interconnect stack with fat top metal layer that has reduced effectivity for interconnecting logic CMOS. (c) The combination of thin/dense interconnects for logic CMOS and fat metallization for RF passive components.

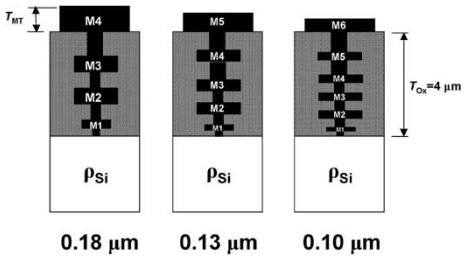

Fig. 2. Interconnect schemes for three CMOS generations [4]. Only one global metal layer is assumed for each technology generation.

with technology advancements. The consequence is that the maximum $Q(Q_{\max})$ is decreased and shifted to a higher frequency $[f(Q_{\max})]$ [3]. Inductor redesign for maximum Q at the target frequency would result in wider metal lines and thus larger coil area and higher capacitance to the substrate [3]. The $Q_{\max}$-values for given inductance and $f(Q_{\max})$, which can be reached through an optimum inductor layout, therefore tend to decrease with technology downscaling (Fig. 3). This trend can to some extent be alleviated by taking advantage of shunting of metal layers (Fig. 3) [6]. Nevertheless, moving to a more advanced technology generation to utilize higher device performance for larger bandwidth is strongly hampered by the fact that the inductor-Q cannot be raised in proportion with the device performance. The inductor-Q can be improved by increasing the thickness of the top metal layer adopted from the CMOS [7], [8]. The associated large metal pitch, however, will make this layer rather ineffective for interconnecting the dense CMOS logic sections [Fig. 1(b)]. From an economic point of

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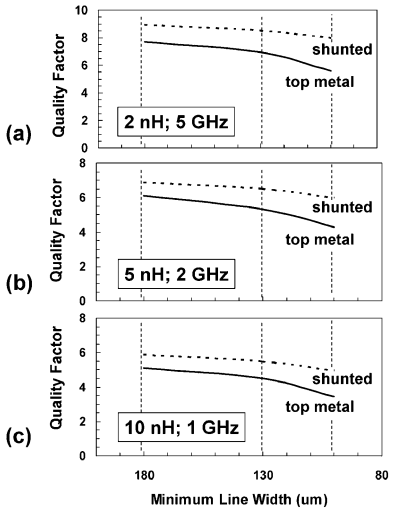

Fig. 3. (Solid lines) Simulated quality factors of optimized 2, 5, and 10-nH inductors for three CMOS generations. Coils built at the top metal layer are compared to (dashed lines) inductors that have shunted M3/M4, M3/M4/M5, and M3/M4/M5/M6 layers for 180, 130, and 100-nm CMOS, respectively. (For details about the simulation program, see Section III.).

view one would then practically invest in an additional overly thick ("fat") metal layer to mainly boost the inductor-Q. In any case one would accept a weak tradeoff, either economically or in circuit performance. It is thus obvious that the most desirable interconnect scheme in a RF integration process would provide both thin and dense wiring for the logic circuits and thick and coarse metal for fabrication of the RF passive components [Fig. 1(c)].

An additional complication arises with the copper (Cu) multilevel interconnects of the current advanced CMOS in conjunction with the requirements for wire bonding. Copper, on the one hand, is attractive for inductor design since its resistivity is only about 60% of that of aluminum (Al). Although high-Q inductors have been demonstrated by using Al-interconnects [8], the best results so far were achieved with Cu-metallization [9]. The multi-level interconnect schemes of almost all advanced CMOS integration processes are based on Cu metallization [1], [10], [11]. A Cu top layer, on the other hand, does not provide a reliable bond-wire connection due to excessive Cu oxidation [12]. Cu-interconnect schemes must therefore either include an Al-cap covering the bond pads [12], [13], or that top metal layer of the Cu-interconnect stack must be an Al layer [7]. The Al-cap is typically applied *after* deposition of the dielectric passivation layer and the opening of the bond pads, i.e., at the end of the chip fabrication process. Extension of the Al-cap layer, applied *prior* to the passivation, to cover all top metal wires with thick Al is not well possible due to the density requirements in the CMOS logic sections. That is, because removing such a thick Al film from the top metal layer in the CMOS logic sections to leave the Al in place only over the bond pads and in the coarse RF circuit sections is very difficult because of the poor selectivity of the Al dry-etch removal over the Cu. Only a local application of the Al-cap layer *after* the passivation, e.g., over the bond pads and the inductor coils, seems feasible. The thickness of the Al-cap layer is limited due to process constraints and thus leads only to a slight improvement in inductor-Q. It is evident that the Al-cap requirement does not apply to the more conservative Al-interconnect schemes [14]. The poor trade-off between wireability of the dense CMOS logic circuits and the quality of the RF passive components, however, is of concern in terms of the optimum local thickness of the top metal layer. Desired is thus a processing scheme that provides dense wiring in the CMOS sections and a thick Cu layer over certain RF structures [Fig. 1(c)], while Al bond pads are provided. That leads to two attractive tradeoffs in current RF integration processes Fig. 4(a1)–(c1) and (a2)–(c2).

1) In an Al-interconnect stack or a Cu-interconnect scheme with an Al top layer [Fig. 4(a1)] a local thickening of the metal in the RF sections can be arranged by local Cu-plating [Fig. 4(b1)]. A passivation layer, in which windows are opened over the bond pads, is added at the end [Fig. 4(c1)].
2) In the full Cu-interconnect scheme [Fig. 4(a2)] an Al bond pad is formed after the passivation [Fig. 4(b2)]. That Al layer is also placed over certain RF structures. Finally, local thickening of the metal by Cu-plating is achieved over those RF features [Fig. 4(c2)]. Metal passivation is then only provided in the dense CMOS sections.

A third relevant case relates to a full Cu-interconnect scheme followed by local Cu-plating over the RF features and by the dielectric passivation and the formation of the Al bond pad. That concept, however, is less favorable compared to the tradeoffs illustrated above, as will be shown later.

In this paper, we present a novel metallization add-on module, called Saddle add-on metallization (SAM) that enables those desired tradeoffs at minimum additional cost. The SAM concept and process are described in Section II. Experimental results, through which the effectiveness of SAM is demonstrated, are discussed in Section III. Conclusions follow in Section IV.

II. SAM Concept and Process

The reduction of the metal losses in an integrated spiral inductor is most important at low RF, at which the inductor area tends to be large and the inductor-Q is limited by the ohmic losses in the coil [3]. Both reduction of the ohmic loss and of the coil area can be achieved by raising the metal thickness, as explained in Section I. Schemes, in which an additional fat metal layer, separated by a thick dielectric layer from the CMOS interconnect stack, is provided, had been published [7]. Those structures aim for addressing both ohmic coil losses and substrate losses at the same time [3], [6]. Even though effective, those add-on processes require at least two additional mask layers and nonstandard process steps and are therefore quite costly. Furthermore, reducing the substrate losses by spacing the inductor coil away from the substrate may be far less relevant than lowering the ohmic losses in the coil at low RF. That is, because future RF integration processes will likely adopt high-resistivity silicon (HRS) substrates to reduce substrate losses and crosstalk at the same time [15], [16]. Sole reduction of the metal losses may thus be sufficient, if achieved at reduced cost. This is the main objective of the SAM concept, in which the top metal layer is increased in thickness only where needed and not where the inherent large metal pitch causes a disadvantage [4]. The SAM

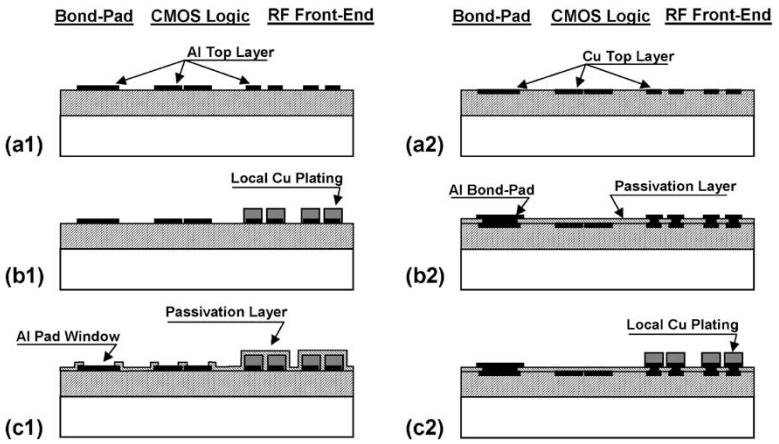

Fig. 4. Illustration of the introduction of SAM into an interconnect scheme with either an Al [left: (a1)–(c1)] or a Cu [right: (a2)–(c2)] top metal layer.

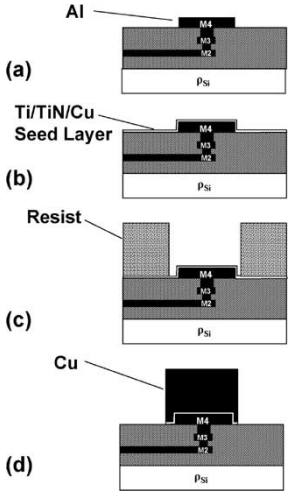

Fig. 5. SAM for local increase of top metal layer thickness. (a) CMOS interconnect stack after finalizing the top Al-layer fabrication. (b) After Ti–TiN adhesion and Cu-seed layer deposition. (c) After formation of the photoresist mold. (d) After Cu-electroplating and resist and seed/adhesion layer removal.

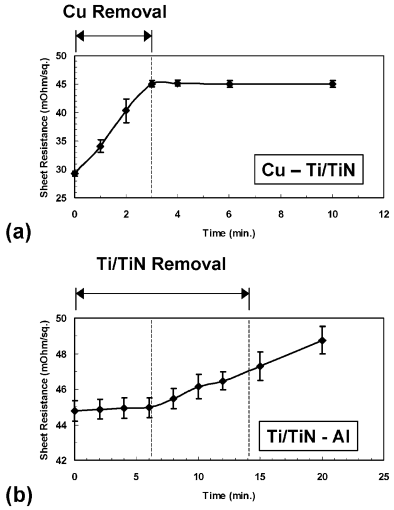

Fig. 6. Indication of etch rate selectivities (average and std. variation) by sheet resistance measurements over time. (a) Cu-seed removal with selectivity to the Ti–TiN adhesion layer with underlying Al layer. (b) Ti–TiN adhesion layer removal from the Al.

process module is applied right after the multi-level interconnect fabrication of the CMOS and prior to the Al-capping of the bond pads [Figs. 4(b) and 5(a)]. First, a Ti–TiN barrier layer (10/50 nm) and a Cu seed layer (200 nm) are deposited onto the wafer before any passivation layer is added, as it is usually done after the final metal layer fabrication [Fig. 5(b)]. The Ti layer is included to improve the adhesion between the seed layer and the Al. Next, a deep photoresist mold is aligned to the top CMOS metal layer with some overlap at the edges [Fig. 5(c)]. The mold is then filled with Cu by electroplating, forming a Cu-saddle over the top metal layer of the CMOS process after the photoresist is stripped off [Fig. 5(d)].

An important aspect of the SAM process module is the possibility for selective removal of the Cu seed and Ti–TiN adhesion layers over the exposed top Al layer. Only if this removal can be done with sufficiently high selectivity can the SAM module be applied with only one photomask. This is an important issue because otherwise the economic advantage over the mentioned concepts based on an additional uniform fat metal layer with thick isolating dielectric underneath would be marginal [7], [8]. In the following, a novel seed/adhesion layer removal process, which is instrumental in achieving that goal, is described. Appropriate selectivities of the different etches had been attempted in the development of the SAM module. After the photoresist mold is stripped off both the plated SAM structure and the Cu seed layer are exposed. Since the Cu-seed layer is very thin in comparison to the SAM, a short wet etch in $Na_2S_2O_8/H_2SO_4/H_2O_2$ is used for its removal. Only $\sim$ 200 nm of Cu of the SAM features will be removed. This Cu etch is developed to have a high selectivity to Ti–TiN (160:1) and to Al, so that the Cu seed layer can entirely be removed without much affecting the metal layers underneath [Fig. 6(a); Table I]. Complete removal of the Cu-seed prior to the Ti–TiN etch ($NH_4OH/H_2O_2/H_2O$) is crucial because the etch rate of Al is considerably high in the Ti–TiN etch and the loss of the Al should be minimized by keeping the Ti–TiN etch as short as possible. Fig. 6(b) shows the sheet resistance measured during the Ti–TiN etch after the Cu-seed layer was removed. The small change in sheet resistance during the first 6 min is obviously a result of the four-point probes of the test apparatus punching through the thin Ti–TiN film so that the thinning of that film was not well apparent in the sheet resistance measurements. After that time the sheet resistance started to change even

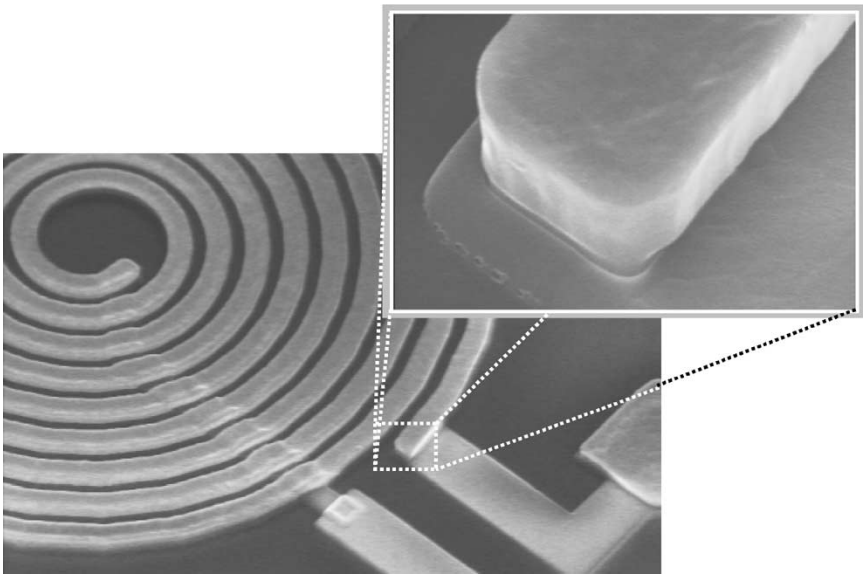

Fig. 7. SEM micrograph of a nine-turn inductor coil built with 1-μm-thick Al top interconnect layer combined with a 3.4-μm-thick SAM layer (prior to the passivation). The contour of the SAM add-on layer is shown by the SEM in the inset.

TABLE I
ETCH RATES OF CU, TI/TIN, AL, AND SiO_2 FOR THE CU-ETCH ($Na_2S_2O_8/H_2SO_4/H_2O_2$) AND THE TI/TIN ETCH ($NH_4OH/H_2O_2/H_2O$) USED FOR THE REMOVAL OF THE SEED/ADHESION LAYERS

Type of Etch:	Etch Rate (nm/min.) of:			
	Cu	Ti/TiN	Al	SiO_2
Cu	57	~ 0	0.35	-
Ti/TiN	14.8	4.2	3.45	~ 0

though the Ti–TiN removal was not completed, as evident from visual inspection [Fig. 6(b)]. Apparently, etching of the underlying Al layer already took place through pinholes in the Ti–TiN film before the Al film was exposed. Nevertheless, only $\sim 3\%$ of the Al layer was sacrificed, so that this etch combination qualified well for the removal of the Cu-seed and Ti–TiN adhesion layers. The loss of Cu thickness of the SAM features will be another ~ 200 nm, amounting to a total Cu loss of ~ 400 nm during the Cu-seed and Ti–TiN layer removal.

The loss in thickness of the top metal layer is considerably increased if a full Cu-interconnect stack is used, which is mentioned in Section I as the third relevant processing option. The etch rate of Cu in the Ti–TiN etch is $\sim$ four times higher than that of Al (Table I). That means that ~ 150 nm of Cu thickness of the top metal layer would be sacrificed, if one assumes the same pinhole effect as observed for the Ti–TiN removal over Al [Fig. 6(b)]. That process option would therefore only become feasible if one reduces the pinhole density of the Ti–TiN film considerably and if one optimizes the Ti–TiN etch to have a lower etch rate of Cu relative to that of Ti–TiN.

III. EXPERIMENTS AND DISCUSSIONS

Circular spiral coils were built by using the equivalent M3 and M4 layers of a four-metal level, 0.18-μm CMOS process on a 2-5 Ω-cm silicon substrate. The M4 layer (1-μm-thick Al, spaced 4 μm from the silicon substrate) was used for the coils with the underpass contact at M3 (0.7-μm-thick). A 4-μm-deep photoresist mold was used, and the final SAM Cu thickness was 3.4 μm. Fig. 7 shows the SEM micrograph of a Cu-plated spiral inductor prior to the passivation [Fig. 4(b)]. From the inset it can be seen that the sidewalls of the SAM layer were sufficiently steep and its surface was flat. It should be noted that the uniformity of the electroplating process was optimized by adding an auxiliary electrode, which was connected to a current source different from that used for plating the wafer, separately near the wafer edge [17].

The spiral inductors were designed and optimized by using a fast, physics-based model on basis of a concentric-ring approximation [18]. In that model, the circular spiral coil is replaced by a series connection of concentric rings with the same number of turns (N), track-width (W), and spacing (S). The overall diameter of the system is determined by equating the overall lengths of the spiral coil and the system of rings. Exploiting the rotational symmetry of the concentric-ring system, one can then simplify the field equations to arrive at a fast, semi-analytical, physics-based model. The model takes into account substrate RF loss as well as the nonuniform distribution of the current density in the inductor windings due to the skin- and current-crowding effects. The concentric-ring model has been shown to be in good agreement with experimental data [3].

Fig. 8 shows experimental and simulated characteristics of a 10-nH SAM inductor, designed for $Q_{\max}$ at 1 GHz. A value $Q_{\max} = 13.25$ was measured; this was a 3.2-fold increase over the Al inductor prior to SAM (not shown in Fig. 8). Even, if the Al coil is optimized for the $Q_{\max}$ at 1 GHz by varying conductor width (W), spacing (S), and number of turns (N), the resulting $Q_{\max}$ is still 2.8 times lower than that of the SAM inductor. The simulation results in Fig. 8 also show that layer shunting does little to reduce that difference. Shunting reduces the ohmic loss in the conductor, but increases the substrate RF

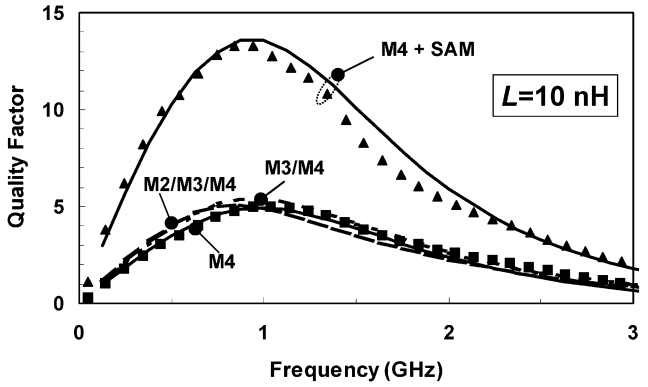

Fig. 8. Comparison of optimized 10-nH inductors, built at M4 or with shunted metal, to an inductor fabricated with SAM (markers: data; lines: simulations).

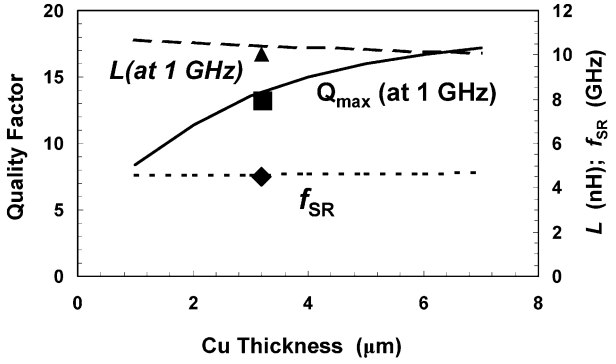

Fig. 9. Simulated Q, L, and $f_{\rm SR}$ of a 10-nH SAM inductor as function of Cu thickness. Markers indicate the experimental results.

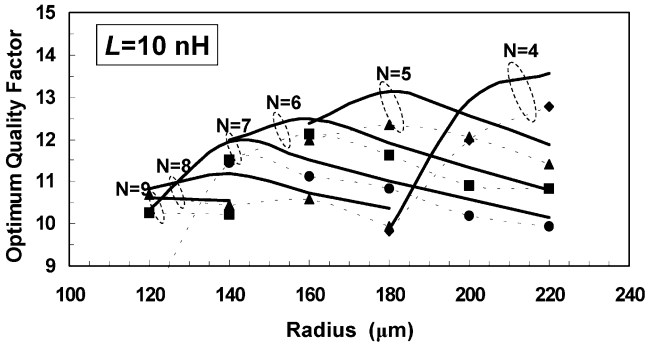

Fig. 10. Quality factor of optimum 10-nH coil designs at fixed numbers of turns (N) as a function of radius at the target frequency of 1 GHz. Experimental results (markers, dashed lines) and simulations (solid lines) are compared (5%–10% difference).

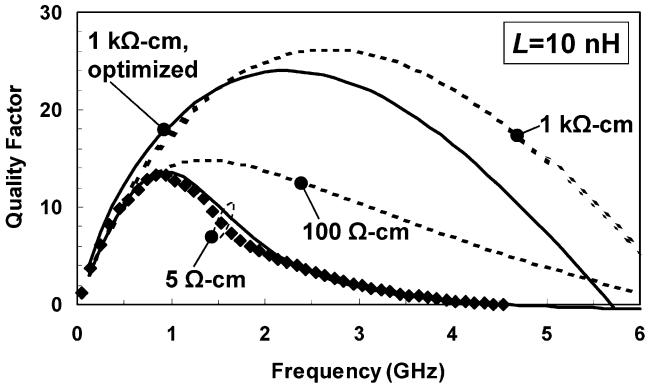

Fig. 11. Quality factor versus inductance of the 10-nH inductor on a 5-Ω-cm silicon substrate (lines = simulation; markers = measurement), and simulated characteristics on 100-Ω-cm and 1 k-Ω-cm substrates. Also shown is a redesign of the coil on 1 k-Ω-cm silicon.

loss by reducing the substrate-coil spacing leading to a larger substrate-coil parasitic capacitance [6]. SAM, however, does not reduce the substrate-coil separation. The reasonably good agreement of simulation and measurement allows for extrapolation of design parameters to gain further insight into the merits of the SAM process. One can, e.g., study the potentially diminished effectiveness of SAM with increasing Cu-thickness due to skin effect and interwire capacitance (between adjacent windings with sidewalls facing each other). In order to study these effects we have simulated the inductance, the maximum quality factor, and the resonance frequency of a $\sim$ 10-NH, Cu-plated coil as function of Cu-thickness (Fig. 9). The skin effect was indeed evident from the trend to saturation of $Q_{\rm max}$ with increasing Cu-thickness. The inter-wire capacitance was increased only slightly and was compensated by a decreasing inductance with SAM thickness, so that $f_{\rm SR}$ was affected only very little (Fig. 9). As a result, $Q_{\rm max}$ of the 10-nH coil can in principle be brought to a value of ~ 18 by raising the SAM thickness to ~ 8 μm without any considerable degradation of the electrical characteristics. It is important to note that, in contrast to sputtered Al, Cu plating is a cold process and thus little prone to mechanical stress. Such thick SAM layers are therefore well feasible from a process technology point of view.

Fig. 10 indicates how the 10-nH SAM inductor can be optimized for both $Q_{\rm max}$ and coil area. Using the concentric-ring model, we have calculated the maximum attainable quality factor obtained by optimizing the width (W) and spacing (S) of the coils for a given radius (R) and number of turns (N). The experimental results (represented by markers and dashed lines) are 5-10% below the simulated ones. Note that reduction of the coil radius from 220 to 120 μm (70% area reduction) only leads to a 15% lower $Q_{\rm max}$. SAM thus allows one to build a 10-nH inductor with nine turns and $Q_{\rm max} = 11.5$ at only 240 μm diameter on 5-Ω-cm silicon (Fig. 10).

The extrapolations to higher substrate resistivities in Fig. 11 indicate, that the effect of SAM in reducing ohmic losses in the coil is far more significant at 1 GHz than the substrate losses. Simulations for the 10-nH coil of Fig. 5 show that changing the substrate resistivity from 5 to 100 Ω-cm barely increases Q at 1 GHz, whereas the increase in $Q_{\rm max}$ upon using a high-resistivity 1 k-Ω-cm wafer is only 25%. Had we optimized the geometry of the coil for the high-resistivity substrate, the difference would hardly have been noticeable at 1 GHz (Fig. 11).

The effectiveness of SAM in improving the quality factor of integrated inductors becomes evident if one compares the results obtained, with the (experimental) values for $Q_{\rm max}$ at different inductances, achieved for a conventional interconnect process (1-μm Al, 10 Ω-cm Si) [3] and an innovative process based on a 4-μm Cu interconnect process on a 3 kΩ-cm float-zone silicon substrate [19]. The result for the 10-nH SAM inductor nearly matches that achieved with the innovative process, in spite of the conventional 5-Ω-cm substrate used, indicating once again the importance of ohmic loss reduction by SAM. For smaller inductors, however, where the maximum quality factor $Q_{\rm max}$

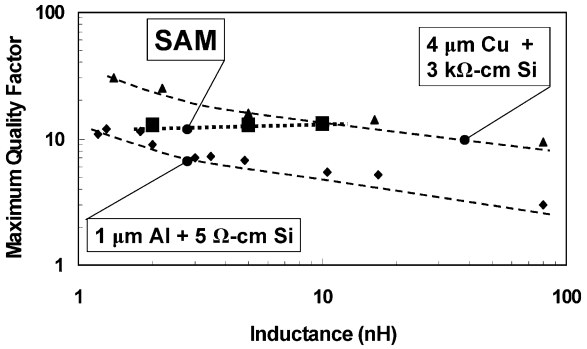

Fig. 12. Maximum Q versus inductance for 2-, 5-, and 10-nH SAM inductors on 5-Ω-cm silicon in comparison to results for conventional (1-μm Al, 5-Ω-cm Si) and optimum (4-μm Cu, 3-kΩ-cm Si) interconnect processes [8].

is achieved at higher frequencies, substrate RF loss becomes dominant. Nevertheless, considerable enhancement of $Q_{\max}$ is evident at all inductance values addressed in Fig. 12.

IV. Conclusions

SAM offers a cost-effective add-on process module for reduction of ohmic losses in RF inductors and interconnects. SAM is based on the local thickening of the top metal layer of the thin CMOS interconnects by Cu-plating and is particularly suitable for enhancing RF/BiCMOS and RF/CMOS technologies build on logic CMOS processes. The SAM process presented here is optimized for an Al top metal layer or a Cu top metal layer with an Al cap. The effectiveness of SAM is expressed by a record quality factor of ~ 13 achieved for a 10-nH inductor on a conventional 5-Ω-cm silicon substrate. SAM is particularly effective in improving the quality factor of large inductors operating at low radio frequencies. Furthermore, it allows the reduction of the size of large inductors without any significant loss of quality factor.

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