CONTROL OF A 3-PHASE MOTOR DRIVE EMPLOYING A SLIM DC-LINK

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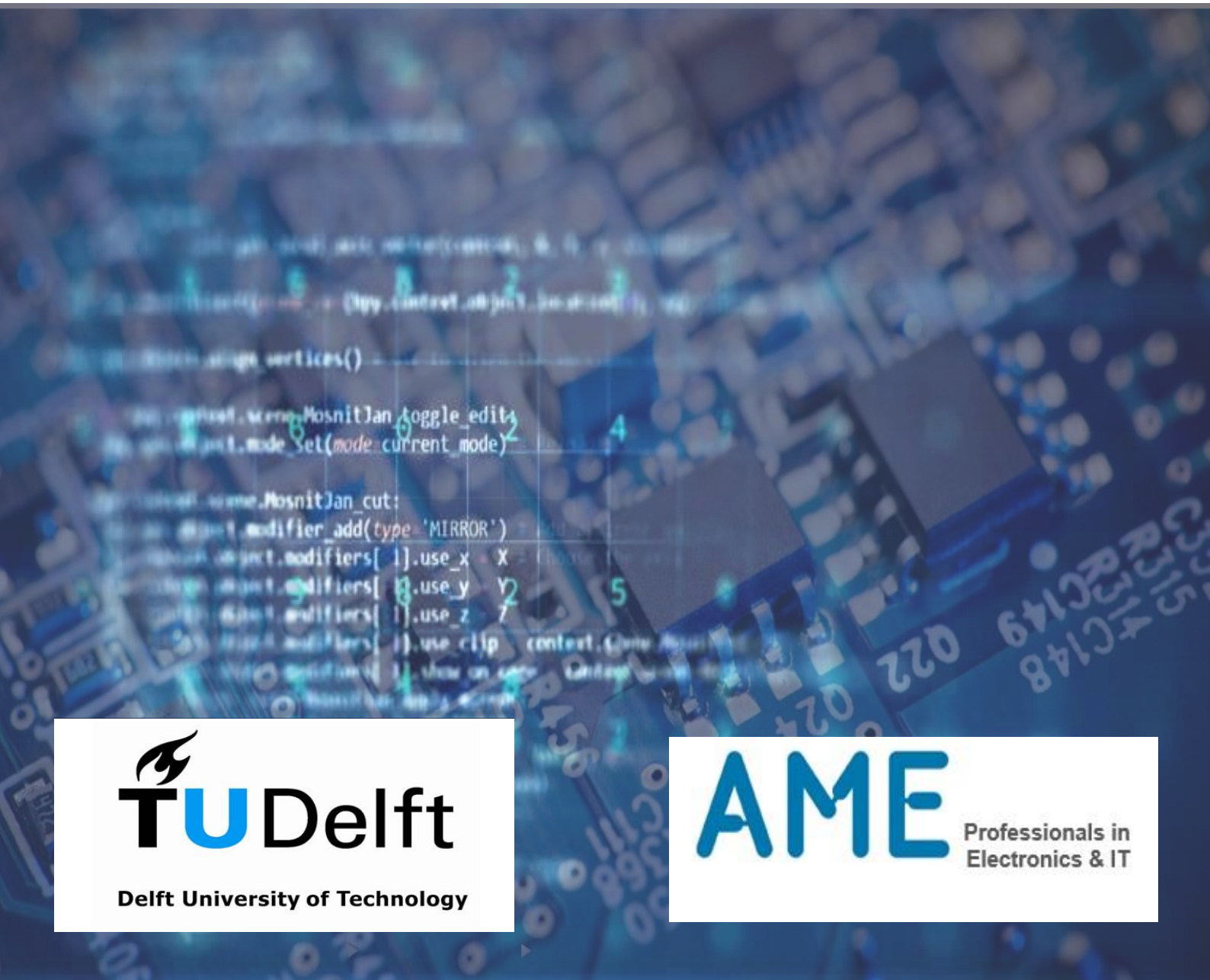

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by Samyuktha Sivaram

Abstract

A variable speed AC motor drive, fed by a 3-phase AC supply, often consists of a 3-phase bridge diode rectifier, a DC link capacitor and a pulse width modulated inverter. Recently, a new type of capacitor known as film capacitor or slim capacitor has become popular for use in DC link. This capacitor has a lower value of capacitance and a longer life span than the conventional electrolytic capacitor. A film (slim) capacitor is advantageous over the electrolytic capacitor for use in the DC link because, for a low power motor, it results in a varying DC link voltage. This produces a less distorted grid current thereby improving the power factor. However, drives with slim DC link fed by a soft grid exhibits the tendency to oscillate at higher frequencies. This can be attributed to the LC resonance between the grid inductance and the small DC link capacitance, which results in significant but unwanted voltage ripples on the DC link. The unwanted harmonics affect the performance of the motor and the current drawn from the grid. As a result, the motor drive does not comply with the IEC 61000-3-2 harmonic standard. The objective of this project is to formulate, model and test a control algorithm to suppress the effects of the LC oscillations. This thesis proposes a novel compensation method that estimates the ideal DC link voltage without the unwanted ripples and feed-forwards the reconstructed DC link voltage to the motor drive algorithm, thereby altering the behavior of the motor drive to be more resistive such that the ripple gets damped. By doing so, the current drawn by the motor from the grid will have lesser harmonic content. Therefore, the power factor of the system will improve and the system will adhere to the harmonic standards.

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To my beloved Mother and Father...

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Abbreviations

AC	Alternating Current
ADC	Analog to Digital Converter
AME	Applied Micro Electronics
AMDF	AME Motor Drive Framework
D	Derivative Controller
d-axis	Direct axis
DC	Direct current
EMI	Electromagnetic Interference
FOC	Field Oriented Control
I	Integral Controller
LPF	Low Pass Filter
P	Proportional Controller
PLL	Phase Locked Loop
PMSM	Permanent Magnet Synchronous Motor
PWM	Pulse Width Modulator
q-axis	Quadrature axis
RPM	Revolutions Per Minute
SVM	Space Vector Modulation
SVPWM	Space Vector Pulse Width Modulation
THD	Total Harmonic Distortion
VCO	Voltage Controlled Oscillator
VSD	Variable Speed Drive

List of Symbols

N_s : Synchronous speed of the PMSM.

f : Frequency of the AC supply.

P : Number of stator pole pairs.

V_a, V_b, V_c : Voltage of the phase A, B and C respectively of the 3 phase AC supply.

V_{in} : Voltage waveform of a single phase AC supply.

I_a, I_b, I_c : Current drawn from phase A, B, C respectively of the input supply.

V_{dc} : Voltage across the DC link.

a', b', c' : The three phases of the stator.

I'_a, I'_b, I'_c : Current drawn by the three phase a', b' and c' of the stator windings respectively.

$v_1, v_2, v_3, v_4, v_5, v_6$: Switching state vectors of the inverter's upper leg.

V_{ref} : Reference voltage for the space vector modulation.

T_{sw} : Switching period of the PWM.

t_1, t_2, t_7, t_8 : Time for which switching states v_1, v_2, v_7, v_8 are realised respectively.

$a-b-c$ axis : Three phase stationary reference frame where the axes are 120° apart from one another.

$\alpha-\beta-0$ axis : Two phase stationary reference frame where the axes are 90° apart.

$d-q-0$ axis : Two phase rotating reference frame where the axes are 90° apart.

$T_{\alpha\beta0}$: Clark's transformation matrix.

$T^{-1}_{\alpha\beta0}$: Inverse Clark's transformation matrix.

$T_{dq0}(\theta)$: Park's transformation matrix.

$T_{dq0}(\theta)^{-1}$: Inverse Park's transformation matrix.

θ : The angular displacement of the rotor.

$T_{abc-dq0}(\theta)$: Transformation matrix combining the Clark's and Park's transformation to transform from a-b-c to d-q-0 frame.

$T_{abc-dq0}(\theta)^{-1}$: Inverse transformation matrix combining inverse Clark's and inverse Park's transformation to transform from d-q-0 to a-b-c reference frame.

L_q : Inductance of q-axis.

L_d : Inductance of d-axis.

R : Resistance of the stator winding .

ω_r : Angular velocity of the rotor.

V_q : Voltage across the q-axis.

V_d : Voltage across the d-axis.

i_q : Current across the q-axis.

i_d : Current across the d-axis.

λ : Flux in the stator windings induced by the permanent magnets of the rotor.

T_e : Electromagnetic torque.

τ : Mechanical torque.

K_t : Torque constant of the motor.

i_{qRef} : Current reference set point for the q-axis current controller.

i_{dRef} : Current reference set point for the d-axis current controller.

$V_{a'Ref}, V_{b'Ref}, V_{c'Ref}$: Reference voltage for the phases a', b', c' of the stator respectively.

V_{dRef}, : Reference voltage for the d-axis.

V_{qRef} : Reference voltage for the q-axis.

ϕ : Phase difference between the input current and input voltage waveform.

I_2, I_3, I_4, I_n : $2^{nd}, 3^{rd}, 4^{th}$ and n^{th} harmonic component of the input current respectively.

I_1 : Fundamental component of the input current.

L_g : Grid Inductance.

C_{dc} : DC link capacitance.

m : Modulation index.

ω_i, ω' : Frequency of the input and output waveform of the PLL.

ϕ_i, ϕ' : Phase of the input and output waveform of the PLL.

K_{vco} : Gain of the voltage controlled oscillator.

V_{peak} : Peak of the DC link voltage.

K_p : Proportional gain of a P controller.

K_i : Integral gain of a I controller.

K_d : Derivative gain of a D controller.

D_p : Pole that is added to a D controller.

$u(t)$: Input to the system which is the output of the PID controller.

$e(t)$: Difference between measured value and the set point which is the error.

$y(t)$: Output of the plant.

$C(s)$: Laplace of the controller's transfer function.

D : Damping coefficient of the motor load.

J : Inertia constant of the motor load.

ω_c : Cut off frequency of the low pass filter.

T_s : Sampling time of the discrete low pass filter in sec.

K : Euler's integration constant.

Chapter 1

Introduction

1.1 About the company

Applied Micro Electronics "AME" BV is an independent developer and manufacturer of high quality electronic products. It is located in a top technological region of the world (Brainport Eindhoven). The goal of the company is to create innovative products that exceed customer expectations. AME accomplishes this by integrating product development and manufacturing and keeping a clear focus on the product and its function. Driven by technology, AME strives for the best solution combining the disciplines of Electrical, Mechanical, Software and Industrial Engineering. Through creativity, passion, ambition, motivation and a highly educated level of the employees AME secures its goal of being a profitable company. AME caters to diverse customers in the field of electric vehicles, home appliances and industrial automation. Some of the projects at AME are motor drives for circulation pumps, power converters for battery charging units and connectivity solutions (eg, wi-fi, Zigbee).

Power electronics is a fast growing area in which AME is active. Over the last several years, power demand is rising and currently AME has expertise in power conversion applications up to several tens of kilo Watts. Motor drives, especially variable speed drives for ventilation applications is a fast growing area in power electronics within AME.

1.2 Description of the project

Traditionally variable speed drives with DC link capacitors are designed such that a relatively stable DC link voltage is obtained. The slim DC link is based on a small DC link capacitance, e.g. a film capacitor, allowing significant voltage ripple on the DC link. The variation of the DC link voltage results in wider current spikes that are drawn from the AC grid due to continuous conduction of the capacitor. The distortion of the AC current waveform with respect to the AC voltage becomes less, thereby improving the power factor of the system. As a result, the reactive power drawn from the grid becomes less, which in turn results in lower losses in the AC power distribution grid.

1.2.1 Problem statement

There are, however, a few catches with slim DC-link systems. When the grid is weak the DC link voltage has the tendency to oscillate with the parasitic grid inductance thereby creating LC resonance. As a result, unwanted higher order harmonics are introduced in the DC link voltage. This voltage variation greatly affects the current drawn from the grid. The problem statement is explained in detail in chapter 3.

1.2.2 Research question

"How can the unwanted oscillations in the grid current, drawn by the motor drive employing slim DC link, be damped or suppressed such that the motor drive complies with the IEC 61000-3-2 harmonic standard?"

To address this problem, any part of the motor drive like control algorithm for inverter, the switching of the rectifier or the electronics can be modified. However, this assignment aims to improve the performance, by modifying the control systems without any change in the hardware. Therefore, a feed-forward control algorithm for the inverter has been proposed. The idea is to reconstruct the ideal DC link voltage without the LC ripples and use it to control the switching of the inverter. The estimated DC link voltage is then fed to the Pulse Width Modulator of the inverter so that it can suppress for the ripple. The design of the complete control of the motor comprises of:

- A motor model with the rippled DC-link voltage containing LC harmonics.
- An algorithm to reconstruct the DC-link voltage without ripples.

1.3 Scope of the graduation assignment

The master thesis focuses on the development of a control algorithm to answer the research question. This implies that research is done to design an innovative feed-forward algorithm to damp the unwanted ripples. The implementation of the closed loop speed control of the Permanent Magnet Synchronous Motor (PMSM) using Field Oriented Control (FOC) is also included in the scope of this assignment. The embedded software for the control is also developed.

This is an assignment for graduation in embedded systems but an additional study on the working of PMSM, field oriented control and the use of slim DC link was performed. It is necessary to understand the motor drive system in order to design of a suitable control system. A summary of this study has been documented in this report in chapter 2 and 3 of this report. However, an in-depth perception of these topics is not in the scope of this master thesis. Any changes in the electronics is also not in the scope of this assignment.

1.4 Methodology

Literature study:

The commencement of the problem analysis is marked by literature study. This phase is necessary for a thorough understanding of the motor drive working and the causes for the ripple in slim DC link and its effects. An in-depth knowledge of the system is necessary for the formulation of a control strategy to address the issue. A deep and sound literature study will set a solid foundation for the future work and will avoid any incoherence that might arise. Upon completion of the literature study a suitable control algorithm for the project is formulated.

Modeling and simulation:

The second phase is to design and implement the control algorithm formulated in the previous phase. The control is categorized as feedback and feed-forward control loops. A classical feedback control is implemented for the speed control and the proposed control in this thesis is the feed-forward control. The motor drive along with its control loop its simulated using MATLAB simulink. The controller parameters are then tuned based on the results of the simulation.

Embedded software Development:

Once satisfactory results are obtained from the simulation, the control algorithm is developed in embedded software. The embedded software implementation will be an extension of the AME Motor Drive Framework (AMDF). The AMDF is a framework that allows MATLAB model-based development of embedded software. The simulation model that contains motor control blocks will have their software counter-parts implemented in C.

1.5 Structure of the report

- The first part of the literature study involving the study of the feedback control of a PMSM using Field Oriented Control (FOC) is described in detail in chapter 2.
- The need for slim DC link along with its pros and cons are discussed in chapter 3.
- The formulation of a suitable feed-forward control algorithm and it's choice has been defended in chapter 4.
- The design of the feedback and feed-forward control loop and selection of the various block parameters is defended in chapter 5.
- Simulation results of the formulated algorithm using MATLAB are shown in chapter 6.
- The embedded software development and working of AMDF are explained in chapter 7.
- Chapter 8 gives the conclusion and the scope for future work.

1.6 System Specification

This project focuses on the development of control algorithm and its embedded software for a fixed and existing electronics and motors setup. The simulation and mathematical modeling is done for the same.

- The motor used is a surface mounted permanent magnet synchronous motor with a power rating of 2000W.
- The electronics includes a 3 phase bridge diode rectifier connected to a 3 phase inverter via a slim DC link.
- The micro-controller used for the control of motor drive system shall be STM32F303RC(T6TR). This controller supports Floating point operations.

Chapter 2

Speed control of permanent magnet synchronous motor

The working of a Permanent Magnet Synchronous Motor (PMSM) and its control is explained in this chapter. The chapter begins by explaining the properties, construction and the working principle of a PMSM. The concepts of variable speed drives and Clark's and Park's transform are introduced for a better understanding of the forthcoming topics. Then the chapter proceeds to describe the technique of speed control called field oriented control or vector control. Finally the use of space vector modulation to control the duty cycle of the inverter is explained.

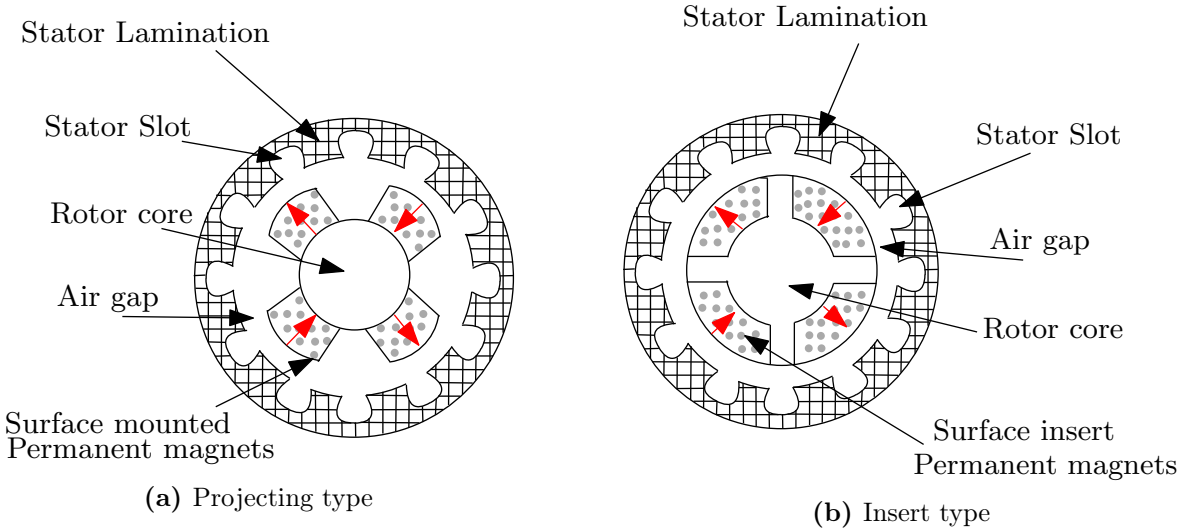
2.1 An introduction to PMSM

A synchronous motor is an AC motor where the speed of rotation of the rotor needs to be synchronous to the frequency of the AC supply. The three phase AC supply windings are wound in the stator slots. The rotor is energized either by a DC supply or by permanent magnets mounted on the rotor. When magnets are used to create a constant magnetic field in the rotor, it is called a permanent magnet synchronous motor. Permanent magnet synchronous motors are used in applications that require high efficiency, reliability and low power density. Therefore, they are becoming popular in low cost and low power applications like fans, compressors, pumps and household appliances such as washing machines. The high reliability of the PMSM can be attributed to the use of permanent magnets to generate the rotor flux.

The permanent magnets can be on the surface of the rotor or embedded in the interior of the rotor. Therefore, based on the position of the magnets they are classified as,

- Surface mounted PMSM
- Interior PMSM

Surface mounted PMSM, shown in Figure 2.1, is the simplest and the most economical means of constructing a PMSM. The magnet is mounted on the surface of the rotor by means of epoxy glue making it less robust than interior PMSM. There are two types of surface mounted PMSM namely projecting type and the insert type. In the projecting type the magnets project from the surface of the rotor as shown in Figure 2.1a. This type has an uniform air-gap as the relative permeability of air and permanent magnet are almost equal. The insert type is also a surface mounted PMSM but the magnet does not project out of the rotor core as shown in Figure 2.1b. If the permanent magnet is embedded inside the rotor core as shown in Figure 2.2 then it is known as interior PMSM [1]. The red arrows in the figure denote the direction of the magnetic field.



(a) Projecting type

(b) Insert type

Figure 2.1: Surface mounted PMSM

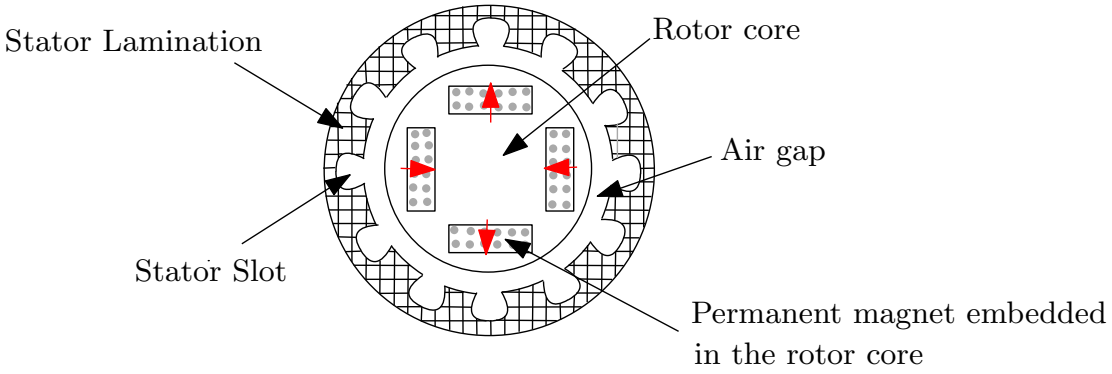


Figure 2.2: Interior PMSM

Principle of Operation:

The working of the synchronous motor is based on the principle that the current through a conductor produces a magnetic field. Coiling the conductor will result in increased magnetic field for the same amplitude of current. Accordingly, when the stator windings are energized by the 3 phase AC supply, a rotating magnetic field is created in the air gap between the rotor and stator. As the magnetic field due to the permanent magnets present in the rotor tries to align with the magnetic field produced by the stator current, a torque is generated. As a result of the torque, the rotor starts to rotate. Once the north pole of the rotor's magnetic field is aligned with the south pole of the stator's magnetic field the motor is said to be in lock condition. In this state the rotor starts to rotate at the speed of the rotating magnetic field due to the alternating stator current. This speed is also known as the synchronous speed. The synchronous speed N_s in RPM (Revolutions Per Minute) is given by,

$$N_s = \frac{60f}{P} \tag{2.1}$$

where, f is the frequency of the AC supply in Hz and P is number of stator pole pairs. Therefore, it can be concluded that the speed of the motor is proportional to the frequency of the stator supply, f [2].

2.2 Variable Speed Drives

The use of electric motors has spread to almost all branches of engineering from fans to space applications. Being able to control the speed of the motor is one of its most attractive features. From equation (2.1), it can be concluded that the speed of the PMSM can be controlled by varying the frequency of the stator current. For this purpose it is necessary to control the frequency of motor supply. However, in practice it is not possible to obtain a variable frequency supply from the grid.

Advancements in the field of power converts helped solve this constraint. Channeling the grid power to the electric motor via a series of conversion stages, as shown in Figure 2.3, enables control of the motor's supply frequency. The grid supply having a fixed frequency is passed through a 3 phase diode rectifier that converts the AC supply to DC, which is then fed to the inverter. The output of the inverter is a 3 phase AC supply having the desired frequency. The frequency of the obtained AC supply can be controlled by varying the duty cycle of the inverter. Scalar and vector control are the two methods of controlling the inverter switching but the most suitable technique for PMSM is vector control also known as Field Oriented Control (FOC). This is because vector control improves the overall performance of the system by providing higher efficiency, torque control for the full speed range and decoupled control of torque and flux. Therefore, FOC is the chosen method of speed control for this assignment.

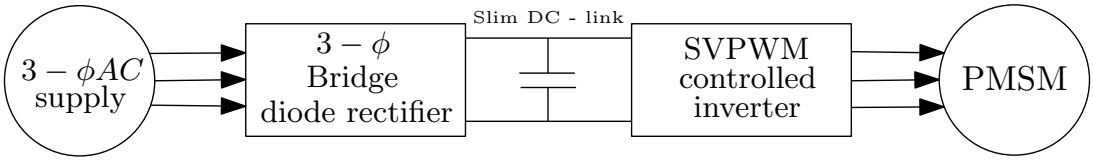


Figure 2.3: Block diagram of a Variable speed drive

2.3 Park's and Clark's transform

The behavior and performance of the PMSM can be analyzed by the equations for the current drawn by the motor and voltage applied to the stator winding. In general, these parameters are represented in the three phase stationary reference frame commonly known as the $a-b-c$ axis which are 120° apart. When represented in this frame of reference, the equations are complex to solve as the current, induced voltage and flux linkage are time dependant variables when the rotor is in motion. In order to simplify the machine model, various mathematical transformations have been proposed to decouple the time dependent variables by selecting an appropriate reference frame. The most prominently used are the Clark's and Park's transform. These transformations are extremely helpful as they not only simplify the analysis of the machines but also aid in the digital control of the motors [3].

E. Clarke proposed a transformation by which the circuit could be represented in a stationary, two phase reference frame know as α-β-0 axis. It is considered a two phase reference frame because the zero axis contains only DC and all the third harmonic content. These frames are orthogonal to each other as shown in Figure 2.4 . The transformation is mathematically given by the equation (2.2) [4].

$$\left[f_{\alpha\beta 0}\right] = T_{\alpha\beta 0}\left[f_{abc}\right] \tag{2.2}$$

where, $f_{\alpha\beta 0}$ is the representation in $\alpha-\beta-0$ reference frame, f_{abc} is the representation in $a-b-c$ reference frame, and $T_{\alpha\beta 0}$ is the Clark's transformation matrix and is given by,

$$T_{\alpha\beta 0} = 2/3 \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/2 & 1/2 & 1/2 \end{bmatrix}$$

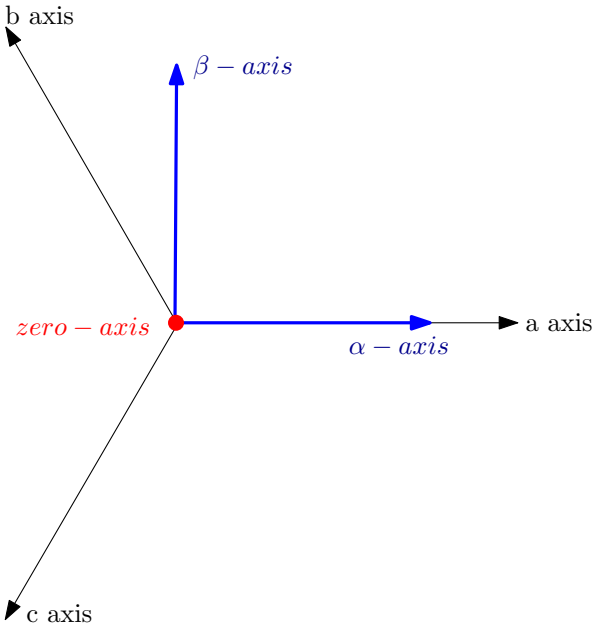


Figure 2.4: Representation of reference frame of Clark's transform

The inverse Clark's transform to convert from $\alpha - \beta - 0$ back to $a - b - c$ reference frame is given by equation (2.3).

$$\left[f_{abc}\right] = T_{\alpha\beta0}^{-1}\left[f_{\alpha\beta0}\right] \tag{2.3}$$

where $T_{\alpha\beta0}^{-1}$ is the inverse Clark's transformation matrix and is given by,

$$T_{\alpha\beta0}^{-1} = \begin{bmatrix} 1 & 0 & 1 \\ -1/2 & \sqrt{3}/2 & 1 \\ -1/2 & -\sqrt{3}/2 & 1 \end{bmatrix}$$

Park's transformation is a transformation from two phase stationary frame to two phase rotating frame. The rotating frames obtained are known as (d) direct axis and (q) quadrature axis and are $90°$ apart. R.H. Park proposed a transformation according to which the variables are expressed in terms of a reference frame that is fixed to the rotor which means that the frame is rotating with the motor. Therefore, the variables can be observed as constant values with respect to the rotor thereby eliminating all the time dependent variables from the equation, even when the rotor is spinning. Hence in this refernce frame the variables are not alternating values. The graphical representation of the d-q reference frame is shown in Figure 2.5. The Park's transformation is given by equation (2.4).

$$\left[f_{dq0}\right] = T_{dq0}(\theta)\left[f_{\alpha\beta0}\right] \tag{2.4}$$

where $T_{dq0}(\theta)$ is the Park's transformation matrix and is given by,

$$T_{dq0}(\theta) = \begin{bmatrix} cos(\theta) & sin(\theta) & 0 \\ -sin(\theta) & cos(\theta) & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

θ is the angular displacement of the rotor and hence the angular displacement of the rotating reference frame.

Inverse Park transform is used to transform from $\alpha - \beta - 0$ to $d - q - 0$ reference frame and is given by equation (2.5).

$$\left[f_{\alpha\beta0}\right] = T_{dq0}(\theta)^{-1}\left[f_{dq0}\right] \tag{2.5}$$

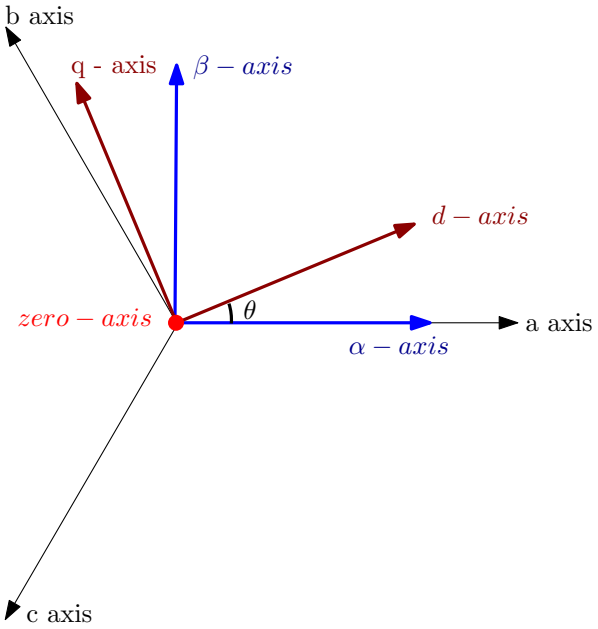


Figure 2.5: Vector representation of reference frames of Clark's and Park's transform

where $T_{dq0}(\theta)^{-1}$ is the inverse transformation matrix and is given by,

$$T_{dq0}(\theta)^{-1} = \begin{bmatrix} cos(\theta) & -sin(\theta) & 0 \\ sin(\theta) & cos(\theta) & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

The transformation from $a-b-c$ to $d-q-0$ frame can be perceived as Park's transform on top of Clark's transform. Though these transformation can be applied for any waveform it is especially suitable for the three phase current and voltage generally depicted in the $a-b-c$ reference frame. The transformation from $a-b-c$ frame to $d-q-0$ frame is given by equation (2.6).

$$\left[f_{dq0}\right] = T_{abc-dq0}(\theta)\left[f_{abc}\right] \tag{2.6}$$

where $T_{abc-dq0}(\theta)$ is the transformation matrix combining the Clark's and Park's transformation to transform from $a-b-c$ to $d-q-0$ frame and is given by,

$$T_{abc-dq0}(\theta) = 2/3 \begin{bmatrix} cos(\theta) & cos(\theta - 2\pi/3) & cos(\theta + 2\pi/3) \\ sin(\theta) & sin(\theta - 2\pi/3) & sin(\theta + 2\pi/3) \\ 1/2 & 1/2 & 1/2 \end{bmatrix}$$

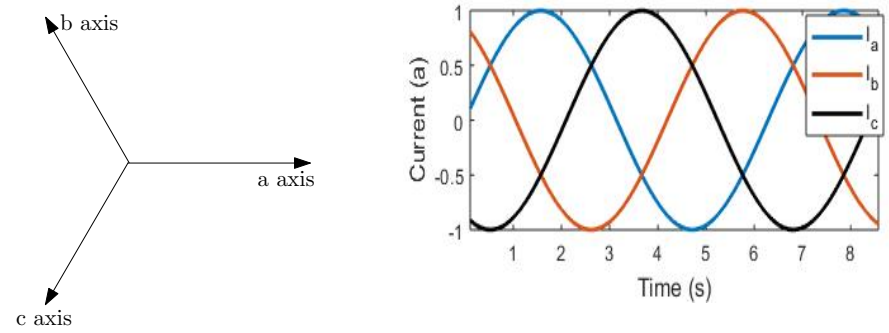
Inverse transform is used to convert the $d-q-0$ to $a-b-c$ frame and is given by the equation (2.7).

$$\left[f_{abc}\right] = T_{abc-dq0}(\theta)^{-1}\left[f_{dq0}\right] \tag{2.7}$$

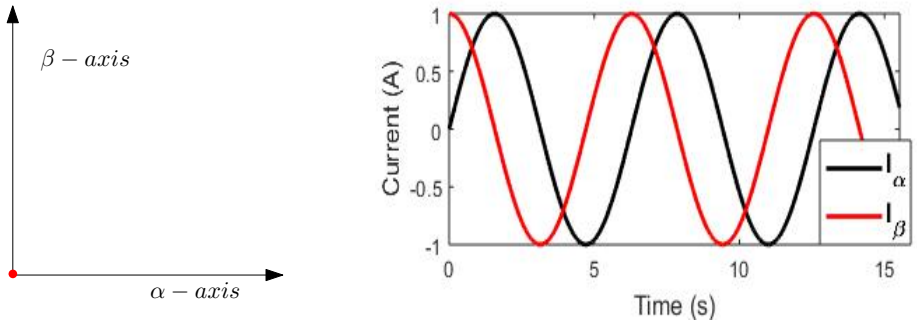
where $T_{abc-dq0}(\theta)^{-1}$ is the inverse transformation matrix and is given by,

$$T_{abc-dq0}(\theta)^{-1} = \begin{bmatrix} cos(\theta) & sin(\theta) & 1 \\ cos(\theta - 2\pi/3) & sin(\theta - 2\pi/3) & 1 \\ cos(\theta + 2\pi/3) & sin(\theta + 2\pi/3) & 1 \end{bmatrix}$$

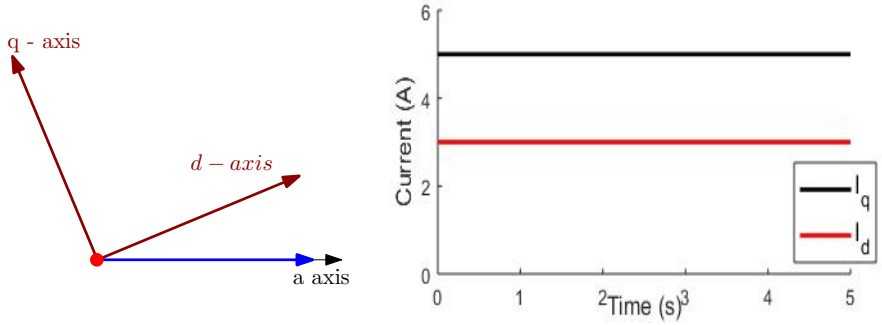
The Figure 2.6 shows the 3 reference frames and how the current varies with respect to time when represented in each of the frames [5].



(a) a-b-c reference frame



(b) $\alpha - \beta - 0$ reference frame



(c) d-q-0 reference frame

Figure 2.6: Reference frames and their corresponding graphical representation in the steady state condition

2.4 Mathematical modeling of the PMSM in d-q reference frame

The motor can be represented in the $d - q - 0$ frame, ie. rotor reference frame, by the equations (2.8) - (2.10) [6].

$$\frac{di_d}{dt} = \frac{1}{L_d}V_d - \frac{R}{L_d}i_d + \frac{L_q}{L_d}P\omega_r i_q \tag{2.8}$$

$$\frac{di_q}{dt} = \frac{1}{L_q}V_q - \frac{R}{L_q}i_q - \frac{L_d}{L_q}P\omega_r i_d - \frac{\lambda P\omega_r}{L_q} \tag{2.9}$$

$$T_e = \frac{3}{2}P[\lambda i_q + (L_d - L_q)i_d i_q] \tag{2.10}$$

Where,
L_q and L_d are the inductance of q axis and d axis.
R is the stator winding resistance.
V_q and V_d are the voltages across the q axis and d axis.
i_q and i_d are the currents in the q axis and d axis.
ω_r is the angular velocity of the rotor.

P is number of pole pairs.
λ is the flux in the stator windings induced by the permanent magnets of the rotor.
T_e is electromagnetic torque.

$\frac{di_q}{dt}$ and $\frac{di_q}{dt}$ will be equal to zero during the steady state of the motor, as i_q and i_q are a constant value in this state. For a surface mounted - permanent magnet synchronous motor $L_d = L_q$ and so the equation (2.10) becomes,

$$T_e = 1.5P\lambda i_q \tag{2.11}$$

From equation (2.11) it can be seen that the torque is dependent only on i_q component of the current thereby simplifying the speed control [7].

2.5 Field Oriented Control

In order to control the speed of the PMSM, field oriented control is implemented as shown in Figure 2.7. Field oriented control is realized by measuring the 3 phase stator current and transforming it from the $a - b - c$ reference frame to the d-q-0 reference frame by Clark's and Park's transformation using the measured value of rotor position. This is because, upon transformation, the d component points directly to the flux and the q component is the torque reference thereby simplifying the control of the motor. The d-q-0 current components are controlled individually using two independent current controllers. As discussed above, for a Surface mounted permanent magnet synchronous motor the torque is not dependent on the i_d component and so the i_{dRef} set point can be set to any arbitrary value. To avoid unnecessary power dissipation it is set to 0. The set point for the i_q current, i_{qRef}, can be obtained from a speed controller. The speed controller generates an equivalent torque set point by comparing the measured speed and the reference speed. The current drawn by the stator is proportional to the mechanical torque as shown in equation (2.12).

$$\tau \propto i_{qRef} \tag{2.12}$$

$$\therefore \tau = K_t \cdot i_{qRef} \tag{2.13}$$

where K_t is the proportionality constant and is know as the motor torque constant. Therefore Dividing the torque reference with the motor constant will give the current set point, i_{qRef}, according to equation (2.13) which is given as input to the 'q' current controller. Based on the error between the current set point and the measured current values in the d-q reference frame, the i_q and i_d current controllers generate the voltage set points v_{qRef} and v_{dRef} respectively. Upon applying the inverse Clark's and inverse Park's transform on these two voltage components, the 3 phase voltage references V_{aRef}, V_{bRef}, V_{cRef}, that are the input for the state vector modulation, can be obtained. The reference voltage vector $\vec{V_{ref}}$ is calculated by projecting each of the voltage vectors on a rotating vector and this is used to determine the switching pattern of the inverter and this will be discussed in Section 2.6 [8]. An accurate measurement of the stator current and the rotor position is necessary for the proper transformation and therefore, precise control of the motor.

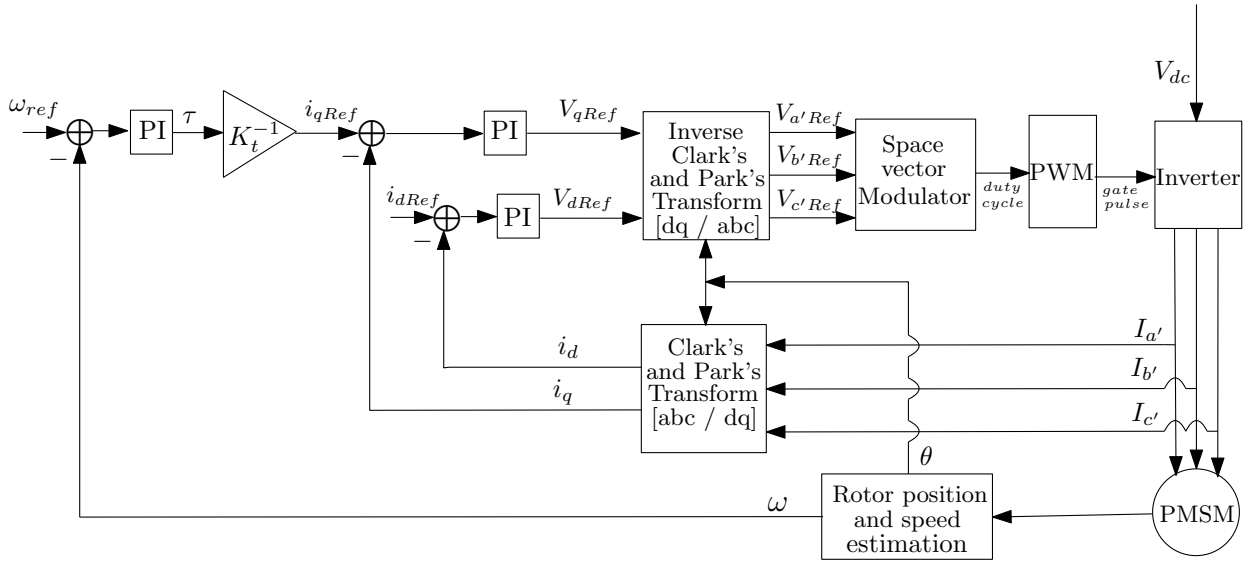


Figure 2.7: Schematics of field Oriented control

2.6 Space Vector Modulation for PMSM

Space Vector Modulation is a method for providing the desired stator voltage for the variable speed AC motor. The SVM scheme determines the duty cycles of the inverter switches. In order to understand the working of the SVM it is necessary to know the constraints for inverter switching. As seen in the Figure 2.8, there are six switches in the inverter. An important constraint is that both the switches of one leg should not be in the ON state. This is because if the switches in the same leg are ON, the inverter leg creates a short circuit. Due to this constraint, the state of the lower leg switches will be the complement of the upper switch. Another observation is that, if all the switches in the upper part are ON or OFF at the same time, the current will not have a closed path. Therefore, if all the switches in the upper leg or lower leg are in the ON state the voltage across the phase windings will be zero. [9]. As there are three switches in the upper legs it can be deduced that there are eight possible switching combinations (2^3 as each switch can be either ON or OFF) and each of the switching combinations can be represented by a vector as shown below (0 is OFF and 1 is ON).

$$v_1 = \begin{bmatrix}1 & 0 & 0\end{bmatrix} \quad v_2 = \begin{bmatrix}1 & 1 & 0\end{bmatrix} \quad v_3 = \begin{bmatrix}0 & 1 & 0\end{bmatrix} \quad v_4 = \begin{bmatrix}0 & 1 & 1\end{bmatrix}$$
$$v_5 = \begin{bmatrix}0 & 0 & 1\end{bmatrix} \quad v_6 = \begin{bmatrix}1 & 0 & 1\end{bmatrix} \quad v_7 = \begin{bmatrix}1 & 1 & 1\end{bmatrix} \quad v_8 = \begin{bmatrix}0 & 0 & 0\end{bmatrix}$$

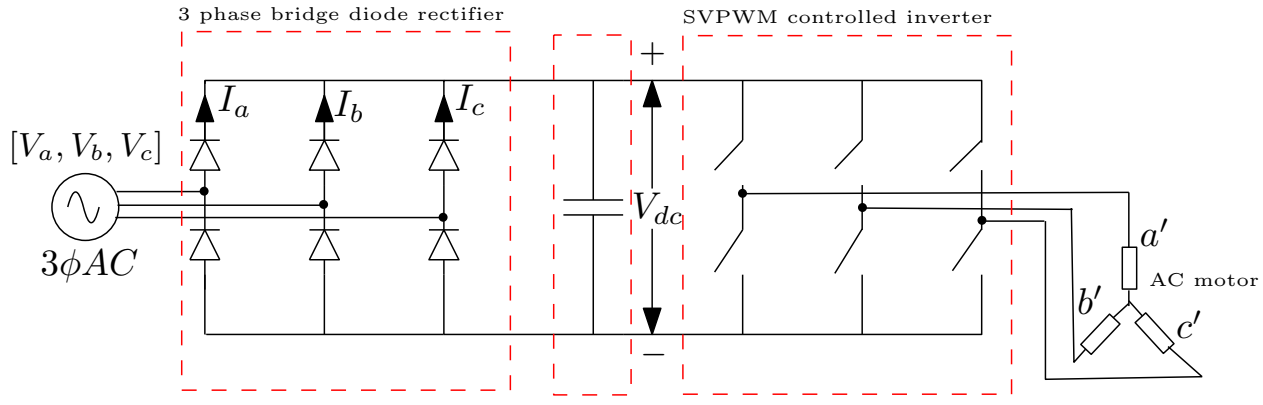


Figure 2.8: Topology of a VSD

The vectors from $v_1 - v_8$ can create six sectors as shown in Figure 2.9 (v_7 and v_8 are in the center). It can be seen that the adjacent vectors of a sector differ only by one bit. Therefore, when the reference voltage vector $\vec{V_{ref}}$ moves from one sector to another, only one of the transistors in the upper leg will switch. This reduces the losses due to switching. Based on the sector in which the reference voltage lies the two adjacent vectors and the zero vectors (v_7 and v_8) are realized for a weighted amount of time.

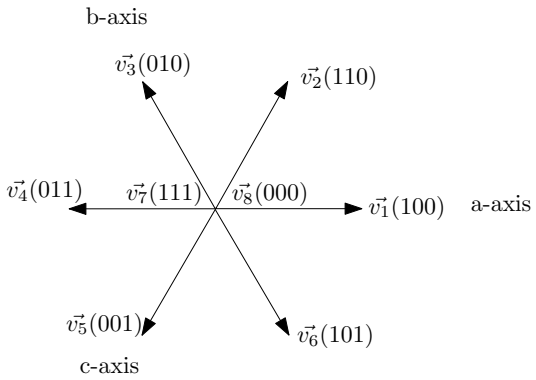


Figure 2.9: Sector formation in SVM

This can be better understood from the illustration in Figure 2.10. The reference voltage $\vec{V_{ref}}$ is represented as a sum of $\vec{v_1}$ and $\vec{v_2}$ as it lies in sector 1. The switching duration is determined by the magnitude of $\vec{v_1}$ and $\vec{v_2}$. In this case vector $\vec{v_1}$ is applied for time t_1 and $\vec{v_2}$ for time t_2 according to the vector diagram. The switching order is given by $v_8 -> v_1 -> v_2 -> v_7$.

$$T_{sw} = t_8 + t_1 + t_2 + t_7 \tag{2.14}$$

Where T_{sw} is the switching period of the inverter which is the inverse of the PWM frequency (Appexdix B.2). t_7, t_8 are the time for which vector v_7 = [1 1 1] and v_8 =[0 0 0] are realised. As all the times add to the switching time, we can calculate t_7 and t_8 as,

$$t_7 = t_8 = \frac{T_{sw} - t_1 - t_2}{2} \tag{2.15}$$

The reference vector V_{ref} keeps rotating over the six sectors and for each position the switching pattern and its corresponding switching duration is calculated.

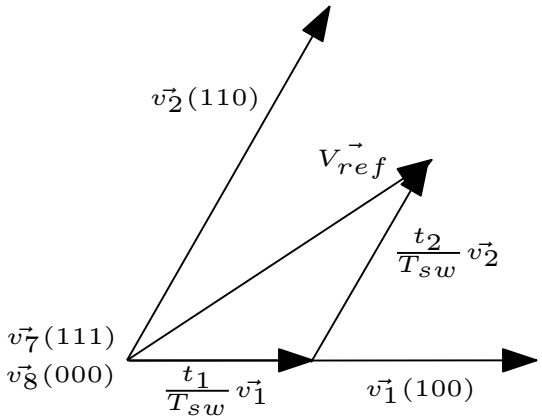


Figure 2.10: Example of SVM

2.6.1 Role of DC link voltage

For calculating the switching duration, it is essential to consider the DC link voltage V_{dc} which is the input to the inverter as seen in Figure 2.8. When one of the vectors from v_1 to v_6 is the state of the inverter switches, the output of the inverter will be equal to V_{dc}. For example, if the vector v_3 = [1 0 0] is the switching pattern of the inverter, that is the top switch in the first leg and the bottom switch of leg two and three are ON, then the 3 phase output voltage can be given as,

$$V_{a'b'} = V_{dc}; \qquad V_{b'c'} = 0; \qquad V_{c'a'} = -V_{dc}$$

where a', b', c' are the stator phases as shown in Figure 2.8. Hence DC link voltage plays an important role in the computation of duty cycle and hence in the determination of the output voltage of the inverter.

2.6.2 Modulation index calculation using measured DC link voltage

From Section 2.6.1 it is clear that the duty cycle of the inverter and hence it's output voltage depends on the DC link voltage. The space vector modulation assumes that when the switching state is one of the vectors, v_1 to v_6, the output voltage across the active phases of the motor will be equal to V_{dc}. It is essential to consider that when using slim DC link, the DC voltage has ripples and is varying with time. Therefore, by considering this phenomena when calculating the duty cycle, the output of the inverter will be closer to the voltage set point $V_{a'Ref}, V_{b'Ref}, V_{c'Ref}$ [10]. For this purpose modulation index m is defined as,

$$m = \frac{V_{ref}}{V_{dc(t)}/2} \tag{2.16}$$

where $V_{dc}(t)$ is the measured value of DC link voltage at time t and the reference voltage vector $\vec{V_{ref}}$ is calculated by projecting each of the reference voltage vectors $V_{a'Ref}$, $V_{b'Ref}$, $V_{c'Ref}$ on a rotating vector. The duty cycle is then determined from the modulation index. This is a feed-forward method where $V_{dc}(t)$ is used to calculate the duty cycle of the inverter.

Chapter 3

Slim DC-link

The terms power factor and Total Harmonic Distortion (THD) are defined in this chapter and it explains the importance of a good power factor. Then the chapter proceeds to explain the importance of having a capacitor in the DC link and the problems faced when using a traditional electrolytic capacitor. An alternative for the electrolytic capacitor is then put forward and the advantages and disadvantages of the proposed capacitor are discussed.

3.1 Total Harmonic Distortion and Power Factor

Power factor of a system is defined as the real power drawn by the load to the reactive power in the system. Power factor has two components, the displacement power factor and distortion power factor. In the ideal case, the displacement power factor is said to be unity when the current drawn by the load is in phase with the voltage [11]. From this statement, it can be deduced that the displacement power factor is not unity when the voltage and current waveforms are out of phase as show in Figure 3.1. Displacement power factor can be calculated using equation (3.1)

$$\text{Displacement power factor} = cos(\phi) \tag{3.1}$$

where ϕ is the phase difference between the input current and the voltage.

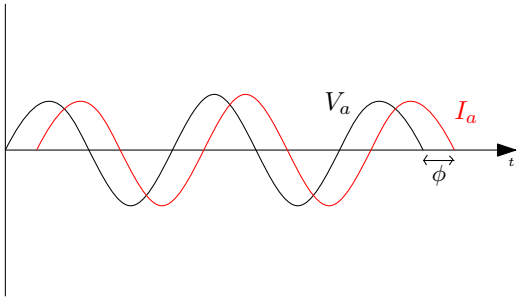


Figure 3.1: Phase difference between current and voltage waveform

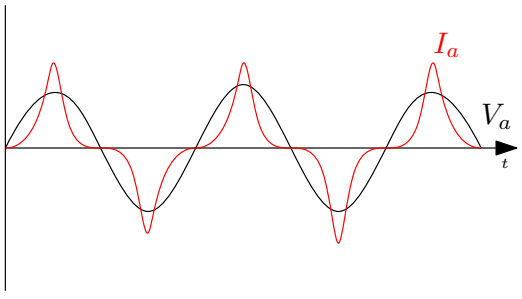


Figure 3.2: Distorted current waveform

The distortion of an ideal waveform by waveforms of varying frequencies is known as harmonics. The distortion power factor is not unity when the current is severely distorted due to harmonics as shown in Figure 3.2. Here the distortion power factor is calculated using equation (3.2),

$$\text{Distortion power factor} = \frac{1}{\sqrt{1 + THD^2}} \tag{3.2}$$

where THD is the Total Harmonic Distortion and is determined by,

$$THD = \frac{\sqrt{I_2^2 + I_3^2 + I_4^2 + ... + I_n^2}}{I_1}$$

I_2, I_3, I_4, I_n are the 2^{nd}, 3^{rd}, 4^{th} and n^{th} harmonic component of the signal respectively and I_1 is the fundamental component. Hence the THD is the square root of sum of squares of all harmonic component divided by the fundamental component of the signal. When the distortion power factor is not unity, it means that there is harmonic distortion in the current drawn from the grid. This affects the other devices powered from the same source. In order to avoid unwanted harmonics in the current waveform and prevent grid distortion the harmonic standards IEC 61000-3-2 was formulated (Appendix A.1), which limits the magnitude of each of the harmonic component. Therefore, it is mandatory for the motor drives to comply with this standard.

3.2 Significance of DC-link Capacitor

The line between the rectifier and the inverter is known as the DC link (as shown in Figure 2.3). There is a capacitor in the DC link to provide adequate energy when the rectified voltage drops thereby smoothing the rectified voltage and almost making it an almost constant value as shown by V_{dc} in Figure 3.3 (black curve).

The DC link capacitor serves to minimize the voltage ripple in the DC link by balancing the instantaneous power between the supply and load [12]. As the capacitor is connected in parallel to the supply, it maintains a stable voltage across the input of the inverter thereby safeguarding the inverter from EMI and surges. It also absorbs the current ripple due to switching and decouples the input grid supply and the output of the inverter which have different frequencies.

On the contrary, it is important to observe that when using a DC link capacitor the current drawn from the grid becomes spiky as shown by the I_a waveform in Figure 3.3 (red curve). This is because the capacitor get charged and hence conducts current only when the input voltage to the capacitor (V_a in this case) is greater than the voltage across the capacitor V_{dc}. This discontinuous conduction of the capacitor results in distorted current drawn form the grid and thereby decreased distortion power factor. Therefore, it is essential to find an alternative solution to the conventional DC link capacitor.

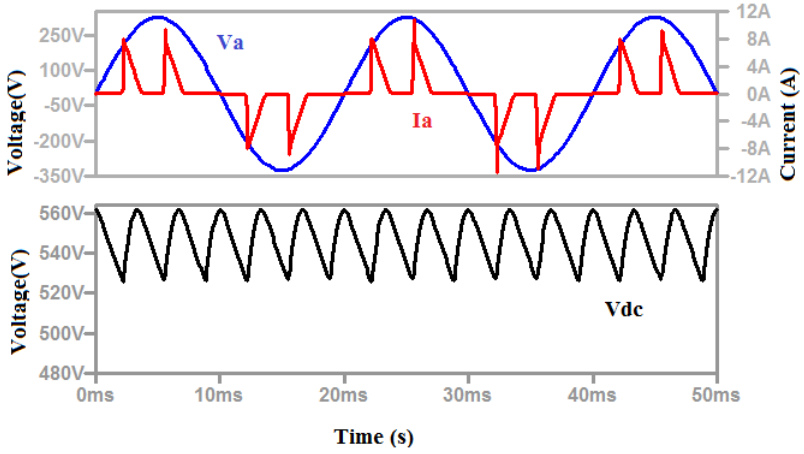


Figure 3.3: Input voltage (blue), Input current (red), DC link voltage(black) using a traditional DC link capacitor

3.3 Small DC link capacitor

Traditionally the capacitor used in the DC link is an electrolytic capacitor. These electrolytic capacitors have a high value of capacitance of the order of hundreds of μF to several mFs and therefore, have a high density, energy storage capability and a low cost. But as it ages the equivalent series resistance increases and the capacitance reduces. Also the electrolyte in the capacitors is susceptible to heat due to ripple in the current which reduces the life span of the capacitor. The electrolytic capacitor has a shorter life span than any other power electronics component in the drive thereby reducing the overall life of the drive system [13].

Another motivation for finding a suitable alternative to the traditional capacitor is the need for DC link capacitor with reduced capacitance. Figure 3.4 shows a comparison of the ripple content in the output of the single phase and 3 phase rectifier. In general, the DC link voltage ripple is lesser in three phase rectified output as opposed to single phase rectified output. This is because the other phases start conducting before the voltage goes down to zero in a three phase rectifier. As the DC link voltage has an inherently smoother waveform with reduced ripple it is sufficient to use a capacitor with lower capacitance value for a three phase supply.

Owing to the need for a capacitor with small capacitance value and increased life span, film capacitors became popular. Film capacitors are capacitors that use a thin film made of polycarbonate, polypropylene or polyester as the dielectric. These film capacitors not only have a longer life span but are also cost efficient if designed appropriately. They also have lower value of capacitance, low self-inductance and low equivalent series resistance [14, 15, 16]. A DC link containing a capacitor of the order of 5-10μF is known as slim DC link and in this cases uses a film capacitor.

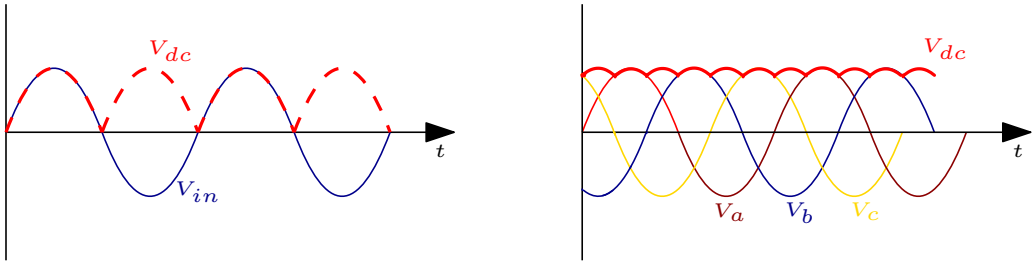


Figure 3.4: Ripple in the rectified voltage of single phase and 3 phase supply

3.4 Effects of slim DC link

The use of slim DC link has certain pros and cons. This section focuses on the advantages and disadvantages of using a slim DC link capacitor, to get a better understanding of the effects of using a small capacitor. This knowledge will assist in improving the system.

3.4.1 Enhancement in the system performance due to Slim DC link

Besides having a longer life span the slim DC link has another important advantage. The slim DC link with a small capacitance has a reduced smoothing effect on the DC link voltage than the traditional capacitor. Therefore, a voltage ripple on the DC link can be observed while using a slim capacitor. This is because the conduction time of the rectifier diode increases due to the small capacitance value. Continuous conduction results in the input current approaching a sinusoidal curve as shown in Figure 3.5 (red curve) as opposed to the distorted current waveform obtained when a large capacitance is used as seen in Figure 3.3 (red curve) [17]. As a result the total harmonic distortion of the input current decreases and hence the power factor increases as per equation (3.2).

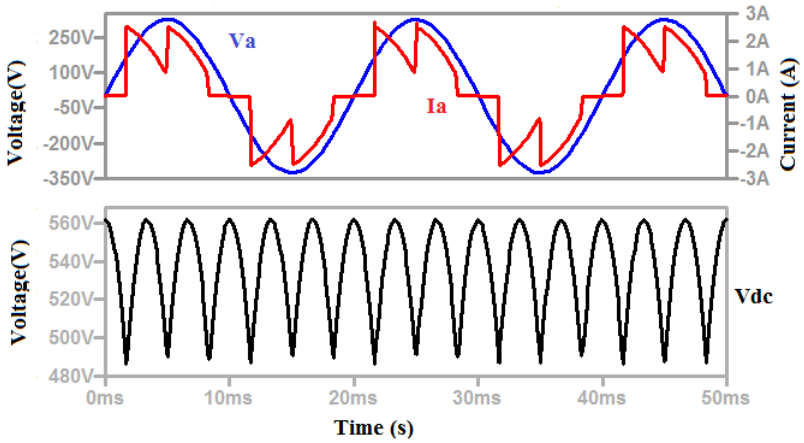


Figure 3.5: Input voltage (blue), Input current (red), DC link voltage (black) using a slim DC link

3.4.2 Harmonic issues with a Slim DC link

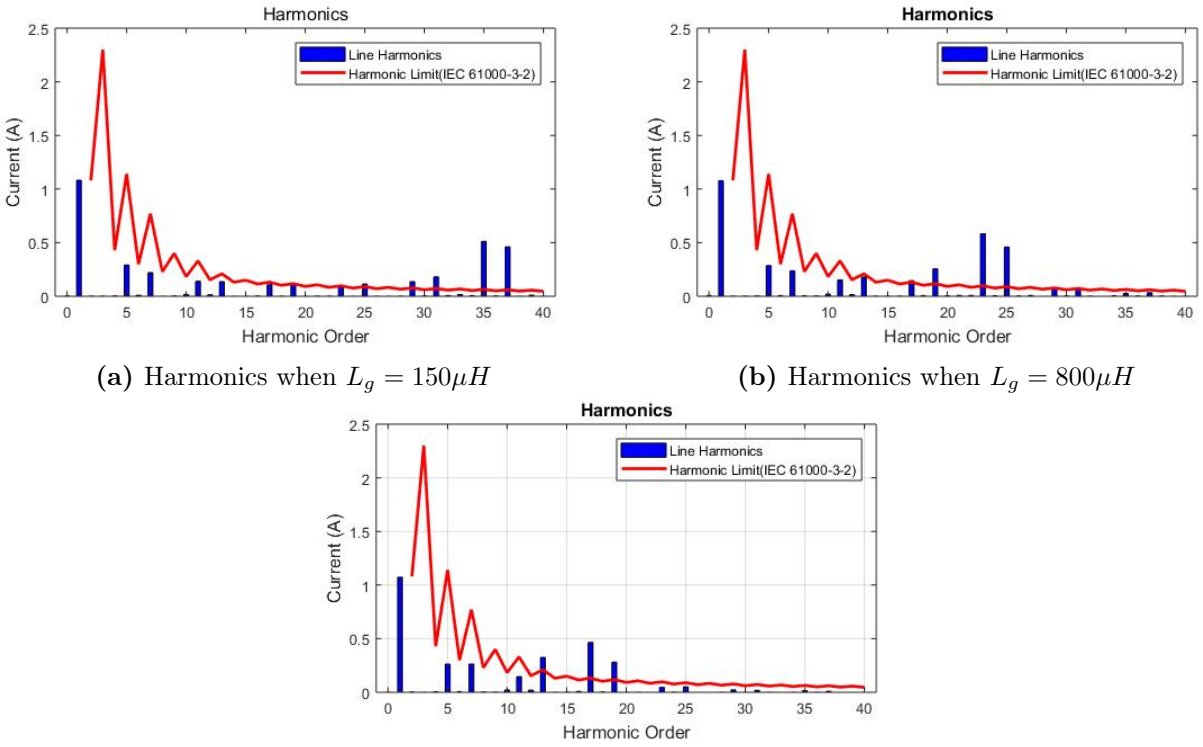
There are a few catches with slim DC-link systems. When the grid is weak the DC link voltage has the tendency to oscillate at high frequency with the parasitic grid inductance [18]. According to [19], a grid is said to be weak when the grid inductance is greater than 70 μH. From the formula (3.3) it can be seen that, as the capacitance decreases the resonance frequency increases.

$$\text{Resonance frequency} = \frac{1}{2\pi\sqrt{L_g C_{dc}}} \tag{3.3}$$

Where L_g is the grid inductance in Henry and C_{dc} is the DC link capacitance in Farad. A PMSM with a slim DC link is simualted in MATLAB and the harmonics of the current drawn by the grid is analysed and tabulated for various grid inductance. Table 3.1 shows the THD of the grid current for various values of grid inductance values. It can be seen that as the grid gets weaker, that is as the grid inductance increases, the current exceeds the harmonic limit given in Appendix A.1. The graphical results of the simulation is shown in Figure 3.6.

Table 3.1: THD for different grid inductance values (Output Power = 1.45KW, $C_{dc} = 8\mu F$)

L_g (μH)	THD [%]	Current harmonics that exceed IEC limits
40	35.8	-
60	36.1	-
80	36.8	$31^{th}, 37^{th}$
100	37	$25^{th}, 29^{th}, 31^{th}, 35^{th}, 37^{th}$



(a) Harmonics when $L_g = 150\mu H$

(b) Harmonics when $L_g = 800\mu H$

(c) Harmonics when $L_g = 1500\mu H$

Figure 3.6: Harmonic content for various grid inductance ($OutputPower = 1.45KW, C_{dc} = 8\mu F$).

These harmonics reflect as unwanted high frequency ripples in the DC link voltage. Figure 3.7 shows the distortion in the DC link voltage due to the harmonics in the input current. The harmonics in the DC link due to the LC oscillations affects the current drawn from the grid, thereby reducing the power factor.

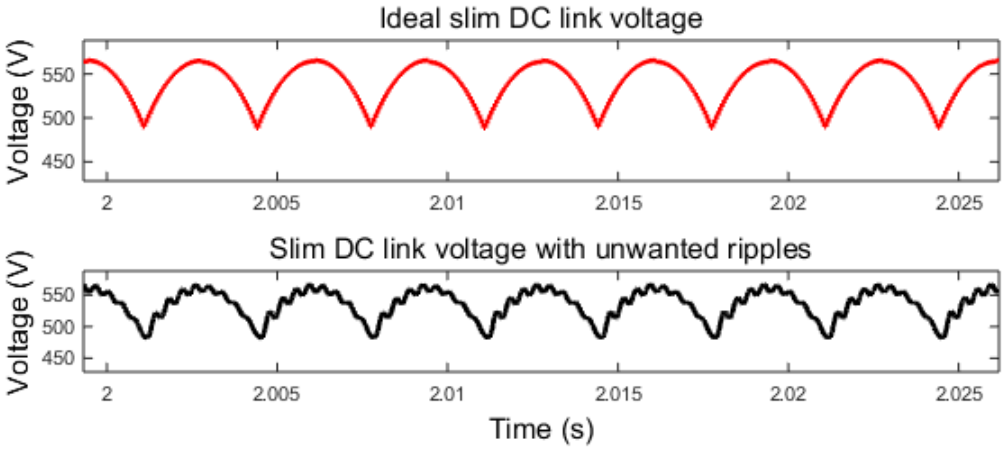


Figure 3.7: Ideal Slim DC link voltage and slim DC link voltage with LC resonance

Chapter 4

Formulation of a control algorithm

Slim DC link has a longer lifespan and improves the power factor of the system. In comparison to these advantages, the unwanted harmonics in the DC link due to LC resonance is a small price to pay. However it is essential to reduce the effects of the unwanted DC link ripple, especially the harmonics induced in the grid current, as the system should comply with the harmonic standards IEC 61000-3-2. This brings us to the research question discussed in Section 1.2.2 which is revisited here. This assignment aims to propose a control algorithm that can suppress the LC resonance such that the total harmonic distortion of the grid current reduces and the power factor of the system improves.

4.1 Effect of the load on harmonic content of the grid current

Adding a resistor R in series to the DC link capacitor will damp the harmonics in the DC link voltage by forming a series RLC circuit. The damping factor ζ of a series RLC circuit with resistance R, capacitor C and inductance L is given by equation (4.1) [20].

$$\zeta = \frac{R}{2}\sqrt{\frac{C}{L}} \tag{4.1}$$

Although the damping increases as R increases, the power dissipation across the resistor also increases resulting in more losses. Instead, the resistance of the load can be increased. the effect of this on the input current is analysed. For this purpose, the circuit shown in Figure 4.1 is simulated in MATLAB and the compliance of the input current to the harmonic standard is analysed. The circuit consists of a *constant power load* and a *resistive load* R connected in parallel. The model is simulated by individually varying the values of power drawn by the resistive and the constant power load, but keeping the total power output equal to 1400W.

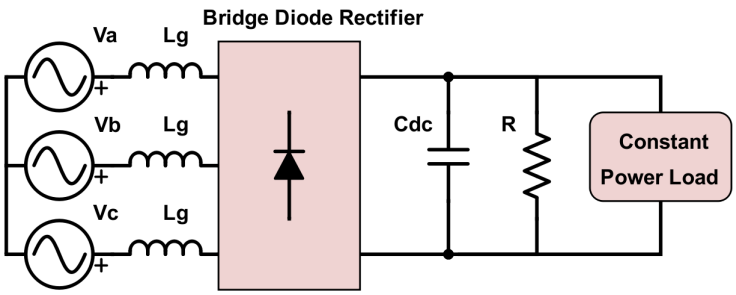


Figure 4.1: Combined resistive load and constant power load

From Table 4.1 it can be seen that as the load becomes more resistive the input current complies with the harmonic standards. Therefore the aim is to formulate an algorithm that makes the load more resistive to damp the harmonics.

Table 4.1: Harmonic compliance for combined resistive load and constant power load

P_R [W]	P_{CP} [W]	IEC 61000-3-2 compliance
-	1400	Not compliant
200	1200	Not compliant
400	1000	Not compliant
600	800	Not compliant
800	600	Compliant
1000	400	Compliant
1200	200	Compliant
1400	-	Compliant

4.2 Formulation of a suitable control algorithm

One way of making the load more resistive is by adding a resistor in series to the motor but this will result in more losses. Instead the existing resistor in the stator can be used to damp the harmonics. The DC link voltage has unwanted ripples as seen in Figure 3.7. As a result, when the measured DC link voltage is fed to the SVM for the calculation of the modulation index as discussed in Section 2.6.2, the duty cycle of the inverter is adjusted such that the output of the inverter is equal to the reference voltages $V_{a'Ref}$, $V_{b'Ref}$, $V_{c'Ref}$ given to the SVM. In this case, the ripples are not passed to the stator and cannot be damped by the stator resistance. But it is necessary to channel the ripples to the stator voltage so that the stator resistance can be used to damp the oscillations. The methods by which the DC link voltage ripple can be made to appear in the stator voltage are given below.

- Controlling the current set point.
- Feed-forwarding the ideal DC link voltage.

4.2.1 Controlling the current set point

This method proposes to control the reference current i_{dRef}, such that the voltage set points to the SVM includes the ripples. As a result, the inverter output will also contain the harmonic ripples and the effect of these ripples will be damped by the dissipation of the additional power across the resistors [21]. The problem faced with this kind of control is that the bandwidth of the current controller should be greater than the frequency of the LC harmonics. The LC resonance frequency depends on the grid inductance and the slim DC link capacitance where as the bandwidth of the current controller will depend on the switching frequency of the SVM. This makes this method unreliable as the system becomes unstable when the grid becomes an extremely weak grid [22]. Another disadvantage of this method is that the current rating of the inverter will increase due to additional d current which is not desirable.

4.2.2 Feed-forwarding the ideal DC link voltage

This is the novel method proposed in this thesis. According to this method by calculating the modulation index with the ideal DC link voltage, the ripples in the input of the inverter will be passed to the output of the inverter and is therefore dissipated in the stator resistance of the motor. To obtain the ideal DC link voltage without ripples, the unwanted high frequency oscillation can be eliminated by using an analog low pass filter. But there is a difference between the time of measurement and the time of control thereby introducing a delay in the control. Also digital filtering introduces an additional delay and requires more memory. These disadvantages can be overcome by predicting ahead of time the ideal DC link voltage, which is the DC link voltage without the higher order harmonics, so that the problem of delay and unwanted harmonics can be eliminated. A feed-forward method is advantageous as it achieves a response without any delay.

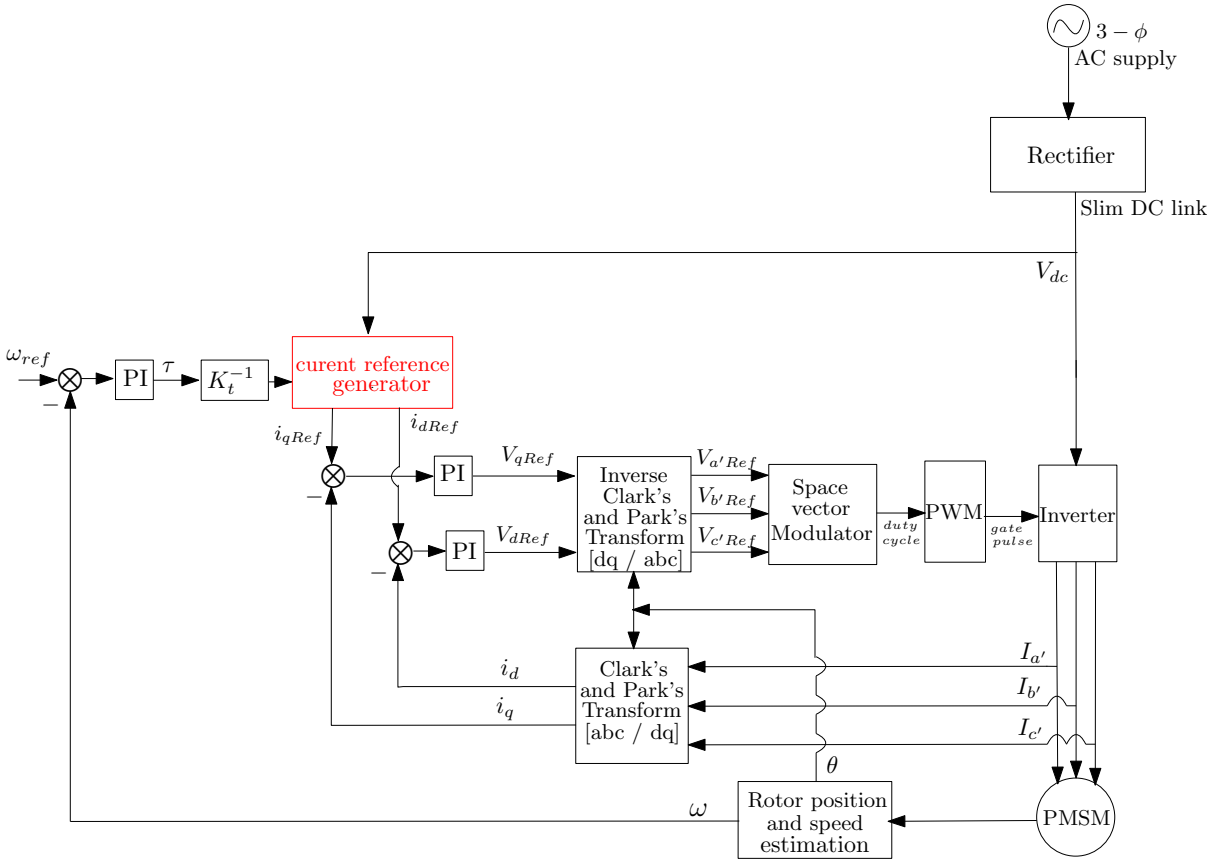


Figure 4.2: Current reference generator

4.3 Design of an algorithm for ideal voltage reconstruction

One of the simplest ways to reconstruct the ideal DC link voltage is by determining the phase and magnitude of the DC link and reconstructing the grid voltage based on the measured values of phase and magnitude. This can then be rectified to obtain the ideal DC link voltage. The simplest method of determining the phase is by detection of zero crossing. But the DC link voltage waveform is distorted by harmonics due the high switching frequencies and LC Resonance and hence has more zero crossings than the ideal waveform. This will result in inaccurate estimation of the frequency and so detection of zero crossing is not a suitable method for determining the phase for this application. A more accurate method of determining the phase and frequency of a given input signal is by using a phase locked loop. Another method of estimating the voltage is by using a model predictive control or a Kalman filter [23]. But these two methods of predictive control require high computational power and hence increases the cost and size of the micro-controller. This kind of accuracy is not necessary for a 2 kW motor for fan applications. Therefore, using a PLL to determine the phase is a good trade off between accuracy and cost. The feed-forward control algorithm using a PLL for voltage estimation is depicted in the Figure 4.3.

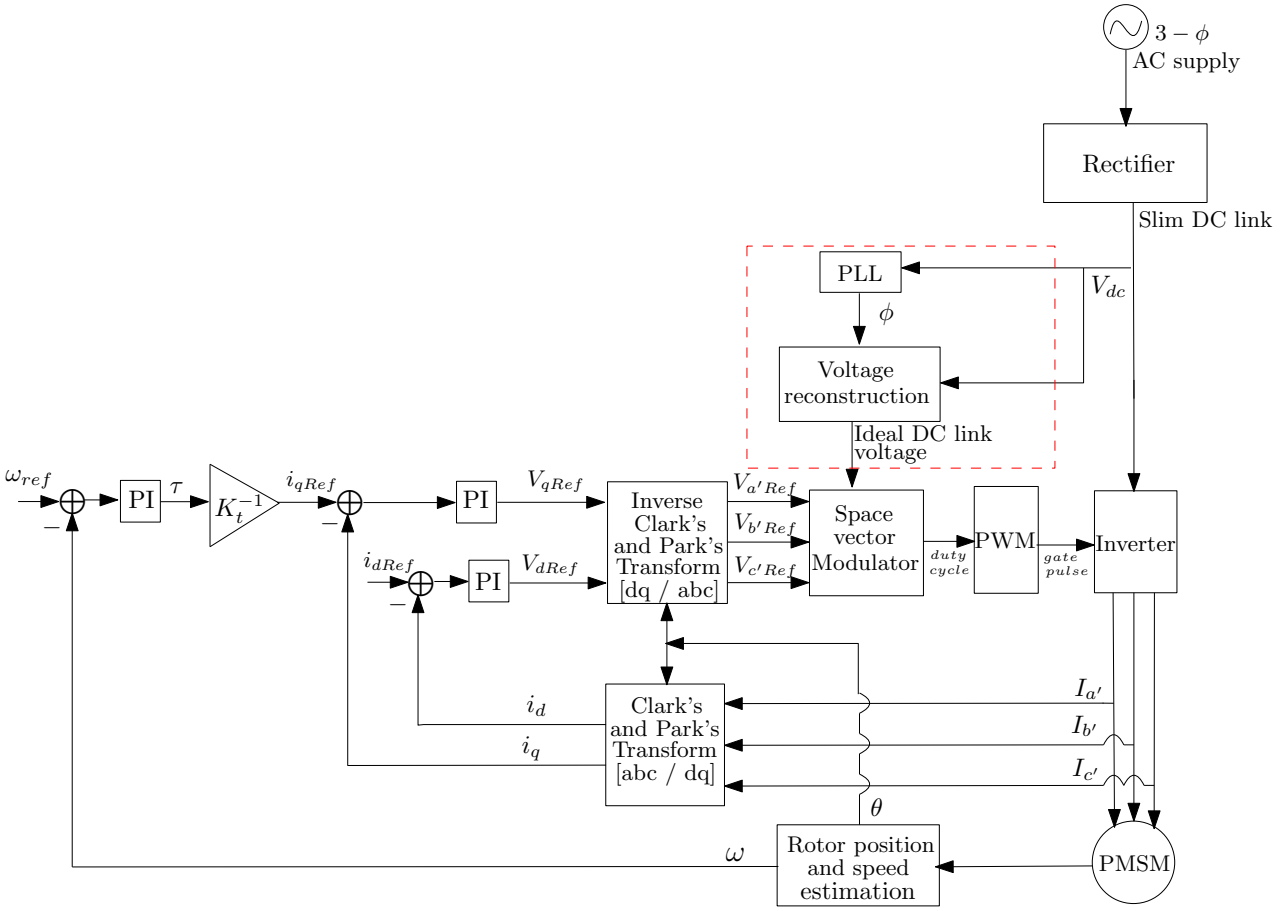


Figure 4.3: Feed-forward control strategy

4.3.1 PLL

The main components of a simple PLL are Phase detector (PD), PI controller and Voltage Controlled Oscillator (VCO) as shown in Figure 4.4. The Phase detector consists of a multiplier and a low pass filter. The multiplier computes the product of the input signal, V_i whose phase needs to be measured (given by eqn (4.2) and the output signal of the PLL, V' (given by eqn (4.3)) which is given as feedback. The output of the multiplier is given by equation (4.5) [24, 25].

$$V_i = cos(\omega_i t + \phi_i) \tag{4.2}$$

$$V' = sin(\omega' t + \phi') \tag{4.3}$$

$$V_i \cdot V' = \cos(\omega_i t + \phi_i) \cdot \sin(\omega' t + \phi') \tag{4.4}$$

$$\implies \frac{1}{2}\sin[(\omega_i + \omega')t + (\phi_i + \phi')] + \frac{1}{2}\sin[(\omega_i - \omega')t + (\phi_i - \phi')] \tag{4.5}$$

where, ω_i and ω' are the frequency of the input and output waveform of the PLL. ϕ_i and ϕ' are the phase of the input and output waveform of the PLL. From equation (4.5) it can be seen that the output of the multiplier has two components. The low frequency component comprises of the phase error, $\phi_i - \phi'$. Therefore, to obtain the error signal the output of the PD is passed through the low pass filter filter so that the high frequency AC component $(\omega_i + \omega') + (\phi_i + \phi')$ is removed. Therefore the output of the low pass filter is,

$$\frac{1}{2}\sin[(\omega_i - \omega')t + (\phi_i - \phi')] \tag{4.6}$$

The PLL is tuned such that ω_i can be made equal to ω'. Output of low pass filter will become,

$$\frac{1}{2}\sin[(\phi_i - \phi')] \tag{4.7}$$

As the phase difference between the input and the output of the PLL is very small,

$$\sin[(\phi_i - \phi')] \approx (\phi_i - \phi') \tag{4.8}$$

Therefore, output of LPF will be equal to

$$\frac{1}{2}(\phi_i - \phi') \tag{4.9}$$

A PI controller is used to reduce the phase error and generates a suitable control output. This is then multiplied by a gain K_{vco} and is added with ω_c. In this assignment, ω_c value is hard coded to the frequency of the DC link voltage ripple and it is equal to six times the grid frequency. This is the tuning done to make equation (4.7) valid. In the event that the grid frequency varies, the error in grid frequency will be added to the error in phase and the controller will automatically try to compensate for both. The value obtained from the sum block is then integrated to obtain the corresponding angle and it's sine value is obtained. Therefore the VCO generates a waveform that is shifted in phase with respect to the input waveform, as a function of the PI controller output. Once the difference in phase between the input and output of the PLL become zero, the PLL is said to be in lock [26].

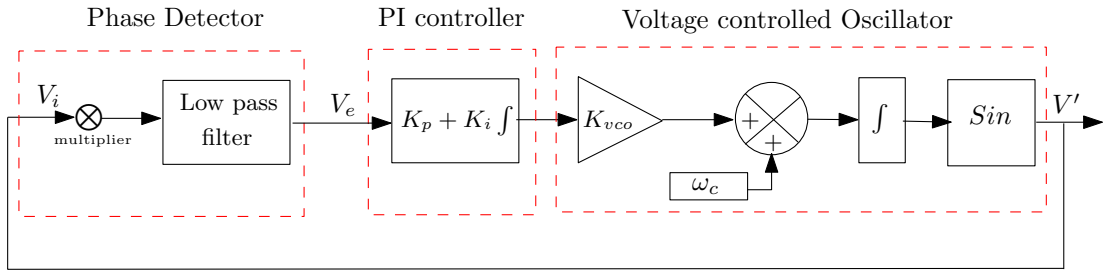


Figure 4.4: Schematics of a simple PLL

4.3.2 Voltage estimation

Once the PLL is synchronized to the measured DC link voltage and the peak is determined, the DC link waveform without harmonics is reconstructed. The method of peak determination and voltage reconstruction is explained in the following chapter. The modulation index is calculated with this value instead of the measured DC link voltage value using equation (2.16) by the SVM.

Chapter 5

Design of the feedback and feed-forward control scheme

The control of a variable speed PMSM employing a slim DC link can be grouped into two main control loops as feedback and feed-forward control, marked by red in the Figure 5.1. The feedback loop controls the speed of the motor using the field oriented control algorithm. The feed-forward control compensates for the effect of the unwanted harmonics in the DC link voltage, by reconstructing the ideal DC link voltage. This chapter defends the design decisions for implementing the control algorithm proposed in chapter 4.

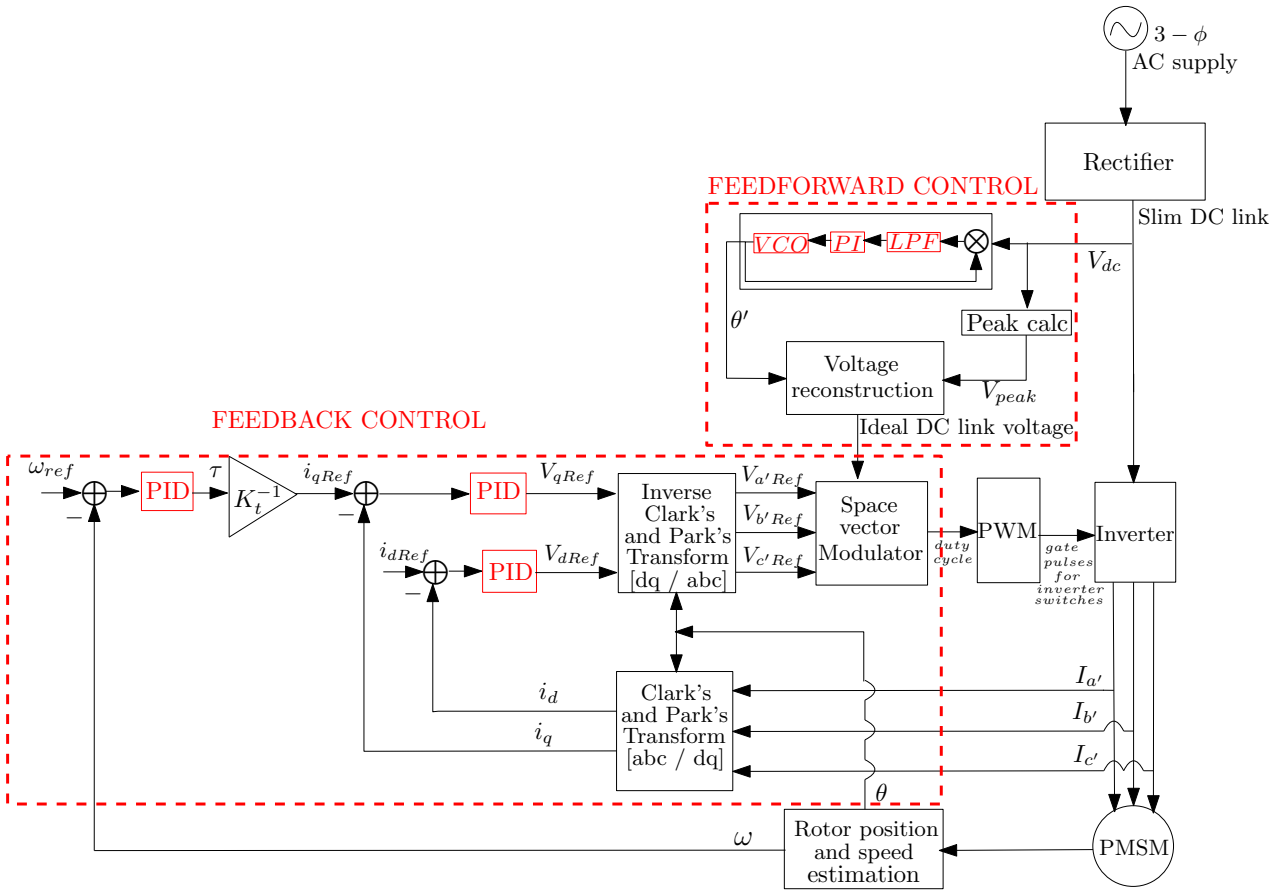


Figure 5.1: Feedback and feed-forward control

5.1 Feedback control loop

The feedback control is nothing but the field oriented control and consists of 1 PID controller to control the speed and 2 PID controllers to control the current as shown in Figure 5.1. As the control algorithms are implemented using a micro-controller, the control algorithm is implemented in the discrete domain. A simple PID controller can be used for all the three controllers.

5.1.1 Classical controllers

PID controllers are the most commonly used error based feedback controllers for linear systems. A PID controller provides a corrective action based on the difference between the set point and the measured output value. The corrective action could be to reduce steady-state error, improve disturbance rejection, increase the speed of response or to damp the over shoot. Depending on the kind of control action required the type controller is decided. The controller can be a P, PI, PD, or PID controller. The transfer function and bode plot of each of the controllers are given below [27]. Bode plot is the plot of gain vs frequency and the phase vs frequency for a given transfer function. It is used to understand the frequency response of the transfer function.

PI controller

The transfer function of a PI controller is given by equation (5.1),

$$C(s) = K_p + \frac{K_i}{s} = \frac{K_p s + K_i}{s} \tag{5.1}$$

Where K_p is the proportional gain and K_i is the integral gain.

The bode plot of a PI controller is given in Figure 5.2.

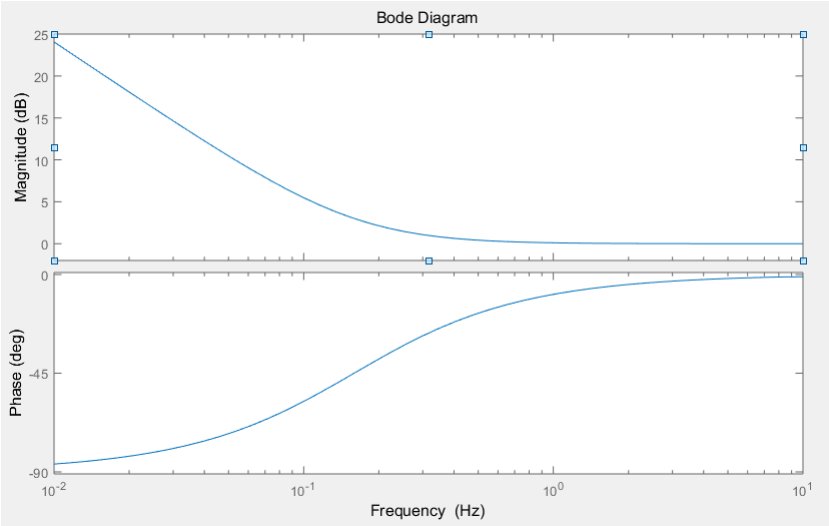


Figure 5.2: Bode plot of a PI controller

From the bode plot it can be seen that the gain is 0 for higher frequencies. Therefore, the PI controller can be used as a low pass filter where the pole is placed in the cut off frequency. This is a preferred method of implementing the low pass filter as it holds only one value of data whereas the conventional low pass filter will require a larger buffer to hold all the samples.

PD controller

The transfer function of a PD controller is given by equation (5.2),

$$C(s) = K_p + K_d s \tag{5.2}$$

Where K_p is the proportional gain and K_d is the derivative gain.

The bode plot of a PD controller is given in Figure 5.3.

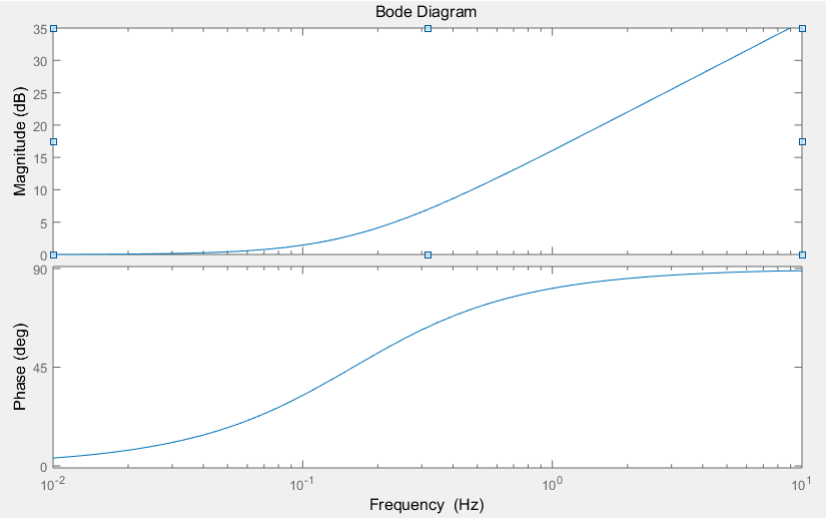


Figure 5.3: Bode plot of a PD controller

From the bode plot it can be seen that the magnitude tends to infinity at higher frequencies. As a result the high frequency noises will be amplified. To avoid this a stand alone PD controller is rarely used. A pole is added to stabilize the gain at higher frequencies as given by equation (5.3) [28].

$$C(s) = K_p + \frac{K_d s}{s + D_p} \tag{5.3}$$

D_p is the pole that is added and this type of PD controller is known as filtered derivative. The bode plot of the new system is given by the Figure 5.4.

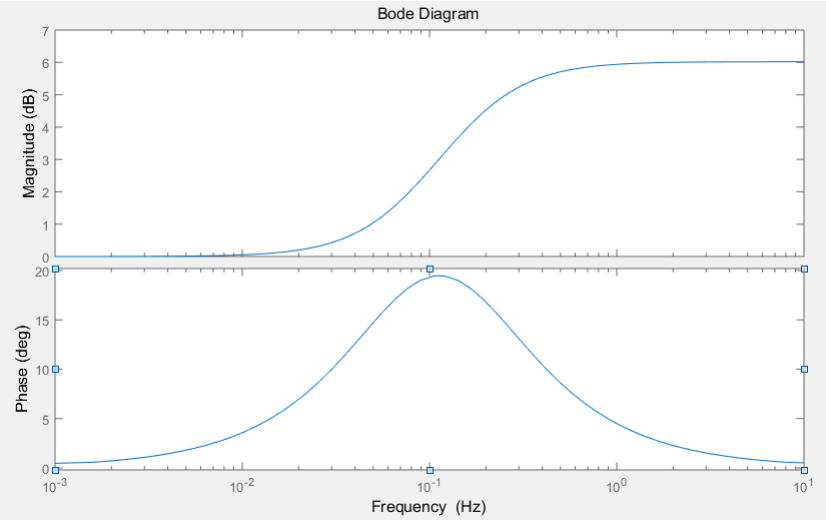


Figure 5.4: Bode plot of a filtered PD controller

PID controller

A simple PID control is a combination of the PI and PD controller and is given by the equation (5.4).

$$C(s) = K_p + \frac{K_i}{s} + \frac{K_d s}{s + D_p} = \frac{K_p s(s + D_p) + K_i(s + D_p) + K_d s^2}{s(s + D_p)} \tag{5.4}$$

Where K_p is the proportional gain, K_i is the integral gain, K_d is the derivative gain and D_p is the pole that is added to stabilise the gain at high frequency for the PID controller. From equation (5.4) it can be seen that the order of the numerator and denominator are both two. Hence it can be concluded that a PID controller with a filtered derivative will have two poles and two zeros.

As discussed, is necessary to implement the controller in the discrete domain. A double pole-zero controller in the z domain is given by the equation (5.5) [29].

$$k \cdot \frac{(z - a_1)(z - a_2)}{(z - b_1)(z - b_2)} \tag{5.5}$$

where K is the gain, a_1 and a_2 are the zeros, b_1 and b_2 are the poles of the controller. To obtain a PI or a PD controller which are single pole-zero systems, the parameters a_2 and b_2 can be set to zero. In order to tune the controller parameters (k, a_1, a_2, b_1, b_2) and obtain a stable system, the state space model of the motor drive system is derived and the stability can be assessed by using the bode plot of the control loop.

5.1.2 Stability of a closed loop system

Bode plot for stability analysis

Figure 5.5 shows the closed loop configuration of a system with a feedback control. The open loop transfer function for this system is the ratio of the output 'y' to the error 'e'. From the bode plot of the open loop transfer function the phase margin and the gain margin can be calculated and this will give information on the stability of the control loop. For the closed loop to be stable, both the gain margin and the phase margin should be positive. For each of the controllers implemented, the stability of the control loop is assessed by using the bode plot.

Phase margin

Gain cross over frequency: It is the frequency at which the gain is 0 dB, ie. the input is equal to the output.

The phase margin is determined by adding 180 degrees to the phase, at the gain cross over frequency.

Gain margin

Phase cross over frequency: It is the frequency at which the phase becomes -180 degree.

The gain margin is defined as negative of the gain, at the phase cross over frequency.

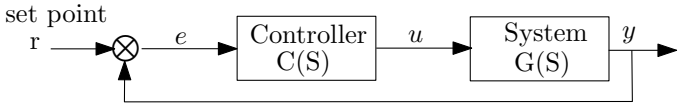


Figure 5.5: Architecture of a feedback system

5.1.3 Current controller

The electrical part can be modeled using the current equation given by (2.8) which is once again given below for reference.

$$\frac{di_d}{dt} = \frac{1}{L_d}V_d - \frac{R}{L_d}i_d + \frac{L_q}{L_d}P\omega_r i_q \tag{5.6}$$

As discussed, $L_q = L_d$ and henceforth denoted as L and $V_d = -LP\omega_r i_q$, . Therefore, the Laplace transform of the equation (5.6) is given by equation (5.7). This is the transfer function of the electrical system.

$$G(S) = \frac{i_d}{V_d} = \frac{1}{Ls + R} \tag{5.7}$$

The current controller chosen for this system is the PID controller given by equation (5.5). The open loop transfer function for the control loop consisting of the current controller and electrical system is computed. The bode plot of this open loop transfer function is plotted and the current controller is tuned such that the plot becomes stable. The bode plot of the tuned control system is shown in Figure 5.6 The phase margin is 52.1 degree and the gain margin is 15.5 dB and so it can concluded that the current control loop is stable.

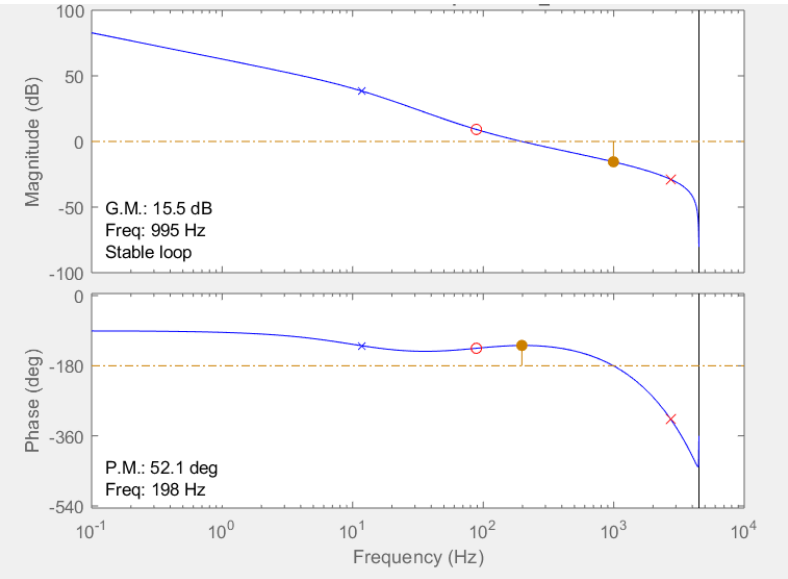


Figure 5.6: Bode plot of electrical system with a current controller

As i_q and i_d have the same system equation their respective controllers can be tuned to have the same parameters. The current controller needs to be fast enough to generate the set point for the space vector but slower than the frequency of the PWM. The controller can be updated once every PWM cycle. The PWM update frequency is 9kHz and it is described in more detail in Appendix B.2. Therefore the sampling time of the system T_s, is 0.11ms. The step response of a closed loop system is obtained by giving a unit step pulse as set point to the controller and plotting the time taken for the output of the system to become unity. The step response of the electrical system with the tuned current controller is shown in Figure 5.7. From the figure it can be seen that the settling time of the controller is in the order of milliseconds.

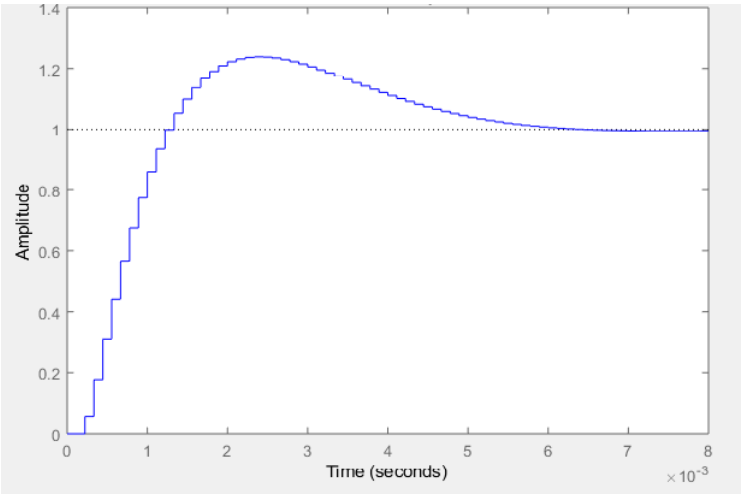


Figure 5.7: Step response of the electrical system with a current controller

5.1.4 Speed Controller

The mechanical part of the motor can be mathematically modelled as

$$\frac{d\omega}{dt} = \frac{1}{J} \cdot (\tau - D \cdot \omega) \tag{5.8}$$

where ω is the mechanical speed and τ is the torque. D is the damping coefficient and J is the inertia constant. The transfer function is then obtained by taking the Laplace transformation of the above equation and it is given as,

$$\frac{\omega}{\tau} = \frac{1}{Js + D} \tag{5.9}$$

The speed controller can be tuned for the system given by the above equation in the same way as the current controller. Therefore the bode plot is then analysed for the open loop transfer function of the speed controller and mechanical system. From Figure 5.8 it can be seen that the gain margin is 19.6 dB and the phase margin is 74.1 degree. As they are both positive it can be concluded that the control loop is stable.

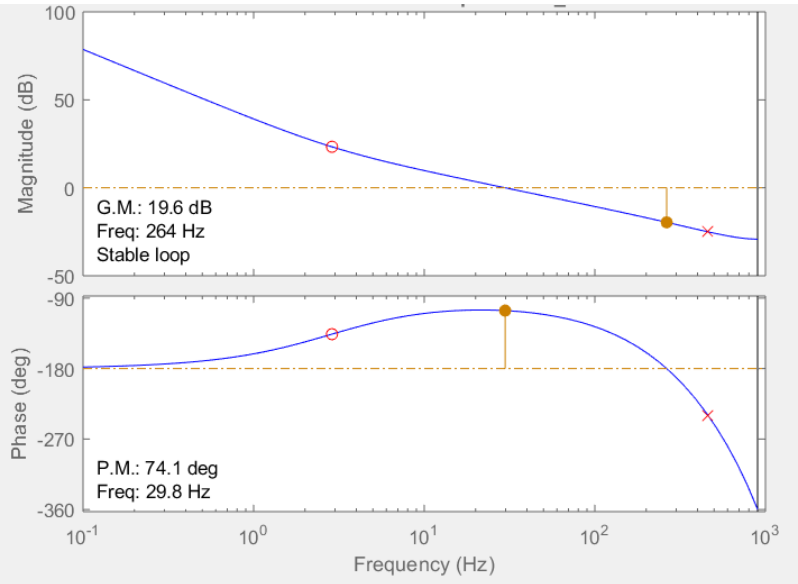


Figure 5.8: Bode plot of mechanical system with a speed controller

The update frequency of the speed controller can be much slower than the sampling frequency of the current controller. This is because the two controllers are cascaded and the inner controller should have a higher bandwidth than the outer controller for a stable system, preferably by a factor of 5 to 10. Another constraint for selecting the sampling frequency of the speed controller is the response time of the mechanical system. In general the mechanical response will be slower and in the order of seconds. Therefore, a sampling frequency of $\frac{1}{10}$ of the switching frequency is taken as the sampling frequency of the speed controller. The Figure 5.9 shows the step response of the mechanical system with the designed speed controller and it can be seen that the settling time is about 0.2 seconds.

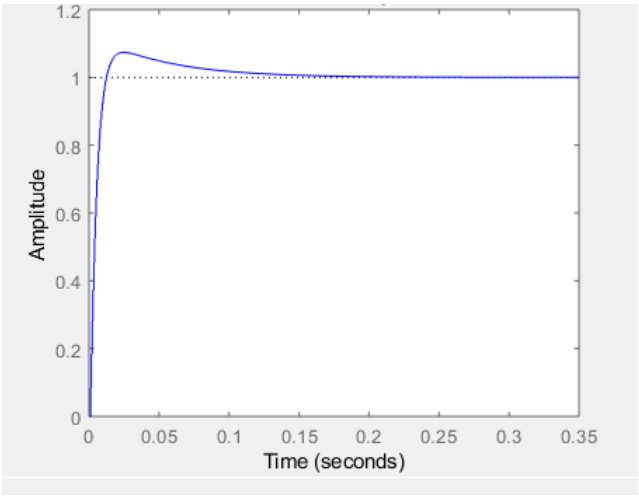


Figure 5.9: Step response of the mechanical system with a speed controller

5.2 Feed-forward Control

The feed-forward control consists of three major blocks as shown in Figure 5.1. They are the PLL, Peak detection and voltage reconstruction. The implementation of each of the blocks in the discrete domain is discussed in this section.

5.2.1 PLL

From Figure 5.1 it can be seen that the main components of the PLL are multiplier, low pass filter, PI controller and the voltage controlled oscillator. The PLL can be considered as a simple feedback control loop where the low pass filter and the PI form the controller and the VCO can be considered as the system.

Low pass filter - Phase Detector

A low pass filter is necessary to filter the high frequency component in the error waveform. For this a discrete first order filter can be used . A first order discrete low pass filter can be given by (5.10) [30].

$$y[k] = \alpha u[k] + [1 - \alpha]y[k - 1] \tag{5.10}$$

where $\alpha = \frac{\omega_c Ts}{1+\omega_c \cdot Ts}$ and hence $[1 - \alpha] = \frac{1}{1+\omega_c \cdot Ts}$

where ω_c is the cut off frequency for the low pass filter in rad/sec and Ts is the sampling time of the discrete low pass filter in sec. $u[k]$ is the output of the multiplier in phase detector and $y[k]$ is the error in phase V_e. The cut off frequency for this low pass filter should be $((\omega_i + \omega') + (\theta_i + \theta'))$ as per equation (4.5). From equation (5.10) it can be seen that this low pass filter implementation is similar to a single pole zero implementation.

PI

The output of the low pass filter is the difference between the phase of the input signal and the phase of the PLL output, which is the error V_e. In order to reduce the error a simple PI controller can be used and is implemented using a single zero pole compensator.

Voltage controlled oscillator

The voltage controlled oscillator integrates ω and gives an output θ using the discrete integrator. This θ increases at the rate proportional to frequency of the DC link. In order to obtain the grid frequency it has to be divided by a factor of six as for a 3 phase grid supply the rectified voltage is six times the grid frequency. The state space is given by,

$$\frac{d\theta}{dt} = \omega \tag{5.11}$$

$$\frac{\theta}{\omega} = \frac{1}{s} \tag{5.12}$$

Discrete Integration:

In order to integrate in the discrete domain, Backward Euler's formula is used. It is given by the equation (5.13)

$$y(n) = y(n-1) + K \cdot [t(n) - t(n-1)] \cdot u(n) \tag{5.13}$$

where K is the Euler's integration constant and [t(n) - t(n-1)] is nothing but the time difference between subsequent samples which is equal to the sampling time Ts. Hence equation (5.13) can be rewritten as,

$$y(n) = y(n-1) + K \cdot Ts \cdot u(n) \tag{5.14}$$

Stability of PLL

The low pass filter could also be represented as a zero pole compensator. The PI controller along with low pass filter forms a double pole zero. The plant is given by the equation (5.12). Therefore, the stability of the PLL can be analysed using the bode plot of the open loop transfer function shown in Figure 5.10. As the phase margin and the gain margin are positive it can be said that the system is stable.

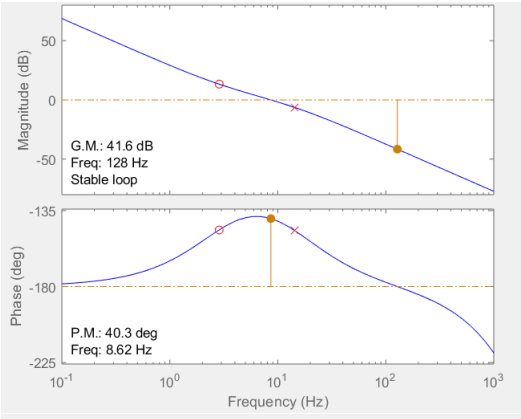


Figure 5.10: Bode plot of the PLL

5.2.2 Peak detection

The peak detection is used to calculate the peak of the DC link voltage. This peak will in turn give the value of the peak of the grid voltage. The most common method of peak detection is to sample the entire wave and find the maximum of the samples. This takes up a lot of buffer space, which is not acceptable in embedded systems with limited memory. The frequency of the DC link voltage is 300 Hertz. The peak calculation block designed for this thesis, samples the DC link voltage during the rising period of the wave and compares it to the previous sample. If it is higher than the previous value it holds it else discards the sample. This value is used as the peak value for the second half period of the DC link voltage thereby reducing the amount of data stored to two bytes. The value is not updated immediately to avoid detection of local peaks due to the ripple.The same data is used for the first half of the next cycle when the DC link voltage gets sampled. The output of the peak detection block is shown in Figure 5.11. The simulation results shown in the figure is the case when one of the phases of the three phase input supply has a higher amplitude. It can be seen from the figure that for the first case in which the amplitude increases the peak is updated only after half the cycle. Though there is a delay of half a period this algorithm is robust when the DC link voltage is rippled and therefore appropriate for this application.

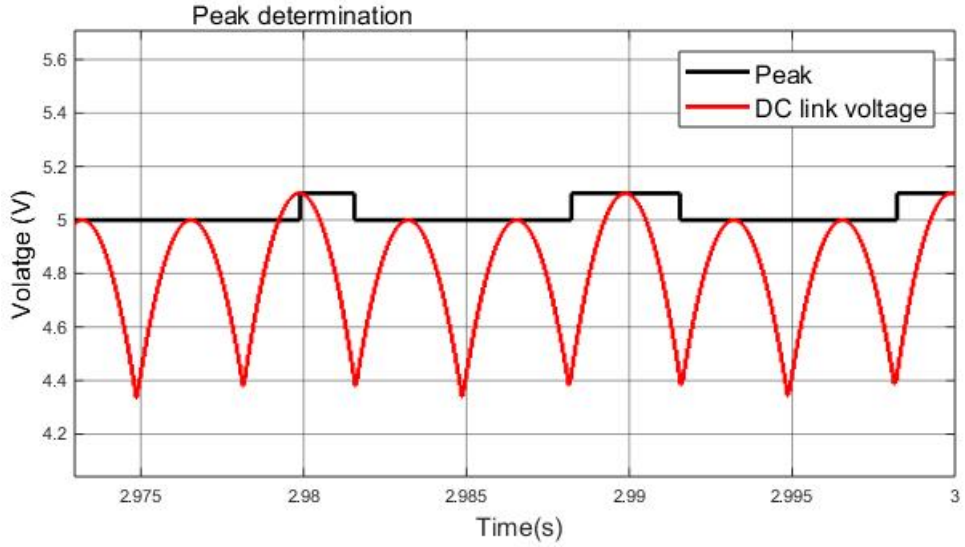


Figure 5.11: Peak detection

5.2.3 Voltage estimation

Once the PLL is in lock with the DC link voltage ripple and the grid frequency is determined, the ideal DC link voltage can be reconstructed. The voltage reconstruction block recreates the 3 phase grid voltages using the peak value of the voltage V_{peak} and the grid frequency ω using the equations in (5.15). The maximum of the absolute value of the 3 phase voltage waveform recreates the DC link voltage.

$$V_a = V_{peak} \cdot sin(wt); \qquad V_b = V_{peak} \cdot sin(wt + 2\pi/3); \qquad V_c = V_{peak} \cdot sin(wt - 2\pi/3) \tag{5.15}$$

Chapter 6

Modeling and Simulation

In order to check the feasibility of the feedback and feed-forward control, designed in chapter 5, the motor drive along with it's control loop is simulated using MATLAB simulink software. The modeling is split into two parts, one part is modeling the field oriented control for the speed control of the permanent magnet synchronous motor and the other part is simulating the phase locked loop to lock to DC link waveform. These two parts are implemented one after the other such that the PLL can lock with the DC link voltage of the closed loop speed control model. This chapter mirrors the structure of the previous chapter. For the design of every block in chapter 5 there is an equivalent section in this chapter showing the simulation results and validating the design of that section.

6.1 Simulation results of the feedback controller

The feedback control is implemented in order to realise the FOC discussed in chapter 2. The scope of this thesis includes simulation of the designed speed and current controller whereas the motor and the electronics are simulated using the MATLAB toolbox. The parameters for which the motor is simulated is given in the table 6.1

Table 6.1: Specifications of PMSM and its electronics

PARAMETER	VALUE	UNIT
DC link capacitance	8	μF
Grid inductance	100	μH
Stator resistance	1.5	Ω
Stator Inductance	15	mH
No. of pole pairs	5	-
Rotor inertia (J)	0.01	$kg \cdot m^2$
Damping coefficient (B)	0.0000923	$N \cdot m/(rad/s)$
Rated speed	3000	rpm
Rated power	2	kW

6.1.1 Current controller

In order to test the current controller designed in Section 5.1.3, a closed loop system as shown in Figure 5.5 is simulated using the current system given by equation (5.7) and the designed current controller. The step response shown in Figure 6.1 is obtained upon simulation. As per the design, a step response in the order of milliseconds was expected. The step response of the simulated model is about $4 \times 10^{-3}s$ seconds thereby validating the designed current controller.

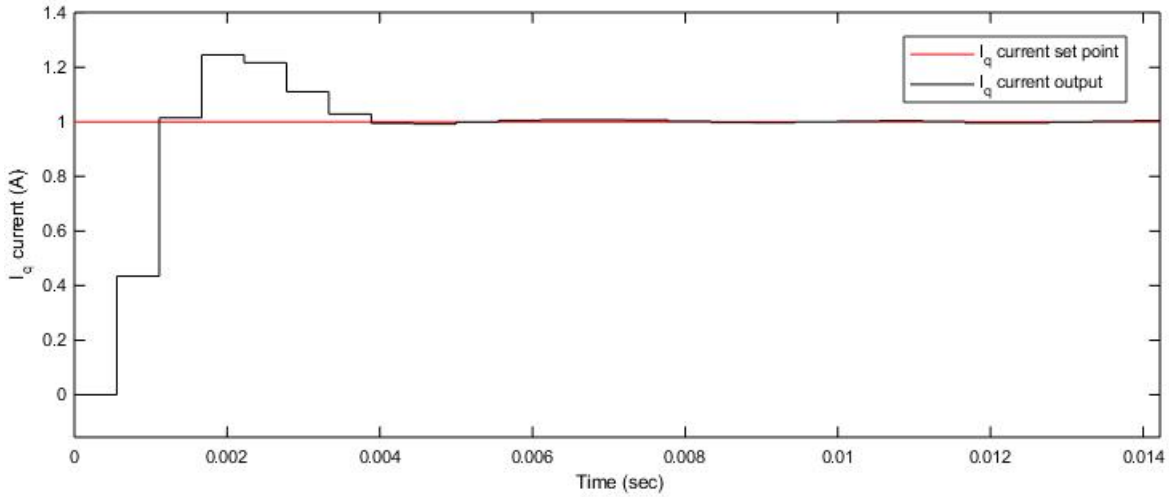


Figure 6.1: Simulation results showing the response of electrical system with the current controller

6.1.2 Speed controller

The speed controller is simulated with the motor and the complete FOC. The black line in Figure 6.2 shows a mechanical speed set point of 314 rad/sec which is the rated speed of the motor and the red curve shows the speed of the motor. The The response of the motor can be considered fast as it reaches this speed at about 1.725 seconds. The response of the speed controller is in accordance with the design which was in the order of seconds, thereby validating the design.

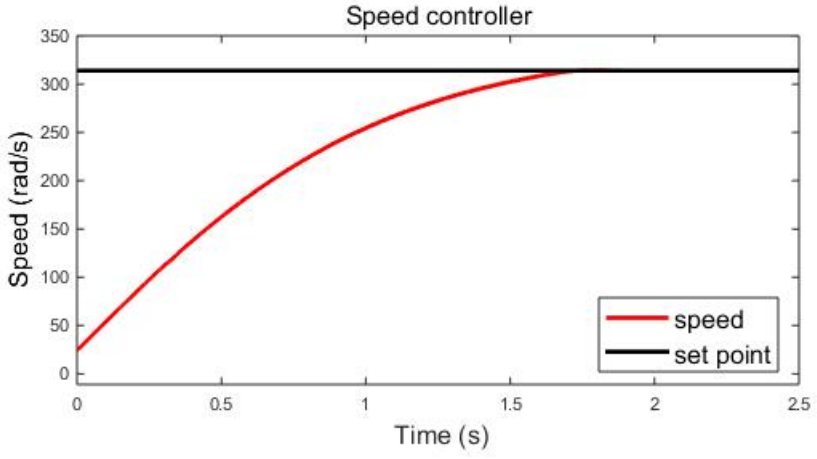


Figure 6.2: Simulation results showing the response of the motor with the speed controller

6.2 Simulation results of the feed-forward controller

The voltage estimation is implemented for the DC link voltage waveform containing higher order harmonics due to LC resonance. Upon achieving a lock using the PLL and an accurate voltage estimation, the feed-forward control will be integrated to the motor model implemented in the previous section.

6.2.1 PLL

The Figure 6.3 shows 2 graphs. The first waveform is the slim DC link voltage with unwanted higher order harmonic ripples V_{dc}, shown in Figure 5.1. This waveform is obtained from MATLAB simulink upon simulation of the feedback control described in Section 6.1, and is given as the input for the PLL. The second waveform is the output of the integrator and the input of the sine block in the VCO. From the graph it can see that the two waveforms are in phase and have the same frequency. Therefore, the PLL is said to be in lock with the DC link voltage.

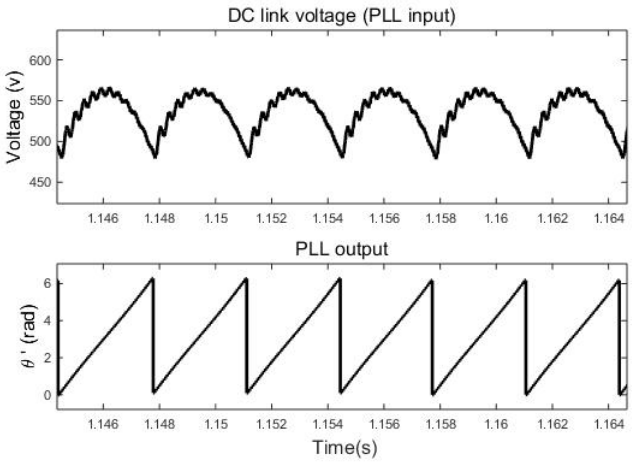


Figure 6.3: Simulation results of the PLL

6.2.2 Simulation results of the Voltage estimator

Figure 6.4 shows the simulation results of the voltage reconstruction block. The black graph represents the DC link voltage with LC oscillations. The red graph shows the output of the voltage estimator using a PLL simulated in the previous section. It can be seen that the estimated voltage is close to the ideal DC link voltage and has almost no unwanted higher order harmonic ripples. It can also be seen that there is no delay between the reconstructed value and the measured value.

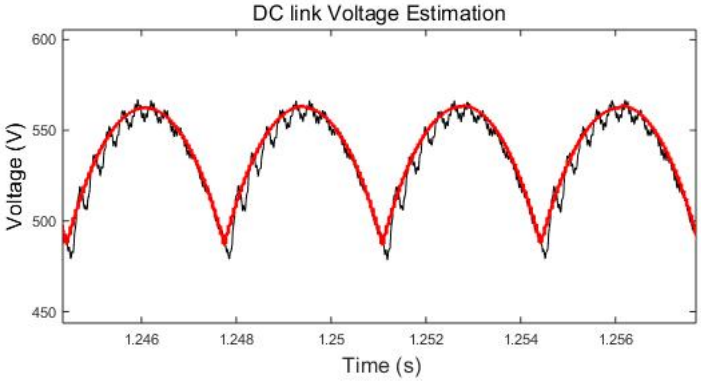


Figure 6.4: Simulation results of the Voltage estimator

6.3 Harmonic content of the grid current

The feed-forward control is integrated with the field oriented control by giving the reconstructed voltage as input to the space vector modulator. The integrated model is then simulated and the grid current is plotted as shown in Figure 6.5. The Fast Fourier Transform (FFT) of the measured current is determined to calculate the harmonic content of the current. Figure 6.6 shows the harmonic content of the grid current and it can be seen that all the harmonic order are within the IEC 61000-3-2 standard thereby proving that the proposed feed-forward control suppresses the harmonics in the grid current. The control was simulated for various grid inductance values above $70\mu H$. The same system simulated without the feedforward algorithm is shown in Figure 3.6a. In comparison, it can be seen that the higher order harmonics are damped and the system complies with the harmonic standards when the proposed feedforward control is used. The system complies with the harmonic standards for a maximum grid inductance of 150 μH, for a motor running at the rated speed and in the full load condition.

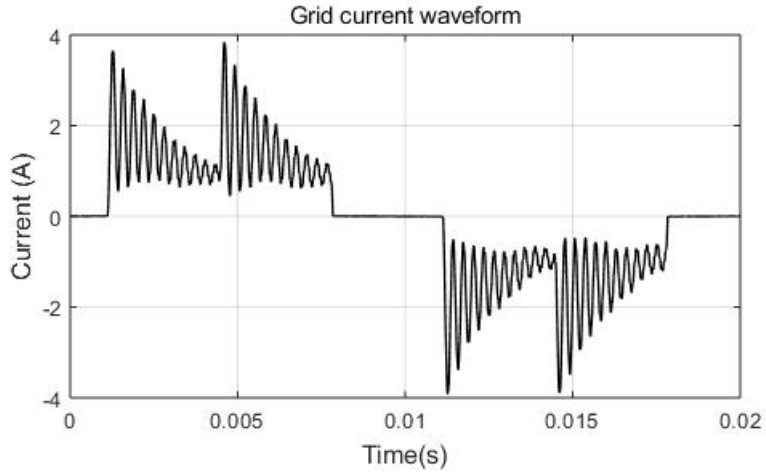


Figure 6.5: Grid current ($OutputPower = 1.45KW, C_{dc} = 8\mu F, L_g = 150\mu H$)

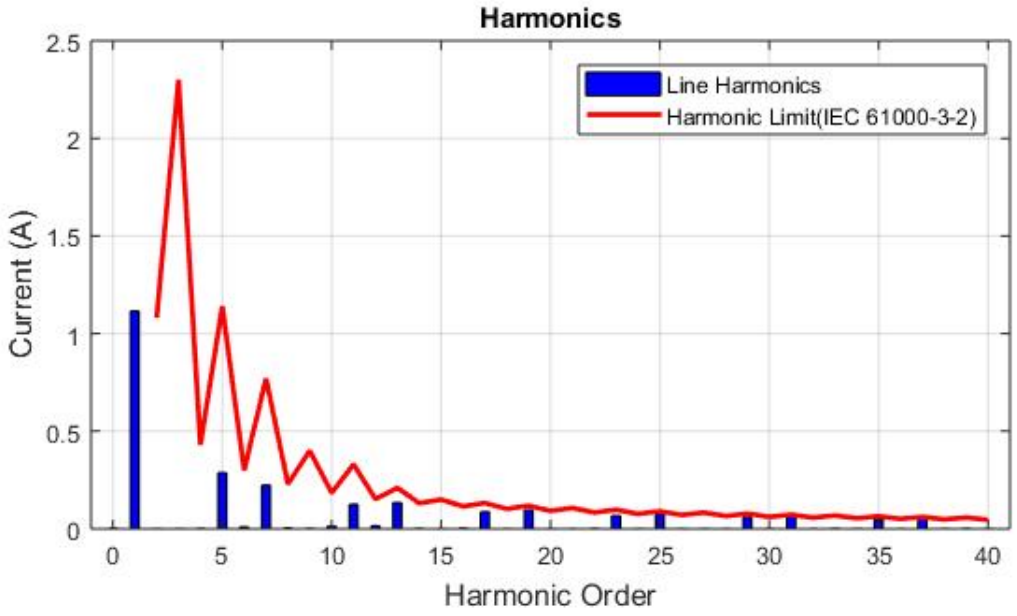


Figure 6.6: Harmonic content in the grid current ($OutputPower = 1.45KW, C_{dc} = 8\mu F, L_g = 150\mu H$).

Chapter 7

Micro-controller Implementation

This chapter describes the software architecture used and how it supports model based software development. This chapter then explains the advantages and disadvantages of using AMDF for the development of embedded software.

7.1 Influence of the embedded controller on the design parameters

The notable feature of embedded systems is the ability to control a working device in real time. The size and the computational power of the micro-controller for a specific application poses a severe limitation on the functionality that can be performed. The micro-controller chosen for the 2 KW motor drive system is the STM32F303RC. The advantage of using this controller is that it has a floating point unit. It has a flash memory of 128 kB and a RAM of 48 kB. The Keil μ -vision 5 is the compiler that is used. For this thesis, the following features need to be implemented in the micro-controller,

- Sensorless speed estimation.
- Field oriented control (or) feedback speed control.
- The feed-forward control to dampen the unwanted harmonics due to LC resonance.

It is necessary to code effectively in order to ensure that the RAM size is not exceeded. Many design decisions such the algorithm for peak detection and the design of a low pass filter have been made based on this constraint. Also the PWM switching frequency is limited by the capability of the micro-controller. This in turn determines the bandwidth of the speed and the current controller. Also, in order to ensure that there are no timing issues in the embedded controller, investigation has to be made to ensure that the code size and the performance is within the capability of the micro-controller.

7.2 Software architecture

The control system of a power converter requires high precision and complex computations. Therefore, it is necessary to ensure that the developed embedded software for control is stable and reliable. Figure 7.1 shows the embedded software architecture developed for the realisation of the control algorithm using a micro-controller. The Hardware Abstraction Layer (HAL) is the lowest layer and its configuration is explained in detail in Appendix B. The AMDF, infrastructure and the application layers are designed such that the architecture supports model based software programming and these blocks are explained in detail in the following section.

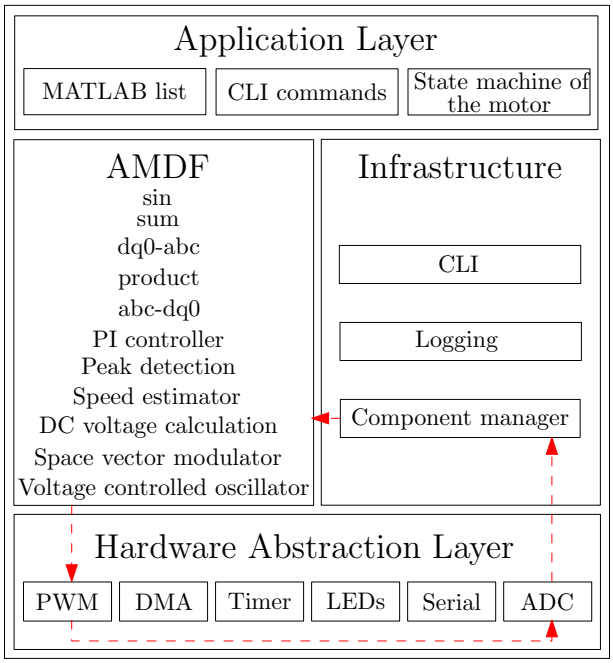


Figure 7.1: Embedded software architecture

7.3 Model based software development

AME Motor Drive Framework (AMDF) is a software platform developed for power drives in order to standardise the control blocks. AMDF is versatile for a wide range of power drive applications, eg. battery management units, motor control units. The key feature of AMDF is that it supports model based software development. Model based software development enables the translation of a simulation model to embedded software. This feature will ensure that the embedded software is in accordance with the designed control loop thereby avoiding any discrepancy in functionality during code development. The block diagram in Figure 7.2 shows the realisation of the model based software development.

It can be seen that the once the control is designed and validated in simulation, a list of the SIMULINK blocks used is generated using a MATLAB script. This MATLAB list is a .h file and gives information on the blocks present and its order of execution. This list is specific for every control algorithm and hence unique for each application. Therefore it comes in the application layer. The AMDF block contains C functions for the various mathematical and control operations. The component manager in the infrastructure block executes the C function in the AMDF block, in the order given by the MATLAB list. Therefore the infrastructure and AMDF is generic for all the applications.

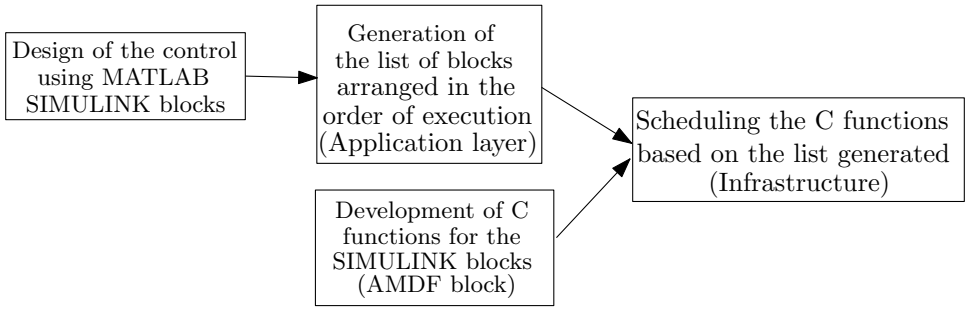


Figure 7.2: Block diagram showing model based software development

7.4 AMDF blocks

The blocks that are needed for the control are listed inside the AMDF block in the Figure 7.1. The functionality and design of each of these blocks have been discussed in Chapter 5. Based on the design, these blocks have been programmed in C and included in the AMDF library as a part of this thesis. They are made generic and can be used for other control algorithms.

Advantages of the designed AMDF block

- Reusability of code - When the control algorithm has multiple instances of the same block, the corresponding C function in AMDF can be used for all the instances. For example the PI controller function in AMDF can be for both speed controller and current controller by varying the parameters.
- Robust code development - This method of code development ensures correct implementation of the control in embedded software. The functionality of the simulation is mapped to code by the architecture thereby eliminating human error.

Timing for the control

The C functions, developed as a part of the AMDF block, are compiled along with the generated MATLAB list and then flashed in the controller. Then the worst case execution time of each of the blocks is measured. The total worst case execution time of the designed control algorithm is measured at run time and it is determined to be 81.45 μS. The duty cycle is updated once every 83.34 μS (This is explained in Appendix B.2 with the PWM timing diagram). Therefore we can see that there is just enough time to complete the control. In the event that the duty cycle needs to be updated at a higher frequency for other applications, there will not be sufficient time for the control. AMDF aims to be compatible with a wide range of applications but because of the timing constrains it will not be suitable for high frequency applications.

Chapter 8

Conclusion

In this thesis a feed-forward control algorithm was proposed and then developed as embedded software using AMDF. The assignment comprises of two parts - design of a control system to reduce the harmonics in the grid current and the development of AMDF blocks to support model based software programming. Chapter 2 explained the concept of field oriented control which is a vector method for speed control. Chapter 3 discussed the need for film capacitors in the DC link and its effects on the performance of the motor drives. It introduced the problem of LC resonance due to the grid inductance which brings us to the research question.

"How can the unwanted oscillations in the grid current, drawn by the motor drive employing slim DC link, be damped or suppressed such that the motor drive complies with the IEC 61000-3-2 harmonic standard?"

Various control algorithms to suppress the oscillations and its pros and cons were discussed in chapter 4. A novel method of feed-forward control was put forth whereby the DC link voltage is measured, and using this the ideal DC link voltage is reconstructed. This reconstructed voltage is given as input to the space vector modulation which determines the duty cycle of the inverter. By controlling the inverter switching, the motor can be made to behave as a resistive load and as a result reduces the reactive power absorbed by the motor. This implies that the current drawn by the motor drive from the grid will be in phase with the supply voltage and the current waveform will be less distorted from the sinusoidal waveform. The design of the proposed feed-forward algorithm along with the field oriented control was explained in chapter 5. The stability analysis of the control loop is included in this chapter as well. The designed control strategy was simulated and the results are included in chapter 6. From the results it can be concluded that the proposed control algorithm can be used to successfully suppress the harmonics in the grid current such that the motor drive complies with the IEC 61000-3-2 harmonic standard. Once the control system design was validated using simulation, the motor drive framework was extended to support embedded software development using model based software development for 3-phase motor drives. The AMDF blocks for the designed control algorithm were developed and optimised such that the worst case execution time of the control is within the threshold.

8.1 Scope for future work

Extension of the feed-forward control

The proposed method can damp the harmonics in the input current for a maximum grid inductance of 150 μH. This is because the proposed algorithm aims to make use of the existing stator resistor to damp the harmonics. As this resistance value is fixed, research can be done to integrate other methods of damping to the proposed algorithm such that the motor behaves as close as possible to a resistive load. This behavior of the motor will improve the power factor.

Improving the Infrastructure block

In chapter 7, it was shown that the AMDF will not be able to meet the timing constraints for applications that operate at higher frequencies. As AMDF is developed to be generic for a wide range of applications, research can be done to reduce the time taken to implement the control by investigating the infrastructure block. The component manager can be studied to see if there is scope for improvement such that the time spent in fetching each of the AMDF blocks is reduced. Other methods of scheduling can also be investigated to replace the component manager.

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Appendix A

Limits for harmonic current emissions

A.1 IEC 61000-3-2 for low power applications

A variable speed drive for which the current drawn by one of the phases is less than 16A needs to comply with the current harmonics rating of class A of the IEC 61000-3-2 standard, which is the limits for harmonic current emissions (equipment input current ≤16 A per phase) [31]. As the system under consideration in this thesis, is a drive for low power motors and the current drawn is less than 4A it falls under this category.

Harmonic order (h)	Maximum permissible harmonic current (A)
3	2.3
5	1.14
7	0.77
9	0.4
11	0.33
13	0.21
15 <= h <= 39	0.15 * 15/h

Table A.1: Limits for Class A equipment

Appendix B

Hardware abstraction layer

The configuration of the ADC (Analog to Digital Conversion) and PWM is described in this section. The figure B.1 shows the pin mapping of the ADCs, PWMs, clock and the communication channels. The pin assignment was done during the PCB design and it is then configured in the software.

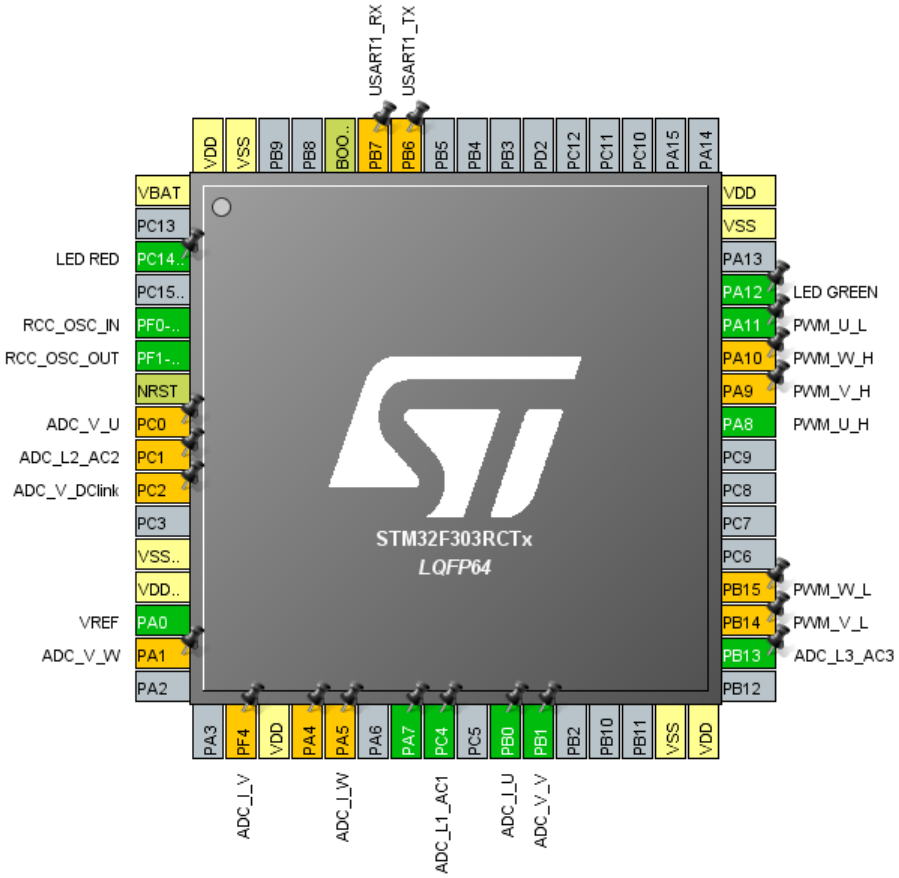

Figure B.1: Pin configuration for STM32f3 controller

B.1 ADC

For implementing the feed-forward control, seven parameters have to be measured by the ADC. The voltage across the stator windings (V'_a, V'_b, V'_c) and the current drawn by the motor (I'_a, I'_b, I'_c)

shown in Figure 2.7, are necessary for the estimation of rotor speed and angle. The DC link voltage V_{dc} measurement is needed for the DC voltage estimation. This controller has four ADCs. The three phase current and voltage have to be measured at the same time instant for the control to be accurate. That is to say, the three voltages are measured simultaneously at one time instance and then the three currents are measured simultaneously in the next time instance. For this reason, 3 ADCs out of the 4 present in the micro-controller are used. Also it is necessary to measure the stator currents and voltages once all the PWMs are triggered and the motor bridge has reached the stable state, in order to get the accurate current and voltage measurements. Therefore, injected conversion is used. In injected conversion the measurement of the parameter is triggered by an event whereas in regular conversion the ADCs are sampled periodically. The completion of the ADC sampling is know as End Of Conversion (EOC), upon which the control algorithm is executed.

In figure B.1, the labels ADC_V_U, ADC_V_V and ADC_V_W refer to the three phase stator voltages and ADC_I_U, ADC_I_V and ADC_I_W represent the three phase stator currents. ADC_V_DClink represents the DC link voltage. ADC_L1_AC1, ADC_L2_AC2, ADC_L3_AC3 are the three phase line voltages.

B.2 PWM

The micro-controller includes a hardware PWM, which implies that a triangular wave also known as the carrier wave of the desired frequency will be generated by the micro- controller. Once the duty cycle is determined by the control algorithm, the state vectors of the inverter switches are determined by the micro-controller by comparing the duty cycle and the carrier wave. In this thesis, the PWM updates the inverter switches at the frequency of 18kHz. As bandwidth of the controller is large, it is sufficient if the duty cycle is updated every alternate PWM cycle which gives the controller more time to implement the control. Therefore the duty cycle is updated at the frequency of 9kHz. From the Figure B.2 it can be seen that the ADC sampling is triggered once the PWM counter reaches the peak. Upon the end of conversion of the ADC, the control algorithm is triggered and the duty cycle is updated to the PWM after one and half PWM cycles. Therefore the time available for the ADC sampling and the computation of the duty cycle is 83.34μ s. For an accurate ADC reading, the next ADC sampling should start after the motor bridge stabilizes and so it begins after half a PWM cycle. In the figure B.1, PWM_U_H, PWM_V_H, PWM_W_H are the PWM signals for the upper switches of the inverter and PWM_U_L, PWM_V_L, PWM_W_L are the PWM signals for the lower switches of the inverter.

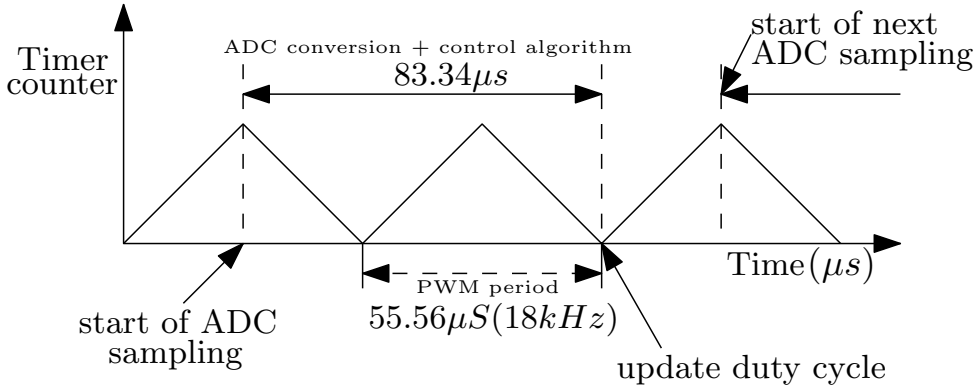

Figure B.2: PWM timing diagram