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System Design of a 2.75-mW Discrete-Time Superheterodyne Receiver for Bluetooth Low Energy

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(Invited Paper)

***Abstract*— This paper introduces a system-level approach to develop the first-ever fully discrete-time (DT) superheterodyne receiver (RX) for Internet-of-Things applications, such as Bluetooth low energy (BLE). It exploits fast switching speed and low internal capacitances of deep-nanoscale CMOS devices to realize a high intermediate-frequency (IF) architecture based on switched-capacitor-based charge-domain bandpass filtering. Power consumption is minimized by aggressively reducing the size of MOS devices and judiciously applying a sampling-rate decimation. The resultant increase in the flicker noise is mitigated by placing the IF frequency beyond the flicker corner frequency. Likewise, the decimation-induced aliasing is mitigated by DT filtering of preceding stages. The BLE RX is fully standard-compliant and achieves a record-low-power consumption of 2.75 mW (including its local oscillator) while delivering the state-of-the-art performance: 6.5-dB noise figure and −19-dBm third-order input intercept point, with a direct antenna connection and thus without the typical external bandpass filters.**

***Index Terms*— Bandpass filter (BPF), Bluetooth low energy (BLE), charge sharing (CS), discrete-time receiver (DT-RX), Internet of Things (IoT), superheterodyne, switched capacitor (SC), ultra-low-power (ULP).**

I. Introduction

DISCRETE-TIME receiver (DT-RX) architectures have been adopted in commercial Bluetooth [1] and 2G cellular [2] radios and are the main alternative for software-defined radio applications, mainly thanks to their versatility [3]. Easy implementation of programmable capacitors in the switched-capacitor (SC) structures, together with an accurate programming of their sampling rates, adds architectural flexibility, while also making it more digitally intensive and reducing sensitivity to process, voltage, and temperature variations [4].

Recent DT-RX advancements in SC-based charge-sharing (CS) complex-domain bandpass filtering have pushed their intermediate-frequency (IF) operation into tens or even hundreds of megahertz range (thus making it superheterodyne) in order to remove all issues associated with flicker noise, time-variant dc offsets, and the second-order nonlinearity [5], [6], and have culminated in a commercial 4G cellular RX [7] featuring record-low-power consumption while maintaining the state-of-the-art performance.

Bluetooth low energy (BLE) [8] is currently the most popular radio standard for Internet-of-Things (IoT) applications. IoT nodes are mainly battery operated but increasingly use energy harvesting to sustain their long-term operation. This places heavy emphasis on ultra-low-power (ULP) aspects of IoT Rx, which is considered the most energy-hungry subsystem. Unfortunately, those versatile high-performance RXs developed for the *cellular* market suffer from relatively high-power dissipation, which naturally prevents their use in the emerging IoT applications that take the ULP dissipation and relatively low performance as their starting point.

In this paper, we introduce a system-level approach to develop such an ULP discrete-time (DT) high-IF superheterodyne RX architecture. It is realized in a deep-nanoscale CMOS technology as amenable to such ULP implementations while maintaining among the best-in-class performance and high level of system integration. To the best of our knowledge, this is the first superheterodyne DT-RX targeting this new emerging market [9]. Besides gain, linearity, noise figure (NF), and analog-to-digital converter (ADC) dynamic range (DR), which are typical figures-of-merit for RX front-ends, the design of a multirate DT-RX for BLE includes additional important requirements related to aliasing due to the successive clock decimations.

This paper is organized as follows. Section II presents a brief review of the state of the art in BLE RX. Section III discusses specifications for a competitive RX. Section IV introduces the RX architecture, tradeoffs, sampling rates and transfer functions (TFs) with antialiasing filtering to mitigate

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TABLE I
SUMMARY OF BLE RX REQUIREMENTS

Requirement	
Sensitivity	-70 dBm
Maximum input signal	-10 dBm
Out-of-band blocking requirements	
30 MHz–2000 MHz	-30 dBm
2003–2399 MHz	-35 dBm
2484–2997 MHz	-35 dBm
3000 MHz–12.75 GHz	-30 dBm
In band interferer requirements	
Co-Channel interference, $C/I_{co-channel}$	21 dB
Adjacent (1 MHz) interference, $C/I_{1\ MHz}$	15 dB
Adjacent (2 MHz) interference, $C/I_{2\ MHz}$	-17 dB
Adjacent ($\geq 3\ MHz$) interference, $C/I_{\geq 3\ MHz}$	-27 dB
Image frequency Interference, C/I_{Image}	-9 dB
Adjacent (1 MHz) interference to in-band image frequency	-15 dB

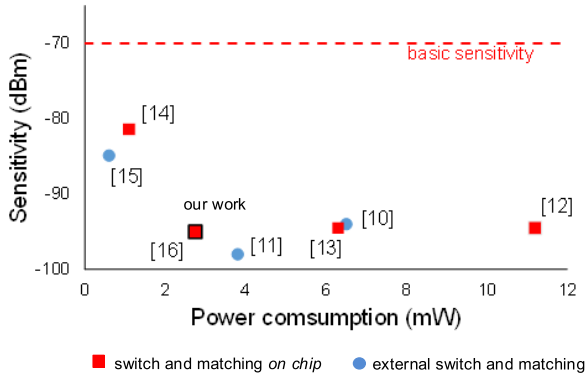

Fig. 1. State of the art in BLE RXs.

the decimation, and details to achieve the BLE requirements. Sections IV-C and V show circuit implementation and measurement results. Finally, Section VI offers conclusions and summary.

II. STATE OF THE ART IN BLUETOOTH LOW-ENERGY RECEIVERS

BLE is an extension of the Bluetooth standard fine-tuned for energy-efficient operation of IoT devices. Its main RX requirements are listed in Table I [8]. Compared with the main Bluetooth standard, linearity is relaxed and a wider (i.e., 2×) channel separation (2 MHz) is defined. For out-of-band (OOB) and in-band linearity tests, the input signal should be 3 dB above the sensitivity level, while the interferers should respect the mask listed in Table I. Typically, BLE demodulators are implemented with at least 15 dB of signal-to-noise ratio (SNR), which results in a budget NF of 29 dB for the complete RX when the basic −70-dBm sensitivity is targeted.

Recently reported BLE RXs easily surpass the main requirements of Table I, reaching sensitivity levels of −80 dBm and well below, as shown in Fig. 1. These works can be classified into two groups: high-performance RXs [10]–[13], and low-power low-performance RXs [14], [15]. Architecturally, they are classified as: low-IF or direct conversion [12], [14], [15], and sliding-IF [10], [11], [13]. So far, they are all analog-intensive and operate in the continuous-time domain. Fig. 1 recognizes (with square markers) highly integrated solutions that manage to avoid external RF components, thus making it more attractive from the cost and board area standpoint. However, they are still *either* of low performance [14] or high power [12], [13].

We have recently introduced [9], [16] the first-ever DT BLE RX that features record-low-power consumption while maintaining high RF performance. The RX is fully integrated at the BLE transceiver level and requires no external RF components, thus allowing for a direct antenna connection. The new transceiver comprises an all-digital phase-locked loop (ADPLL) that further enables operation in open loop to reduce power consumption during reception/transmission. The ULP circuit design strategies adopted in the RX, the internal *soft switch*, which connects RX and transmitter (TX) to the same antenna, as well as the ADPLL are explained in detail in [16].

The RX system-level design focusing on its OOB linearity aspects and its clock decimation strategies are revealed in detail in Sections III and IV.

III. SYSTEM-LEVEL SPECIFICATIONS

We shall start by identifying system-level specification figures that attain the most up-to-date state-of-the-art BLE performance. From the BLE references identified earlier [10]–[13], we define a sensitivity of −93 dBm, and the third-order input intercept point (IIP3) of −19 dBm. To achieve a competitive power consumption for such high-performance RXs, we aim at 2 mW, without the local oscillator (LO), which shall consume <1 mW.

NF is calculated as $\text{NF} = S - KTB - \text{SNR}_{\text{out}}$, all in dB scale, where S is the target sensitivity, KTB is the noise floor for the $B = 1$-MHz BLE channel (≈ -114 dBm), and SNR_{out} is the required SNR of the detector. Consequently, 6 dB of NF is required for a sensitivity of −93 dBm and SNR_{out} of 15 dB.

With a maximum input of −10 dBm and a sensitivity of −93 dBm, a DR of 83 dB is required. To save power in the ADC design, an automatic gain control (AGC) is implemented and a 9-b, 20-MS/s successive approximation register (SAR) ADC is selected. The ADC with 55 dB of DR can absorb part of the RX's DR while the AGC complements the RX total gain. Considering a maximum signal level of 4 dBm (including a margin of 2 dB) at the chosen ADC input, a minimum gain of 12 dB is required for the input signal of −10 dBm. Quantization noise of −51 dBm (= 4 dBm − 55 dB) with an SNR of 15 dB and a margin of 6 dB establishes the required maximum gain of 63 dB (= −51 dBm + 15 dB + 6 dB − sensitivity).

In-band interferers presented in Table I need to be attenuated as not to saturate the ADC input, as well as to avoid aliasing. Additional filtering can easily be added in the digital domain later down the stream. An analog implementation of the baseband (BB) (or IF) filter to completely remove the interferers would require a sixth-order filter solution, demanding high power and complexity for IoT applications, as observed in [4]. Assuming only the ADC saturation requirement and

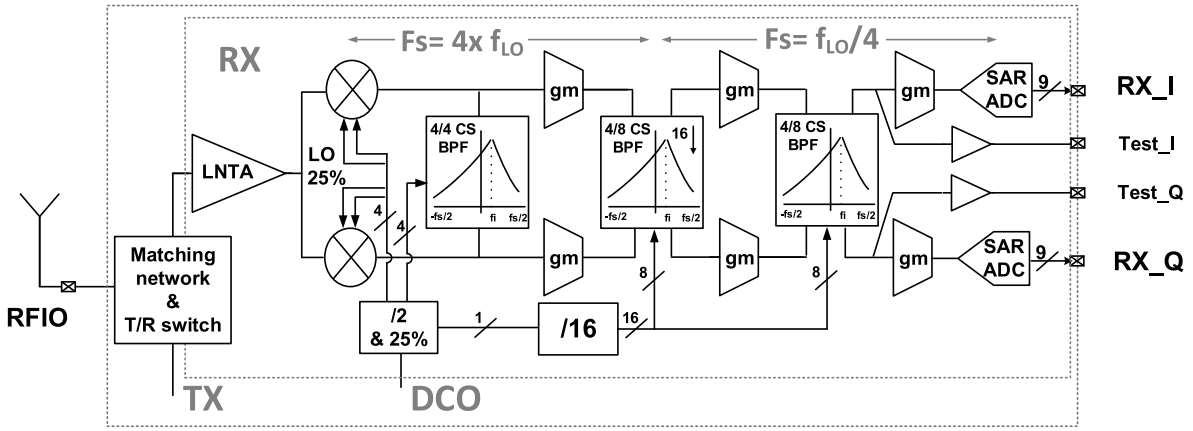

Fig. 2. Architecture of the proposed DT BLE RX.

the in-band linearity case with -70 dBm $+ 3$ dB sensitivity, 46 dB of AGC gain will require an attenuation of 4 dB ($= -67$ dBm$+46$ dB$+27$ dB-2 dBm) of adjacent interferers ($\geq$ 3 MHz), which is reasonably less challenging. Aliasing requirements for ADC are much tougher, though. An attenuation of interferers at $f_{s,\mathrm{ADC}} + f_{\mathrm{IF}}$ and $-f_{s,\mathrm{ADC}} - f_{\mathrm{IF}}$ needs to be considered for an IF digitization. At these frequencies, the BLE standard (Table I) specifies an attenuation of 48 dB [$=$ 21 dB $-$ ($-$27 dB)] from the cochannel and adjacent-channel requirements.

IF selection in a superheterodyne RX plays an important role in two main aspects: 1) conventional zero-IF/low-IF related issues that are getting worse in nanoscale CMOS and 2) ADC sampling-rate selection. The first aspect suggests increasing the IF frequency in order to escape from time-variant dc offsets, 1/f (i.e., flicker) noise, in-band LO leakage, and the second-order nonlinearity [7], [17]. On the other hand, increasing the ADC sampling rate increases its power consumption, but the recent advances in SAR-ADC architectures and circuit techniques make its power consumption of tens of hundreds of μW a small fraction of the RX's power. Size of passive components is another aspect to be considered in the increase of IF frequency, since it reduces capacitor and resistor area in the implementation of blocking capacitors, biasing resistors, and passive filters. Unfortunately, the quality factor (Q) of the bandpass DT filters adopted here is almost constant, and so the selectivity of the filter decreases at higher IF frequencies, which goes against the ADC sampling-rate increase. With all these aspects considered, 5 MHz was tentatively selected to keep a safe separation from flicker-noise corner, allowing for the adoption of a 9-b, 20-MS/s dual SAR ADC, with an estimated power consumption of 250 μW. The IF frequency is reviewed in Section IV-B once the complete architecture is detailed.

IV. Discrete-Time Receiver Architecture

The high-IF superheterodyne RX is composed of two DT RX sections that operate at vastly different sampling rates, as shown in Fig. 2: the *full-rate sampling* section, with the sampling rate of $f_s = 4f_{\mathrm{LO}}$, where f_{LO} is the LO frequency in the vicinity of the desired RF signal, and the *decimated-sampling* section that operates at a reduced clock of $f_{\mathrm{LO}}/4$ for substantial power savings.

Typically, the early (i.e., front-end) section of an RX chain functions to provide adequate antenna impedance matching with high gain and low NF. In our design, due to the avoidance of the off-chip band-select filter and the fully DT nature of the signal path, the full-rate sampling section must additionally provide the OOB filtering; otherwise, residual energy of the far-out interferers/blockers would potentially alias to the frequencies of interest at the decimation stage. Consequently, the full-rate front-end section must provide an effective filtering as an antialiasing protection to the following decimated-rate section.

The *decimated-sampling section* is responsible for the gain and in-band filtering, consequently, protecting the ADC from saturation in the presence of adjacent interferers listed in Table I.

A. Full-Rate Sampling Section

The front-end RX section is presented in detail in Fig. 3. It is composed of a narrowband low-noise transconductance amplifier (LNTA), followed by a 25% duty-cycle sampling mixer, and a 4/4 CS bandpass filter (BPF), introduced in [5] for high-performance cellular applications and adapted here for low power. The RX front-end is connected to the RF input pad and TX through an internal matching network that enables half-duplex operation of the BLE transceiver.

Both the sampling mixer and CS BPF operate at $f_s = 4f_{\mathrm{LO}}$ (where f_{LO} = $\sim$2.45 GHz is close to the Bluetooth band) to avoid aliasing with OOB blockers. The first folding appears at $3f_{\mathrm{LO}}$, or $\sim$7.35 GHz. The process of sampling at $4f_{\mathrm{LO}}$ in the mixer includes both folding due to the sampling and due to the mixing with f_{LO}, as can be observed in Fig. 4. Both issues can be solved by a combination of LNTA's LC-tank filtering, window integrated sampling, and 4/4 CS BPF.

In order to be compliant with the OOB blocking mask, the interferers in Table I at $3f_{\mathrm{LO}}, 4f_{\mathrm{LO}}$, and $5f_{\mathrm{LO}}$ should be attenuated according to

$$\mathrm{Att} = P_{\mathrm{interf}} - (S + \ 3\mathrm{dB} - \mathrm{SNR} - \mathrm{margin}) \qquad (1)$$

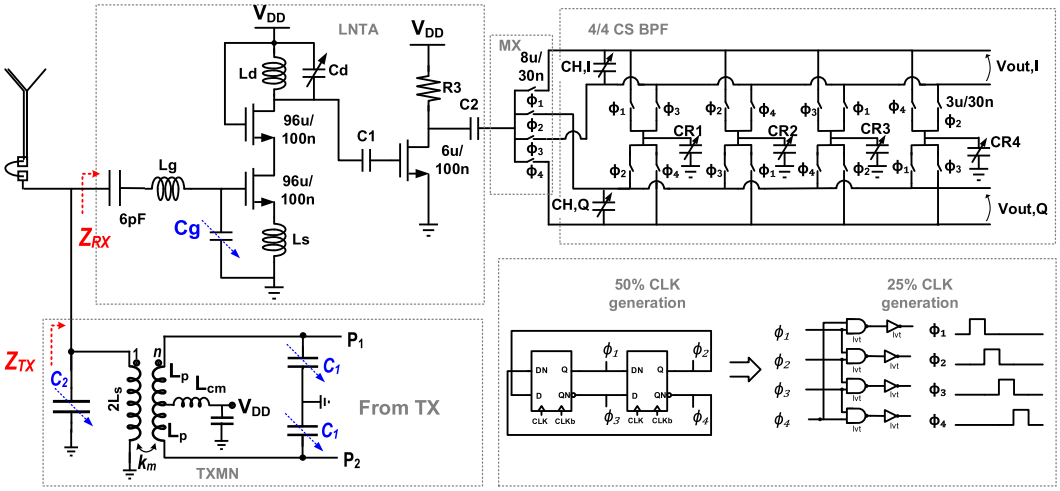

Fig. 3. Schematic of the full-rate-sampling front-end section.

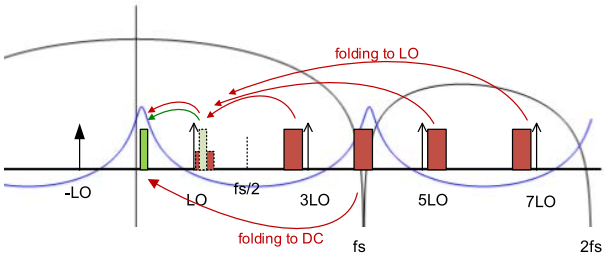

Fig. 4. Aliasing in the $4f_{\mathrm{LO}}$ sampling.

where P_{interf} is the interferer power defined in Table I, S is the required sensitivity, and SNR is the value required for demodulation, considered 15 dB in this analysis.

We start an analysis of the full-rate sampling section with the passive mixer translation property. It was recently shown in [17] and [18] that a BB output load of a 25% duty-cycle current-driven passive mixer is frequency translated back at the input to f_{LO}, $2f_{\mathrm{LO}}$, $3f_{\mathrm{LO}}$, ..., according to

$$\begin{aligned} Z_{\mathrm{in}}(\omega) \approx\ & R_{\mathrm{sw}} + \frac{1}{4}Z_{BB}(\omega) \\ & + \frac{2}{\pi^2}[Z_{BB}(\omega-\omega_{\mathrm{LO}}) + Z_{BB}(\omega+\omega_{\mathrm{LO}})] \\ & + \frac{1}{\pi^2}[Z_{BB}(\omega-2\omega_{\mathrm{LO}}) + Z_{BB}(\omega+2\omega_{\mathrm{LO}})] \\ & + \frac{2}{9\pi^2}[Z_{BB}(\omega-3\omega_{\mathrm{LO}}) + Z_{BB}(\omega+3\omega_{\mathrm{LO}})] \\ & + \cdots \end{aligned} \tag{2}$$

where Z_{in} is the impedance seen at the mixer's single-ended input, R_{sw} is the mixer's switch resistance, and Z_{BB} is the impedance at the mixer output, which is actually the IF impedance in our case. Thanks to the differential topology of the sampling mixer, the even multiples of f_{LO} are not translated back to the IF; hence, they are not considered further in our analysis.

The output load of the mixer is provided by the 4/4 CS BPF. According to (2), the filter TF is translated to the mixer, thus directly attenuating the OOB blockers. The 4/4 CS BPF

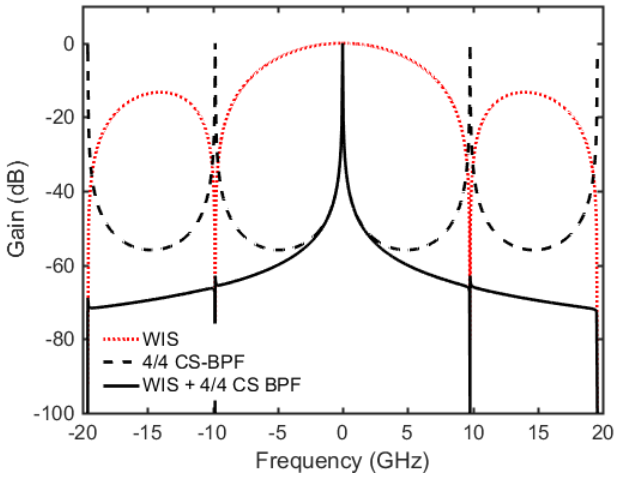

Fig. 5. TF of 4/4 CS BPF showing pulse shaping effect.

implements a complex-domain infinite impulse response filter with z-domain TF given by [19]

$$H_{4/4\ \mathrm{CS-BPF}}(z) = \frac{V_{\mathrm{out}}(z)}{Q_{\mathrm{in}}(z)} = \frac{1/(C_H + C_R)}{1 - [\alpha + j(1-\alpha)]z^{-1}} \tag{3}$$

where C_R is the rotating capacitor, C_H is the history capacitor, and $\alpha = C_H/(C_H + C_R)$.

The ideal TF of CS BPF is presented in Fig. 5. Due to the sampling period ($T_s = 1/f_s$), the repetition peaks of the DT TF can be observed (as the black dashed curve) at the multiples of ~9.8 GHz. The sampling of integrated current with an ideal square pulse originates a pulse shaping effect characterized by a window integration sampling (WIS) function (4) [20], shown in red dotted curve. Since the 4/4 CS BPF operates with a 25% duty-cycle clock and $\Delta t = 1/4f_s$, the WIS nulls appear at the same repetition points of the filter's TF, except for the IF frequency ($f_{\mathrm{IF}} = 5$ MHz) difference. Cascaded effect produces an attenuation greater than 60 dB at the repetition points, only due to the combination of sampling mixer

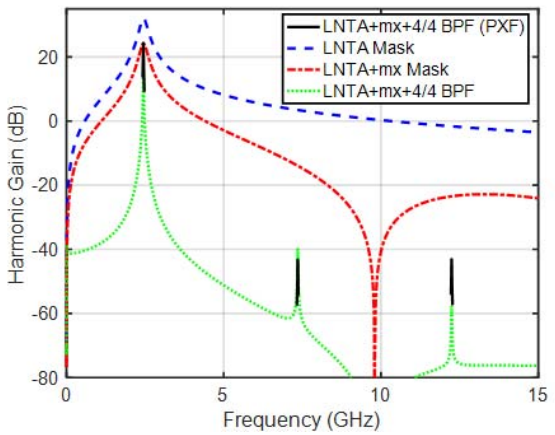

Fig. 6. TF of the full-rate section.

and CS BPF [4]

$$H_{\mathrm{WIS}}(f) = \frac{\sin(\pi f \Delta t)}{\pi f \Delta t} \tag{4}$$

where $\Delta t = 1/4f_{\mathrm{LO}}$ is the sampling pulse created by the 25% duty-cycle clock period, as previously shown in Fig. 3.

The LNTA selectivity is the last effect to be included in this analysis and it is mainly due to the second-order RLC tank load impedance (L_d and C_d in Fig. 3) that can be modeled by

$$|Z_T(\omega)|^2 = \frac{L^2\omega^2}{(1 - LC\omega^2)^2 + \frac{L^2\omega^2}{R^2}} \tag{5}$$

where $\omega = 2\pi f$.

If the resonance frequency and quality factor Q of the tank are given by $\omega_{\mathrm{LO}} = 1/\sqrt{LC}$ and $Q = R/L\omega_{\mathrm{LO}}$, normalized LNTA gain is given from (5) as

$$|G_{\mathrm{LNTA}}(\omega)|^2 = \frac{|Z_T(\omega)|^2}{R^2} = \frac{\frac{\omega^2}{\omega_{\mathrm{LO}}^2 Q^2}}{\left(1 - \frac{\omega^2}{\omega_{\mathrm{LO}}^2}\right)^2 + \frac{\omega^2}{\omega_{\mathrm{LO}}^2 Q^2}}. \tag{6}$$

At $\omega = 3\omega_{\mathrm{LO}}$, the expected attenuation ($\mathrm{Att} = 1/G_{LNTA}$) due to the LNTA filtering is given by

$$\mathrm{Att}^2 = \frac{(1-9)^2 + 9/Q^2}{9/Q^2} \tag{7}$$

which corresponds to an attenuation of 28.5 dB for an LNTA with $Q = 10$. The combined voltage gain of the full-rate section is given by the effective LNTA transconductance (gm_{LNTA}) and the impedance Z_{in} seen at the mixer input

$$A_V = \frac{V_{\mathrm{out},I}}{V_{\mathrm{in}}} = gm_{\mathrm{LNTA}} \cdot Z_{\mathrm{in}} \tag{8}$$

where V_{in} is a voltage at the antenna input. Fig. 6 presents the TF of LNTA mask (6), and impedance translation (2) of the 4/4 CS BPF (3). It shows the expected conversion gain from the harmonics of f_{LO} with an attenuation of more than 60 dB at $3f_{\mathrm{LO}}$ and $5f_{\mathrm{LO}}$, which satisfies the required blocker attenuation of $\approx$57 dB $= -30$ dBm $-$ (-67 dBm $-$ 15 dB $-$ 5 dB) given by (1). Cascaded results presented in green dotted curve are compared with the schematic-based PSS/PXF analysis using Cadence SpectreRF$^{\mathrm{TM}}$, thus verifying the mathematical model.

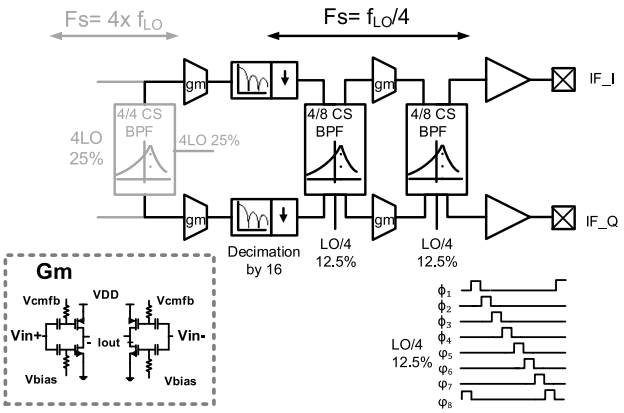

Fig. 7. Block diagram of the decimated-sampling back-end section.

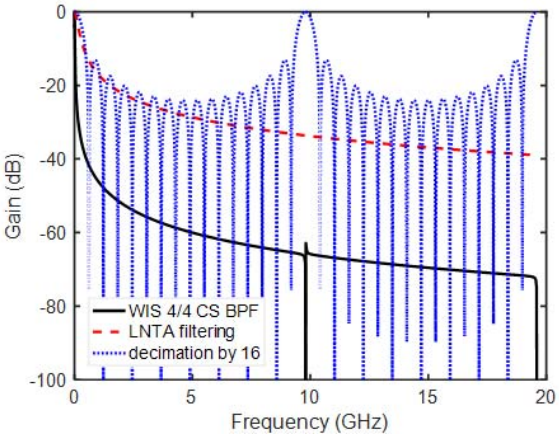

Fig. 8. FIR filter realized with the clock decimation by 16.

B. IF Filtering at Decimated Clock

The second (i.e., back-end) section, redrawn in Fig. 7 with more details, is also based on DT BPFs but they operate at a much lower (i.e., $\div$16) sampling rate and thus offer a much better selectivity. Transconductance (i.e., I/V) gain is provided by differential inverter-based transconductor (Gm) cells, which condition the signal for current/charge-domain processing in the passive CS filters. To ensure such current-mode behavior, the input impedance of the filters needs to be at least 3$\times$ lower than the output impedance of the Gm cells.

Right at the beginning of the IF processing strip ($f_{\mathrm{IF}} = 5$ MHz), there is a clock decimation by 16 in order to substantially reduce power consumption. This decimation is realized by integrating 16 input samples on the rotating capacitor using the LO clock that is divided by 16. This creates a "self" antialiasing sinc-type filter with a z-domain TF presented in (9). It is called *sinc-type*, because its TF is similar to a sinc TF as can be observed in Fig. 8 [3].

$$H(z) = \frac{1 - z^{-16}}{1 - z^{-1}} = \left|\frac{\sin(\pi f\ 16/f_s)}{\sin(\pi f/f_s)}\right| \tag{9}$$

where f_s is the sampling rate of the filter.

The above $\div$16 sampling-rate decimation can cause aliasing. To mitigate folding of large OOB interferers into the

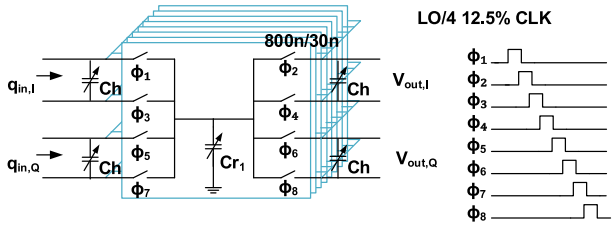

Fig. 9. Architecture and operation of 4/8 CS BPF.

weak received signal, the RX's front-end should substantially attenuate such interferers via filtering. Here, we exploit the sinc-type antialiasing filtering naturally inherent in DT CS filters. The worst case interferer of $P_{\text{interf}} = -30$ dBm lies $f_s = 4f_{\text{LO}}/16 = 612.5$ MHz away from the signal at the adjusted BLE sensitivity level of $S = -67$ dBm. This results in a blocking attenuation requirement of 57 dB, as derived from (1). Stopband loss, $H_B(kf_s)$, of the FIR filter across a bandwidth B at the k^{th} filter null is given by [21]

$$H_B(kf_s) \approx \frac{B}{kf_s}. \tag{10}$$

For $f_s = 4f_{\text{LO}}/16 = 612.5$ MHz, IF of 5 MHz, and a signal of 1 MHz, we can estimate a bandwidth B of 20 MHz (with some margin) that results in an attenuation of $20\log 10(B/kf_s) \approx -30$ dB for the first null. Attenuation provided by the LNTA can be estimated at 13 dB with $f = f_{\text{LO}} + 612.5$ MHz in (6).

Fig. 8 shows the TFs of the 4/4 CS BPF with WIS effect, LNTA filter, and decimation-by-16 sinc-type filter. The LNTA filter represents the filtering effect of the LNTA after frequency translation by the mixer. The combined effects of the LNTA, decimation by 16, and 4/4 CS BPF offer a very good antialiasing protection of around 83 dB = 13dB + 30dB + 40dB.

The second and the third filter stages presented in Fig. 7 are also complex-domain BPFs based on CS principle but in a somewhat different architecture. They provide increased selectivity with a theoretical image attenuation per filter that is 5 dB better.

The 4/8 CS BPF presented in Fig. 9 has a structure similar to the 4/4 CS filter previously shown in Fig. 3. The filter is composed by four history capacitors (C_H) that share charge with eight rotating capacitors (C_R) throughout eight different phases. Unlike in the 4/4 filter, the output (voltage) and input (current/charge) are physically separated here. Just like in the previous case, the sampling operation of the input current creates a similar WIS filtering characteristic.

The 4/8 CS BPF TF in z-domain is [7]

$$H(z) = \frac{V(z)}{Q(z)} = \frac{k}{(1-\alpha z^{-1})^2 - j[(1-\alpha)z^{-1}]^2} \tag{11}$$

$$k = \frac{1}{C_H + C_R}, \quad \alpha = \frac{C_H}{C_H + C_R}. \tag{12}$$

The cascaded effect produced by the LNTA, WIS, 4/4 CS BPF, decimation by 16, and the two 4/8 CS BPFs with WIS pulse shaping is presented in Fig. 10. A zoomed-in version of the cascaded filters is shown in Fig. 11 and compared with the normalized cascaded TF obtained through

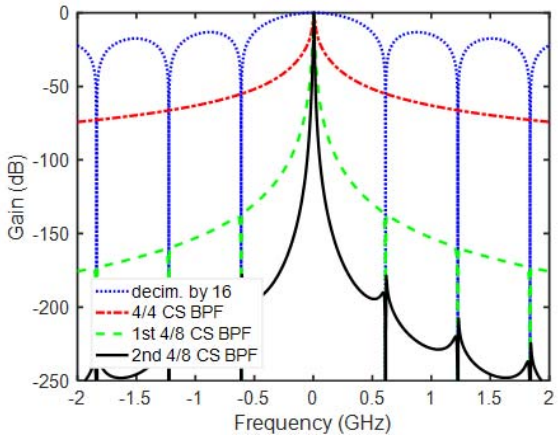

Fig. 10. Cascaded TFs of the RX.

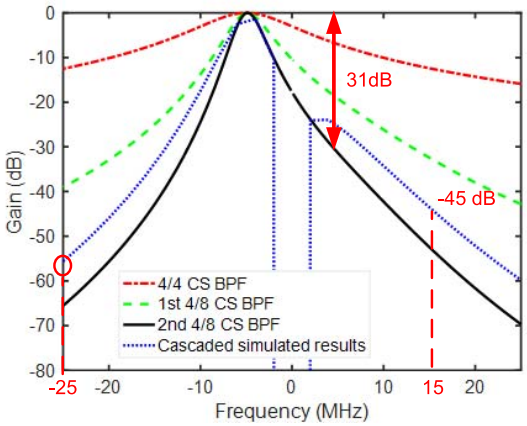

Fig. 11. Zoomed-in cascaded TFs of the RX.

simulations using PSS/PAC analysis (SpectreRF). A theoretical image attenuation of 31 dB is obtained with the TF model.

In-band interferer requirements presented in Table I call for 30 dB of image rejection due to the cochannel requirement of 21 dB and an image interferer protection of −9 dB. However, this is a requirement of the complete RX and should include BB processing, which is quite straightforward to do.

Since the presented model does not consider the Q-factor reduction of the filter due to the finite output impedance of the LNTA and transconductors as well as the nonideal square pulse implementation, an image attenuation of about 26 dB is observed in the simulations in Fig. 11. Here, there is a tradeoff in the input impedance choice, since the reduction of the input impedance of the filters to improve the Q-factor requires better and larger switches, which are power hungry and thus not compatible with the power efficiency philosophy of IoT solutions. Nevertheless, image rejection can still be easily achieved in the complex-domain signal processing in the digital domain provided that the RX quadrature imbalance is not significant.

At this point, it is necessary to evaluate the aliasing effect caused by an I/Q SAR ADC of 20 MS/s. A complex-domain demodulation following the ADC exhibits aliasing at $f_{s,\text{ADC}} + f_{\text{IF}}$ and $-f_{s,\text{ADC}} - f_{\text{IF}}$, which correspond to 15 and −25 MHz

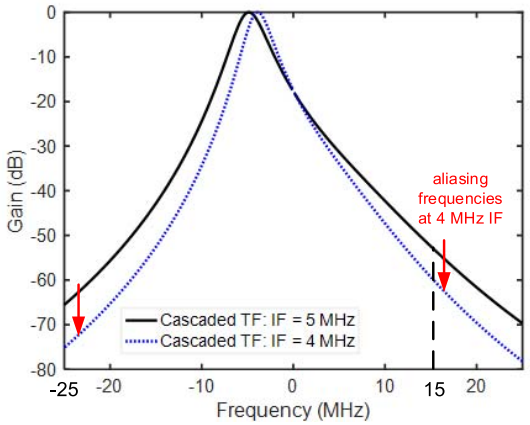

Fig. 12. Comparison of 4- and 5-MHz IF cascaded TFs of the RX.

in Fig. 11. At these frequencies, a requirement of 48 dB is presented, as observed in Section III.

The simulation results in Fig. 11 show a rejection of only 45 dB at 15 MHz, which would require an increase in ADC sampling rate, the use of an additional antialiasing filter, or even the IF reduction in order to achieve the blocking requirement at that frequency. With an IF reduction to 4 MHz, also due to the change of aliasing points to 16 and −24 MHz, an improvement of around 10 dB is expected as can be observed in the TF comparison presented in Fig. 12.

C. Circuit Implementation

The full-rate section of Fig. 3 is implemented with an LNTA composed of two stages: a common-source cascode low-noise amplifier (LNA) and a transconductor amplifier (TA). Both stages operate in moderate inversion ($\mathrm{gm}/I_d = 18$ and 12 V^{-1}) in order to reduce power consumption with a current biasing of only 400 and 100 μA, respectively. The LNTA (i.e., LNA + TA) is designed with 31 dB of gain when loaded by a 1-kΩ input impedance of the CS BPF filter, which is frequency translated to the RF mixer input by (2). The passive sampling mixer has a reduced conversion gain of $\sqrt{2}/\pi$, which corresponds to −6.9 dB, resulting in 24 dB of total gain for this section.

Both the rotating capacitor C_R and history capacitor C_H are 5-b binary programmable, from 22 to 150 fF, and from 2×8.5 to 2×18.7 pF, respectively. The required input impedance of 1 kΩ for the 4/4 CS BPF is set by $1/(C_R f_s)$, where C_R is programmed to 100 fF and $f_s = 9.8$ GHz. The center frequency of 5 MHz is adjusted by programming C_H according to

$$f_c = \frac{f_s}{2\pi} \arctan\left(\frac{C_R}{C_H}\right). \tag{13}$$

Each Gm cell is composed of parallel unit-controlled "inverterlike" stages, shown in Fig. 7, allowing four possible gains of 1.7, 7.1, 10.5, and 12.5 dB. Devices are sized in moderate inversion to reduce power consumption, but with $L = 200$ nm to achieve a higher output impedance of 15 kΩ. Blocking capacitors and biasing resistors at the input and output of the Gm cells define a frequency corner of 1 MHz, thus with a minimum channel/band attenuation and without increasing too much of the capacitor and resistors size. Gm cells are highly linear with a simulated IIP3 of 40 dBm.

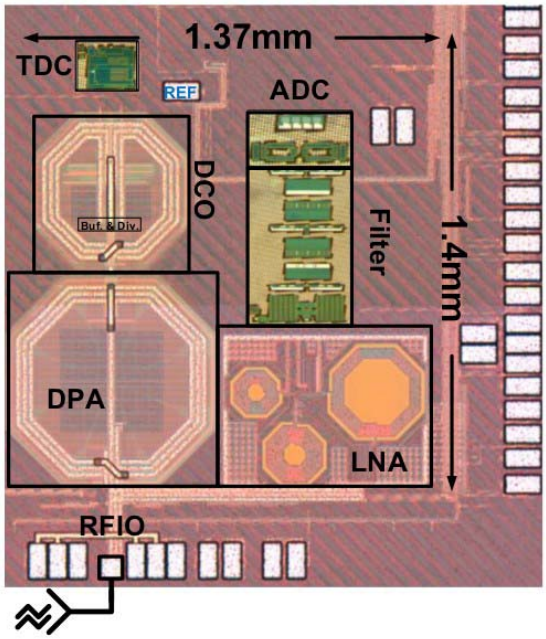

Fig. 13. Chip micrograph of the complete transceiver [9].

The 4/8 CS BPF stages contain C_R and C_H capacitors that are also programmable using five binary bits. The filters have an input impedance of 3.3 kΩ, which is much smaller than the Gm's output impedance in order to improve the filter's Q-factor.

The 25% and 12.5% duty-cycle clock phases needed for the DT-RX operation are generated in several steps using customized CMOS logic with low-V_t devices. A differential input clock of 4.9 GHz, coming from a digitally controlled oscillator (DCO), is divided by two to generate the in-phase (I) and quadrature (Q) LO signals, which are then combined to generate 25% duty-cycle clocks (see Fig. 3). The 12.5 % duty-cycle clocks are generated using an 8-b synchronous standard-cell counter [4].

The TX and RX are interconnected on-chip by a matching network introduced in [9] that implements a "soft" switch in transmit and receive modes (Fig. 3). During reception, the TX's final stage connected to P_1 and P_2 is turned OFF and its impedance (Z_{TX}) peak seen at the RX input is tuned to the RX's center frequency through programmable capacitors C_1 and C_2 ($\omega_{LO}^2 \approx 1/(L_p C_1 + L_s C_2)$. The impedance at the resonant frequency ($\sim f_{LO}$) has a maximum value of 250 kΩ, causing a penalty of less than 1 dB in the RX NF. In the transmit mode, capacitance C_g is set to resonate at a higher frequency. The resulting capacitive impedance seen in parallel with the transmit output gives a minimum penalty of $\sim 3\%$ in the transmit drain efficiency [9].

V. Experimental Results

The DT RX proposed in this paper was realized together with an all-digital PLL (ADPLL)-based TX [9] in 28-nm TSMC bulk CMOS process technology. The transceiver area is 1.4 mm^2, as shown in Fig. 13. The complete RX consumes

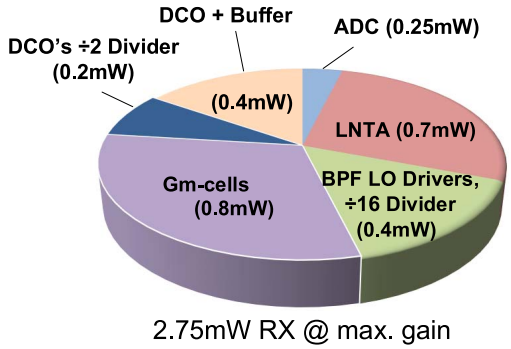

Fig. 14. Power breakdown of RX at high gain.

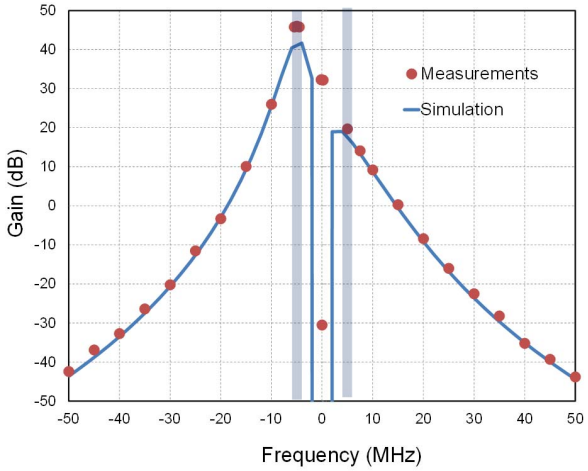

Fig. 15. Measured and simulated RX TF at IF = 5 MHz.

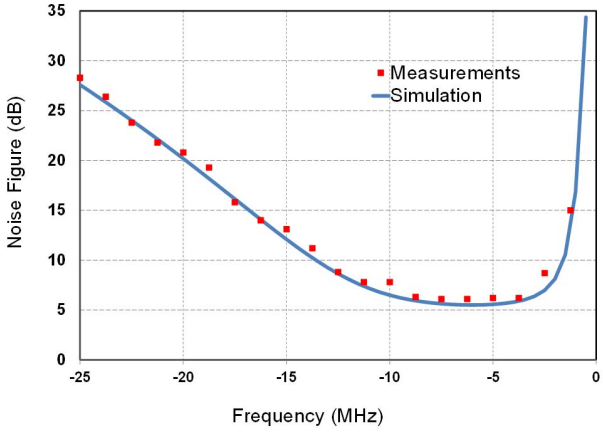

Fig. 16. Measured and simulated NF.

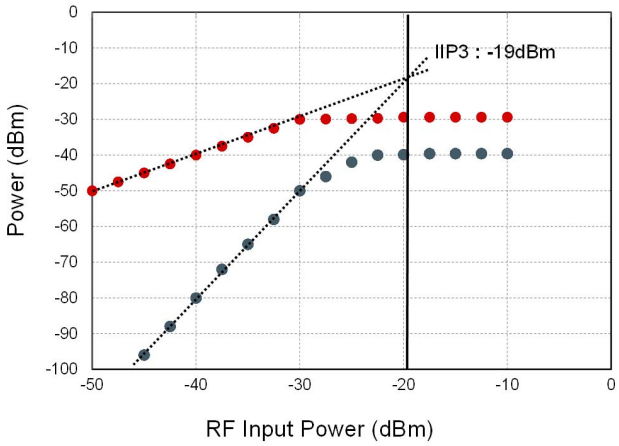

Fig. 17. Measured IIP3.

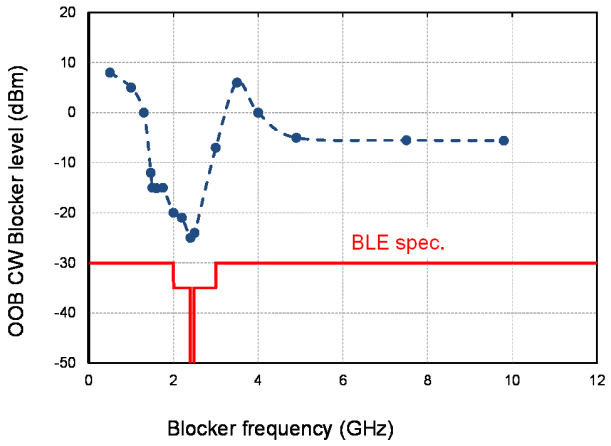

Fig. 18. Measured OOB blocker interference.

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH BLE STATE-OF-THE-ART RXS

	This Work	[11]	[12]	[13]
CMOS node	28 nm	90nm	55nm	40nm
Data rate & modulation	1-Mbps GFSK	1-Mbps GFSK	1-Mbps GFSK	1-Mbps GFSK
Noise figure (dB)	6.5	6	N/A	6.5
Sensitivity (dBm)	-95	-98	-94.5	-94.5
IIP3 (dBm)	-19	-19	N/A	N/A
On-chip T/R Switch	Yes	No	Yes	Yes
Supply voltage (V)	1	1.2	0.9-3.3	1.1
Integrated transceiver	Yes	Yes	Yes	Yes
Power dissipation (mW)	2.75	3.3	11.2	6.3
Figure of Merit (dB)∗	-121	-123	-114	-116.5

∗FoM = RxSensitivity + $10\log_{10}(Idc@1V)$

2.75 mW at 5-MHz IF and at the high measured gain of 46 dB. The RX's power breakdown, which includes the DCO and its buffer, is shown in Fig. 14. The measured TF is shown in Fig. 15. It agrees well with simulations and indicates the image attenuation of 26 dB. The Gm blocking capacitors and biasing resistors define the 1-MHz corner, which can be observed in Fig. 15. Fig. 16 shows simulated and measured NF of 6.5 dB at the 5-MHz IF. Fig. 17 shows the measured IIP3 of −19 dBm.

Effectiveness of the proposed OOB filtering strategy, which comprises the LNTA, mixer, and 4/4 CS BPF, and which results in the elimination of external filters, can be verified in Fig. 18. The dotted curve shows that the RX can tolerate high-power blockers with good margin, while satisfying the required packet error rate of 30.8%. In this measurement,

the desired BLE signal is fixed at channel 12 with an input power of −67 dBm while the amplitude and frequency of blockers are swept [16]. The DT sampling frequencies at $4f_{LO}/16 = 612.5$-MHz offset from ∼2.45 GHz and at $4f_{LO} = 9.8$ GHz are verified with at least 10 dB of margin in the blocking protection.

Table II presents the performance summary of the implemented DT-RX and compares it with recently disclosed high-performance RXs with similar sensitivity. Comparison shows the lowest power consumption, only comparable to [11], which needs an external T/R switch and a matching network.

VI. Conclusion

This paper presented a top–down design of the first DT RX for BLE. It starts with the BLE RX system specifications and translates them to the architecture of charge-domain DT processing, which has been applied successfully to high-performance commercial cellular RXs. With the new constraint of ultimate reduction of power consumption, the transistor sizes are maximally reduced. The resulting flicker noise, which extends to several megahertz, is mitigated by setting the IF at 5 MHz. The design is fabricated in TSMC 28-nm bulk CMOS with an active area of 0.7×1.4 mm^2. It attains the record-low-power consumption of 2.75 mW while maintaining the state-of-the-art performance, with no external matching networks or external TX/RX switch required. The IIP3 of −19 dBm and the NF of 6.5 dB with −95 dBm of sensitivity are competitive with the best reported BLE continuous-time RXs.

References

[1] R. B. Staszewski *et al.*, "All-digital TX frequency synthesizer and discrete-time receiver for Bluetooth radio in 130-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2278–2291, Dec. 2004.

[2] K. Muhammad *et al.*, "The first fully integrated quad-band GSM/GPRS receiver in a 90-nm digital CMOS process," *IEEE J. Solid-State Circuits*, vol. 41, no. 8, pp. 1772–1783, Aug. 2006.

[3] R. Bagheri *et al.*, "An 800-MHz–6-GHz software-defined wireless receiver in 90-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2860–2876, Dec. 2006.

[4] M. Tohidian, I. Madadi, and R. B. Staszewski, "Analysis and design of a high-order discrete-time passive IIR low-pass filter," *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2575–2587, Nov. 2014.

[5] I. Madadi, M. Tohidian, and R. B. Staszewski, "A 65 nm CMOS high-IF superheterodyne receiver with a high-Q complex BPF," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Apr. 2013, pp. 323–326.

[6] M. Tohidian, I. Madadi, and R. B. Staszewski, "A fully integrated highly reconfigurable discrete-time superheterodyne receiver," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, Sep. 2014, pp. 1–3.

[7] I. Madadi, M. Tohidian, K. Cornelissens, P. Vandenameele, and R. B. Staszewski, "A high IIP2 SAW-less superheterodyne receiver with multistage harmonic rejection," *IEEE J. Solid-State Circuits*, vol. 51, no. 2, pp. 332–347, Feb. 2016.

[8] Bluetooth SIG. *Specification of the Bluetooth System V4.2*. accessed on Dec. 2, 2014. [Online]. Available: http//www.Bluetooth.org

[9] F.-W. Kuo *et al.*, "A Bluetooth low-energy (BLE) transceiver with TX/RX switchable on-chip matching network, 2.75 mW high-IF discrete-time receiver, and 3.6 mW all-digital transmitter," in *Proc. IEEE VLSI Circuits Symp.*, Apr. 2016, pp. 1–2.

[10] A. C. W. Wong *et al.*, "A 1 V 5 mA multimode IEEE 802.15.6/Bluetooth low-energy WBAN transceiver for biotelemetry applications," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, Apr. 2012, pp. 300–302.

[11] Y.-H. Liu, A. Ba, J. H. C. van den Heuvel, K. Philips, G. Dolmans, and H. de Groot, "A 1.2 nJ/bit 2.4 GHz receiver with a sliding-IF phase-to-digital converter for wireless personal/body area networks," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, Sep. 2014, pp. 166–167.

[12] J. Prummel *et al.*, "A 10 mW Bluetooth low-energy transceiver with on-chip matching," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, Sep. 2015, pp. 1–3.

[13] T. Sano *et al.*, "A 6.3 mW BLE transceiver embedded RX image-rejection filter and TX harmonic-suppression filter reusing on-chip matching network," *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, Sep. 2015, pp. 1–3.

[14] J. Masuch, and M. Delgado-Restituto, "A 1.1-mW-RX −81.4 −dBm sensitivity CMOS transceiver for Bluetooth low energy," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 8, pp. 1660–1673, Apr. 2013.

[15] A. Selvakumar, M. Zargham, and A. Liscidini, "A 600 μW Bluetooth low-energy front-end receiver in 0.13 μm CMOS technology," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, Sep. 2015, pp. 1–3.

[16] F.-W. Kuo *et al.*, "A Bluetooth low-energy (BLE) transceiver with 3.7 mW all-digital transmitter, 2.75 mW high-IF discrete-time receiver, and TX/RX switchable on-chip matching network," *IEEE J. Solid-State Circuits*, vol. 52, no. 4, pp. 1–19, Apr. 2017.

[17] A. Mirzaei, H. Darabi, and D. Murphy, "A low-power process-scalable super-heterodyne receiver with integrated high-Q filters," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2920–2932, Feb. 2011.

[18] A. Mirzaei, H. Darabi, J. C. Leete, and Y. Chang, "Analysis and optimization of direct-conversion receivers with 25% duty-cycle current-driven passive mixers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 9, pp. 2353–2366, Sep. 2010.

[19] I. Madadi, M. Tohidian, and R. B. Staszewski, "Analysis and design of I/Q charge-sharing band-pass-filter for superheterodyne receivers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 8, pp. 2114–2121, Aug. 2015.

[20] G. Xu and J. Yuan, "Performance analysis of general charge sampling," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 52, no. 2, pp. 107–111, Feb. 2005.

[21] A. A. Abidi, "The path to the software-defined radio receiver," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 954–966, May 2007.

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