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# Oxygen-plasma-based digital etching for GaN/AlGaN high electron mobility transistors

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## Abstract

Digital etching is an effective method to lower dry etch damages in AlGaN/GaN HEMTs. This work systematically investigated O<sub>2</sub>-plasma-based digital etching of AlGaN and p-GaN. AlN layers were used as the etch stop layers in the AlGaN etch. Important process aspects such as the use of the AlN layers, the RF power, the oxygen flow rate, the oxidation time and the resulting roughness were studied. These are technically relevant to obtain controllable, uniform etch surfaces with low surface damages for better HEMT performance.

## 1. Introduction

AlGaN/GaN high electron mobility transistors (HEMTs) are able to provide higher breakdown voltages and higher current drive than conventional Si-based power devices [1]-[3]. Normally-off GaN HEMTs are greatly needed to lower power consumption and to simplify circuit and system architecture, which is one of the major challenges in GaN HEMT technology. Using recessed AlGaN and/or p-type GaN gate are two most important approaches to address the problem, both of which demand high quality etching that have good selectivity between AlGaN and GaN, high smoothness, low defects and good controllability and uniformity [2], [4]. Dry etching can provide high selectivities between AlGaN and GaN. However, it may cause significant damages to AlGaN/p-GaN interface because of physical bombardment [3]-[6], which significantly deteriorate devices' uniformity and performance.

To solve the damage problem in AlGaN etching, Z. Xu et al. utilized the selective thermal oxidation of AlGaN over GaN at 500 to 600 °C and a wet etch in a potassium hydroxide (KOH) solution [7-9]. Two extra GaN layers are needed as the capping layer and the etch

stop layer. This method can generate very smooth surfaces with root mean square (RMS) smoothness below 0.3 nm. However, the selective thermal oxidation is limited for practical application due to the more complicated epitaxy and extra thermal oxidation steps.

Digital etching is an alternative two-step etch method that produces much less damages and defects. In the first step, oxidizing plasma is used to oxidize GaN or AlGaN. Then, in the second step, the oxidation products are etched away. Many digital etching methods have been under extensive research [1,10-14]. The GaN etch recipe containing oxygen (O<sub>2</sub>) was first shown by S. D. Burnham et al. in 2010 [10]. P-type GaN HEMTs made using digital etching have been demonstrated last year, where 1nm AlN was used as the stop layer to remove 60 nm p-type GaN with the nitrous oxide (N<sub>2</sub>O) plasma [1].

However, the digital etching of AlGaN has only been studied in limited literature. One work by R. Sokolovskij et al. used pure O<sub>2</sub> plasma combined with HCl wet etching for AlGaN/GaN sensors without any etch stop layers [11]. In this work, we investigated a digital etching method with an AlN etch-stop layers to fabricate recesses with better surface roughness as well as great controlling on AlGaN/GaN structure.

For p-GaN digital etching, N<sub>2</sub>O or O<sub>2</sub> are commonly used to oxidize p-GaN, and a dry BCl<sub>3</sub> plasma etching or an HCl wet etching step is used to remove oxide layer [1, 13-14]. In Ref. [1], there is a 1 nm AlN layer under p-GaN as stop layer to achieve self-terminated digital etching. For the oxidation step, the oxidation depth in p-GaN depends on the oxidation time and the plasma bombardment strength, which is controlled by the radio frequency (RF) power and the O<sub>2</sub> flow. It can also be seen that higher bombardment strength means higher etch depth per circle but more surface damages. Therefore, these parameters need to be carefully tuned. Although O<sub>2</sub>-plasma-based digital etching of p-GaN has been

reported in [1], important etch recipe parameters were not discussed, which was studied in this work.

## 2. O<sub>2</sub>-plasma-based digital etching of AlGaN

### 2.1 Experiments

Oxygen plasma in an inductively coupled plasma (ICP) tool was used as the oxidant. The wafers were provided by Enkris Semiconductor Inc.. From the top to the bottom of a wafer, there were a 2.5 nm GaN cap layer, a 19 nm Al<sub>0.25</sub>Ga<sub>0.75</sub>N barrier layer, a 0.8 nm AlN spacer layer, and a 700 nm intrinsic-GaN above the buffer and the Si substrate. A layer of 100 nm silicon dioxide (SiO<sub>2</sub>) acted as the hard mask in the dry etching (Figure 1). The first step was to oxidize by O<sub>2</sub> plasma for 3 min. The O<sub>2</sub> flow rate was 40 sccm and the pressure was at 8 mTorr. A 90 sec wet etching in an HCl solution (DI water: HCl = 5:1) was used in the wet etch step. Then, the etch depth was confirmed by atomic force microscopy (AFM). Also, all the oxides were etched away by buffered oxide etch (BOE) solutions before AFM measurements.

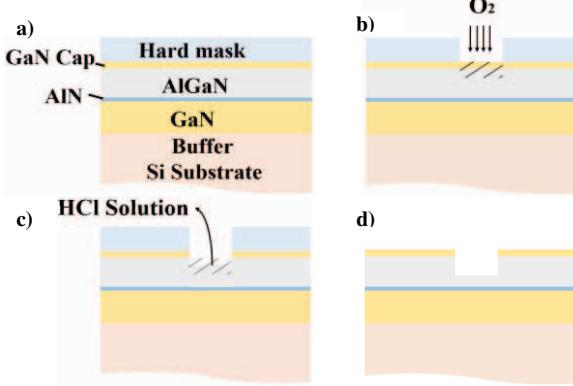


Figure 1. Schematics showing the cross-sections of the epitaxy structure (a) before etching with the hard mask, (b) during the ICP oxidation (dry etching), (c) after the HCl wet etching and (d) after removing the hard mask.

### 2.2 Discussion

For each cycle, defining the etch depth dependence on the oxidation time was important. A series of samples were oxidized with the oxidation times from 2 to 5 min under the RF power settings of 40 W. 75 W RF was also tested, but the etch rate was too high to be well controlled. The oxidation depth plateaued at 3 min with the 40 W RF power, showing the self-limiting behavior. Therefore, we chose 3 min oxidation time in our recipe.

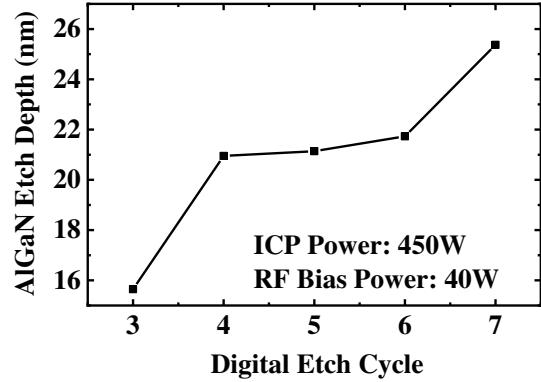
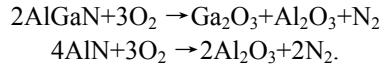
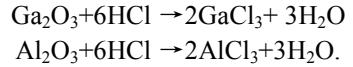


Figure 2. Etch depth vs. the cycle number using 3 min oxidation time in each cycle at 40 W RF power.

As seen in Figure. 2, the etching depth reached a plateau at the 4<sup>th</sup> cycle, and then it continued after the 6<sup>th</sup> cycle. Oxygen plasma reacted with Al<sub>0.25</sub>Ga<sub>0.75</sub>N and AlN, when the following chemical reactions occurred:



The oxidation products were etched in HCl according to the following reactions:



Digital etching paused after 4 etching cycles as shown in Fig. 2., when the etching of AlGaN was completed. After the 4<sup>th</sup> cycle, the etch depth was 20.53 nm measured by AFM. It means that all the Al<sub>0.25</sub>Ga<sub>0.75</sub>N layer was etched. In the 5<sup>th</sup> cycle, the AlN barrier layer was oxidized and became a layer of Al<sub>2</sub>O<sub>3</sub> on GaN. However, the HCl solution's etch rate was too slow to remove Al<sub>2</sub>O<sub>3</sub> in 90 sec [11], [12]. Therefore, the etching seems to be paused by this Al<sub>2</sub>O<sub>3</sub> layer.

Table 1. Average roughness values of different cycles measured on 6 1μm × 1μm areas after etch cycle 3 and 7.

Cycle #	RMS roughness	Mean roughness
No etch	0.855 nm	0.855 nm
3	0.656 nm	0.465 nm
7	0.330 nm	0.263 nm

The surface morphology of the AlGaN/GaN samples after 3 and 7 cycles of the digital etching process was compared in Figure 3. Each surface was characterized using a root-mean-square (RMS) roughness and a mean roughness (Table 1). After the 7<sup>th</sup> cycle, the RMS improved from 0.656 to 0.330 nm.

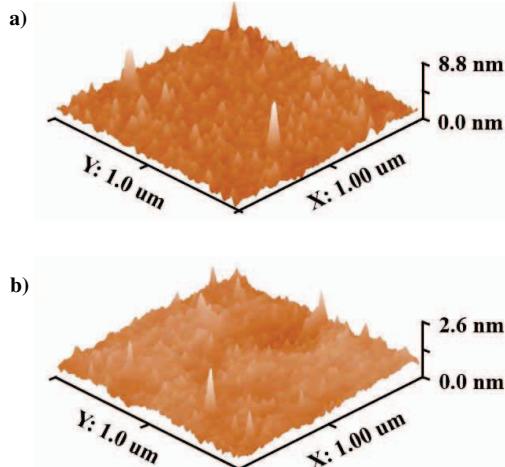


Figure 3. AFM images showing  $1 \mu\text{m} \times 1 \mu\text{m}$  area after (a) 3 cycles, and (b) 7 cycles of digital etching.

### 2.3 Summary of O<sub>2</sub>-plasma-based digital etching of AlGaN

O<sub>2</sub>-plasma-based digital etching of Al<sub>0.25</sub>Ga<sub>0.75</sub>N with 0.8 nm AlN spacer on GaN was investigated using an ICP etcher. At 40 W RF bias power and 40 sccm oxygen flow, the etch depth of Al<sub>0.25</sub>Ga<sub>0.75</sub>N was 5.7 nm per cycle. The 0.8 nm AlN spacer layer acted as an etch-stop layer for AlGaN recess. The surface roughness improved after the digital etching cycles to 0.330 nm. Compared to the dry etch only approach, this technique causes less damages. Compared to the selective oxidation with a wet etch approach, this method is less demanding on the epitaxial growth and saves the oxidation process. The presence of AlN as an etch-stop layer for the digital etching guarantees the better recess control for the preparation of gate-recessed HEMT.

## 3. O<sub>2</sub>-plasma-based digital etching of p-GaN

### 3.1 Experiments

Fig. 4 shows the p-GaN epitaxial structures in this work provide by Enkris Semiconductor Inc., and the digital etching process. A 300 nm thick SiO<sub>2</sub> by plasma enhanced chemical vapor deposition (PECVD) was used as the hard mask, which was then patterned using in an ICP etcher with SF<sub>6</sub> plasma. Secondly, p-GaN was oxidized by O<sub>2</sub> plasma. Finally, the oxidation products were removed by an HCl solution (deionized water: HCl = 4:1) for 3 min.

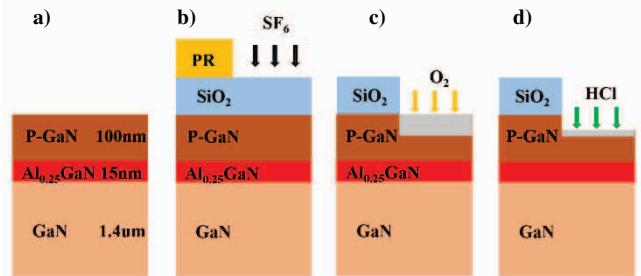


Figure 4. Schematics showing a) cross-sections of the starting epitaxy structure, b) SiO<sub>2</sub> hardmask patterning, c) dry oxidation by O<sub>2</sub>, and d) wet etching by HCl.

### 3.2 Results and Discussion

For etch circle digital etching, p-GaN oxidize depth per cycle, which is also the etch depth, will saturate with the oxygen flow and oxidation time. Fig. 5 (a) shows the oxygen flow dependence with 100 W ICP power and 40 W RF power. The oxidation depth saturates at 40 sccm. The oxidation depth also saturates with the oxidation time as seen in Fig. 5 (b).

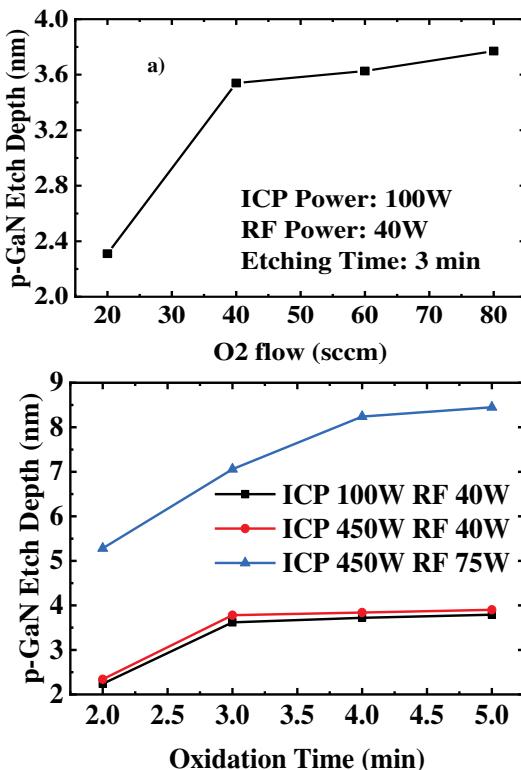


Figure 5. (a) P-GaN etch depth per cycle under different O<sub>2</sub> flow with ICP power 100W, RF power 40W and etching time 3 mins, (b) P-GaN etch depth per cycle under different ICP power and RF power with oxidation time increase when O<sub>2</sub> flow is 40 sccm.

A shallower etch depth per cycle is preferred for a better etch controllability. There is a very weak dependence on the ICP power. Therefore, 100 W ICP power and 40 W RF were chosen. 40 sccm O<sub>2</sub> flow and 3 min oxidation time were chosen, at which, the oxidation depth, also the etch depth, started to saturate. The choice of these parameters were to obtain the peak etch depth with the minimum oxidation time and flow to introduce less surface damages.

Surface roughness before and after 6 cycles of digital etching was measured by AFM and summarized in Table. 1. Our etch recipe (100 W ICP power, 40 W RF power, 40 sccm oxygen, 3 min oxidation time and 3 min HCl solution wet etch) generated a RMS surface roughness of 0.638 nm, which is quite reasonable.

Table 1. Surface roughness before and after 6 cycles of digital etching.

Etch condition	RMS roughness	Mean roughness
Un-etched	0.991 nm	0.787 nm
ICP 450 W RF 75 W	1.201 nm	0.446 nm
ICP 100 W RF 40 W	0.638 nm	0.487 nm

### 3.3 Summary of O<sub>2</sub>-plasma-based digital etching of p-GaN

In summary, key parameters for O<sub>2</sub>-plasma-based digital etching of p-GaN were investigated. p-GaN etch depth per cycle saturates with the oxygen flow and oxidation time. 100 W ICP power, 40 W RF power, 40 sccm oxygen, 3 min oxidation time and 3 min HCl solution wet etch formed a good etch recipe, which can obtain 3.6 nm etch depth per circle and the achieved RMS surface roughness was around 0.638 nm after etching. These are technically relevant to obtain controllable, uniform etch surfaces with low surface damages.

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### References

- [1] H. Chiu, Y. Chang, B. Li, H. Wang, H. Kao, F. Chien, C. Hu, and R. Xuan, IEEE Transactions on Electron Devices, 65(11), pp. 4820-4825 (2018).
- [2] K. Chen, and C. Zhou, Phys. Status Solidi A, 208 (2), pp. 434–438 (2011).
- [3] C. Chen, S. Keller, E. Haberer, L. Zhang, S. DenBaars, E. Hu, U. Mishra, and Y. Wu, Journal of Vacuum Science & Technology B, 17(6), pp. 2755-2758 (1999).
- [4] D. Buttari, A. Chini, T. Palacios, R. Coffie, L. Shen, H. Xing, S. Heikman, L. McCarthy, A. Chakraborty, S. Keller, and U. Mishra, Applied Physics Letters, 83(23), pp. 4779-4781 (2003).
- [5] J. Lee, J. Kim, D. Jung, C. Kim, W. Lee, J. Lee, J. Shin, M. Shin, J. Oh, and J. Lee, Jpn. J. Appl. Phys. Part 2 (Letters), 40(3), pp. 198-200 (2001).
- [6] V.Liberman, G.Haase and R. OsgoodJr., Surf. Sci. 277, pp. 282-300 (1992).
- [7] S. Lin, M. Wang, F. Sang, M. Tao, C. Wen, B. Xie, M. Yu, J. Wang, Y. Hao, W. Wu, J. Xu, K. Cheng, and B. Shen, IEEE Electron Device Letters, 37(4), pp. 377-380 (2016).
- [8] Z. Xu, J. Wang, J. Liu, C. Jin, Y. Cai, Z. Yang, M. Wang, M. Yu, B. Xie, W. Wu, X. Ma, J. Zhang, and Y. Hao, IEEE Electron Device Letters, 35(12), pp.1197-1199 (2014).
- [9] Z. Xu, J. Wang, Y. Liu, J. Cai, J. Liu, M. Wang, M. Yu, B. Xie, W. Wu, X. Ma, and J. Zhang, IEEE Electron Device Lett., 34(7), pp. 855–857 (2013).
- [10]S. Burnham, K. Boutros, P. Hashimoto, C. Butler, D. Wong, M. Hu, and M. Micovic, Phys. Status Solidi C 7, 7(8), pp. 2010-2012 (2010).
- [11]R. Sokolovskij, J. Sun, F. Santagata, E. Iervolino, S. Li, G. Zhang, P. Sarro, and G. Zhang, 30th Eurosensors Conference Procedia Engineering, 168, pp. 1094-1097 (2016).
- [12]O. Breitschädel, B. Kuhn, F. Scholz, and H. Schweizer, Journal of Electronic Materials, 28(12), pp.1420-1423 (1999).
- [13] A. Baharin, R.S. Pinto et.al, Conference on Optoelectronic and Microelectronic Materials and Devices, pp. 145-146 (2010).
- [14] Yuan Lin, Yueh Chin Lin, Franky lumbantoruan et.al, IEEE International Conference on Semiconductor Electronic, pp. 121-123 (2018).