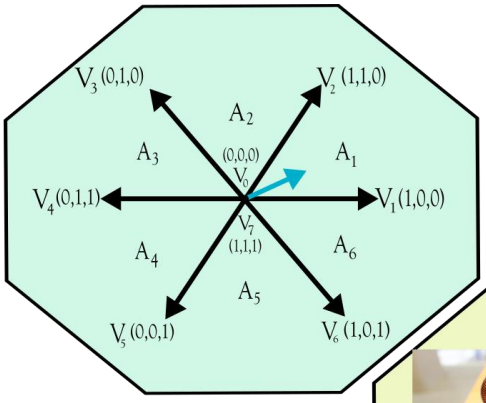
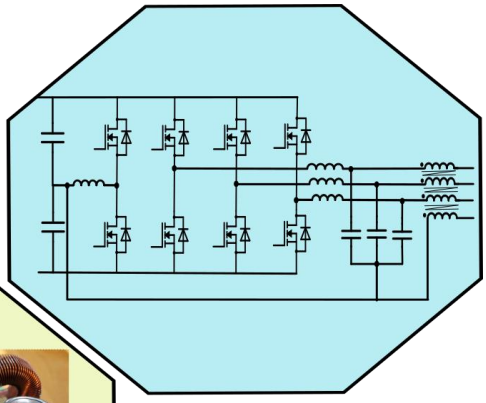
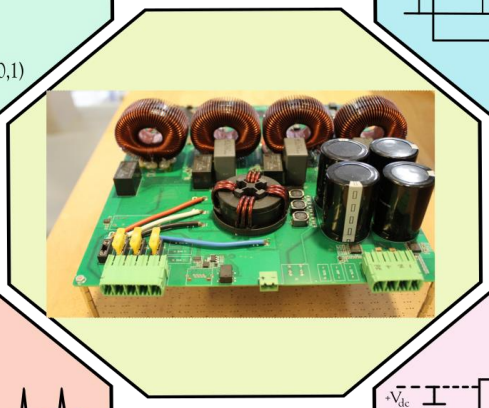
Design of Control for Bidirectional DC/AC Converters

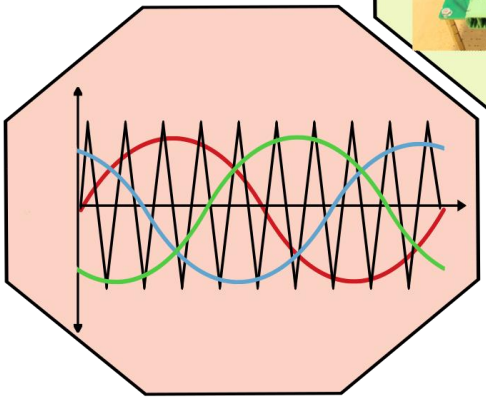
by

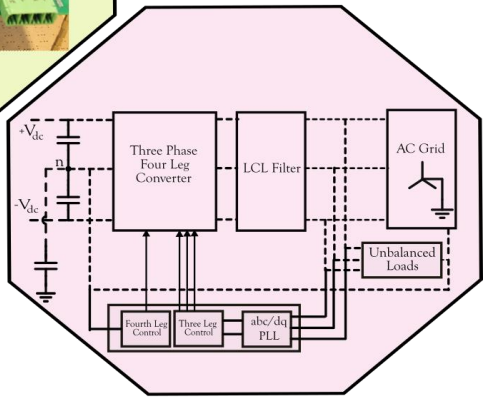
Aniruddh Kulkarni











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Design of Control for Bidirectional DC/AC Converters

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Abstract

The increasing penetration of the distributed energy sources and the increasing load on the AC grid demands for integration of DC grids in AC distribution network. This has resulted in the requirement of power electronic converters such as DC/AC converters. For different operating conditions of the DC/AC converter it is not recommended for the converter to operate in open loop. Hence, while designing the control for the converter there are challenges such as the presence of unbalance on the grid leading to higher losses, offsetting of AC voltages at the output and grounding of the converter leading to higher common mode voltage and currents. This thesis explores the control strategy that can be implemented on the converter to mitigate the unbalance in different operating conditions and compares different modulation techniques to reduce the common mode voltage and currents.

To begin with the islanded operation is considered for the converter and the voltage control is implemented on this type of converter. Further a modification on this type of control is proposed for the operation of converter under overcurrent scenario. Subsequently the control strategy for grid connected operation is analyzed such that the issue of unbalanced currents on the grid is mitigated. Three different operating modes are considered under grid connected operation for validating the control strategy proposed. Following the controlled operation in islanded and grid connected scenario, the active methods for reducing the common mode voltage are reviewed by comparing different modulation techniques.

On the discussed control strategies for different operating conditions of the DC/AC converters, an optimized implementation of the control on the microcontroller is presented. Other functionalities such as protection of the converter against unwanted actions is investigated through implementation of state machine. The results of the controlled DC/AC converter operating in islanded operation is presented and modifications in the existing PCB are discussed to make it compatible to operate under grid connected condition. The operation of control strategies implemented is validated for the real time application of the converter with unbalanced load conditions.

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List of Abbreviations

DER	Distributed Energy Resources
PV	Photovoltaic
LV	Low Voltage
CMV	Common mode Voltage
CMC	Common mode Current
PLL	Phase locked loop
PCC	Point of Common Contact
THD	Total Harmonic Distortion
SRF	Synchronous Reference Frame
DDSRF	Decoupled Double Synchronous Reference Frame
SO	Symmetrical Optimum
DSRF	Double Synchronous Reference Frame
P control	Proportional Control
PR control	Proportional Resonant Control
PI control	Proportional Integral Control
KVL	Kirchhoff's Voltage Law
mA	milli-Ampere
CM	Common Mode
RCMV PWM	Reduction of Common Mode Pulse Width Modulation
SPWM	Sine Wave Pulse Width Modulation
PS-SPWM	Phase Shifted Sine Wave Pulse Width Modulation
SVM	Space Vector Modulation
AZSPWM	Active Zero State Pulse Width Modulation
SiC	Silicon Carbide
PCB	Printed Circuit Board
MCU	Microcontroller Unit
ADC	Analog to Digital Conversion
FEM	Finite Element Method

List of Symbols

Symbol	Figure	Description
$S1$ to $S8$	Figure 1.3	MOSFET
V_{dc}	Figure 2.1	Pole to Pole DC Voltage
L_a, L_b, L_c	Figure 2.1	Filter inductance
C_{xa}, C_{xb}, C_{xc}	Figure 2.1	X – capacitors
C_{ya}, C_{yb}, C_{yc}	Figure 2.1	Y – capacitors
R_{La}, R_{Lb}, R_{Lc}	Figure 2.1	Load Resistance
L_{La}, L_{Lb}, L_{Lc}	Figure 2.1	Load Inductance
N, n	Figure 2.1	Neutral point
C_{cm}	Figure 2.1	Grounding capacitor
$V_{3ph,converter}$	Figure 2.4	Measured converter voltages (3-phase)
$V_{\alpha\beta 0}$	Figure 2.4	Stationary reference frame of measured converter voltages.
θ_{ref}	Figure 2.4	Angle reference for transformation.
V_{dq}^{p}	Figure 2.4	Positive sequence of measured converter voltages in synchronous reference frame.
V_0	Figure 2.4	Zero sequence voltage of measure converter voltages.
$V_{d,reference}^{p}$	Figure 2.5	Positive sequence d–axis reference voltage in synchronous reference frame.
$V_{d,measured}^{p}$	Figure 2.5	Positive sequence d–axis measured voltage in synchronous reference frame.
$V_{q,reference}^{p}$	Figure 2.5	Positive sequence q–axis reference voltage in synchronous reference frame.
$V_{q,measured}^{p}$	Figure 2.5	Positive sequence q–axis measured voltage in synchronous reference frame.
K_p	Figure 2.5	Proportional gain
K_i	Figure 2.5	Integral gain
V_d^p	Figure 2.5	Controlled output of d–axis voltage controller in positive sequence.
V_q^p	Figure 2.5	Controlled output of q–axis voltage controller in positive sequence.

V_a^p, V_b^p, V_c^p	Figure 2.5	Controlled output in three–phase positive sequence.
V_{dq}^n	Figure 2.6	Negative sequence c converter voltages in synchronous reference frame.
V_d^n	Figure 2.6	Controlled output of d–axis voltage controller in negative sequence.
V_q^n	Figure 2.6	Controlled output of q–axis voltage controller in negative sequence.
V_{abc}^p	Figure 2.7	Controlled output in three–phase positive sequence.
V_{abc}^n	Figure 2.7	Controlled output in three–phase negative sequence.
$V_{dc,upper}$	Figure 2.8	Upper capacitor voltage on DC side
$V_{dc,lower}$	Figure 2.8	Lower capacitor voltage on DC side
$V_{n,ref}$	Figure 2.8	Controlled output voltage of the fourth leg voltage controller.
V_{ga}, V_{gb}, V_{gc}	Figure 3.1	Grid voltages
$\theta_{calculated}$	Figure 3.5	Angle calculated from measured voltages.
ω_{PLL}	Figure 3.5	Frequency from output of PLL.
θ_{PLL}	Figure 3.5	Angle from output of PLL.
$i_{3ph,converter}$	Figure 3.6	Measured three phase converter currents.
$i_{\alpha\beta 0}$	Figure 3.6	Measured converter currents in stationary reference frame.
i_{dq}^p	Figure 3.6	Measured converter currents in positive sequence synchronous reference frame.
i_{dq}^n	Figure 3.6	Measured converter currents in negative sequence synchronous reference frame.
i_o	Figure 3.6	Zero sequence of measured converter currents.
$i_{d,reference}^p$	Figure 3.7	Positive sequence d–axis reference current in synchronous reference frame.
$i_{d,measured}^p$	Figure 3.7	Positive sequence d–axis measured current in synchronous reference frame.
$i_{q,reference}^p$	Figure 3.7	Positive sequence q–axis reference current in synchronous reference frame.

$i^{p}_{q,measured}$	Figure 3.7	Positive sequence q–axis measured current in synchronous reference frame.
$i^{n}_{d,reference}$	Figure 3.8	Negative sequence d–axis reference current in synchronous reference frame.
$i^{n}_{d,measured}$	Figure 3.8	Negative sequence d–axis measured current in synchronous reference frame.
$i^{n}_{q,reference}$	Figure 3.8	Negative sequence q–axis reference current in synchronous reference frame.
$i^{n}_{q,measured}$	Figure 3.8	Negative sequence q–axis measured current in synchronous reference frame.
$i_{0,load}$	Figure 3.9	Zero sequence of load currents.
$i_{0,converter}$	Figure 3.9	Zero sequence of converter currents.
C_{upper}	Figure 3.12	Upper capacitor on DC side.
C_{lower}	Figure 3.12	Lower capacitor on DC side.
i_{Ln}	Figure 3.12	Current through the neutral inductor.
i_n	Figure 3.12	Current in the neutral line.
i_c	Figure 3.12	Current in the line connecting neutral point to the split capacitors.
$V_{ni,ref}$	Figure 3.13	Controlled output voltage of the fourth leg current controller.
$V1$ to $V6$	Figure 3.14	Defined vectors in space vector modulation.
$A1$ to $A6$	Figure 3.14	Sectors defines by the vectors in space vector.

Chapter-1
Introduction

The global climate is now changing as a result of the human exploitation of resources such as fossil fuels for generation of electricity. The solution to abate the degradation of the global climate is transitioning the electricity generation from the conventional fossil fuel based sources to renewable sources. The generation of electricity using renewables is sparse because the type of renewable source available varies based on geographical location. These types of sources are classified under "Distributed Energy Resources (DER's) [1]."

However, the current scenario is developing in terms of generating electricity through renewable sources. Figure 1.1 shows the increase in electricity generation based on renewable sources [2]. The merging of these natural DER's with the controllable loads within defined electrical boundaries forms a flexible entity which is called a "Microgrid" [3]. Microgrids can be either AC or DC depending on the source used. Based on the literature on different types of microgrids it has been seen that the DC microgrids are flourishing [4], [5]. This thesis concerns such DC microgrids formed based on Solar PV [6].

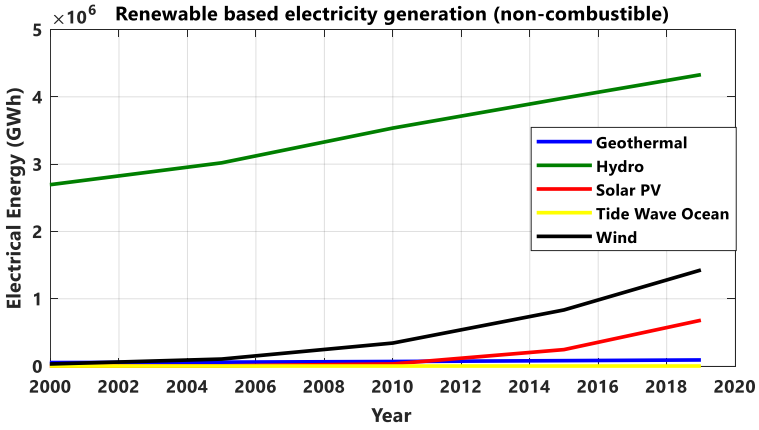

Figure 1.1 Electricity generation based on non-combustible renewable sources

Simultaneous to the development of electricity generation, the sustainable transition is also taking over the automobile industry through e-mobility. Although this transition helps the motive of transitioning towards sustainability, it has been seen that there will be an increase in the energy demand because of the EV industry. The EV's act as active loads which increase the power demand on the distribution

network [7]. One such example is the analysis done by McKinsey on the German grid which shows that the local peak demand on the grid will increase approximately by 30% [8]. Hence, the use of renewable energy can be done to compensate for the additional energy demand.

The development of power electronic devices is the solution to reliably connect renewable sources to the low voltage distribution grid. These power electronic devices act as interface between the source and the low voltage grid. This thesis focuses on the control of power electronic device which acts as an interface between a bipolar DC grid and the AC distribution grid. This would lead to an increased flexibility of the grid and provide a sustainable solution to meet the higher peak demand. The block diagram of the converter is shown in Figure 1.2. The intermittency in the power generation using DER's makes it challenging to integrate it in the existing distribution grid [9].

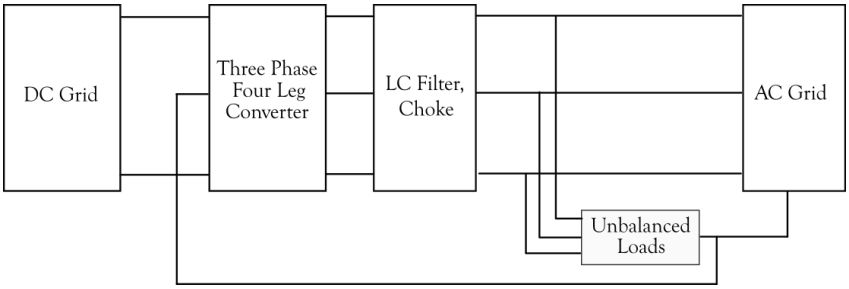

Figure 1.2 DC/AC converter block diagram

Also, with the increasing flexibility and increasing load demand, there is also unbalance introduced. More specifically, in three-phase four-wire systems the unequal distribution of loads give rise to large neutral currents [10], [11]. As seen the increasing loads are connected on the distribution side rather than the transmission grid. The DER's when integrated with the AC distribution grid also interconnect the ever increasing loads such as air-conditioning, EV chargers etc., on the grid [5].

The problem of phase unbalance is existing in many countries. For example, the analysis of a UK based consultancy firm on 89 LV substations showed that 165 out of 233 feeders in these substations had phase unbalance [12]. The causes of the phase unbalance are described as follows [12],[13]:

1. The non-uniform load allocation on the grid creates an accumulation of unbalance over time based on the addition of new users of the network.
2. The asymmetry existing in the grid.
3. Real time load behavior by the customers is unpredictable at the finest level thereby causing the phase unbalance.

4. Faults occurring on individual phases or phase-phase (except three phase fault) creating an unbalance on the other phases.

The challenges in controlling the power electronic device are explained in the following subsection.

1.1. Challenges in converter control design

It is important to note that the output voltage obtained from the photovoltaic panels (PV panels) is DC, and the low voltage distribution grid operates on AC. Power electronic devices such as inverters are used to interface the PV based DC microgrids and the low voltage (LV) distribution grid. Power electronic interface devices such as three-phase four-leg DC/AC converter can be controlled to integrate with the distribution grid [9],[14]. Addressing this issue, DC Opportunities has designed a bidirectional DC/AC converter. The existing DC/AC converter is a **four-leg split capacitor topology**, and the schematic is shown in Figure 1.3.

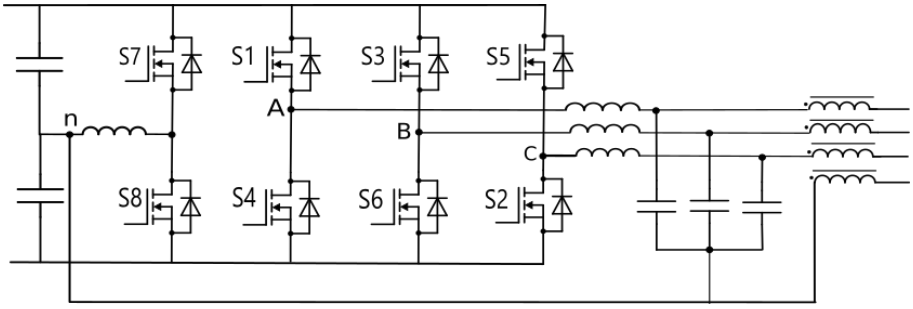

Figure 1.3 Three-Phase Four-leg Converter Schematic

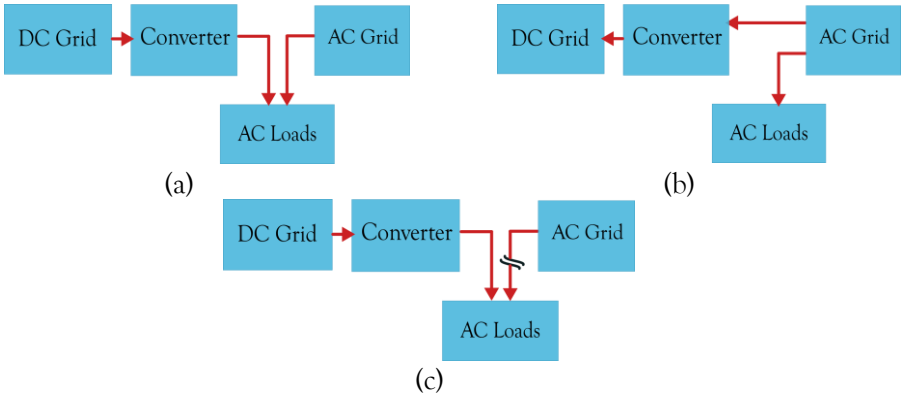

Figure 1.4 (a) Grid connected – DC grid and AC grid providing power to AC loads (b) Grid connected – AC grid providing power to DC grid as well as AC loads (c) Islanded Operation

The existing converter is operating as an uncontrolled interface and the purpose of this thesis is to design the control of the inverter such that it can interface with the grid and can also fulfil the energy requirements of the load. There are two different operations of the converter [9].

- Islanded operation
- Grid connected operation

The different operating modes of the converter are shown in Figure 1.4. The challenges which form the criteria for the control structure are briefly introduced the following subsections.

1.1.1. Islanded operation

The islanded operation refers to the absence of the AC distribution grid. Hence, under islanded condition there is no reference for the voltage and the converter has to operate in grid forming mode. As the AC loads (single/three phase) are still connected at the output of the converter it is important that the output of the converter should have balanced three phase voltages under healthy operating conditions.

Also, as seen from the above literature there is presence of unbalance in the AC loads connected at the output. Hence, under varying unbalanced loads and variable DC voltage on the DC grid, the converter will not be able to maintain balanced voltages while operating in open loop. For unbalanced AC loads, the converter should be able to control operations for overcurrent in one, two or three phases. These challenges exist while designing the control for the three phase converter operating in islanded mode.

1.1.2. Grid Integration

The primary challenge in interfacing the DC microgrid with the LV grid is the synchronization of four parameters: voltage magnitude, frequency, phase, phase sequence. When the converter is operating in grid connected mode, the solar panel is a grid supporting source. Hence, the converter is connected with the LV grid as well as the loads simultaneously.

The challenges seen in islanded operation are similar in this type of operation. However, there are some additional challenges in grid connected mode. As per IEEE Std 519-1992, the grid connected converter must have less than 5% harmonic injection in voltage and current [15]. In distribution grids, the unbalance impacts the grid. Hence, the challenge is to control the currents such that the grid remains balanced while the converter mitigates the unbalance.

1.1.3. DC Voltage Balancing

Figure 1.3 shows that the converter uses a split capacitor topology. Hence, one of the main challenges is to avoid the DC offset in the AC phases. As the neutral

point of the bipolar DC input is connected to the AC side of the converter, the absence of control on neutral point can inject unbalance on the AC output. If the voltage on the capacitors is not properly balanced, the neutral point will have a DC offset voltage which will shift the AC output voltages by the same offset.

1.1.4. Common mode Voltage and Common mode Current

The common mode current in the power electronic devices is a major concern. For a three phase DC-AC converter, the common mode voltage is defined as the potential difference between the neutral point on the converter and the ground. As a result of this voltage, common mode current flows through the neutral to the ground.

The common mode leakage current impacts the net losses, results in increased grid harmonics and can create a strong radiated EMI [16]. The magnitude of common mode current depends on the parasitic capacitance formed between the converter and the ground [16], [17]. Also, the method of grounding also determines the impedance in the common mode path which determines the magnitude and the frequency of the common mode current. Also, the common mode current can cause false tripping of protective devices.

1.1.5. Hardware Implementation

Apart from the control challenges the thesis also addresses the challenges to be addressed while implementing the control on the controller and testing of the converter. For hardware implementation of the control, it is important to ensure that the response of the converter is fast.

Another important challenge with the control on the microcontroller is that the control frequency for the microcontroller is considerably low. This leads to reduced resolution for the control. For testing the converter, it is important to prevent the converter from unwanted voltages and currents in case of incorrect operation.

1.2. Research Questions

The objective of this thesis is to implement the control strategies on the existing DC/AC converter for islanded operation and integrating DC bipolar grid with AC distribution grid. The research questions addressed in this thesis are stated as follows:

1. What are the control strategies that have to be implemented on islanded converter and how to implement them?
2. What are the control strategies that have to be implemented on grid connected converter and how to implement them?
3. What are the different modulation techniques to reduce common mode voltage in grid connected DC/AC Converter?

Apart from the major three research questions, the thesis also focuses on how to implement the control on hardware.

1.3. Overview of Chapters

The research questions are addressed in the different chapters of thesis and different solutions for the control design are provided. The structure of this thesis consists of six chapters. An overview of each of the chapter is given below.

- Chapter-1 provides an introduction to the project, motivation for the detailed study on this topic, information on each of the challenges and methods to address the challenges.
- Chapter-2 focuses on the control of the converter when it is operating in islanded mode i.e., without the grid. The various control strategies that are necessary to be implemented on the islanded converter to mitigate the discussed challenges in subsection 1.1.1 are explained in detail. Further to this, the chapter provides the simulation results for the converter.
- Chapter-3 focuses on the control of the converter when it is operating in grid connected condition. The various control strategies that are necessary to be implemented on the grid connected converter to address the challenges discussed in subsection 1.1.2 are explained. Further to this, the chapter provides the simulation results for the converter.
- Chapter- 4 provides insight on the common mode voltage (CMV) and common mode currents (CMC) in such type of converter, how it depends on the connection of the neutral point and explains different types of modulation techniques to reduce the common mode voltages and currents. Finally, this chapter provides a comparison of the simulation of all modulation techniques and the resultant common mode currents and the criteria used in this thesis for adapting to a particular modulation technique.
- Chapter-5 discusses the challenge in the hardware design of the converter. The implementation of the control, modulation technique on the microcontroller is discussed. The hardware test results of converter at high voltage for the islanded operation is provided. Further to this, the chapter suggests some modifications on the PCB design for the grid connected converter based on the necessary control strategy.
- Chapter-6 provides a conclusion to the thesis, on the control strategies and the hardware implementation of the converter. This chapter then provides a brief description of the future scope for implementing additional control on the converter.

Chapter-2
Control of Islanded Converter

As seen in Chapter-1 , one of the modes of operation of the converter is islanded mode. In islanded mode, the converter is directly connected to the 3–phase load, or it can be connected to separate single phase loads. The schematic of the converter operating in islanded mode of operation is shown in Figure 2.1. For islanded operation, the current from the converter is provided based on the load demand. As there is no presence of a grid reference voltage or frequency, the converter operates in grid forming mode. The objective of the converter in this type of operation is to output a balanced three phase voltage with 230V RMS per phase.

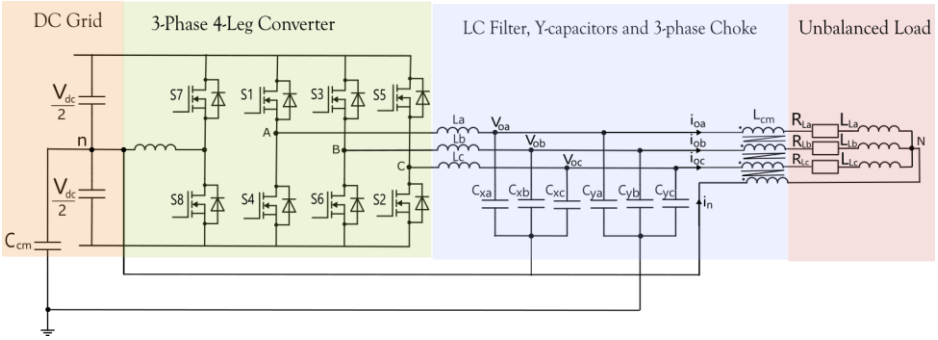

Figure 2.1 Block diagram of Islanded mode of converter.

2.1. Converter Topology

As seen from the schematic, the converter is a 3-phase 4-leg topology with split capacitor on the DC side. The three legs of the converter are utilized to convert to AC output while the fourth leg is connected to the split capacitors. At the AC output of the converter, LC filter is used to filter the higher order harmonics introduced due to switching. The neutral of the X-capacitors (i.e., capacitors for each phase of LC filter) is connected to the neutral of the bipolar grid on DC side as well as it forms the neutral path for the unbalanced load neutral.

Each phase also has Y-capacitors which are connected from phase to ground. These capacitors have low capacitance to avoid the high frequency signals entering the ground by providing high impedance. The inductor on the load side of the converter is a three-phase four winding common mode choke. The LC filter is added by another inductance introduced by the leakage inductance of the common mode choke. As the common mode choke is intended to provide high impedance for the higher frequency component, the leakage inductance is very low. The

modeling and the values for leakage inductance of the common mode choke are discussed in the later subsection.

As the neutral point on the bipolar grid is connected to the AC side, it is also important to control the neutral point such that the voltage across the DC split capacitors is balanced. Hence, as the requirement is to establish a balanced three phase output voltage, a voltage control is relevant for this type of operation.

2.2. Axes transformation

The first and the foremost step before designing the controller is the usage of dq0-reference frame or the synchronous reference frame. The three phase parameters have a periodic wave which is sinusoidal in nature. Hence, in such cases, if the instantaneous values are used to control the converter, the error which is used in a PI control will be fluctuating. Hence, the error generated will be a non-zero quantity. Hence, by changing the reference axis of the parameters the sinusoidal waves can be analyzed as DC quantities in a synchronous reference frame. The conversion involves two steps:

1. **Clarke Transformation:** This transformation converts the sinusoidal quantities from a three phase to a fixed reference frame with two axis and the third is considered as the zero axis. This is called the αβ0- reference frame.

2. **Park Transformation:** This transformation converts the αβ quantities to a synchronous reference frame i.e., the axis rotates at the same frequency as the quantities. Due to the rotation of frame of reference, the quantities can be analyzed as DC quantities.

The co-ordinate axes corresponding to the three-phase, the αβ0 and the synchronous reference frame (dq0) are shown in Figure 2.2. For converting the three-phase quantities into space vector i.e., the αβ reference frame Clarke transform is used as shown by equation (2.1) and to convert from space vector to synchronous reference frame, Park transform is used given by equation (2.2).

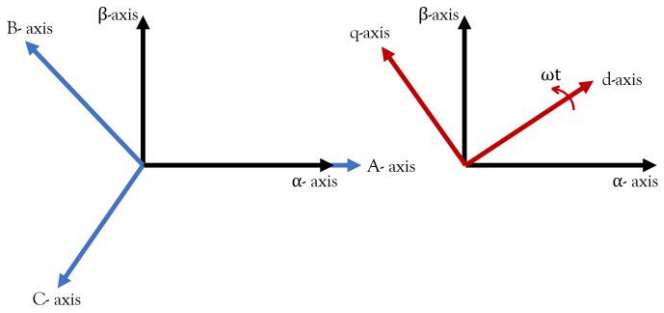

Figure 2.2 (a) abc-αβ reference frame (b) αβ-dq reference frame

It is important to note that in the space vector axes, the quantities are still sinusoidal in nature but in the synchronous reference frame, the rotational component i.e., the 'θ' is removed and hence the quantities can be analysed as DC quantities. In a similar way to convert from the synchronous reference frame to the three-phase quantities Inverse Park Transform and Inverse Clarke Transform are used given by equations (2.3) and (2.4) respectively.

There are two types of Clarke Transform: a.) Amplitude Invariant b.) Power Invariant. The difference between these two transformation is the co-efficient. For amplitude invariant $\frac{2}{3}$ is used while for power invariant $\sqrt{\frac{2}{3}}$ is used. Equation (2.1) represents the amplitude invariant.

Clarke Transform:
$$\begin{bmatrix} u_\alpha \\ u_\beta \\ u_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} \quad (2.1)$$

Park Transform:
$$\begin{bmatrix} u_d \\ u_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix}\begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} \quad (2.2)$$

Inverse Park Transform:
$$\begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix}\begin{bmatrix} u_d \\ u_q \end{bmatrix} \quad (2.3)$$

Inverse Clarke Transform:
$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 \\ \frac{-1}{2} & \frac{\sqrt{3}}{2} & 1 \\ \frac{-1}{2} & \frac{-\sqrt{3}}{2} & 1 \end{bmatrix}\begin{bmatrix} u_\alpha \\ u_\beta \\ u_0 \end{bmatrix} \quad (2.4)$$

2.3. PI Controller and PR Controller

There are two widely used methods for implementing the voltage control of the converter: PR controller and PI controller. For a three phase converter, the PR controller can be used to track the sinusoidal waveforms [18]. The PR controller provides high gain at the resonant frequency i.e., the fundamental frequency in this case and attenuates all the other frequencies [18], [19]. An added advantage of PR controller is that the number of times axes transformation has to be done is reduced.

The PI controller is more commonly implemented on converter and provides very high gain at zero frequency. Hence, the PI controller are used mostly for DC signals. Even the PR controller is efficient for controlling sinusoidal signals and

minimizing the steady state errors, the PR controller is not very efficient while dealing with unbalanced voltages. During axes transformation of unbalanced signals, oscillations are introduced which make the PR control less efficient to be implemented [18]. However, for implementing PI control the number of times axes transformation is done is increased by one. As this thesis deals with controlling the converter under unbalanced load operation, PI controllers will be used for all the control strategy discussed. The steps followed to design the control of the islanded converter are discussed in this chapter.

2.4. Converter Control strategy

The converter operates in grid forming mode in case of islanded operation. In the islanded operation, the converter output has to be a balanced three phase voltage with a frequency of 50Hz. Hence, voltage control is used for the converter operating in islanded operation. In case of islanded operation, there is no reference for the converter to align itself to operate at 50Hz frequency. Hence, to address this issue, the reference of the angle is provided as a control input. Hence, the reference of the angle is given as a part of the control and the waveform of the angle is shown in Figure 2.3. This fulfils the purpose of the "phase-locked-loop (PLL)" in case of grid connected operation [20].

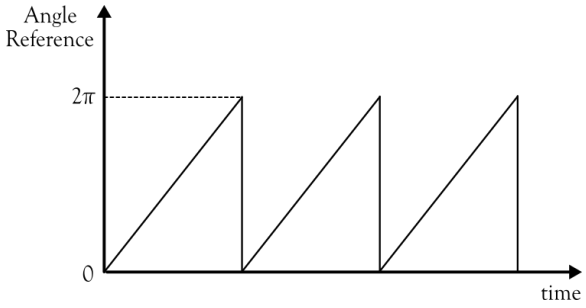

Figure 2.3 Angle reference for the voltage controller.

Once the angle reference is set, the three phase parameters are transformed into the synchronous reference frame. As the objective is to control the voltage instead of the power, amplitude invariant form is used for transformation. As mentioned before, the output of the converter is rated similar as the LV grid i.e., balanced three phase voltages with 230V rms voltage on one each phase and the purpose of the controller is to provide the required output. To solve this purpose, a PI controller is used.

Figure 2.4 shows the control block diagram of a three-phase 3-leg converter. As seen from the block diagram, there are two PI controllers used, one controls the d-axis voltage and the other one controls the q-axis voltage. The PI controllers should be tuned such that the voltage on the d-axis is aligned to the peak magnitude of the AC voltage i.e., $230\sqrt{2}$V and the voltage on the q-axis is aligned to 0V.

The operation of individual PI controllers within the voltage control block is shown in Figure 2.5. The output of the PI controller is a reference voltage which is then used to modulate the duty ratios such that the converter maintains a stable voltage at the output. The theoretical calculation for obtaining the balanced three phase voltages is shown below.

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \begin{bmatrix} cos\theta & -sin\theta \\ sin\theta & cos\theta \end{bmatrix} \begin{bmatrix} 230\sqrt{2}\,V \\ 0\,V \end{bmatrix} \tag{2.5}$$

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \begin{bmatrix} 230\sqrt{2}cos\theta\,V \\ 230\sqrt{(2)}sin\theta\,V \end{bmatrix} \tag{2.6}$$

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \frac{-1}{2} & \frac{\sqrt{3}}{2} \\ \frac{-1}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \begin{bmatrix} 230\sqrt{2}cos\theta\,V \\ 230\sqrt{(2)}sin\theta\,V \\ 0\,V \end{bmatrix} \tag{2.7}$$

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} 230\sqrt{2}cos\theta\,V \\ 230\sqrt{(2)}cos(\theta - 120^o)\,V \\ 230\sqrt{(2)}cos(\theta - 240^o)\,V \end{bmatrix} \tag{2.8}$$

As seen from equations (2.5) to (2.8), it can be seen that if the voltages are aligned at 230√2V and 0V for d-axis and q-axis respectively, the final output obtained will be a balanced three-phase system.

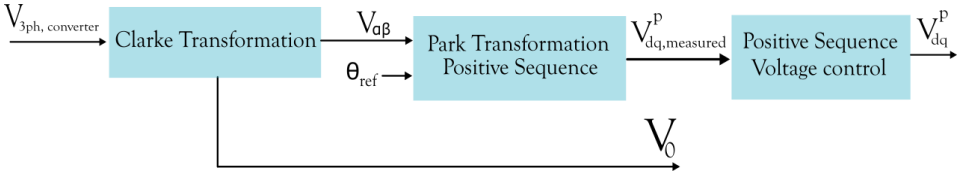

Figure 2.4 Voltage control of the converter.

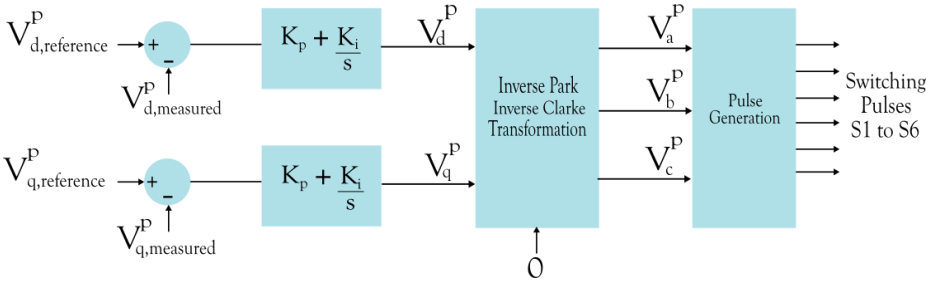

Figure 2.5 PI control for voltages in dq-reference axis.

2.4.1. Current limit control

The control strategy discussed above is to provide balanced three phase voltage at the output of the converter. As mentioned previously the converter operates in grid forming mode in islanded operation. Hence, with the variable output power, the converter provides the current demanded by the loads. However, with the unbalanced phase loads under overcurrent condition, the current in single phase, two phase or all three phases can increase beyond the limit that the converter can provide. Especially for a single phase or two phase overcurrent the single phase power of the converter exceeds the limit, but the three phase power does not exceed the limit. This can cause damage to the components of the converter.

Thus, a modification of the control is necessary. Also, to prevent the converter from getting damaged the modified control should have fast response. The control of the current can be done by reducing the voltage thereby limiting the current to the maximum rated value of the converter. It is important to detect the overcurrent per phase. Hence, the voltage corresponding to the phase in overcurrent should be reduced and the other phases should maintain the same amplitude.

As seen from the previous subsection, the voltage control of the converter operates in synchronous reference frame (dq-reference frame) hence the per phase voltages have to be controlled in dq-reference frame. This can be achieved using the concept of symmetric components. The symmetric components have been explained in detail in 3.1. For a three phase system the presence of negative sequence along with positive sequence indicates unbalance. Hence, in the modified control strategy, the unbalance is injected into the system by injecting the negative sequence along with the positive sequence control such that the output of the controller would have reduced phase voltages only on the phase with overcurrent.

In this control strategy only positive and negative sequence controllers are used and the zero sequence is given the reference of zero. This is because if the zero sequence is not zero then the other phase will also have an impact on the magnitude if one phase reduces. Hence, to act only on one phase the negative sequence will set reference points in dq accordingly and make the zero sequence voltage equal to zero. The modified control block diagram is shown in Figure 2.6 and the modified controller structure is shown in Figure 2.7.

As the negative sequence voltage control is activated only during overcurrent, the instantaneous measurements of phase currents are compared to the maximum current that the converter can provide. If the phase current/currents exceeds the maximum current limit, a signal is provided to activate the negative sequence controller through C-script in PLECS and a three phase system with reduced voltage amplitude is given as reference for the negative sequence controller. The signal is also responsible for detecting the phase in overcurrent and used to reduce the

amplitude of the voltage of the corresponding phase. The C-script is given in the Appendix for reference.

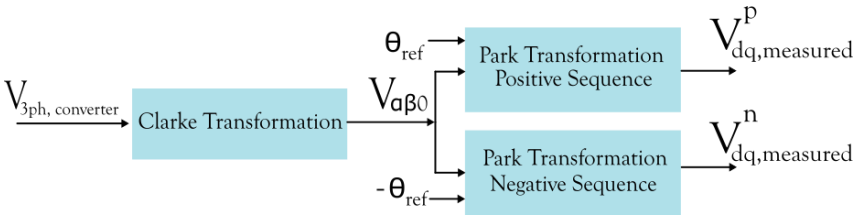

Figure 2.6 Modified voltage transformation

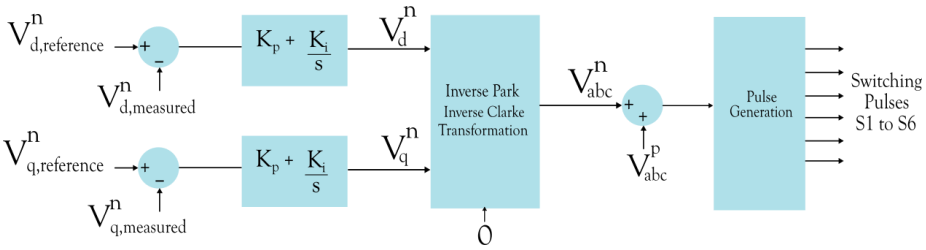

Figure 2.7 Negative sequence voltage controller

2.4.2. Control of the Fourth Leg

As seen from the schematic of the converter in Figure 2.1, the DC grid is interfacing the converter with two capacitors thereby forming a split capacitor topology. In inverter systems which interface unbalanced loads or interface the grid, a neutral wire is provided in order to regulate the neutral current [21]. Generally, there are three types of topologies for AC/DC converters which use the neutral point on DC side: a.) A split capacitor topology b.) a fourth leg with DC link capacitor and c.) fourth leg with split capacitor topology. In the converter being used, a fourth leg is introduced to regulate the voltage on the split capacitors.

This neutral point on the DC side should be ideally at a potential such that the voltage on the two capacitors must be balanced [21]. If the neutral point is not well balanced, there will be neutral current injected to the AC side which can induce the unbalance in the currents [22]. The advantage of using the fourth leg to balance the neutral point of the capacitor is that the control of the fourth leg can be made independent from the three phase control of the converter [22].

The voltage of the neutral point can be calculated based on equation (2.9). The primary objective of the fourth leg is to maintain ε at zero. Reference [21] presents a double control loop consisting of neutral point voltage and the neutral wire current control to mitigate the issue of fluctuating neutral point voltage. However, due to practical limitations such as measurement of the currents on the neutral wire, the current control loop increases the complexity. Hence, in the current control strategy, only the voltage control loop is used.

$$\varepsilon = (V_{dc,upper} - V_{dc,lower}) \tag{2.9}$$

This can be achieved by using a control loop using a proportional controller. Figure 2.8 shows the control block diagram of the fourth leg.

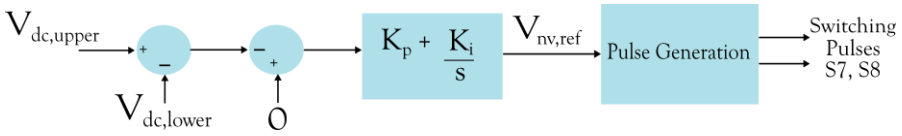

Figure 2.8 Control block diagram of the fourth leg.

2.5. Simulation of Converter

The DC/AC converter is simulated in PLECS software to analyze the control strategies discussed in this chapter. The methodology, analysis points and the results of the simulation are discussed in this subsection. For analyzing the implemented control strategy, the schematics used in PLECS are given in Appendix.

The measurements which provide the parameters to the controller are highlighted in the schematic. These points indicate the same position which is being measured on the PCB. For analyzing the control, the simulation parameters initialized in PLECS are set as given in Table 2.1.

Parameters	Symbol in Schematic	Values
DC Bus voltage	V_{dc}	$700V$
Converter side inductance	L_a, L_b, L_c	$340\mu H$
X–capacitance	C_{xa}, C_{xb}, C_{xc}	$1\mu F$
Y–capacitance	C_{ya}, C_{yb}, C_{yc}	$4.9nF$
Common mode inductance	L_{cm}	$750\mu H$
d–axis set point (peak)	$V^{p}_{d,reference}$	$230\sqrt{2}\,V$
q–axis set point	$V^{p}_{q,reference}$	$0\,V$

Table 2.1 Simulation parameters

The control strategy implemented in the simulation is the modified control as per the current limit control. The voltage controller structure for the three leg is shown by Figure 2.18.

2.5.1. Modeling of choke

As mentioned in subsection 2.1, the leakage inductance of the common mode choke is added at the output of the LC filter. Figure 2.9 shows the model of common mode choke and the dotted line illustrates the path of the leakage flux.

The common mode choke is using a ring core with nanocrystalline material which has very low leakage inductance. To obtain the leakage inductance of the common mode choke, a FEM simulation is done on FEMM 4.2 software.

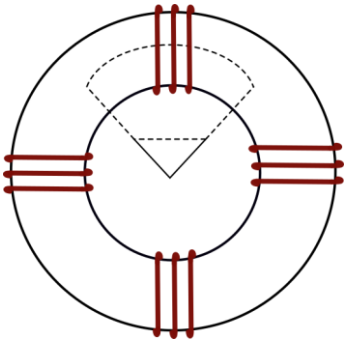

Figure 2.9 Common mode choke and leakage flux path.

The simulation results in Figure 2.10 shows the flux path when only one phase is energized so that the leakage in one phase can be calculated. The green shaded area represents the volume section for the leakage region when only one phase is energized. Based on this region the magnetic field energy is calculated using the software. The magnetic field energy is given by equation (2.10). Based on the magnetic field energy the leakage inductance can be calculated.

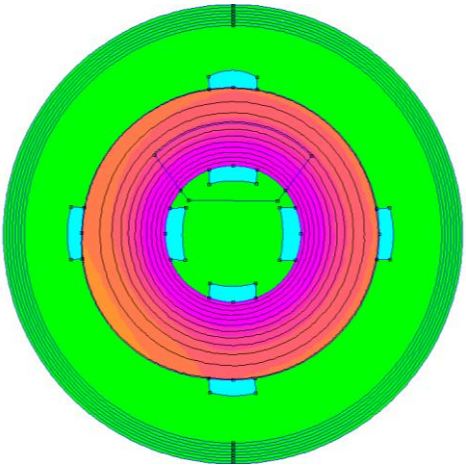

Figure 2.10 FEMM 4.2 simulation results of common mode choke (when only one phase is energized).

$$E = \left(\frac{1}{2}Li^2\right) Joules \tag{2.10}$$

Using this value of leakage inductance, the common mode choke is modeled in PLECS. For magnetic modeling of common mode choke, the magnetic library is used with saturation blocks. The saturation blocks in PLECS use the same data of as mentioned in the datasheet of the common mode choke.

Figure 2.11 shows the PLECS schematic of the common mode choke modeled in PLECS. As the magnetic library of PLECS represent the ideal core and saturation, the leakage inductance can be modeled by adding parallel leakage path.

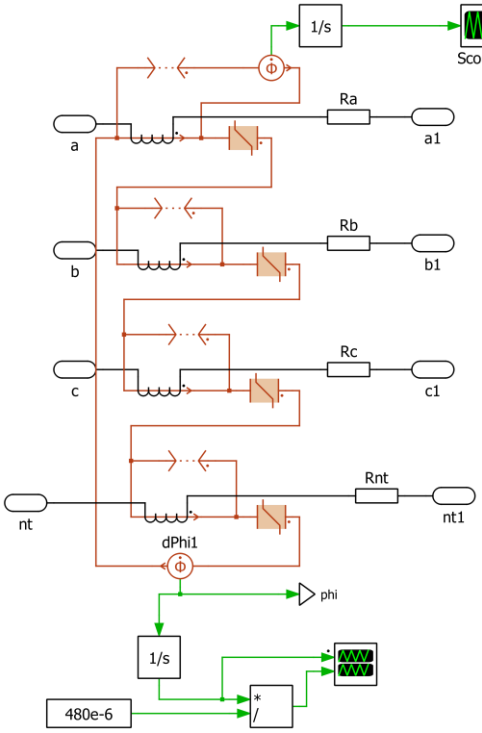

Figure 2.11 Schematic of common mode choke.

2.5.2. Simulation results

This subsection illustrates the various parameters obtained at the end of simulation. The results correspond to the operating parameters mentioned in Table 2.1. For conventional operation i.e., operation under healthy conditions the voltage output of the converter should result in three phase balanced voltages with 230V as RMS value. The voltage and currents are measured after LC filter.

While the current provided by the converter matches the load current demand. The fourth leg controls the DC voltages on the split capacitor at equal values and half of the DC bus voltage. The simulation results are shown in Figure 2.12, Figure 2.13 and Figure 2.14.

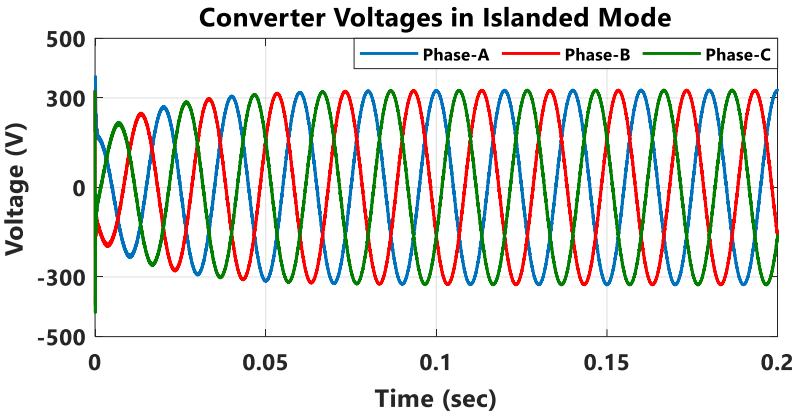

Figure 2.12 Converter output voltages

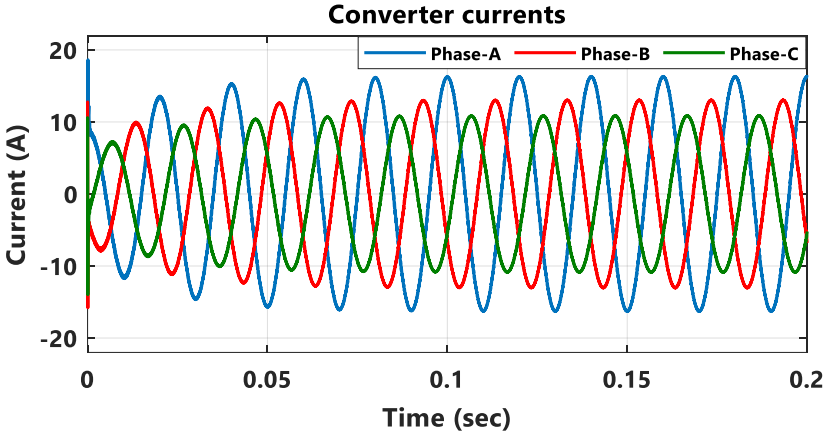

Figure 2.13 Converter output currents

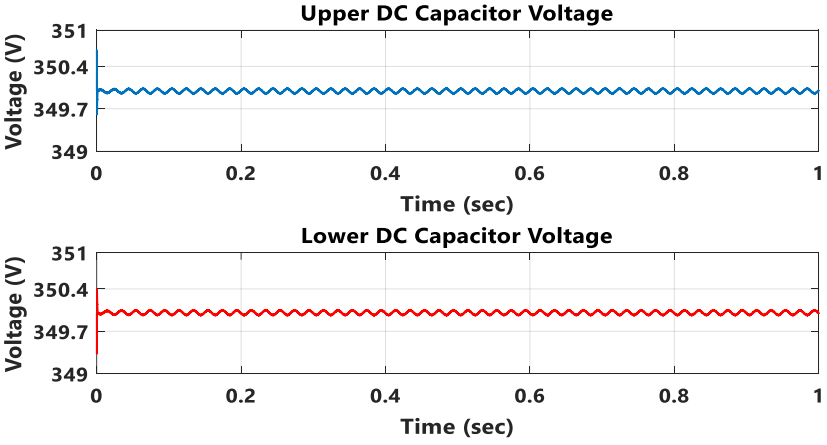

Figure 2.14 DC capacitor voltages.

As discussed in subsection 2.4.1, when the load demand exceeds the current limit of the converter, the modified control is used. Hence, to verify the modified controller operation, the overcurrent scenario is simulated.

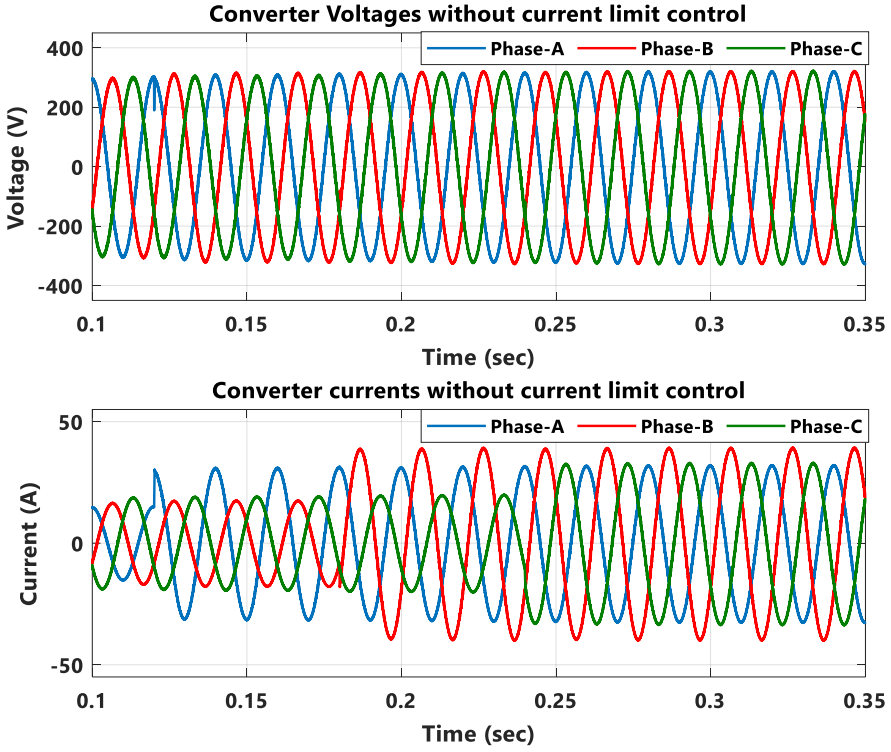

Figure 2.15 Converter voltages and currents without modified control under overcurrent.

As shown in Figure 2.15, the load is increased i.e., current demanded is higher than converter rating for Phase-A at t=0.12 sec, Phase-B at t=0.18 sec and Phase-C at t=0.24 sec and the voltage remain unaffected based on conventional voltage control method. However, the converter will have to provide more current than rated. The results with same load conditions with modified control which limits overcurrent is shown in Figure 2.16.

As seen from Figure 2.16, the voltage of Phase-A decreases when the converter undergoes overcurrent at t=0.12 sec and the same is observed for Phase-B and Phase-C at t= 0.18 sec and t=0.24 sec. It can also be observed that there is negligible drop in the voltage of other two phases even after one phase decreases. Finally, when all the three phases are in overcurrent a reduced balanced voltage system is established. If the overcurrent remains in one/two of the phases, the converter will provide unbalanced voltage at the output.

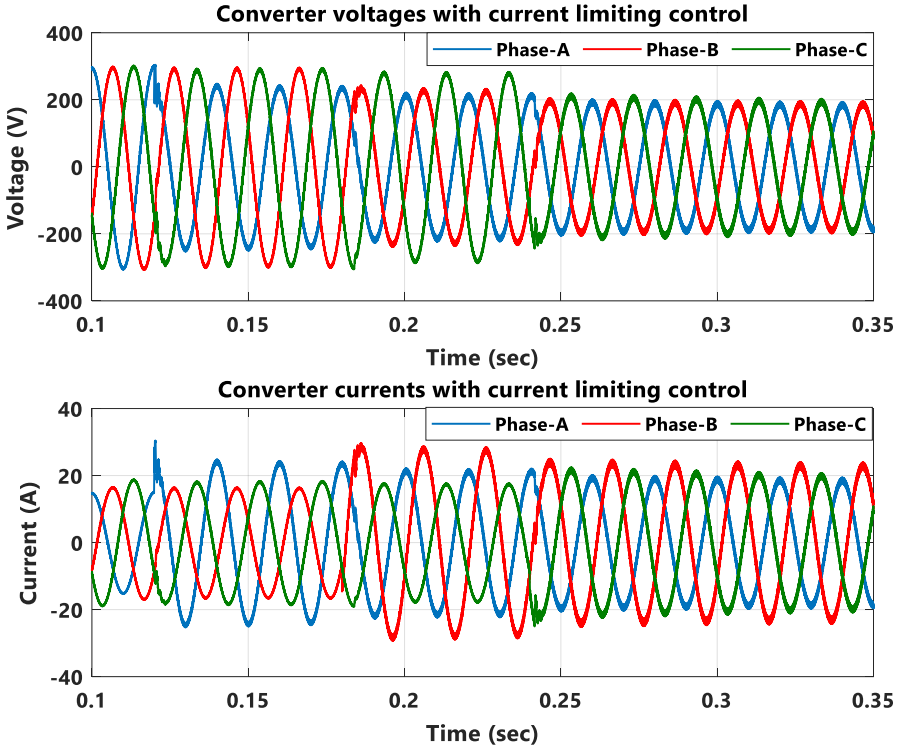

Figure 2.16 Converter voltages and currents with modified control under overcurrent.

2.6. Summary

This chapter discussed about the converter structure and operation under islanded conditions. The schematic of the converter under islanded operation of the converter is explained. Based on the schematic, the conventional voltage control strategy is explained. However, to prevent the converter from overcurrent, a modified controller structure is proposed by injecting a negative sequence to reduce the phase voltages. The control of fourth leg (or the neutral leg) is explained so that a neutral point is balanced, and the unbalanced load is provided with a neutral line.

Further to this the control strategies are simulated in PLECS software to validate the theory. As the existing converter has a common mode choke, a method to model the common mode choke in PLECS has been presented. Also, a FEM simulation is done for the choke to obtain the leakage inductance present per phase which contributes to the structure of LC filter. Finally, the simulation results for the conventional control and modified control are presented and thereby validated.

Chapter-3
Control of Grid Connected Converter

When the converter is connected to the grid as well as the load on the AC side, it is called grid connected operation. In this situation the control of the converter is different as compared to the islanded condition as the specific grid conditions have to be met. Figure 3.1 shows the schematic of the converter operating in grid connected mode. This chapter explains the control of the converter in grid connected condition under unbalanced load conditions.

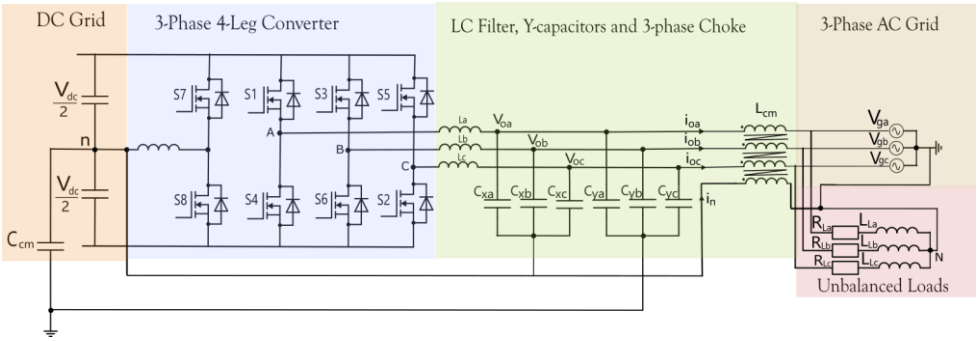

Figure 3.1 Schematic of grid connected converter.

3.1. Symmetric Components

A three phase system can be analyzed by splitting into three sets of sequence components: positive, negative and zero sequence components. As the name suggests the components represent the rotation direction of the phases. For a given three phase system V_a, V_b, V_c the definition of the symmetric components is given below [23].

- Positive Sequence Components: It consists of all the three phasors which are shifted by 120^o and the direction of rotation is positive, as shown in Figure 3.2.
- Negative Sequence Components: It consists of all the three phasors which are shifted by 120^o and the direction of rotation is negative, as shown in Figure 3.2.
- Zero Sequence Components: It consists of all the three phasors with equal magnitudes with zero phase shift, as shown in Figure 3.2.

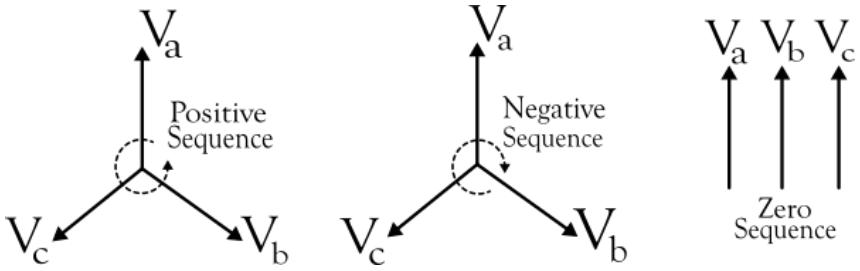

Figure 3.2 Positive, Negative and Zero sequence components.

The equations to obtain the symmetric components for any three phase system is shown by equation (3.1). A balanced three phase system consists of three individual phases of equal amplitude and phase shifted by 120°.

$$V_{pos} = \frac{1}{3}\left[V_a + e^{j\frac{2\pi}{3}}V_b + e^{j\frac{4\pi}{3}}V_c\right]V$$
$$V_{neg} = \frac{1}{3}\left[V_a + e^{j\frac{4\pi}{3}}V_b + e^{j\frac{2\pi}{3}}V_c\right]V \quad (3.1)$$
$$V_{zero} = \frac{1}{3}[V_a + V_b + V_c]\,V$$

Consider a balanced three phase system represented by equation (3.2),

$$V_a = V_{amp}cos(\omega t) = V_{mag}e^{j(\omega t+0)}\,V$$
$$V_b = V_{amp}cos\left(\omega t - \frac{2\pi}{3}\right) = V_{mag}e^{j\left(\omega t-\frac{2\pi}{3}\right)}V \quad (3.2)$$
$$V_c = V_{amp}cos\left(\omega t - \frac{4\pi}{3}\right) = V_{mag}e^{j\left(\omega t-\frac{4\pi}{3}\right)}V$$

If this system is separated into its symmetric components as shown by equation (3.1), the result is shown by equation (3.3).

$$V_{pos} = \frac{1}{3}V_{amp}\,e^{j\omega t}\left[e^{j0} + e^{-j\frac{2\pi}{3}}e^{j\frac{2\pi}{3}} + e^{-j\frac{4\pi}{3}}e^{j\frac{4\pi}{3}}\right] = V_{amp}$$
$$V_{neg} = \frac{1}{3}V_{amp}e^{j\omega t}[e^{j0} + e^{-j\frac{4\pi}{3}}e^{j\frac{4\pi}{3}} + e^{-j\frac{2\pi}{3}}e^{j\frac{2\pi}{3}}] = 0 \quad (3.3)$$
$$V_{zero} = \frac{1}{3}V_{amp}e^{j\omega t}[e^{j0} + e^{-j\frac{2\pi}{3}} + e^{-j\frac{4\pi}{3}}] = 0$$

This shows that for a three phase balanced system, only the positive sequence exists [23]. However, for unbalanced three phase systems this is not the case. The unbalance in three phase system exists because of two reasons: (a) difference in the amplitude of the phases (b) unequal phase difference or the combination of both

(a) and (b). In both the cases of unbalanced three phase systems, the negative and zero sequence components will be non-zero [23], [24], [25].

Note that all these voltages are phase voltage and not line voltages. For line voltages, the zero component i.e., the sum of all voltages will result in zero in both balanced as well as unbalanced system. The consequences of having a balanced and unbalanced three phase system on the control strategy of the converter will be discussed in the following subsection.

3.2. Control strategy

In the grid connected operation, the converter operates in grid supporting mode. The junction at which the converter, the loads and the grid are connected is called the "Point of Common Contact (PCC)." Throughout this report, the grid is considered to be a strong grid i.e., there will be lower instability on the grid itself. Any unbalance considered will be introduced purely by the loads connected at the PCC.

The unbalance in the system can be caused either by voltage or current. In case of balanced three phase systems, it is seen that the negative and zero sequence components resulting in only positive sequence component. For such type of systems, a single PI controller can be used as shown in Figure 3.3. This is the same type of control strategy that is used for voltage control in islanded operation mode as seen in Figure 2.5. However, for unbalanced system, the control strategy is different.

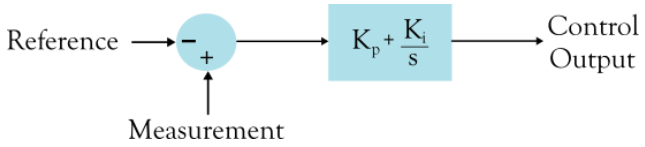

Figure 3.3 Block diagram for implementation of PI controller

In case of islanded operation, the control parameter was the voltage as the operation was of grid formation, but in the grid connected operation, the strong grid provides the reference for the voltage. Other than the criteria for grid synchronization discussed in subsection 1.1.2, the IEEE standards also state that the rms current value should have lower than 5% of total harmonic distortion (THD).

3.2.1. Phase Locked Loop (PLL)

Phase locked loop system is used to track the phase of any signal for obtaining information such as the frequency [26]. The structure of PLL consists of a phase detector, a low pass filter and a voltage control oscillator . The structure of PLL is shown in Figure 3.4. The PLL are categorized into three types [26]:

1. Zero Crossing Detection based PLL
2. Stationary reference frame based PLL
3. Synchronous rotating frame based PLL (SRF-PLL)

Figure 3.4 Block diagram of Phase locked loop system

The methods of zero crossing detection and the stationary reference frame for tracking the phase of a signal is not very accurate especially when the system tends to be frequency fluctuation and voltage unbalanced respectively [26]. The converter has a three phase voltage output which has to be synchronized with the three phases of the LV-grid. Hence, the third method i.e., the SRF-PLL is being used.

3.2.1.1 SRF-PLL

However, some advanced PLL systems are modified in this reference frame. Different PLL structures have been reviewed in papers [27], [28], [29] and tested under different conditions. Based on the [27] the two types which provide optimal performance are SRF-PLL and DDSRF-PLL (Decoupled double synchronous reference frame PLL). Hence, to verify the performance of the PLL on the converter system, these two types of PLL are reviewed in this thesis.

As seen from the equations (2.5) to (2.8), if the voltage on the d-axis is aligned to the peak of the grid voltage and the voltage on q-axis voltage is aligned to zero, the output will result in a three phase balanced system. Hence, the PLL is used to obtain the phase angle and the frequency such that the q-axis is aligned to zero. The block diagram of the SRF- PLL used is shown in Figure 3.5 where ω is the angular frequency and θ is the phase angle. Hence, this replaces the angle input which was provided to the converter operating in islanded mode shown by Figure 2.2.

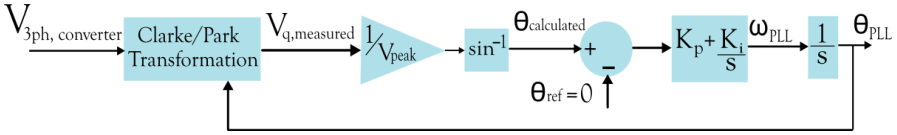

Figure 3.5 Block diagram of SRF-PLL

The three phase voltage output is transformed to synchronous reference frame using the Clarke and Park transform as shown by equations (2.1) and (2.2). After the transformation, the voltage on q-axis can be calculated as shown by equation (3.4).

$$V_q = V_{peak}\, sin(\theta - \theta_{PLL})\, V \tag{3.4}$$

As shown in the block diagram, the inverse sine function calculates the angle which shifts from the reference value (which is zero). The error generated is controlled using a PI controller which then gives the value of the frequency locked with the grid frequency and integrating the frequency gives the phase angle. An important point to note here is that the integrator used for obtaining the phase angle from frequency should be wrapped so that the angle is maintained between 0 to 2π.

3.2.1.2 DDSRF-PLL

As seen from the process of SRF-PLL, the control is focused only on the positive sequence of the three phase transformation. Hence, under unbalanced voltage conditions at the output of the converter the presence of negative sequence will create an impact on the PLL. Hence, due to the negative sequence there is an injection of 100Hz oscillations in the synchronous reference frame quantities of the voltage.

Hence, to obtain a more robust PLL for the operating under unbalanced voltages, a DDSRF-PLL can be used [29]. The DDSRF stands for decoupled double synchronous reference frame control. This can be implemented in a similar way as the SRF-PLL. The difference is the consideration of positive and negative sequence of voltages as opposed to only positive sequence voltages in SRF PLL.

The operation of DDSRF-PLL has already been explained in detail in reference [28]. Hence, from these two types of PLL's it can be expected that the SRF-PLL will be operating optimally under balanced voltage conditions however under unbalanced voltage, the second harmonic oscillations will be present. However, the DDSRF-PLL is more robust against the unbalanced voltages and will eliminate the presence of the oscillations. However, the control complexity persists with this type of PLL.

3.2.1.2 Tuning of PLL

A consideration is made here that a strong grid is present at the output of the converter. This means that there are lower fluctuations on the grid parameters such as the voltage and frequency. Hence, from the two PLL types discussed operating in synchronous reference frame, SRF-PLL is opted for the system. This is primarily based on the less complexity of the PLL. For tuning the PI of the PLL, Symmetrical Optimum (SO) is used as reference as discussed in [30], [31]. The primary equations used to tune the PI are given by equation (3.5) to (3.7). The factor 'α' is called scaling factor. Based on the selection of the damping factor in the range of $\frac{1}{\sqrt{2}}$ to 1, the value of scaling factor is determined and therefore the gains of the control loop are determined based on the delay of the controller i.e., the control frequency represented by T_{swd}.

$$Damping\ Factor = \frac{\alpha - 1}{2} \tag{3.5}$$

$$K_{p,PLL} = \frac{1}{\alpha V_{peak} T_{swd}} \tag{3.6}$$

$$\frac{K_{p,PLL}}{K_{i,PLL}} = \alpha^2 T_{swd} \tag{3.7}$$

3.2.2. Current Control Strategy

Once the PLL is tuned to synchronize with the grid, the angle output can be used to transform the three phase current measurements to synchronous reference frame. The unbalance in the system is caused purely due to the three phase or single phase loads at the PCC. If the unbalance is not removed from the grid, the oscillations at second harmonic will be injected thereby increasing the harmonic content on the grid [32].

To mitigate the unbalance in the grid currents, a double synchronous reference frame (DSRF) current controller is used. In this type of control, the current is separated into positive, negative and zero sequence components and all the symmetric components are independently controlled. Figure 3.2 shows that the positive and negative sequence components rotate in opposite directions.

Hence, if the positive sequence rotates in anti-clockwise direction with an angular frequency of 'ω' then the negative sequence rotates with '$-\omega$.' As the Clarke transform doesn't consider rotation the stationary frame remains common. Hence, the angle used for Park Transform will be 'θ' for positive sequence and '$-\theta$' for negative sequence. This transformation is shown in Figure 3.6.

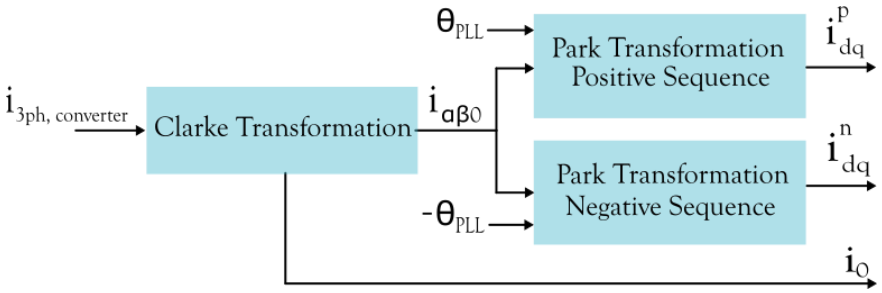

Figure 3.6 Positive and Negative sequence rotation

The positive, negative and zero sequence currents obtained are controlled independently in order to form a close loop system. For the control structure of the synchronous frame currents, the mathematical model of converter has to be analyzed. The KVL applied to the filter inductance on the grid side for three phase system is given by equation (3.8).

$$L_2\begin{bmatrix} di_{fa}/dt \\ di_{fb}/dt \\ di_{fc}/dt \end{bmatrix} = \begin{bmatrix} V_{a,ref} \\ V_{b.ref} \\ V_{c,ref} \end{bmatrix} - R_2\begin{bmatrix} i_{fa} \\ i_{fb} \\ i_{fc} \end{bmatrix} - \begin{bmatrix} V_{ga} \\ V_{gb} \\ V_{gc} \end{bmatrix} \tag{3.8}$$

Where, "$i_{fa,b,c}$" represents the grid side currents. The space vector transformation i.e., another representation of Clarke transformation is given by equation (3.9).

$$\vec{\imath}(t) = \frac{2}{3}\left[i_{fa}e^{j0} + i_{fb}e^{j\frac{2\pi}{3}} + i_{fc}e^{j\frac{4\pi}{3}}\right]A \tag{3.9}$$

Hence, multiplying equation of Phase-A with e^{j0}, Phase-B with $e^{j\frac{2\pi}{3}}$ and Phase-C with $e^{j\frac{4\pi}{3}}$ and adding will result in the space vector equations. The space vector equation is given in equation (3.10).

$$L_2\begin{bmatrix} \dfrac{di_{f\alpha}}{dt} \\ \dfrac{di_{f\beta}}{dt} \end{bmatrix} = \begin{bmatrix} V_{\alpha,ref} \\ V_{\beta,ref} \end{bmatrix} - R_2\begin{bmatrix} i_{f\alpha} \\ i_{f\beta} \end{bmatrix} - \begin{bmatrix} V_{g\alpha} \\ V_{g\beta} \end{bmatrix} \tag{3.10}$$

When equation (3.10) is transformed to synchronous reference frame, a cross coupling component is introduced. The KVL equations in synchronous reference frame for positive sequence is given by equation (3.11). The superscript 'P' refers to the parameters in the positive sequence.

$$L_2\begin{bmatrix} \dfrac{di_{fd}^P}{dt} \\ \dfrac{di_{fq}^P}{dt} \end{bmatrix} = \begin{bmatrix} V_{d,ref}^P \\ V_{q,ref}^P \end{bmatrix} - R_2\begin{bmatrix} i_{fd}^P \\ i_{fq}^P \end{bmatrix} - \omega L_2\begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix}\begin{bmatrix} i_{fd}^P \\ i_{fq}^P \end{bmatrix} - \begin{bmatrix} V_{gd}^P \\ V_{gq}^P \end{bmatrix} \tag{3.11}$$

However, for transformation of equation (3.10) to synchronous frame of negative sequence, the inverse Park transformation matrix changes as shown in equation (3.12).

$$\begin{bmatrix} i_{f\alpha} \\ i_{f\beta} \end{bmatrix} = \begin{bmatrix} cos(-\theta) & -sin(-\theta) \\ sin(-\theta) & cos(-\theta) \end{bmatrix}\begin{bmatrix} i_{fd} \\ i_{fq} \end{bmatrix} \tag{3.12}$$

This results in the addition of rotational component as opposed to the positive sequence which when transformed to synchronous reference frame cancels the rotational component. The final KVL equation for negative sequence currents in synchronous reference frame is obtained as shown in equation (3.13). Note that the value of angular frequency should be taken positive as the negative rotation has already been accounted in the rotational matrix. The superscript 'N' on the parameters represents the negative sequence.

$$L_2\begin{bmatrix}\frac{di_{fd}^N}{dt}\\ \frac{di_{fq}^N}{dt}\end{bmatrix} = \begin{bmatrix}V_{d,ref}^N\\ V_{q,ref}^N\end{bmatrix} - R_2\begin{bmatrix}i_{fd}^N\\ i_{fq}^N\end{bmatrix} + \omega L_2\begin{bmatrix}sin(2\theta) & -cos(2\theta)\\ cos(2\theta) & sin(2\theta)\end{bmatrix}\begin{bmatrix}i_{fd}^N\\ i_{fq}^N\end{bmatrix} - \begin{bmatrix}V_{gd}^N\\ V_{gq}^N\end{bmatrix} \quad (3.13)$$

As seen from equation (3.13) the cross coupling component has twice the phase angle i.e., '2θ' because of the rotation in opposite direction. Hence, the synchronous component values in negative sequence will oscillate at twice the frequency (100Hz). Hence, a low pass filter is used in this case to suppress this effect.

Based on equations (3.11) and (3.13), the structure of positive and negative sequence current controller is obtained. The block diagram of the positive and

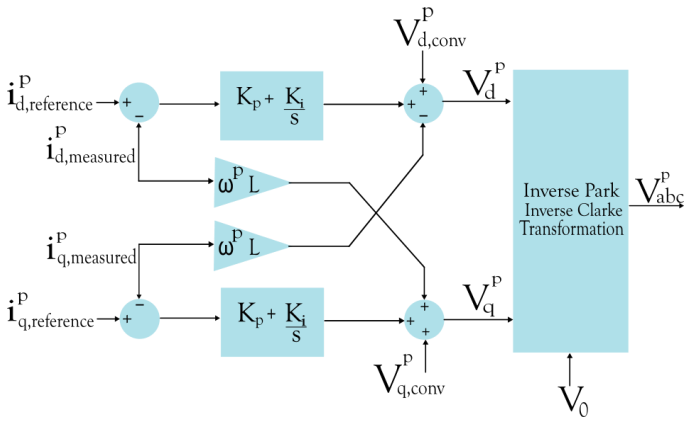

Figure 3.7 Positive Sequence Current controller

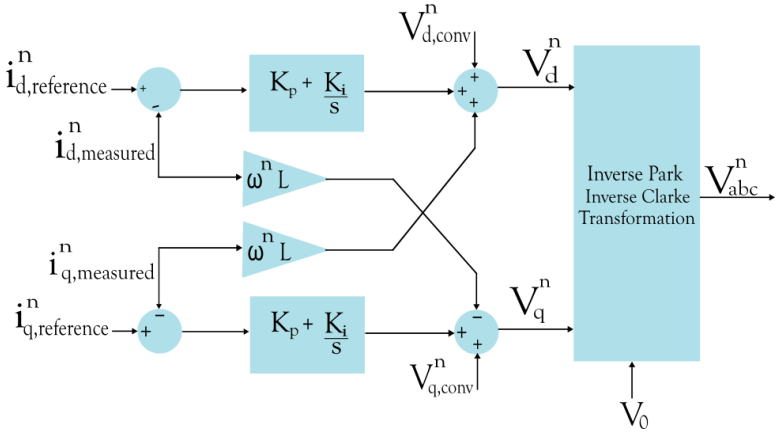

Figure 3.8 Negative Sequence Current controller

negative sequence current controllers is shown in Figure 3.7 and Figure 3.8 respectively.

The DSRF current control strategy aims at controlling the positive sequence, negative sequence and the zero sequence currents. As mentioned in the subsection 3.1, the zero sequence represents the summation of all the three phases without any phase shift. Hence, in case of any phase unbalance this component is not zero. Hence, the zero sequence controller implemented in this control strategy also gives an additional degree of freedom to control the amount of unbalance that can be provided by the converter.

One of the cases of unbalance mitigation is considered in the simulation. As the grid connected converter is also operating with unbalanced AC loads the converter has an added functionality of replicating the unbalance currents thereby resulting in balanced grid currents. Hence, the zero control is shown in Figure 3.9.

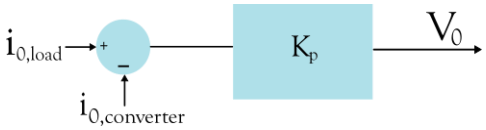

Figure 3.9 Zero sequence controller

Another important consideration here is that the zero sequence component is obtained in the stationary reference frame (or αβ reference frame) hence the ideal controller for such type of signals is the PR controller. However, as the function of the zero sequence control is to replicate the unbalance on the load hence the P-control (proportional control) is sufficient.

3.2.3. Reference Current Generator

The controllers in positive, negative and zero sequence require a reference based on which the power injection, balance/unbalance of the converter is determined. For obtaining the reference currents, the reference current generator is used. The subsection 3.2.2 discusses in detail about the DSRF current control strategy. As seen from the control block diagrams in Figure 3.7, Figure 3.8 and Figure 3.9 the measured converter current has to align with the reference current. This subsection discusses about different reference current generators for the current controllers.

As the converter is operating for mitigating the unbalance on the AC loads, the negative sequence and the zero sequence controller will have reference currents as the negative sequence and zero sequence load currents respectively. If the converter aligns with the unbalance demanded by the load, the grid current will remain stable as per the KCL at the PCC. For the positive sequence controller two types of reference current generator are discussed.

1. Power based reference current generator

2. DC link voltage based reference current generator

3.2.3.1 Power based reference current generator

For three phase systems it is important to achieve the currents based on the active power injection from the converter to the AC loads. Hence, the power based current reference generator operates based on the amount of power to be injected or received to/from the AC side. As the reference current values required by the controllers exist in synchronous frame it is important to represent the active and reactive power in synchronous reference frame.

The active and reactive power can be represented in the form of fundamental and the second harmonic components. Due to the presence of unbalance in the three phase currents, the synchronous frame will have oscillations. Therefore, the oscillations in current will lead to oscillations in power. The active/reactive power equations are given by equations (3.14) and (3.15).

$$P = P_0 + P_2 \cos(2\omega t) + P_2 \sin(2\omega t) \tag{3.14}$$

$$Q = Q_0 + Q_2 \cos(2\omega t) + Q_2 \sin(2\omega t) \tag{3.15}$$

However, for the reference current generator, the reactive current (i.e., the q-axis current) and second harmonic components should be zero. Hence, the reference current can be generated using the fundamental component of active power. The active power in synchronous reference frame can be given by equations (3.16) and (3.17).

$$P = \frac{3}{2}[V_d i_d + V_q i_q] \tag{3.16}$$

$$Q = \frac{3}{2}[V_q i_d - V_d i_q] \tag{3.17}$$

There is a degree of freedom to decide how much power needs to be injected or drawn which further determines the reference current. This allows to operate the converter at different power levels with the same DC link voltage within the limits of the converter ratings. The power based reference current generator block diagram is shown in Figure 3.10.

However, this type of reference current generator has a drawback. This method introduces practical challenges related to the measurement of power demanded by the load. This method can either be based on user defined parameters for active power or it will require additional measurement for determining the load power demand.

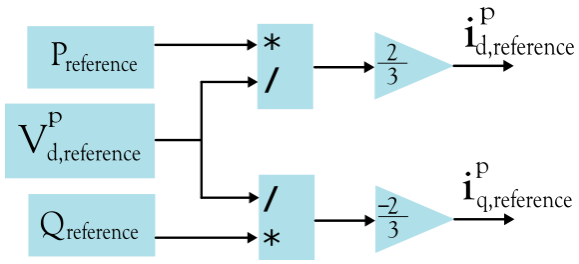

Figure 3.10 Power based reference current generator

3.2.3.2 DC link voltage based reference current generator

The DC link voltage based reference current generator establishes a relation between the DC link voltage and the d-axis positive sequence current. This relation is bounded by the power rating of the converter at the maximum and minimum converter ratings. Figure 3.11 shows the relation that has been established with the DC link voltage and the d-axis current.

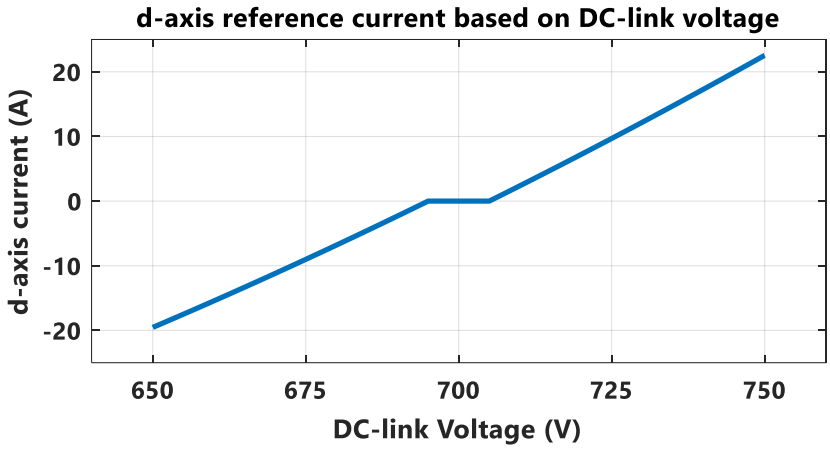

Figure 3.11 DC link voltage based reference current generator

With this type of reference current generator, the measurement issue existing in power based current generator is eliminated. As seen from the figure above, the bidirectional operation of the converter can be easily defined by applying conditions on the DC side voltages. For the fourth leg control of the converter, the measurement of DC split capacitors is already present thereby eliminating the requirement of additional measurement devices.

Also, with this type of reference current generator, the converter can operate at zero power injection at certain voltage. In this mode the unbalance is circulated through the converter while the grid provides balanced currents to the load.

3.2.4. Control of Fourth Leg

The control for the fourth leg i.e., the neutral leg is already discussed in subsection 2.4.2 using voltage control. As the DC grid side is the same, the same controller structure can also be implemented for grid connected inverter however it has been observed that the ripple in the output of the voltage is higher than expected. Hence, this control is modified by adding a current based control along with the voltage control on the fourth leg [21]. The purpose of adding the current control is to lower the ripple on the pole voltages. As this concerns addition of the current measurement, the comparison of voltage and voltage–current control is shown in subsection 5.4.1 of Chapter–5.

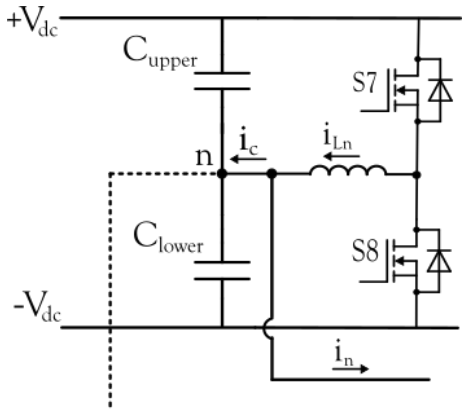

Figure 3.12 Neutral leg control for grid connected operation.

Figure 3.12 shows the neutral leg connection with the DC grid. For the modified control of the fourth leg, the current through the neutral inductor "i_{Ln}" is controlled to the current flowing through the neutral wire. Under ideal operations if both these currents are equal, there will be no oscillations of the neutral point "n." However, due to the unbalanced currents on the load side the oscillations are introduced and therefore the control is modified. The modified control structure is shown in Figure 3.13.

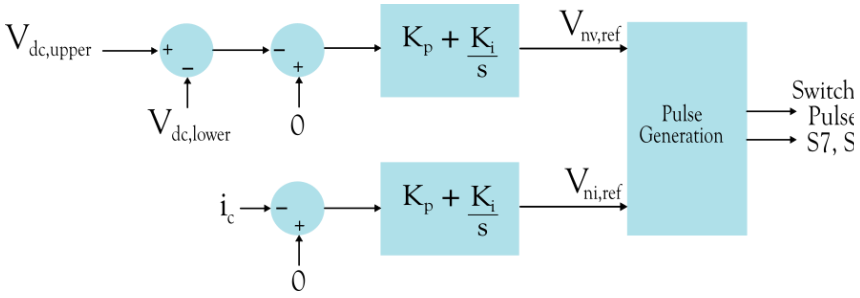

Figure 3.13 Control block diagram for neutral leg.

3.3. Simulation Results

The control strategy discussed in this chapter is simulated for the three-leg four-wire topology in PLECS and the simulation results are analyzed. The operation of PLL is ensured if by observing the frequency and the angle output. Further, the voltage at the PCC is observed for the amplitude and phase sequence. The THD is also noted for the phases to ensure the grid codes. As stated in 3.2.3, the DC link based current generator is used which divides the operation in three different modes. The three different modes with their corresponding voltage at which converter is simulated are mentioned in Table 3.1.

Mode of operation	DC voltage levels
Three-phase grid and converter providing power to AC loads.	$750V$
AC Grid provides power to the load as well as the DC Grid.	$650V$
Zero power injection in which grid currents are balanced and there is no power injected by the DC grid to the load.	$700V$

Table 3.1 Modes of operation and the corresponding DC voltage used in simulation.

The primary observation to be made in the three phase currents is the mitigation of unbalance on the loads and balanced grid currents under all three operations. For the zero power injection operation, the converter mitigates the unbalance and does not provide any active power to the load. Figure 3.14 shows the output of the PLL in terms of the frequency and the reference angle (which is later used for axes transformation). As seen from the simulation results the frequency is maintained at 314.15 rad/sec (which corresponds to 50Hz) and the angle is wrapped in the range of 0 to 2π.

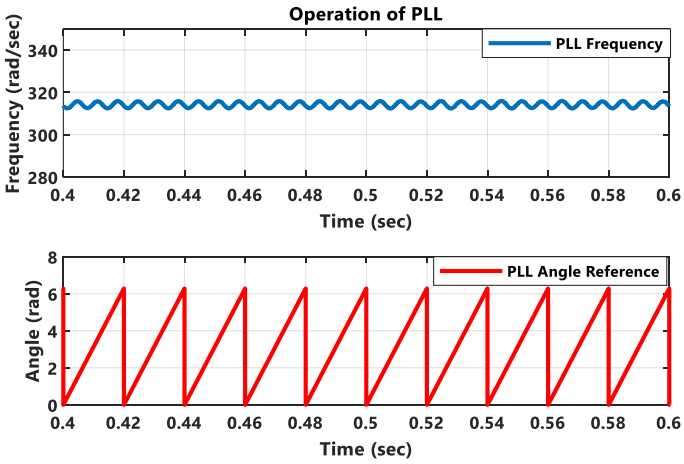

Figure 3.14 Output of PLL

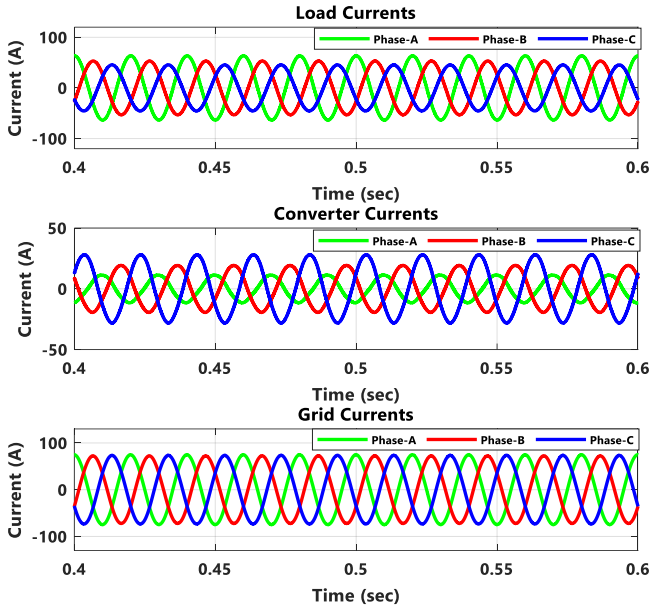

Figure 3.16 Currents in case of grid providing power to the loads and converter

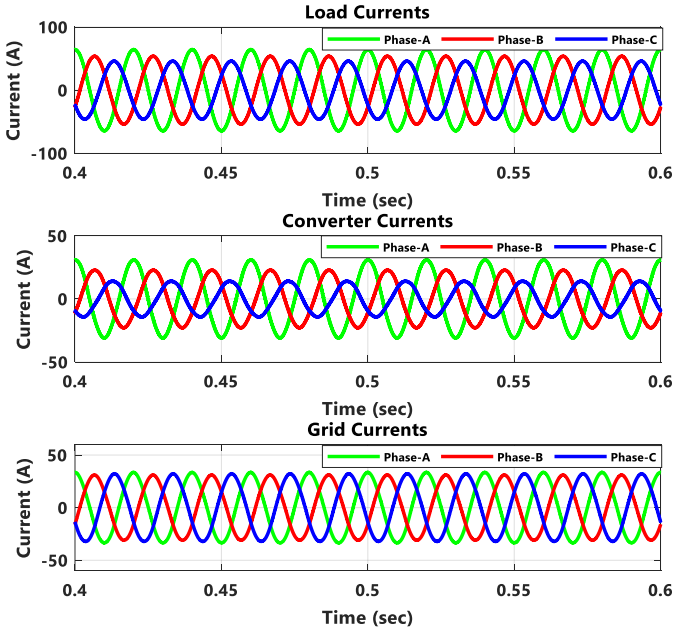

Figure 3.15 Currents in case of converter and grid providing power to the loads.

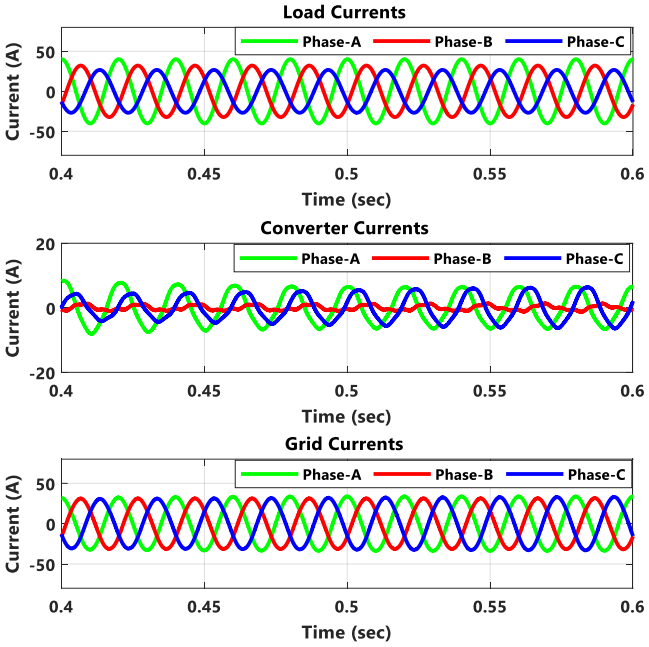

Figure 3.18 Currents in case of zero power injection by converter and grid providing power to converter.

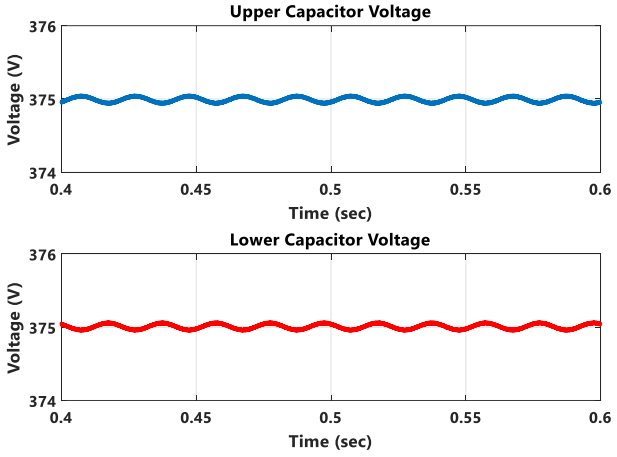

Figure 3.17 DC capacitor voltages with fourth leg control.

As seen from the results of the simulation, for all three operations, the converter is able to mitigate the unbalance currents demanded by the loads and thereby making the grid currents balanced. Figure 3.15 shows the situation where the DC grid as well as the AC grid provide currents to the AC loads. It can be observed that the corresponding phase of the converter currents, grid currents and the load currents are the same. Hence, this represents that the DC grid is injecting active

power i.e., providing current to the AC loads. Considering this point, Figure 3.16 represents opposite phase of the converter currents while grid currents and load currents are in the same phase. Hence, it can be stated that the DC grid demands current from the AC grid while the grid also provides currents to the AC loads.

Figure 3.18 shows that the converter is only responsible for mitigating the unbalance on the grid currents. The phase currents depend on the amount of unbalance demanded by the AC loads. Simultaneously the fourth leg controls the neutral point such that the voltages are balanced across the positive and negative pole. To ensure the control strategy complies to the requirement of the grid side currents of the converter being under 5% an observation for each phase current is summarized in Table 3.2.

Phase	**THD** (%)
Phase–A	2.05%
Phase–B	2.72%
Phase–C	4.25%

Table 3.2 THD value of grid side currents of the converter.

3.4. Summary

In this chapter, the symmetric components are analyzed for three phase systems. The need of PLL and different types of PLL are explained for the grid connected system. Further, the double synchronous reference frame (DSRF) current control strategy is explained for the grid connected operation. The control strategy is analyzed based on the symmetric components. Next to this, two different types of reference current generators are explained which are relevant to the operation. The DC link based current generator is selected for the operation which provides the positive sequence reference currents for the current controller. Finally, the modified control for the fourth leg is explained by adding the current controller in parallel to the voltage control for balancing the pole voltages.

The final subsection presents the simulation results for the system for validating the proposed control strategy for the converter. Based on the simulation results it can be concluded that the selection of SRF-PLL is providing a satisfactory operation by locking the converter to 50Hz frequency. From the current control operation, it can be concluded that the converter is able to balance the currents on the grid while compensating for the unbalance within the maximum limits of the converter for all the three different operations of the converter. Finally, the results of the voltage on the split capacitors by controlling the fourth leg is shown. As seen from the phase current THD values, the control strategy complies to the grid code of having THD value less than 5%.

Chapter-4
Reduction of Common Mode Voltage

Till now, the control of converter under islanded and grid connected operations were discussed. However, in these chapters the information about the modulation technique was not presented. In this chapter different modulation techniques have been analyzed and the criteria for the selection has been presented.

Before discussing the theory behind the different modulation techniques, an important factor for the system under analysis is discussed, which is common mode voltage and current. The power converters when grounded have a potential difference of their neutral with respect to the ground voltage (i.e., absolute zero). This results in the presence of "Common Mode Voltage (CMV)" and due to the impedance in the path of the grounding, a "Common Mode Current (CMC)" flows from the power converter to the ground.

If the DC/AC converter is left in an ungrounded condition, during ground to pole faults, although the current would be zero but the voltage on healthy pole would reach twice the voltage [33], [34]. This chapter discusses the different types of grounding, the type of grounding employed for the DC/AC converter, the standards which are applicable for common mode voltages and currents. Further, a comparison is made between different modulation techniques which are used to reduce CMV and a criterion for selection is made as per which the different modulation techniques are classified.

4.1. Grounding of DC/AC Converter

In the DC/AC converter for grid connected operation, the grounding is done from the AC grid side as well as the DC side. The AC side grounding is generally done at the substation from where the LV distribution grid is connected. However, the DC side of the converter is considered to be a DC grid as shown in Figure 4.1.

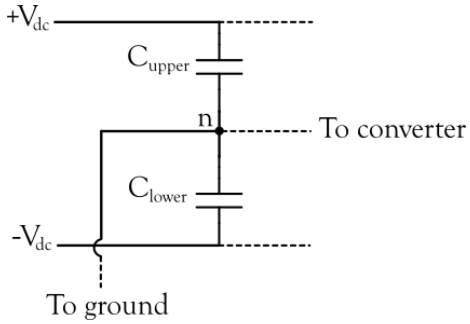

Figure 4.1 DC grid side of the DC/AC Converter.

The neutral point 'n' is the neutral of the DC grid which is connected to the ground.

There are three different ways to ground a DC grid which are briefly explained in [33] and they are summarized below:

1. **Solid grounding:** The point neutral point 'n' is connected to the ground through a conducting wire (i.e., no additional impedance). With this type of grounding, in fault conditions the neutral point remains stable thereby maintaining the stability of the pole voltages. However, the currents entering the ground will be very high due to very low impedance offered by the conductors connecting the neutral to the ground.

2. **Low impedance grounding:** The neutral point 'n' is connected to the ground through a small impedance. The purpose of this impedance is to maintain the voltage at the neutral point to be as close as possible to the ground potential but also limiting the fault currents to some extent. However, with this type of grounding, the fault currents are still higher but lower as compared to solid grounding.

3. **High impedance grounding:** The neutral point 'n' is connected to the ground through very high impedance with the primary objective of limiting the fault currents entering the ground. However, in this case the pole voltages tend to shift higher as compared to the solid grounding and low impedance grounding.

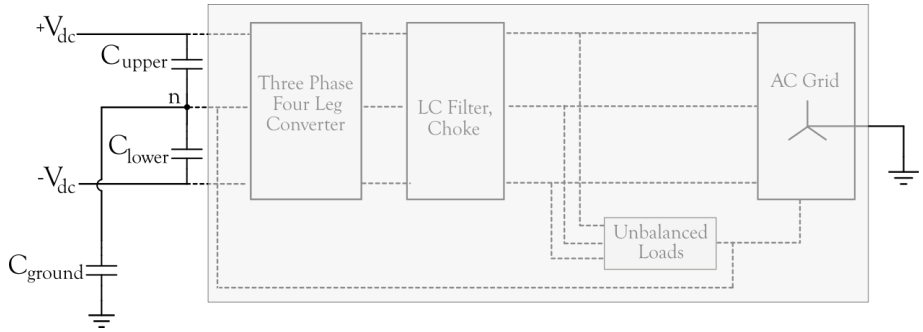

Figure 4.2 Grounding of DC/AC Converter.

From the above mentioned types of grounding, the DC/AC converter is considered to have low impedance grounding. In the low impedance grounding, the DC/AC converter is employing capacitive grounding. This consideration is based on the implementation of the DC protection system which employs a capacitive grounding. The grounding of the converter on DC side and the AC side is shown in Figure 4.2. The DC protection system is not in the scope of this thesis.

The behavior of capacitor is to act as open circuit for DC while short circuit for AC. As the converter has neutral point short circuited with the AC side, the neutral point 'n' tends to oscillate. In this situation, the DC offset will be completely blocked by the capacitor and no DC current will enter the ground, but the AC currents will not be blocked by capacitor.

For limiting the currents under fault conditions, a parallel circuit is implemented to the capacitor. However, it is important to note that in this report, only healthy operating conditions are discussed i.e., fault conditions are not considered. Under normal operating conditions, higher capacitance value results in lower impedance as per equation (4.1). For the DC/AC converter the grounding capacitor is set at a value of 50μF.

$$|Z_{cap}| = \left(\frac{1}{2\pi f C_{ground}}\right) \Omega \tag{4.1}$$

This subsection concludes that there is a very high impact of the capacitance value on the common mode voltage and currents. Hence, before addressing the issue of reducing the common mode quantities, it is important to understand the effects of common mode and the standards concerning this problem. The subsequent subsection discusses the standards for CMV and CMC.

4.2. Standards for CMV and CMC

The different type of grounding system results in different common mode voltage and currents. The common mode quantities also dependent on the converter ratings such as the topology, the switching frequency, power ratings. Hence, it is important to understand the standards which should be followed for operating the converter.

The IEC 60479-1 summarizes the effects of alternating currents of various frequencies on the human body. The different effects on human body mark the limits for the common mode currents. The effects are summarized as follows [33], [35]:

1. **Perception Threshold:** The limit of the current where a minor prickling sensation are felt by the test subjects defines the perception threshold.
2. **Let-go Threshold:** The limit of current where the test subjects lose control of muscle while holding on to electrode (i.e., cannot "let-go" of the charged electrode) defines the Let-go threshold.
3. **Ventricular Fibrillation Threshold:** The limit of current where the test subject experiences ventricular fibrillation i.e., the heartbeat becomes irregular defines the Ventricular Fibrillation Threshold.

As per the Clause-5 of IEEE 60479-1, the threshold current values for the three different effects are mentioned in Table 4.1 [35]. Although this table only mentions

values till 150Hz, it is important to understand what happens to the current thresholds at higher frequencies. The reason to understand this is that the power converters operate at a higher frequency range (in order of kHz; 50kHz for the DC/AC converter) which makes the neutral point oscillate at a higher frequency. This will give rise to currents of higher frequency which cannot be blocked by the grounding capacitor.

Effect	Current threshold values (mA)	
	AC (15 to 150Hz)	DC
Perception threshold	0.5	2
Let-go threshold	5	-
Ventricular fibrillation	30	150

Table 4.1 Current threshold values based on the three effects on test subjects.

Residual current device (RCD) is a safety equipment which acts as a circuit breaker to detect and trip in case of higher residual currents. The RCD is tuned as per the current thresholds based on different frequencies in order to trip accurately. For example, if a 30mA alternating current at 50Hz flows continuously through a human body for more than 300ms, it can result in misfunctioning of cardiac systems [36]. Therefore, the limits of RCD are determined such that it can trip to avoid such incidents.

However, at higher frequencies this value is different. For the DC/AC converter system RCD of Type-B will be used. The Type-B RCD detects alternating sinusoidal currents, pulsed direct currents, direct currents (DC) and is recommended to connect with the PV converters where no other protection against DC fault currents for above 6mA is provided [36].

As the frequency of the current increases the current threshold limit increases [35]. This can be explained by a factor which is termed as "Frequency Factor." Hence, the negligence of frequency factor in current threshold will result in unwanted tripping of RCD's [36]. The IEC 60479-1 [35] mentions the effect of higher frequency on the current threshold values and it has been summarized in tabular form in [36] as shown in Table 4.2.

Frequency (Hz)	100	200	300	400	500	600
Frequency Factor	1.5	2.0	4.5	5.8	7.0	9.2
Current Threshold (mA)	45	60	135	174	210	276

Table 4.2 Frequency range with corresponding frequency factor and current threshold values as defined in IEC 60479-1.

Therefore, the standards defined in IEC60479 and the tripping of RCD's provide a limit of the common mode parameters under which the DC/AC converter should be operated. It has to be noted that even if the ratings of RCD increase with the frequency, the current spikes (just near to avoid tripping of RCD's) can also cause damage. Hence, the objective is not just to have lower magnitude at lower frequencies but also decrease the higher frequency components.

4.3. Common Mode in DC/AC converter

During the operation of three phase converter, the instantaneous sum of all the three phase voltages is not zero at all times even if the voltages are balanced. This is the primary reason for the existence of common mode voltage. The common mode voltage can be given by the equation (4.2).

$$V_{cm} = \frac{V_a + V_b + V_c}{3} \tag{4.2}$$

The most common methods to reduce common mode voltage include using a CM transformer and a CM choke (which is a high impedance common mode filter). However, using these methods to reduce common mode results in high cost, higher space utilization of the converter. Also, as mentioned the presence of common mode voltage is due to the non-zero summation of the individual phases which represents asymmetry and hence passive devices such as transformers and a CM choke will not be able to filter the CM component to a very high extent [37].

To avoid these limitations of passive reduction of common mode, different modulation techniques are implemented, and they are called "Reduced Common Mode Voltage Pulse Width Modulation (RCMV- PWM)" techniques. The different modulation techniques (conventional and RCMV-PWM) are explained in this subsection.

4.3.1. Sine Pulse Width Modulation (SPWM)

The SPWM technique is implemented individually on three phases. SPWM consists of three modulation waves for the three legs of the converter (i.e., phase-A,

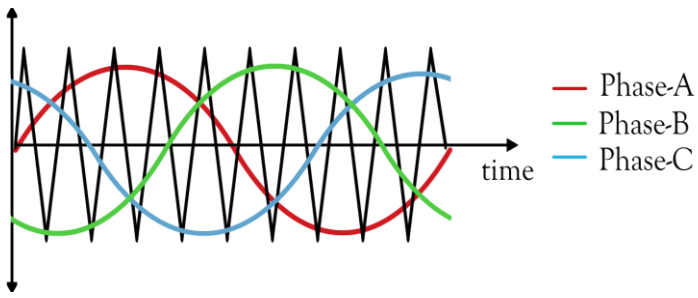

Figure 4.3 Modulation waves and carrier wave for SPWM.

phase-B, and phase-C) and one triangular carrier wave. The three sinusoidal waves are superimposed on the carrier wave as shown in Figure 4.3. The intersection of the sinusoidal modulation wave with the triangular carrier wave marks the switching of the respective phase. The SPWM switching is shown in Figure 4.4.

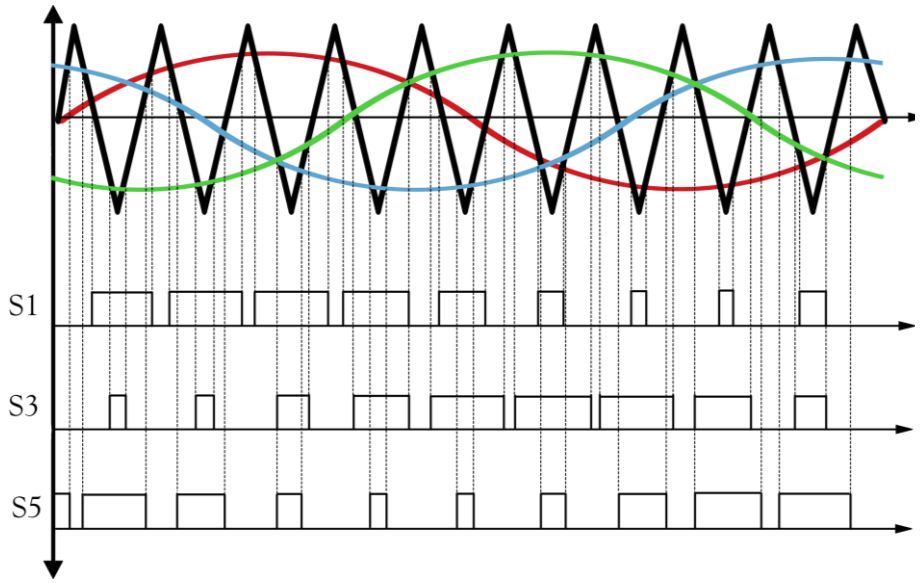

Figure 4.4 SPWM and the corresponding switching. (**Figure is not to scale)*

The switching in Figure 4.4 shows the switching for the upper switches for each leg. The lower switches (i.e., S_4, S_6, S_2) operate complementary to the upper switches. As seen, there are certain switching times where none of the upper switches are operating which means there is a zero switching state created and all the lower switches are ON. Hence, due to these instances, the common mode exists in three-phase converters with SPWM technique.

As observed from the switching, the zero states are created near to the peaks of the carrier wave. There are multiple methods to modify the SPWM technique in a way that can reduce the common mode such as "phase-shifted SPWM," "jump-edge delay control strategy," "pulse delay control strategy," and "shortest interval state exchange control strategy." Reference [37] discusses these techniques to reduce the common mode voltage in a three phase converter.

4.3.2. Phase-Shifted SPWM

As mentioned in 4.3.2, the SPWM can be modified in order to reduce the time which causes the common mode voltage. The simplest way to achieve this is to use phase-shifted carrier waves. In this modulation technique each modulation wave (corresponding to each of the phases) will have a corresponding carrier wave.

Hence, there will be three triangular carrier waves which will be 120° phase shifted from each other. By phase shifting the carrier wave, the peaks of the carrier wave are displaced by 120° which results in reduced time intervals during which all the upper switches are completely on or off.

4.3.3. Space Vector Modulation (SVM)

The switching states i.e., ON and OFF can be defined for each switch as given by equation (4.3). As the switching action is complementary the lower switches will be off when the upper switches are in on state. For space vector modulation with six switches, 6 vector states are defined on a plane (V_1 to V_6) which demarcates the division of the plane into six equal sectors (A_1 to A_6), thereby forming a hexagon. The plane of space vector modulation is shown in Figure 4.5.

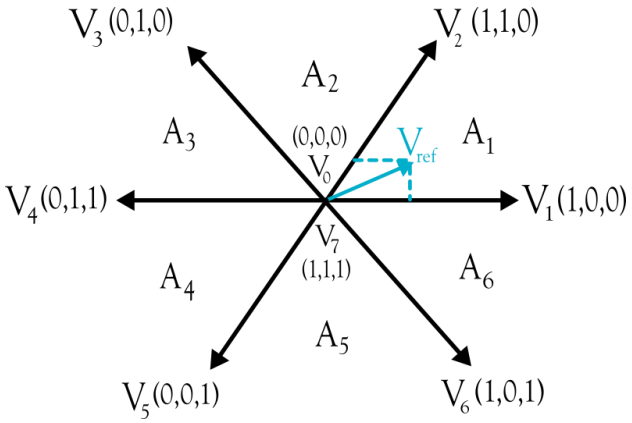

Figure 4.5 Conventional Space Vector Modulation (SVM) for sector-1

ON state of upper switch k: $S_k = 1$; k =1,3,5

OFF state of Switch k: $S_k = 0$; k =1,3,5 (4.3)

A reference voltage is generated in the stationary reference frame (i.e., αβ reference frame) which rotates through this plane. The α-component and β component of the reference voltage are aligned with the vector states and the time duration spent on these vector states defines the duty cycle as shown in Figure 4.5.

The calculation of time duration of the reference voltage components on the vector states for sector-1 can be given by equation (4.4).

$$V_{ref}T_{sw} = V_1T_1 + V_2T_2 + \left(V_0\frac{T_0}{2} + V_7\frac{T_0}{2}\right) \quad (4.4)$$

As the zero vector represents zero voltage the last term of equation (4.4) can be neglected. This equation can be further expanded to equation (4.5) and (4.6).

$$\begin{bmatrix} V_{\alpha,ref} \\ V_{\beta,ref} \end{bmatrix} T_{sw} = \frac{2}{3} V_{dc} \begin{bmatrix} 1 \\ 0 \end{bmatrix} T_1 + \frac{2}{3} V_{dc} \begin{bmatrix} cos60^o \\ sin60^o \end{bmatrix} T_2 \tag{4.5}$$

$$T_0 = T_{sw} - T_1 - T_2 \tag{4.6}$$

This calculation can be extended to all the sectors and the generalized equation can be presented for all the sectors as shown by equation (4.7).

$$\begin{aligned} T_{odd} &= \frac{\sqrt{3} V_{ref}}{V_{dc}} sin(60^o - \varphi) \\ T_{even} &= \frac{\sqrt{3} V_{ref}}{V_{dc}} sin(\varphi) \end{aligned} \tag{4.7}$$

where,

$$V_{ref} = \sqrt{V_\alpha^2 + V_\beta^2}\, V \tag{4.8}$$

$$tan\varphi = \frac{V_\alpha}{V_\beta};\ \ \varphi \in [0, 60^o] \tag{4.9}$$

As there are 6 sectors and the fundamental frequency of the sine wave is 50Hz, the reference vector is present in each sector for 300Hz. Equation (4.6) represents that the total of all the time duration in one cycle is equal to the switching time. Hence, the number of switching cycles in one sector can be calculated as 300Hz*Ts.

The duty cycle for the switches for all sectors is shown in Figure 4.6. The switching sequence for SVM is given in Table 4.3. As observed, the transition from one sector to other sector involves switching of only one switch to reduce the losses. In this type of modulation, the advantage is more utilization of the DC link voltage by 15% more than the SPWM techniques. This is achieved by using the third harmonic in the sinusoidal wave.

Sector	Switching sequence of Vectors
A_1	$V_7 \rightarrow V_2 \rightarrow V_1 \rightarrow V_0 \rightarrow V_1 \rightarrow V_2 \rightarrow V_7$
A_2	$V_7 \rightarrow V_2 \rightarrow V_3 \rightarrow V_0 \rightarrow V_3 \rightarrow V_2 \rightarrow V_7$
A_3	$V_7 \rightarrow V_4 \rightarrow V_3 \rightarrow V_0 \rightarrow V_3 \rightarrow V_4 \rightarrow V_7$
A_4	$V_7 \rightarrow V_4 \rightarrow V_5 \rightarrow V_0 \rightarrow V_5 \rightarrow V_4 \rightarrow V_7$
A_5	$V_7 \rightarrow V_5 \rightarrow V_6 \rightarrow V_0 \rightarrow V_6 \rightarrow V_5 \rightarrow V_7$
A_6	$V_7 \rightarrow V_6 \rightarrow V_1 \rightarrow V_0 \rightarrow V_1 \rightarrow V_6 \rightarrow V_7$

Table 4.3 Switching sequence of SVM in all sectors.

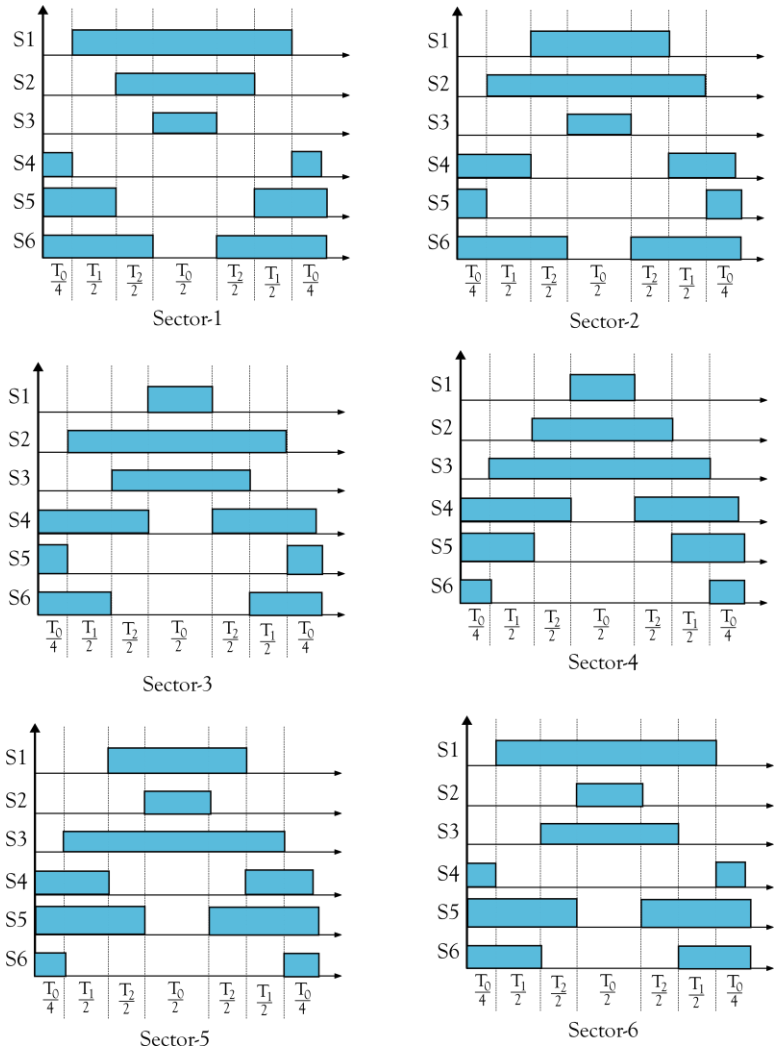

Figure 4.6 Duty cycle for all sectors with conventional SVM

The zero vector and the seventh vector (V_0 = (0,0,0) and V_7 = (1,1,1)) contribute to the common mode voltage. The time duration of these vectors is given by T_0. The common mode voltage in each state is given in Table 4.4. As seen, the zero states contribute the highest to the common mode voltage.

Switching State	**Inverter Pole Voltages**			**Common mode voltage (V)**
	V_{ao}	**V_{bo}**	**V_{co}**	
V_0	$-V_{dc}/2$	$-V_{dc}/2$	$-V_{dc}/2$	$-V_{dc}/2$

V_1	$V_{dc}/2$	$-V_{dc}/2$	$-V_{dc}/2$	$-V_{dc}/6$
V_2	$V_{dc}/2$	$V_{dc}/2$	$-V_{dc}/2$	$V_{dc}/6$
V_3	$-V_{dc}/2$	$V_{dc}/2$	$-V_{dc}/2$	$-V_{dc}/6$
V_4	$-V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/6$
V_5	$-V_{dc}/2$	$-V_{dc}/2$	$V_{dc}/2$	$-V_{dc}/6$
V_6	$V_{dc}/2$	$-V_{dc}/2$	$V_{dc}/2$	$V_{dc}/6$
V_7	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$

Table 4.4 Common mode voltage in each vector state.

The characteristic waveform of the space vector modulation is shown in Figure 4.7. Due to the existence of the third harmonic, there is an increase in the utilization of DC voltage while converting it to AC. In terms of control this translates to operation for a larger modulation index.

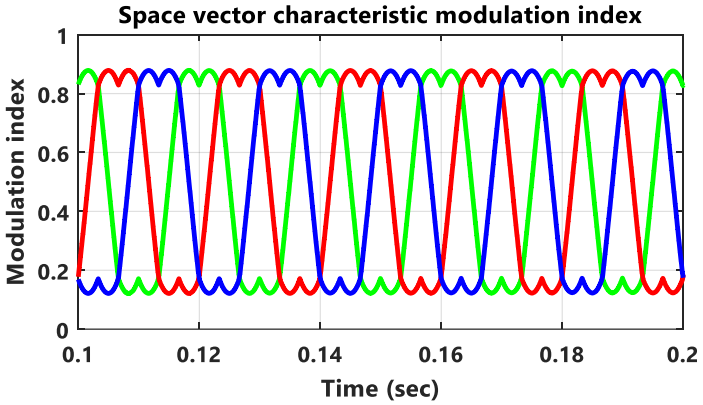

Figure 4.7 Output of space vector modulation.

4.3.4. Active Zero State PWM (AZSPWM)

This active zero state PWM (AZSPWM) is similar to space vector modulation. It uses the same active vectors to output the voltage but for creating the zero state, the modulation uses two opposite active vectors instead of using zero vectors [38]. An example of AZSPWM in sector-1 is shown in Figure 4.8. In conventional space vector modulation, in sector-1 the zero state are created by (0,0,0) and (1,1,1). But in case of AZSPWM, the zero state is created by using two opposite active vectors i.e., V_3 (0,1,0) and V_6 (1,0,1) in sector-1.

Shows the time calculation for sector-1. This still stands valid for AZSPWM if vectors V_3 and V_6 are used in the last term instead of V_0 and V_7. The modification is given by equation (4.10). Similarly, opposite active vectors are used for other sectors.

$$V_{ref}T_{sw} = V_1T_1 + V_2T_2 + \left(V_3\frac{T_0}{2} + V_6\frac{T_0}{2}\right) \tag{4.10}$$

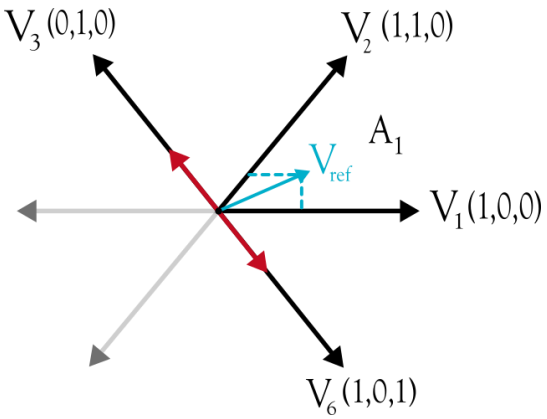

Figure 4.8 Active zero state PWM (AZSPWM) in Sector-1

It is important to note that when equation (4.10) is expanded, the third and the sixth vector cancel out each other leaving the exact same equations as given by equations (4.5) and (4.6). Hence, the final equations for time durations T_1, T_2 and T_0 remain same as conventional SVM. Similarly, all the sectors will have a specific pair of active vectors creating the zero state. The sequence and the active zero vectors are given in Table 4.5.

Sector	Switching sequence of Vectors
A_1	$V_3 \rightarrow V_2 \rightarrow V_1 \rightarrow V_6 \rightarrow V_1 \rightarrow V_2 \rightarrow V_3$
A_2	$V_4 \rightarrow V_3 \rightarrow V_2 \rightarrow V_1 \rightarrow V_2 \rightarrow V_3 \rightarrow V_4$
A_3	$V_5 \rightarrow V_4 \rightarrow V_3 \rightarrow V_2 \rightarrow V_3 \rightarrow V_4 \rightarrow V_5$
A_4	$V_6 \rightarrow V_5 \rightarrow V_4 \rightarrow V_3 \rightarrow V_4 \rightarrow V_5 \rightarrow V_6$
A_5	$V_1 \rightarrow V_6 \rightarrow V_5 \rightarrow V_4 \rightarrow V_5 \rightarrow V_6 \rightarrow V_1$
A_6	$V_2 \rightarrow V_1 \rightarrow V_6 \rightarrow V_5 \rightarrow V_6 \rightarrow V_1 \rightarrow V_2$

Table 4.5 Switching sequence of AZSPWM in all sectors.

As AZSPWM modulation avoids the usage of zero vectors, the zero states which contribute to the common mode voltage are avoided. Hence, the common mode voltage is reduced in this type of modulation. However, with this modulation the characteristic waveform is as shown in Figure 4.7. As the third harmonic characteristic of conventional SVM exists in AZSPWM, the advantage of higher utilization of DC voltage holds valid. From this figure it can be seen that there is a third harmonic which exists. Because of this third harmonic the DC link voltage also oscillates at third harmonic.

4.4. Simulation Results

As discussed above, the DC/AC converter is simulated for islanded, and grid connected operation with different modulation techniques and same load conditions. The common mode voltage and current waveforms for all the modulation of their respective mode of operation are compared in this subsection.

Lower value of common mode voltage is integral in grid connected operation. For the schematic under analysis, the common mode voltage and current is higher for the grid connected operation. This is because there is a low impedance path formed because of two grounding points (DC side and AC side). Hence, based on the analysis of the common mode parameters of grid connected operation, the modulation technique is selected and the same will also be implemented or islanded operation.

4.4.1. Results for grid connected operation

Lower value of common mode voltage is integral in grid connected operation. Hence, the above mentioned modulation techniques are compared for the operating model for the same system. The common mode voltage for different modulation techniques is shown by Figure 4.9. For simulating the system, the operating conditions used as the same as grid connected operation i.e., 750V DC.

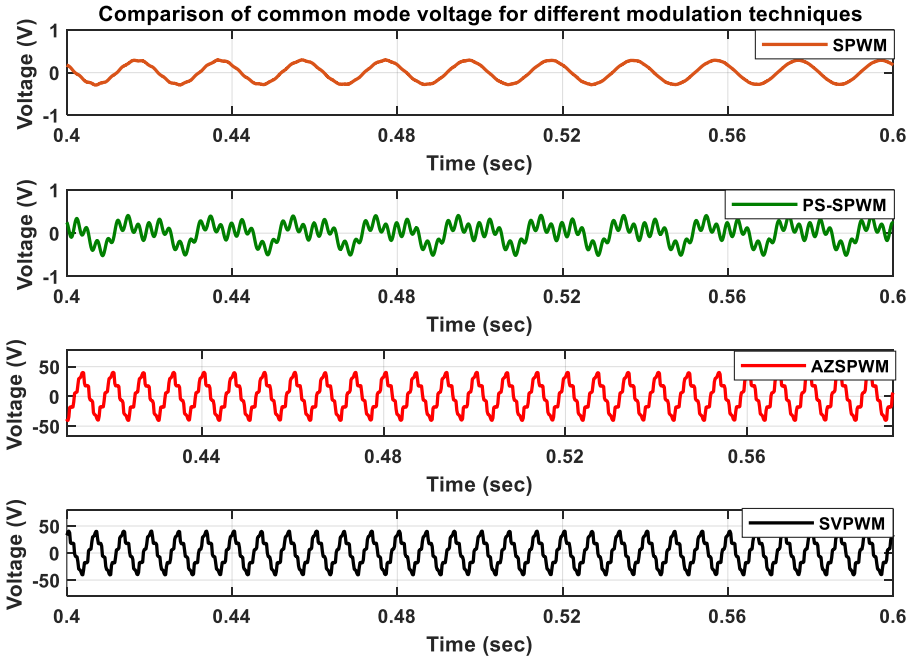

Figure 4.9 Comparison of common mode voltage with different modulation techniques.

As seen from the results, the common mode voltage is very less for the sine characteristic modulations i.e., the custom space vector, SPWM and PS-SPWM. As seen from Figure 4.4, for sinusoidal modulation techniques the common mode (i.e., the zero states) are caused near the tip of the carrier and modulating waves. Hence, it can be inferred that higher the modulation index lower will be the common mode for sinusoidal modulation techniques. As the current system is operating at higher modulation index ($0.86<m<1$) the common mode is very less.

However, for the space vector modulation the DC voltage is increased by injecting the third harmonic [38]. With the third harmonic injection, as the DC neutral and AC neutral are short circuited, the DC pole voltages tend to oscillate at third harmonic. Due to this oscillation, there is a large current injected into the ground. The step change in the common mode voltage and current occur at 300Hz which corresponds to each sector change as stated in 4.3.3. The DC pole voltages for sinusoidal modulation techniques and space vector modulation techniques are shown in Figure 4.10.

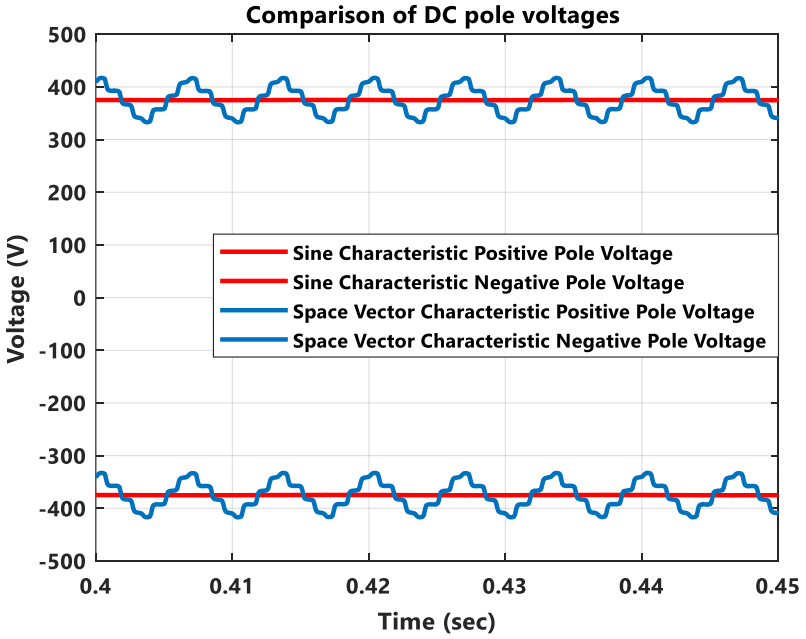

Figure 4.10 DC pole voltage characteristic for sinusoidal modulation versus space vector modulation.

This oscillation of the pole voltages increases the common mode voltage for the system. This also increases the common mode current in a similar pattern as the voltage. The common mode current for the space vector will have spikes in magnitude depending on the crests and troughs of the voltage oscillation. The comparison of all the common mode currents for different modulation techniques

is shown in Figure 4.11. Based on the common mode voltage and the currents waveforms the sine wave characteristic is opted for modulation.

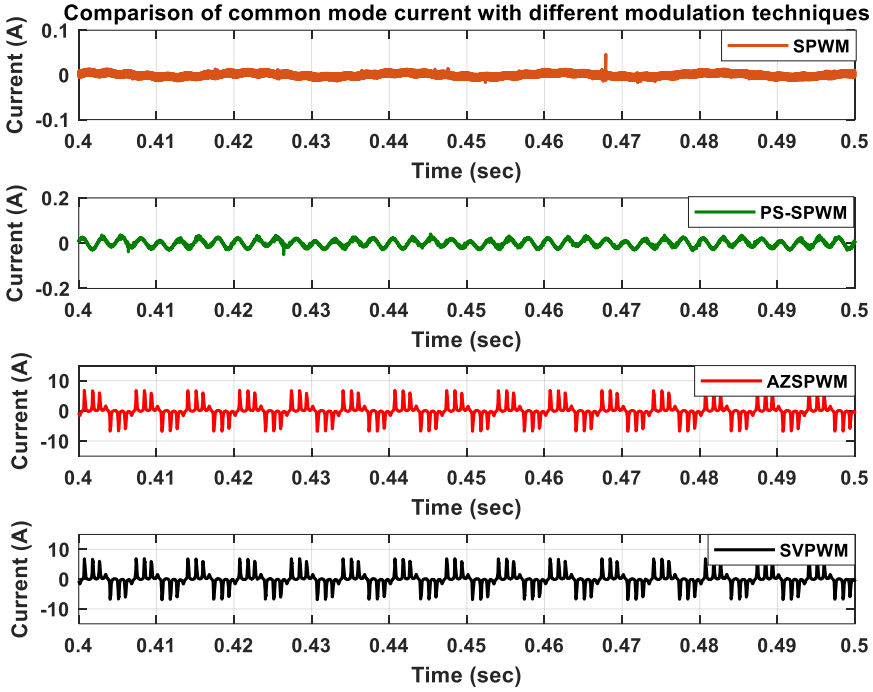

Figure 4.11 Comparison of common mode currents for different modulation techniques.

4.5. Summary

This chapter discussed about the grounding of the converter for the existing system. The different standards for common mode parameters and the effects have been stated. Based on these two factors i.e., type of grounding (capacitive considered for the system under analysis) and standards for common mode the different modulation techniques are discussed and the resulting common mode are simulated.

In this chapter the theory behind different modulation techniques has been explained. The criteria for determining the modulation technique are summarized in Table 4.6. As known by the operating conditions, the modulation index is within the maximum limits for all the modulation techniques mentioned. The DC pole voltage oscillation and the common mode voltage are discussed in this chapter for different modulation techniques. Finally, the simulation results are analyzed, and selection criteria for the different modulation techniques is explained. The data for common mode voltage and the DC oscillation is adopted from the simulation results.

Modulation Type	SPWM	PS-SPWM	SVPWM	AZSPWM
DC Voltage Utilization	Low	Low	High	High
DC Voltage Oscillation	Not Present	Not Present	Present	Present
Common Mode Voltage	Low	Low	High	High
Complexity of hardware implementation*	High	Very High	Low	Low

Table 4.6 Criteria for selection of modulation technique.(**This criteria has been explained in Chapter-5)*

Chapter-5
Hardware Implementation

Chapter–2 to Chapter–4 discuss the control strategies and present the simulation results for the same. Now that the satisfactory results are obtained in simulations, this chapter will discuss in detail about the hardware implementation of the control. For the control of the converter STM G4 micro-controller is used. The environment used for implementing the code is STM Cube IDE [39]. The existing PCB of the DC/AC converter is shown in Figure 5.1.

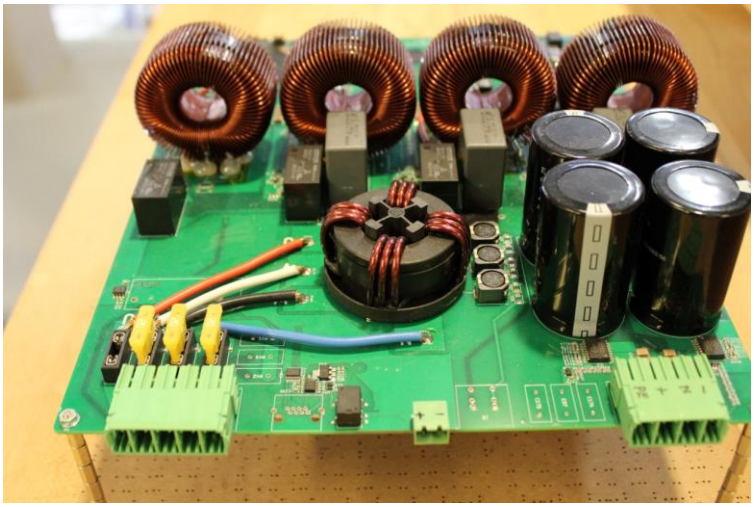

Figure 5.1 PCB of existing DC/AC converter

The components used in the DC/AC converter with the parameter values used are mentioned in Table 5.1. Before operating the converter under closed loop control it has to be ensured that the converter is well protected under testing conditions. To ensure this, "State Machines" are implemented in the microcontroller.

Components	**Value**
DC link capacitor	$2mF$
Filter inductance	$340\mu H$
X-capacitance[40]	$1\mu F$
Y-Capacitance [41]	$4.9nF$

Common mode inductance 3-phase, 4-winding [42]	$750\mu H$
Switches C3M0065100J, Silicon carbide (SiC) switch [43]	

Table 5.1 Components used on PCB of DC/AC converter

5.1. State Machine

A state machine is a mathematical model of the system which directs the operation under different operating states [44]. The state machine is implemented for the converter for the protection of the system under miscellaneous conditions. The protection verifies if there are any short circuit, erroneous preset values, ADC protection.

For example, if the converter has a short circuit somewhere in the circuit due to some external circumstances and the operator does not know about it, there will be a huge inflow of current when the converter is operated. Hence, to protect the converter from failure or incorrect operation, the state machine is implemented. The state machine implemented for the converter is shown in Figure 5.2. The circles in the figure represent the states in which the converter will operate. The operation in the states is explained below.

- **IDLE:** This state represents the OFF state of the converter.

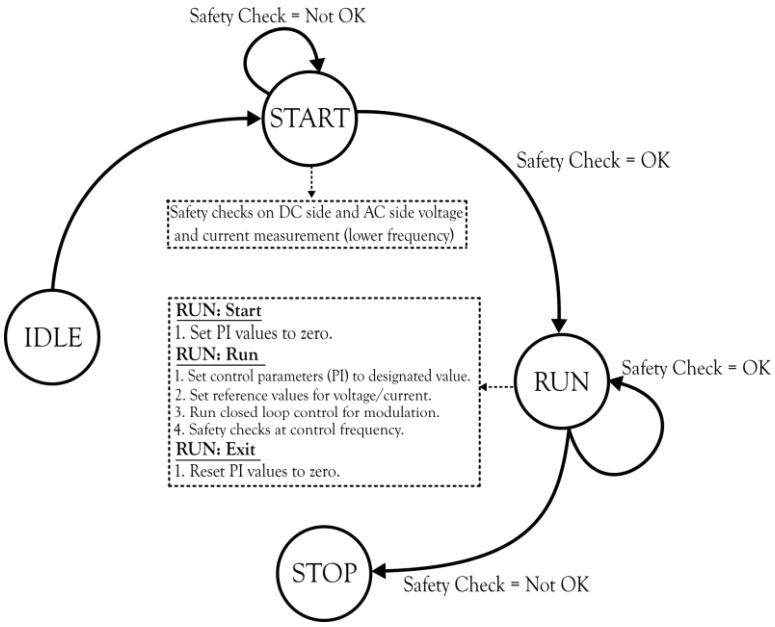

Figure 5.2 State Machine diagram for DC/AC converter

- **START:** In this state the various parameters of the converter such as DC capacitor voltages, voltage across switches, output voltages, currents and any

existing short circuit is checked. Hence, during in this state the converter does not operate but it is in ON state. The output of this state is to provide information about the safety checks. If the safety check results in unhealthy system, it stays in START state and does not move further.

- **RUN:** If the safety check results in a healthy condition, the converter enters the RUN state. In this the "RUN: Start" substate resets the PI controller values, reference values for the controller as required. Next to that the converter enters the "RUN: Run" substate where the converter operates in closed loop by setting the proper PI values. During this substate the safety checks also run parallel to the converter operation to address any unwanted operation. If the safety check results in healthy condition, then the converter keeps on running. If it results in unhealthy conditions, the PI controller values, and reference values are reset to ensure dormancy of converter.
- **STOP:** If the safety checks result in unhealthy condition, the state is changed to STOP where the converter again moves back into the OFF state.

The state diagram drawn represents one cycle of operation. For continuous operation the state STOP state will be further connected to the START state.

5.2. Modulation on MCU

For implementing the control and the modulation, STM32G474VET6 is used, and the environment used is STM32 Cube IDE. As seen from the simulations, the modulation involves multiple complex numerical calculations which cannot be easily processed by the microcontroller and can result in response delay (it can reach up to a few seconds). Hence, it is important to optimize the calculations in order to obtain fast response from the microcontroller.

As concluded from the previous chapter it is known that the sine characteristic yields the lowest common mode voltage. However, the implementation of SPWM and PS-SPWM would be highly time consuming especially considering a discrete control frequency 10 times less than the switching frequency. Hence, there will be 10 steps of the same value before the interrupt of the microcontroller updates with a new value.

Further modification has been developed for improving the resolution of the modulation. As known, the fundamental frequency of the output is 50Hz, while the control frequency is 5kHz and the switching frequency is 50kHz. Hence, in the modulation one rotation corresponds to 50Hz, while the angle for axes transformation gets updated at 5kHz which is the control frequency. However, these values are used within the 50kHz loop for switching. The resolution can be obtained as given by equations (5.1) and (5.2).

$$Control\ Steps\ in\ one\ fundamental\ cycle = \frac{5kHz}{50Hz} = 100 \tag{5.1}$$

$$Angle\ resolution = \frac{360^o}{100} = 3.6^o \tag{5.2}$$

$$Intended\ angle\ resolution = \frac{360^o}{\frac{50kHz}{50Hz}} = 0.36^o \tag{5.3}$$

Hence, if this scaling is ignored, then the same value of the voltages will be used for 10 consecutive switching cycles. To improve this resolution, an interrupt based loop is used in which a counter is set to count 10 times. Once, the interrupt value is updated the angle within the 5kHz cycle, the internal loop is run at 50kHz cycle thereby updating the most recent value by 0.36°. Hence, the resolution of the modulation is improved even when the controller frequency is slower.

5.3. Hardware results for islanded operation

In this subsection, the hardware results of the converter in islanded operation have been shown and analyzed. The test setup is shown in Figure 5.3 for observing the impact of control on the converter. The setup consists of unbalanced resistive loads which are equipped with fans for maintaining the temperature (thereby the resistance of the loads). All the test waveforms are obtained from PicoScope 2000, and the waveforms are plotted in MATLAB.

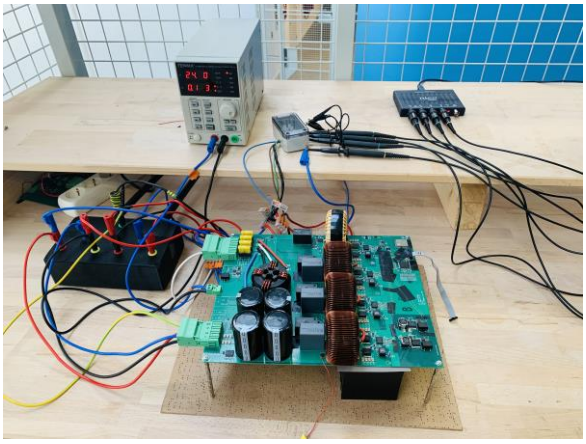

Figure 5.3 Test setup for the converter with unbalanced resistive loads

5.3.1. Web Interface - Grafana

As mentioned in subsection 5.1 it is important to verify the proper operation of the converter prior to and during the operation to avoid incorrect operation while testing. Hence, the data of the state of operation, the trip reason are transmitted through the Wi-Fi module on the converter over to an interface which is called Grafana. The display of the Grafana is shown in Figure 5.4.

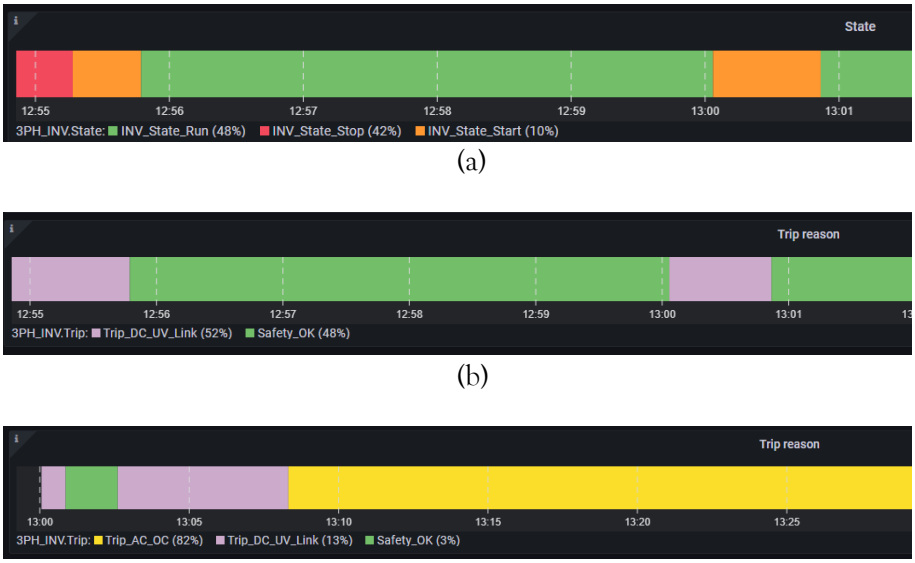

Figure 5.4 (a) Operating state of the converter in Grafana during healthy operation (b) Trip reason of the converter in Grafana (c) Trip reason of the converter in Grafana during a fault condition.

Apart from the state and the trip reason other data within the microcontroller such as the value of measured parameters through ADC of the controller can also be observed on this interface. As the entire control of the converter for both islanded and grid connected operation is in synchronous reference frame the observation of control input and output parameters becomes difficult while testing. Hence, this interface is used to transmit the data of synchronous reference frame to ensure the correct operation of the converter. However, the data is transmitted at a substantially larger delay than a control frequency i.e., approximately 100Hz.

5.3.2. Operation of three leg converter

Based on the test setup, the converter is tested at 700V with soft start. The soft start is implemented so that the start-up error is not amplified, hence avoiding the overshoot. For implementing the soft start, the reference setpoint of the PI controller is gradually increased in finite steps. The test results for three-leg converter are shown in Figure 5.5.

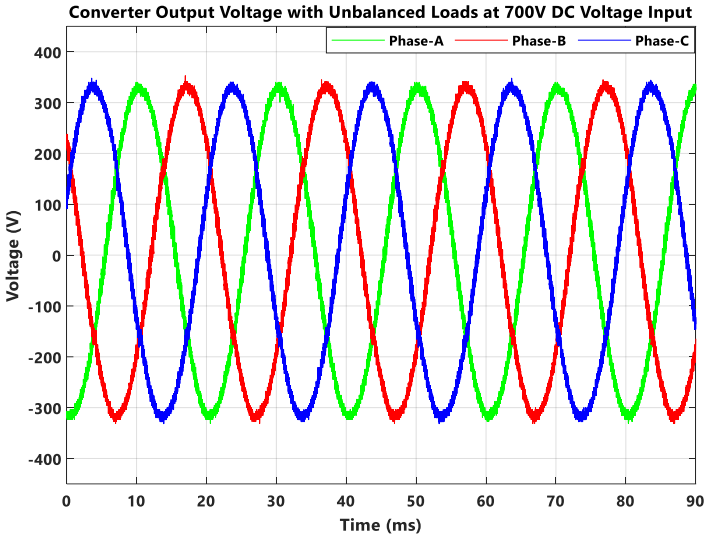

Figure 5.5 Results of the converter at 700V DC voltage

5.3.3. Fourth leg control – Islanded Operation

Note that in the previous operation the fourth leg is not used. As seen from Chapter-2, the fourth leg is used to control the neutral point so that there is no offset on the AC phases. The Figure 5.6 shows the neutral point voltage when the fourth leg is not operated. As seen from the zoomed portion the DC pole voltage error i.e., has a DC offset. Once, the fourth leg is implemented on the controller, the neutral is mitigated. However, the neutral point voltage will oscillate around zero. The results from the fourth leg control are shown in Figure 5.7.

Till now, the voltage control and the fourth leg control has been verified through the hardware results. However, these results represent when converter is load demands current within converter ratings.

As discussed in Chapter-2, when the converter in islanded operation is operated in overcurrent for a single, two or three phases the modified control strategy is used to limit the current within the limits. This is done by reducing the phase voltage of the particular phase. This control has already been implemented on the microcontroller and it is currently being tested. However, the final test results have yet to be obtained and thereby not presented here.

5.4. Modifications in PCB Schematic

The above subsection addressed the hardware implementation of the islanded converter with unbalanced loads. However, based on the control strategies discussed in Chapter-3 for grid connected operation, there are some changes that

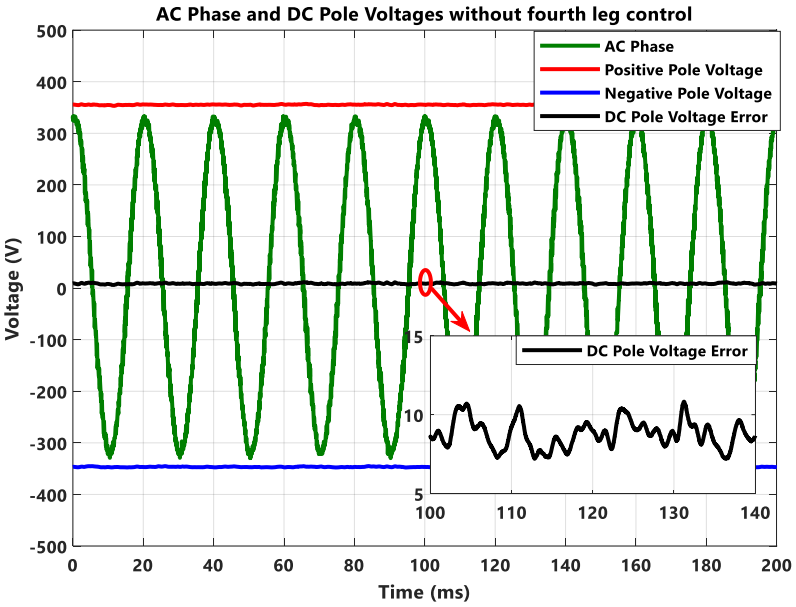

Figure 5.6 DC pole voltages and AC phase and neutral point offset without fourth leg control

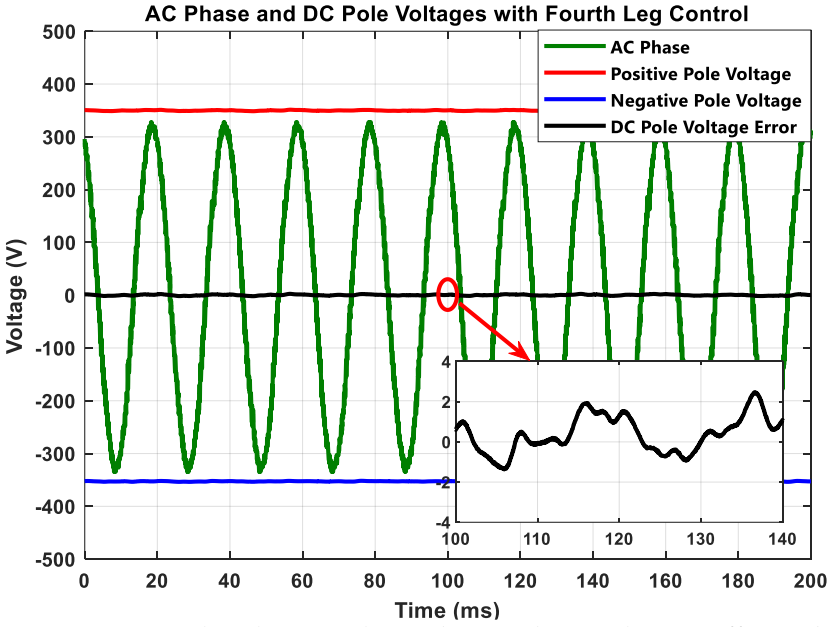

Figure 5.7 DC pole voltages and AC phase and neutral point offset with fourth leg control.

can be implemented on the PCB schematic for better operation of the converter which is discussed in this subsection.

5.4.1. Fourth Leg Control

As discussed in 3.2.4 the fourth leg is controlled with a voltage and a current control. This control is a modified strategy as compared to the control of fourth leg in case of islanded operation discussed in 2.4.2 which uses only voltage control. In the voltage only control strategy, the split capacitor voltages is used to control the switching action hence the requirement is only for the voltage sensors. However, for the modified control, voltage and current sensors both are required to implement the voltage and current control.

The control strategy in both cases is compared to ensure the better performance of voltage and current control in grid connected operation. The comparison is done in simulation and the results are presented in Figure 5.8.

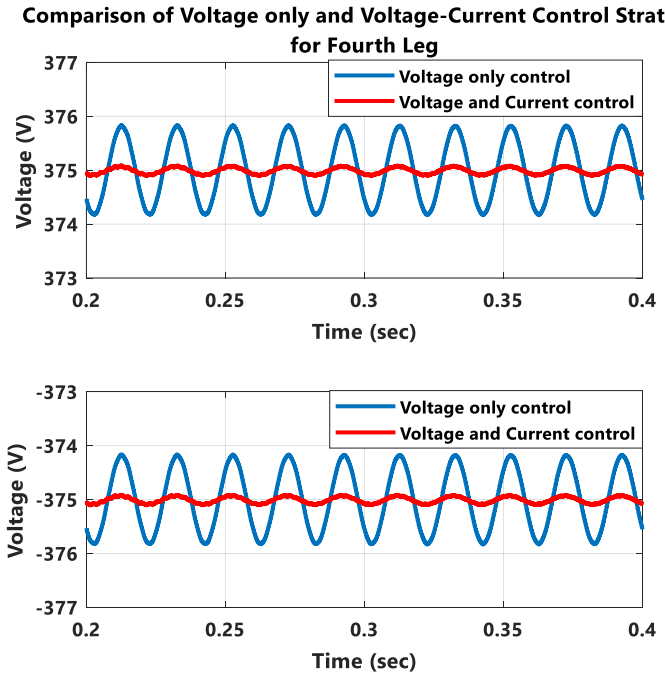

Figure 5.8 Comparison of Voltage only and Voltage-Current Control for control of fourth leg in Grid Connected Operation.

Based on the results, it can be determined that the voltage-current control has a much better response as compared to the voltage only control. However, the existing PCB has only voltage sensors present for the split capacitors. Hence, the modifications to be done in the PCB design is to add current sensors on the neutral line for voltage-current control of the split capacitors.

5.5. Summary

In this chapter, the hardware implementation of the control strategy is discussed. For preventing the converter against incorrect operation during testing as well as under conventional operation, the state machine is implemented. The various states and the conditions to transition between these states is explained. Once, the state machine is implemented, the control strategy discussed for islanded operation is implemented on the microcontroller. For this implementation certain computational limitations of the microcontrollers are taken into account and an optimized method of implementing the control is presented.

Based on the implemented state machine and control strategy the converter is tested with a DC source at the input and unbalanced AC loads at the output. For ensuring the proper operation of the state machine, a Wi-Fi module is used to transmit the data of the state machine to a web interface called Grafana. Finally, the test results are illustrated and based on the results it can be inferred that the control strategy proposed and simulated is now valid for real time operation. Lastly certain suggestions are made to modify the existing PCB so that the grid connected operation can be carried out.

Chapter-6
Conclusion and Further Developments

From this thesis it is now known that the increasing electricity generation through renewable resources can be integrated with the existing loads as well as the distribution grid through the power electronic interface. This thesis discussed in detail about DC/AC bidirectional operation having a topology of three-phase four-leg split capacitor and the challenges faced for closed loop control of the converter. This chapter provides final conclusion and discussion points from the thesis is presented which answers the research questions presented in the beginning of the thesis and some challenges are presented which can be further researched and explored.

Chapter–1 Introduction

The recent transition to the renewable sources for generating electricity is seen in this chapter. Based on the literature review it is conclusive that there is a significant increase expected in the AC loads present on the AC distribution grid. To increase the flexibility and mitigate the load demand, renewable sources can be utilized. Through investigation of grid conditions of different areas in literature, multiple reasons are examined due to which the problem of unbalance persists which also introduces a challenge for the integration of DER's. To mitigate these issues and integrating DER's the power electronic interface of DC/AC converter with the topology of four leg split capacitor is used. This chapter provides the background and the motivation for the research.

Chapter–2 Control of Islanded Converter

The challenges stated for the islanded operation of the DC/AC converter are addressed in this chapter. Based on the literature review it is concluded that the PI controller is more relevant to control as compared to PR controller the converter operating under unbalance load conditions. As the PI control is used in synchronous reference frame, the axes transformation is explained. The conventional voltage control and modified voltage control are compared in this chapter. To avoid the overcurrent scenario, the current limit control is presented through the injection of negative sequence which represents the modified voltage control. The neutral point control is presented through control of the fourth leg using voltage control. The modeling of common mode choke is explained in order to simulate the converter. The simulation results validate the control strategy proposed.

Chapter–3 Control of grid connected converter

The challenges stated for the grid connected operation of the DC/AC converter are addressed in this chapter. As stated, the four primary conditions to ensure proper grid connection are the voltage, frequency, phase, phase sequence. These requirements lead to the design of the PLL. A review has been done for the SRF-PLL and DDSRF-PLL which led to the outcome of using SRF-PLL due to less complexity and consideration of strong grid connection. For the control of the converter, the double synchronous reference frame current control is proposed with the objective of mitigating the unbalance on the grid currents. Two different types of reference current generators are examined i.e., power based, and DC-link voltage based reference current generator.

For the existing control strategy, a DC-link based reference current generator is used which is also responsible for determining the bidirectional operation of the converter other than providing the current reference in synchronous reference frame. Finally, the control strategy proposes a modification on the fourth leg control for better response of the grid connected converter by introducing the current control loop on the fourth leg inductor. Finally, based on the simulation results, the proposed control strategy is verified.

Chapter–4 Reduction of Common Mode Voltage

The problem of common mode voltage and common mode current in DC/AC converter is addressed in this chapter. The standards defining the threshold values of the common mode voltage and current are reviewed as a part of literature. A short literature review on the different grounding techniques is presented and a consideration is made that the DC/AC converter employs a capacitive grounding. Lastly as a part of the literature review, the frequency factor is introduced which changes the RCD threshold limits for tripping. Different modulation techniques such as SPWM, PS-SPWM, SVPWM and AZSPWM are explained in detail.

All the modulation techniques are simulated to compare and analyze the performance of converter for the common mode voltage. The converter is simulated for all the PWM techniques to compare the response of common mode voltage and common mode current. Finally, based on simulation results a selection criterion is presented.

Chapter–5 Hardware Results

The control strategy discussed in the initial chapter was implemented on the microcontroller to validate the real time operation with the simulation results. As shown in this chapter the state machine is added to the control to protect the converter against incorrect operation or control actions. Further to that the optimization of resolution is explained in order for the controller to operate more effectively. Further in this chapter, the results have been illustrated on the control strategy implemented for the islanded operation of converter with unbalanced loads

at 700V. From the results it is clear that the suggested control strategy is operational in real time as well.

6.1. Research Questions

The research questions stated in Chapter-1 are answered in this thesis. The answers corresponding to the research questions are answered as follows:

1. **What are the control strategies that have to be implemented on islanded converter and how to implement them?**

   In the islanded operation, the converter operates in grid forming mode. Thus, for establishment of balanced three phase AC output, the voltage control strategy is used. To implement the voltage control on the DC/AC converter a PI controller is used in the synchronous reference frame. The advantage of using PI control over PR control in unbalanced conditions is addressed. A modified control is presented which aims at operating the converter within the ratings even in case of overcurrent. This is achieved by using a negative sequence voltage controller which injects an unbalance in the AC output voltage and reduces the phase voltage in which overcurrent exists. This control strategy is for the three–leg converter. The neutral point of the split capacitor is independently controlled through the fourth leg. For implementing this type of control, a voltage control is used which aims at minimizing the error in the voltage between the two split capacitors. Through this type of control, the converter can be operated in islanded conditions.

2. **What are the control strategies that have to be implemented on grid connected converter and how to implement them?**

   For the grid connected operation, the DC/AC converter operates in grid supporting mode. The primary conditions for grid connection can be fulfilled by PLL (phase locked loop). For the control strategy of PLL two methods are reviewed namely SRF–PLL and DDSRF–PLL and considering the advantages and limitations of each type of PLL, SRF–PLL is opted. For controlling the converter, double synchronous reference frame current control is opted with the objective of mitigating unbalance on the grid and operating in either power injecting, power receiving or zero power injection modes. For operating the controller, the DC link based reference generator is used to clearly define the operation of the converter in three different modes.

   The fourth leg is controlled in a modified way as compared to islanded operation by adding current control on the neutral leg. The control is implemented using a PI controller operating for individual sequences with the objective of mitigating the unbalance on the grid introduced by the AC loads. To operate the fourth leg two P controllers are used in parallel which balance the voltage as well as reduce the current from the converter to the neutral point. Finally, there operating modes of converter in grid connected operation are

discussed and based on the control strategy unbalance is mitigated in all three modes.

3. **What are the different modulation techniques to reduce common mode voltage in grid connected DC/AC Converter?**

   Considering the capacitive grounding for the system, the different modulation techniques are compared to reduce the common mode voltage actively. Based on the common mode current values, the objective is to decrease the magnitude of the current as well as increase the frequency. The modulation techniques compared in this thesis are SPWM, PS-SPWM, SVPWM, and AZSPWM. Based on the grounding technique and the operating range of the converter, the sine characteristic of modulation is seen to have a better common mode voltage performance. Therefore, based on the criteria of common mode voltage, DC oscillation, DC voltage utilization and ease of hardware implementation sine characteristic modulation is selected.

6.2. Further developments

This thesis presented control strategies under different operating condition of the DC/AC converter. However, these strategies focus on the fundamental control of the converter and additional control strategies can be added based on evaluation of other real-time operating conditions. Some of the recommendations for the further developments in control are suggested below.

6.2.1. Hardware testing for grid connected operation

In this thesis, the hardware testing of islanded operation has been discussed. It would be interesting to validate the control strategy proposed in the thesis to test with grid connected at the output. This would also lead to analysis of the converter performance under different grid conditions.

6.2.2. Unequal DC Bipolar Voltage

In the existing operation, the input voltage is applied across the capacitor and the fourth leg is controlled for the voltage to be balanced on the two capacitors. However, in case of DC bipolar grid the voltage is dependent on the availability and hence, can be unequal. In such cases the neutral point will have an offset. In such operations the AC neutral point of the converter should not be connected to the DC neutral point.

In this case, the fourth leg operation is to control the neutral point on the AC side so that the voltages will have no offset because of the different pole voltages. This control of this type of converter topology is already analyzed in simulations but not included in the thesis. The hardware testing of this control would lead to more insights.

6.2.3. Combination of power and voltage based current references

As discussed in Chapter-3, the reference current is generated based on voltage based reference current generator. However, this does not take into consideration the amount of power that has to be injected. The power is determined based on the DC link voltage available. It would be interesting to research if both the control loops are simultaneously implemented.

6.2.4. Transition from grid connected to islanded operation

In this thesis the two different operations of the DC/AC converter i.e., islanded and grid connected operations are reviewed. However, in real time operations, under fault conditions the grid can transition to islanded mode. Hence, it would be interesting to explore the control strategy which can allow smooth transition from grid connected to islanded operation.

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Appendix

1. Simulation schematic of islanded operation of DC/AC converter.

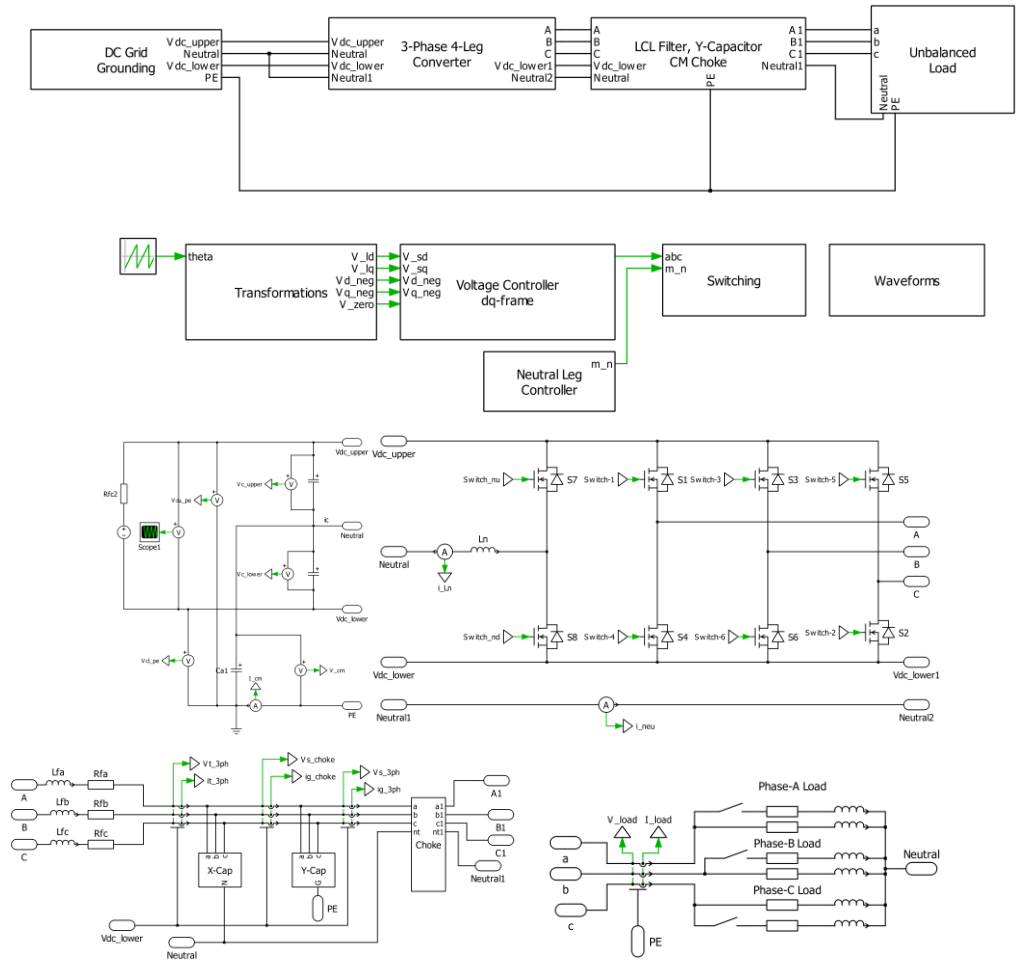


Figure 2.17 PLECS schematic of converter

2. Controller structure for islanded operation of DC/AC converter.

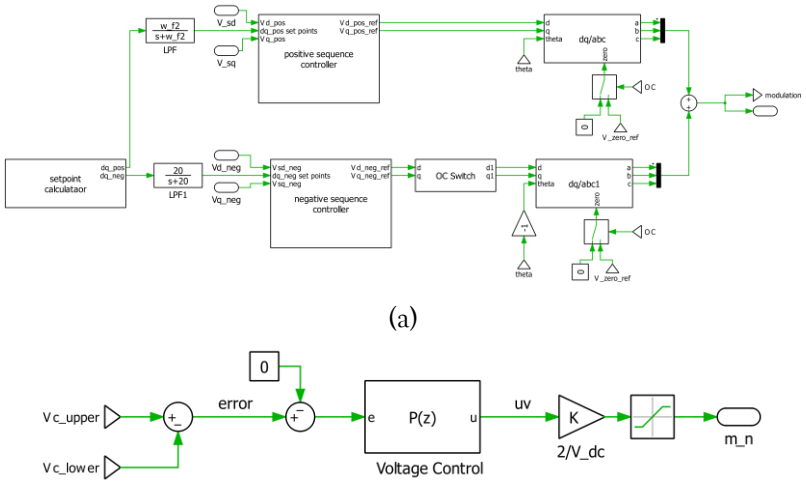


Figure 2.18 (a) Modified Voltage Control in PLECS (b) Voltage control for fourth leg for balancing split capacitor voltage.

3. Simulation Schematic of grid connected operation of DC/AC Converter.

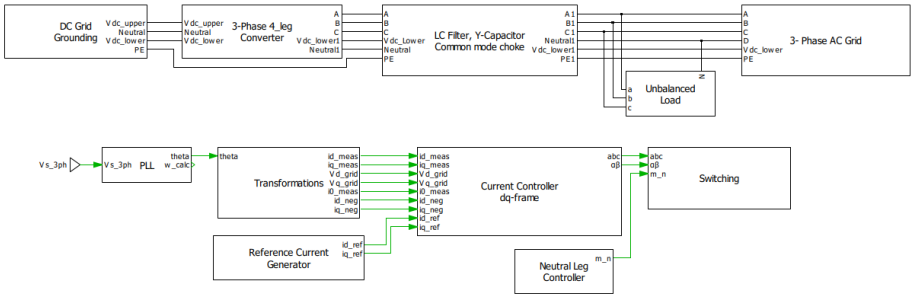
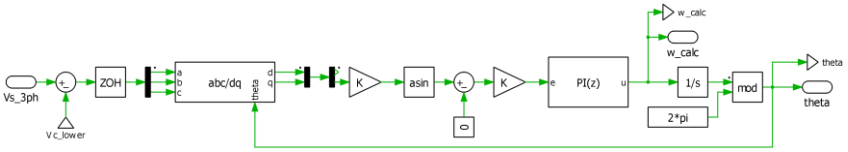


Figure 3.19 Schematic of grid connected operation of DC/AC Converter.

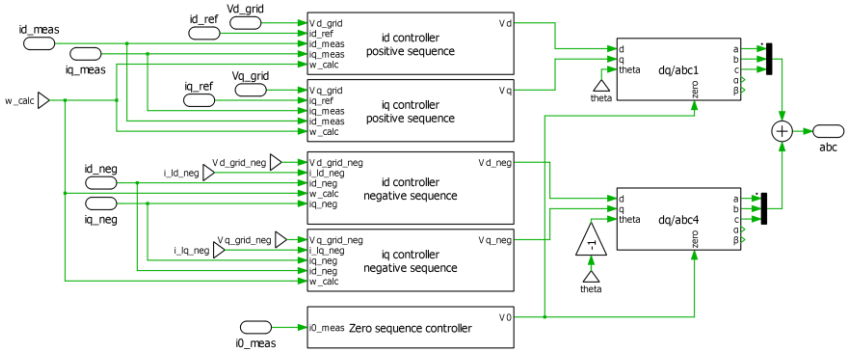
4. C-script for modified voltage control

```
double ia, ib, ic, Va_max, Vb_max, Vc_max, V_nom;
static double a=0, b=0, c=0;
ia= fabs(Ia);
ib= fabs(Ib);
ic= fabs(Ic);
V_nom= 230*sqrt(2);
%checking which zone of overcurrent is the operation
%Phase-A
if(ia > 24){
    a= 1;
    na= 1;}
else if(ia < 24 && a==1){
    na= 1;}
else{
    na= 0;}
%Phase-B
if(ib > 24){
    b= 1;
    nb= 1;}
else if(ib < 24 && b==1){
    nb= 1;}
else{
    nb= 0;}
%Phase-C
if(ic > 24){
    c= 1;
    nc= 1;}
else if(ic < 24 && c==1){
    nc= 1;}
else{
    nc= 0;}
Va_max = 230*sqrt(2) - na*100*sqrt(2);      %reducing the amplitude
Vb_max = 230*sqrt(2) - nb*100*sqrt(2);      %reducing the amplitude
Vc_max = 230*sqrt(2) - nc*100*sqrt(2);      %reducing the amplitude
Va_final= Va_max*cos(theta);                %Phase-A of three phase system
Vb_final= Vb_max*cos(theta - 2*pi/3);       %Phase-B of three phase system
Vc_final= Vc_max*cos(theta - 4*pi/3);       %Phase-C of three phase system
if(a ==1) {
    OC = 1;}
else {
    OC = 0;}
```

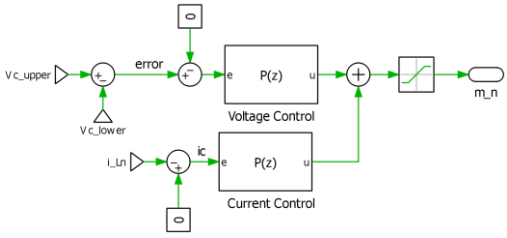
5. Controller Structure for grid connected operation of DC/AC converter.



(a)



(b)



(c)

Figure 3.20 (a) SRF- PLL schematic (b) Double synchronous reference frame (DSRF) current control (c) Fourth leg control

6. Initialization file for grid connected operation.

```
%% Power Parameters
fs= 50e3;        %switching frequency (50kHz)
Ts= 20e-6;       %Switching time
V_dc= 750;       %DC side voltage
f0= 50;          %grid side frequency
w0= 2*pi*f0;     %frequency in radians
C_dc= 2e-3;      %DC split capacitor value

%% LCL Parameters
L1= 340e-6;      %filter inductance of phase-A
R1= 6.3e-3;      %leakage resistance of converter side inductor
L2= 0.3e-6;      %grid side inductance value of phase-A
R2= 0.44e-3;     %Leakage resistance of grid side inductor
C_x= 5e-6;       %filter capacitance (differential Capacitor)
C_y= 4.7e-9;     %Common mode capacitance

%% Low pass filter (LPF) parameters
w_f1= 50;        %Low pass filter for negative sequence.
w_f2= 1000;      %Low pass filter for positive sequence.

%% Grid side parameters
Lg= 1000e-6;             %Grid inductance for X/R = 7
Rg= 0.4e-1;              %Grid resistance for X/R = 7

%% 3-Phase Load Values
Ra_load= 5;              %Load out of converter rating limits
Rb_load= 6;              %Load out of converter rating limits
Rc_load= 7;              %Load out of converter rating limits
La_load= 2e-6;           %Load out of converter rating limits
Lb_load= 4e-6;           %Load out of converter rating limits
Lc_load= 3e-6;           %Load out of converter rating limits

%% PLL Values
%For lower sampling frequency use the below values
Kp_pll= 1.5;             %Adjusted based on SO method values
Ki_pll= 200;             %Adjusted based on SO method values

%% Current control PI values
%For lower sampling frequency use the below values
Kpi_pos= 1;              %Positive sequence current controller prop. gain
Kii_pos= 40;             %Positive sequence current controller integral gain
Kpi_neg= 1;              %Positive sequence current controller prop. gain
Kii_neg= 30;             %Positive sequence current controller integral gain
Kp_zero= 1;              %Positive sequence current controller prop. gain
Ki_zero= 20;             %Positive sequence current controller integral gain

%% Neutral leg control
wi= 5000;                %bandwidth of the inner loop control (wi=5000)
wo= 3000;                %bandwidth of the outer loop control (wo=3000)
%wo= 50;                 %use when voltage only control for fourth leg is being used
kpin= wi*L1;             %prop. gain for current loop
kpvn= wo^2*L1*C_dc;      %prop. gain for voltage loop
```