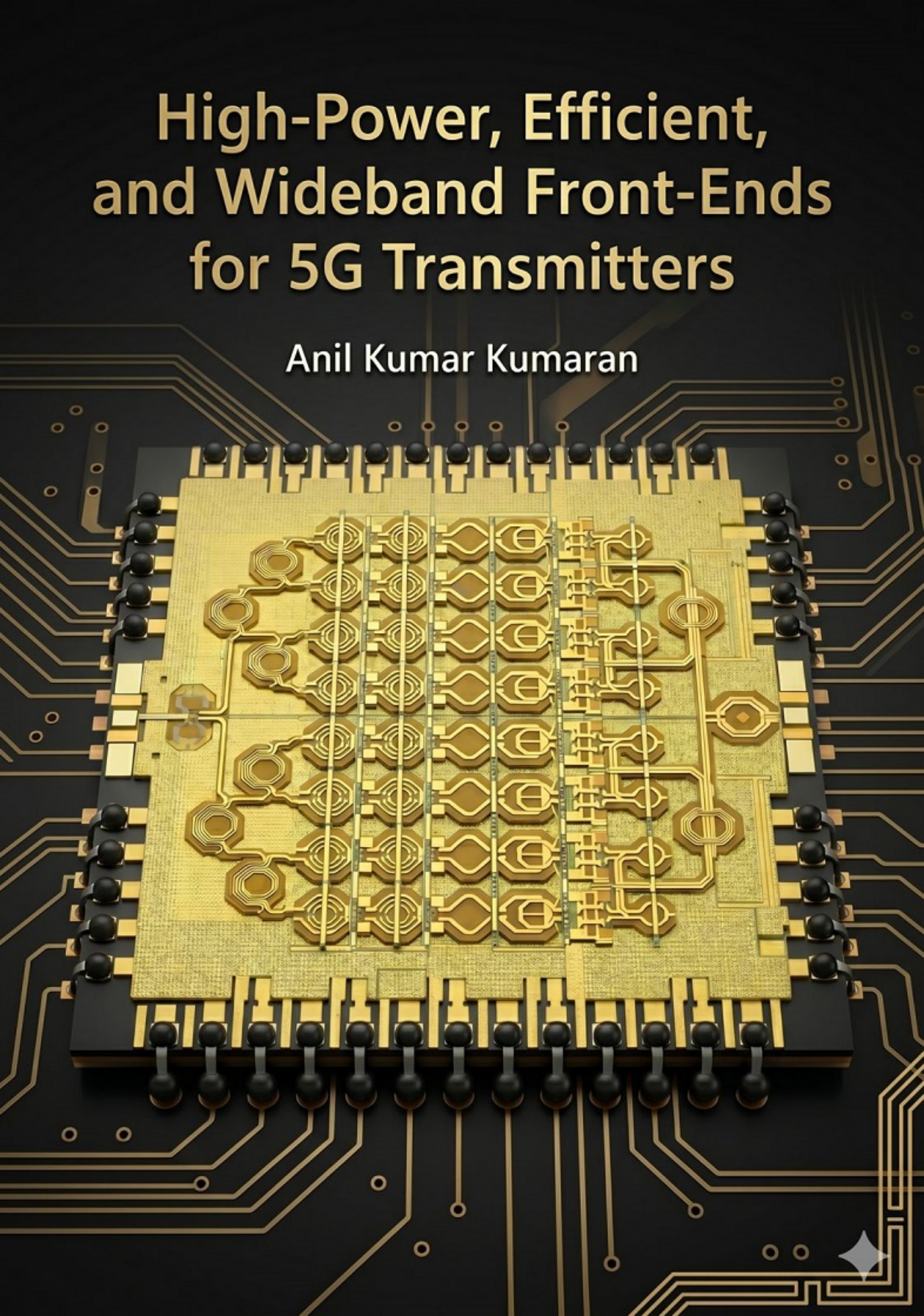
High-Power, Efficient, and Wideband Front-Ends for 5G Transmitters

Anil Kumar Kumaran



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Anil Kumar Kumaran

HIGH-POWER, EFFICIENT, AND WIDEBAND FRONT-ENDS FOR 5G TRANSMITTERS

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by

Anil Kumar KUMARAN

This dissertation has been approved by the promotors.

Composition of the doctoral committee:

Rector Magnificus,	chairperson
Dr. S.M. Alavi,	Delft University of Technology, NL, promotor
Prof. dr. ing. L.C.N. de Vreede,	Delft University of Technology, NL, promotor

Independent members:

Prof. dr. K.A.A. Makinwa	Delft University of Technology, NL
Prof. dr. ir. W.A. Serdijn	Delft University of Technology, NL
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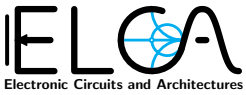

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This work is dedicated to everyone's implicit and explicit contributions.

Anil Kumar Kumaran

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1

INTRODUCTION

1

Over the past decade, the wireless industry has grown significantly and has become an essential part of modern life (Fig. 1.1). The advent of 6G networks is on the horizon, with fully standardized systems expected to launch by 2030, promising unprecedented levels of connectivity. This growth has been driven by the increasing demand for high-data-rate wireless communication systems, fueled by mobile broadband, gaming, home networking, and multimedia streaming applications. Fig. 1.2(a) illustrates the increasing need for high-data-rate communication in both long-range (e.g., cellular) and short-range (e.g., Wireless Fidelity (WiFi)) applications over the years [1, 2].

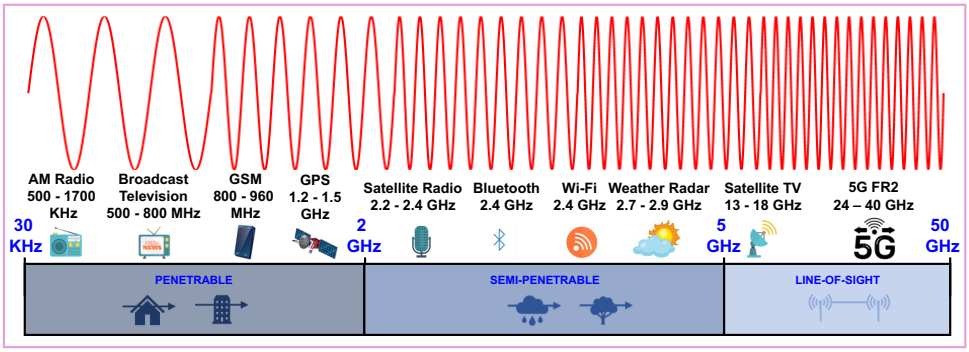


Fig. 1.1. Radio frequency (RF) and microwave spectrum, highlighting the frequency ranges utilized by various applications.

1.1. MOTIVATION

Fifth-generation (5G) networks aim to satisfy the universal demand of multi-gigabit data rates and provide low network latency, improved link robustness, mobility, energy efficiency, and spectral efficiency compared to the previous generations in the cellular network (Fig. 1.2(b)). 5G new radio (NR) spectrum has three frequency bands: low bands (<1 GHz), mid bands (1-7 GHz), and high bands (24+ GHz) (refer Fig. 1.3). In millimeter-wave (mm-wave) spectrum or high bands, larger modulation bandwidth can be used, which, along with spectrally efficient complex modulation schemes and phased array operation, helps 5G networks in achieving multi-Gbit/s data transmission and low latency line-of-sight links [3–5].

5G networks leverage multi-carrier modulation techniques like orthogonal frequency-division multiplexing (OFDM), offering high spectral efficiency, tolerance to multipath delay spread, immunity to frequency-selective fading channels, and power efficiency. OFDM signals are generated by the superposition of multiple orthogonal subcarriers, which are mutually independent, as illustrated in Fig. 1.4. The constructive interference of these subcarriers can cause high peaks in the signal amplitude, while destructive interference results in low power levels. These fluctuations lead to high peak-to-average power ratio (PAPR), a major drawback in OFDM systems.

When combined with digital modulation schemes like quadrature amplitude modulation (QAM), the related OFDM signals exhibit a wide range of amplitude variation due

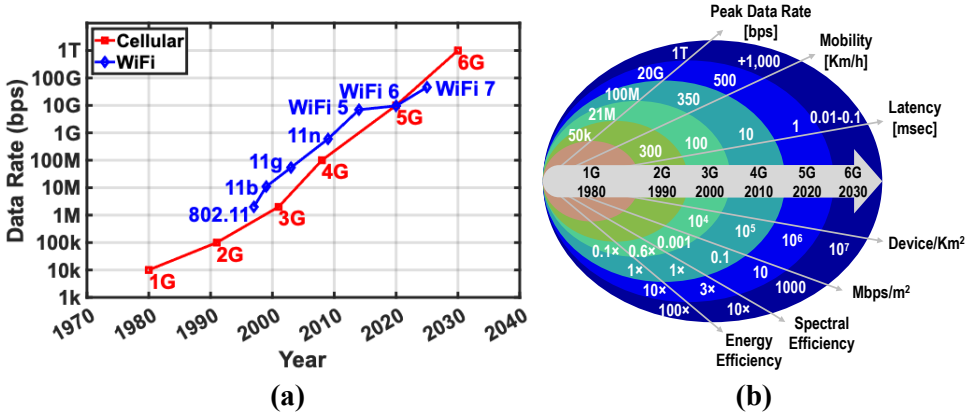


Fig. 1.2. (a) Evolution of data rates: Cellular vs. WiFi, and (b) comparison of the performance parameters of different cellular generations.

to the constellation points in QAM. Higher-order QAM schemes (16/64/256-QAM) exacerbate the PAPR by their greater amplitude variations. Another challenge for OFDM systems is that they require high linearity from transmitters (TXs) to avoid nonlinear distortion and spectral spreading.

Most radio systems employ class A/AB/B power amplifiers (PAs) in the TX lineup to achieve sufficient radio frequency (RF) output power. These PAs must operate at or near saturation to achieve their maximum efficiency. However, the high peaks encountered in QAM OFDM signals can drive the PA into saturation, increasing nonlinear distortion and spectral regrowth. To prevent this issue, the PA is backed off to ensure that the peaks of the QAM OFDM signal do not exceed the saturation level, reducing signal distortion and improving the bit error rate (BER) of the communication system. However, this back-off reduces PA efficiency, making the amplification process less efficient and leading to more costly TXs. Therefore, 5G TXs must be efficient both at peak and during power back-off (PBO) conditions, unlike traditional TXs [7, 8].

Table 1.1
PAPR AND EVM REQUIREMENT FOR MODULATION SCHEMES [10, 11]

PAPR for various modulations (Filter roll-off factor = 0.25)						
Modulation	QPSK SC	16 QAM SC	64 QAM SC	QPSK OFDM	16 QAM OFDM	64 QAM OFDM
PAPR (dB)	5	6.9	7.1	9.7	10.4	11

3GPP minimum EVM requirement					
Modulation	BPSK	QPSK	16 QAM	64 QAM	256 QAM
Required EVM (dB)	-10.5	-15	-18	-21.9	-29.1

Using higher-order modulation schemes helps to achieve higher data rates but also places stringent demands on error vector magnitude (EVM) for in-band linearity, and ad-

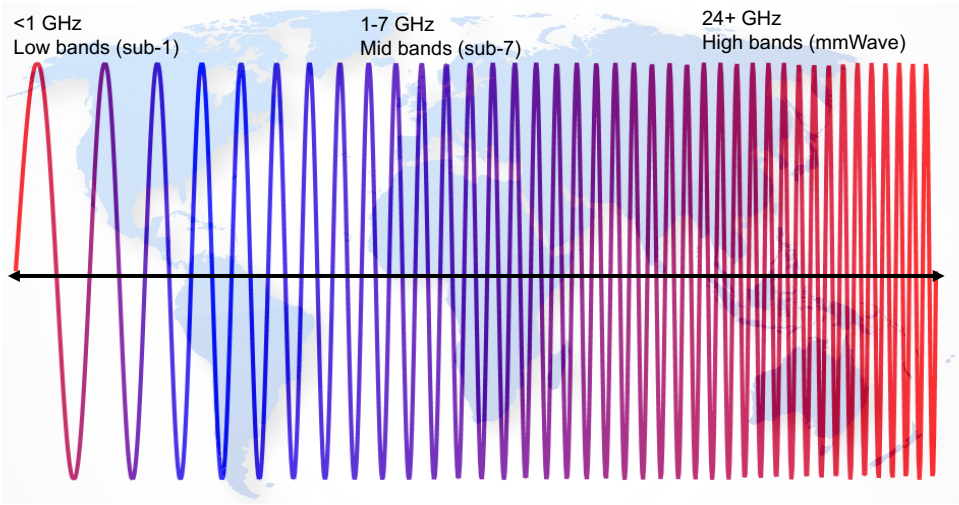


Fig. 1.3. 5G spectrum [6].

jacent channel leakage ratio (ACLR) for out-of-band spectral purity. The PAPR and 3rd Generation Partnership Project (3GPP) minimum EVM requirements are summarized in Table 1.1 for different communication standards. For instance, simpler modulation schemes like quadrature phase shift keying (QPSK) with single carrier (SC) transmission have a PAPR of 5 dB, whereas more spectrally efficient complex modulation schemes like 64-QAM OFDM have a PAPR of 11 dB. Similarly, as the modulation order increases, the signal-to-noise ratio (SNR) and EVM requirements become more stringent as the symbols become closer in the constellation diagram (see Fig. 1.5). For example, binary phase shift keying (BPSK) requires an EVM of −10.5 dB, while 256-QAM requires −29.1 dB. Thus, average efficiency and linearity (EVM and ACLR) are critical metrics for 5G TXs.

Table 1.2
5G 28/39 GHz APPLICATION SCENARIOS AND REQUIREMENTS [10–12]

Scenarios	Handset	Access point	Base station-1	Base station-2	Backhaul
EIRP (dBm)	30	45	55	55	60
Number of antennas (N_{ant})	4-6	32	64	16	256
P_{avg}/PA (dBm)	11-15	12	16	28	9
saturated output power (P_{sat})/PA (dBm) (PAPR=12dB)	23-27	24	28	40	21
P_{1dB}/PA (dBm)	18-23	19-20	23-24	35-36	16-17
Average Efficiency (%)	20	20	20	20	20
DC power (W)	0.4-0.6	2.5	12	50	10

P_{sat} = EIRP(dBm) - 20log10(N_{ant}) - G_{ant}(dB) + L_{ant}(dB)
antenna gain $G_{ant} \approx 5$ dB, frontend loss $L_{ant} \approx 2$ dB

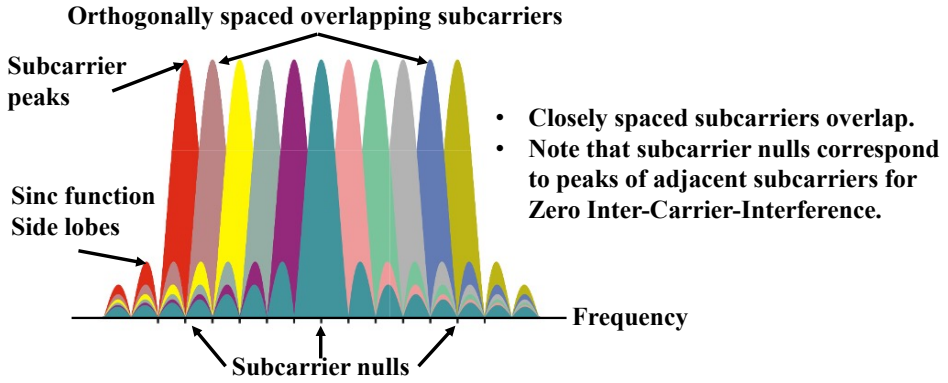


Fig. 1.4. OFDM signal frequency spectra [9].

Friis' equation (1.1) presents the free-space path loss(1.2), indicating that signal attenuation increases with frequency:

$$P_r = \frac{P_t G_t G_r \lambda^2}{4\pi d^2} \tag{1.1}$$

where, P_r is the power at the receiving antenna, P_t is the output power of the transmitting antenna, G_t is the gain of the transmitting antenna, G_r is the gain of the receiving antenna, λ is the wavelength, and d is the distance between the antennas.

$$L(dB) = 20\log_{10}(d[m]) + 20\log_{10}(f[Hz]) + 20\log_{10}\left(\frac{4\pi}{c}\right), \text{where } c = 3\times10^8\ m/s \tag{1.2}$$

Leveraging the mm-wave spectrum for 5G transmissions efficiently requires overcoming challenges such as increased scattering and environmental absorption, resulting in significantly higher path loss than in lower frequency bands. To address these challenges, PAs must deliver relatively high output power. The required output power (P_{out}) is determined by regulations and the link budget derived from the Friis transmission equation (1.1).

Knowing the required receiver power, antenna gains, distance, and carrier wavelength, the necessary transmitter power can be calculated. For RF PAs, output power levels for handsets typically range between 20 and 36 dBm, depending on standards and applications, with exceptions like Bluetooth and low-energy systems. In the mm-wave range, the output power requirement is closely related to the array size and the assumed total equivalent isotropically radiated power (EIRP).

Here, a small antenna array requires higher P_{out} per element to meet EIRP requirements, while a large array reduces the individual element's power requirements. However, larger arrays necessitate more accurate beamforming and more system overhead. Table 1.2 outlines the relationship between array size, EIRP, the PA element-level average output power (P_{avg}) and saturated output power (P_{sat}), highlighting how these parameters are interrelated across various 5G applications.

1

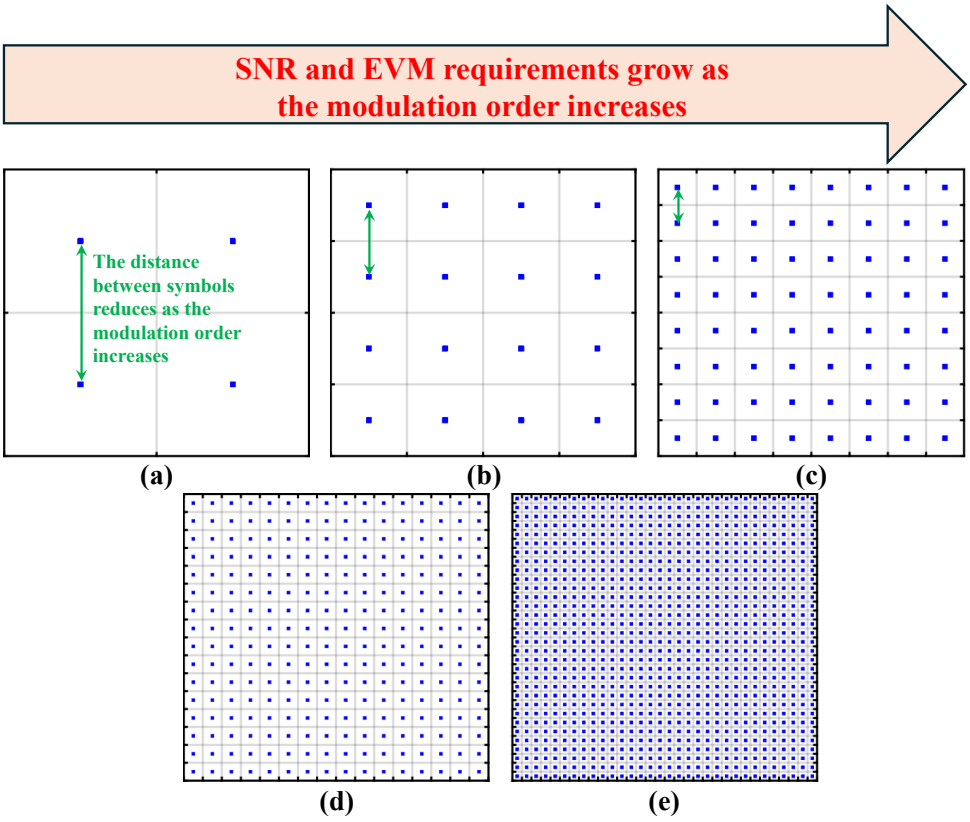


Fig. 1.5. (a) 4-QAM, (b) 16-QAM, (c) 64-QAM, (d) 256-QAM, and (e) 1024-QAM.

According to the Shannon-Hartley theorem, the capacity (C) of a wireless channel is finite for a given SNR and bandwidth (BW) in hertz (1.3) [13].

$$C = BW \cdot \log_2 (1 + SNR) \tag{1.3}$$

To achieve the multi-gigabit data rate envisioned by 5G communication systems (Fig. 1.2), the channel capacity must be augmented either by increasing the bandwidth or by increasing the modulation order. The latter increases the SNR and EVM requirements, necessitating a highly linear and low-noise operation. Increasing the available bandwidth is limited due to the finite RF spectrum, which must be shared among various applications. Studies [14, 15] show that the introduction of multiple-input multiple-output (MIMO) capability into communication systems can increase the capacity limit to:

$$C = N_t \cdot BW \cdot \log_2 (1 + SNR), \tag{1.4}$$

where N_t is the number of transmit antennas.

5G networks use beamforming to focus the RF energy in one or more directions by adjusting the signal phase or delay of each antenna element, helping to compensate

for channel loss and achieve wireless links over reasonable distances. Combined with MIMO, this technique breaks the capacity limit imposed by the Shannon-Hartley theorem.

Analog beamforming is the simplest operational form of these antenna arrays, offering low complexity but typically supporting only one beam per (sub-) panel, while requiring extensive power splitters for scaling. Analog beamforming is therefore not suitable for use in multi-user massive multiple-input multiple-output (mMIMO) systems, which enable higher data rates in the lower GHz range. Digital beamforming architectures offer higher flexibility and capacity enhancement, since they can support the multi-beam/-user mMIMO and digital pre-distortion (DPD) for each TX channel. However, the extensive digital signal processing (DSP) involved significantly increases the cost and power consumption of the system [16–18]. Hybrid beamforming systems combine both digital and analog beamforming, supporting both single-user and/or multi-user mMIMO [19].

However, in all beamforming architectures, the antennas of different TX elements are closely spaced, which can cause impedance variations due to mutual coupling and other environmental factors. This impedance variation, expressed in terms of voltage standing wave ratio (VSWR), can affect the TX's output power, efficiency, and linearity as the TX chain is designed for normal 50 Ω loading. Therefore, TXs must maintain performance despite changes in VSWR.

Complementary metal-oxide-semiconductor (CMOS) technology has become a cornerstone in 5G innovation. CMOS is known for its high density, cost-effectiveness, and performance in digital designs. It benefits from more than four decades of continuous scaling, dictated by *Moore's Law*. The high integration required for beamforming in mm-wave 5G systems demands that multiple TXs are integrated into the same chipset, making the footprint of each TX critical.

While compound semiconductors like gallium arsenide (GaAs) pseudomorphic high-electron-mobility transistor (pHEMT) and gallium nitride (GaN) high-electron-mobility transistor (HEMT) offer higher breakdown voltages and superior output power, CMOS technology has distinct advantages for 5G applications. These include multiple thick metal layers that enable vertically coupled structures like transformers, as well as customized ground reference plane, ideal for designing compact, multi-way power-combining networks.

The trade-off between PA output power and the number of antenna elements is illustrated in Fig. 1.6. High-power GaN PAs enable small arrays with limited integration, GaAs provides moderate RF power and integration, and silicon germanium (SiGe) Bipolar CMOS (BiCMOS), silicon-on-insulator (SOI), and bulk CMOS support large arrays with a lower RF power per-element. This highlights a key design choice: fewer high-power PAs versus many low-power, highly integrated PAs. Although CMOS excels in integration, enabling compact, cost-effective large-scale arrays, the lower RF output power per PA necessitates careful consideration of size, weight, power consumption, and cost.

Nevertheless, integrating a highly efficient system on chip (SoC) with CMOS TXs also presents challenges. CMOS technology is constrained by lower breakdown voltages and thus a low supply source (V_{DD}), which complicates meeting power requirements such as P_{sat} and output power at 1dB compression (P_{1dB}). Additionally, the conductive nature of the silicon substrate and low impedance levels of the output matching structures

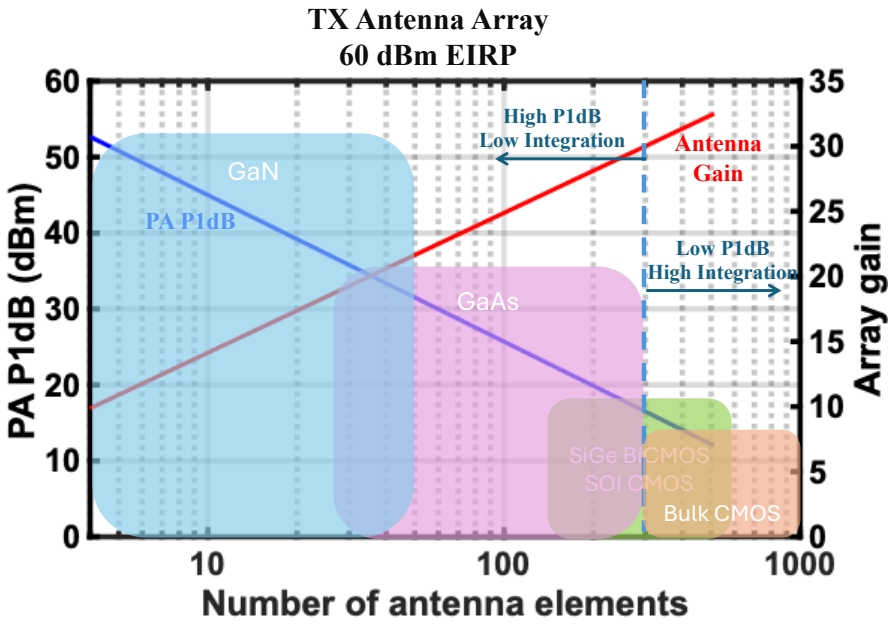


Fig. 1.6. PA P_{1dB} and array gain versus the number of antenna elements that can be integrated for different technologies [20].

degrade both output power and efficiency. Dedicated engineering solutions are therefore needed to balance CMOS's high integration capabilities with its lower RF power per-element performance.

1.2. THESIS OBJECTIVES

Mm-wave CMOS TXs for 5G applications are expected to deliver sufficient output power, operate efficiently under high PAPR signals, remain linear, be cost-effective, and support compact form factors for phased-array integration. Among all TX components, the PA plays a crucial role in determining the output power, average efficiency, thermal behavior, and the overall system reliability. However, designing mm-wave PAs in bulk CMOS is highly challenging due to low transistor gain, high passive losses, and process variability. These challenges are magnified in 5G systems, which require PAs to operate efficiently at significant power back-off (typically around 11 dB) to support complex yet spectrally efficient modulation schemes. Additionally, multistage PA designs often rely on numerous passive elements for inter-stage and output matching networks, which increase the chip area and cost, further complicating integration into dense phased-array systems.

This dissertation aims to identify and address the main design challenges limiting the performance and scalability of mm-wave PAs for 5G TXs through the development of novel amplifier architectures in CMOS technology. The research is driven by the following three key challenges:

1. *Achieving high efficiency at peak and power back-off*: In 5G TXs, average efficiency is a critical metric due to the high PAPR of the modulated signals. The first challenge is to maintain high energy efficiency at a significant power back-off level without sacrificing output power or linearity. To address this, the N-way Doherty architecture is systematically investigated. This work presents a design methodology that analyzes the trade-offs in output power, passive efficiency, and power-combining loss as the order of the Doherty structure increases.

2. *Overcoming bandwidth and area constraints*: Higher-order Doherty architectures typically suffer from limited bandwidth due to the increased complexity and number of passive components. The second challenge is to enhance the bandwidth and compactness of the Doherty output network without compromising performance. To this end, a 3-way Doherty PA with a balun-first, compact output network is designed, implemented, and measured in 40 nm CMOS technology to validate the proposed approach.

3. *Providing VSWR resilience*: In practical 5G systems, mismatches between the PA and antenna load — captured by the voltage standing wave ratio (VSWR) — degrade performance and reliability. The third challenge is to improve efficiency and robustness to load mismatch while minimizing additional passive losses. A novel 2-way Doherty architecture incorporating quadrature hybrid couplers (QHCs) is proposed to enhance VSWR resilience and average efficiency without significantly increasing insertion loss. This architecture is fabricated using 40 nm CMOS and experimentally validated.

By tackling these challenges, this dissertation contributes new design methodologies and architectures for scalable, wideband, and energy-efficient mm-wave PAs, suitable for next-generation 5G TX systems.

1.3. THESIS OUTLINE

This dissertation is organized into six chapters, each addressing a specific aspect of the design, analysis, and implementation of mm-wave PAs for 5G TX systems:

Chapter 1 – Introduction

This chapter introduces the motivation behind mm-wave 5G TX development in CMOS technology, it outlines the critical role of PAs in achieving performance targets, and defines the research challenges addressed in this work. It concludes with an overview of the thesis structure.

Chapter 2 – Metrics and design techniques for mm-wave PAs

This chapter introduces the fundamental performance metrics of PA design — namely output power, efficiency, linearity, and bandwidth — which are all critical in mm-wave 5G TXs. It emphasizes the PA's role as a primary bottleneck in achieving high-performance, energy-efficient transmission. Various PA operation classes are reviewed, along with their respective trade-offs in linearity and efficiency. The chapter then examines the specific challenges of mm-wave PA design, including efficiency at power back-off, bandwidth limitations, area constraints, and resilience to load mismatch. A comprehensive

review of state-of-the-art solutions is provided, highlighting their limitations and motivating the research directions pursued in the subsequent chapters.

Chapter 3 – Design and Analysis of Compact N-Way Doherty Power Combiners
This chapter introduces the Doherty PA as a promising solution for achieving high efficiency under power back-off. The N-way Doherty architecture is analyzed in detail, focusing on the design methodology and scaling behavior as the number of auxiliary paths increases. Trade-offs in output power, average efficiency, and passive loss are discussed. The chapter also establishes criteria for determining the optimum Doherty order based on signal PAPR and system-level performance requirements.

Chapter 4 – A Single-Supply Balun-First Three-Way Doherty PA
To address the bandwidth and area limitations of higher-order Doherty architectures, this chapter proposes a compact output network architecture employing a balanced-to-unbalanced (balun)-first design. The implementation and measurement of a 3-way Doherty PA in 40 nm CMOS technology are presented, demonstrating enhanced bandwidth, reduced passive complexity, and improved integration potential for phased-array TXs.

Chapter 5 – A 4xTwo-Way mm-wave Doherty CMOS PA
This chapter introduces a novel architecture that combines a 2-way Doherty structure with QHCs to improve average efficiency while enhancing resilience to load mismatches (VSWR). The design benefits from reduced insertion loss and superior linearity under varying load conditions. Results of the prototype fabricated in 40 nm CMOS are presented to validate the architecture's robustness and performance advantages.

Chapter 6 – Conclusion and Future Work
The final chapter summarizes the key contributions of the dissertation and reflects on the effectiveness of the proposed architectures in meeting 5G PA requirements. It outlines potential directions for future research, including further optimization of passive structures, integration of the proposed PAs into complete TX frontends, and exploration of alternative CMOS and fully depleted silicon-on-insulator (FD-SOI) platforms.

2

Metrics and Design Techniques for mm-wave PAs

This chapter explores the fundamental performance metrics in PA design for mm-wave 5G systems. Additionally, it provides an overview of various PA classes and highlights the challenges associated with mm-wave operation, along with existing solutions to address these challenges. The chapter also delves into the design equations of a 2-way Doherty PA, offering insights into its operation and performance.

2.1. INTRODUCTION

Direct up-conversion (DUC) is one of the simplest TX architectures. It is well-suited for beamforming TXs since it can provide less power consumption, less silicon area, and allows for full CMOS integration. As shown in Fig. 2.1, DUC consists of the following parts: 1.) baseband digital-to-analog converters (DACs) and low-pass filter (LPF), 2.) voltage controlled oscillator (VCO), 3.) a quadrature signal generator and an in-phase/quadrature (I/Q) mixer, and 4.) front-end (pre-driver (PDRV), driver (DRV) and PA).

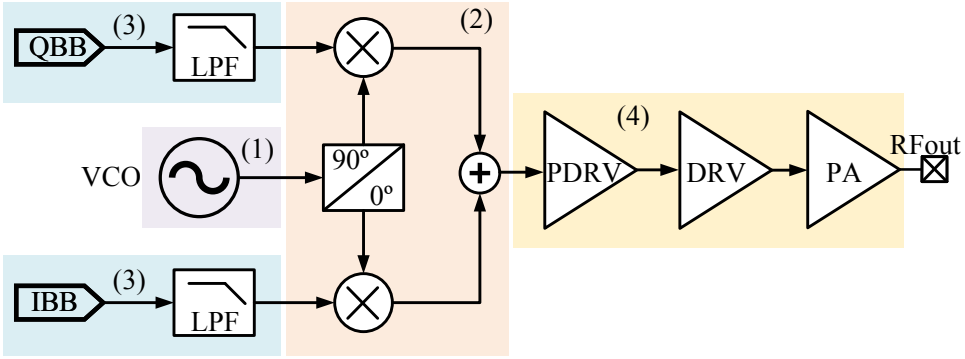


Fig. 2.1. A simplified direct up-conversion (DUC) TX architecture.

As discussed earlier, 5G communication systems use complex modulation schemes such as 64-QAM OFDM signals, which require stringent in-band linearity, quantified by EVM. The nonideality of each component in a DUC TX affects its overall EVM, which can be estimated by (2.1).

$$EVM_{TX} = \sqrt{EVM_{PN}^2 + EVM_{QN}^2 + EVM_{SFDR}^2 + EVM_{IRR}^2 + EVM_{LOFT}^2 + EVM_{IMD}^2} \quad (2.1)$$

where EVM_{PN}, EVM_{QN}, EVM_{SFDR}, EVM_{IRR}, EVM_{LOFT}, and EVM_{IMD} are the EVM degraded by phase noise (PN) of the VCO, quantization noise (QN), spurious free dynamic range (SFDR), I/Q modulation imbalance, local oscillator feedthrough (LOFT) and the inter-modulation distortion (IMD), respectively. The main contributor to IMD is the PA's nonlinearities, such as the voltage-dependent nonlinear parasitic drain-source capacitance (C_{ds}), nonlinear transconductance (g_m), and gain compression at P_{sat} [21].

The PA predominantly determines the linearity of a TX, as it must perform the linear amplification of large signals. Furthermore, PA accounts for the majority of the TX's power consumption. As a result, the overall TX linearity is primarily constrained by the PA. Designing a highly linear PA with high efficiency is particularly challenging, making it the main bottleneck in 5G TX systems. Before exploring the specific challenges of mm-wave PA design, it is essential first to understand the fundamentals of PA operation and its associated performance metrics.

2.2. BASICS OF PA

Power amplifiers (PAs) are the final active circuit stages in a wireless TX, interfacing directly with the antennas to generate sufficient signal strength for wireless transmission. PAs are indispensable components in many wireless systems, including mobile devices, fixed wireless systems, radar and imaging systems, and satellite communication.

Fig. 2.2 illustrates a general PA architecture comprising a PDRV, DRV, and PA, along with input, interstage, and output matching networks. In general, PA design can be categorized into active circuit design and passive network design.

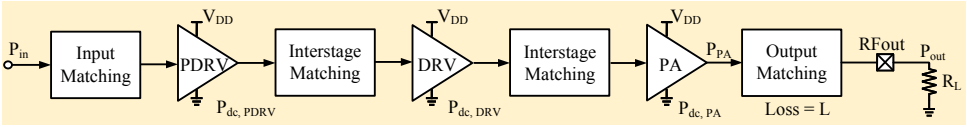


Fig. 2.2. Conceptual PA schematic.

Active circuit design deals with device performance aspects such as gain, efficiency, linearity, PA classes, harmonic-based waveform shaping, stability, and reliability. On the other hand, passive network design addresses impedance transformation, power combining, waveform shaping, and bandwidth filtering. In particular, the inter-stage matching networks between the PDRV, DRV, and PA play a critical role in determining the overall bandwidth and gain of the entire chain.

2.2.1. PA PERFORMANCE METRICS

This section defines the fundamental performance metrics of a PA, a key component of wireless TXs. Referring to Fig. 2.2, the input power is denoted as P_{in}, the power at the PA output stage as P_{PA}, and the power delivered to the load as P_{out}. The total direct current (dc) power consumed by the PA, PDRV, and DRV stages is given by:

$$P_{dc} = P_{dc,PA} + P_{dc,DRV} + P_{dc,PDRV} \tag{2.2}$$

The power gain G_P of the PA is defined as:

$$G_P = \frac{P_{out}}{P_{in}} \tag{2.3}$$

in which P_{out} is the power that is actually delivered to the RF load and P_{in} is the RF power available from the source.

PA efficiency is commonly described using the drain efficiency (DE), defined as:

$$\text{DE} = \frac{P_{out}}{P_{dc,PA}} \tag{2.4}$$

Another critical metric is the power-added efficiency (PAE), which incorporates the impact of P_{in}:

$$\text{PAE} = \frac{P_{out} - P_{in}}{P_{dc}} \tag{2.5}$$

For PAs with limited power gain, PAE becomes particularly important. If the gain is high, PAE can be approximated as P_{out}/P_{dc}.

Consider a PA delivering a P_{out} of 1 W (30 dBm) with a DE of 40 %, a typical value for mm-wave PAs. Using (2.4), the PA's dc power consumption ($P_{dc,PA}$) is 2.5 W. This implies that 1.5 W of the dc power is dissipated as heat, which poses challenges to thermal management and device reliability. If V_{DD} is 1 V, the total DC current will be 2.5 A, requiring low resistance traces, vias, and grounding networks to avoid $I \cdot R$ drops and mitigate reliability issues such as electromigration.

If the output matching network has a 2 dB loss, its passive efficiency is approximately 63 %. To achieve a DE of 40 % at P_{out} = 1 W, the intrinsic PA efficiency must be around 64 % (40%/63%). The RF power loss in the output matching network alone would be 587 mW, highlighting the critical importance of low-loss passive network design.

Assume a G_P of 20 dB, which is a typical design choice to ensure stability. From (2.3), the required P_{in} is 10 mW (10 dBm). At mm-wave frequencies, generating P_{in} poses challenges for up-conversion mixers due to limited gain in this frequency range.

Equation (2.6), described in [10], is helpful in describing the fundamental factors that limit the achievable efficiency of a PA. The PAE of the PA is determined by five factors, as shown in (2.6):

$$\text{PAE} = \eta_{\text{Device}} \times \eta_{\text{PA Mode}} \times \eta_{\text{PA Gain}} \times \eta_{\text{Output Loss}} \times \eta_{\text{Thermal Aging}} \tag{2.6}$$

The first term, η_{Device}, represents the intrinsic efficiency of the device and can be approximated as:

$$\eta_{\text{Device}} \approx (1 - \frac{V_{knee}}{V_{DD}}) \cdot \frac{Z_{out}}{(Z_{out} + Z_L)} \tag{2.7}$$

Here, the knee voltage (V_{knee}) defines the minimum voltage at which the power device output can swing. The RF voltage swing at the output is determined by (V_{knee}) and V_{DD}. Additionally, the device's large-signal output impedance is a critical factor in η_{Device}, as it will load the device output and shunt away some of the P_{out}. A higher output impedance improves efficiency by reducing power dissipation.

The second term, $\eta_{\text{PA Mode}}$, is associated with the PA's operating mode. Different PA classes, harmonic shaping, and termination techniques are employed to enhance efficiency.

The third term, $\eta_{\text{PA Gain}}$, accounts for the device's power gain and is given by:

$$\eta_{\text{PA Gain}} = (1 - \frac{1}{G_P}) \tag{2.8}$$

This factor determines the required input power and influences the overall PAE of the PA. When the active device has insufficient power gain, this term becomes dominant and reduces efficiency.

The fourth term, $\eta_{\text{Output Loss}}$, represents the loss in the PA's output network and is given by:

$$\text{Loss} = \frac{P_{out}}{P_{PA}} \tag{2.9}$$

The previous example shows that output network loss significantly impacts PA efficiency. Using a balun transformer to convert differential signals to single-ended signals in differential (push-pull) PAs further contributes to power loss and should be carefully considered.

Finally, $\eta_{\text{Thermal Aging}}$ captures the effects of thermal stress, device aging, and reliability on the PA's efficiency. These factors are critical in PA design but are not covered in this dissertation.

2.2.2. CONJUGATE MATCHING VS LOAD LINE MATCHING

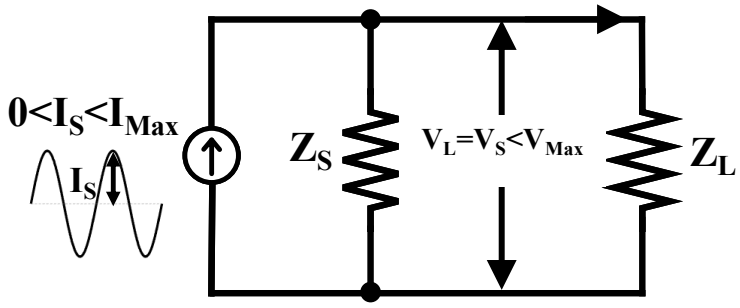


Fig. 2.3. Schematic illustrating the differences between conjugate matching and load line matching.

Fig. 2.3 illustrates a simple circuit model with an RF current source, where the source impedance is Z_S and the load impedance is Z_L. A PA can be designed using conjugate matching or load line matching techniques. Let's explore the differences between these two approaches and determine which is more suitable for PA design.

When the RF current source has no output voltage limitations, conjugate matching ensures maximum power transfer to the load. In this case, the optimal load impedance should be the complex conjugate of the source impedance, given by:

$$\mathrm{Z_L = Z_S{}^*} \tag{2.10}$$

This is known as maximum power transfer matching, where the maximum power delivered to the load is expressed as:

$$\mathrm{Max\ P_L = (1/8) \times (I_{max})^2 \cdot Re\,[R_S]} \tag{2.11}$$

Nevertheless, when the RF current source has both voltage and current limitations, load line matching is more effective in maximizing power delivery. If the source impedance is significantly larger than the load impedance, the optimal load impedance is approximately:

$$\begin{aligned} &\mathrm{Re}(R_L) \approx \frac{V_{\mathrm{Max}}}{I_{\mathrm{Max}}} \quad \text{if} \quad \mathrm{Re}(Z_L) \ll \mathrm{Re}(Z_S), \\ &\mathrm{Im}(Z_L) = (-1) \times \mathrm{Im}(Z_S). \end{aligned} \tag{2.12}$$

In this case, the maximum output power is given by:

$$\text{Max } P_L = (1/2) \times (I_{\max}) \times (V_{\max}) \tag{2.13}$$

Consider a numerical example to better understand the differences between these two matching techniques. Assume a silicon power device with a maximum RF output current amplitude of I_{Max} = 1 A, a maximum RF output voltage amplitude of V_{Max} = 1 V, and a source impedance of R_S = 50 Ω.

For convenience, R_S is assumed to be equal to the output impedance of the active device, which is therefore set to 50 Ω. Consequently, under conjugate matching, the real part of the optimal load impedance is also 50 Ω. Using (2.11), the maximum output power delivered to the load is 6.25 W at I_{Max} = 1 A. This power is represented by the large triangle shaded in light red in Fig. 2.4.

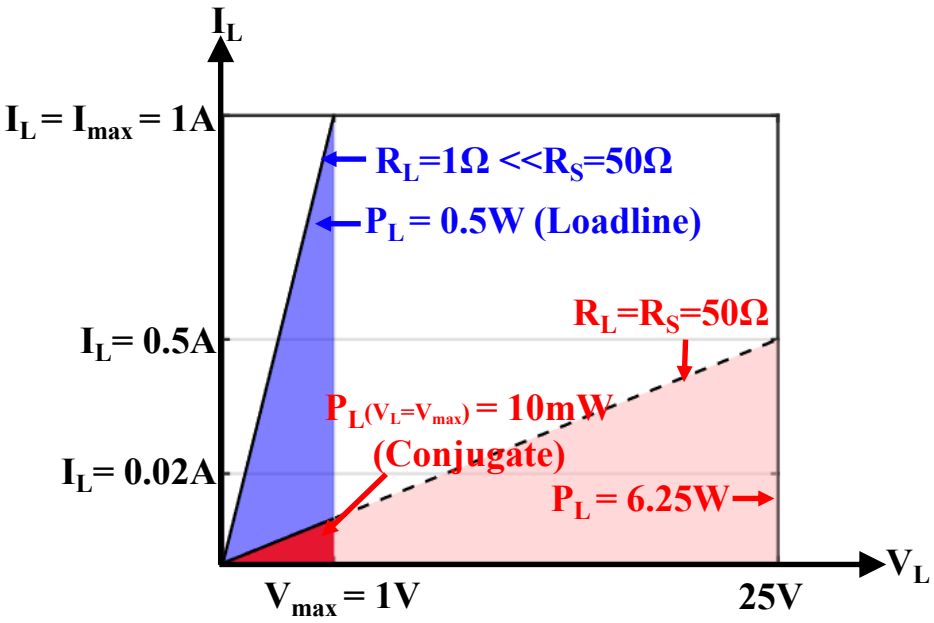


Fig. 2.4. Conjugate versus load line matching.

Nonetheless, under these conditions, the device's output voltage amplitude will be 25 V (0.5 A*50 Ω), far exceeding the 1 V output voltage limit. This condition will lead to device breakdown. If the maximum output voltage is limited to 1 V, the RF current through the 50 Ω load can only be 20 mA, while the source output current (I_S) will be 40 mA. As a result, the actual load power, calculated using (2.13), drops significantly to just 10 mW. This scenario is depicted in Fig. 2.4 as a smaller, dark red triangle.

In contrast, for load line matching, the optimal load impedance is given by the ratio of the maximum voltage swing to the maximum current swing, yielding R_L = 1 Ω (1 V/1 A). Since this impedance is much smaller than the device output impedance (1 << 50), the

assumption for load-line matching holds. Using (2.13), the resulting output power is 0.5 W, which is significantly higher than the power delivered under conjugate matching when considering both current and voltage limitations of the active device. This scenario is represented by the blue triangle in Fig. 2.4.

As shown in Fig. 2.4, the load line matching enables a much larger triangle area, indicating higher output power and efficiency. However, it requires a relatively small load impedance of 1 Ω. Consequently, impedance transformation networks are necessary, inevitably introducing losses and reducing bandwidth. Despite this trade-off, load line matching remains the most efficient approach for PA design, as all practical power devices have maximum output voltage and current constraints that must be considered for reliable operation.

2.2.3. PA CLASSES

Table 2.1 summarizes the most common and fundamental PA classes, which can be broadly categorized into linear mode and switching mode PAs.

Table 2.1
POPULAR PA CLASSES AND THEIR GENERAL PROPERTIES [12]

	Linear mode PAs	**Switching mode PAs**
PA classes	A, B, AB, C, J .... F,[#] F^{-1}[#]	D, D^{-1}, E ....
Transistor operation	RF current source	RF switch
Linearity	Can provide a linear input-output relation	Additional circuits arrangements are needed to obtain a linear signal transfer
Drain efficiency (DE)	Medium - Low	High (100 % Theoretically)
Modulations	Varying amplitude (QAM, etc.)	Constant amplitude
Harmonics	Harmonics suppression	Waveform shaping
Gain	High	Low
Operating frequency	High	Low - Medium

[#] Class F/F^{-1} PAs can be viewed as overdriven linear PAs with harmonic terminations..

Linear PA modes include class A, B, AB, C, and J. Power devices operate primarily as RF current sources with high output impedance in these classes. They offer good linearity, but are limited in efficiency. Due to their ability to support non-constant envelope modulation schemes such as QAM, they are well-suited for applications requiring high linearity. These PAs typically require short-circuit conditions for all output harmonics, except in class J, which utilizes harmonic tuning for improved RF operating bandwidth. Additionally, linear PAs provide high power gain, making them popular choices for mm-wave applications.

The switching PA classes include class D, D^{-1}, and E. Class F/F^{-1} PAs can also be considered switching PAs, but are sometimes viewed as overdriven linear PAs with selective harmonic terminations. In switched-mode PAs, the power devices operate more like RF switches, sacrificing linearity in exchange for higher (theoretical) efficiency, which

can reach up to 100 %. The output harmonics are carefully shaped to achieve the desired voltage and current waveforms, minimizing their overlap and thus maximizing efficiency. However, due to their switching nature, these PAs typically require higher input power and exhibit lower power gain. As a result, they are more commonly used in low- to mid-frequency PA applications rather than in mm-wave systems.

LINEAR MODE PAS

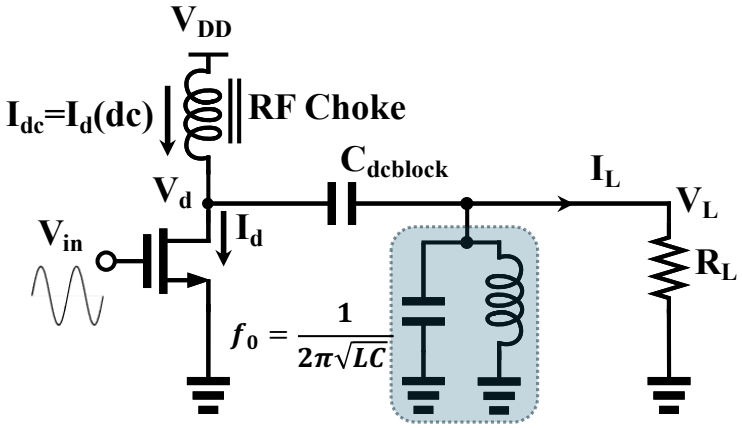


Fig. 2.5. Generic schematic of a linear mode PA.

The generic circuit for the linear mode PAs is shown in Fig. 2.5. The power supply is provided through a large choke inductor (RF choke), while the output is ac-coupled to the load. The load (R_L) represents the optimum load impedance for PA. A shunt LC tank, resonating at f_0, ensures the short termination of all harmonic components.

In **class A** operation, the dc level of the input sine wave (input voltage (V_{in})) driving the device is set above the threshold voltage (V_{TH}). Since the device operates linearly, the output current follows a sinusoidal waveform in phase with V_{in} over the whole RF cycle. The corresponding waveforms for V_{in}, drain current (I_d), and drain voltage (V_d) at maximum P_{out} for class A operation are shown in Fig. 2.6(a).

The ac coupling capacitor ensures that V_L appears around zero volts. Additionally, the RF choke sets the dc value of V_d at V_{DD}, causing V_d to swing between 0 and $2V_{DD}$. Since the LC tank resonates at f_0 and short-circuits all higher harmonics, only a sinusoidal output voltage waveform can exist. The maximum efficiency achievable in class A operation is 50 %, as expressed in (2.14):

$$\begin{aligned} \text{Max } P_L &= (1/2) \cdot V_{DD} \cdot I_{max} \\ \text{Class A } R_{opt} &= V_{DD}/I_{max} \\ \text{Max } P_{dc} &= V_{DD} \cdot I_d(dc) = V_{DD} \cdot I_{max} \\ \text{Max DE} &= P_L/P_{dc} = 50\% \end{aligned} \tag{2.14}$$

Moreover, in back-off mode, when V_{in} is reduced, the output power decreases, but the

dc power consumption remains constant since the dc drain current is fixed for a class A PA. As a result, the back-off efficiency of a class A PA scales linearly with its output or input power.

In **class B** operation, the dc voltage of V_{in} is set at V_{TH}, meaning the device conducts only half of the RF cycle. When the device is ON, the output current follows the input overdrive voltage linearly, producing a half-wave sine waveform, as shown in Fig. 2.6(b). Although the output current waveform is clipped, in the idealized case, the fundamental output power maintains a linear relationship with the input, making class B a linear PA.

The waveforms for V_{in}, I_d, and V_d at maximum $\mathrm{P_{out}}$ for class B are shown in Fig. 2.6(b). Interestingly, the fundamental RF current amplitude of the half-wave sine wave in class B is exactly the same as in class A. However, the dc current is different. Similarly, the maximum V_d swing remains between 0 and $2\mathrm{V_{DD}}$, just like in class A operation. The key difference is that the dc power consumption in class B is lower, enabling it to achieve a peak efficiency of 78.5 % (refer (2.15)).

$$\begin{aligned} \text{Max } \mathrm{P_L} &= (1/2)\cdot V_{DD}\cdot I_{max} \\ \text{Class B } R_{opt} &= V_{DD}/I_{max} \\ \text{Max } \mathrm{P_{dc}} &= V_{DD}\cdot I_d(dc) = V_{DD}\cdot(2/\pi)\cdot I_{max} \\ \text{Max DE} &= \mathrm{P_L}/\mathrm{P_{dc}} = 78.5\% \end{aligned} \tag{2.15}$$

Class AB and class C PAs operate on similar principles. In **class AB** operation, the V_{in} is biased slightly above V_{TH}, but the input swing still drops below V_{TH}, causing the device output current to be clipped. Fig. 2.6(c) illustrates the waveforms for V_{in}, I_d, and V_d at maximum power. Its efficiency is between those of class B and class A.

In **class C** operation, the V_{in} is biased below V_{TH}, meaning that only a small portion of the input waveform rises above V_{TH}, turning the device on for a short period of time. Fig. 2.6(d) shows the waveforms of V_{in}, I_d, and V_d at maximum power. However, the output voltage becomes a clean sinusoidal waveform when passed through an LC resonator.

All linear PA classes can be characterized by their conduction angle (θ), which is defined as:

$$\theta = 2\pi\cdot(\text{Transistor's On Time}/T_0) \tag{2.16}$$

where T_0 is the period of the carrier frequency. Fig. 2.7(a) summarizes the conduction angles and key properties of different linear PA classes.

The dc current (I_{dc}) and the n^{th} harmonic drain current magnitude (I_n) can be expressed as functions of the conduction angle (θ) in radians (refer (2.17) and (2.18)).

$$I_{dc} = \frac{I_{\max}}{2\pi}\cdot\frac{2\cdot\sin(\theta/2)-\theta\cdot\cos(\theta/2)}{1-\cos(\theta/2)} \tag{2.17}$$

$$I_n = \frac{1}{\pi}\cdot\int_{-\alpha/2}^{\alpha/2}\frac{\mathrm{I_{max}}}{1-\cos(\alpha/2)}\cdot(\cos\theta-\cos(\alpha/2))\cdot\cos(n\theta)\,d\theta \tag{2.18}$$

The fundamental component of the drain current ($n=1$) is given by:

$$I_{\text{fund}} = \frac{\mathrm{I_{max}}}{2\pi}\cdot\frac{\alpha-\sin\alpha}{1-\cos(\alpha/2)} \tag{2.19}$$

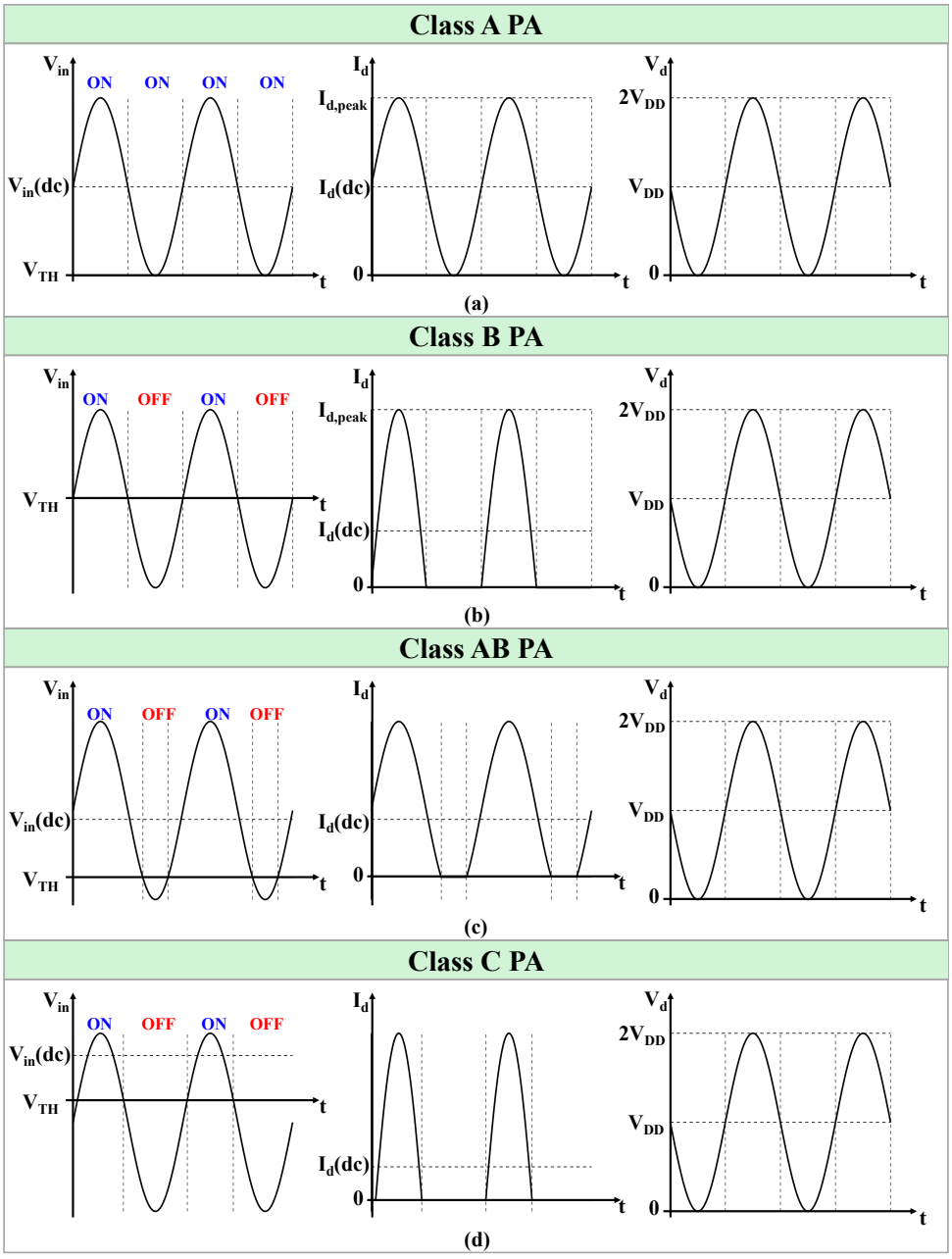


Fig. 2.6. Waveforms of input drive (V_{in}), drain current (I_d), and drain voltage (V_d) for (a) class A, (b) B, (c) AB, and (d) C at maximum power, when using short-circuited conditions for the harmonics.

Consequently, the peak drain efficiency (DE) of a linear PA can be mathematically expressed as a function of the conduction angle:

$$\mathrm{DE} = \frac{1}{4} \cdot \frac{\theta - \sin\theta}{\sin\left(\frac{\theta}{2}\right) - \frac{\theta}{2}\cos\left(\frac{\theta}{2}\right)} \tag{2.20}$$

Class	A	AB	B	C
Gate bias point	0.5	0-0.5	0	<0
Quiescent current	0.5	0-0.5	0	0
Conduction angle	2π	π-2π	π	0-π
Peak efficiency (%)	50	50-78.5	78.5	100
Gain	Maximum by matching	Moderate	Poor	Poor
Linearity	Good	Moderate	Poor	Poor

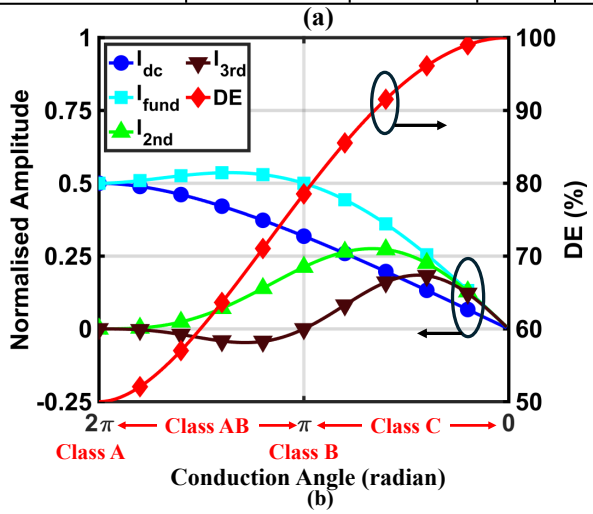


Fig. 2.7. (a) Properties of the linear PA classes (gate bias and output current are normalized between 0-1, and (b) DE, dc, fundamental and harmonics of drain current versus conduction angle.

The DE can be plotted along the dc current (I_{dc}) and the RF currents (I_{fund}, I_{2nd}, and I_{3rd}) as a function of the conduction angle (θ) in Fig. 2.7(b). The fundamental current in class A and class B PAs is actually the same. From Fig. 2.7(b), it is evident that the second and third harmonic components increase as the conduction angle decreases from 2π to $\pi/2$, causing a higher harmonic content as we move from class A to class C PAs, with class C having the highest harmonic content. On the other hand, in deep class C operation, as the conduction angle decreases, the efficiency approaches 100 %. However, the output power also decreases to zero, making deep class C PAs impractical for most applications [22].

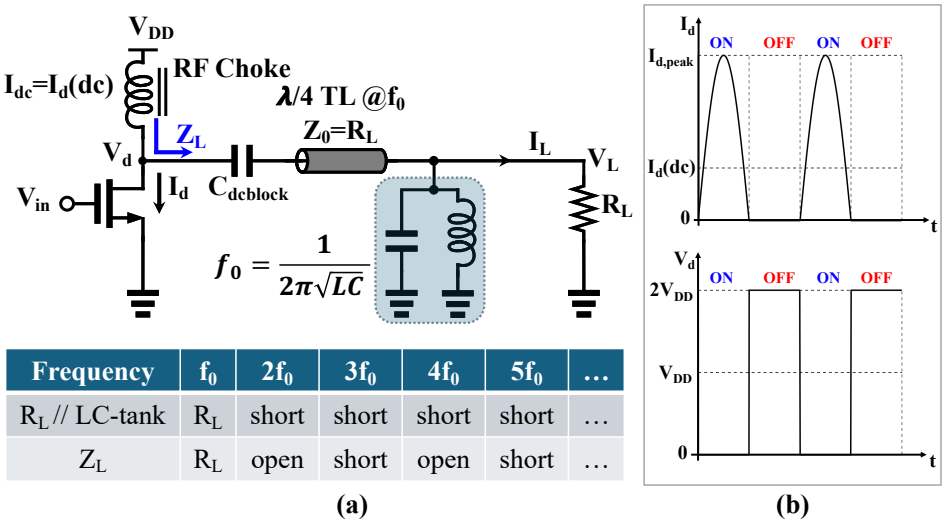
Class J and class J* PAs are linear PAs with reactive 2^{nd} harmonic terminations. The additional second-harmonic components are used only for RF waveform shaping to en-

hance the operating bandwidth and do not contribute to the RF output power. As a result, class J and class J* PAs have the same RF output power, dc power consumption, and efficiency as class B PAs. As stated, the main advantage of class J and class J* PAs is their wideband capability. However, this comes at the cost of a drain voltage swing exceeding $2V_{DD}$, which can pose reliability concerns [23–25].

OVERDRIVEN MODE PAS

A class F PA can be considered as a switching PA but also as an overdriven linear PA with harmonic terminations. The schematic of a class F PA is shown in Fig. 2.8(a). In this configuration, the power device output is connected to a $\lambda/4$ transmission line (TL), loaded with a parallel LC tank that resonates at the fundamental frequency (f_0), parallel to the load, R_L.

The loading of the TL is only equal to R_L at f_0 and will be a short termination at all harmonic frequencies due to the parallel LC tank. Due to $\lambda/4$ TL, Z_L will be R_L at f_0, a short termination at all even-order harmonics, and an open termination at all odd-order harmonics. Therefore, the drain current I_d of the device can only contain the fundamental frequency and even-order harmonics. On the other hand, the drain voltage V_d can only contain the fundamental frequency along with odd-order harmonics.



Frequency	f_0	$2f_0$	$3f_0$	$4f_0$	$5f_0$	…
R_L // LC-tank	R_L	short	short	short	short	…
Z_L	R_L	open	short	open	short	…

(a) (b)

Fig. 2.8. (a) Generic schematic of class F PA, and (b) drain current (I_d) and voltage (V_d) waveforms at maximum power.

Consequently, for 50 % duty cycle operation, V_d will be a square wave, whereas I_d is a half-sine wave, as shown in Fig. 2.8(b). The RF output power (P_{out}) in a class F PA is given as:

$$P_{out} = \frac{1}{2}\left(\frac{4}{\pi}V_{DD}\right)I_{\max} \tag{2.21}$$

The optimum impedance (R_{opt}) in class F is calculated as:

$$R_{opt} = \left(\frac{4}{\pi} V_{DD}\right) I_{\max} \tag{2.22}$$

With the same power device and supply voltage, both P_{out} and R_{opt} are larger than those of class A or class B PAs (see (2.14) and (2.15)). Since there is no voltage or current overlap, there is no power dissipation in the active device of the output stage, and its DE can theoretically reach 100 %.

It has been observed that in practical class F implementation, including many higher harmonics, does not significantly increase efficiency. Moreover, controlling higher harmonics while accommodating drain-source capacitance (C_{ds}) tends to increase circuit complexity and reduce the passive efficiency of the output network. Therefore, most practical class F PAs use up to the third harmonic in the voltage waveform to obtain a good trade-off between DE and output network complexity [26]. Class F PAs can theoretically operate with an efficiency of 90.7 % when considering up to the third harmonic, but are limited to narrow bandwidths due to the stringent requirement for short- and open-circuit harmonic terminations. To overcome this bandwidth limitation, the concept of continuous-mode class F operation has been introduced [27].

Continuous class F (CCF) PAs have the following properties:

1. The fundamental impedance (Z_{1f}) is on a constant resistance circle and can have a reactive part, unlike class F PAs.

2. The second harmonic impedance (Z_{2f}) has a reactive part and no ohmic part.

3. The reactive part of Z_{1f} is inversely proportional to the reactive part of Z_{2f}.

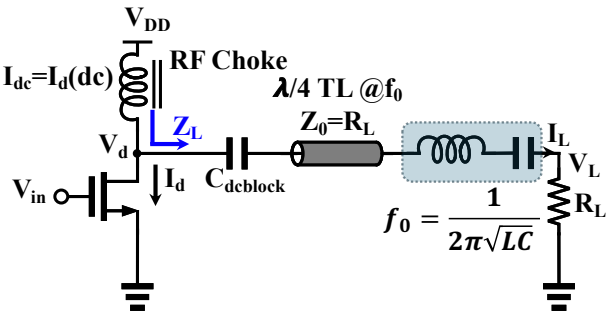
4. The third harmonic impedance (Z_{3f}) is open-circuited, similar to class F PAs.

The key point in CCF PA mode lies in varying the reactive parts of Z_{1f} and Z_{2f} so that PA maintains a constant high efficiency state and maximum output power across the bandwidth. This set of viable loads provides a new design space that increases flexibility in the PA design.

The most important observation to highlight is that PA designers do not necessarily need to provide a short circuit at Z_{2f}, but have the option of a significantly wider design space in which the maximum DE is maintained. This feature helps PA operate in a wider bandwidth. However, the voltage swing in CCF is higher than in class F PA, which can lead to reliability issues that must be considered during the design.

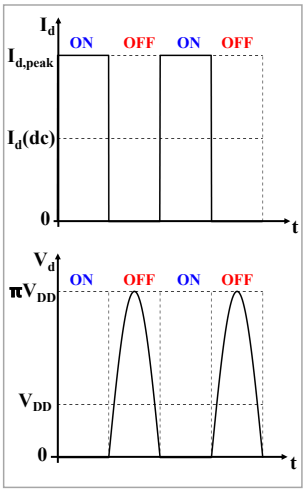
Compared to CCF, extended continuous class F (ECCF) provides flexibility in the real part of Z_{2f} and a variable real part in Z_{1f}, further increasing the design space and flexibility for PA designers. However, this comes at the cost of reduced peak DE [28–31].

The schematic of class F^{-1} PA is shown in Fig. 2.9(a). Compared to class F PA, the class F^{-1} PA uses a series LC tank at f_0 together with load R_L. Due to the presence of $\lambda/4$ TL, Z_L will be R_L at f_0, an open termination at all even-order harmonics, and a short termination at all other harmonics. Therefore, the drain current (I_d) of the power device can only contain the fundamental frequency and all the odd-order harmonics. In contrast,



Frequency	f_0	$2f_0$	$3f_0$	$4f_0$	$5f_0$	…
R_L + LC-tank	R_L	open	open	open	open	…
Z_L	R_L	open	short	open	short	…

(a)



(b)

Fig. 2.9. (a) Generic schematic of class F^{-1} PA, and (b) drain current (I_d) and voltage (V_d) waveforms at maximum power.

the drain voltage (V_d) contains the fundamental frequency and all the even-order harmonics. Fig. 2.9(b) shows a square wave for I_d and a half-wave sine wave for V_d. These waveforms belong to the class F^{-1} PA, which is the dual form of the class F PA.

The P_{out} in a class F^{-1} PA is given by:

$$P_{out} = \frac{1}{2}\left(\frac{4}{\pi} I_{\max}\right)\left(\frac{\pi}{2} V_{DD}\right) = V_{DD} I_{\max} \tag{2.23}$$

The optimum impedance (R_{opt}) in class F^{-1} is calculated as:

$$R_{opt} = \left(\frac{\pi}{2} V_{DD}\right)\left(\frac{4}{\pi} I_{\max}\right) \tag{2.24}$$

Similar to class F, both P_{out} and R_{opt} are larger than those of class A or class B PAs (see (2.14) and (2.15)) when using the same power device and supply voltage. Furthermore, as in class F, there is no overlap between the drain voltage and current waveforms, which leads to zero power dissipation within the device and a theoretical 100 % DE.

SWITCHING MODE PAS

Class B PAs have a nonzero overlap between the drain voltage and current waveforms, which results in power loss within the device and therefore limits PA efficiency.

In contrast, switching PAs operate their active devices as switches. When the switch is on, it behaves like an ideal short circuit, conducting a high current with zero voltage across it. When it is off, it behaves like an ideal open circuit, withstanding large voltage swings without conducting any current. This avoids voltage and current overlap, leading

to zero power dissipation in the device and thus a theoretical efficiency of 100 %. However, switching PAs require careful waveform shaping using combinations of passive and active devices.

One of the most popular switching PAs is the class D PA, which consists of up and down switches driving a series LC tank and load. Since both switches are driven by 50 % complementary square-wave voltages, their resulting currents are complementary half-wave sine waves. The output power (P_{out}) and the dc power consumption (P_{DC}) are the same, so the theoretical drain efficiency is also 100 %. Additionally, class D has low voltage stress, as the voltage across each transistor is equal to the supply voltage [32].

In contrast, class D^{-1} uses two bottom switches with a parallel LC tank and a shunt load. In this configuration, the switch currents are square waves, whereas the voltages are half-wave sine waves. When zero-voltage switching (ZVS) is achieved without any overlap between voltage and current, the theoretical efficiency of class D^{-1} is also 100 % [33, 34].

In class E PAs, the non-negligible device output capacitance is absorbed into the output network. There are two types of class E PAs: zero-voltage switching (ZVS) and zero-current switching (ZCS). In ZVS, the transistor turns on at zero voltage and may also turn on at zero voltage derivative. In these designs, the transistor output capacitance, the choke parasitic capacitance, and the stray capacitance are absorbed into the shunt capacitance. In ZCS, the transistor turns off at zero current, reducing the turn-off switching loss to zero.

Even though class E PAs have a simple output network, the peak voltage factor is $3.6V_{DD}$, creating reliability issues for practical transistors. Since there is no overlap between the device drain voltage and current, the theoretical efficiency for a class E PA is also 100 % [32].

However, switching-mode PAs typically operate at low to medium frequencies and are not suited for mm-wave operation. Therefore, switching-mode PAs are not within the main focus of this dissertation.

2.3. DESIGN CHALLENGES IN MM-WAVE PAS

The design of mm-wave PAs for 5G systems presents unique challenges and strict requirements. This section explores these challenges and outlines existing solutions to address them, as detailed below.

1. INCREASE SATURATED OUTPUT POWER (P_{SAT}):

   Fig. 2.10 shows the P_{sat} of reported CMOS PAs versus operating frequency, based on the survey conducted in [35]. It is observed that at low frequencies, P_{out} is typically limited by application and regulatory constraints. As frequency increases, a monotonic decrease in P_{out} is observed due to device limitations. Additionally, the efficiency of CMOS PAs also decreases with frequency. In summary, achieving high output power and high efficiency at high frequencies remains a significant challenge.

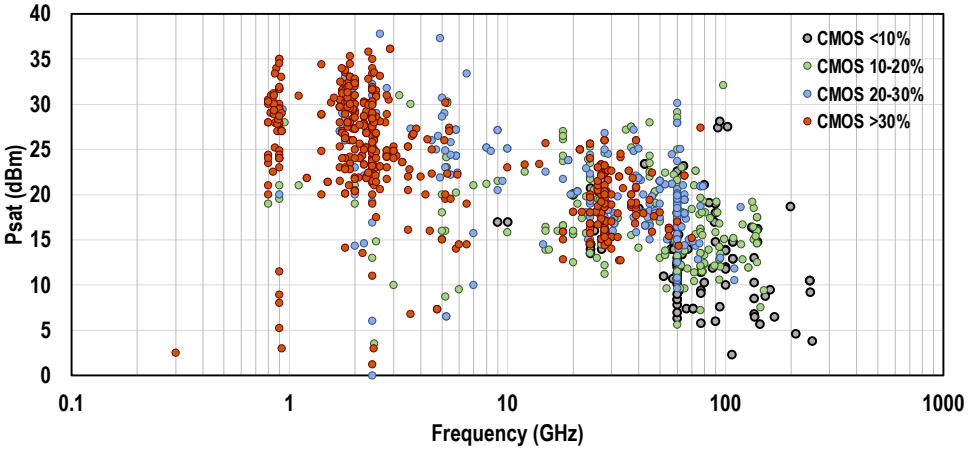


Fig. 2.10. P_{sat} versus frequency for CMOS PAs [35].

The P_{sat} required for each PA in a phased array varies depending on the application scenario, as summarized in Table 1.2. However, as CMOS technology scales to smaller technology nodes, its breakdown voltage decreases, making it increasingly difficult to achieve the required P_{sat}. Existing solutions in the literature can be broadly categorized into techniques focusing on active devices and those focusing on passive structures.

An approach involving active devices to increase the effective breakdown is the stacking of transistors [38] as shown in Fig. 2.11(a). This technique increases both P_{out} and the output impedance, facilitating easier matching to 50 Ω. However, each stacked transistor introduces a time delay, leading to an increase in overlap between the current and voltage waveforms, which reduces efficiency. Furthermore, transistor reliability must be carefully considered during the design process [31].

Alternatively, P_{sat} can be enhanced by power-combining techniques applied to passive structures. One common method is a distributed active transformer (DAT), illustrated in Fig. 2.11(b). The DAT simultaneously performs impedance transformation and power combining for multiple PAs, thus achieving the required P_{out}. This method utilizes symmetric push–pull amplifiers, ac virtual grounds, and magnetic coupling for series power combining [36]. Conventional DAT uses slab inductors as shown in Fig. 2.11(c). A hybrid power combining technique, which integrates DAT with 8-shaped transformers [37], eliminates impedance imbalance between the positive (PA+) and negative (PA−) paths (Fig. 2.11(d)). However, in back-off modes, the efficiency of combining decreases due to increased switch resistance, and the circuit becomes more complex, resulting in greater passive losses.

The Doherty architecture is another widely used power-combining technique. It can be extended from a 2-way to an N-way configuration [39] to achieve higher

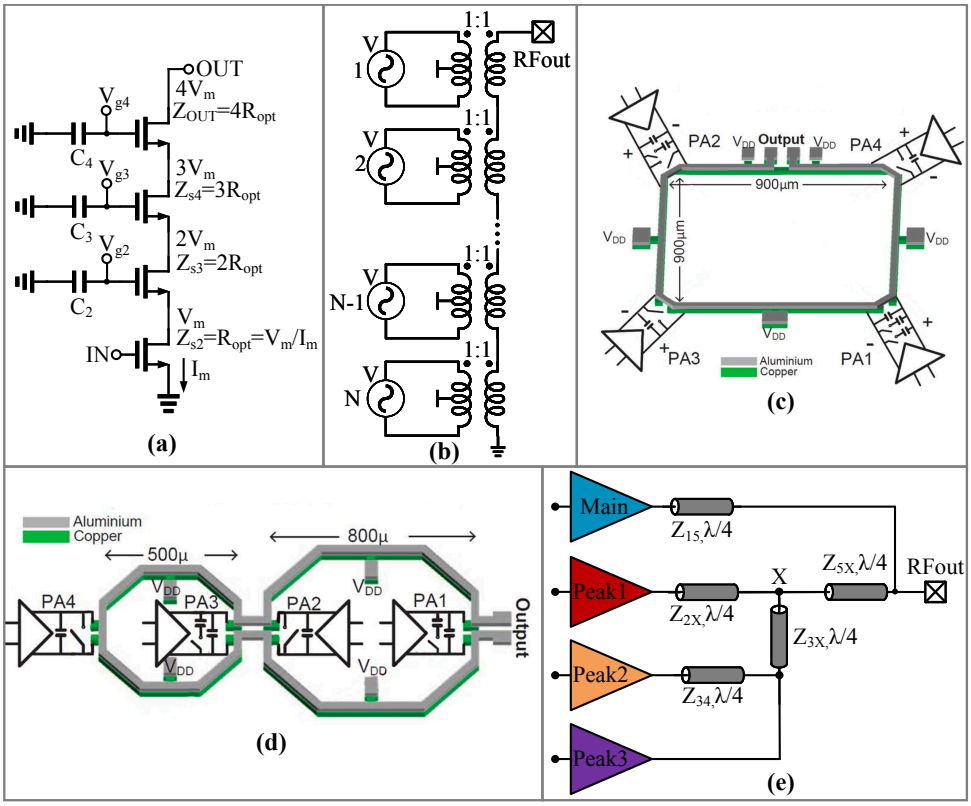


Fig. 2.11. (a) Stack of transistors, (b) *N*-way distributed active transformer (DAT) schematics [36], (c) 4-way DAT layout [37], (d) power combining using hybrid transformer [37], and (e) 4-way Doherty PA.

P_{sat}. A schematic of a 4-way Doherty network is shown in Fig. 2.11(e). This technique also enhances efficiency at deep PBO, significantly improving the average efficiency. Consequently, the Doherty method addresses both the need for higher P_{sat} and better average efficiency. However, the complexity of the output network increases, resulting in greater passive losses, which ultimately degrade the peak efficiency.

2. ENHANCE PA EFFICIENCY:

One of the main challenges in PA design is maintaining high efficiency at saturated output power (P_{sat}). CMOS devices have limited power and voltage swing. Therefore, to generate a large P_{out}, either the output RF current must be increased, or the load impedance must be reduced. This requires larger devices or more devices in parallel. Additionally, a lower impedance necessitates a larger impedance transformation through the matching network. Both of these factors introduce more loss and degrade the overall efficiency of the PA.

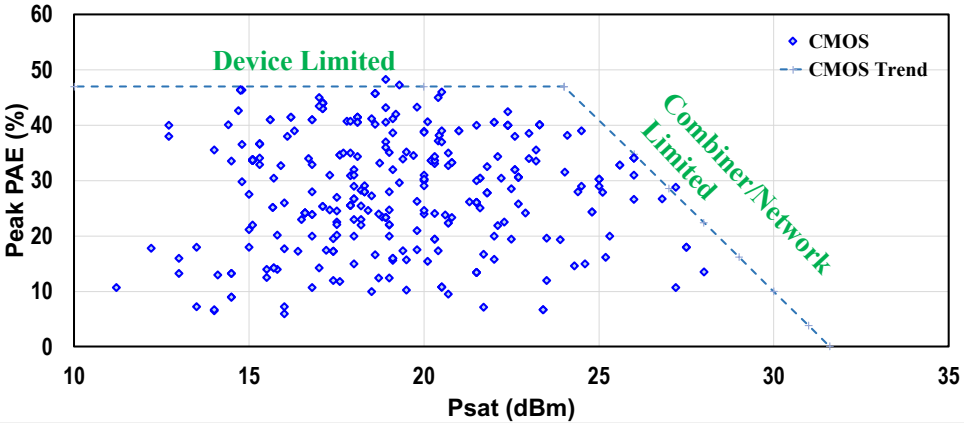
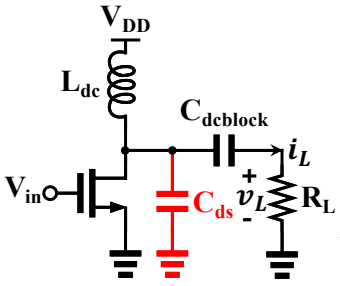


Fig. 2.12. Peak PAE versus P_{sat} for 20 to 50 GHz CMOS PAs [35].

Fig. 2.12 summarizes the saturated power-added efficiency (PAE_{sat}) versus P_{sat} for CMOS PAs operating between 20 and 50 GHz. At P_{sat}<20 dB, the PA's PAE_{sat} is around 45 % for 20 and 50 GHz, which is primarily limited by the intrinsic efficiency of CMOS devices and typical passive losses. This region is referred to as the device-limited regime, as highlighted in Fig. 2.12. However, for P_{sat}>23 dBm, efficiency degrades rapidly because a single silicon device can no longer deliver such a large P_{out}. As a result, more devices and complex passive combining networks are required, which introduce additional losses. This region is known as the combiner/network-limited regime. Therefore, achieving PAs with high P_{out}, high efficiency, and compact area remains a significant challenge.



$$\omega_0 = \frac{1}{\sqrt{L_{dc}C_{ds}}}, i_{L,\omega_0} = \frac{\alpha i_{max}}{2}, v_{L,\omega_0} = \alpha v_{max}$$

$$P_L = \frac{v_L i_L}{2} = \frac{\alpha^2 v_{max} i_{max}}{4} \xrightarrow{v_{max}=V_{DD}} \frac{\alpha^2 V_{DD} i_{max}}{4}$$

$$P_{dc} = V_{dc} I_{dc} = \frac{\alpha V_{DD} i_{max}}{\pi}$$

$$DE_{max} = \frac{P_{L,max}}{P_{dc,max}} = \frac{\pi}{4} (\alpha{=}1)$$

$$DE_{PBO} = \frac{P_L}{P_{dc}} = \alpha \frac{\pi}{4} = \alpha DE_{max}$$

Fig. 2.13. A simplified schematic of class B CMOS PA.

Most traditional linear PAs are designed to operate in class A, AB, B, or C, each differing in conduction angle (refer to Section 2.2.3). However, in these classes, efficiency depends on the input signal and reaches its peak only when the PA operates at maximum power [22]. To illustrate this, Fig. 2.13 shows a simplified schematic of

a CMOS PA. The dc feed inductor (L_{dc}) acts as an RF choke, isolating the dc supply from higher harmonic components, which are shunted by C_{ds}. The output power (P_L) is proportional to α^2, whereas the dc power consumption (P_{dc}) of a class B PA is proportional to α since V_{DD} remains constant. This relationship implies that the efficiency of a class B PA is directly proportional to the input signal amplitude (α) or the square root of the output power.

At PBO, the dc power of a class A PA remains constant, as previously discussed, which means that its efficiency is proportional to the square of the input voltage or directly proportional to P_{out}. Fig. 2.14 illustrates the normalized DE versus P_{out} for class A and class B PAs. At a 6 dB PBO, the efficiency of a class A PA is only 25 % of its peak value, while that of a class B PA is 50 % of its peak value. However, the peak efficiencies of class A and class B PAs are 50 % and 78.5 %, respectively.

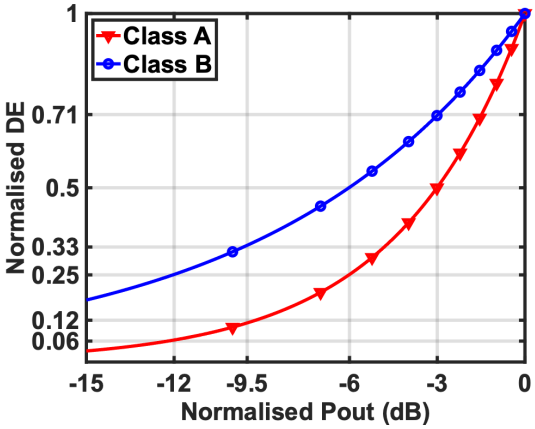


Fig. 2.14. Normalized efficiency versus normalised P_{out} for the class A and class B PAs.

At 6/9.5/12 dB PBO, the efficiency of a class A PA drops to 12.5 %/6 %/3 %, while the efficiency of a class B PA remains higher at 39.25 %/25.9 %/19.6 % for the same PBO levels.

An obvious way to increase the PA efficiency at PBO is to enhance its maximum efficiency. This can be achieved by using class-F/F^{-1} configurations, which differ from class B PAs by keeping odd/even harmonics open-circuited, as discussed in Section 2.2.3. This shaping of voltage waveforms reduces their overlap with current waveforms, thereby increasing peak efficiency. However, these designs require a complex output network to control higher harmonics and are inherently narrowband. To achieve a wider operational bandwidth, continuous classes such as class J/J^* [25] and CCF [30, 31, 40–43] can be employed. Despite their advantages, these techniques involve more complex networks and higher voltage swings, which may raise reliability concerns. Recently, novel PA architectures such as the low-loss distributed balun [44] and dual drive [45] have been proposed to enhance peak efficiency.

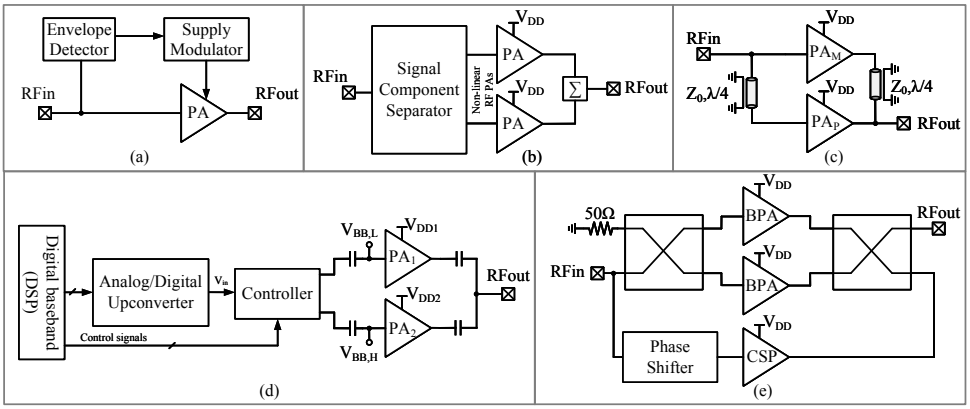


Fig. 2.15. Efficiency enhancement architectures : (a) envelope tracking (ET) PA, (b) outphasing PA, (c) Doherty PA, (d) supply interpolating transmitter, and (e) load-modulated balanced amplifier (LMBA).

As discussed earlier, 5G systems employ complex modulation schemes, such as OFDM and QAM, which exhibit a high PAPR ($\approx$ 11 dB) to achieve a multi-gigabit data rate. Consequently, modern mm-wave PAs must operate in deep PBO. Since the efficiency is proportional to signal amplitude (α) (refer Fig. 2.14), average efficiency degrades in PBO, which negatively impacts the overall TX efficiency. Therefore, achieving high efficiency in both peak and PBO conditions is critical for 5G mm-wave systems, necessitating novel PA architectures with efficiency enhancement techniques.

Efficiency enhancement techniques aim to maintain peak efficiency also at PBO by making the efficiency independent of the signal amplitude (α). These techniques can be broadly classified into supply modulation and load modulation approaches. Envelope tracking (ET) is a technique in which the PA's supply voltage is modulated to track the envelope of the output signal (Fig. 2.15(a)). This makes the PA's power consumption proportional to α^2 instead of α, leading to constant efficiency [46–48]. However, ET PAs require high-speed supply modulators with a high dynamic range. State-of-the-art ET designs currently achieve modulation bandwidths only up to tens of megahertz, making them unsuitable for mm-wave 5G TXs that require modulation bandwidths of up to 1.4 GHz.

In the supply interpolation technique (Fig. 2.15(d)), multiple amplifier branches are connected to different supply voltages. Output power is controlled by activating amplifier branches corresponding to the most desired supply voltages, thereby maintaining efficiency [49]. However, linearity issues during supply switching and the risk of common-mode oscillations at the output require careful design consideration.

Another approach to improve PA efficiency at PBO is by modulating the load. This method keeps the voltage swing constant, and the power delivered to the load becomes proportional to α instead of α^2, thus maintaining the constant efficiency at PBO. Outphasing PAs (Fig. 2.15(b)) combine two phase-modulated constant-

envelop signals to generate the required output signal while maintaining efficiency at both peak and PBO [50–54]. Although outphasing techniques allow the use of nonlinear PAs, such as class E PAs, they require extensive baseband computation, nonlinear I/Q to phase conversion (leading to bandwidth expansion), and complex DPD.

Load-modulated balanced amplifiers (LMBAs) are another example of load modulation techniques (Fig. 2.15(e)). LMBAs consist of balanced PAs (BPAs), a control signal power (CSP) source, and a quadrature hybrid coupler (QHC). LMBAs can handle large RF operating bandwidths since there are no impedance inverters in the output network and the main PA sees a constant loading impedance in contrast to peak amplifiers [55–60]. However, LMBAs make use of hybrid couplers, which require significant die board area that increases passive loss and reduces peak efficiency.

Doherty PAs (Fig. 2.15(c)) also use load modulation techniques. These PAs use quarter-wave transmission lines (QTLs) as impedance inverters, making them inherently narrowband [61–63]. While their efficiency enhancement at PBO is narrowband, broadband operation can be achieved by increasing the complexity of the Doherty network—although at the cost of higher passive losses [64–66].

In conclusion, every technique for enhancing efficiency at PBO has its advantages and limitations. Therefore, developing a compact mm-wave PA with efficiency enhancement capabilities at PBO remains a critical research area for advancing 5G systems.

3. ENSURE PA LINEARITY:

Linearity is one of the most important characteristics of the TX, and the PA is one of the main components dictating the linearity. If the linearity of the TX does not meet the specifications of the standard, then recreating data at the receiver becomes impossible–even if the signal strength is sufficient.

5G networks use advanced complex modulation schemes which demand stringent EVM requirements for in-band linearity, such as $-25/-30$ dB for 64/256-QAM, as well as compliance with emission mask to achieve out-of-band spectral purity [10, 11]. Recent mm-wave linear class B and class AB PA designs [44, 67–74] meet the stringent EVM and ACLR requirements of 5G systems. But these designs don't improve average efficiency. Unfortunately, the linearity performance of a typical Doherty PA is not sufficient to comply with the emission mask of the adopted modulation schemes.

Consequently, DPD techniques, usually implemented in the digital domain, are mandatory to bring the Doherty PA output spectrum within the specified limits [75, 76]. However, this need reduces the benefits of the higher PBO efficiency and represents the most significant drawback for using the Doherty PA configuration in mm-wave antenna arrays. Consequently, finding design solutions to increase Doherty PA's linearity performance remains a critical research area.

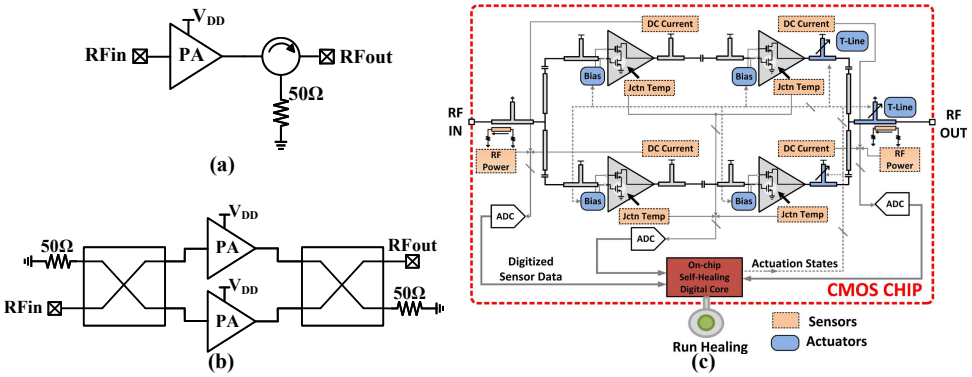


Fig. 2.16. (a) PA with an isolator, (b) balanced PA (BPA), and (c) self-healing PA showing amplifier and self-healing loop [77].

4. INCREASE PA GAIN:

In mm-wave phased array architectures, the input signal reaches each PA's input with a low power level due to losses from preceding stages such as power splitters, phase shifters, and mixers. Thus, the PAs need to have a high gain to compensate for this loss. This will relax the design constraints of the preceding stages [18, 74].

5. PA RESILIENT TO VSWR:

The reflection coefficient (Γ) and voltage standing wave ratio (VSWR) are defined in terms of the load impedance (Z_L) and characteristic impedance (Z_0), which is typically considered to be 50 Ω. They are given by (2.25) and (2.26).

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{2.25}$$

$$VSWR = \frac{1 + |\Gamma|}{1 - |\Gamma|} \tag{2.26}$$

PAs are typically designed assuming that the antenna impedance is 50 Ω or VSWR = 1. However, a higher VSWR will vary the load impedance seen by the PA, degrading P_{sat}, efficiency, and linearity of the entire TX chain. There are two causes for having VSWR $\neq$ 1: a.) Antenna mismatch arises due to environmental conditions. This scenario occurs in handsets. b.) Mutual antenna coupling in phased arrays gives rise to time-varying VSWR. Moreover, efficiency enhancement techniques employing load modulation, such as Doherty, outphasing, and LMBA, make PAs more sensitive to the VSWR [11].

A conventional solution to make PA resilient to VSWR is by employing an isolator at its output (Fig. 2.16(a)). Unfortunately, such ferrite circulators, which provide non-reciprocal isolation, cannot be integrated into a CMOS fabrication process

because they require an external magnet [78]. Consequently, they occupy a large area and are expensive, making them a nonviable solution for a dense phased array. The non-magnetic CMOS circulator using temporal modulation can be integrated, has high antenna-to-TX isolation, and makes the PA resilient to static/time-vary VSWR [79–82]. However, state-of-the-art of integrated mm-wave circulators occupy a large area (>1.3 mm^2), have high TX-to-antenna loss (>3.2 dB) and need additional power to generate their quadrature clocks.

Active load pulling Doherty PA proposed in [83] consists of a reconfigurable unit cell, and it exploits mutual coupling through a multi-port network to achieve VSWR tolerance. It provides PBO efficiency enhancement and output power robustness under VSWR. However, it is resilient to only static VSWR and compromises peak efficiency and linearity.

Similarly, [84] switches between series and parallel Doherty to attain output power robustness under VSWR. While the Doherty operation contributes to PBO efficiency enhancement, the solution is also resilient only to static VSWR variations, compromising peak efficiency and linearity.

The self-healing PA shown in Fig. 2.16(c) maintains output power, efficiency, and linearity robustness under Static/time-varying VSWR, process variation, and transistor mismatch. It consists of a tunable matching network and bias. However, it also requires additional detection, actuation, and control components, which increases overhead. Moreover, it needs time to restore PA performance (around 0.8 seconds) [77].

Recently, mm-wave balanced PAs (BPAs) have been proposed to make the PA resilient to VSWR [21, 74, 85, 86]. These BPA consist of two identical PAs and a QHC, as shown in Fig. 2.16(b). When there is an antenna impedance mismatch, the QHC presents a real load to one PA, whereas the other sees an inverted impedance. This balanced loading condition enables BPA designs to be resilient to VSWR under PBO conditions. However, their implementation requires a large area and introduces additional losses.

6. PA SUPPORTS WIDE MODULATION BANDWIDTH:

To fully leverage the available spectrum, a 5G mm-wave TX needs to support wide modulation bandwidths–up to 1.4 GHz–to achieve multi-gigabit data rates. Therefore, the PA must maintain P_{out}, efficiency, gain, and linearity across the modulation bandwidth. As mentioned earlier, Doherty PAs are inherently narrowband due to QTL. So, developing a PA architecture that supports a wide modulation bandwidth is critical for 5G systems.

2.4. 2-WAY PARALLEL DOHERTY PA

The *N*-way Doherty PA is a promising solution as it provides high output power and improves average efficiency. The most basic form of an *N*-way Doherty PA is the 2-way

Doherty PA. To support the reader, this section analyzes the operation of the 2-way Doherty PA and presents the relevant design equations.

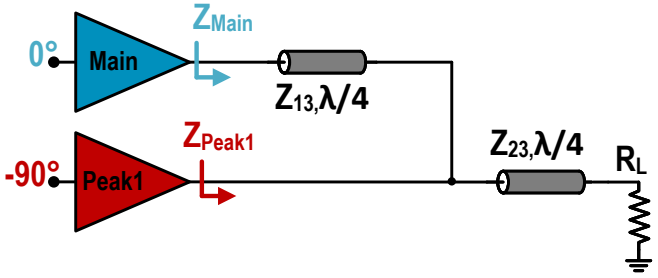


Fig. 2.17. 2-way Doherty schematics.

To generate a given P_{out} and match it to a given load (R_L), a Doherty PA requires two TLs, as shown in Fig. 2.17. The characteristic impedances (Z_0) of these TLs are given by (2.27):

$$\begin{aligned} R_{\text{optmax}} &= \frac{V_{\text{DD}}^2}{2 \cdot P_{\text{sat}}} \\ Z_{13} &= \frac{R_{optmax}}{K1} \\ Z_{23} &= \sqrt{R_L \cdot R_{optmax}} \end{aligned} \tag{2.27}$$

The derivation of these equations is available in Appendix A.

A Doherty PA can be designed as symmetric or asymmetric.

1. Symmetric 2-way Doherty PAs use equal-sized amplifiers, fixing the K_1 at 0.5.
2. Asymmetric Doherty PAs use unequal-sized amplifiers, meaning the PAs deliver different maximum currents, determined by the back-off point (K_1).

In integrated circuit (IC) design, a symmetrical Doherty PA is preferred because it enables the reuse of the same circuit topology for each PA, simplifying the design process and reducing the development time.

Fig. 2.18(a)/(b)/(c) present the voltage, current, and impedance profiles for the main and peak PAs in a symmetric 2-way Doherty PA designed to generate 22 dBm. The efficiency curve for the symmetric 2-way Doherty PA is illustrated in Fig. 2.18(d).

2.5. SUMMARY

In this chapter, the PA is identified as one of the main bottlenecks in TX design. Performance metrics and primary PA classes are discussed, followed by a summary of the key challenges and trade-offs in mm-wave PA design, as illustrated in Fig. 2.19.

The advantages and disadvantages of existing solutions to these challenges are examined, along with a simple 2-way parallel Doherty PA. N-way Doherty PAs are promising candidates for achieving the required power levels and improving the average efficiency

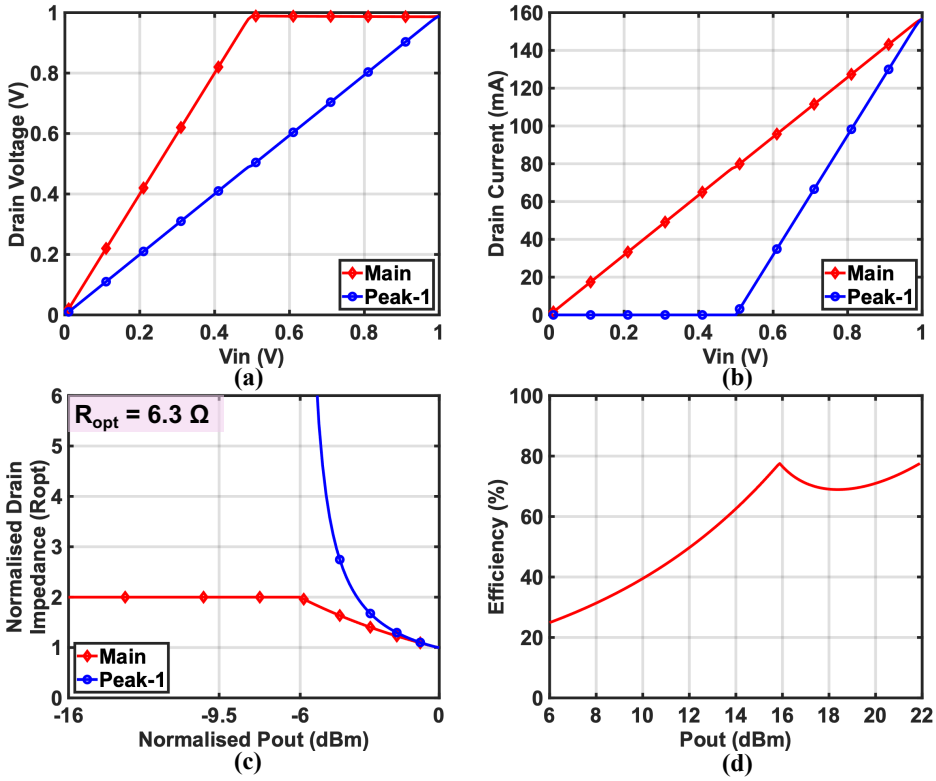


Fig. 2.18. (a) Drain voltage, (b) drain current, (c) drain impedance, and (d) DE of a symmetrical 2-way Doherty network.

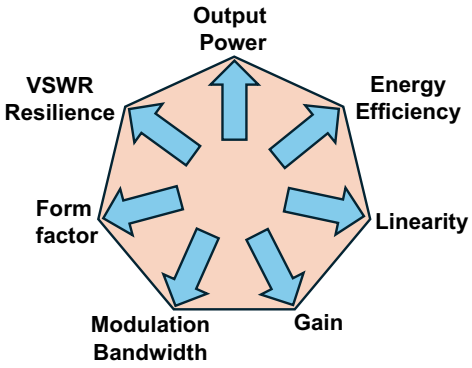


Fig. 2.19. Design challenges in PA

in CMOS technology, which is limited by the supply voltage. However, they are typically narrowband, have low gain, exhibit nonlinearity, and are more sensitive to VSWR. Since mm-wave N-way Doherty PAs remain an active area of research, Chapter 3 will explore the design methodology of N-way parallel Doherty PAs and the trade-offs involved in selecting the optimal Doherty order.

3

Design and Analysis of Compact N-Way Doherty Power Combiners

This chapter presents a design procedure for compact lumped-element 3-/4-/5*-way Doherty power combiners suitable for mm-wave 5G TXs. Among them, the* 3*-way Doherty power combiner is favored due to its low complexity and compact layout, while providing an excellent average drain efficiency (DE_{avg}) in deep power back-off (PBO). Based on the metal stack of a 40 nm CMOS process, a 3-way Doherty power combiner can provide a simulated passive efficiency of more than 60 % at* 12 dB *PBO and a 10 % drain-efficiency bandwidth ($BW_{DE10\%}$)/3 dB power bandwidth (BW_{3dB}) of 8/15 GHz at 30 GHz.*

This chapter is based on the paper published in the IEEE Int. Symp. on Circuits and Syst. [87].

3.1. INTRODUCTION

As previously discussed, the mm-wave spectrum is important to many emerging applications, including radar sensors and 5G cellular networks. The latter networks employ spectrally efficient complex modulation schemes such as QAM and OFDM to achieve multi-Gbit/s data transmission and low-latency line-of-sight links [3–5]. As detailed in Table 1.2, these modulation schemes pose significant challenges due to their high PAPRs. These challenges place stringent demands on PAs, requiring considerations for P_{out}, average efficiency, EVM for in-band linearity, and ACLRs for out-of-band spectral purity [10, 11]. The P_{avg} and P_{sat} requirements for various 5G scenarios are detailed in Table 1.2.

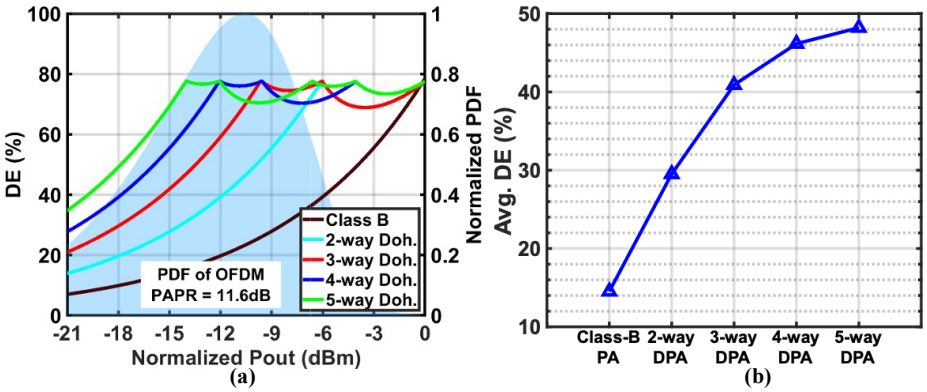


Fig. 3.1. (a) DE vs. P_{out}, and (b) an OFDM signal's average DE with PAPR = 11.6 dB for class B and N-way Doherty PAs.

Fig. 3.1(a) shows DE versus normalized P_{out} for different PA architectures, including 2-way, 3-way, 4-way, and 5-way Doherty configurations using ideal class B PAs and output networks. The average DE, shown in Fig. 3.1(b), is calculated by multiplying the probability distribution function (PDF) of the 256-QAM OFDM signal with the DE of the PA and integrating versus power. This graph shows the average DE for the mentioned PA architectures using an OFDM signal with a PAPR of 11.6 dB. However, Fig. 3.1(b) shows that high PAPR requires a mm-wave TX with high efficiency in PBO. Specifically, a single TX line up in class B achieves with such a signal only 14 % average DE assuming an ideal PA and lossless output network.

This explains why recent mm-wave linear (class B and AB) PA designs do not achieve high average efficiency, even though they meet the EVM and ACLR requirements of 5G systems [44, 67–73]. To address the average efficiency and P_{out} issues in TXs, techniques such as outphasing [51–54], LMBAs [57, 58], and N-way Doherty architectures [21, 64–66, 84, 88–98] have been explored. Outphasing PA demands significant baseband resources for generating outphasing signals. LMBA supports wideband RF operation, but its power combiner occupies a substantial die area, resulting in high insertion loss and reduced peak efficiency. Moreover, applying DPD in LMBA architectures is also challenging.

Among the various N-way Doherty configurations, the 2-way Doherty PA is most commonly realized [21, 64–66, 84, 88–95]. Nonetheless, this configuration does not fully ad-

dress the challenge of enhancing average efficiency for signals with high PAPRs, approximating 12 dB, as inferred from Fig. 3.1(b). Additionally, generating more than 21 dBm P_{out} for the backhaul scenario (Table 1.2) by utilizing only two power devices with CMOS technology is challenging without using additional power combining. Furthermore, the average DE does not show substantial improvement beyond the 4-way Doherty architecture for signals with a PAPR of 12 dBm.

Section 3.2 of this chapter discusses design equations for calculating the Z_0 impedances of the TLs used in the compact N-way Doherty power combiners (3-/4-/5-way Doherty). In Section 3.3, 3-/4-/5-way Doherty networks are designed with lumped components, replacing TLs by their high-pass (HP) equivalent. This section also analyzes the designed N-way Doherty PAs in terms of P_{out} and DE at peak power and PBO versus frequency and under VSWR conditions.

3.2. DESIGN OF N-WAY DOHERTY NETWORKS

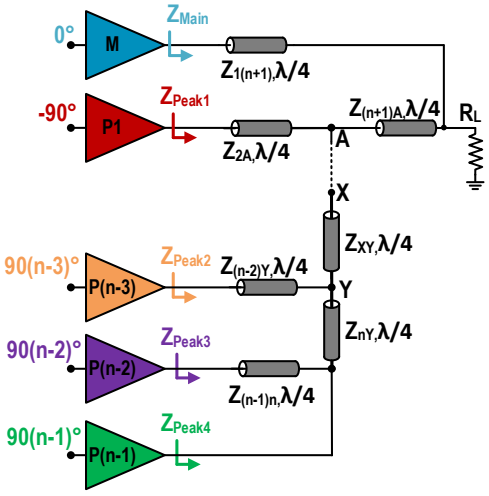


Fig. 3.2. N-way Doherty structure.

Fig. 3.2 depicts N-way Doherty combiners that are inspired by [39]. In this combiner, in deep PBO, when only the main PA is active, the (direct) signal path between the main PA output and the overall Doherty PA output entails minimal power loss. Moreover, its efficiency is only affected by the off-state impedance of the peak-1 PA. Note that, for a symmetrical 3-/4-/5-way Doherty, the deep back-off point happens at 9.5 dB, 12 dB, and 14 dB, respectively, indicating that, at 12 dB PBO, 4-/5-way Doherty combiners are ideal candidates to enhance DE. The following sub-sections disclose the design procedures of 3-/4-/5-way Doherty combiners and subsequently compare their performance at 12 dB PBO.

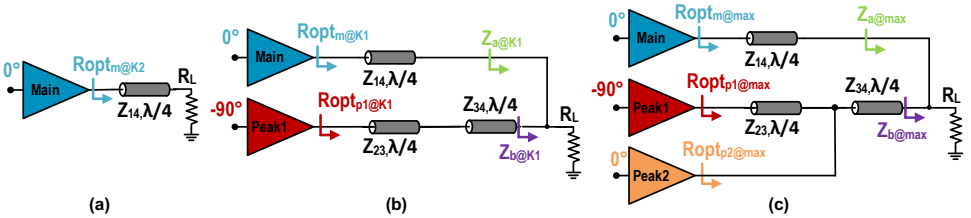


Fig. 3.3. 3-way Doherty network at (a) back-off K_2, (b) back-off K_1, and (c) peak power.

3.2.1. 3-WAY DOHERTY PA

Fig. 3.3(c) shows the 3-way Doherty structure using quarter-wavelength TLs. Their characteristic impedances (Z_{14}, Z_{23}, and Z_{34}) can be determined by analyzing the circuit's Kirchhoff's Voltage Law (KVL) and Kirchhoff's Current Law (KCL) at the back-off conditions (K_2 and K_1) and its full (maximum) power. At the second back-off (K_2), the following conditions are enforced for the voltage of the main PA ($V_{\mathrm{m@K_2}}$), the currents of the peak-1 PA ($I_{\mathrm{p1@K_2}}$), peak-2 PA ($I_{\mathrm{p2@K_2}}$), and main PA ($I_{\mathrm{m@K_2}}$):

$$\begin{aligned} V_{\mathrm{m@K_2}} &= V_{\max} = V_{\mathrm{DD}} \\ I_{\mathrm{p1@K_2}} &= I_{\mathrm{p2@K_2}} = 0 \\ I_{\mathrm{m@K_2}} &= I_{\mathrm{m@F}} \cdot K_2 \end{aligned} \tag{3.1}$$

At the first back-off point (K_1), the following conditions are inferred for the voltages of the main PA ($V_{\mathrm{m@K_1}}$), peak-1 PA ($V_{\mathrm{p1@K_1}}$), currents of peak-2 PA ($I_{\mathrm{p2@K_1}}$), main PA ($I_{\mathrm{m@K_1}}$), and peak-1 PA ($I_{\mathrm{p1@K_1}}$):

$$\begin{aligned} V_{\mathrm{m@K_1}} &= V_{\mathrm{p1@K_1}} = V_{\max} = V_{\mathrm{DD}} \\ I_{\mathrm{p2@K_1}} &= 0 \\ I_{\mathrm{m@K_1}} &= I_{\mathrm{m@F}} \cdot K_1 \\ I_{\mathrm{p1@K_1}} &= I_{\mathrm{p1@F}} \cdot \frac{K_1 - K_2}{1 - K_2} \end{aligned} \tag{3.2}$$

At its maximum power, the following conditions are assumed for the voltages of the main PA ($V_{\mathrm{m@F}}$), peak-1 PA ($V_{\mathrm{p1@F}}$), and peak-2 PA ($V_{\mathrm{p2@F}}$):

$$V_{\mathrm{m@F}} = V_{\mathrm{p1@F}} = V_{\mathrm{p2@F}} = V_{\max} = V_{\mathrm{DD}} \tag{3.3}$$

The back-off points can be defined as

$$\begin{aligned} K_2^2 &= \frac{P_{\mathrm{m@K_2}}}{P_{\mathrm{total@max}}} \\ K_1^2 &= \frac{P_{\mathrm{m@K_1}} + P_{\mathrm{p1@K_1}}}{P_{\mathrm{total@max}}} \end{aligned} \tag{3.4}$$

where, $P_{\mathrm{total@max}} = P_{\mathrm{m@max}} + P_{\mathrm{p1@max}} + P_{\mathrm{p2@max}}$

Using (3.1), (3.2), (3.3), and (3.4), we can calculate ratios of the maximum current carried by main, peak-1, and peak-2 PAs.

$$I_{\text{m@max}} : I_{\text{p1@max}} : I_{\text{p2@max}} = [K_2 : K_1 \cdot (1-K_2) : (1-K_1) \cdot (1-K_2)] \cdot I_{\text{max}} \\ \text{where, } I_{\text{max}} = I_{\text{m@max}} + I_{\text{p1@max}} + I_{\text{p2@max}} \tag{3.5}$$

The optimum impedance that a single PA requires to deliver a given P_{sat} is:

$$Ropt_{\text{max}} = \frac{V_{\text{DD}}^2}{2 \cdot P_{\text{sat}}} = \frac{V_{\text{DD}}}{I_{\text{max}}} \tag{3.6}$$

At peak power, the optimum impedances seen by the main, peak-1, and peak-2 PAs are given by (3.7), (3.8), and (3.9).

$$Ropt_{\text{m@max}} = \frac{V_{\text{DD}}}{I_{\text{m@max}}} = \frac{V_{\text{DD}}}{I_{\text{max}} \cdot K_2} = \frac{Ropt_{\text{max}}}{K_2} \tag{3.7}$$

$$Ropt_{\text{p1@max}} = \frac{V_{\text{DD}}}{I_{\text{p1@max}}} = \frac{Ropt_{\text{max}}}{K_1 \cdot (1-K_2)} \tag{3.8}$$

$$Ropt_{\text{p2@max}} = \frac{V_{\text{DD}}}{I_{\text{p2@max}}} = \frac{Ropt_{\text{max}}}{(1-K_1) \cdot (1-K_2)} \tag{3.9}$$

At back-off K_2, the impedance seen by the main PA can be obtained by using (3.7) and (3.1).

$$Ropt_{\text{m@K}_2} = \frac{V_{\text{m@K}_2}}{I_{\text{m@K}_2}} = \frac{V_{\text{DD}}}{I_{\text{m@max}} \cdot K_2} = \frac{Ropt_{max}}{K_2^2} \tag{3.10}$$

From the schematic in Fig. 3.3(a), we can get the following equation:

$$Z_{14} = \sqrt{R_{\text{L}} * Ropt_{\text{m@K}_2}} \tag{3.11}$$

The impedance seen by the main and peak-1 PAs at back-off K_1 is given by (3.12) and (3.13), respectively.

$$Ropt_{\text{m@K}_1} = \frac{V_{\text{m@K}_1}}{I_{\text{m@K}_1}} = \frac{V_{\text{DD}}}{I_{\text{m@max}} \cdot K_1} = \frac{Ropt_{max}}{K_1 \cdot K_2} \tag{3.12}$$

$$Ropt_{\text{p1@K}_1} = \frac{V_{\text{p1@K}_1}}{I_{\text{p1@K}_1}} = \frac{Ropt_{max}}{K_1 \cdot (K_1 - K_2)} \tag{3.13}$$

From the schematic in Fig. 3.3(b), we can get the following equation:

$$\frac{1}{Z_{\text{a@K}_1}} + \frac{1}{Z_{\text{b@K}_1}} = \frac{1}{R_{\text{L}}} \tag{3.14}$$

The impedance seen by each PA (main, peak-1, and peak-2) is given by (3.7), (3.8), and (3.9). From the schematic in Fig. 3.3(c), we can obtain the following equation.

$$\frac{1}{Z_{\text{a@max}}} + \frac{1}{Z_{\text{b@max}}} = \frac{1}{R_{\text{L}}} \tag{3.15}$$

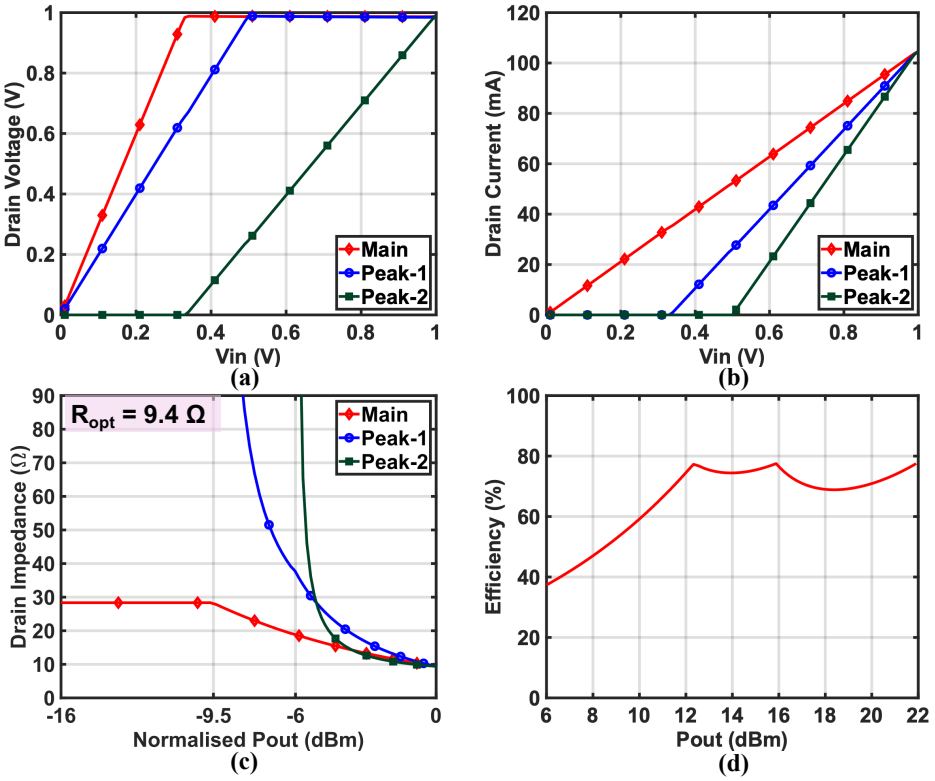


Fig. 3.4. (a) Drain voltage, (b) drain current, (c) drain impedance, and (d) DE of a symmetrical 3-way Doherty network.

In this regard, from the three equations ((3.11), (3.14), and (3.15)), the generalized equations for the Z_0 of the three TLs (Z_{14}, Z_{23}, and Z_{34}) can be calculated in terms of $Ropt_{\max}$, V_{DD}, R_L, K_1, and K_2 (3.16).

$$\begin{aligned} Z_{14} &= \frac{\sqrt{R_L \cdot Ropt_{\max}}}{K_2} \\ Z_{23} &= \frac{Ropt_{\max}}{K_1 \cdot (1-K_2)} \\ Z_{34} &= \frac{\sqrt{R_L \cdot Ropt_{\max}}}{(1-K_2)} \end{aligned} \tag{3.16}$$

The equations for a symmetrical 3-way Doherty, along with their corresponding back-off points, are provided in Table 3.1. Fig. 3.4(a)/(b)/(c) present the voltage, current, and impedance profiles for the main and peak PAs in a symmetrical 3-way Doherty PA. The efficiency curve for the symmetrical 3-way Doherty PA is illustrated in Fig. 3.4(d).

3.2.2. 4-WAY DOHERTY PA

Fig. 3.5(d) depicts the 4-way Doherty network using quarter-wavelength TLs. The characteristic impedance of TLs (Z_{15}, Z_{2X}, Z_{3X}, Z_{5X}, and Z_{34}) can be calculated by analyzing the circuit at the back-off conditions (K_1, K_2, and K_3) and peak power. At 3^{rd} back-off (K_3), the following conditions can be obtained:

$$\begin{aligned} V_{\mathrm{m@K_3}} &= V_{\max} = V_{\mathrm{DD}} \\ I_{\mathrm{p1@K_3}} &= I_{\mathrm{p2@K_3}} = I_{\mathrm{p3@K_3}} = 0 \\ I_{\mathrm{m@K_3}} &= I_{\mathrm{m@F}} \cdot K_3 \end{aligned} \tag{3.17}$$

At 2^{nd} back-off (K_2), the following conditions can be obtained:

$$\begin{aligned} V_{\mathrm{m@K_2}} &= V_{\mathrm{p1@K_2}} = V_{\max} = V_{\mathrm{DD}} \\ I_{\mathrm{p2@K_2}} &= I_{\mathrm{p3@K_2}} = 0 \\ I_{\mathrm{m@K_2}} &= I_{\mathrm{m@F}} \cdot K_2 \\ I_{\mathrm{p1@K_2}} &= I_{\mathrm{p1@F}} \cdot \frac{K_2 - K_3}{1 - K_3} \end{aligned} \tag{3.18}$$

At 1^{st} back-off (K_1), the following conditions can be obtained:

$$\begin{aligned} V_{\mathrm{m@K_1}} &= V_{\mathrm{p1@K_1}} = V_{\mathrm{p2@K_1}} = V_{\max} = V_{\mathrm{DD}} \\ I_{\mathrm{p3@K_1}} &= 0 \\ I_{\mathrm{m@K_1}} &= I_{\mathrm{m@F}} \cdot K_1 \\ I_{\mathrm{p1@K_1}} &= I_{\mathrm{p1@F}} \cdot \frac{K_1 - K_3}{1 - K_3} \\ I_{\mathrm{p2@K_1}} &= I_{\mathrm{p2@F}} \cdot \frac{K_1 - K_2}{1 - K_2} \end{aligned} \tag{3.19}$$

At peak power, the following conditions can be obtained:

$$V_{\mathrm{m@F}} = V_{\mathrm{p1@F}} = V_{\mathrm{p2@F}} = V_{\mathrm{p3@F}} = V_{\max} = V_{\mathrm{DD}} \tag{3.20}$$

The back-off point can be defined as

$$\begin{aligned} K_3^2 &= \frac{P_{\mathrm{m@K_3}}}{P_{\mathrm{total@max}}} \\ K_2^2 &= \frac{P_{\mathrm{m@K_2}} + P_{\mathrm{p1@K_2}}}{P_{\mathrm{total@max}}} \\ K_1^2 &= \frac{P_{\mathrm{m@K_1}} + P_{\mathrm{p1@K_1}} + P_{\mathrm{p2@K_1}}}{P_{\mathrm{total@max}}} \end{aligned} \tag{3.21}$$

$$\text{where, } P_{\mathrm{total@max}} = P_{\mathrm{m@max}} + P_{\mathrm{p1@max}} + P_{\mathrm{p2@max}} + P_{\mathrm{p3@max}}$$

Using the Eqs. (3.17) to (3.21), we can calculate the ratios of the maximum current carried by the main, peak-1, peak-2, and peak-3 PAs by analyzing the circuit's KVL and KCL

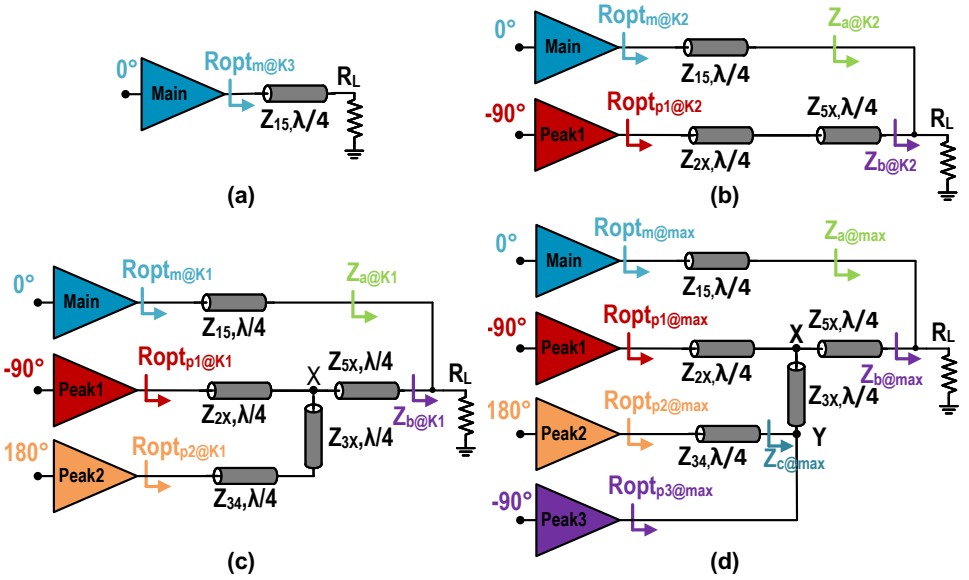


Fig. 3.5. 4-way Doherty network at (a) back-off K_3, (b) back-off K_2, (c) back-off K_1, and (d) peak power

conditions at the back-off points (K_1, K_2, and K_3) and the full power, similar to its 3-way Doherty counterpart.

$$\begin{aligned} &I_{\mathrm{m@max}} : I_{\mathrm{p1@max}} : I_{\mathrm{p2@max}} : I_{\mathrm{p3@max}} = \\ &[K_3 : K_2 \cdot (1-K_3) : (1-K_2) \cdot (K_1-K_3) : (1-K_1) \cdot (1-K_2)] \cdot I_{\max} \end{aligned} \tag{3.22}$$

At peak power, the optimum impedance seen by the main, peak-1, peak-2, and peak-3 PAs are given by (3.23), (3.24), (3.25), and (3.26)

$$Ropt_{\mathrm{m@max}} = \frac{Ropt_{\max}}{K_3} \tag{3.23}$$

$$Ropt_{\mathrm{p1@max}} = \frac{Ropt_{\max}}{K_2 \cdot (1-K_3)} \tag{3.24}$$

$$Ropt_{\mathrm{p2@max}} = \frac{Ropt_{\max}}{(1-K_2) \cdot (K_1-K_3)} \tag{3.25}$$

$$Ropt_{\mathrm{p3@max}} = \frac{Ropt_{\max}}{(1-K_1) \cdot (1-K_2)} \tag{3.26}$$

At back-off K_3, the impedance seen by the main PA can be calculated by using (3.23) and (3.17).

$$Ropt_{\mathrm{m@K_3}} = \frac{V_{\mathrm{m@K_3}}}{I_{\mathrm{m@K_3}}} = \frac{V_{\mathrm{DD}}}{I_{\mathrm{m@max}} \cdot K_3} = \frac{Ropt_{max}}{K_3^2} \tag{3.27}$$

From the schematic in Fig. 3.5(a), we can get the following equation.

$$Z_{15} = \sqrt{R_{\mathrm{L}} * Ropt_{\mathrm{m@K_3}}} \tag{3.28}$$

The impedance seen by the main PA at back-off K_2 can be calculated by using (3.23) and (3.18).

$$Ropt_{\mathrm{m@K2}} = \frac{V_{\mathrm{m@K_2}}}{I_{\mathrm{m@K_2}}} = \frac{V_{\mathrm{DD}}}{I_{\mathrm{m@max}} \cdot K_2} = \frac{Ropt_{max}}{K_2 \cdot K_3} \tag{3.29}$$

The impedance seen by the peak-1 PA at back-off K_2 can be calculated by using (3.24) and (3.18).

$$Ropt_{\mathrm{p1@K_2}} = \frac{V_{\mathrm{p1@K_2}}}{I_{\mathrm{p1@K_2}}} = \frac{V_{\mathrm{DD}}}{I_{\mathrm{p1@max}}} \cdot \frac{1-K_3}{K_2-K_3} = \frac{Ropt_{max}}{K_2 \cdot (K_2-K_3)} \tag{3.30}$$

From the schematic in Fig. 3.5(b), we can get the following equation:

$$\frac{1}{Z_{\mathrm{a@K_2}}} + \frac{1}{Z_{\mathrm{b@K_2}}} = \frac{1}{R_{\mathrm{L}}} \tag{3.31}$$

The impedance seen by the main PA at back-off K_1 can be calculated by using (3.23) and (3.19).

$$Ropt_{\mathrm{m@K_1}} = \frac{V_{\mathrm{m@K_1}}}{I_{\mathrm{m@K_1}}} = \frac{V_{\mathrm{DD}}}{I_{\mathrm{m@max}} \cdot K_1} = \frac{Ropt_{max}}{K_1 \cdot K_3} \tag{3.32}$$

The impedance seen by the peak-1 PA at back-off K_1 can be calculated by using (3.24) and (3.19).

$$Ropt_{\mathrm{p1@K_1}} = \frac{V_{\mathrm{p1@K_1}}}{I_{\mathrm{p1@K_1}}} = \frac{V_{\mathrm{DD}}}{I_{\mathrm{p1@max}}} \cdot \frac{1-K_3}{K_1-K_3} = \frac{Ropt_{max}}{K_2 \cdot (K_1-K_3)} \tag{3.33}$$

The impedance seen by the peak-2 PA at back-off K_1 can be calculated by using (3.25) and (3.19).

$$Ropt_{\mathrm{p2@K_1}} = \frac{V_{\mathrm{p2@K_1}}}{I_{\mathrm{p2@K_1}}} = \frac{V_{\mathrm{DD}}}{I_{\mathrm{p2@max}}} \cdot \frac{1-K_2}{K_1-K_2} = \frac{Ropt_{max}}{(K_1-K_2) \cdot (K_1-K_3)} \tag{3.34}$$

From the schematic in Fig. 3.5(c), we can get the following equation:

$$\frac{1}{Z_{\mathrm{a@K_1}}} + \frac{1}{Z_{\mathrm{b@K1}}} = \frac{1}{R_{\mathrm{L}}} \tag{3.35}$$

The impedance seen by each PA (main, peak-1, peak-2 and peak-3) is given by (3.23), (3.24), (3.25, and (3.26). From the schematic in Fig. 3.5(d), we can get the following equation:

$$\frac{1}{Z_{\mathrm{a@max}}} + \frac{1}{Z_{\mathrm{b@max}}} = \frac{1}{R_{\mathrm{L}}} \tag{3.36}$$

The current delivered by peak-2 and peak-3 PAs at peak power is $(1-K_2) \cdot (K_1-K_3) \cdot I_{\mathrm{max}}$ and $(1-K_1) \cdot (1-K_2) \cdot I_{\mathrm{max}}$, respectively (3.22). To determine the ratio between the impedances $Z_{\mathrm{c@max}}$ and $Ropt_{\mathrm{p3@max}}$, we apply KCL at node Y (See 3.5(d)), yielding the fifth equation.

$$\begin{aligned} Z_{\mathrm{c@max}} &= Ropt_{\mathrm{p3@max}} \cdot \frac{1-K_1}{K_1-K_3} \\ Z_{34} = \sqrt{Z_{\mathrm{c@max}} \cdot Ropt_{\mathrm{p2@max}}} &= \frac{Ropt_{\mathrm{max}}}{(1-K_2) \cdot (K_1-K_3)} \end{aligned} \tag{3.37}$$

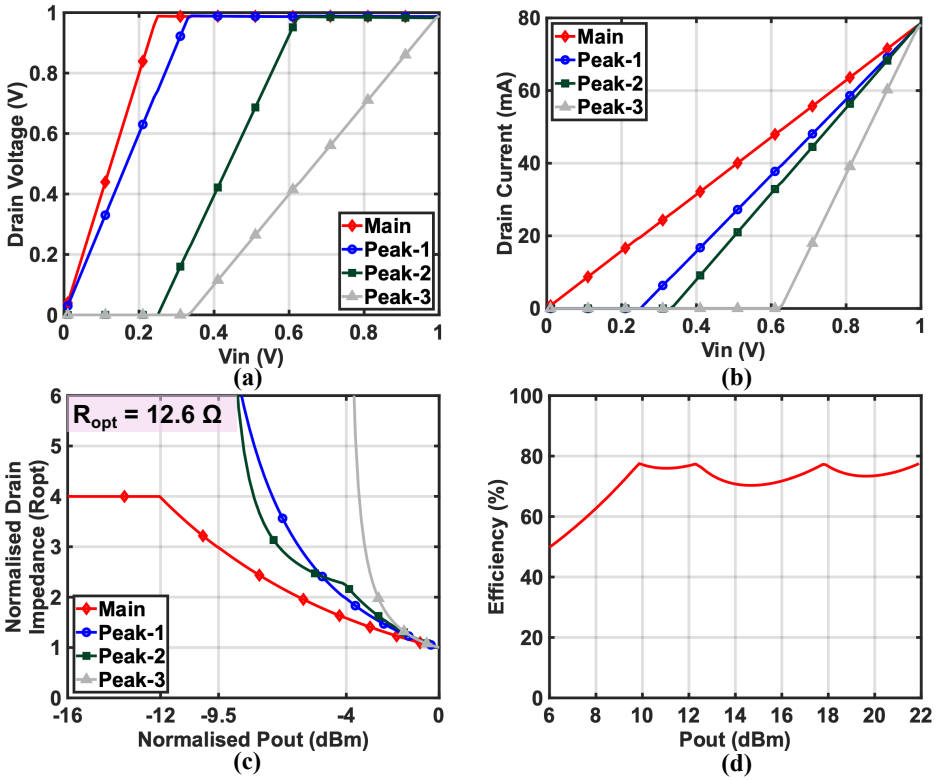


Fig. 3.6. (a) Drain voltage, (b) drain current, (c) drain impedance, and (d) DE of a symmetrical 4-way Doherty network.

Now, on solving the five equations (3.28), (3.31), (3.35), (3.36), and (3.37), we find that Z_{2X}, Z_{3X}, and Z_{5X} have a dependent relation, giving the designer one degree of freedom in choosing the Z_0 of either $Z_{2X}/Z_{3X}/Z_{5X}$. The generalized Z_0 of the TLs can be calculated using $Ropt_{\max}$, V_{DD}, R_L, K_1, K_2, and K_3 (Eq. (3.38)).

$$
\begin{aligned}
Z_{15} &= \frac{\sqrt{R_L \cdot Ropt_{\max}}}{K_3} \\
Z_{2X} &= \frac{\sqrt{R_L \cdot Ropt_{\max}} \cdot Z_{5x}}{K_2 \cdot R_L} \\
Z_{3X} &= \frac{\sqrt{R_L \cdot Ropt_{\max}} \cdot Z_{5x}}{(1-K_2) \cdot R_L} \\
Z_{34} &= \frac{Ropt_{\max}}{(1-K_2) \cdot (K_1 - K_3)}
\end{aligned}
\tag{3.38}
$$

The equations for a symmetrical 4-way Doherty with their associated back-off points can be seen in Table 3.1. Fig. 3.6(a)/(b)/(c) illustrate the voltage, current, and impedance

characteristics of the main and peak PAs in a symmetrical 4-way Doherty PA. The efficiency performance of the symmetrical 4-way Doherty PA is depicted in Fig. 3.6(d).

3.2.3. 5-WAY DOHERTY PA

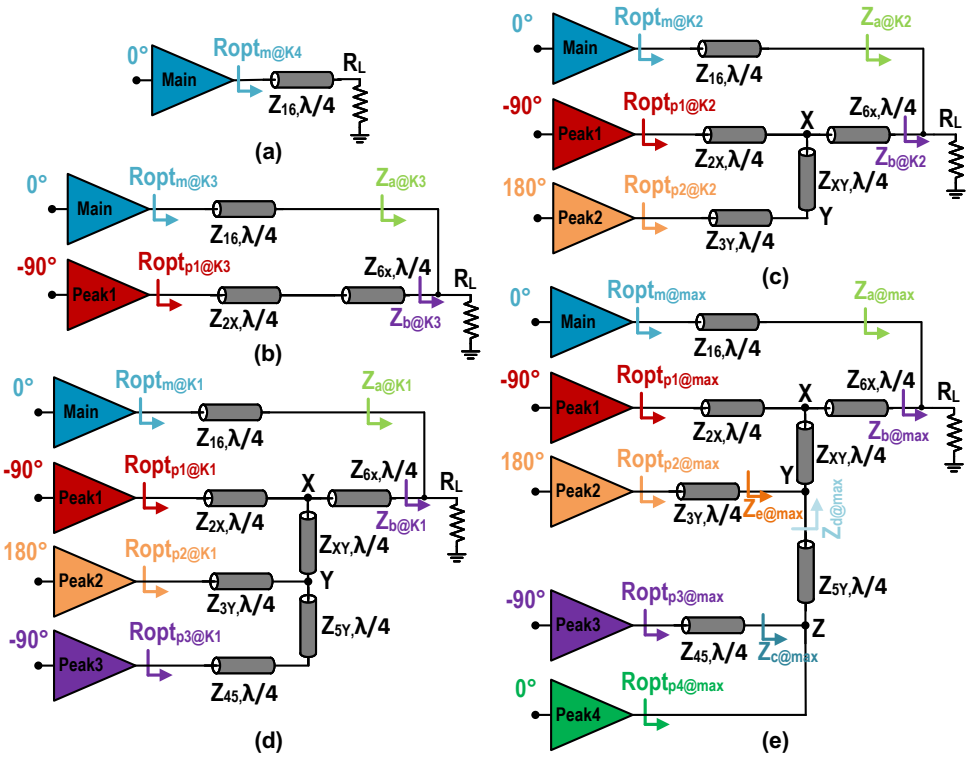


Fig. 3.7. 5-way Doherty network at (a) back-off K_4, (b) back-off K_3, (c) back-off K_2, (d) back-off K_1, and (e) peak power

Fig. 3.7(e) exhibits the 5-way Doherty network using quarter-wavelength TLs. The Z_0 of TLs (Z_{16}, Z_{2X}, Z_{6X}, Z_{XY}, Z_{3Y}, Z_{5Y}, and Z_{45}) can be calculated by analyzing the circuit at the back-off conditions (K_1, K_2, K_3, and K_4) and peak power. At 4^{th} back-off (K_4), the following conditions can be obtained:

$$\begin{aligned} V_{\mathrm{m@K_4}} &= V_{\max} = V_{\mathrm{DD}} \\ I_{\mathrm{p1@K_4}} &= I_{\mathrm{p2@K_4}} = I_{\mathrm{p3@K_4}} = I_{\mathrm{p4@K_4}} = 0 \\ I_{\mathrm{m@K_4}} &= I_{\mathrm{m@F}} \cdot K_4 \end{aligned} \tag{3.39}$$

At 3^{rd} back-off (K_3), the following conditions can be obtained:

$$\begin{aligned} V_{\mathrm{m@K_3}} &= V_{\mathrm{p1@K_3}} = V_{\max} = V_{\mathrm{DD}} \\ I_{\mathrm{p2@K_3}} &= I_{\mathrm{p3@K_3}} = I_{\mathrm{p4@K_3}} = 0 \\ I_{\mathrm{m@K_3}} &= I_{\mathrm{m@F}} \cdot K_3 \\ I_{\mathrm{p1@K_3}} &= I_{\mathrm{p1@F}} \cdot \frac{K_3 - K_4}{1 - K_4} \end{aligned} \tag{3.40}$$

At 2^{nd} back-off (K_2), the following conditions can be obtained:

$$\begin{aligned} V_{\mathrm{m@K_2}} &= V_{\mathrm{p1@K_2}} = V_{\mathrm{p2@K_2}} = V_{\max} = V_{\mathrm{DD}} \\ I_{\mathrm{p3@K_2}} &= I_{\mathrm{p4@K_2}} = 0 \\ I_{\mathrm{m@K_2}} &= I_{\mathrm{m@F}} \cdot K_2 \\ I_{\mathrm{p1@K_2}} &= I_{\mathrm{p1@F}} \cdot \frac{K_2 - K_4}{1 - K_4} \\ I_{\mathrm{p2@K_2}} &= I_{\mathrm{p2@F}} \cdot \frac{K_2 - K_3}{1 - K_3} \end{aligned} \tag{3.41}$$

At 1^{st} back-off (K_1), the following conditions can be obtained:

$$\begin{aligned} V_{\mathrm{m@K_1}} = V_{\mathrm{p1@K_1}} = V_{\mathrm{p2@K_1}} = V_{\mathrm{p3@K_1}} &= V_{\max} = V_{\mathrm{DD}} \\ I_{\mathrm{p4@K_1}} &= 0 \\ I_{\mathrm{m@K_1}} &= I_{\mathrm{m@F}} \cdot K_1 \\ I_{\mathrm{p1@K_1}} &= I_{\mathrm{p1@F}} \cdot \frac{K_1 - K_4}{1 - K_4} \\ I_{\mathrm{p2@K_1}} &= I_{\mathrm{p2@F}} \cdot \frac{K_1 - K_3}{1 - K_3} \\ I_{\mathrm{p3@K_1}} &= I_{\mathrm{p3@F}} \cdot \frac{K_1 - K_2}{1 - K_2} \end{aligned} \tag{3.42}$$

At peak power, the following conditions can be obtained:

$$V_{\mathrm{m@F}} = V_{\mathrm{p1@F}} = V_{\mathrm{p2@F}} = V_{\mathrm{p3@F}} = V_{\mathrm{p4@F}} V_{\max} = V_{\mathrm{DD}} \tag{3.43}$$

The back-off point can be defined as

$$\begin{aligned} K_4^2 &= \frac{P_{\mathrm{m@K_3}}}{P_{\mathrm{total@max}}} \\ K_3^2 &= \frac{P_{\mathrm{m@K_3}} + P_{\mathrm{p1@K_3}}}{P_{\mathrm{total@max}}} \\ K_2^2 &= \frac{P_{\mathrm{m@K_2}} + P_{\mathrm{p1@K_2}} + P_{\mathrm{p2@K_2}}}{P_{\mathrm{total@max}}} \\ K_1^2 &= \frac{P_{\mathrm{m@K_1}} + P_{\mathrm{p1@K_1}} + P_{\mathrm{p2@K_1}} + P_{\mathrm{p3@K_1}}}{P_{\mathrm{total@max}}} \end{aligned} \tag{3.44}$$

where, $P_{\mathrm{total@max}} = P_{\mathrm{m@max}} + P_{\mathrm{p1@max}} + P_{\mathrm{p2@max}} + P_{\mathrm{p3@max}} + P_{\mathrm{p4@max}}$

Using (3.39), (3.40), (3.41), (3.42), (3.43), and (3.44), we can calculate the ratios of maximum current carried by the main, peak-1, peak-2, peak-3, and peak-4 PAs by analyzing the circuits' KVL and KCL at its back-off points (K_1, K_2, K_3, and K_4) and the full power.

$$\begin{aligned} &I_{\text{m@max}} : I_{\text{p1@max}} : I_{\text{p2@max}} : I_{\text{p3@max}} : I_{\text{p4@max}} = \\ &[K_4 : K_3 \cdot (1-K_4) : (1-K_3) \cdot (K_2 - K_4) : \\ &(K_1 - K_3) \cdot (1-K_2) : (1-K_3) \cdot (1 + K_4 - 2K_2)] \cdot I_{\text{max}} \end{aligned} \tag{3.45}$$

At peak power, the optimum impedance seen by main, peak-1, peak-2, peak-3, and peak-4 PAs are given by (3.46), (3.47), (3.48), (3.49), and (3.50)

$$Ropt_{\text{m@max}} = \frac{Ropt_{\text{max}}}{K_4} \tag{3.46}$$

$$Ropt_{\text{p1@max}} = \frac{Ropt_{\text{max}}}{K_3 \cdot (1-K_4)} \tag{3.47}$$

$$Ropt_{\text{p2@max}} = \frac{Ropt_{\text{max}}}{(1-K_3) \cdot (K_2 - K_4)} \tag{3.48}$$

$$Ropt_{\text{p3@max}} = \frac{Ropt_{\text{max}}}{(K_1 - K_3) \cdot (1-K_2)} \tag{3.49}$$

$$Ropt_{\text{p4@max}} = \frac{Ropt_{\text{max}}}{(1-K_3) \cdot (1 + K_4 - 2 \cdot K_2)} \tag{3.50}$$

At back-off K_4, the impedance seen by the main PA can be calculated by using (3.46) and (3.39).

$$Ropt_{\text{m@K}_4} = \frac{V_{\text{m@K}_4}}{I_{\text{m@K}_4}} = \frac{V_{\text{DD}}}{I_{\text{m@max}} \cdot K_4} = \frac{Ropt_{max}}{K_4^2} \tag{3.51}$$

From the schematic in Fig. 3.7(a), we can get the following equation.

$$Z_{16} = \sqrt{R_{\text{L}} * Ropt_{\text{m@K}_4}} \tag{3.52}$$

At back-off K_3, the impedance seen by the main PA can be calculated by using (3.46), and (3.40).

$$Ropt_{\text{m@K}_3} = \frac{V_{\text{m@K}_3}}{I_{\text{m@K}_3}} = \frac{V_{\text{DD}}}{I_{\text{m@max}} \cdot K_3} = \frac{Ropt_{max}}{K_3 \cdot K_4} \tag{3.53}$$

The impedance seen by the peak-1 PA at back-off K_3 can be calculated by using (3.47) and (3.40).

$$Ropt_{\text{p1@K}_3} = \frac{V_{\text{p1@K}_3}}{I_{\text{p1@K}_3}} = \frac{V_{\text{DD}}}{I_{\text{p1@max}}} \cdot \frac{K_3 - K_4}{1-K_4} = \frac{Ropt_{max}}{K_3 \cdot (K_3 - K_4)} \tag{3.54}$$

From the schematic in Fig. 3.7(b), we can get the following equation.

$$\frac{1}{Z_{\text{a@K}_3}} + \frac{1}{Z_{\text{b@K}_3}} = \frac{1}{R_{\text{L}}} \tag{3.55}$$

The impedance seen by the main PA at back-off K_2 can be calculated by using (3.46) and (3.41).

$$Ropt_{\mathrm{m@K_2}} = \frac{V_{\mathrm{m@K_2}}}{I_{\mathrm{m@K_2}}} = \frac{V_{\mathrm{DD}}}{I_{\mathrm{m@max}} \cdot K_2} = \frac{Ropt_{max}}{K_2 \cdot K_4} \tag{3.56}$$

The impedance seen by the peak-1 PA at back-off K_2 can be calculated by using (3.47) and (3.41).

$$Ropt_{\mathrm{p1@K_2}} = \frac{V_{\mathrm{p1@K_2}}}{I_{\mathrm{p1@K_2}}} = \frac{V_{\mathrm{DD}}}{I_{\mathrm{p1@max}}} \cdot \frac{1-K_4}{K_2-K_4} = \frac{Ropt_{max}}{K_3 \cdot (K_2-K_4)} \tag{3.57}$$

The impedance seen by the peak-2 PA at back-off K_2 can be calculated by using (3.48) and (3.41).

$$\begin{aligned} Ropt_{\mathrm{p2@K_2}} = \frac{V_{\mathrm{p2@K_2}}}{I_{\mathrm{p2@K_2}}} &= \frac{V_{\mathrm{DD}}}{I_{\mathrm{p2@max}}} \cdot \frac{1-K_3}{K_2-K_3} \\ &= \frac{Ropt_{max}}{(K_2-K_3) \cdot (K_2-K_4)} \end{aligned} \tag{3.58}$$

From the schematic in Fig. 3.7(c), we can get the following equation

$$\frac{1}{Z_{\mathrm{a@K_2}}} + \frac{1}{Z_{\mathrm{b@K_2}}} = \frac{1}{R_{\mathrm{L}}} \tag{3.59}$$

The impedance seen by the main PA at back-off K_1 can be calculated by using (3.46) and (3.42).

$$Ropt_{\mathrm{m@K1}} = \frac{V_{\mathrm{m@K_1}}}{I_{\mathrm{m@K_1}}} = \frac{V_{\mathrm{DD}}}{I_{\mathrm{m@max}} \cdot K_1} = \frac{Ropt_{max}}{K_1 \cdot K_4} \tag{3.60}$$

The impedance seen by the peak-1 PA at back-off K_1 can be calculated by using Eqs. (3.42) and (3.47).

$$Ropt_{\mathrm{p1@K_1}} = \frac{V_{\mathrm{p1@K_1}}}{I_{\mathrm{p1@K_1}}} = \frac{V_{\mathrm{DD}}}{I_{\mathrm{p1@max}}} \cdot \frac{1-K_4}{K_1-K_4} = \frac{Ropt_{max}}{K_3 \cdot (K_1-K_4)} \tag{3.61}$$

The impedance seen by the peak-2 PA at back-off K_1 can be calculated by using 3.48) and (3.42).

$$Ropt_{\mathrm{p2@K_1}} = \frac{V_{\mathrm{p2@K_1}}}{I_{\mathrm{p2@K_1}}} = \frac{V_{\mathrm{DD}}}{I_{\mathrm{p2@max}}} \cdot \frac{1-K_3}{K_1-K_3} = \frac{Ropt_{max}}{(K_2-K_4) \cdot (K_1-K_3)} \tag{3.62}$$

The impedance seen by the peak-3 PA at back-off K_1 can be calculated by using 3.49) and (3.42).

$$Ropt_{\mathrm{p3@K_1}} = \frac{V_{\mathrm{p3@K_1}}}{I_{\mathrm{p3@K_1}}} = \frac{V_{\mathrm{DD}}}{I_{\mathrm{p3@max}}} \cdot \frac{1-K_2}{K_1-K_2} = \frac{Ropt_{max}}{(K_1-K_2) \cdot (K_1-K_3)} \tag{3.63}$$

From the schematic in Fig. 3.7(d), we can get the following equation

$$\frac{1}{Z_{\mathrm{a@K_1}}} + \frac{1}{Z_{\mathrm{b@K_1}}} = \frac{1}{R_{\mathrm{L}}} \tag{3.64}$$

The impedance seen by each PA (main, peak-1, peak-2, peak-3 and peak-4) is given by (3.46), (3.47), (3.48), (3.49), and (3.50). From the schematic in Fig. 3.7(e), we can get the following equation:

$$\frac{1}{Z_{\mathrm{a@max}}} + \frac{1}{Z_{\mathrm{b@max}}} = \frac{1}{R_{\mathrm{L}}} \tag{3.65}$$

Since the current delivered by peak-3 and peak-4 at the peak power is $(1-K_2)\cdot(K_1-K_3)\cdot I_{\max}$ and $(1-K_3)\cdot(1+K_4-2\cdot K_2)\cdot I_{\max}$ respectively (3.45), we can calculate the ratio between the impedances $Z_{\text{c@max}}$ and $Ropt_{\text{p4@max}}$ by applying KCL at node Z (refer Fig. 3.7(e)).

$$\begin{aligned} Z_{\text{c@max}} &= Ropt_{\text{p4@max}} \cdot \frac{(1-K_3)\cdot(1+K_4-2\cdot K_2)}{(1-K_2)\cdot(K_1-K_3)} \\ Z_{45} &= \sqrt{Z_{\text{c@max}} \cdot Ropt_{\text{p3@max}}} = \frac{Ropt_{\max}}{(1-K_2)\cdot(K_1-K_3)} \end{aligned} \tag{3.66}$$

We apply KCL at node Y to obtain the 7$^{\text{th}}$ equation, which allows us to find the Z_0 of all the TLs.

$$Z_{\text{e@max}} = \frac{Z_{\text{d@max}}\cdot((K_1-K_3)\cdot(1-K_2)+(1-K_3)\cdot(1+K_4-2\cdot K_2))}{(1-K_3)\cdot(K_2-K_4)} \tag{3.67}$$

Now, on solving the seven equations (3.52), (3.55), (3.59), (3.64), (3.65), (3.66), and (3.67),

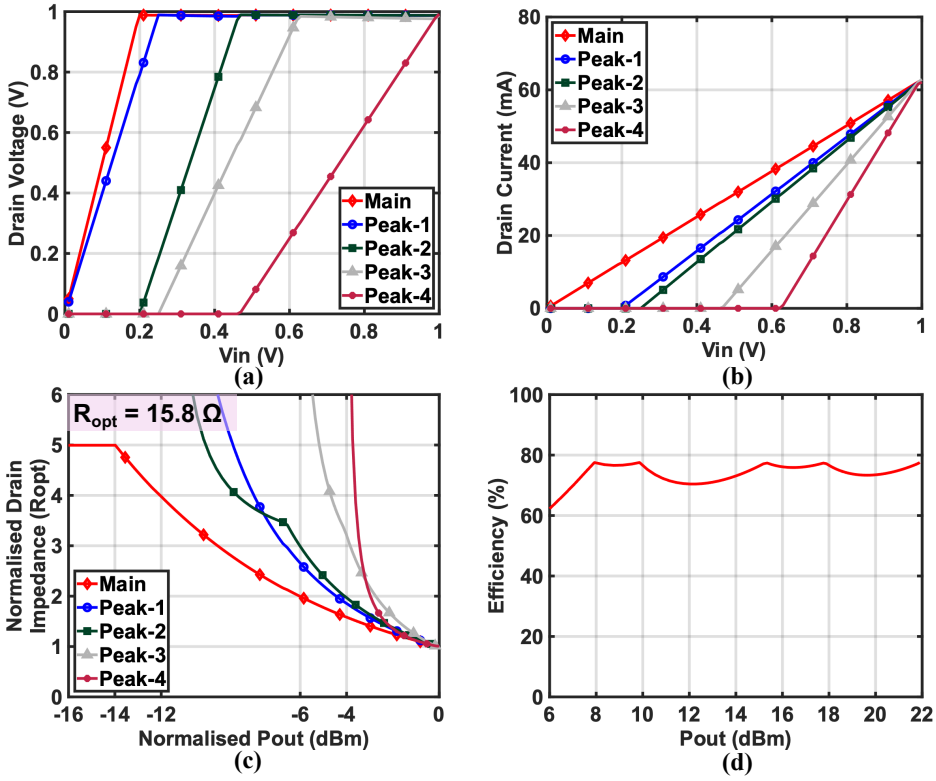


Fig. 3.8. (a) Drain voltage, (b) drain current, (c) drain impedance, and (d) DE of a symmetrical 5-way Doherty network.

we find that Z_{2X}, Z_{3Y}, Z_{5Y}, Z_{XY}, and Z_{6X} have a dependent relation, providing the designer two degrees of freedom in choosing the Z_0 of two TLs among Z_{2X}, Z_{3Y}, Z_{5Y}, Z_{XY},

and Z_{6X}. The generalized Z_0 of the TLs can be calculated using $Ropt_{max}$, V_{DD}, R_L, K_1, K_2, K_3, and K_4 (3.68).

$$
\begin{aligned}
Z_{16} &= \frac{\sqrt{R_L \cdot Ropt_{max}}}{K4} \\
Z_{2X} &= \frac{\sqrt{R_L \cdot Ropt_{max}} \cdot Z_{6x}}{K3 \cdot R_L} \\
Z_{3Y} &= \frac{\sqrt{K3 \cdot R_L \cdot Ropt_{max} \cdot (K2-K3)} \cdot (1-K3) \cdot Z_{XY}}{K3 \cdot Z_{6X} \cdot (K3 \cdot K2 - K3 \cdot K4 - K2 + K4)} \\
Z_{5Y} &= \frac{\sqrt{K3 \cdot R_L \cdot Ropt_{max} \cdot (K2-K3)} \cdot (1-K3) \cdot Z_{XY}}{K3 \cdot Z_{6X} \cdot ((2+K4-3 \cdot K2) \cdot K3 + (K1+2) \cdot K2 - K1 - K4 - 1)} \\
Z_{45} &= \frac{Ropt_{max}}{(1-K2) \cdot (K1-K3)}
\end{aligned}
\tag{3.68}
$$

The equations for symmetrical 5-way Doherty can be seen in Table 3.1. Fig. 3.8(a)/(b)/(c) depict the voltage, current, and impedance profiles of the main and peak PAs in a symmetrical 5-way Doherty PA, respectively. The efficiency of the symmetrical 5-way Doherty PA is presented in Fig. 3.8(d).

Table 3.1
COMPARISON OF 3-/4-/5-WAY DOHERTY COMBINERS

Parameters	3-way Doherty	4-way Doherty	5-way Doherty
Transmission lines	3	5	7
Lumped components	Ind-4 & Cap-3	Ind-6 & Cap-5	Ind-8 & Cap-7
Degrees of freedom	0	1	2
P_{sat} per PA* (dBm)	$Pout_{max} - 10 \cdot \log(3)$ = 17.2	$Pout_{max} - 10 \cdot \log(4)$ = 16	$Pout_{max} - 10 \cdot \log(5)$ 15
Back-off points*	K_1=0.5, K_2=0.333	K_1=0.625, K_2=0.333, K_3=0.25	K_1=0.625, K_2=0.467, K_3=0.25, K_4=0.2
Ropt for each PA @P_{sat}* (Ω)	$\frac{Ropt_{max}}{K2}$ = 9.4	$\frac{Ropt_{max}}{K3}$ = 12.6	$\frac{Ropt_{max}}{K4}$ = 15.8
Z_0 of TLs* (Ω)	$Z_{14} = 3 \cdot \sqrt{R_L \cdot Ropt_{max}}$ $Z_{23} = 3 \cdot Ropt_{max}$ $Z_{34} = \frac{3 \cdot \sqrt{R_L \cdot Ropt_{max}}}{2}$	$Z_{15} = 4 \cdot \sqrt{R_L \cdot Ropt_{max}}$ $Z_{2X} = \frac{3 \cdot \sqrt{R_L \cdot Ropt_{max}} \cdot Z_{5x}}{R_L}$ $Z_{3X} = \frac{3 \cdot \sqrt{R_L \cdot Ropt_{max}} \cdot Z_{5x}}{2 \cdot R_L}$ $Z_{34} = 4 \cdot Ropt_{max}$ Z_{5X} - user-defined	$Z_{16} = 5 \cdot \sqrt{R_L \cdot Ropt_{max}}$ $Z_{2X} = \frac{4 \cdot \sqrt{R_L \cdot Ropt_{max}} \cdot Z_{6X}}{R_L}$ $Z_{3Y} = \frac{3.5 \cdot \sqrt{R_L \cdot Ropt_{max}} \cdot Z_{XY}}{Z_{6X}}$ $Z_{5Y} = \frac{3.5 \cdot \sqrt{R_L \cdot Ropt_{max}} \cdot Z_{XY}}{2 \cdot Z_{6X}}$ $Z_{45} = 5 \cdot Ropt_{max}$ Z_{6X} & Z_{XY} - user-defined

* To generate P_{sat} = 22 dBm with V_{DD} = 1 V in the symmetrical Doherty for a load (R_L) of 25 Ω

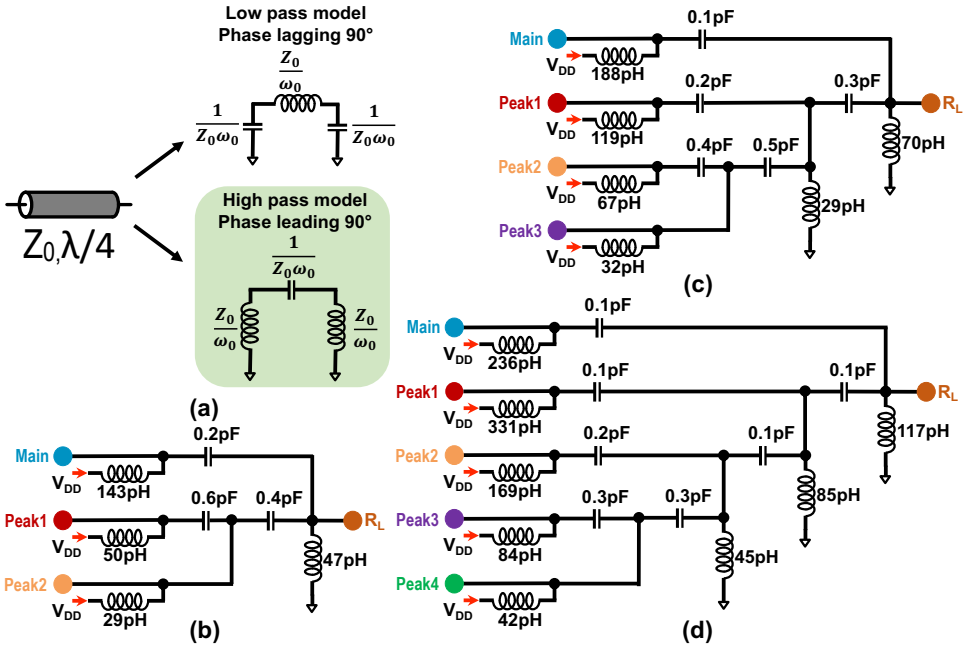


Fig. 3.9. (a) HP and low-pass (LP) model of TL, (b) 3-way Doherty network, (c) 4-way Doherty network, and (d) 5-way Doherty network using lumped components.

3.3. ANALYSIS OF 3-/4-/5-WAY DOHERTY COMBINERS

In this section, we design the symmetrical 3-/4-/5-way Doherty PAs that can deliver a P_{sat} of 22 dBm to a load (R_L) of 25 Ω (for a single-ended Doherty PA) with a V_{DD} of 1 V using the equations in Table 3.1. The TLs can be replaced by an HP lumped component (Fig. 3.9(a)) at the center frequency of 30 GHz (Fig. 3.9(b)/(c)/(d)). Since the HP lumped component model allows a dc feed for each PA, a differential implementation is straightforward. As exhibited, moving from N to N+1 Doherty, the number of TL elements increases by 2. Similarly, in the case of lumped components, the number of inductors and capacitors increases by 2.

3.3.1. COMPARISON OF P_{OUT} AND DE

The branch PAs are modeled as an ideal current source in the Advanced Design System (ADS) to analyze the P_{out} and DE of a 3-/4-/5-way Doherty configuration at peak and back-off power levels at the mm-wave band centered around 30 GHz. According to Fig. 3.10 (a), the designed 3-/4-/5-way Doherty network using lossless lumped components yields 3/4/5 DE peaks of 78.5 % (ideal class B) while delivering P_{sat}=22 dBm. The peak DE and bandwidth can be improved further by utilizing class J [25] or (continuous) class F PAs [99].

Subsequently, the 3-/4-/5-way Doherty with ideal branch PAs are modeled with lossy elements assuming quality factors (QFs) of 15/25 for the inductors/capacitors, respec-

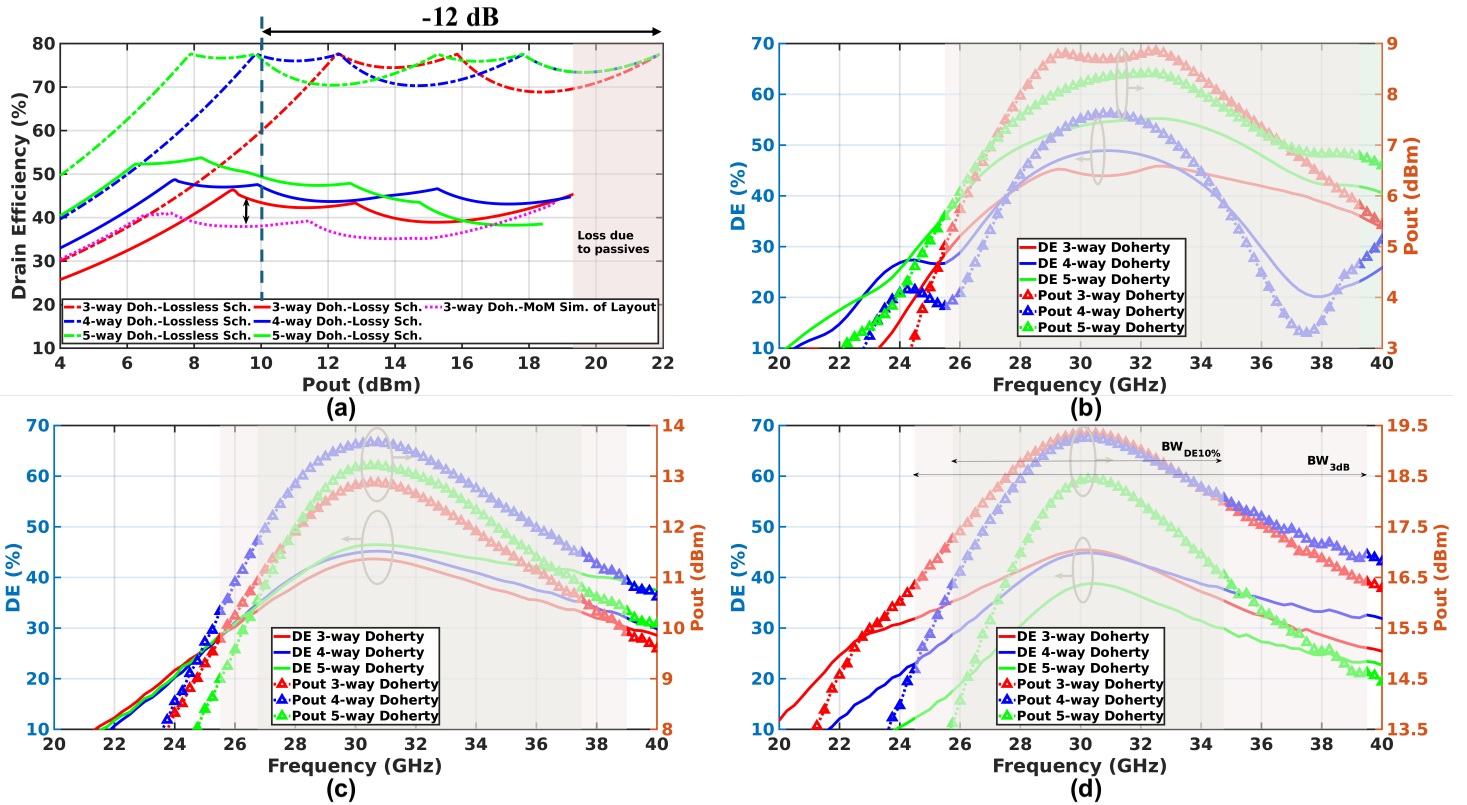


Fig. 3.10. (a) DE vs. P_{out} for 3-/4-/5-way Doherty at 30 GHz using lossless and lossy lumped components, (b) DE vs. P_{out} vs. frequency for 3-/4-/5-way Doherty at PBO 12 dB, (c) PBO 6 dB, and (d) full power using inductors/capacitors of quality factors (QFs) of 15/25, respectively.

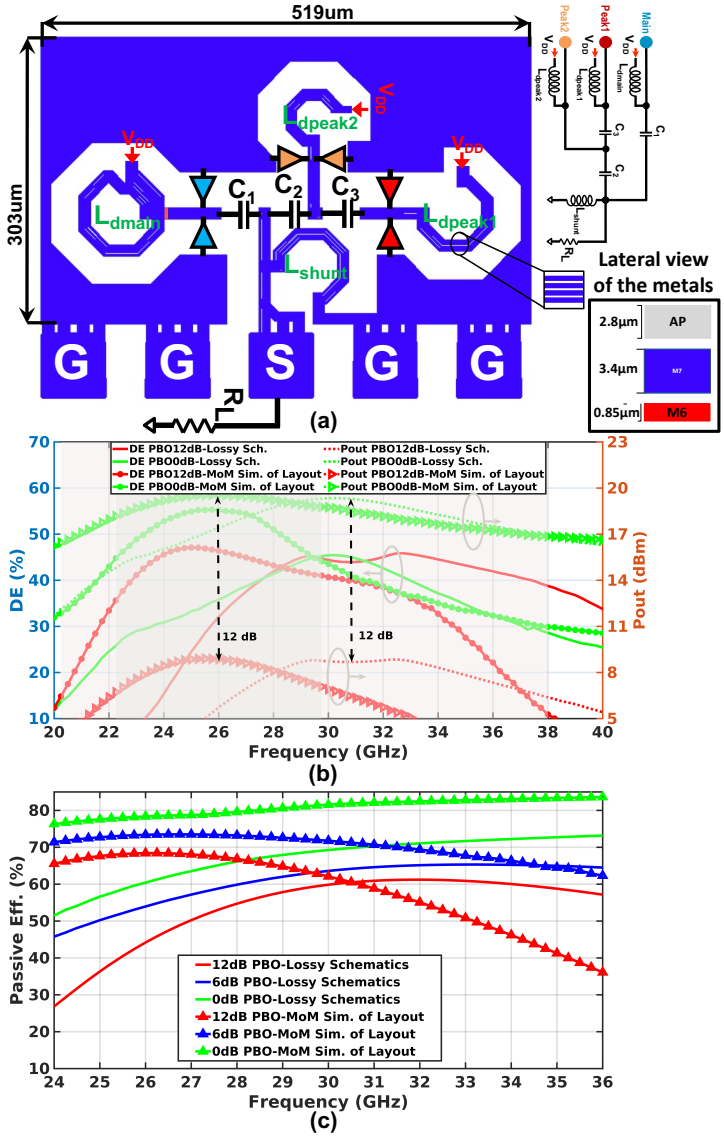


Fig. 3.11. (a) Layout of 3-way Doherty (b) DE vs. frequency for 3-way Doherty at 12 dB PBO and maximum power, and (c) passive efficiency (PE) vs. frequency for 3-way Doherty at 12 dB PBO, 6 dB PBO and maximum power using inductors/capacitors of quality factors (QFs) of 15/25, respectively, and momentum simulation of the layout.

tively, and simulated to capture their overall P_{out} and DE at the mm-wave band centered around 30 GHz. According to Fig. 3.10(a), the 5-way Doherty achieves a lower peak P_{out} and associated DE since the number of lumped components in the power combiner is higher, entailing higher loss.

At its 12 dB back-off point at the input (Fig. 3.10(b)), the 3-way Doherty with lossy power combiner has the highest P_{out} since only the main PA is active. Nevertheless, the 5-way Doherty has the best DE performance because it already benefits from load modulation, since K_4=0.2. The 3-/4-way Doherty PAs have similar performance at 30 GHz because, in the 3-way Doherty, the load modulation has not yet started. In the 4-way Doherty, it is on the threshold of starting load modulation (peak-1 PA turns on at K_3=0.25). On the other hand, the bandwidth at which DE drops by 10 % ($BW_{DE10\%}$) and 3 dB power bandwidth (BW_{3dB}) are the highest for the 5-way Doherty, followed by the 3-/4-way Doherty at 12 dB back-off ($BW_{DE10\%}/BW_{3dB}$ of 3-way Doherty is shaded in green/red in Fig. 3.10(b)/(c)/(d)).

At 6 dB input PBO (Fig. 3.10(c)), the DE performance is similar for all three architectures. However, the 4-way Doherty shows the highest P_{out} because its peak-3 PA is still off, keeping the current lower. In the 3-way Doherty, all three PAs are on, which increases the current and losses, resulting in lower P_{out}. In the 5-way Doherty, fewer PAs are active, so the current is lower, but the larger number of lumped components adds more loss, also reducing P_{out}. The $BW_{DE10\%}/BW_{3dB}$ at 6 dB back-off are comparable for all three cases. At full power (Fig. 3.10(d)), both DE and P_{out} are lowest for the 5-way Doherty due to the higher loss from more lumped components. Meanwhile, the 3-/4-way Doherty show similar performance at full power. In general, for all Doherty versions, $BW_{DE10\%}$ is smaller at full power than at back-off, and it decreases as we go from 3-way to 5-way Doherty (Fig. 3.10(b)/(c)/(d)).

Consequently, the 3-way Doherty seems to be the best choice for implementing a PA in the mm-wave frequency bands. Moreover, it turns out that employing a 4-way Doherty or higher-order Doherty PA delivers a lower output power for the same total gate width, due to the increased insertion loss of its lumped-element power combiner, despite its lower impedance transformation. Furthermore, the performance of the 3-way Doherty is comparable to the 4-way Doherty at 12 dB back-off, but it has better performance at peak power. Since it only consists of three quarter-wavelength TLs, providing a minimal lumped-element high-pass equivalent TLs and thus a compact power combiner.

The proposed 3-way Doherty structure is laid out in 40 nm CMOS process (Fig. 3.11(a)) with a size of $519 \times 303\,\mu m^2$. In this regard, QF of the spiral/slab inductors is increased more than twofold using parallel slot lines of minimum width than utilizing one thick line of the required width, as shown in Fig. 3.11(a). Since the signal travels at the surface due to the skin effect, splitting the lines increases surface area, reducing resistance and increasing QF [100]. The ADS (Momentum) simulation results of the layout are depicted in Fig. 3.11(b)/(c), which indicates at most 10 % deviation in passive efficiency (PE) from the assumed lossy network. Also, the proposed layout reaches PE of 60 % at 12 dB PBO while operating at 30 GHz.

The center frequency has shifted to 26 GHz due to the addition of the ground plane, which affects the related inductance of the network. This arrangement can be tuned if necessary. Moreover, using an ideal PA, the proposed design achieves a peak RF P_{out}/DE of more than 20 dBm/55 %, respectively, and its $BW_{DE10\%}/BW_{3dB}$ is 8/15 GHz, shaded green/red, respectively (Fig. 3.11(b)).

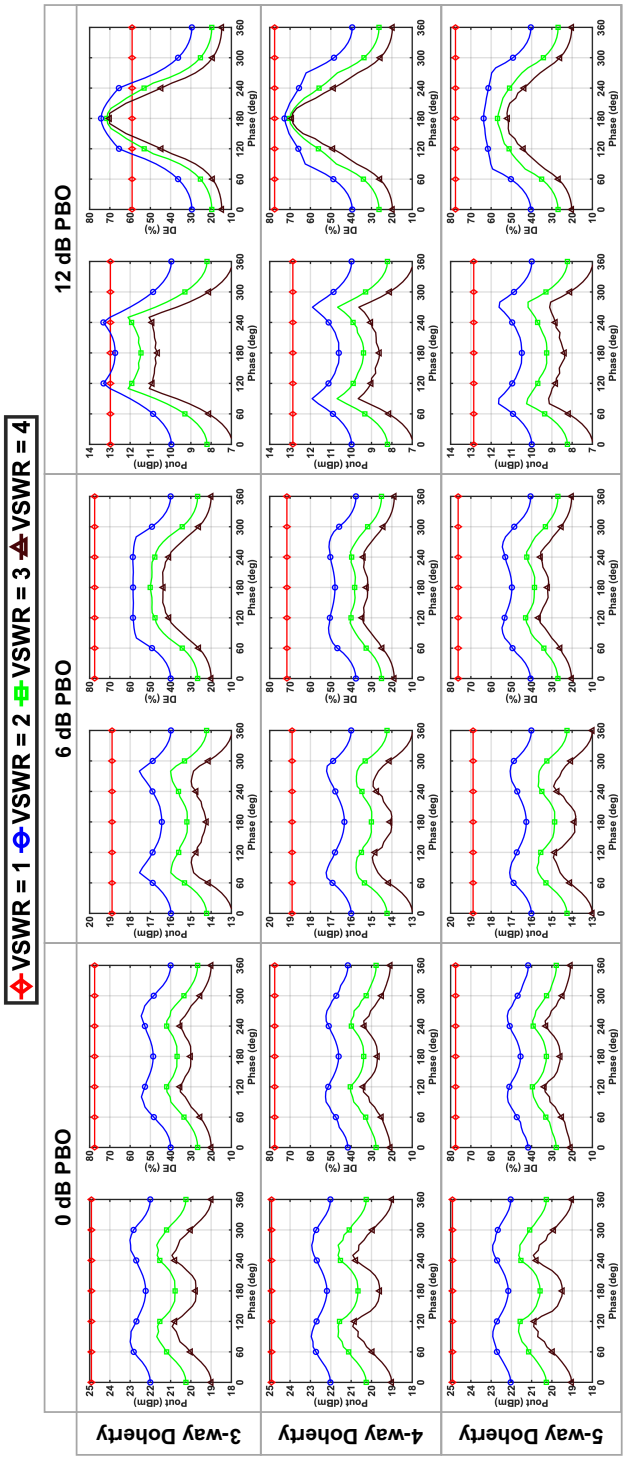


Fig. 3.12. Performance of 3-/4-/5-way Doherty with ideal components across VSWR.

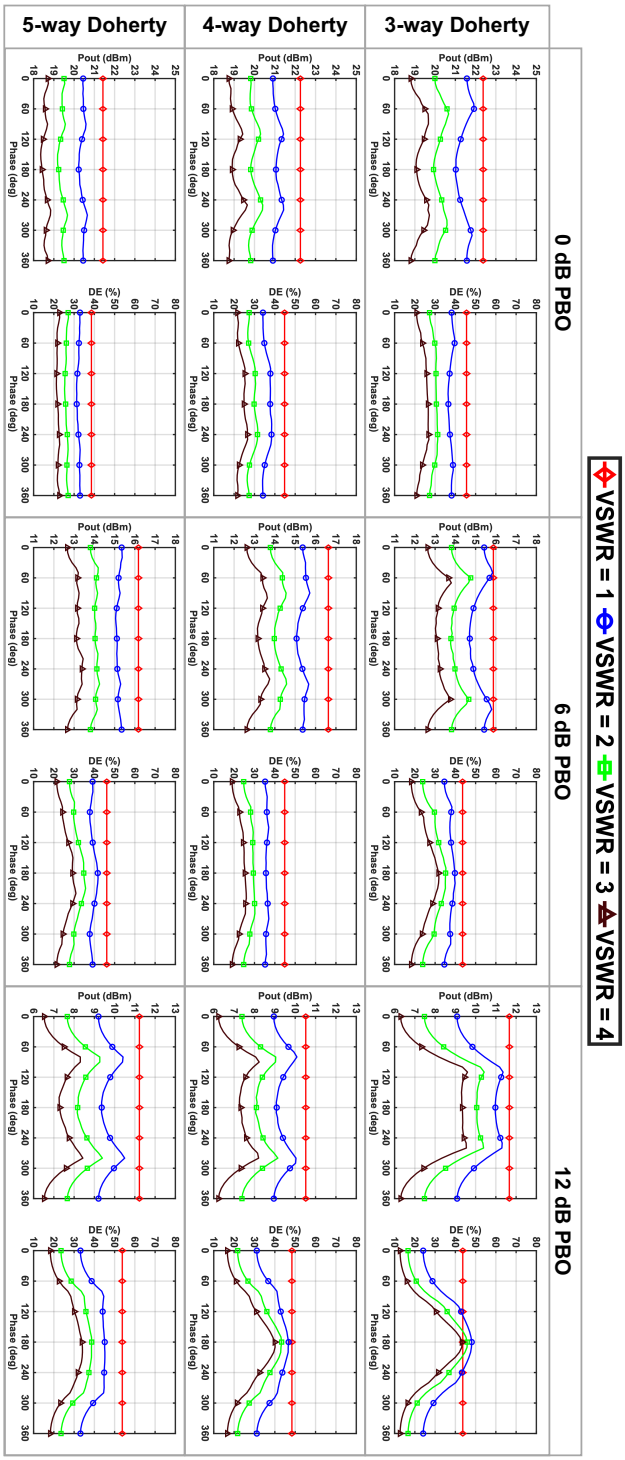


Fig. 3.13. Performance of 3-/4-/5-way Doherty with lossy components ($Q_C = 25$ and $Q_L = 15$) across VSWR.

3.3.2. PERFORMANCE UNDER VSWR

The 3-/4-/5-way Doherty PAs (Fig. 3.9(b)/(c)/(d)) are converted into push-pull structures using a balun and can generate an P_{out} of 25 dBm for a R_L of 50 Ω. These structures are tested with ideal current sources to evaluate their performance under varying VSWR conditions.

Fig. 3.12 illustrates the P_{out} and DE for the 3-/4-/5-way Doherty PAs with lossless components at 0/6/12 dB PBO across different VSWR values (1, 2, 3, and 4). It is evident that VSWR significantly affects the performance of the PAs, especially at PBO, as load modulation does not function as intended. At 0 dB PBO, P_{out} and DE degrade by at least 5 dB and 50 %, respectively, for the 3-way Doherty PA at a VSWR of 3. A similar degradation in performance is observed for the 4- and 5-way Doherty PAs at peak power.

At 6 dB PBO, the 4-way Doherty PA achieves lower efficiency at a VSWR of 1 because 0.5 is not a back-off point, preventing it from reaching 78.5 % efficiency (ideal class B peak efficiency). P_{out} and DE degradation for the 3-/4-/5-way Doherty PAs at 6 dB PBO are similar to the degradation observed at 0 dB PBO.

The symmetric 3-way Doherty PA does not achieve any additional efficiency improvements beyond 9.5 dB PBO. At 12 dB PBO, only the main PA remains active, while the auxiliary PAs are completely turned off. So, at a VSWR of $2\angle 180°$, the impedance is initially low, but the impedance inverter TL translates it to a higher impedance, causing the PA to saturate earlier and achieve higher efficiency. This explains why efficiency at a VSWR of $2\angle 180°$ is higher than at a VSWR of 1.

Fig. 3.13 presents P_{out} and DE for the 3-/4-/5-way Doherty PAs with lossy components (Q_C = 25 and Q_L = 15) at 0/6/12 dB across different VSWR values (1, 2, 3, and 4). At 0 dB PBO, efficiency degradation with respect to VSWR is lower due to the lossy network, which prevents the PA's drain from experiencing significant impedance changes caused by VSWR. As a result, higher-order Doherty PAs exhibit greater passive loss but are less affected by VSWR. A similar trend is observed at 6 dB and 12 dB PBO for the 3-/4-/5-way Doherty PAs.

3.4. SUMMARY

This chapter elaborates on the systematic design procedure for 3-/4-/5-way Doherty PAs using TLs and their HP lumped element equivalent schematics. These power combiners are designed and compared using both lossless and lossy components with a QF of 15/25 for inductors/capacitors at 30 GHz, while their PAs are modeled as ideal current sources.

Based on these analyses, we conclude that, using a realistic QF for the inductors, the 3-way Doherty network is the best candidate for mm-wave frequency bands. This is because it requires only four inductors and three capacitors, resulting in lower complexity, a more compact layout, and performance comparable to that of the 4-way Doherty at 12 dB back-off.

In general, an N-way Doherty network is more sensitive to VSWR conditions compared to traditional single linear class A/B/AB PAs, as VSWR mismatch conditions affect the Doherty load modulation and, consequently, its back-off efficiency. When losses are introduced into the components, the output networks introduce higher losses, which in turn reduce the impact of VSWR.

The next chapter describes a technique to enhance the bandwidth of the 3-way Doherty network.

4

A Single-Supply Balun-First Three-Way Doherty PA

This chapter introduces a single-supply balun-first 3-way parallel Doherty PA tailored for mm-wave 5G applications. It incorporates a bandwidth enhancement technique that widens the operational frequency range, offers broadband PBO efficiency, while reducing the impedance mismatch between the differential PAs. Realized in 40 nm CMOS bulk technology with a core area of 0.77 mm^2, the prototype delivers a P_{sat}/gain surpassing 20 dBm/16 dB, and it demonstrates a DE exceeding 15 %/22 %/33 % at 9.5 dB/6 dB/0 dB PBO across a 24-to-30 GHz band. The proposed mm-wave PA achieves EVM/ACLR values of -24.3 dB/-30.1 dBc for a 1 GHz 64-QAM OFDM signal, operating at a P_{avg} of 9.4 dBm with a DE_{avg} of 15 %. For a 50 MHz 1024-QAM OFDM signal, it achieves a P_{avg}/DE_{avg} of 8.6 dBm/12 % with EVM/ACLR of -30 dB/-36.3 dBc.

This chapter is based on the paper published in the IEEE Trans. Microw. Theory Tech. [101, 102].

4.1. INTRODUCTION

This chapter introduces a compact, single-supply, mm-wave, three-stage, 3-way Doherty PA that employs a bandwidth enhancement technique for broader operational frequency bandwidth coverage. It details the architectural analysis, circuit-level design considerations, and comprehensive measurement results. The previous chapter highlighted that the average DE does not significantly improve for N-way Doherty configurations beyond the 3-way architecture. Therefore, the 3-way Doherty PA is a strong candidate for mm-wave frequencies. Moreover, its performance at a 12 dB PBO is comparable to 4-/5-way Doherty architectures, while offering a more compact combiner at reduced design complexity Fig. 3.1.

Recent implementations of 3-way [97, 98] and 4-way [96] mm-wave Doherty PA architectures are narrowband, especially at deep PBO levels. Additionally, they often require two supply voltages in cascode PA structures and complex power management systems in their front-end stages to achieve the desired gain and radiated power. Consequently, designing a compact mm-wave front-end with high average efficiency across a wide frequency range, using a single supply, while adhering to the strict element-to-element $\lambda/2$ lattice spacing requirement of phased arrays, remains a significant challenge.

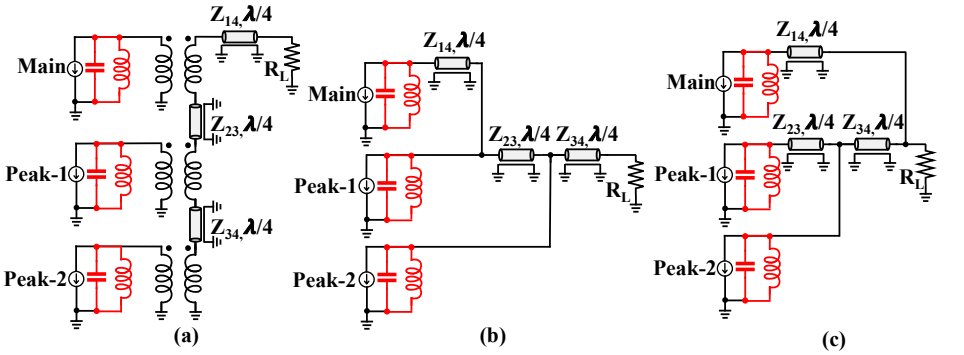
Section 4.2 explores the analysis of different 3-way Doherty topologies, focusing on their operational bandwidth. Section 4.3 details an enhanced bandwidth technique and explains the phase and magnitude variations of HP and low-pass (LP) models of TL for different Z_0. Following the design methodology outlined in Section 4.4, a compact power combiner comprising three identical balun transformers, an inductor, and three capacitors is synthesized. Section 4.5 provides insights into the circuit implementation of the proposed Doherty PA prototype, fabricated using 40 nm bulk CMOS technology. Experimental results are presented in Section 4.6, and Section 4.7 examines the impact of lossy C_{ds} on back-off efficiency. Section 4.8 compares the performance of the proposed PA with state-of-the-art PAs. Finally, the chapter concludes in Section 4.9.

4.2. 3-WAY DOHERTY VARIANTS

The 3-way Doherty architecture can be deployed in a series configuration or a parallel configuration. Various design iterations of the 3-way Doherty architecture are illustrated in Fig. 4.1. The design equation for the proposed 3-way Doherty structure is detailed in [87]. An inductor is employed to counteract the parasitic drain-source capacitance of the PA, as indicated by the red color in all three schematics. The key advantages of the proposed 3-way parallel Doherty combiner are as follows:

- Among the different configurations, the conventional idealized 3-way series Doherty configuration exhibits superior performance in terms of DE and P_{out} across the frequency spectrum (as shown in Fig. 4.2). However, this configuration necessitates three transformers for the main, peak-1, and peak-2 devices. In contrast, the parallel Doherty configuration only requires a balun for differential operation. Using three transformers in the series configuration leads to significant DE and P_{out} degradation compared to the parallel Doherty setup.

- A traditional 3-way parallel Doherty demands the current of the main device to



Transmission line (TLs)	Conventional 3-way series Doherty (a)	Conventional 3-way parallel Doherty (b)	Proposed 3-way parallel Doherty (c)
Z_{14}	$\frac{\sqrt{R_L * R_{opt\_max}}}{K2}$	$\frac{R_{opt\_max}}{K1 * K2}$	$\frac{\sqrt{R_L * R_{opt\_max}}}{K2}$
Z_{23}	$\frac{R_L * K2}{K1}$	$\frac{R_{opt\_max}}{K1}$	$\frac{\sqrt{R_L * R_{opt\_max}}}{1-K2}$
Z_{34}	$\frac{R_L * K2^2}{K1 * (1-K2)}$	$\sqrt{R_{opt} R_L}$	$\frac{R_{opt\_max}}{K1 * (1-K2)}$

(d)

Fig. 4.1. (a) Conventional 3-way series Doherty, (b) conventional 3-way parallel Doherty, (c) proposed 3-way parallel Doherty [101], and (d) equations for calculating Z_0 of each TL for each design.

increase linearly with the input RF voltage up to the first back-off point and then to maintain a constant level up to full power. Executing this feature is challenging in analog PAs and can lead to nonlinearity issues [103].

- During deep PBO, the proposed combiner operates with only the main PA active, establishing a direct signal path between the main PA output and the overall Doherty PA output. This results in minimal power loss. The off-state impedance of the peak-1 PA primarily influences the efficiency of the proposed combiner.

The symmetrical Doherty configuration offers the advantage of employing the same building block for the main, peak-1, and peak-2. Consequently, the proposed parallel Doherty architecture is designed symmetrically (with $K_1 = 0.5$ and $K_2 = 0.33$). However, Fig. 4.2 highlights that the proposed 3-way Doherty configuration still has limitations regarding its operational bandwidth.

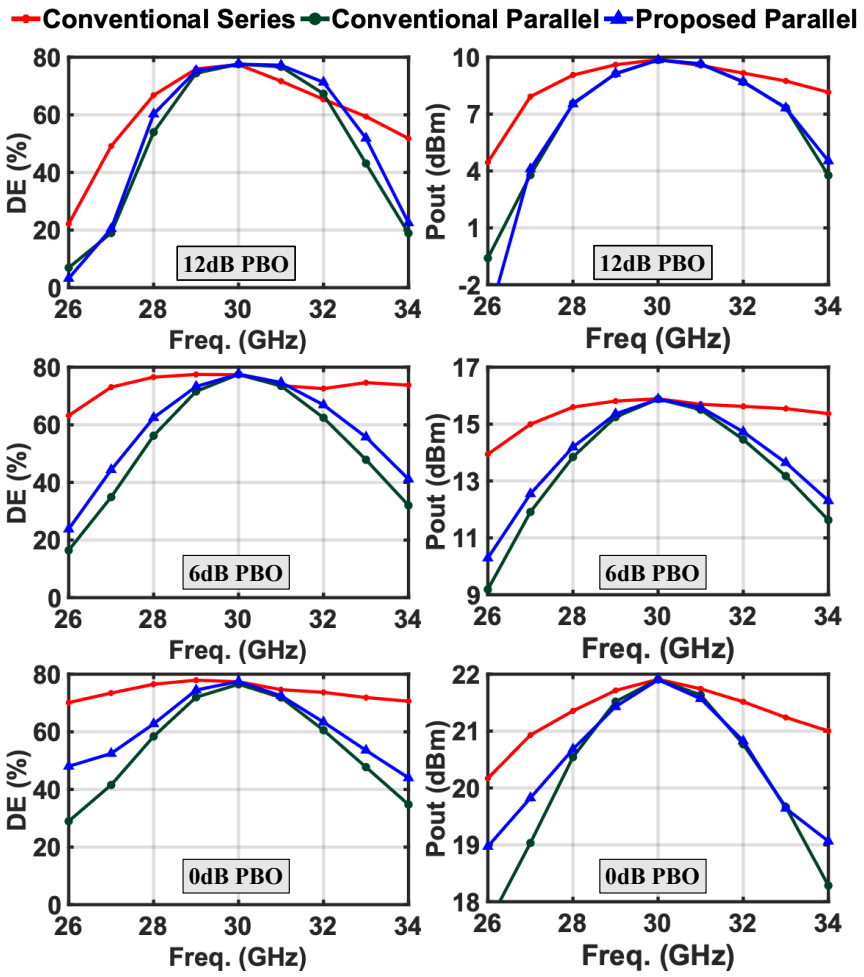


Fig. 4.2. DE and P_{out} across frequency at 12/6/0 dB PBO for K_1 = 0.5 and K_2 = 0.25.

4.3. BANDWIDTH ANALYSIS

Due to its impractical size for on-chip implementation at mm-wave frequencies, the TL can be substituted with either an HP configuration (depicted in Fig. 4.3(a)) or an LP counterpart (illustrated in Fig. 4.3(b)) using lumped-element models. The HP model is chosen because it incorporates shunt inductors acting as a dc feed and provides inherent transformation into a differential circuit. Upon replacing each of the TL components (Z_{14}, Z_{23}, and Z_{34}) with the HP model, the parallel elements are consolidated, resulting in the schematic depicted in Fig. 4.3(c). The values of the inductor and capacitor in the lumped element model are computed based on the Z_0 of the TL (refer to Fig. 4.3(a)/(b)). Z_{14}, Z_{23}, and Z_{34} correspond to Z_0 of each respective TL.

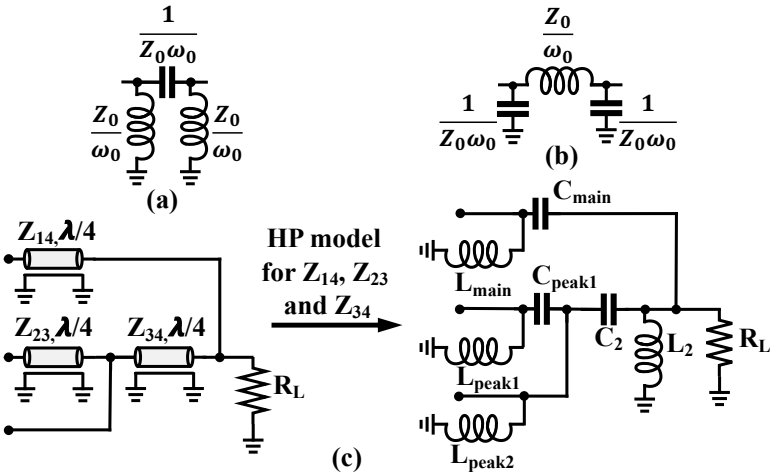


Fig. 4.3. (a) HP lumped element model, (b) LP lumped element model, and (c) proposed 3-way parallel Doherty using lumped elements.

4.3.1. BANDWIDTH ENHANCEMENT TECHNIQUE

Fig. 4.4 depicts a step-by-step design procedure for the proposed enhanced bandwidth (EBW) onto the suggested 3-way parallel Doherty network. This technique is applied to the main PA's path, which experiences the most prominent power losses. The process starts by substituting the Z_{14} TL with its LP lumped element equivalents. Subsequently, the capacitors and the inductor within the main path are divided, accompanied by a Norton transformation [104]. This transformation then leads to replacing the obtained transformer (turn ratio N_{EBW}) with the following adjustments: reducing the main V_{DD} by N_{EBW}, increasing the g_m of the power device by N_{EBW}, augmenting capacitors by N_{EBW}^2, and decreasing inductors and impedance seen at the drain node by N_{EBW}^2, as shown in (4.1). Finally, a more compact 3-way combiner configuration is achieved through the utilization of a star-to-delta transformation.

$$\begin{aligned} V'_{DD} &= \frac{V_{DD}}{N_{EBW}} \\ gm' &= gm * N_{EBW} \\ C' &= C * N_{EBW}^2 \\ L' &= \frac{L}{N_{EBW}^2} \\ R' &= \frac{R}{N_{EBW}^2} \end{aligned} \tag{4.1}$$

Fig. 4.5 displays three versions of the concept. In version #1, the HP model is applied to all the TLs alongside the lumped element equivalence illustrated in Fig. 4.3(c). Version #2 employs the LP model, replacing the Z_{14} TL. In version #3, the EBW technique is em-

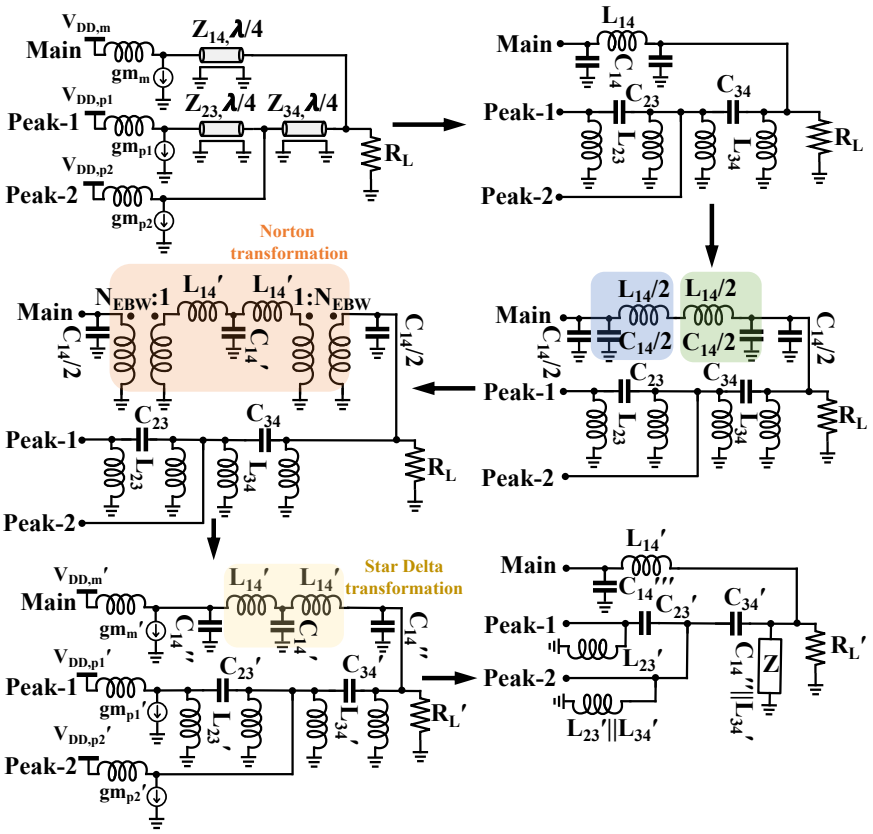
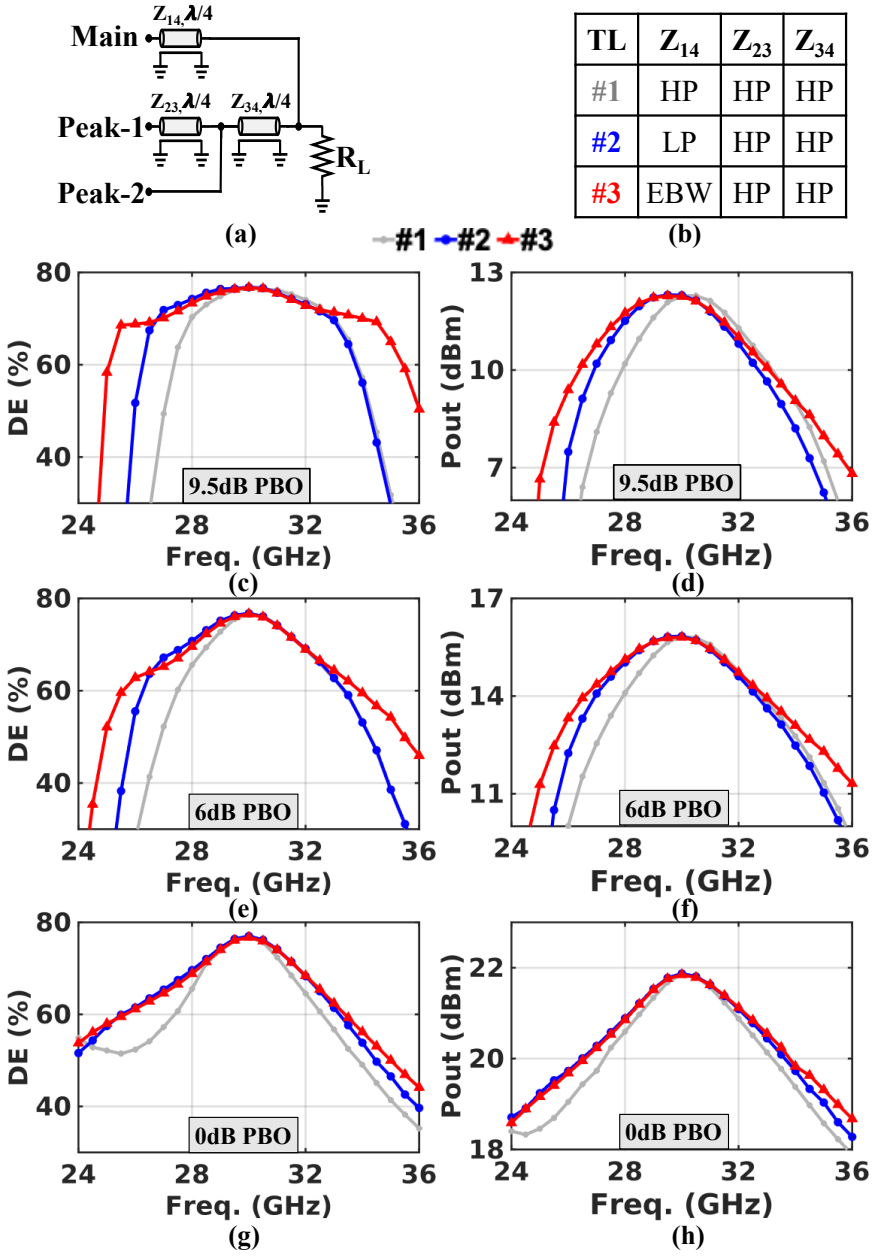


Fig. 4.4. The proposed compact EBW technique on a 3-way Doherty combiner.

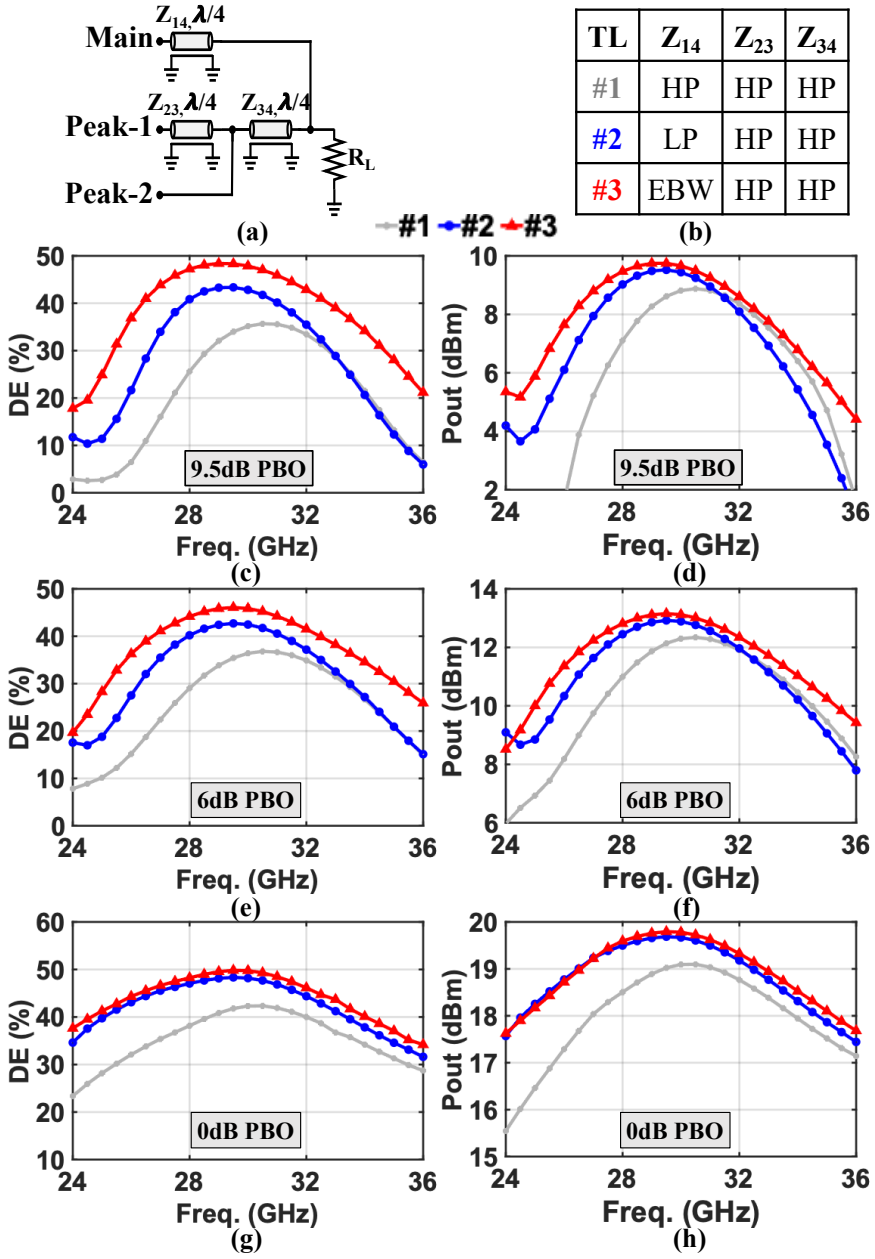
ployed on the Z_{14} TL, incorporating the final lumped-element circuit shown in Fig. 4.4. Each version is simulated using an ideal current source and ideal components with infinite QF. Fig. 4.5 reveals that version #3 exhibits enhanced bandwidth for DE, particularly noticeable at deep PBO levels. Considering a QF of 15 for the inductors and 25 for capacitors, all three cases are simulated [87, 105]. Fig. 4.6 presents the enhancement in DE and P_{out} at 0/6/9.5 dB PBO levels across the bandwidth for the proposed 3-way Doherty structure integrated with EBW.

Variations in the 3-way Doherty architecture can be achieved by alternating between the LP and HP models for the Z_{23} and Z_{34} TLs, as illustrated in Fig. 4.7(a). All simulations are carried out with an ideal PA model and a QF of 15/25 for the capacitors and inductors. The results indicate that alternative #4 in Fig. 4.7(a) outperforms its counterparts across frequencies at 9.5/6/0 dB PBO. The observed improvement in performance can be comprehended through an analysis of the HP and LP models of the TLs. Discrepancies in output powers, as shown in Figs. 4.6 and 4.7, stem from variations in passive losses, given that the HP model of the TL incorporates two inductors compared to the LP model, thereby increasing passive losses.



TL	Z_{14}	Z_{23}	Z_{34}
#1	HP	HP	HP
#2	LP	HP	HP
#3	EBW	HP	HP

Fig. 4.5. (a) The 3-way Doherty structure, (b) variations in the 3-way Doherty architecture, (c) DE versus frequency at 9.5 dB PBO, (d) P_{out} versus frequency at 9.5 dB PBO, (e) DE versus frequency at 6 dB PBO, (f) P_{out} versus frequency at 6 dB PBO, (g) DE versus frequency at 0 dB PBO, and (h) P_{out} versus frequency at 0 dB PBO using the ideal inductor and capacitor.



TL	Z_{14}	Z_{23}	Z_{34}
#1	HP	HP	HP
#2	LP	HP	HP
#3	EBW	HP	HP

Fig. 4.6. (a) The 3-way Doherty structure, (b) variations in the 3-way Doherty architecture, (c) DE versus frequency at 9.5 dB PBO, (d) P_{out} versus frequency at 9.5 dB PBO, (e) DE versus frequency at 6 dB PBO, (f) P_{out} versus frequency at 6 dB PBO, (g) DE versus frequency at 0 dB PBO, and (h) P_{out} versus frequency at 0 dB PBO using QF of 25/15 for capacitors and inductors.

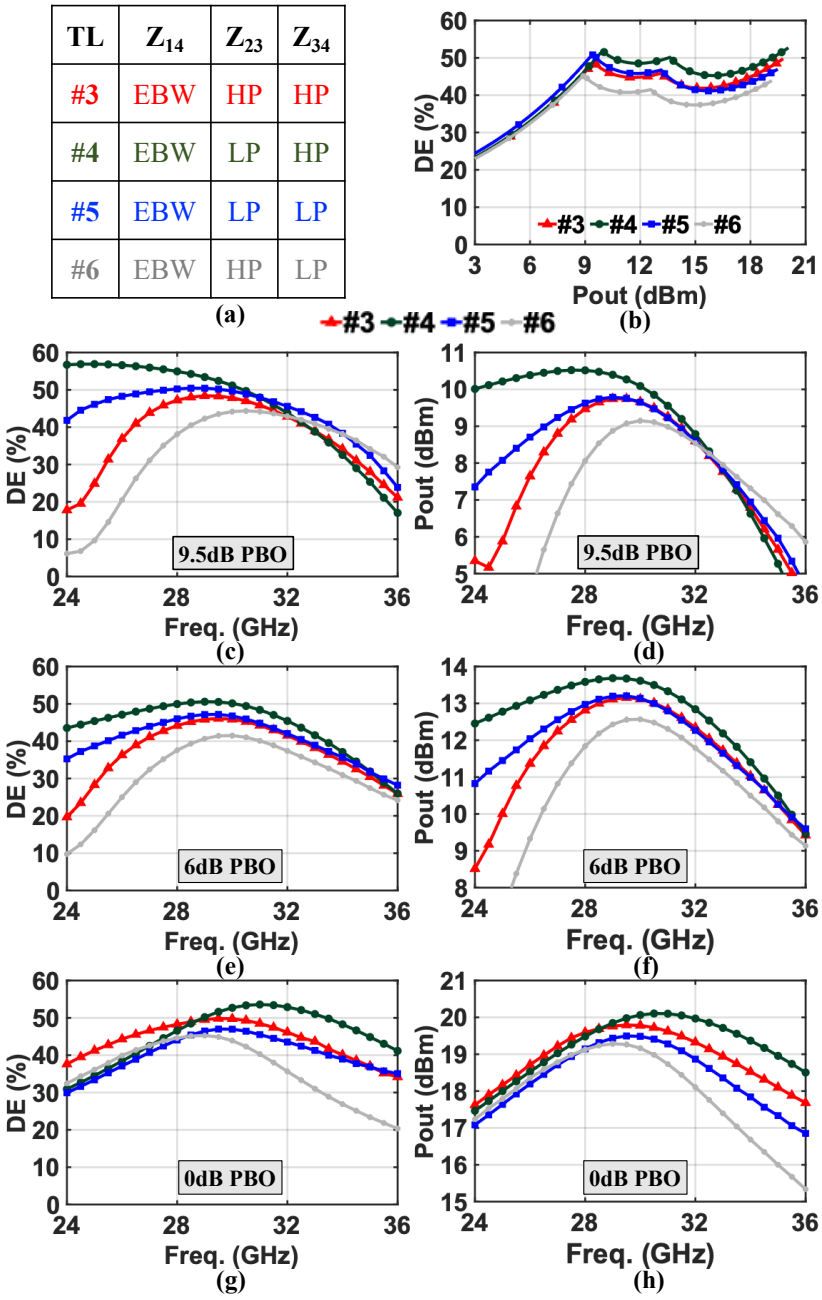


Fig. 4.7. (a) Variations in the 3-way Doherty architecture, (b) DE versus P_{out}, (c) DE across frequency at 9.5 dB PBO, (d) P_{out} across frequency at 9.5 dB PBO, (e) DE versus frequency at 6 dB PBO, (f) P_{out} across frequency at 6 dB PBO, (g) DE across frequency at 0 dB PBO, and (h) P_{out} across frequency at 0 dB PBO using QF of 25/15 for capacitors and inductors.

4.3.2. ANALYSIS OF HIGH-PASS AND LOW-PASS MODELS OF TRANSMISSION LINES

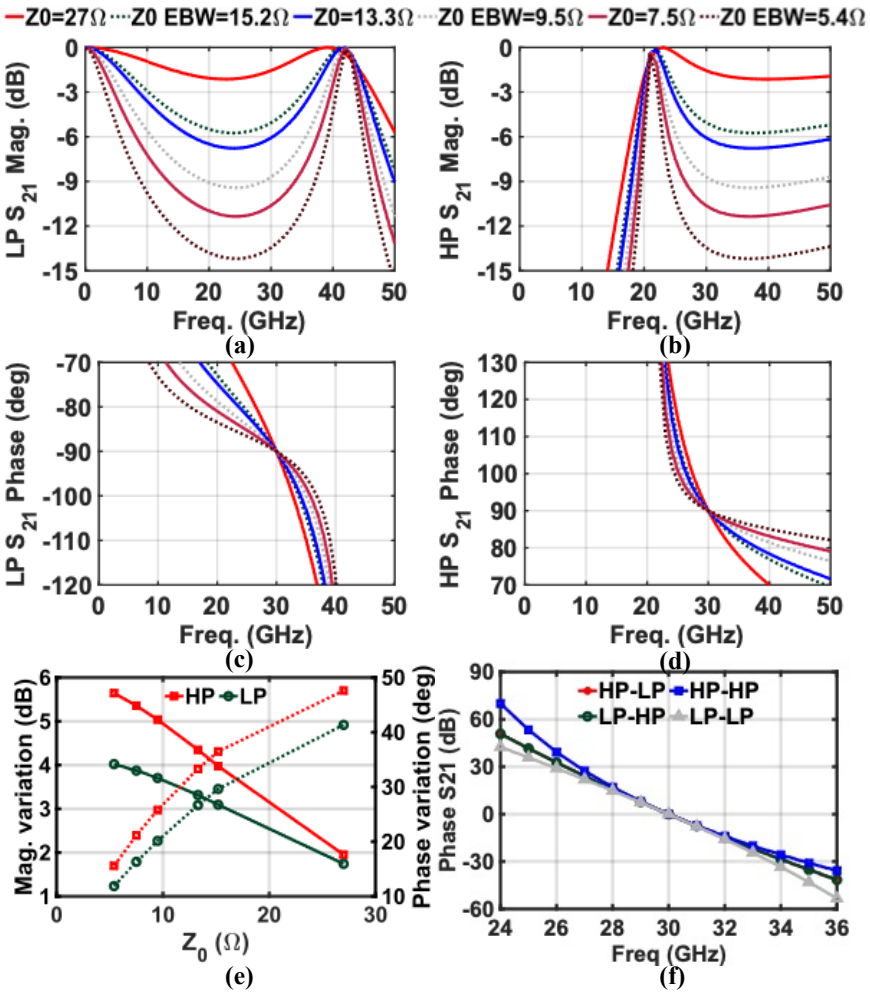


Fig. 4.8. Magnitude of TL for different Z_0 for (a) LP, (b) HP, phase of TL for different Z_0 for (c) LP, (d) HP, (e) magnitude variation and phase variation versus Z_0 of TL across the frequency 24 –to-36 GHz, and (f) phase variation of S_{21} of the cascaded lumped element models of the TLs with Z_0 = 50 Ω versus frequency.

Fig. 4.8(a)/(b)/(c)/(d) presents the magnitude and phase profiles of S_{21} for the LP and HP lumped element models (as illustrated in Fig. 4.3(a)/(b)) of the TL over various Z_0 settings spanning the frequency range of 24-to-36 GHz. After applying the EBW technique, the new value of the inductors and capacitors can be calculated using (4.1). Then, the Z_0 EBW in Fig. 4.8(a)/(b)/(c)/(d) can be calculated. The Z_0 and Z_0 EBW can be related as

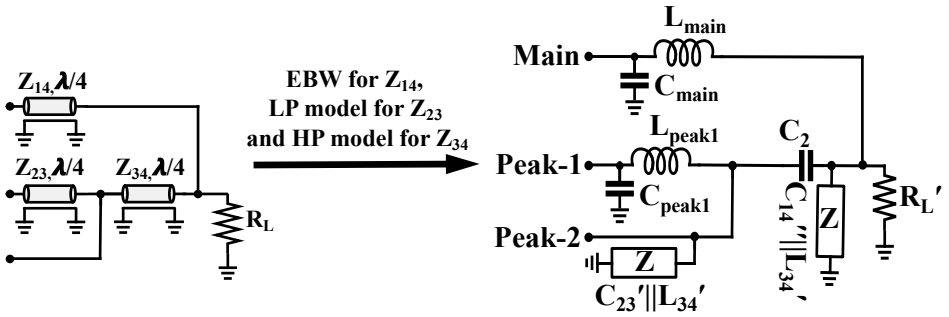


Fig. 4.9. Version #4 schematics, which uses EBW for Z_{14}, LP for Z_{23} and HP for Z_{34}.

shown in (4.2).

$$Z_0 \text{ EBW} = \frac{Z_0}{N_{EBW}^2} \tag{4.2}$$

Additionally, Fig. 4.8(e) exhibits the variations in magnitude and phase of TL's S_{21} within the frequency range of 24-to-36 GHz, relative to different Z_0 values. These visualizations reveal a noteworthy trend: as the Z_0 of the TL decreases, phase variation diminishes, while the reverse is observed for magnitude variation. Furthermore, the LP model of the TL exhibits lower phase and magnitude variations compared to the HP model. In Fig. 4.8(f), the phase variation of S_{21} is presented against frequency, examining cases where lumped element models of the TLs (with $Z_0 = 50\,\Omega$) are arranged in distinct configurations, such as HP-LP, LP-HP, HP-HP, and LP-LP. This analysis suggests that both HP-LP and LP-HP configurations exhibit relatively flat phase responses across frequencies when contrasted with the other configurations.

Among all considered versions, version #4 (depicted in Fig. 4.9) demonstrates superior performance in terms of bandwidth. This feature can be attributed to its integration of two LP models for the TLs and the application of EBW, which consequently reduces the Z_0 of each TL. Furthermore, version #4 incorporates a hybrid of LP and HP circuits within the peak PAs, leading to diminished phase variation in the equivalent passive network as compared to version #5. The adjacency of an LP structure to the active power devices contributes to the absorption of parasitic drain-source capacitance. Additionally, the utilization of EBW results in reduced inductor values, facilitating smoother layout implementation and less susceptibility to QF influences. Finally, the proposed 3-way Doherty architecture resembles an inverted 2-way Doherty PA [65, 106], enhancing its operational bandwidth.

The impact of the EBW technique, combined with the use of an equal number of HP and LP models for the TLs, is more pronounced in higher-order Doherty architectures. Appendix B illustrates the application of the EBW technique to a 4-way Doherty PA. Among the variations analyzed, the version incorporating the EBW technique and utilizing an equal distribution of HP and LP models for the TLs demonstrates superior performance.

4.4. PROPOSED BALUN-FIRST 3-WAY DOHERTY POWER COMBINER

Mm-wave PA implementations commonly adopt push-pull PAs to enhance stability and increase output power. Moreover, these push-pull PAs typically integrate a balun transformer at their end, catering to single-ended antenna configurations. Fig. 4.10(a) displays the schematic of version #4, presented in a push-pull configuration, while its corresponding layout is realized in 40 nm Bulk CMOS, as depicted in Fig. 4.10(b).

Fig. 4.10(c)/(d) reveals that push-pull PAs encounter varied impedances, particularly during PBO, due to unintended coupling among traces within the layout. Furthermore, the final circuit in Fig. 4.10(a) necessitates extra RF chokes to provide dc voltages to the main, peak-1, and peak-2 PAs, adding to the circuit's intricacy. These challenges can be addressed by splitting the output balun into three separate baluns and strategically relocating them to the drain terminals of the respective PAs [91].

4.4.1. DESIGN METHODOLOGY

Fig. 4.11(a) outlines the stepwise progression involved in the design of a balun-first 3-way Doherty combiner. The balun's turn ratio (NT) is derived using (4.3), where n signifies the ratio between secondary inductance (L_s) and primary inductance L_p (4.4), and k_m represents the balun's coupling factor.

$$NT = n * k_m \tag{4.3}$$

$$n = \sqrt{\frac{L_s}{L_p}} \tag{4.4}$$

First, L_2 is repositioned to the main path, followed by the relocation of C_m, L_m, and L_2 to the drain side of the main PA through (4.5), (4.6), and (4.7).

$$L_{k\_m} = L_m * NT_m^2 \tag{4.5}$$

$$L_{m\_m} = L_2 * NT_m^2 \tag{4.6}$$

$$C'_m = \frac{C_m}{NT_m^2} \tag{4.7}$$

The main balun's design parameters (L_{p_m}, L_{s_m}, and $k_{m,m}$) are then computed using (4.8), (4.9), and (4.10) [107]. NT_m can be flexibly chosen, making n equal to 1. Consequently, the primary and secondary inductances can match size-wise, resulting in a single-turn balun. This type exhibits higher self-resonance than multi-turn baluns. NT_m and $k_{m,m}$ within the range of 0.6 to 0.7 is easier to implement in the layout at mm-wave. Next, practical balun transformers with L_{p_m}, L_{s_m}, and $k_{m,m}$ replace the ideal transformer, magnetizing inductance (L_m), and leakage inductance (L_k) in the main path.

$$L_{k\_m} = (1 - k_{m,m}^2) * L_{s\_m} \tag{4.8}$$

$$L_{m\_m} = k_{m,m}^2 * L_{s\_m} \tag{4.9}$$

$$n * k_{m,m} = NT_m \tag{4.10}$$

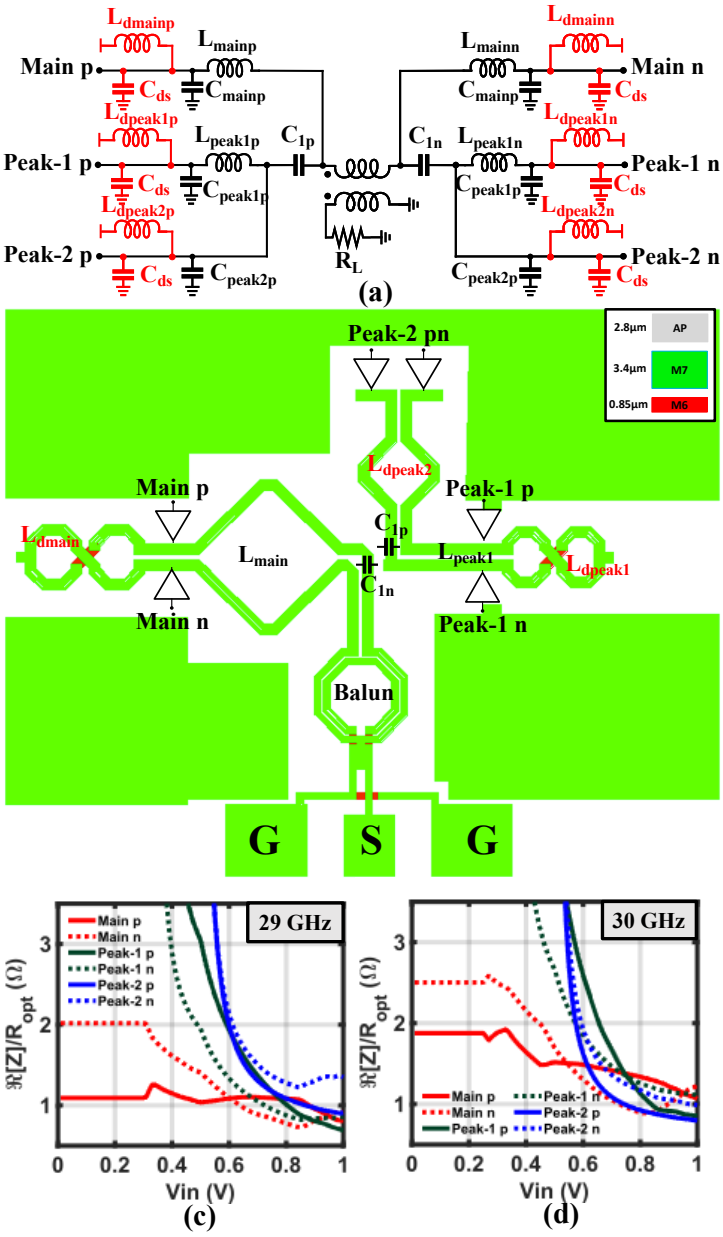


Fig. 4.10. Version #4 push-pull (a) schematic, (b) layout, and (c) normalized impedance of main, peak-1 and peak-2 PA versus V_{in} at 29 GHz, and (d) 30 GHz.

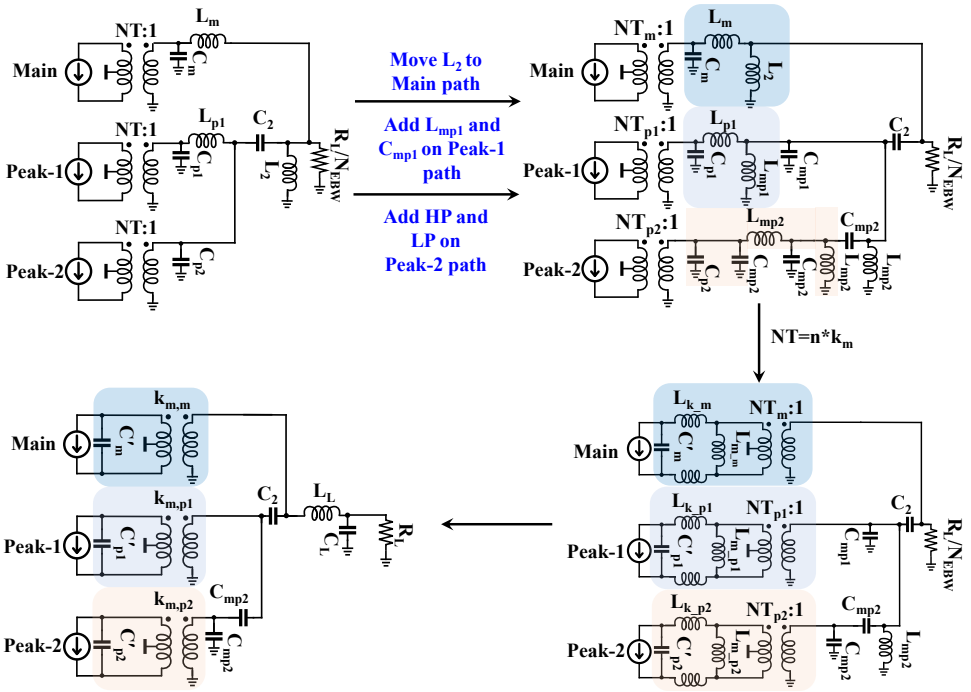


Fig. 4.11. Procedure to design the proposed balun-first 3-way Doherty.

Subsequently, L_{mp1}/C_{mp1} are introduced to the peak-1 path. C_{p1}, L_{p1}, and L_{mp1} are also shifted to the drain side of the peak-1 PA using (4.5), (4.6), and (4.7). The peak-1 balun is fashioned similarly to the main balun employing (4.8), (4.9), and (4.10). The LP/HP models of the TL are then incorporated into the peak-2 path. Analogous to the main and peak-1 PA paths, C_{p2}, C_{mp2}, and L_{mp2} can be relocated to the drain side of the peak-2 PA using (4.5), (4.6), and (4.7). The ideal transformer in the peak-2 PA path is replaced with practical balun transformers bearing L_{p_p2}, L_{s_p2}, and $k_{m,p2}$.

Finally, using the following equations, an L-match (L_L and C_L) is harnessed to convert R_L/N_{EBW} to R_L. The L-match proves advantageous by incorporating pad capacitance into C_L, and the trace connecting the Doherty output and pad is utilized for L_L design, thereby minimizing additional component losses in comparison to a C-match (refer to (4.11), and (4.12)).

$$\Re\{Z_L'\} = \frac{R_L}{N_{EBW}} = \frac{R_L}{1+\omega^2 C_L^2 R_L^2} \tag{4.11}$$

$$\Im\{Z_L'\} = 0 \implies L_L = \frac{C_L R_L^2}{1+\omega^2 C_L^2 R_L^2} \tag{4.12}$$

The final circuit depicted in Fig. 4.11 features a compact network, incorporating only one inductor, four capacitors, and three baluns. The balun's turn ratio (NT), C_{mp1}, and L_{mp2} are design parameters adaptable to achieve optimized values for layout synthesis. In

this regard, C_{mp1} and L_{mp2} are selected to resonate at the desired operational frequency (30 GHz). C'_m, C'_{p1}, and C'_{p2} can be used to absorb the parasitic C_{ds} of the main, peak-1, and peak-2 PA.

In summary, with a specified P_{out}, V_{DD}, and R_L, a balun-first 3-way Doherty with bandwidth enhancement can be designed using the equations outlined in Fig. 4.1(d), coupled with the closed-loop equations above. These equations furnish initial values for the design parameters. Ultimately, the balun-first 3-way Doherty configuration is realized within the available technology and optimized through electromagnetic (EM) simulations.

4.4.2. LAYOUT AND EM SIMULATION RESULTS

The implementation of the proposed balun-first 3-way Doherty layout is carried out using 40 nm CMOS bulk technology, as depicted in Fig. 4.12(a). This layout comprises three baluns, with coupling factors of 0.7, 0.64, and 0.7 assigned to the main, peak-1, and peak-2 respectively. The QF of the spiral/slab inductors is increased more than twofold using parallel slot lines of minimum width than utilizing one thick line of the required width, as shown in Fig. 4.12(a). The rationale behind this choice lies in the signal's surface travel due to the skin effect, where splitting the lines increases the surface area, thereby reducing resistance and augmenting the QF [100]. This QF enhancement is particularly noticeable in slab and single-turn inductors/baluns, highlighting the preference for single-turn baluns in the proposed output network. Through optimization of component values based on the initial calculations presented in the preceding section, improved performance is achieved, and these updated values are displayed in Fig. 4.12(b).

All simulation results depicted in Fig. 4.12(c)/(d)/(e)/(f) are executed utilizing the EM model of the proposed output network (depicted in Fig. 4.12(a)) generated using Momentum, capacitors possessing a QF of 25, and ideal PA models. In Fig. 4.12(c), the impedance encountered by the main, peak-1, and peak-2 push-pull PAs is illustrated when employing the EM model of the proposed balun-first technique, which is normalized to R_{opt}. The mismatch in impedance experienced by the push-pull counterparts remains below 0.5. The relationship between DE and P_{out} exhibited in Fig. 4.12(d) confirms the desired 3-way Doherty operation at 30 GHz. Furthermore, the proposed output network achieves a passive efficiency surpassing 47 % at 30 GHz. Ultimately, the proposed 3-way Doherty combiner demonstrates a DE exceeding 20/25/30 % at PBO levels of 9.5/6/0 dB across the 27-to-34 GHz frequency band (as depicted in Fig. 4.12(f)). Fig. 4.12(g)/(h)/(i) shows the normalized impedance of the main, peak-1 and peak-2 PA versus V_{in} across frequency. Z_{Diff} is the differential impedance seen by the main, peak-1 and peak-2 PA. It is normalized to $2R_{opt}$ where R_{opt} is the single-ended optimum impedance to achieve the required output power.

4.5. CIRCUIT IMPLEMENTATION

Fig. 4.13(a) illustrates a detailed diagram of the proposed PA configuration. The initial component is an input splitter (Fig. 4.14(a)) consisting of three QHCs. Subsequently, each branch, namely the main, peak-1, and peak-2 paths, includes an input balun (Fig. 4.14(b)),

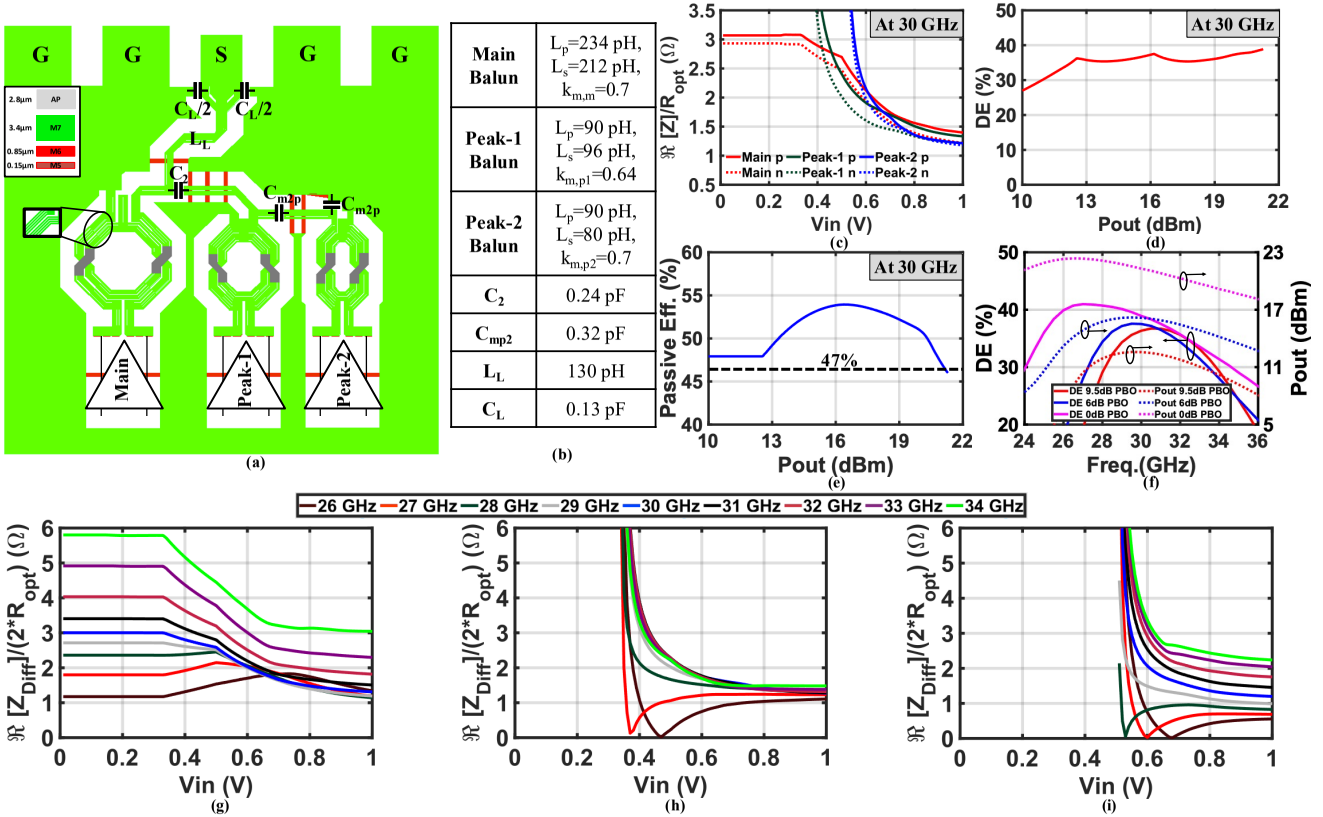


Fig. 4.12. (a) Layout of the proposed balun first 3-way Doherty, (b) components' value, (c) impedance of main, peak-1, and peak-2 PA versus V_{in} at 30 GHz, which is normalized to R_{opt}, (d) DE versus P_{out} at 30 GHz, (e) passive efficiency of the proposed balun first 3-way Doherty combiner at 30 GHz, and (f) DE and P_{out} across frequency at 0/6/9.5 dB PBO, (g) impedance of main PA, (h) peak-1 PA, and (i) peak-2 PA versus V_{in} which is normalized to $2R_{opt}$.

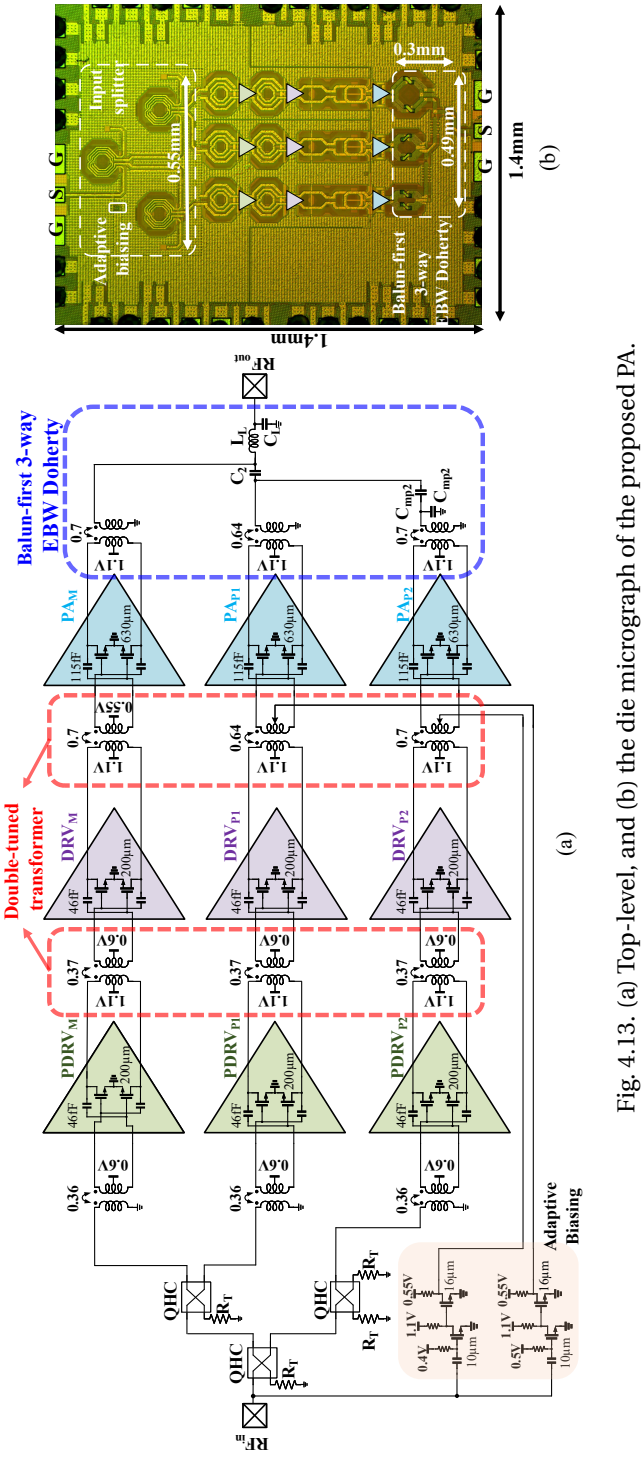


Fig. 4.13. (a) Top-level, and (b) the die micrograph of the proposed PA.

PDRV, inter-stage matching (Fig. 4.14(c)), DRV inter-stage matching (Fig. 4.14(d)), and the PA itself.

The arrangement of the input splitter, shown in Fig. 4.14(a), consists of three transformer-based single-ended QHCs [108] designed to generate phase shifts of 90° and 180°. The unused (port 5) and isolation ports are properly terminated at 50 Ω. The type of resistor used is P+ poly resistor without salicide. The S-parameters and phase response of the main, peak-1, and peak-2 paths are depicted in Fig. 4.14(f)/(g), utilizing an EM simulated model of the input splitter. Notably, the input matching (S_{11}) exceeds −16 dB, and the isolation between the main and peak-1/peak-2 paths surpasses −21 dB within the 24-30 GHz frequency range, as indicated in Fig. 4.14(f). The magnitude and phase characteristics of signals in these paths are presented in Fig. 4.14(f)/(g), with the phase difference remaining below 5° within the specified frequency band. Although using three QHCs improves S_{11} variations and phase differences compared to using two, there is a trade-off with an increased insertion loss of 1.8 dB [109].

After the input splitter, a balun is utilized to transform the single-ended signal into a differential signal. This balun employs a double-tuned transformer approach [110, 111] to achieve wide-ranging matching, resulting in a passive efficiency of 71% (as shown in Fig. 4.14(b)). Alternatively, it is possible to use a balun at the input in combination with a differential input splitter. However, this arrangement necessitates the inclusion of an interstage component for proper matching between the input splitter and PDRV, potentially leading to increased passive losses. In this scenario, the balun serves the dual purpose of converting the signal from single-ended to differential and providing interstage matching. The necessary power gain is achieved by integrating two additional stages, each employing a neutralized common-source transistor with 50 fingers and a width of 1 µm (refer to Fig. 4.13(a)). A bias of 0.6 V is applied to PDRVs and DRVs. However, this architectural choice negatively impacts PAE. The inter-stage matching connecting PDRV and DRV utilizes a double-tuned transformer network [110, 111] to achieve wide matching, with its parameter values shown in Fig. 4.14(c). It provides a passive efficiency of 75 %, calculated using the equation from [112].

The PA utilizes common-source transistors and neutralization capacitors set at a bias of 0.55 V. To optimize the cut-off frequency (f_T) and maximize the highest maximum oscillation frequency (F_{max}), the PA design incorporates seven unit cells, each consisting of 50 fingers with a width of 1.8 µm. Fig. 4.15(a)/(b) illustrates two variations of the unit cell layout within the PA. The second iteration reduces side wall capacitance (C_{sw}) by eliminating metal one ($m1$) and contacts (CO) on both sides of the drain, as shown in Fig. 4.15(b). Additionally, the metal five ($m5$) trace is made thinner to reduce overlap capacitance (C_{ov}). These modifications collectively minimize the parasitic C_{ds}. Version 2 accomplishes a C_{ds} of 57 fF, marking an enhancement compared to the 69 fF in version 1, while simultaneously improving F_{max}.

The intermediary stage connecting the DRV and PA employs a double-tuned transformer technique to achieve wideband matching. The schematic of this double-tuned transformer is depicted in Fig. 4.14(e), and the impedance experienced by the DRV (Zd_{DRV}) is computed using (4.13) [31]. Notably, Cin_{OS} and Rin_{OS} correspond to the input capacitance and resistance of the PA, measured at approximately 250 fF and 6 kΩ, respectively. Additionally, R_{SEC} is the resistance in parallel with the PA, and Cds_{DRV} accounts for the

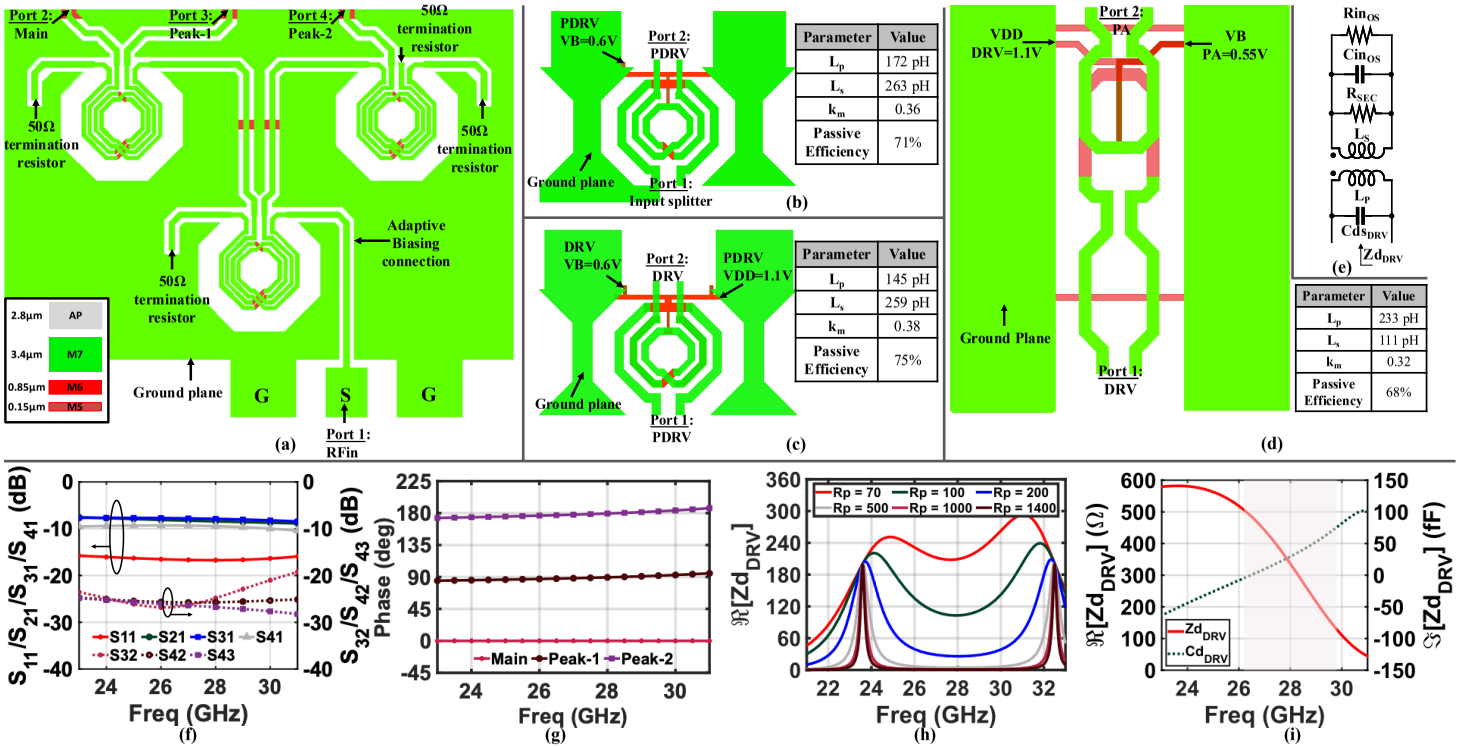


Fig. 4.14. (a) Layout of the input splitter, (b) input balun, (c) PDRV and DRV interstage matching transformer, (d) DRV and PA interstage matching transformer, (e) schematic of double-tuned interstage between DRV and PA, (f) S-parameters (S_{11}, S_{21}, S_{31}, S_{41}, S_{32}, S_{42}, and S_{43}) across frequency, (g) phase of main, peak-1 and peak-2 across frequency, (h) impedance plotted using (4.13) across frequency, and (i) impedance of the EM model across frequency.

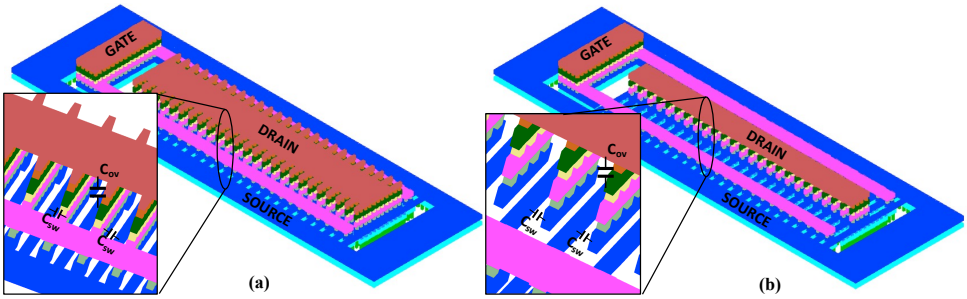


Fig. 4.15. (a) Version 1, and (b) version 2 of the PA unit cell.

parasitic drain-source capacitance of the DRV, respectively. M is the mutual inductance between the primary (L_p) and secondary (L_s) windings.

Fig. 4.14(h) visually illustrates the real part of impedance across varying frequencies as the parameter R_p changes. Most importantly, higher R_p values result in a dip in the center frequency, thereby compromising the matching. Conversely, lower R_p values lead to a reduced voltage swing at the gate of the PA, preventing the PA from entering saturation. It is worth highlighting that the PA's substantial dimensions contribute to an increased Cin_{OS}, making wideband matching challenging. The layout of the interstage and specific component values are provided in Fig. 4.14(d). Fig. 4.14(i) employs the EM model of the interstage to present both the real and imaginary parts of the impedance observed by the DRV. Significantly, the interstage 3 dB bandwidth is constrained to a mere 3 GHz, limiting the operational bandwidth despite the wideband capabilities of the output network.

An adaptive biasing circuit depicted in Fig. 4.13 is employed to implement Doherty load modulation. Adapted from [113], this circuit includes an envelope detector with an RF input and a turn-on voltage, placed as shown in Fig. 4.14(a). The specified turn-on voltage activates the peak PAs, set at 0.5 V and 0.4 V for peak-1 and peak-2 PAs, respectively. The adaptive biasing circuit offers a 3 dB bandwidth of 2.5 GHz.

$$Zd_{DRV} = \frac{-\omega\left(-\mathrm{Cin}_{OS} R_P T\omega^2 + jT\omega - L_P R_P\right)}{\left(jTR_P Cds_{DRV}\,\mathrm{Cin}_{OS}\omega^4 + Cds_{DRV}T\omega^3 + j\left(Cds_{DRV}L_P + \mathrm{Cin}_{OS}L_S\right)R_p\omega^2 + L_S\omega - jR_p\right)}$$

where,

$$T = -L_P L_S + M^2$$
$$M = k_m\sqrt{L_P L_S}$$
$$R_p = R_{SEC} \| \mathrm{Rin}_{OS} \tag{4.13}$$

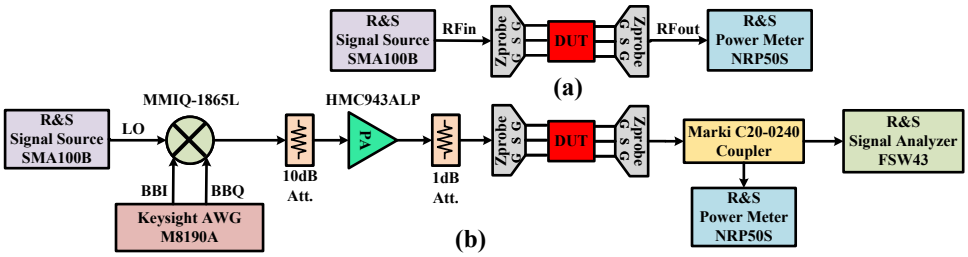


Fig. 4.16. Simplified (a) continuous-wave and (b) modulation measurement setups.

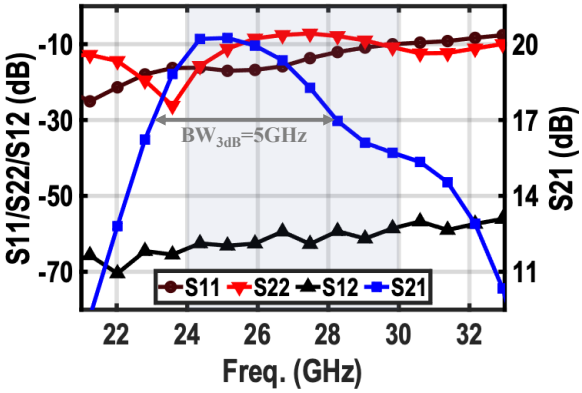


Fig. 4.17. S-parameter measurement results of the proposed balun-first 3-way Doherty PA.

4.6. MEASUREMENT RESULTS

The proposed PA is fabricated in 40 nm bulk CMOS technology (Fig. 4.13(b)). The core (active) area of the proposed balun-first 3-way Doherty is $1.4 \times 0.55\,\text{mm}^2$. All measurements are performed using a high-frequency probe station. The dc supplies, bias voltages, and turn-on voltage for adaptive biasing are wire-bonded directly to an FR4 printed circuit board (PCB). This work uses the 1.1 V supply voltage for the PAs, DRV, and PDRV amplifiers. Fig. 4.16(a)/(b) shows the continuous wave (CW) and modulated measurement setup. The insertion loss of the probes (Z-probe), cables, and directional couplers are measured and de-embedded.

4.6.1. CONTINUOUS WAVE MEASUREMENT RESULTS

The small-signal S-parameter performance is measured using the Keysight HP8753D vector network analyzer. As Fig. 4.17 demonstrates, the proposed PA achieves more than 5 GHz small-signal BW_{3dB} where its S_{11}/S_{12} are less than $-10/-50$ dB over a 23- to-28 GHz band. At 26 GHz, PA's S_{22} is -8.5 dB, while its input matching is -16.8 dB. The PA offers 19.9 dB small-signal gain at 26 GHz.

The large signal CW measurement results are reported in Fig. 4.18 for various opera-

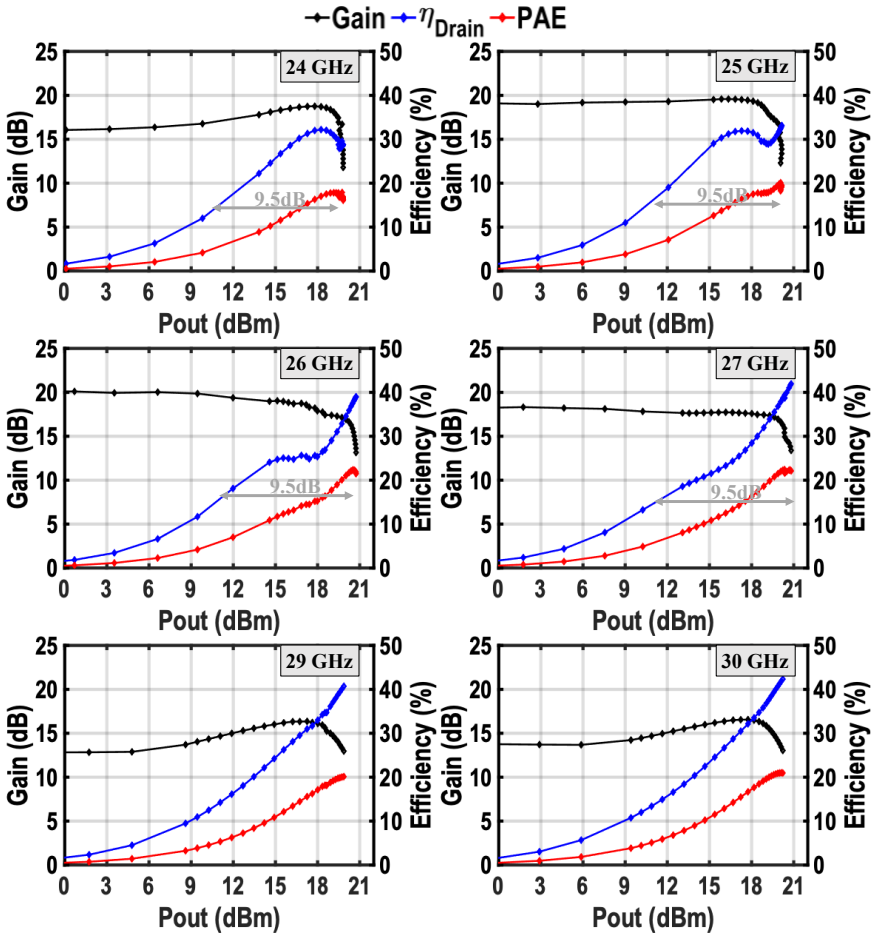


Fig. 4.18. The measured gain, last-stage DE, and PAE versus P_{out} at various frequencies.

tional frequencies. At 25 GHz, the P_{1dB} and P_{sat} are 19.4 dBm and 20.1 dBm, respectively. Its DE at P_{sat}, 6 dB PBO, and 9.5 dB PBO are 33 %, 25 %, and 15 %, respectively. Likewise, Fig. 4.18 indicates active load modulation only materializes over the 24-to-26 GHz band. So, the PBO efficiency enhancement bandwidth is 2 GHz. The efficiency at deep PBO is lower due to the smaller channel resistance of the device and finite QF of C_{ds}, especially of the main PA (refer to Section 4.7). Note that the bandwidth is limited due to the high impedance transformation ratio required by the interstage between DRV and PA, as discussed in the earlier section. PAE is degraded since adaptive biasing is applied only to peak PAs and not the DRV and PDRV.

Fig. 4.19 shows the P_{out} and DE across frequency at 12 dB PBO, 9.5 dB PBO, 6 dB PBO, and full power. It can be seen that the proposed PA achieves more than 20 dBm peak output power and a DE of better than 10 %/15 %/22 %/33 % at 12 dB/9.5 dB/6 dB/0 dB across the 24-to-30 GHz band. The PA achieves a 1 dB bandwidth of 6 GHz with respect

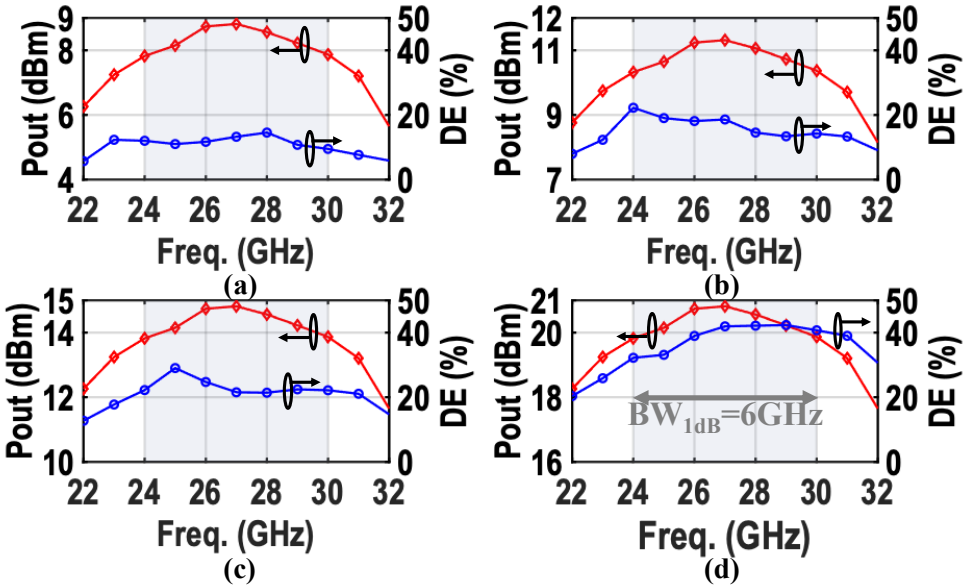


Fig. 4.19. P_{out} and DE across frequency at (a) 12 dB PBO, (b) 9.5 dB PBO, (c) 6 dB PBO, and (d) full power.

to the P_{sat}.

4.6.2. MODULATED SIGNAL MEASUREMENT RESULTS

The PA dynamic performance is verified by wideband modulated signals such as "64-QAM OFDM", "256-QAM OFDM", and "1024-QAM OFDM" signals. As demonstrated in Fig. 4.16(b), the baseband I/Q modulated signals are generated with an arbitrary waveform generator (AWG) (Keysight AWG M8190A) and upconverted using a Marki I/Q mixer (MMIQ-1865L). A directional coupler (Marki C20-0240) is employed at the output to provide the signal for an R&S FSW43 signal analyzer, while an R&S NRP50S measures the output power.

Fig. 4.20(a) exhibits 9.4 dBm/15 % P_{avg}/DE measured for a 6 Gb/s OFDM 64-QAM signal at 26 GHz with 9.8 dB PAPR. Its EVM/ACLR are −24.3 dB/ −30.1 dBc, respectively. Similarly, the proposed PA achieves 9.8 dBm/15 % P_{avg}/DE for a 4.8 Gb/s OFDM 64-QAM signal with EVM/ACLR of −23.5 dB/−29.5 dBc, respectively (Fig. 4.20(b)). For a 1.6 and 0.8 Gb/s OFDM 256-QAM signal with 10.2 dB PAPR, the proposed PA achieves an EVM/ACLR of −26.8 dB/−29.9 dBc and −25.7 dB/−30.5 dBc (Fig. 4.20(d) and Fig. 4.21(a)). The proposed PA is tested with a 0.5 Gb/s OFDM 1024-QAM signal, and the results are shown in Fig. 4.21(b). Furthermore, the spectral purity and constellation of a 400 MHz OFDM 64-QAM signal is measured at 26, 25, 27, 29, and 30 GHz with EVM/ACLR of −24.9 dB/−28.9 dBc, −24.1 dB/−30.7 dBc, −25.4 dB/−30 dBc, −25.5 dB/ −28.5 dBc, and −25 dB/−29.5 dBc which are illustrated in Fig. 4.20(c), Fig. 4.21 (c)/(d), and Fig. 4.22(a)/(b).

Fig. 4.23 illustrates the P_{avg} and DE for an OFDM signal with different bandwidths

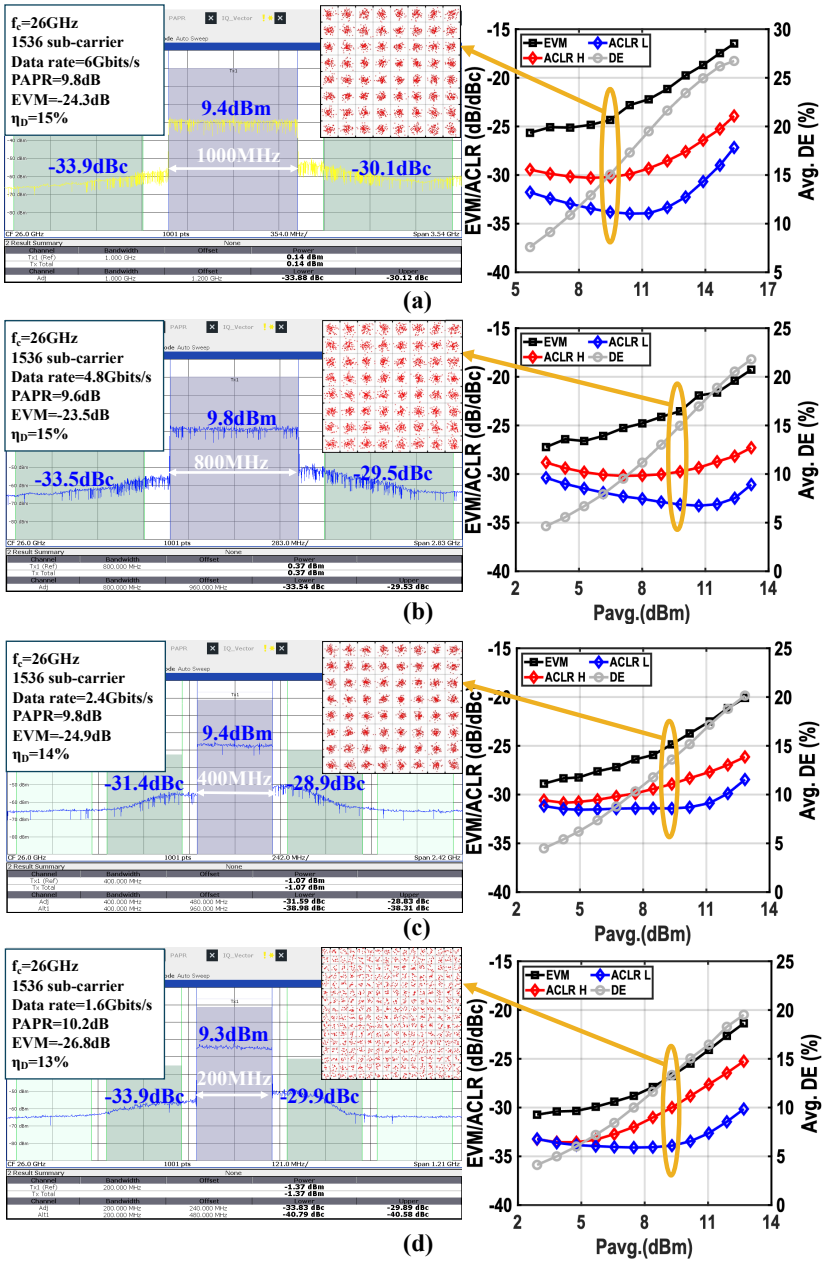


Fig. 4.20. (a) An OFDM 1000 MHz 64-QAM, (b) an OFDM 800 MHz 64-QAM, (c) an OFDM 400 MHz 64-QAM, (d) an OFDM 200 MHz 256-QAM at 26 GHz measurement results.

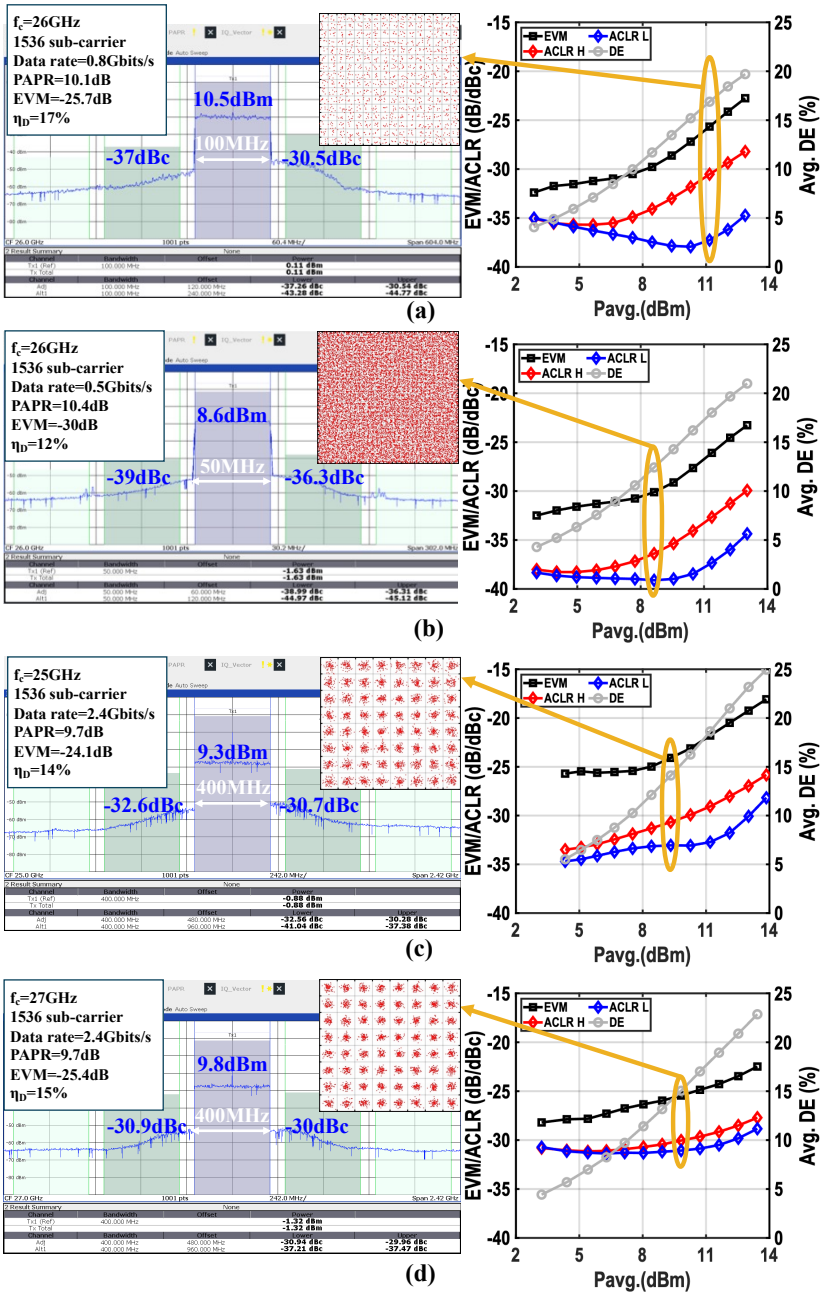


Fig. 4.21. (a) An OFDM 100 MHz 256-QAM, and (b) an OFDM 50 MHz 1024-QAM at 26 GHz, (c) An OFDM 400 MHz 64-QAM at 25 GHz, and (d) 27 GHz measurement results.

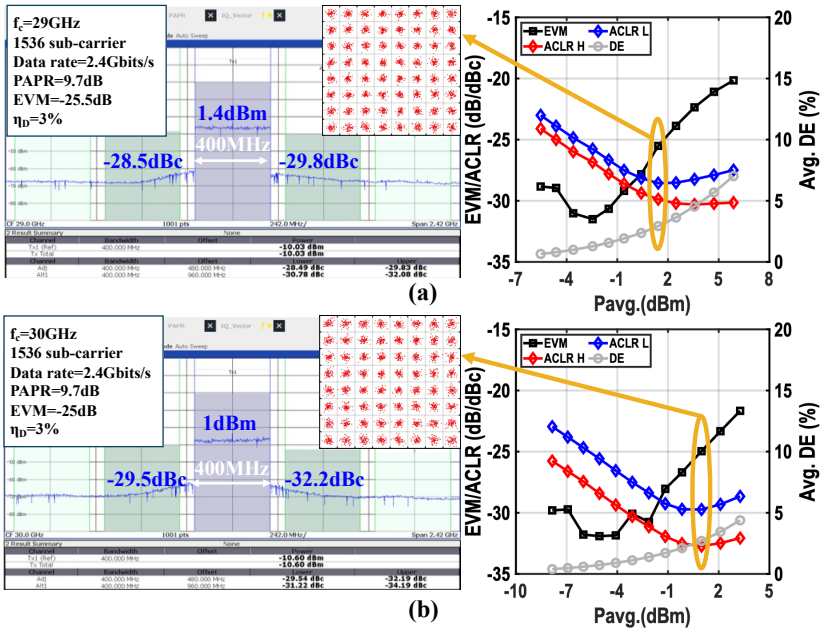


Fig. 4.22. (a) An OFDM 400 MHz 64-QAM at 29 GHz, and (b) 30 GHz measurement results.

(800/400/200/50 MHz) and modulation schemes (64/256/1024) within the 24-to-30 GHz frequency band, aiming to meet specific EVM requirements. To elaborate, considering the minimum EVM requirement for a 64-QAM signal as −21.9 dB (Table 1.2), and providing a 3 dB margin, we present the P_{avg}/DE for an EVM of −25 dB. The proposed power amplifier achieves an average P_{avg}/DE performance surpassing 5.5 dBm/7 % in the 25-to-27 GHz band, as shown in Fig. 4.23(a). Additionally, Fig. 4.23(b)/(c)/(d) exhibit corresponding results for OFDM signals with bandwidths of 400 MHz, utilizing 64-QAM, 200 MHz with 256-QAM, and 50 MHz with 1024-QAM modulation schemes, respectively.

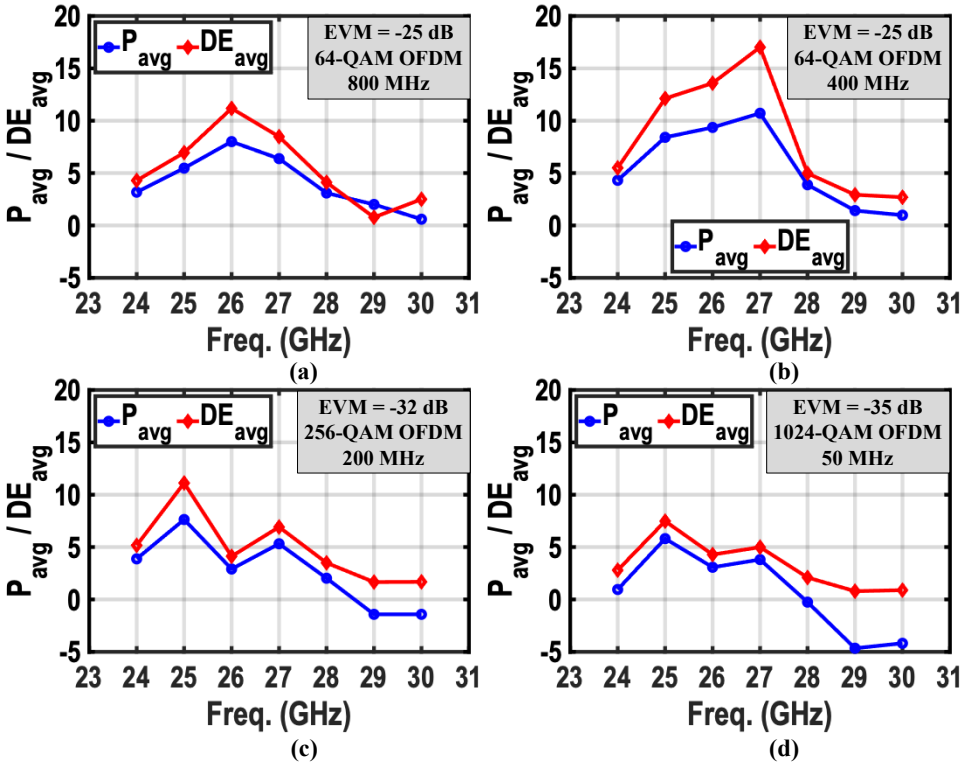


Fig. 4.23. P_{avg} and DE_{avg} for (a) an OFDM 800 MHz 64-QAM, (b) an OFDM 400 MHz 64-QAM, (c) an OFDM 200 MHz 256-QAM, and (d) an OFDM 50 MHz 1024-QAM across frequency to achieve a certain EVM.

4.7. ANALYSIS OF BACK-OFF EFFICIENCY LOSS IN N-WAY DOHERTY ARCHITECTURES

Fig. 4.24(a) illustrates the proposed 3-way Doherty configuration, where C_{ds} represents the drain-source capacitance of the device, and L_{ds} is the inductor used for resonating out the C_{ds}. In practical implementations, the device has a channel resistance, and C_{ds} possesses a finite quality factor. These can be represented by an R_{Loss}, as depicted in Fig. 4.24(a), although ideally, it should be infinite.

Fig. 4.24(b) introduces R_{Loss} to all three PAs (main, peak-1, and peak-2). All other aspects in the simulation are considered ideal. The degradation in DE is less significant when $R_{Loss} = 55\,\Omega$ is added to all three PAs (blue curve) compared to when R_{Loss} is added only to the main PA (red curve). This emphasizes the dominant impact of the main PA's R_{Loss} on deep PBO efficiency compared to that of peak-1 and peak-2 PAs.

Fig. 4.25 illustrates the impedance and current profiles of N-way Doherty PAs designed to achieve P_{sat} of 22 dBm. It is observed that the impedance seen by the main PA at deep PBO increases with higher-order N-way Doherty configurations. Similar to

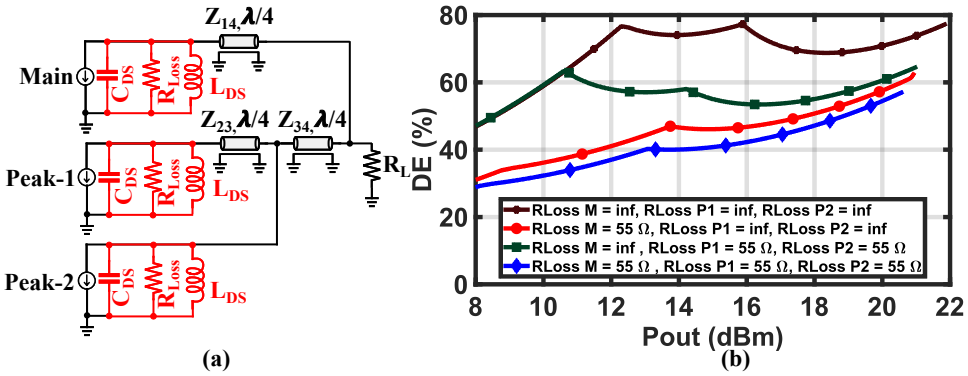


Fig. 4.24. (a) Proposed 3-way parallel Doherty with R_{Loss}, and (b) DE versus Pout with R_{loss} = 55 Ω/ ∞ for the main, peak-1 and peak-2 PA.

Fig. 4.24(a), C_{ds}, L_{ds}, and R_{Loss} can be added to the schematics of the 2-way (Fig. 2.17), 4-way (Fig. 3.5(d)), 5-way Doherty (Fig. 3.7(d)).

For N-way Doherty PAs, the main PA sees a parallel combination of R_{Loss} and R_{main} (the impedance presented to the drain of the main PA). Ideally, R_{Loss} should be close to infinite and R_{main} to be as small as possible. To achieve the same P_{out}, the current is smaller, enabling the use of smaller devices, which reduces C_{ds} and increases R_{Loss} (as shown in Fig. 4.25).

However, despite these adjustments, the efficiency for 3-/4-/5-way linear Doherty PAs at deep PBO levels (6/9.5/12 dB PBO) shows minimal improvement compared to a 2-way Doherty PA. This is because, at back-off, the main PA in higher-order linear Doherty configurations experiences larger load modulation, which amplifies the effect of R_{Loss} due to its parallel combination with R_{main}. Additionally, from Table 3.1, it is seen that higher-order linear N-way Doherty configurations introduce greater passive losses due to the increased number of lumped components, further reducing efficiency. As a result, the back-off efficiency of higher-order N-way Doherty PAs can be lower than that of lower-order designs.

In conclusion, symmetric linear N-way Doherty configurations struggle to achieve high efficiency at deep PBO due to the device's channel resistance and the finite QF of C_{ds}.

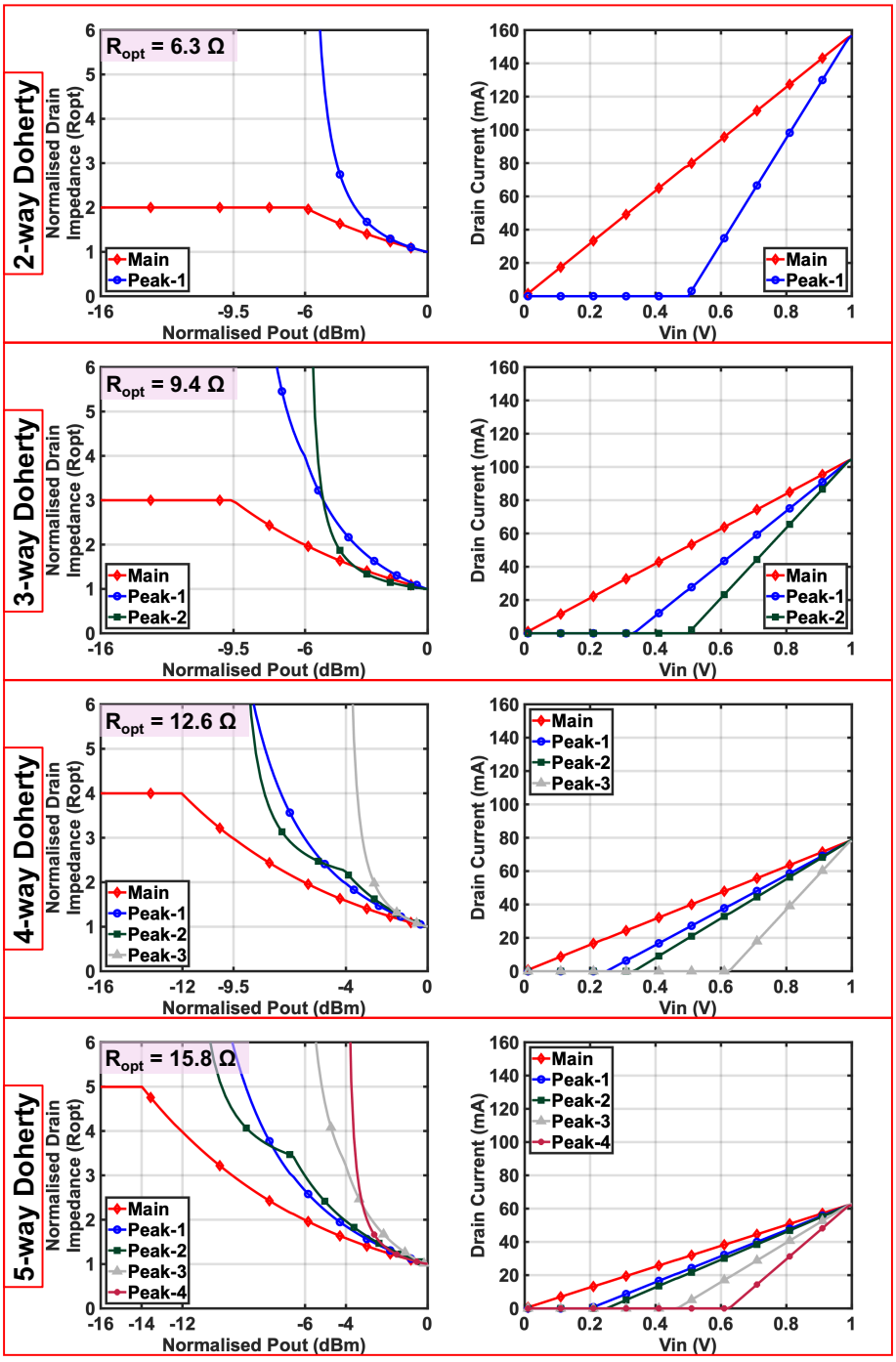


Fig. 4.25. Impedance and current profiles of N-way Doherty that can generate P_{sat} = 22 dBm.

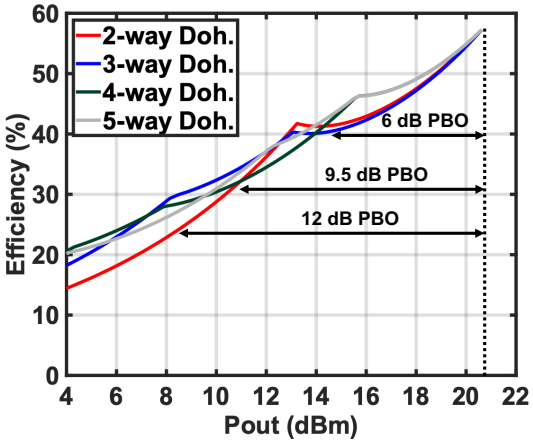


Fig. 4.26. DE vs. P_{out} for N-way Doherty PA with R_{Loss} added to main and peak PAs.

4.8. COMPARISON WITH STATE-OF-THE-ART

The performance evaluation of the balun-first 3-way Doherty PA is summarized in Table 4.1 and compared to that of previous designs. The results highlight that even with a supply voltage as low as 1.1 V, our compact single-supply three-stage mm-wave front-end achieves reasonable P_{avg} and power gain characteristics. Furthermore, its core area is the second best among 3-/4-way Doherty PAs. Across the 24-to-30 GHz frequency range, the proposed PA delivers relatively high peak output power, power gain, and efficiency, with respective values exceeding 20 dBm/16 dB/33 %. Notably, at 12 dB/9.5 dB/6 dB PBO, the DE maintains superiority over 10 %/15 %/22 % across the same frequency spectrum. The DE primarily drops at 6/9.5 dB PBO due to the lossy C_{ds} of the main PA (see Section 4.7) [114].

The lower DE/PAE at the deep PBO is not an inherent limitation of the proposed architecture. Enhancements can be made through improved design choices to reduce C_{ds} of the main PA, such as:

1. Increase V_{DD}: A higher supply voltage allows the use of smaller devices, reducing C_{ds} and increasing R_{Loss}.

2. Adopt asymmetric Doherty configurations: Asymmetric designs can reduce the main PA's R_{Loss}, which has the greatest impact on back-off efficiency. For example, the PA that turns on first should be the smallest, and the one that turns on last should be the largest in N-way Doherty architectures (refer Fig. 4.24(a)). However, each PA will have a different gain, so the preceding stages will differ and cannot be reused in the design phase.

3. Adopt Doherty configurations that feature early current saturation for their main devices and/or deep PBO peaking devices.

4. Utilize advanced technologies: Technologies such as SOI offer lower parasitics,

Table 4.1
PERFORMANCE SUMMARY AND COMPARISON TO DOHERTY MM-WAVE PAS

Specifications	This Work	Z.Ma ISSCC'22 [98]	X.Zhang RFIC'22 [97]	Mortazavi JSSC'22 [96]	Pashaeifar JSSC'22 [95]	Huang ISSCC'21 [66]	Kim RFIC'21 [93]	Mannem JSSC'21 [84]	Wang ISSCC'19 [64]
Architecture	Balun-first 3-way Parallel Doherty PA	3-way Parallel Series Doherty PA	Coupled-inductor based 3-way Doherty PA	Digital polar series 4-way Doherty PA	2-step impedance inversion series Doherty PA	Continuous Coupler Doherty PA	Parallel-series Doherty PA	Role-exchange Doherty PA	Mixed-signal Doherty PA
PA structure	3-stage PAs	2-stage PAs	2-stage PAs	NA	2-stage PAs	2-stage PAs	2-stage PAs	2-stage PAs	2-stage PAs
Technology	40 nm CMOS	55 nm CMOS	45 nm SOI	40 nm CMOS	40 nm CMOS	45 nm SOI	28 nm CMOS	45 nm SOI	45 nm SOI
Supply (V)	1.1	2.4, 1.2^{+}	1.8, 1	2 V, 1 V	1.8, 0.9	2, 1	0.9, 1.8	2, 1	2, 1
Oper. Freq. (GHz)	24-30	28	38	29.5	24-32	26-60	27	26-60	27
PBO Eff. Enh. BW (GHz)	24-26	28	38	29.5	24-28[a]	26-60[b]	27	26-60[b]	27
Core Area (mm^2)	0.77	0.54	1.4	1.1	0.37	0.62	0.16	0.67	0.37
Gain (dB)	20 (26 GHz)	16.1	15	NA	17.4	15.5*	16.5	16*	19.1
P_{sat} (dBm)	20.7 (26 GHz)	25.5	18.9	18.7	20.4	22	18.8	22.6 (32 GHz)	23.3
DE_{sat}/PAE_{sat} (%)	39/22.3 (26 GHz)	32.5/25.2	31*/23.3	36/24	46*/38.2	NA/40.5	36*/30	46.7/41.9	NA/40.1
DE_{6dB}/PAE_{6dB} (%)	24.7/11.7 (26 GHz)	25.4/20.4	20*/17.1	33/15	39*/34	NA/32.5	26*/22	35.1/31.5	NA/33.1
$DE_{9.5dB}/PAE_{9.5dB}$ (%)	18.1/7 (26 GHz)	21*/17	17*/ 13.7	26*/10*	25*/20*	NA/15*	17*/12*	22*/20*	NA/20*
DE_{12dB}/PAE_{12dB} (%)	11.7/4.2 (26 GHz)	18.2/14.2	15*/10*	22/10	10*/10*	NA/10*	13*/10*	15*/11*	NA/12*
Modulation Scheme	64/64/64/256/1024 QAM OFDM (26 GHz)	64 QAM	64 QAM OFDM	64 QAM OFDM	64 QAM OFDM	64 QAM	64 QAM OFDM	64 QAM (28 GHz)	64 QAM
Data rate (Gb/s)	6/4.8/2.4/1.6/0.5	1.5$^{\#}$	0.6	1.8	2.4	3	4.8	3	6
Modulation BW (MHz)	1000/800/400/200/50	250	100	300	400	500	800	500	1000
EVM_{rms} (dB)	-24.3/-23.5/-24.9/-26.8/-30	-25.2	-25	-27.58	-24.5	-25	-25	-24	-25.3
ACLR (dBc)	-30.1/-29.5/-28.9/-29.9/-36	-27	-26.5*	-27.5	-28.2	-28.8	-25.9	-28.8	-29.6
P_{avg} (dBm)	9.4/9.8/9.4/9.3/8.6	17.7	11.3	7.9	8.8	13.4	11.4	10.7	15.9
PAE_{avg} (%)	15/15/14/13/12 (DE)	17.5	14.7	18	15	24.8	18.1	14.5	29.1 (27.6^{++})
DPD	No	No	No	Yes	No	No	No	No	No

$^{\#}$limited by equipment. *Graphically estimated. $^{+}$Nominal voltage of the technology. $^{++}$Efficiency with digital circuits. ^{a}6 dB PAE>29 %. ^{b}6 dB PBO efficiency wrt class B PA>1.

Table 4.2
COMPARISON OF EFFICIENCY TO LINEAR MM-WAVE PAS

Specifications	This Work	F.Wang JSSC'21 [44]	M.Pashaeifar MWCL'22 [72]	W.Zeng ISSCC'23 [73]
Technology	40 nm CMOS	45 nm SOI CMOS	40 nm CMOS	28 nm CMOS
Supply (V)	1.1	2	1	1.8/0.9
Frequency (GHz)	26	28	28	28
P_{sat} (dBm)	20.7	20.4	20.1	20.3
DE_{sat}/PAE_{sat} (%)	39/22.3	50*/45	40.6/-	34.7/33.6
DE_{6dB}/PAE_{6dB} (%)	24.7/11.7	26*/25*	19*/-	15*/15*
$DE_{9.5dB}/PAE_{9.5dB}$ (%)	18.1/7	16*/15*	11*/-	8*/8*
DE_{12dB}/PAE_{12dB} (%)	11.7/4.2	10*/9*	7*/-	5*/5*

*Graphically estimated.

further improving efficiency.

5. Use low-loss power output combiners.

It manages complex signals with a data rate of 4.8 Gb/s while demonstrating EVM/ACLR of −23.5 dB/−29.5 dBc, respectively. Notably, these achievements are attained without employing any digital pre-distortion, which aligns with state-of-the-art standards and explains our design choice for the linear Doherty configuration.

Table 4.2 compares class B/AB PAs having a similar peak output power and frequency of operation with our proposed 3-way Doherty design. The table reveals that our proposed 3-way Doherty surpasses the other three linear PAs in terms of DE at 9.5 dB PBO. Moreover, at 6 dB PBO compared to references [72, 73], our proposed PA exhibits better performance. However, the PAE is not as competitive as other models.

4.9. SUMMARY

In this chapter, a mm-wave 3-way Doherty PA has been implemented that features an enhanced bandwidth technique to expand its operational bandwidth. A step-by-step design procedure for a balun-first configuration has been thoroughly explained. The proposed PA is fabricated using 40 nm CMOS technology, occupying a core area of 0.77 mm^2.

The realized front-end operating at 26 GHz demonstrates a power gain of 20 dB, a peak power of 20.7 dBm, and a DE of 39 %/24.7 %/18.1 % at PBO levels of 0 dB/6 dB/9.5 dB. It attains an EVM and ACLR of −24.9 dB/−28.9 dBc for a 400 MHz 64-QAM OFDM signal with a P_{avg} of 9.4 dBm and a 14 % average DE. For a 100 MHz 256-QAM OFDM signal, the proposed PA achieves EVM/ACLR of −25.7 dB/−30.5 dBc with a P_{avg}/DE of 10.5 dBm/17 %. These results make it a promising choice for adoption in 5G mm-wave TXs.

However, linear 3-way Doherty PAs achieve similar or lower efficiency compared to 2-way Doherty PAs at 9.5 dB PBO, as observed in the state-of-the-art comparison table (Table 4.1). This limitation is due to the finite QF of the C_{ds}, the channel resistance of the device (particularly in the main PA), its higher load modulation, and the higher passive losses in the output network.

The next chapter discusses different PA architectures, including 2-/3-way Doherty configurations, aimed at achieving higher P_{out} while maintaining efficiency at deep PBO levels.

5

A 4xTwo-Way mm-wave Doherty CMOS PA

This chapter introduces a 4×2-way Doherty PA tailored for mm-wave 5G applications. It incorporates an advanced output combiner that consists of four differential 2-way Doherty networks, two QHCs, and a balun to enhance the P_{out}, improving PBO efficiency. Realized in 40 nm CMOS bulk technology with a core area of 1.54 mm^2, the prototype delivers a saturated power/peak gain surpassing 25.2 dBm/25.5 dB, and it demonstrates a DE exceeding 17.5 %/10 % at 0 dB/6 dB PBO across a 26-to-32 GHz band. The proposed mm-wave PA achieves EVM/ACLR values of -25 dB/-33 dBc for a 2 GHz 64-QAM OFDM signal with 9.6 dB PAPR, operating at a P_{avg} of 11.3 dBm with a DE_{avg} of 4 % without using DPD. For a 50 MHz 1024-QAM OFDM signal with 10 dB PAPR, it achieves a P_{avg}/DE_{avg} of 7.2 dBm/2 % with EVM/ACLR of -35 dB/-42 dBc without DPD.

This chapter is based on the paper accepted in the IEEE Trans. Microw. Theory Tech.[115]

5.1. INTRODUCTION

The millimeter-wave (mm-wave) bands of fifth-generation (5G) networks enable the multi-gigabit per second data rates, high capacity, and low latency necessary for the next generation of digital innovation and connectivity. To achieve these capabilities, 5G networks employ phased array beamforming systems and spectrally efficient modulation schemes like quadrature amplitude modulation (QAM) and orthogonal frequency-division multiplexing (OFDM). These modulation methods, however, result in signals with a high PAPR [3–5, 116]. For instance, the commonly used 64-QAM OFDM has a PAPR of 11 dB if no crest factor reduction is applied, necessitating power amplifiers (PAs) to be efficient both at peak power and at 11 dB PBO.

Key requirements for mm-wave front-end design include:

- High P_{sat}: Typically around 24-25 dBm for handsets and access points.
- Efficiency at peak and deep PBO: To improve the average efficiency [10, 11].
- Wide operational bandwidth to cover the 24-to-30 GHz band.
- Large modulation bandwidth (up to 1.4 GHz): To fully leverage the mm-wave spectrum.
- High and flat gain: To compensate for signal losses in preceding stages, such as power splitters, phase shifters, and mixers [18, 117]. Gain flatness can also impact over-the-air performance, such as the coverage area at certain frequencies, and can introduce frequency-dependent distortion and intermodulation distortion.
- Linearity: With stringent error vector magnitude (EVM) requirements, such as −25/−30 dB for 64/256-QAM [10, 11].
- VSWR resilience: Ensuring compatibility with phased array systems [117].

Nanoscale complementary metal-oxide-semiconductor (CMOS) technologies are being investigated for 5G mm-wave TXs because of their high integration, cost-effectiveness, compact size, and efficiency. However, these technologies face challenges such as limited supply voltage, which makes it difficult to achieve the desired P_{sat}. Furthermore, $R_{opt} = \frac{V_{DD}^2}{2P_{sat}}$ cannot be significantly reduced because it still needs to match the impedance of the 50 Ω antenna. This limitation raises the QF requirements of the output match and restricts the operational bandwidth.

Although recent new power combiner topologies satisfy 5G requirements for output power (P_{out}), EVM, and adjacent channel leakage ratio (ACLR), improving average efficiency is still a daunting task [71, 117–120]. The N-way Doherty amplifier is well regarded for delivering high P_{out} and enhancing average efficiency for signals with high PAPR. Among the N-way Doherty configurations, the 2-way [21, 64–66, 84, 88–90, 92–95], 3-way [97, 98, 101], and 4-way Doherty amplifiers [96, 121] are commonly used. However, as noted in reference [87], increasing the number of Doherty stages not only allows one to boost P_{sat}, but unfortunately also adds two inductors and capacitors to the

output network for each additional stage in a linear Doherty PA. These additional components raise passive losses more than conventional combiners, often reducing P_{sat} in practice.

Furthermore, the DE_{avg} shows little improvement for the N-way Doherties beyond the 3-way Doherty configuration for signals with a PAPR of 11 dB. Moreover, the impedance of the main PA in symmetrical N-way linear Doherty designs varies from R_{opt} to N*R_{opt}, which decreases the operational bandwidth due to the higher QF requirement. Efficiency improvements at deep PBO are also limited by the finite channel resistance of the CMOS PAs [102, 114]. Thus, increasing beyond 2-/3-way Doherty configurations does not significantly enhance average efficiency due to the increased losses in these technologies.

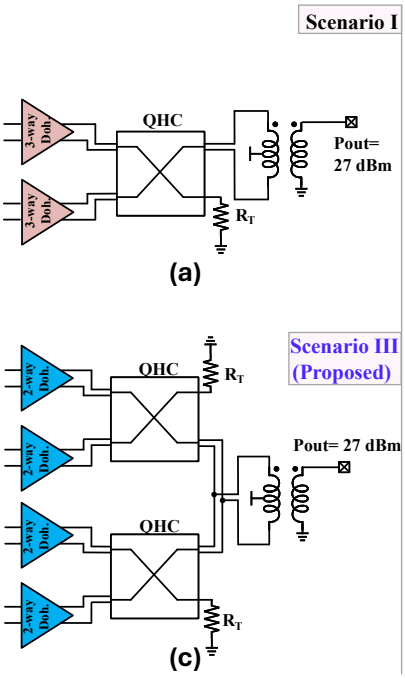
As an alternative approach, this chapter proposes a novel 4 × 2-way Doherty PA that meets the key design requirements outlined earlier, specifically achieving high output power by combining a 4-way power combiner with a 2-way Doherty architecture. In this work, we thoroughly analyze the benefits of the proposed front-end in terms of delivered output power, efficiency, bandwidth, linearity, and VSWR performance. The proposed output network enhances efficiency at PBO, linearity, wide operational bandwidth, and large modulation bandwidth, as the 2-way Doherty network exhibits a lower impedance transformation compared to higher-order symmetrical Doherty networks and requires less complicated adaptive biasing circuitry. Furthermore, the proposed combiner comprises two quadrature hybrid couplers (QHCs), which improve the PA's resilience to VSWR variations.

This chapter covers the following topics: Section 5.2 analyzes various power combiner topologies, and Section 5.3 compares the performance of 2-/3-way Doherty in terms of output power, efficiency, linearity, and VSWR resilience. Section 5.4 details the design methodology for a compact power combiner that integrates four 2-way Doherty amplifiers, two quadrature hybrid couplers (QHCs), and a balun. Section 5.5 explores the circuit implementation of the proposed 4×2-way Doherty PA prototype, which is fabricated using 40 nm bulk CMOS technology. Experimental results are presented in Section 5.6, and a comparison with the state-of-the-art is conducted in Section 5.7; the paper concludes in Section 5.8.

5.2. POWER COMBINER VARIANTS

To meet the handset and access point requirements of the 5G standard, a P_{sat} of 24-25 dBm is necessary. Assuming an output network loss of 2-3 dB, the ideal P_{sat} should reach approximately 27 dBm (0.5 W). Achieving this output power requires an N-way power combiner paired with an N-way Doherty network, as 6–8 devices are typically needed to generate 27 dBm using CMOS 40 nm technology. Moreover, as discussed, the PA must support OFDM signals with high PAPR (≈ 9-12 dB), while operating under load mismatch conditions of up to VSWR 3 : 1.

One approach involves increasing the complexity of the Doherty network while reducing the order of the power combiner to achieve a PAE peaking at ≈ 12 dB PBO. The second approach prioritizes minimizing complexity, thereby improving overall PAE by reducing the output matching network's loss. Based on this trade-off, integrating the power com-



Parameters	Scenario I	Scenario II	Scenario III
Number of combining stages	2	3	3
Stage 1	Two 3-way Doherty	Four 2-way Doherty	Four 2-way Doherty
Stage 2	One QHC	Two QHCs	Two QHCs
Stage 3	-	Non-isolated power combining	One QHC
Balun	Yes	Yes	Yes
Output power per Doherty (dBm)	24	21	21

(d)

Fig. 5.1. (a) Scenario I: a 3-way Doherty and 2-way combiner using one QHC, (b) Scenario II: a 2-way Doherty and 4-way combiner using three QHCs, (c) Scenario III (proposed): a 2-way Doherty and 4-way combiner using two QHCs, and (d) comparison between three scenarios.

biner with 2-/3-way Doherty architectures is the most effective approach, achieving an optimal balance between P_{sat}, average efficiency, and wide bandwidth. There are three possible configurations for combining the power combiner and Doherty network:

- Scenario I: Two 3-way Doherty amplifiers using a QHC combiner (Fig. 5.1(a))

  In this design, the power combiner uses a single QHC to combine the power from two 3-way Doherty PAs. Each 3-way Doherty PA's output network includes either three TLs or, for a high-pass (HP) model, four inductors and three capacitors. Here, the P_{sat} for each 3-way Doherty and PA is 24 dBm and 19.2 dBm, respectively.

- Scenario II: Four 2-way Doherty amplifiers using three QHCs as a power combiner (Fig. 5.1(b))

  This design uses three QHCs in the related power combiner, combining the output from four 2-way Doherty PAs. Each 2-way Doherty PA output network consists of one TL or, for an HP model, two inductors and one capacitor. The P_{sat} for each 2-way Doherty and PA is 21 dBm and 18 dBm, respectively.

- Scenario III (proposed): Four 2-way Doherty amplifiers using two QHCs as a power combiner (Fig. 5.1(c)).

The 4-way power combiner in this design uses a combination of isolated power combining (with two QHCs) and non-isolated power combining in the current domain, which merges the power from the four 2-way Doherty PAs. As with Scenario II, each 2-way Doherty achieves a P_{sat} of 21 dBm.

All three scenarios can be classified as balanced PAs due to the inclusion of QHCs at the output. Balanced PAs improve the PA's resilience to VSWR, as highlighted in [95, 117]. Additionally, a symmetrical N-way Doherty design employs equally sized devices, simplifying the design process and allowing the same chain to be reused for each individual PA within the Doherty configuration. The following section provides a comparison of 2-way and 3-way Doherty configurations in terms of P_{out}, DE, bandwidth, and VSWR, considering their losses in the output network.

5.3. 2-WAY DOHERTY VERSUS 3-WAY DOHERTY

In Fig. 5.2(a)/(b), the schematics for 2-way and 3-way Doherty amplifiers with TLs or lumped components are illustrated. The HP model for the TL is selected due to its integration of shunt inductors that function as a dc feed and naturally convert it into a differential circuit. The figure highlights the device's C_{ds}. In reality, the device includes channel resistance, and C_{ds} has a finite QF, which can be represented by R_{Loss}. These elements, C_{ds} and R_{Loss}, are shown in Fig. 5.2(a)/(b) in red [102, 114]. Ideally, R_{Loss} should be infinite. To achieve the ideal P_{sat} of 27 dBm, each PA in a symmetric 3-way Doherty configuration needs to generate 19.2 dBm[1] (Scenario I), whereas each PA in a symmetric 2-way Doherty configuration should generate 18 dBm[2] (Scenario II and III). This implies that the devices used in the 3-way Doherty are bigger, resulting in a larger C_{ds} and lower R_{Loss} than the 2-way Doherty.

5.3.1. OUTPUT POWER & EFFICIENCY COMPARISON

All simulations in Fig. 5.3(a)/(b)/(c) were conducted with an ideal PA model, and the QF of the capacitors and inductors was set to 25/15, respectively. It is observed that after incorporating the QF into the output network and considering finite R_{Loss}, the 2-way Doherty performs better than the 3-way Doherty, even at PBOs of 9.5 dB and 12 dB (Fig. 5.3(a)). Besides, as QF of the network components decreases, the output network losses increase, reducing both peak output power and efficiency at peak and PBO. The impact of QF degradation is more pronounced in the 3-way Doherty architecture due to its higher component count and higher load modulation of the main PA. The P_{sat} and DE_{sat} are lower for the 3-way Doherty due to higher passive losses in the output network, which has more lumped components than the 2-way Doherty.

At deep PBO, the main PA in the 3-way Doherty experiences an impedance $R_{Loss}||3R_{opt}$ while in the 2-way Doherty, the main PA sees $R_{Loss}||2R_{opt}$. Since the main PA in the 3-way

[1] Each single-ended (SE) PA must generate 16.2 dBm. Thus, a push-pull configuration generates 19.2 dBm. Subsequently, one bank of 3-way Doherty generates 24 dBm, and 2 × 3-way Doherty eventually delivers 27 dBm.

[2] Each SE PA must generate 15 dBm. Thus, a push-pull configuration generates 18 dBm. Subsequently, one bank of 2-way Doherty generates 21 dBm, and 4 × 2-way Doherty eventually delivers 27 dBm.

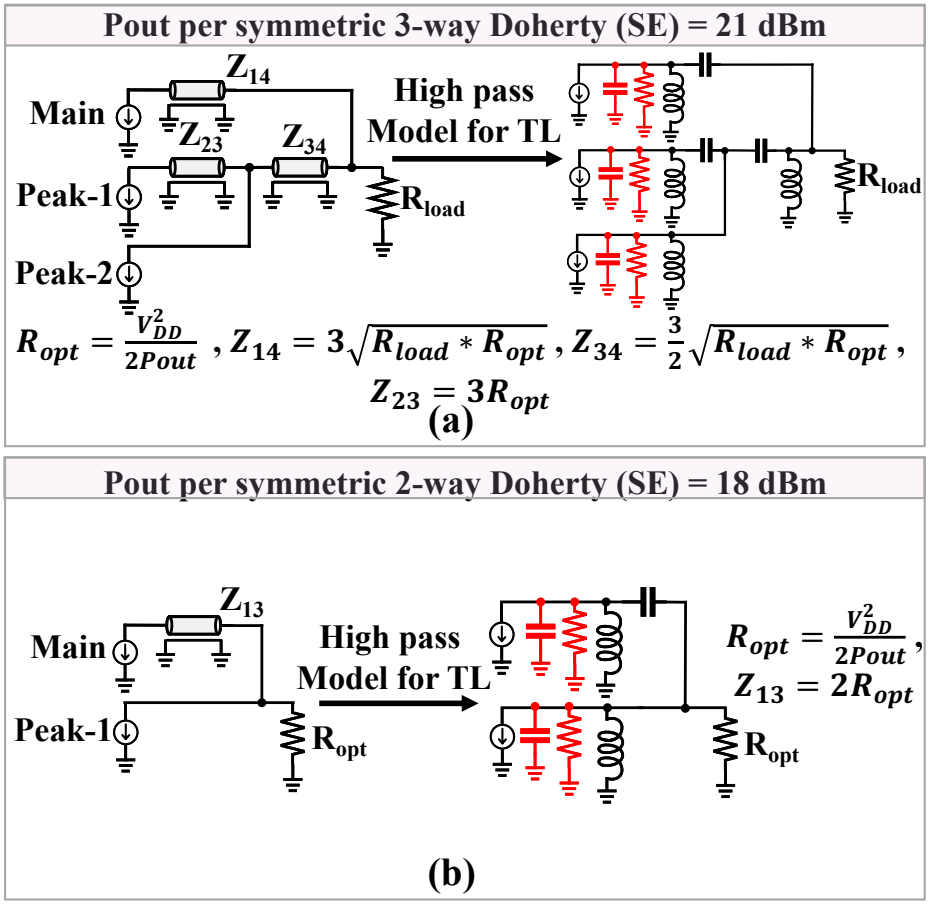


Fig. 5.2. (a) Schematics of 3-way Doherty PA, and (b) 2-way Doherty PA.

Doherty requires a greater impedance transformation (to $3R_{opt}$) at deep PBO compared to 2-way Doherty, its DE peak at 9.5 dB significantly reduced, making it more susceptible to R_{Loss} (refer to Fig. 5.3(d)). This suggests that linear N-way Doherty configurations may not achieve the desired DE peak at deep PBO due to the higher impedance transformation required. Efficiency improvements at deep PBO could be realized through:

1. Asymmetric Doherty designs, which employ a smaller main PA to improve efficiency at deep PBO.
2. Higher supply voltages, allowing the use of smaller devices with larger R_{Loss}.
3. Advances in technology to reduce C_{ds} and have better quality factors.
4. Use of the Doherty configuration that features early current saturation in PBO for the main and/or the peak devices.

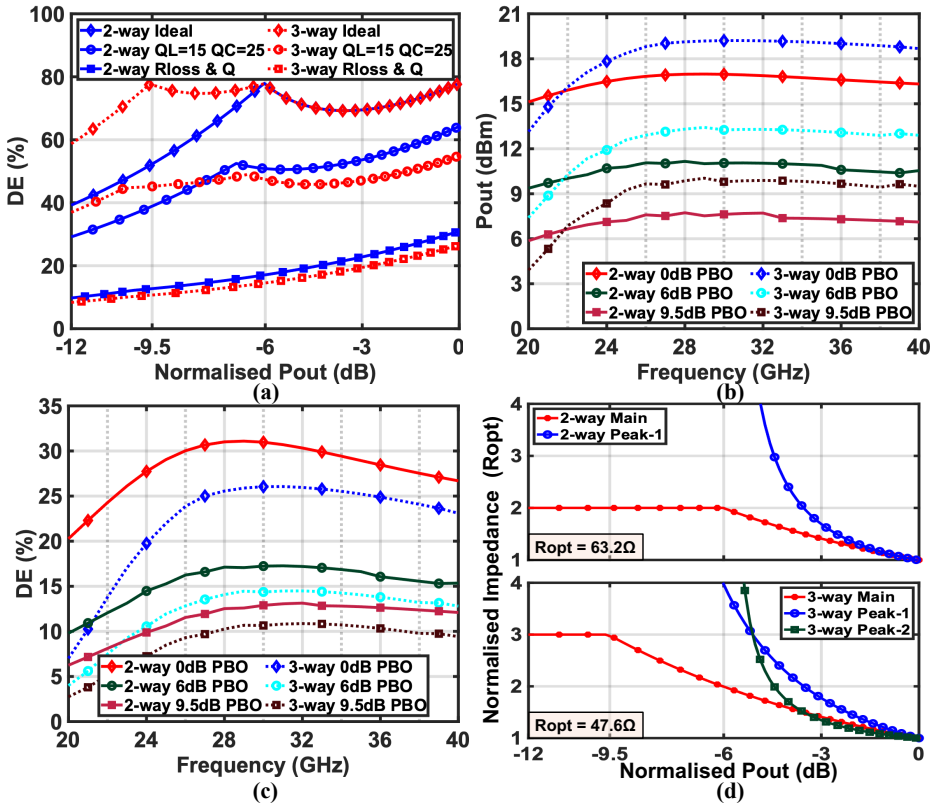


Fig. 5.3. (a) DE versus normalised P_{out} at 30 GHz for symmetric 2-/3-way Doherty for three cases (ideal, with QF of 15 for inductor and 25 for capacitor, with finite R_{Loss}), (b) DE, (c) P_{out} versus frequency for symmetric SE 2-/ 3-way Doherty with $Q_L = 15$, $Q_C = 25$, and finite R_{Loss}, and (d) normalised impedance versus normalised P_{out} at 30 GHz for symmetric 2-/3-way Doherty.

Fig. 5.3(b)/(c) presents the DE and P_{out} versus frequency for symmetric 2-way and 3-way Doherty configurations with finite R_{Loss} and a QF of 15/25 for inductors and capacitors, respectively. In terms of bandwidth for DE and P_{out}, the 2-way Doherty outperforms the 3-way Doherty. It is also noted that while the 3-way Doherty produces higher P_{out}, despite higher passive losses, this is because it is designed for a single-ended (SE) P_{out} of 21 dBm, whereas the 2-way Doherty is designed for 18 dBm.

Fig. 5.3(d) illustrates the normalised drain impedance for the main and peak-1 PAs in a symmetric 2-way Doherty configuration, as well as the normalised drain impedance for the main, peak-1, and peak-2 PAs in a symmetric 3-way Doherty configuration. These simulations employ ideal PAs and output networks, with the impedance normalized to the R_{opt} required to achieve the desired P_{sat}. Notably, R_{opt} differs between the 2-way and 3-way Doherty configurations, as they are designed to generate 18 dBm and 21 dBm, respectively.

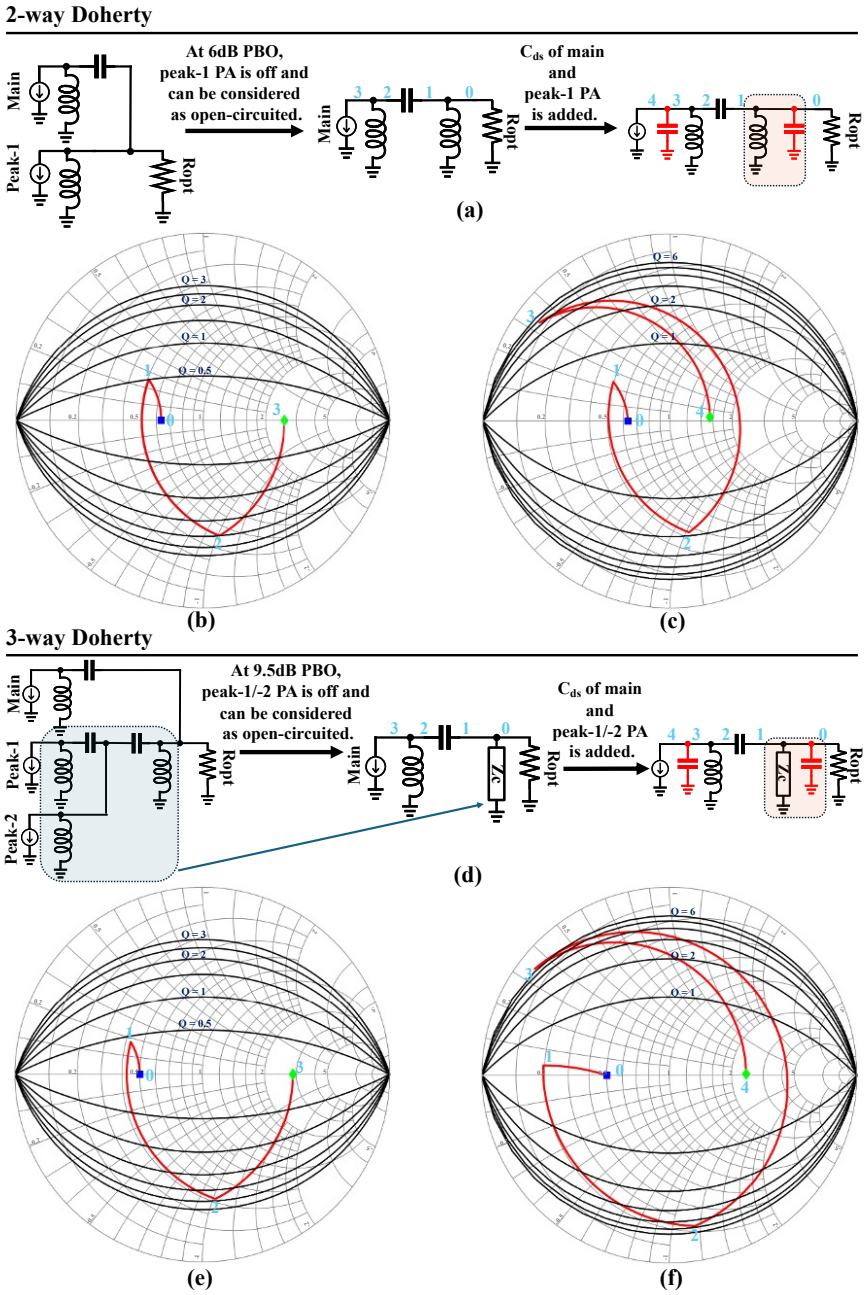


Fig. 5.4. (a) Schematic of a 2-way Doherty at deep PBO, (b) Smith chart illustrating the impedance trajectory of the main PA in the 2-way Doherty with ideal lumped components, and (c) with a QF of 15/25 for inductors/capacitors and parasitic C_{ds}, (d) Schematic of a 3-way Doherty at deep PBO, (e) Smith chart showing the impedance trajectory of the main PA in the 3-way Doherty with ideal lumped components, and (f) with a QF of 15/25 for inductors/capacitors and parasitic C_{ds}.

5.3.2. BANDWIDTH COMPARISON

At 6 dB PBO, the peak-1 PA in the 2-way Doherty is inactive and can be approximated as open-circuited, leaving only the main PA active, as shown in the schematic in Fig. 5.4(a). The impedance at each node is calculated and plotted on the Smith chart (Fig. 5.4(b)) to visualize the main PA's impedance trajectory, which remains within a Q circle of 2. Similarly, at a deep PBO of 9.5 dB, both peak-1 and peak-2 PAs in the 3-way Doherty are inactive, with only the main PA active, as illustrated in Fig. 5.4(d). Fig. 5.4(e) shows the impedance trajectory of the main PA with ideal lumped components, which stays within a Q circle of 2.5. The 3-way Doherty demands a higher QF due to the larger impedance transformation ($3R_{opt}$) at deep PBO, thereby limiting the operational bandwidth compared to the 2-way Doherty as explained by $Q = \frac{f_0}{BW}$. This bandwidth limitation of the 3-way Doherty is also apparent in the DE and P_{out} versus frequency plots (Fig. 5.3(b)/(c)).

When a QF of 15/25 is introduced for the inductors/capacitors and parasitic C_{ds} in the 2-/3-way Doherty configurations, the impedance trajectory shifts, as seen in Fig. 5.4(c)/(f). This reduces the drain impedance of the main PA, extending the trajectory beyond a Q circle of 4 and 6 for the 2-/3-way Doherty configurations, respectively, which further limits the operational bandwidth. The loaded QF (Q_L) at each node can be calculated using $QF = \frac{\Im(Y)}{\Re(Y)}$. Additionally, for a given unloaded network quality factor Q_N and loaded network quality factor Q_L , the insertion loss (IL) can be determined as follows [122]:

$$IL = 10\log\left(\frac{1}{1+\frac{Q_L}{Q_N}}\right) \tag{5.1}$$

For steps 0 and 1, Q_N is equal to Q_{ind}; for other steps Q_N can be approximated as $Q_{ind}||Q_{cap}$ for easier calculation. The total approximate IL for the 2-/3-way Doherty networks is 2.6 dB and 4.2 dB, respectively.

The Q analysis clearly demonstrates that the 2-way Doherty amplifier has a wider operational bandwidth, requiring a smaller impedance transformation and a lower QF compared to the 3-way Doherty. It also has a lower IL due to the reduced number of lumped components.

5.3.3. LINEARITY COMPARISON

A theoretical amplitude-to-phase (AM-PM) analysis is performed on a 2-way parallel Doherty, which is illustrated in Fig. 5.5(a) [123]. The analysis focuses on the main PA, as it primarily determines the linearity of the Doherty PA. Fig. 5.5(b) presents a metal-oxide-semiconductor field-effect transistor (MOSFET) model comprising a voltage-controlled current source ($g_m V_g$), capacitors (gate-source capacitance (C_{gs}), drain-source capacitance (C_{ds}), and gate-drain capacitance (C_{gd})), and a gate resistance (r_g). The admittance Y_{main} represents the output load of the main PA (5.2).

$$Y_{main} = G_{main} + jB_{main}, \quad G_{main} = \frac{1}{R_{main}}, \quad B_{main} = \frac{1}{X_{main}} \tag{5.2}$$

The gate of the transistor is connected to a voltage source (V_S) with an internal impedance of $Z_S = R_S + jX_S$. Applying Miller's theorem to the feedback capacitor (C_{gd}) using (5.3)

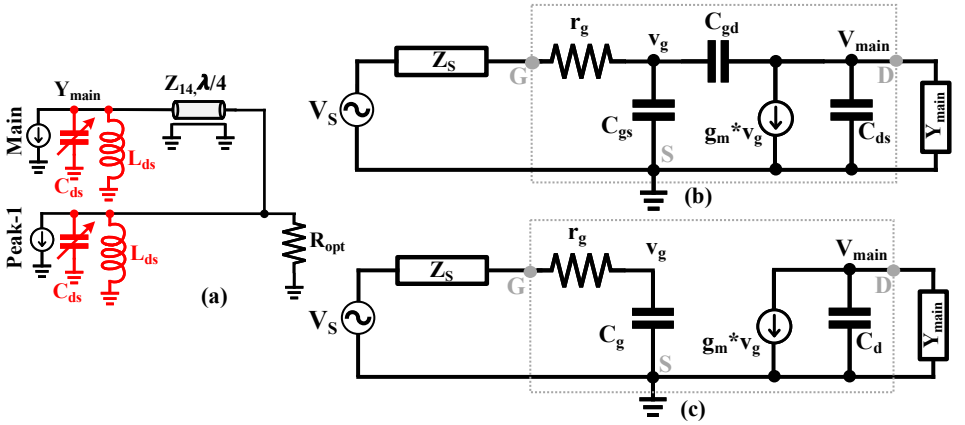


Fig. 5.5. (a) 2-way parallel Doherty, (b) schematic model of the MOSFET device, and (c) MOSFET equivalent circuit after applying Miller's theorem to C_{gd}.

5

yields the equivalent schematic shown in Fig. 5.5(c).

$$\begin{aligned} C_g &= C_{gs} + C_{gd}\left(1 + g_m R_{main}\right) \\ C_d &= C_{ds} + C_{gd}\left(1 + \frac{1}{g_m R_{main}}\right) \end{aligned} \tag{5.3}$$

For simplification, several assumptions are made.

- Maximising P_{out} and DE of the PA: The load at the drain of the transistor must be purely resistive, which implies $B_{main} = \omega C_{ds}$.
- High voltage gain in the PA: The voltage gain satisfies $g_m R_{main} >> 1$, and C_{ds} is is assumed larger than C_{gd}. Under these conditions, (5.3) simplifies to (5.4).

$$\begin{aligned} C_g &\approx C_{gs} + C_{gd}\left(g_m R_{main}\right) \\ C_d &\approx C_{ds} + C_{gd} \approx C_{ds} \end{aligned} \tag{5.4}$$

Using the schematics in Fig. 5.5(c), the gate voltage (V_g) and the voltage at the drain of the main PA (V_{main}) are computed using (5.5) and (5.6) respectively.

$$V_g = \frac{-jV_s}{-j + (C_{gd} g_m R_{main} + C_{gs})(jX_s + R_s + r_g)\omega} \tag{5.5}$$

$$V_{main} = \frac{-V_s g_m R_{main}}{\left(\left(X_s - \frac{1}{\omega(C_{gd} g_m R_{main} + C_{gs})}\right)^2 + (R_s + r_g)^2\right)\omega(C_{gd} g_m R_{main} + C_{gs})} \cdot \left[Xs - \frac{1}{\omega(C_{gd} g_m R_{main} + Cgs)} + j(R_s + r_g)\right] \tag{5.6}$$

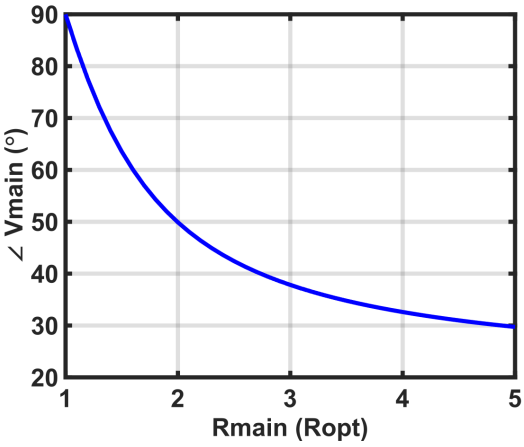


Fig. 5.6. Phase of V_{main} versus R_{main} normalized to R_{opt}=10 Ω at 30 GHz.

The phase of V_{main} is given below:

$$\angle V_{main} = \tan^{-1}\left(\frac{R_s + r_g}{X_s - \frac{1}{\omega(C_{gd} g_m R_{main} + C_{gs})}}\right) \tag{5.7}$$

From (5.7), it is evident that the phase of the V_{main} ($\angle V_{main}$) depends on the transistor's parameters (C_{gs}, C_{gd}, g_m, and r_g) as well as the output impedance presented to the drain of the main PA (R_{main}).

To examine the influence of R_{main}, $\angle V_{main}$ is plotted against R_{main}, normalized to R_{opt} for 40 nm CMOS bulk transistor, as shown in Fig. 5.6. The simulation of nmos transistor with width = 400 µm yields the following parameters: C_{gs} = 129 fF, C_{gd} = 80 fF, r_g = 8 Ω, g_m = 130 mS, R_{opt} = 10 Ω and frequency = 30 GHz. R_s is assumed to be 0. The denominator of (5.7) becomes zero when X_s is calculated as:

$$X_s = \frac{1}{\omega(C_{gd} g_m R_{main} + C_{gs})} \tag{5.8}$$

X_s can only be zero at a specific value of R_{main}. Here, R_{main} = 10 Ω is selected as it represents R_{opt} required for 2-way symmetrical Doherty to generate 22 dBm. As shown in Fig. 5.6, the phase of V_{main} changes by 40 ° when R_{main} varies from R_{opt} to $2R_{opt}$.

In a 2-way symmetrical Doherty configuration, the impedance presented to the main PA varies from R_{opt} to $2R_{opt}$ to enhance efficiency at PBO as shown in Fig. 5.3(d). This variation in R_{main} leads to fluctuations in $\angle V_{main}$. Additionally, in a real device, the parameters g_m, C_{gd}, and C_{gs} depend on the gate's input voltage and are inherently nonlinear. Consequently, the load modulation amplifies these nonlinearities, increasing the overall nonlinearity of the Doherty PA. Equation (5.7) also highlights that if C_{gd} did not exist, the AM-PM dependence on R_{main} could be eliminated. However, this is not feasible in practical transistors. Additionally, R_s and X_s can be adjusted to control AM-PM distortion.

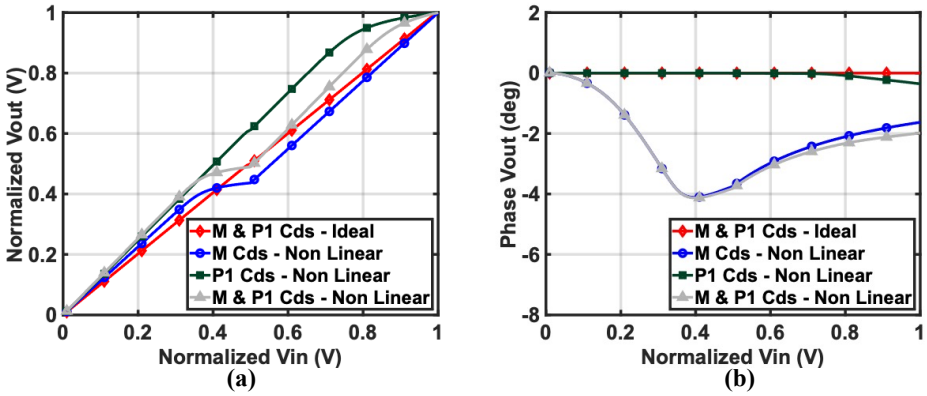


Fig. 5.7. (a) Amplitude-to-amplitude (AM-AM), and (b) AM-PM of 2-way Doherty with and without nonlinear C_{ds} for the main and peak-1 PAs.

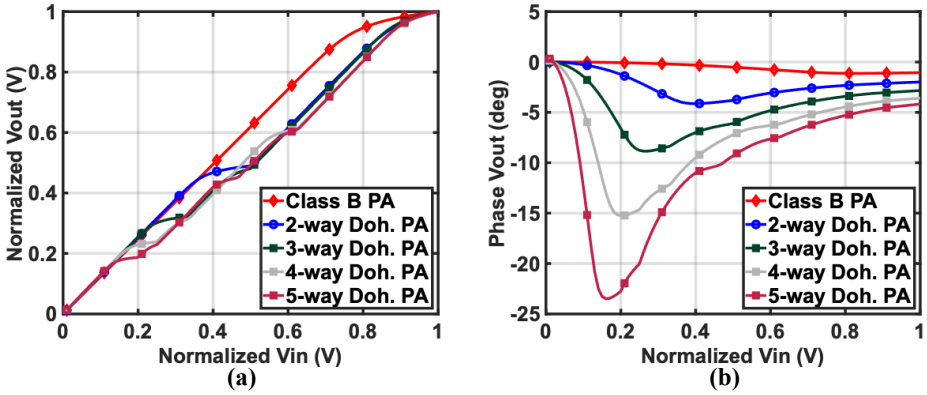


Fig. 5.8. (a) Amplitude-to-amplitude (AM-AM), and (b) AM-PM of N-way Doherty PA and standalone class B PA.

For an N-way symmetrical Doherty PA ($N \geq 3$), the impedance at the main PA's drain varies from R_{opt} to $N \cdot R_{opt}$, as illustrated in Fig. 4.25. Consequently, higher-order N-way Doherty PAs experience greater phase variations at the main PA drain, which makes them increasingly nonlinear as N increases, as described by (5.7).

In Fig. 5.5(a), a nonlinear C_{ds} and L_{ds} (the inductor used for resonating out the C_{ds}) are introduced at the drains of both the main and peak-1 PAs. Fig. 5.7 illustrates the amplitude-to-amplitude (AM-AM) and AM-PM characteristics when the nonlinear C_{ds} is added to the main PA, the peak-1 PA, or both. The results show that most AM-AM and AM-PM distortions originate from the main PA's nonlinear C_{ds}, as it is always active. The impact of nonlinear C_{ds} of the peak-1 PA is noticeable only near saturation power.

Similarly, nonlinear C_{ds} and L_{ds} are added for 3-way Doherty (Fig. 3.3(c)), 4-way Do-

herty (Fig. 3.5(d)), and 5-way Doherty (Fig. 3.7(e)) configurations. Fig. 5.8 compares the AM-AM and AM-PM characteristics of a single PA and N-way Doherty PAs with nonlinear C_{ds}, assuming ideal output network and devices. All configurations, including the standalone class B PA, generate 22 dBm. From Fig. 5.8, it is evident that AM-PM distortion contributes more significantly to nonlinearity than AM-AM distortion for N-way Doherty PAs. Moreover, the AM-PM distortion increases with higher order N-way Doherty PAs, consistent with the behavior predicted by (5.7).

The AM-AM and AM-PM transfer characteristics of the class B PA and N-way Doherty PAs are used to calculate the EVM when a 500 MHz 64-QAM signal is transmitted, in order to understand the individual and combined effects of AM-AM and AM-PM distortions. This analysis is carried out in Appendix C.1, where three cases are considered:

1. Ideal AM-AM and non-ideal AM-PM,

2. Ideal AM-PM and non-ideal AM-AM,

3. Non-ideal AM-AM and non-ideal AM-PM.

The conclusions from this study are summarized as follows:

1. AM-PM Only: EVM degrades as we move from the class B PA to higher-order Doherty PAs due to larger impedance transformation.

2. AM-AM Only: EVM also degrades when transitioning from the class B PA to Doherty PAs. However, within the Doherty configurations, higher-order Doherty shows better EVM performance than lower-order ones due to smoother AM-AM curves.

3. AM-AM and AM-PM Together: When both distortions are considered, the class B PA performs best, followed by lower-order Doherty configurations. This indicates that AM–PM distortion contributes more significantly to nonlinearity than AM–AM distortion.

In Appendix C.2, the analysis is extended using real CMOS transistors instead of ideal devices. The results confirm the earlier observation that AM-PM distortion worsens with increasing Doherty order. This behavior is more pronounced in real transistors because device parameters such as transconductance (g_m), gate-drain capacitance (C_{gd}), and gate-source capacitance (C_{gs}) vary nonlinearly with the gate input voltage. These inherent nonlinearities are further amplified by load modulation in Doherty architectures, resulting in increased overall distortion. Consequently, AM-PM degradation is significantly higher when using real transistors compared to idealized models that only include nonlinear C_{ds}.

In conclusion, AM-PM distortion is a major contributor to the nonlinearity of Doherty PAs, primarily due to load modulation, especially when compared to traditional class B/AB PAs. Higher-order N-way Doherty PAs exhibit greater nonlinearity due to larger impedance transformations.

5.3.4. VSWR Resilience Comparison

Fig. 5.9 shows the schematics of 2-/3-way Doherty PAs, along with the formula for calculating the voltage across the main PA (v_M). Consider the schematic shown in Fig. 5.9(b). Since a $\lambda/4$ TL is used, the current and voltage on either side of the TL can be related as below.

$$\begin{bmatrix} v_M \\ i_M \end{bmatrix} = \begin{bmatrix} 0 & jZ_0 \\ \frac{j}{Z_0} & 0 \end{bmatrix} \begin{bmatrix} v'_M \\ i'_M \end{bmatrix} \tag{5.9}$$

$$\begin{aligned} v_M &= jZ_0 i'_M \\ i_M &= \frac{j v'_M}{Z_0} \end{aligned} \tag{5.10}$$

In this regard, let's consider the main and peak PAs as ideal current sources. Here, the combination of the main current source and $\lambda/4$ impedance inverter operates as a voltage source. Since the output impedance of the voltage source is zero and is in parallel with the load, i_P does not contribute to the output current. Thus, the load's voltage and current relationships are as follows:

$$\begin{aligned} v'_M &= i_L R_L \\ i'_M &= i_L - i_P \end{aligned} \tag{5.11}$$

Using equations (5.9) and (5.11), we can calculate the magnitude of v_M as shown below:

$$|v_M| = \frac{i_M Z_0^2}{R_L} - i_P Z_0 \tag{5.12}$$

Similar to the 2-way Doherty, we can calculate the voltage of the main PA (v_M) for the 3-way Doherty as shown below:

$$|v_M| = \frac{i_M Z_{14}^2}{R_L} - \frac{i_{P1} Z_{14} Z_{23}}{Z_{34}} \tag{5.13}$$

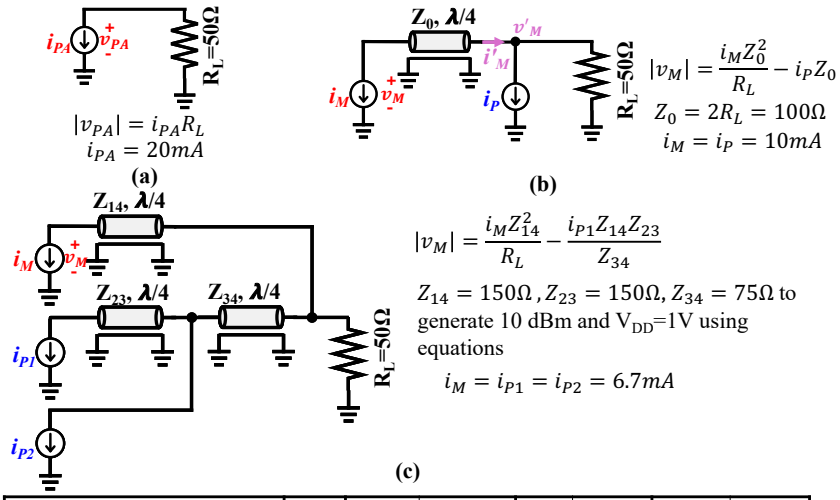
It is evident from (5.12) and (5.13) that one term is load-dependent, while the other is load-independent, unlike in a class-B PA where $v_{PA} = i_{PA} R_L$. Note that at 6 dB PBO, (5.12) and (5.13) become

$$|v_{M6dB}| = \frac{i_M Z_0^2}{2R_L} \quad \text{and} \quad |v_{M6dB}| = \frac{i_M Z_{14}^2}{2R_L} - \frac{i_{P1} Z_{14} Z_{23}}{4Z_{34}}. \tag{5.14}$$

Similarly, at 9.5 dB PBO, (5.12) and (5.13) become

$$|v_{M9p5dB}| = \frac{i_M Z_0^2}{3R_L} \quad \text{and} \quad |v_{M9p5dB}| = \frac{i_M Z_{14}^2}{3R_L}. \tag{5.15}$$

Let's consider the peak currents of the main PA (i_M) and peak PA (i_p) are given as 10 mA, ensuring an output power of 10 dBm with a V_{DD} of 1 V and a load impedance (R_L) of 50 Ω. The table in Fig. 5.9(d) shows the values of v_M at peak P_{out} for different VSWR cases.



VSWR		1	1.5∠0	1.5∠180	2∠0	2∠180	3∠0	3∠180
$R_L(\Omega)$		50	75	33.3	100	25	150	16.7
Class-B	v_M at peak (V)	1	1.5	0.67	2	0.5	3	0.33
2-way Doherty		1	0.33	2	0	3	−0.33	5
3-way Doherty		1	0	2.5	−0.5	4	−1	7
Class-B	v_M at 6dB PBO (V)	0.5	0.75	0.33	1	0.25	1.5	0.17
2-way Doherty		1	0.67	1.5	0.5	2	0.33	3
3-way Doherty		1	0.5	1.75	0.25	2.5	0	4
Class-B	v_M at 9.5dB PBO (V)	0.33	0.5	0.22	0.67	0.17	1	0.11
2-way Doherty		0.67	0.44	1	0.33	1.33	0.22	2
3-way Doherty		1	0.67	1.5	0.5	2	0.33	3

(d)

Fig. 5.9. (a) Class-B PA, (b) 2-way Doherty, (c) 3-way Doherty, and (d) voltage of the main PA across VSWR for all cases.

At VSWR = 2∠0°, v_m is zero. This implies that an ideal symmetrical 2-way Doherty PA with 6 dB PBO efficiency enhancement cannot operate under a VSWR greater than 2. Fig. 5.9(c) illustrates a symmetric 3-way Doherty that generates 10 dBm with a 1 V supply and R_L = 50 Ω. The Z_0 of the TLs is calculated using the formula shown in Fig. 5.2(a). Similarly, for a 3-way Doherty PA, v_M is 0 for VSWR of 1.5∠0°. Thus, 3-way Doherty cannot work under a VSWR greater than 1.5.

At peak output, the currents of each amplifier in a symmetric 2-way Doherty amplifier are equal, and the boundary condition for $v_M = 0$ is given by $R_L < Z_0 = 100\Omega$ when driving an optimum load of 50 Ω. Similarly, for a 3-way Doherty amplifier, the boundary condition for $v_M = 0$ is given by $R_L < \frac{3}{2}R_{load} = 75\Omega$ when driving an optimum load of 50 Ω.

Moreover, it is seen that the reliability of a Doherty PA is more sensitive to the load

Table 5.1
Recap of Section 5.3

Parameters	3-way Doherty	2-way Doherty
Output network (ON)	Consist of 4 inductors and 2 capacitors	Consist of 2 inductors and 1 capacitor
Insertion loss (IL) (dB)	4.2	2.6
Psat with lossy ON	3-way Doherty has more loss than 2-way Doherty when lossy ON is considered	
Impedance transformation for main PA	$3R_{opt}$ to R_{opt}	$2R_{opt}$ to R_{opt}
Efficiency at PBO	Higher degradation in PBO efficiency for linear 3-way Doherty when R_{Loss} is considered (reason - larger impedance transformation)	
Bandwidth	Linear 3-way Doherty is narrow band (reason - higher Q requirement)	
Linearity	3-way Doherty has a larger AM-PM variation (reason - larger impedance transformation)	
VSWR resilience	3-way Doherty can't handle beyond VSWR of 1.5	2-way Doherty can't handle beyond VSWR of 2

impedance variation, and it increases as the Doherty order increases. In terms of VSWR resilience, the 2-way Doherty amplifier demonstrates superior performance and lesser reliability issues compared to the 3-way Doherty.

Furthermore, from the table in Fig. 5.9(d), it is evident that the behavior of the 3-way Doherty at 6 dB PBO is similar to that of the 2-way Doherty at 0 dB PBO. Likewise, the 2-way Doherty at 6 dB PBO and the 3-way Doherty at 9.5 dB PBO behave like a class-B PA. This can significantly affect the performance when operating with high PAPR signals.

This section concludes that the 2-way Doherty amplifier is a more suitable candidate than the 3-way Doherty amplifier, owing to its lower passive losses, wider bandwidth, improved linearity, and superior VSWR resilience, as summarized in Table 5.1.

5.4. Proposed 4xTwo-way Doherty Power Combiner

The proposed power combiner, illustrated in Fig. 5.1(c), employs the 2-way Doherty amplifier due to its lower passive losses, wider bandwidth, better linearity, and superior VSWR resilience compared to the 3-way Doherty configuration. The architecture integrates three types of power combining: (i) Doherty, (ii) isolated power combining using QHCs, and (iii) non-isolated power combining.

While non-isolated power combining could be replaced with QHC-based isolated combining, such a substitution would increase losses, as shown in Fig. 5.1(b). At mm-wave frequencies, simulations indicate that each QHC incurs a loss of 0.4–0.5 dB, depending on the metal stack used [21, 117, 124]. Moreover, adding an additional QHC in the third-

stage power combining does not significantly enhance VSWR resilience.

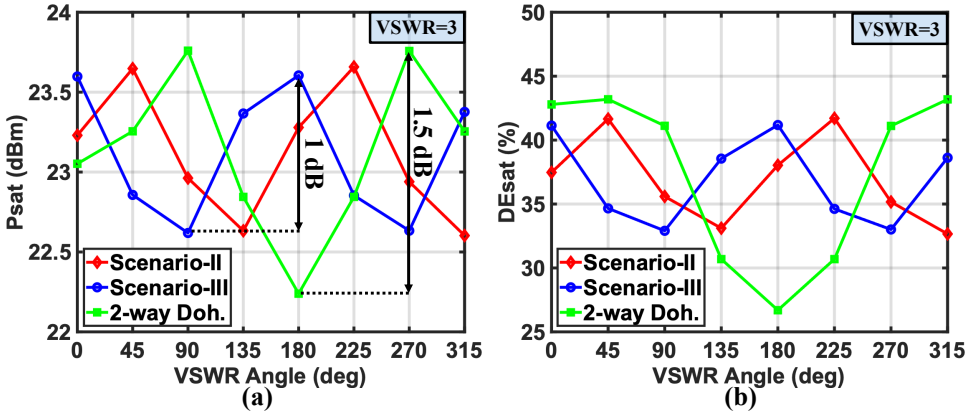


Fig. 5.10. (a) P_{sat} and (b) saturated drain efficiency (DE_{sat}) versus VSWR angle for VSWR magnitude of 3.

5

The proposed design incorporates only two QHCs, minimizing losses and making its performance comparable to the power combiner shown in Fig. 5.1(a). Additionally, placing the QHCs closer to the drain of the PA is advantageous, as it reduces the effect of antenna impedance variations. This proximity helps the QHC maintain impedance stability without adversely affecting Doherty operation. The use of QHCs makes the proposed structure a balanced PA, thereby reducing forward power deviation, delivered power loss, and efficiency degradation in the presence of mutual coupling and impedance mismatch, which are independent sources of performance degradation [125].

Fig. 5.10 shows the variation of P_{sat} and saturated drain efficiency (DE_{sat}) across the VSWR angle for VSWR magnitude of 3 with ideal output network and PAs. The presence of a QHC at the output reduces P_{sat} variation by 0.5 dB compared to a 2-way Doherty network without a QHC. Furthermore, removing one QHC does not compromise VSWR resilience, indicating that Scenario III achieves better passive efficiency while maintaining similar VSWR resilience to Scenario II.

Finally, placing the QHC closer to the PA drain remains advantageous, as it helps sustain impedance stability and ensures proper Doherty operation under dynamic antenna conditions.

5.4.1. DESIGN PROCEDURE

The schematics of the output power combiner are shown in Fig. 5.11. The phase requirement of each PA is important as it is needed for proper Doherty operation and power combining at the output. The phase of each PA and the phase at the input of QHCs are shown in Fig. 5.11. It consists of four 2-way Doherty networks (highlighted in orange), two QHCs, and a balun to convert the differential signal to an SE signal. The Doherty network, comprising two inductors and a capacitor, is depicted in Fig. 5.2(b), and its layout is shown in Fig. 5.12(a). It has an area of 0.028 mm^2. The inductors supply V_{DD} to the main and peak-1 PAs, respectively. To achieve a P_{sat} of 22 dBm with a V_{DD} of 2 V

for a symmetric 2-way Doherty, the SE R_{opt} is 25 Ω calculated using the equations in Fig. 5.2(b). The Z_0 of the TL (Z_{13}), along with the values for the inductor (L_1) and capacitor (C_1) can be determined using (5.16).

$$\begin{aligned} Z_{13} &= 2R_{opt} \\ L_1 &= \frac{Z_{13}}{\omega} \\ C_1 &= \frac{}{Z_{13}\omega} \end{aligned} \tag{5.16}$$

The simulation results shown in Fig. 5.13(a) are based on the EM model of the Doherty output network (illustrated in Fig. 5.12(a)) generated using Keysight's Momentum™, with capacitors having a QF of 25, and ideal PA models. The designed Doherty network achieves a P_{sat} of 22 dBm, with a 2 dB loss in the output network at 30 GHz. The connection between the Doherty output and the QHC is designed as an L-match network to increase the impedance from 25 Ω to 31 Ω.

In the second stage of power combining, QHCs are employed to enhance VSWR resilience. The differential QHC is designed using a transformer with an SE impedance of 31 Ω and has an area of 0.012 mm^2. The high-k transformer-based QHC design is done using (5.17) provided in [109], which helps to reduce the transformer size significantly. ω_0 is the center frequency, k is the coupling, L is the inductance in the transformer, and Z_0 is the characteristic impedance. For Z_0=31 Ω and k=0.8, other parameters can be calculated.

$$\begin{aligned} C &= C_M + C_G \\ \frac{C_M}{C} &= k \\ Z_0 &= \sqrt{\frac{L}{C}} \\ \omega_{\lambda/4} &= \frac{1}{\sqrt{LC(1-k^2)}} \\ \omega_0 &= 0.54\omega_{\lambda/4} \end{aligned} \tag{5.17}$$

The isolation ports are properly terminated at 31 Ω (R_T). The type of resistor used is a P+ poly resistor without salicide. Fig. 5.12(b) shows the layout of the QHC. The parasitic ground capacitance of the physical transformer can be absorbed in C_G, and the parasitic inter-winding capacitance can be absorbed in C_M.

In the third stage, a non-isolated power combining technique is utilized instead of an additional QHC to minimize losses in the output network. The traces are modeled as a coplanar edge-coupled structure (Fig. 5.12(c)) with Z_0 equal to the differential Z_0 of transformer-based QHC. Hence, the 4-way combiner, which employs two QHCs and non-isolated combining, exhibits a 0.8 dB loss at 30 GHz, including the interconnects, as illustrated in Fig. 5.13(b).

The balun (Fig. 5.12(d)) at the output converts the differential-ended signal to a SE signal while also matching it to a 50 Ω SE antenna. The non-isolated combining reduces the differential impedance to 31 Ω since it is a parallel combination. Then, the balun is

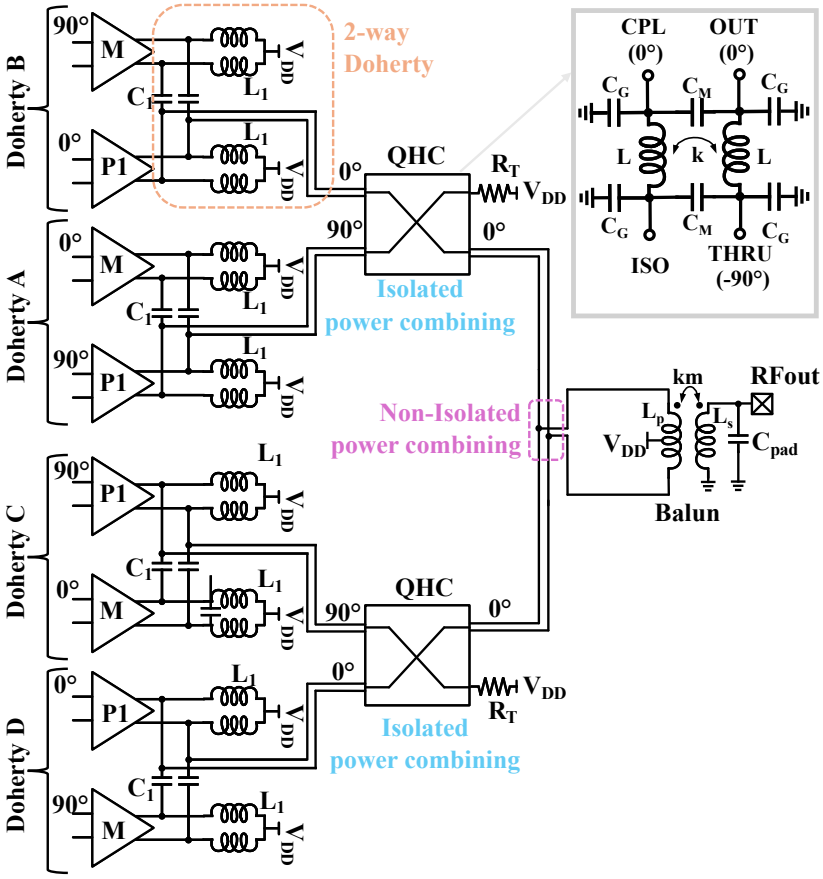


Fig. 5.11. Schematic of the proposed power combiner using 2-way Doherty network and QHCs.

used to match the R_L of 50 Ω and pad capacitance (C_{pad}) to R_P = 31 Ω.

$$N = \frac{R_L}{R_p} = \frac{n}{km}$$
$$n = \sqrt{\frac{L_s}{L_p}} \tag{5.18}$$
$$\omega_0 = \frac{1}{\sqrt{L_s C_{pad}}}$$

However, this comes at the cost of reduced passive efficiency. The balun can be integrated into the Doherty output network to achieve a SE output, as suggested in [95, 98, 102]. The decision to use a differential power combiner (including the Doherty network and QHC) stems from the poor grounding of PAs, particularly for Doherty A and C, due to the ground pads being positioned on either side — a limitation of the technology (see Fig. 5.14). Maintaining the signal differential until the end relatively mitigates this issue.

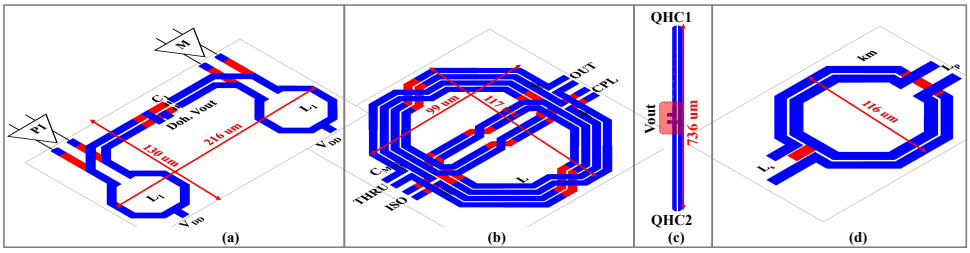


Fig. 5.12. (a) Layout of 2-way Doherty, (b) QHC, (c) non-isolated power combining, and (d) balun.

Fig. 5.13(c)/(d)/(e)/(f) presents the simulation results using the EM model of the proposed network shown in Fig. 5.11, with a QF of 25 for the capacitors and ideal PAs. Fig. 5.13(c)/(d) illustrate the PE and DE versus P_{out} across the frequency range of 26-34 GHz. At 30 GHz, the proposed power combiner achieves a P_{sat} of 26 dBm and a maximum DE of 30 %, with a loss of 4.6 dB in the output network. Fig. 5.13(c) shows that the balun introduces an additional 1 dB of loss. This balun can be omitted if a differential antenna is used or if better technology provides improved grounding for the PAs and allows the balun to be absorbed into the Doherty network, as previously discussed.

Fig. 5.13(e)/(f) show DE and P_{out} at 0/6/9.5 dB PBO for both the individual 2-way Doherty and the proposed power combiner. The proposed power combiner exhibits a 1 dB bandwidth in P_{out} of 10 GHz (24-34 GHz), which is comparable to that of the individual 2-way Doherty. This indicates that the bandwidth of the proposed network is limited by the Doherty network, not by the QHCs or balun. Across the frequency range of 24-34 GHz, the proposed network achieves a DE of more than 25/15 % at 0/6 dB PBO, respectively.

5.5. CIRCUIT IMPLEMENTATION

Fig. 5.14(a) presents a detailed diagram of the proposed PA configuration. The initial component is a SE input splitter that generates the required phase for the main and peak-1 PAs within each Doherty amplifier. The phase of the peak-1 PA must lead by 90° relative to the main PA in each Doherty. Additionally, the output phases of Doherty B and D must be 90° ahead of Doherty A and C to ensure that the power is combined in phase by the output QHCs. The input splitter comprises a Wilkinson divider and six QHCs. The Wilkinson power splitter is designed with lumped components to match a 50 Ω impedance and provide wideband matching [78, 126, 127]. After the power is divided by the Wilkinson, each output is fed to three transformer-based SE QHCs [108], which are designed to produce the necessary phase shifts as depicted in Fig. 5.14(a). The isolation ports are terminated with 50 Ω, using P+ poly resistors without salicide. Fig. 5.15(a) demonstrates that the phase variation across the frequency for the main and peak-1 paths in each Doherty is less than 5°, and the input splitter introduces less than 2 dB of loss in the frequency range 24-32 GHz. Although using three QHCs extends the bandwidth, it also increases the insertion loss [109].

[3] Passive efficiency (PE) accounts for the passive losses across the entire front-end architecture, including

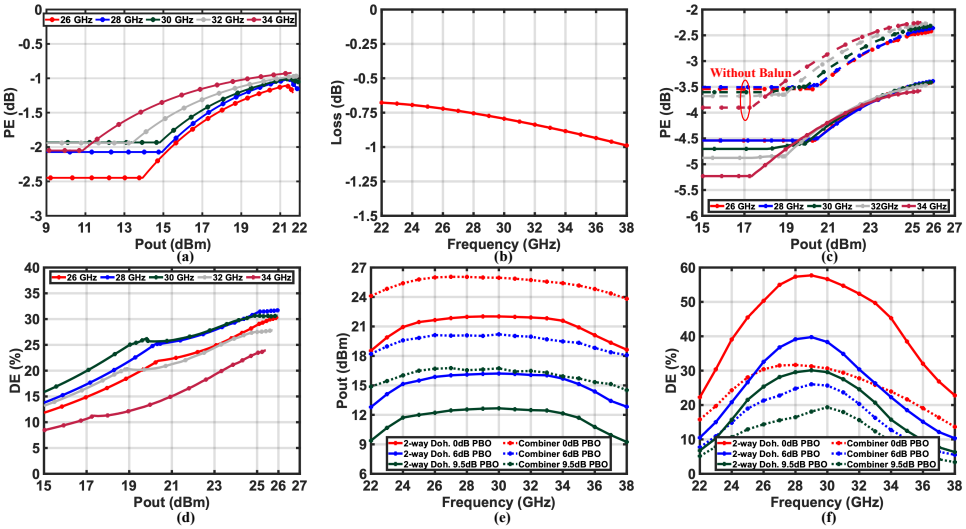


Fig. 5.13. (a) PE versus P_{out} across the frequency using the EM model of 2-way Doherty, (b) loss of QHCs and non-isolated power combining interconnects versus frequency using the EM model, (c) PE^3 versus P_{out}, (d) DE versus P_{out} across the frequency of the proposed power combiner, (e) DE, and (f) P_{out} versus frequency of the individual 2-way Doherty and the proposed power combiner.

Following the input splitter, each branch in the Doherty amplifier, namely the main and peak-1 paths, includes an input balun, PDRV, inter-stage matching, DRV, inter-stage matching, and the PA itself. A balun is then used to convert the SE signal into a differential signal while providing inter-stage matching. This balun employs a double-tuned transformer design [31, 110, 111] to achieve broad matching, resulting in a passive efficiency of 70 %, as calculated using the equation from [112]. The required power gain is attained by incorporating two additional driver stages, each utilizing a neutralized common-source transistor consisting of four unit cells, each with 50 fingers and a width of 1 µm (Fig. 5.14(c)). A bias of 0.6 V is applied to the PDRVs and DRVs. The inter-stage matching between the PDRVs and DRVs employs a double-tuned transformer network to ensure wideband matching, achieving a passive efficiency [112] of 74 %.

The intermediary stage between the DRV and PA also uses a double-tuned transformer technique for wideband matching, achieving a passive efficiency of 69 %. Fig. 5.14(b) shows the detailed schematic of the cascode PA. To maximize output-to-input isolation and ensure unconditional stability [128], two pairs of neutralization capacitors are used for the common-source and common-gate transistors. Additionally, two 21 pH inductors align the voltage and current wave phases, thereby improving drain efficiency [67]. Each common-source transistor in the PA comprises eight unit cells, each with 50 fingers and a width of 1 µm, optimized for f_T and F_{max} while minimizing the effects of device parasitics and interconnections [129]. The cascode transistors include five unit cells with a transistor aspect ratio of 2 µm/40 nm and 40 fingers [95]. The bias is set at 0.55 V for the common-source transistor and 1.6 V for the common-gate transistors. Additionally,

the four 2-way Doherty amplifiers and the 4-way power combiner with and without the balun.

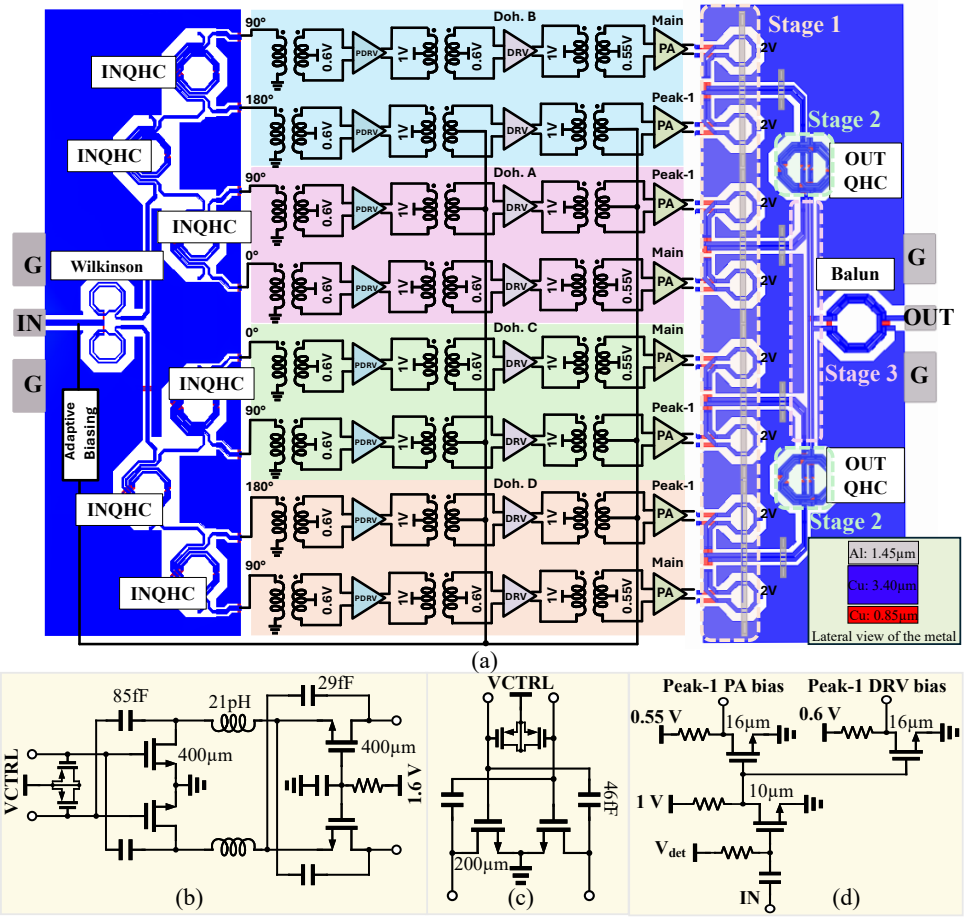


Fig. 5.14. (a) The schematics of the proposed 4 × 2-way Doherty PA, including the output combiner's layout, (b) cascode PA, (c) DRV/PDRV, and (d) adaptive biasing.

two PMOS varactors are employed at the PA and DRV inputs to enhance their AM-PM profiles. The nonlinear variation of the input capacitance of an NMOS transistor can be compensated by adding a PMOS varactor at the input. The varactors at the PA and DRV inputs aren't driven dynamically, and the control voltage (VCTRL) can be used to compensate for PVT variations or model inaccuracy during the design phase [70].

An adaptive biasing circuit, shown in Fig. 5.14(d), is employed to implement the desired current profile of the peak PAs in the Doherty amplifier. Adopted from [113], this circuit includes an SE envelope detector with an RF input and a turn-on voltage (V_{det}), along with two drivers for the DRV and PA. The V_{det} of the envelope detector can be adjusted to control the activation of the peak-1 PA, thereby influencing load modulation. If V_{det} is increased, the peak-1 PAs remain on, causing the output network to function as a power combiner without improving efficiency at PBO. The adaptive biasing circuit

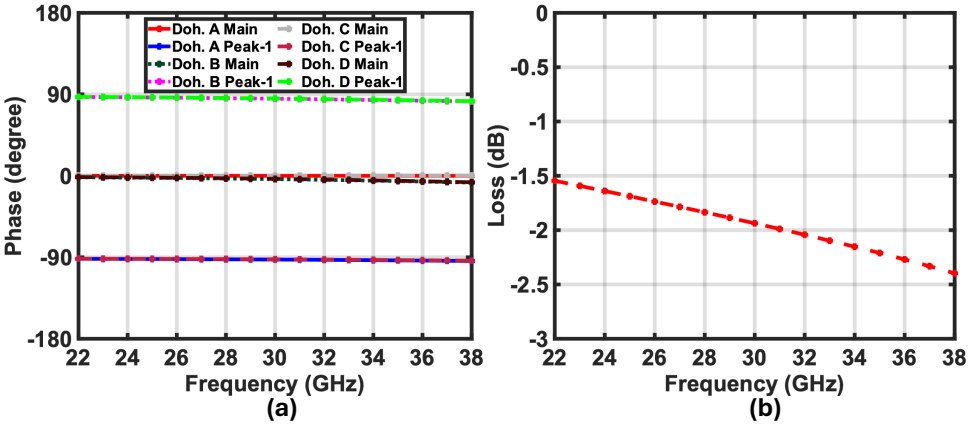


Fig. 5.15. (a) Phase variation across the frequency for the main and peak-1 paths in each Doherty (A, B, C, and D), and (b) loss across the frequency for the input splitter using the EM model.

provides a 3 dB bandwidth of 2.5 GHz.

5.6. MEASUREMENT RESULTS

The proposed PA was fabricated using a 40 nm bulk CMOS technology, as depicted in Fig. 5.16. The core area of the 4 × 2-way Doherty power combiner is 1.1 × 1.4 mm^2. Measurements were conducted using a high-frequency probe station, with DC supplies, bias voltages, and the adaptive biasing turn-on voltage wire-bonded directly to a PCB. The PAs operate with a 2 V supply voltage, while the DRVs and PDRVs within each Doherty amplifier use a 1 V supply. Fig. 5.17 illustrates the setup for CW (blue), modulated (black), and VSWR measurements (red). The insertion loss of the Z-probe, cables, and directional coupler was measured and de-embedded from the results.

5.6.1. CONTINUOUS WAVE MEASUREMENT RESULTS

The small-signal S-parameter performance is measured using the Keysight E8361A vector network analyzer. As Fig. 5.18(a) demonstrates, the proposed PA achieves more than 6 GHz small-signal BW_{3dB} where its S_{11}/S_{12} are less than −8/−50 dB over a 24-to-32 GHz band. At 28 GHz, PA's S_{22} is −18 dB, while its input matching is −9 dB. The PA offers 25.5 dB small-signal gain at 28 GHz.

The large signal CW measurement results are reported in Fig. 5.18(b)/(c)/(d). As V_{det} increases, peak-1 PAs are always on, and there is no load modulation. Thus leading to no efficiency at 6 dB PBO. But if V_{det} is reduced a lot, then the gain won't be flat and the PA becomes nonlinear. Thus, V_{det}=0.5 V is chosen for measurements in Fig. 5.18(b)/(c)/(d). From Fig. 5.18(b), the P_{1dB}, P_{sat} and gain are 23 dBm, 25.2 dBm and 25.5 dB at 28 GHz, respectively. Its DE at P_{sat}, and 6 dB PBO are 20.5 %, and 13.3 %, respectively.

Fig. 5.18(d) shows the P_{sat}, DE, and PAE across the frequency at 6 dB PBO, and full power with V_{det} of 0.5 V. It can be seen that the proposed PA achieves more than 24.5 dBm

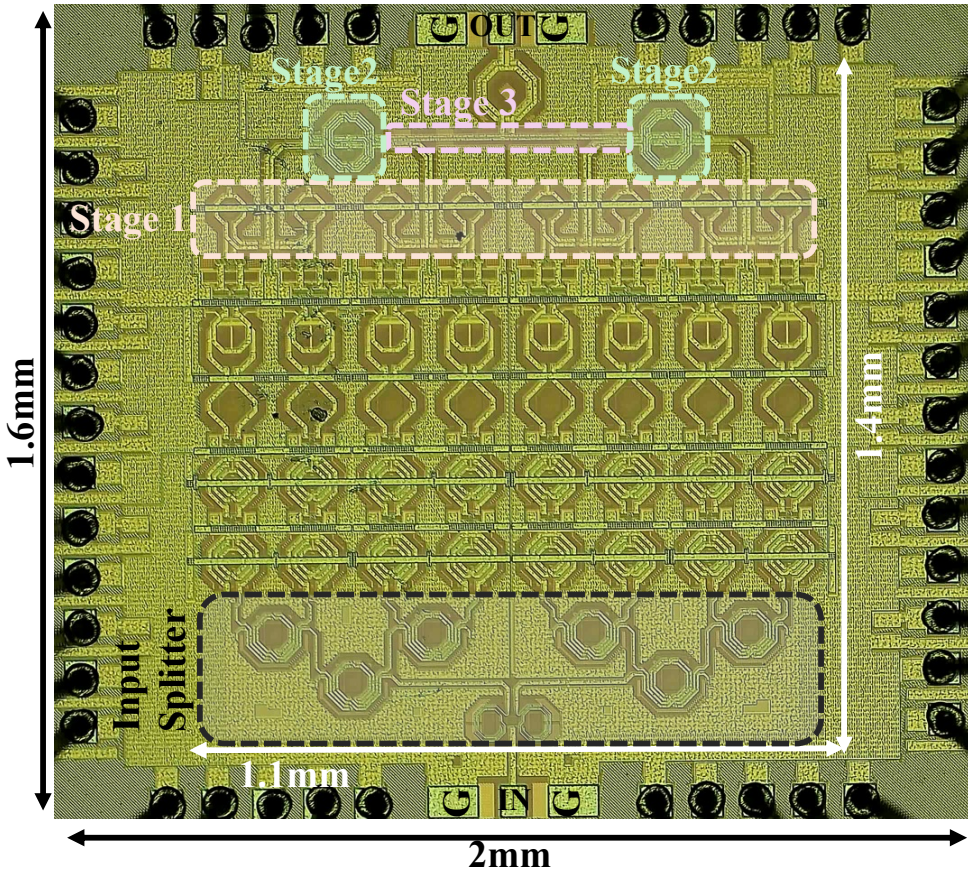


Fig. 5.16. The die micrograph of the proposed 4 × 2-way Doherty PA.

P_{sat} and a DE of better than 17.5 %/10 % at 6 dB/0 dB across the 26-to-32 GHz band. The PA achieves a 1 dB bandwidth of 7 GHz with respect to the P_{sat}.

5.6.2. Modulated Signal Measurement Results

The PA dynamic performance is verified using wideband modulated signals such as "64-QAM OFDM", "256-QAM OFDM", and "1024-QAM OFDM" signals. As demonstrated in Fig. 5.17, the baseband I/Q modulated signals are generated with an arbitrary waveform generator (Keysight AWG M8190A) and upconverted using a Marki I/Q mixer (MMIQ-1865L). A directional coupler (Marki C20-0240) is employed at the output to provide the signal for an R&S FSW43 signal analyzer, while an R&S NRP50S measures the output power. Fig. 5.19(a) exhibits 11.3 dBm/4 % average output power (P_{avg})/average drain efficiency (DE_{avg}) measured for a 12 Gb/s OFDM 64-QAM signal at 28 GHz with 9.6 dB PAPR. Its EVM/ACLR are −25 dB/−33.6 dBc, respectively. Similarly, the proposed PA achieves 11.5 dBm/4 % P_{avg}/DE_{avg} for a 6 Gb/s OFDM 64-QAM signal with EVM/ACLR of −25 dB/

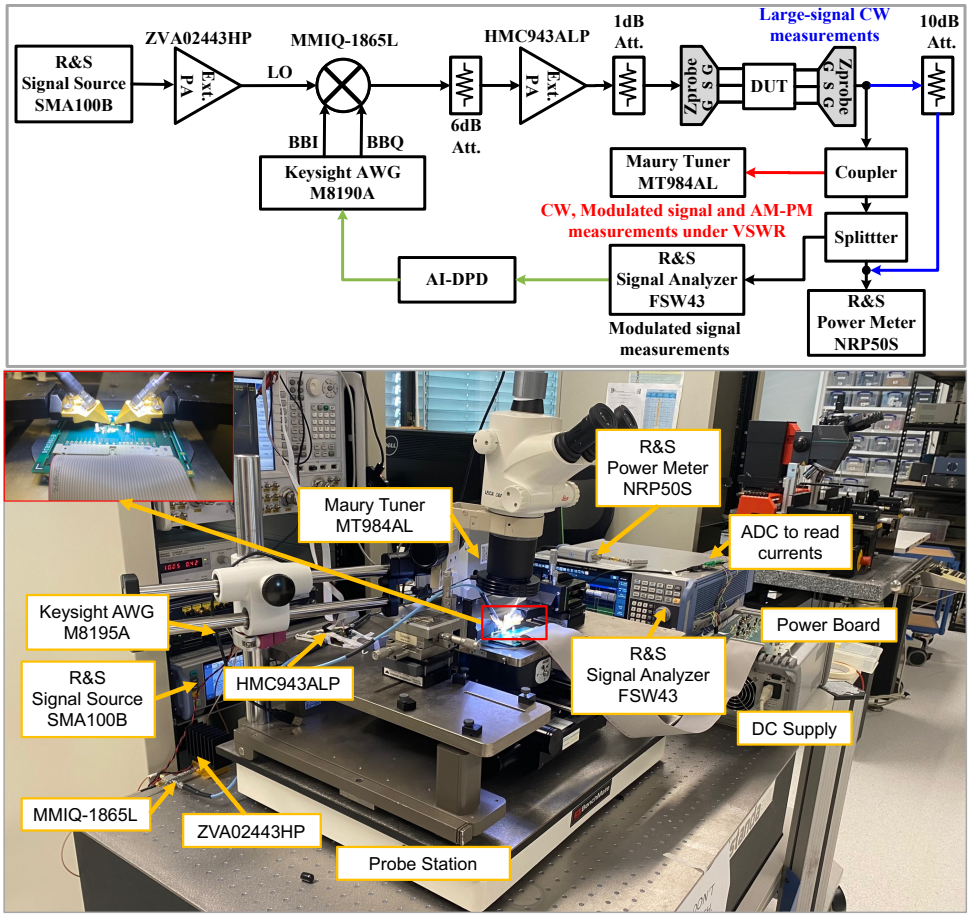


Fig. 5.17. The measurement setup of the proposed 4 × 2-way Doherty PA.

−32.3 dBc, respectively (Fig. 5.19(b)).

For a 6.4 and 3.2 Gb/s OFDM 256-QAM signal with 9.8 dB PAPR, the proposed PA achieves an EVM/ACLR of −30 dB/−39.4 dBc and −30 dB/−39.5 dBc, respectively (Fig. 5.19(c)/(d)). Furthermore, the spectral purity and constellation of a 100 MHz and 50 MHz OFDM 64-QAM signal is measured at 28 GHz with EVM/ACLR of −35 dB/−42.1 dBc and −35 dB/−42.3 dBc which are illustrated in Fig. 5.20(a)/(b).

Figs. 5.21 and 5.22 illustrate the P_{avg} and DE_{avg} for an OFDM signal with different bandwidths (2000/1000/800/400/100 MHz) and modulation schemes (64/256) within the 24-to-33 GHz frequency band, aiming to meet specific EVM requirements. To elaborate, considering the minimum EVM requirement for a 64-QAM signal as −21.9 dB [10, 11], and providing a 3 dB margin, we present the P_{avg}/DE_{avg} for an EVM of −25 dB. The proposed PA achieves a P_{avg}/DE_{avg} performance surpassing 10 dBm/3 % in the 25-to-30 GHz band, as shown in Fig. 5.21(a)/(b). Additionally, Fig. 5.22(a)/(b) exhibit corresponding

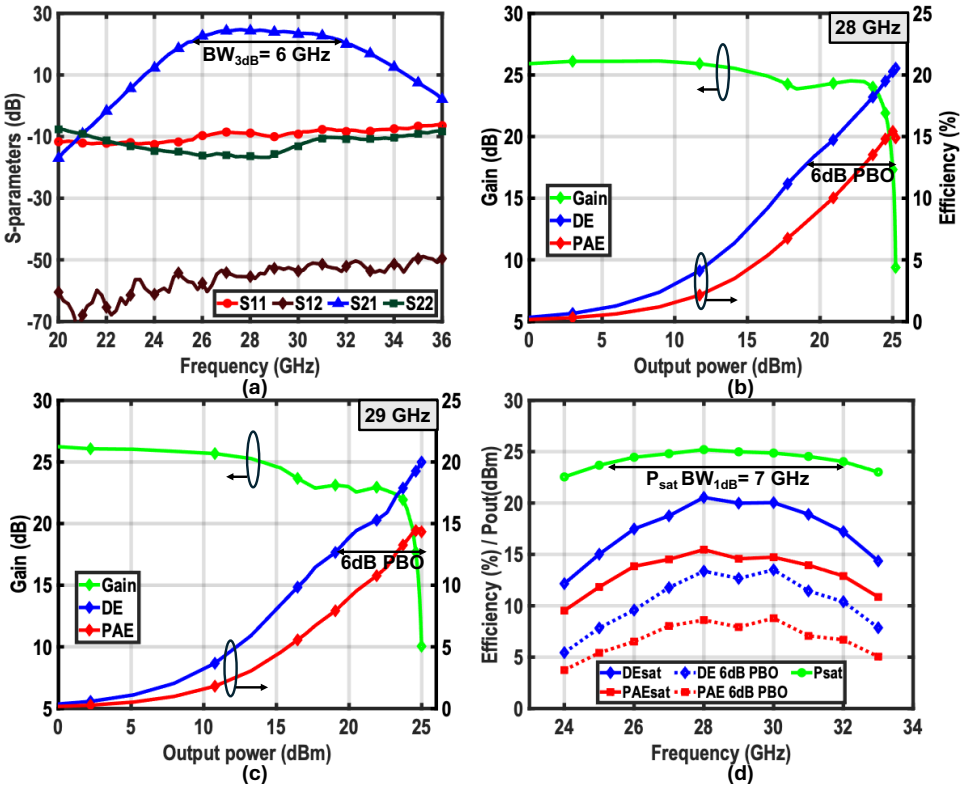


Fig. 5.18. (a) S-parameter measurement, (b) large-signal measurements at 28 GHz, (c) 29 GHz, and (d) P_{sat}, DE, and PAE across the frequency range 24-33 GHz at full power and 6 dB PBO.

results for OFDM 256-QAM signals with bandwidths of 800/400/100 MHz.

5.6.3. Doherty Mode Versus Power Combiner Mode

As previously discussed, V_{det} determines when the peak-1 PAs activate, significantly impacting back-off efficiency. Setting V_{det} = 0.9 V keeps the peak-1 PAs continuously on, causing the output network to function as a simple power combiner without providing any efficiency enhancement at PBO. From Fig. 5.23(a), it can be observed that the power combiner mode exhibits a flat gain but does not offer any efficiency enhancement at 6 dB PBO.

Fig. 5.23(b) presents the EVM and DE_{avg} versus P_{avg} for a 2 GHz 64-QAM OFDM signal under two scenarios: V_{det} = 0.5 V (Doherty mode) and V_{det} = 0.9 V (power combiner mode). It is evident that in the power combiner mode (V_{det} = 0.9 V), P_{avg} increases by 3 dB while still meeting the EVM requirement of −25 dB for the 64-QAM OFDM signal. However, the achieved average efficiency remains at 4 % in both modes, as the Doherty operation, which offers improved efficiency at PBO, compensates for its lower P_{avg}.

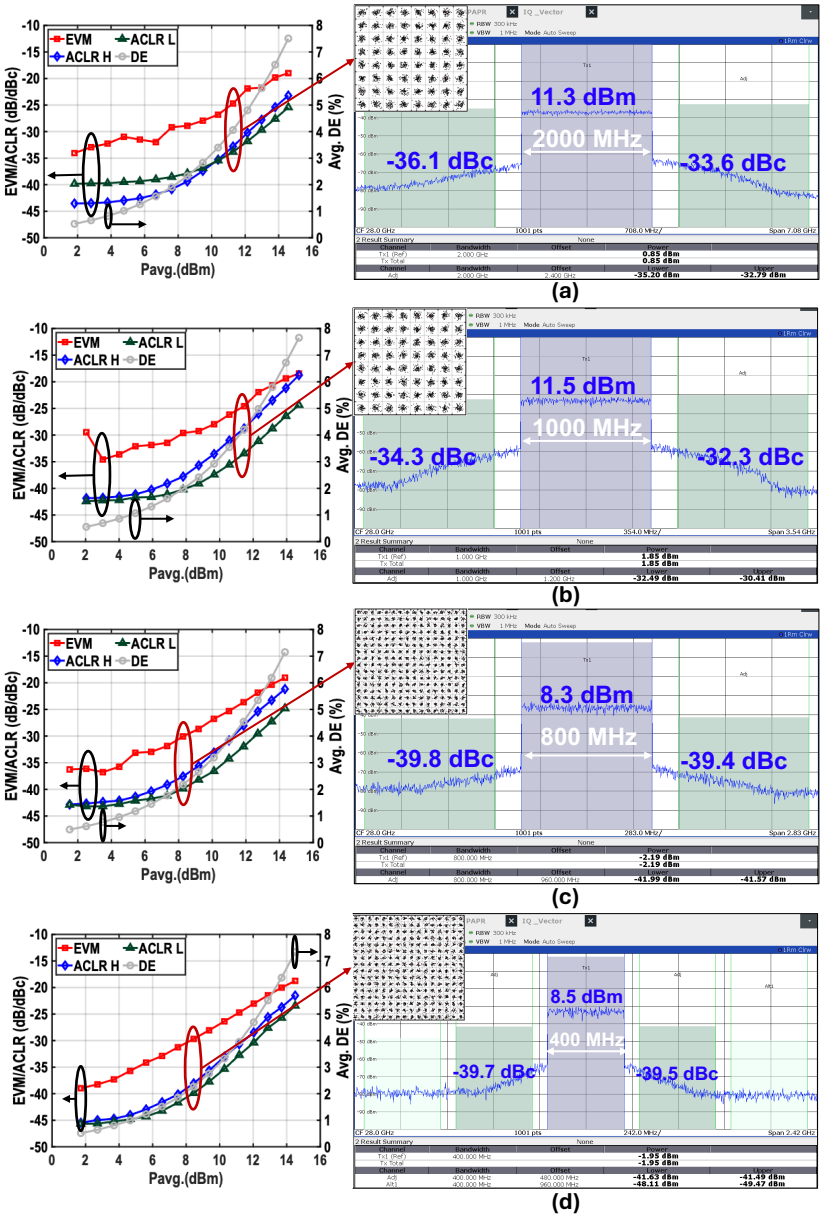


Fig. 5.19. (a) An OFDM 2000 MHz 64-QAM, (b) an OFDM 1000 MHz 64-QAM, (c) an OFDM 800 MHz 256-QAM, and (d) an OFDM 400 MHz 256-QAM at 28 GHz measurement results.

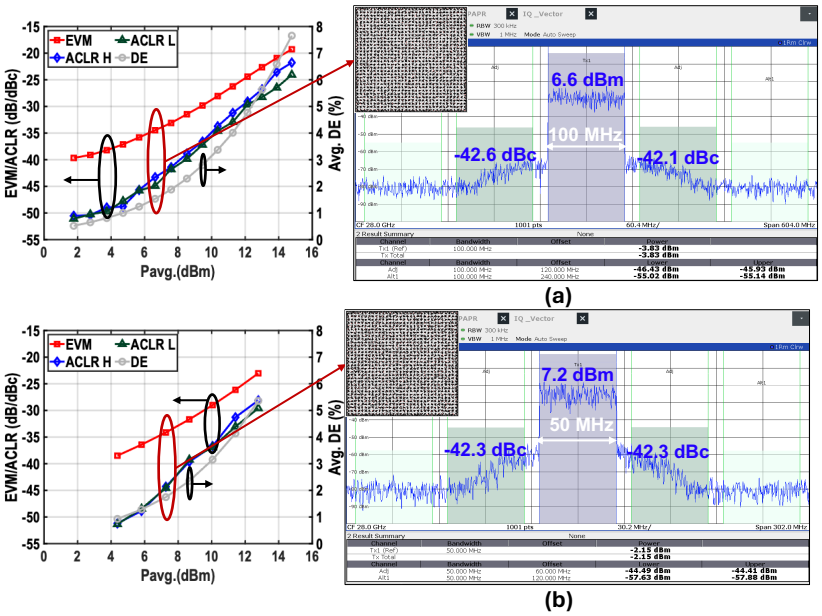


Fig. 5.20. (a) An OFDM 100 MHz 1024-QAM, and (b) an OFDM 50 MHz 1024-QAM at 28 GHz measurement results.

Fig. 5.23(c)/(d) display P_{avg} and DE_{avg} for a 64-QAM OFDM signal with varying bandwidths (2000/400 MHz) across frequencies to achieve an EVM of −25 dB. These results indicate that enabling the power combiner mode improves P_{avg} by at least 2 dB, while DE_{avg} remains similar to Doherty across the frequency range. This suggests that the Doherty mode exhibits greater nonlinearity.

To delve deeper, we analyze AM-AM and AM-PM characteristics for V_{det} = 0.5/0.9 V. Fig. 5.24 shows the AM-AM and AM-PM distortions for Doherty mode (V_{det} = 0.5 V) and power combiner mode (V_{det} = 0.9 V) using a 64-QAM OFDM signal with a bandwidth of 50/1000 MHz across different frequencies. For $P_{avg} \approx 14$ dBm at 28 GHz, where the power combiner mode meets the EVM requirement of −25 dB, the Doherty mode exhibits higher AM-AM and AM-PM distortions, particularly for a 50 MHz bandwidth. This explains the Doherty mode's inferior EVM performance.

At lower $P_{avg} \approx 10$ dBm, both modes show similar AM-AM performance, but the Doherty mode suffers from greater AM-PM distortion. This indicates that AM-PM deterioration occurs earlier in the Doherty mode, contributing significantly to reduced EVM. The primary cause of AM-PM distortion is load modulation, which exacerbates the nonlinearity of transistor parasitics such as C_{ds}, making the Doherty PA inherently nonlinear. Similarly, adaptive biasing and phase misalignment also affect linearity, but these can be considered secondary effects.

These distortions can be mitigated through DPD, which linearizes the AM-AM and AM-PM characteristics, enabling the Doherty PA to operate at higher P_{avg} and achieve the intended efficiency improvements. An off-chip deep recurrent neural network (RNN)-

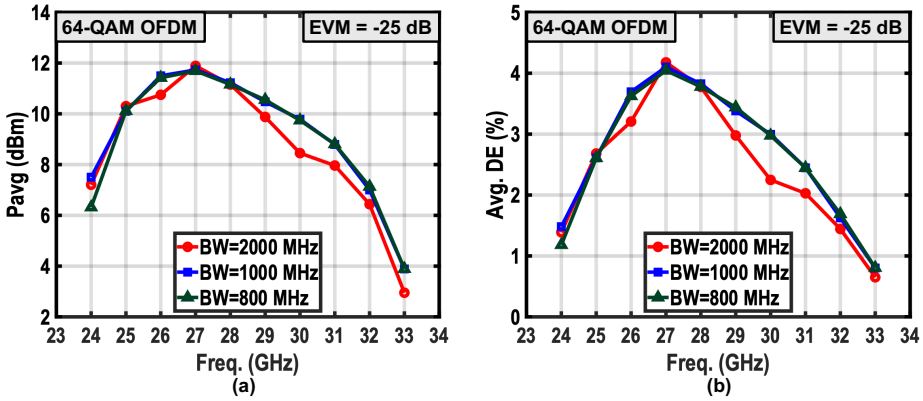


Fig. 5.21. (a) P_{avg}, and (b) DE_{avg} for OFDM 64-QAM across the frequency to achieve a certain EVM.

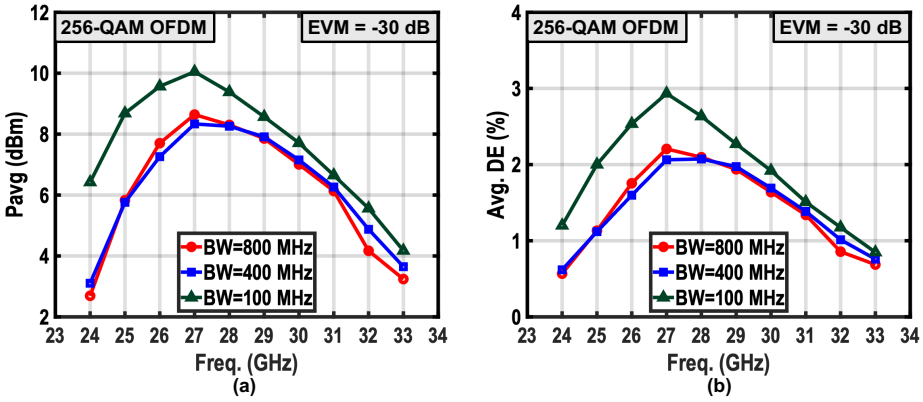


Fig. 5.22. (a) P_{avg}, and (b) DE_{avg} for OFDM 256-QAM across the frequency to achieve a certain EVM.

based DPD is employed to linearize the PA. This system utilizes a gated recurrent unit (GRU) regressor for PA modeling and DPD learning, and it is referred to as artificial intelligence digital pre-distortion (AI-DPD) [130]. The block diagram illustrating the steps involved in AI-DPD can be found in Appendix D.

Fig. 5.25 shows the measured spectrum and constellation of 1-CC 64-QAM OFDM signals with 400/1000 MHz modulation bandwidths at 28 GHz with and without the AI-DPD. With the implementation of AI-DPD, the proposed PA meets the −25 dB EVM requirement for a 64-QAM signal at a similar average power. This enhances the DE_{avg} and allows the proposed PA to operate closer to its saturated power. The related ACLR is also improved by 7 dB. It is noteworthy that the AI-DPD correction is restricted to up to the 1000 MHz modulation bandwidth, as the AI-DPD algorithm requires a sampling rate of at least 3.5-4 times the baseband bandwidth to ensure adequate coverage of adjacent channels and effectively mitigate spurious leakage.

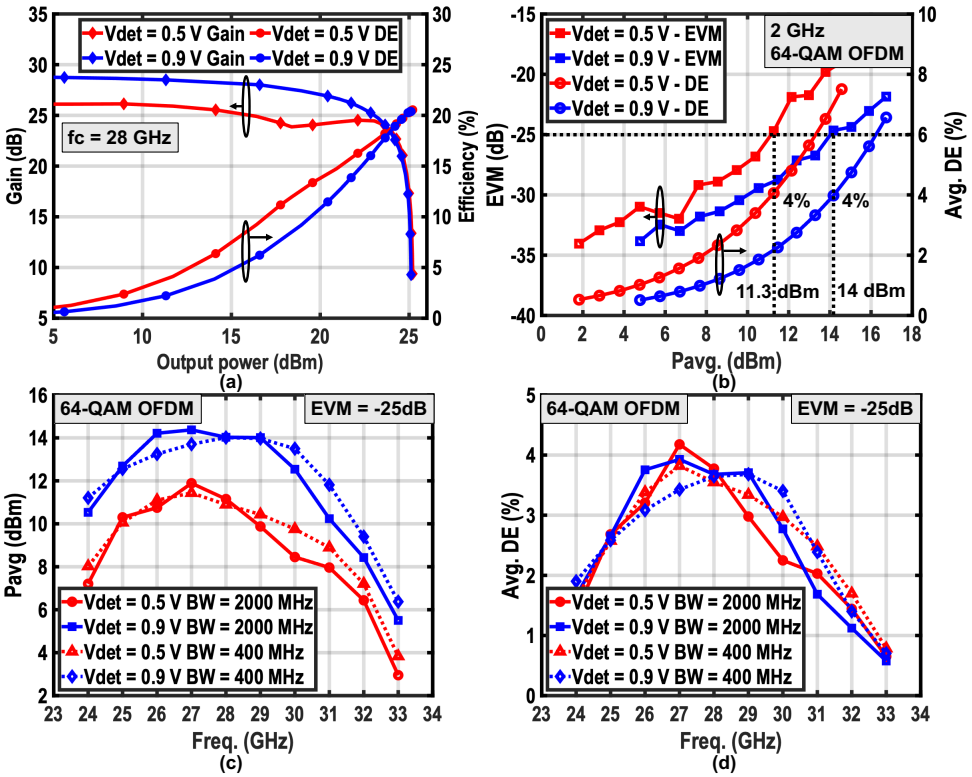


Fig. 5.23. (a) Gain/DE, (b) EVM/DE_{avg} versus P_{avg} for 2 GHz 64-QAM OFDM, (c) P_{avg}, and (d) DE_{avg} versus frequency to achieve EVM = −25 dB with V_{det} = 0.5 V and 0.9 V at 28 GHz.

5.6.4. VSWR Results

As previously discussed, maintaining linearity, gain, and output power stability under load mismatch is critical for mm-wave phased-array systems. The VSWR resilience of the proposed PA is assessed by measuring its AM-PM characteristics and large-signal performance under various VSWR conditions. The PA's VSWR variation shown in Fig. 5.26(a) comprises Gain/P_{1dB}/P_{3dB} (output power at 3 dB compression point)/P_{sat} variations at 28 GHz, demonstrating less than a 1.1 dB maximum variation over different VSWR angles. Its maximum AM-AM and AM-PM variations are less than 0.3 V and −18°, thus showing the VSWR resiliency of the proposed PA.

Fig. 5.26(e) exhibits measured constellations and spectrum of 1-CC 64-QAM OFDM signals with a 50 MHz modulation bandwidth at 28 GHz with and without the AI-DPD of the PA under VSWR = 2∠0. Notably, the AI-DPD model trained for VSWR = 1 or 50 Ω improves the EVM by more than 12 dB, achieving −29 dB with 15.1 dBm average power. The related ACLR is also improved. Fig. 5.26(d) exhibits EVM of 1-CC 64-QAM OFDM signals with 50 MHz modulation bandwidth at 28 GHz with and without the AI-DPD (trained at 50 Ω) under VSWR = 2/3, including eight different angles for 15 dBm average power. For VSWR = 3, the proposed PA achieves the lowest EVM of −21 dB, thanks to the VSWR

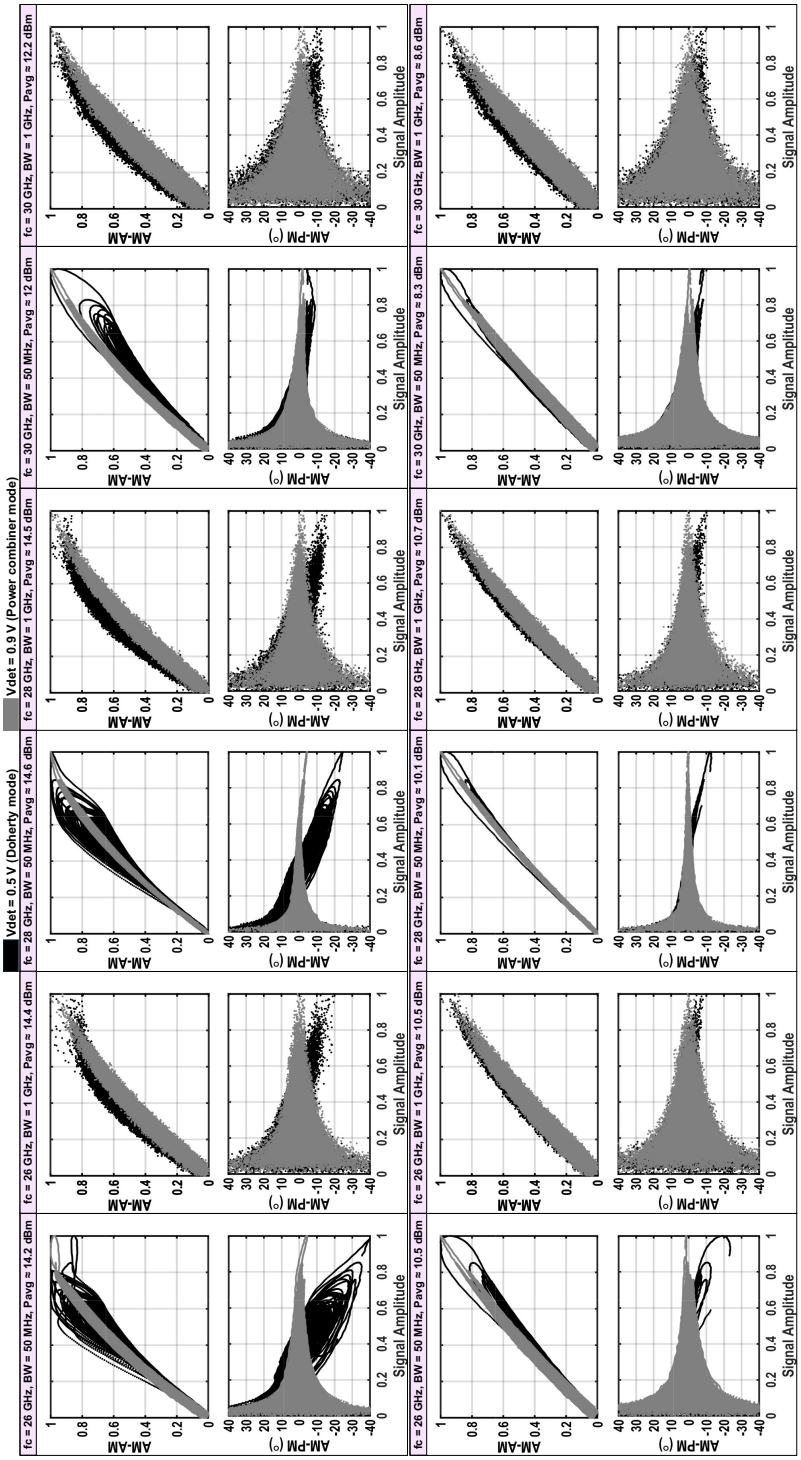


Fig. 5.24. The measured AM-AM/AM-PM of the proposed PA with Doherty mode (V_{det} = 0.5 V) and power combiner mode (V_{det} = 0.9 V) employing 64-QAM OFDM signals with PAPR ≈ 9.5 dB for different frequencies.

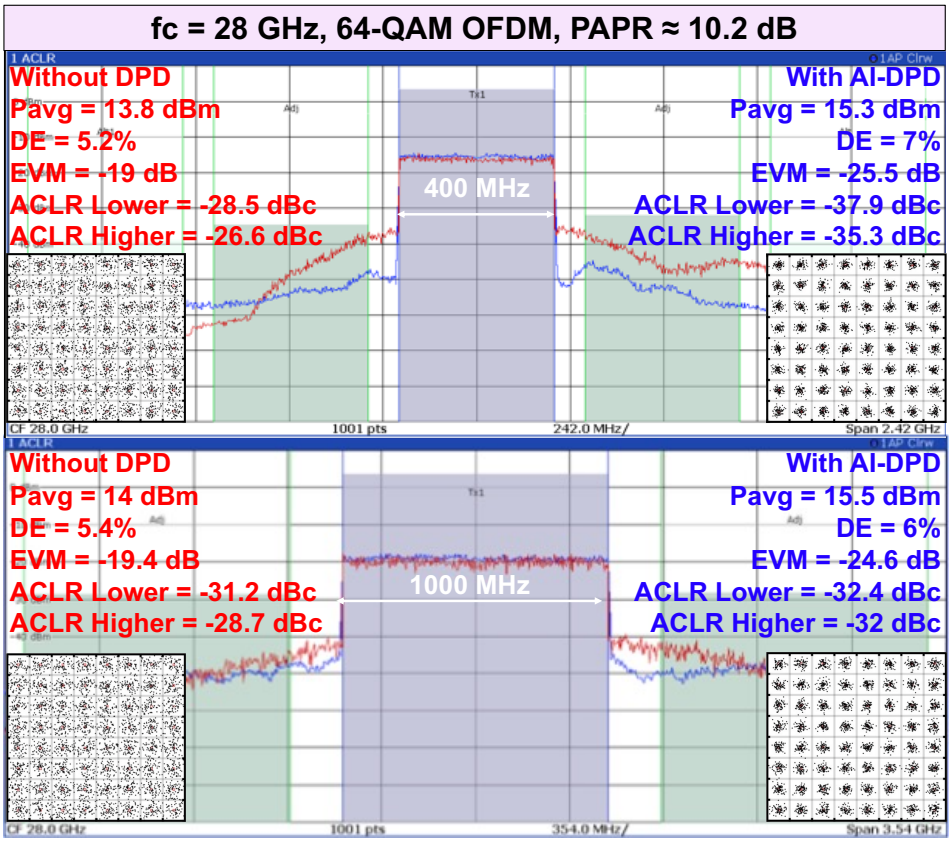


Fig. 5.25. (a) An OFDM 400 MHz 64-QAM, and (b) an OFDM 1000 MHz 64-QAM at 28 GHz measurement results with and without AI-DPD.

resilient output network.

5.7. Comparison with State-of-the-Art

The performance evaluation of the proposed 4 × 2-way Doherty PA is summarized in Table 5.2 and compared to that of previous designs with P_{sat}>23 dBm. The results highlight that even with a supply voltage of 2 V, our compact mm-wave front-end achieves P_{sat} of 25.2 dBm with a power gain of 25.5 dB. Furthermore, its core area (1.54 mm^2) is the second best among the PAs, achieving 25 dBm. The ITRS FoM is included to compare the overall performance [133], and the proposed PA has an FoM of 91.5 dB, which is the second best among efficiency-enhanced PAs. It also supports a 2 GHz 64-QAM OFDM signal with an average power of 11.3 dBm while meeting the EVM requirement of −25 dB. Notably, at 6/0 dB PBO, the DE maintains superiority over 10/17.5 % across the same frequency spectrum of 26-32 GHz. The DE primarily drops at 6 dB PBO due to the lossy C_{ds} of the main PA [102, 114]. The proposed 4 × 2-way Doherty PA is resilient to

Table 5.2

PERFORMANCE SUMMARY AND COMPARISON TO PRIOR ART

Specifications	This Work	Efficiency Enhanced PAs					Mm-Wave 5G PAs		
		X.Zhang TMTT'24 [131]	X.Zhang ISSCC'24 [121]	W.Zhu ISSCC'24 [132]	Z.Ma ISSCC'22 [98]	C.Chappidi JSSC'18 [89]	M.Pashaeifar ISSCC'24 [117]	S.Daneshgar TMTT'20 [120]	H.Ahn RFIC'20 [119]
Architecture	4x2-way Parallel Doherty PA	Rat-race coupler based 4x2-way Doherty PA	4-way Doherty PA	7-Way LMBA PA	3-way Parallel Series Doherty PA	Dual frequency-PBO reconfigurable PA	Chain-Weaver 8-way Balanced PA	2-stacked 4-way power combined PA	8-way Power Combiner
Technology	40 nm CMOS	45 nm SOI	45 nm SOI	65nm CMOS	55 nm CMOS	130 nm SiGe BiCMOS	40 nm CMOS	28nm CMOS	65 nm CMOS
Supply (V)	2(PA) 1(DRV/PDRV)	2.2	2,1	1	2.4, 1.2^{+}	4,1.6	2,1	2.2	NA
Oper. Freq. (GHz)	26-32	34.5-40	42.5-50	27.8-38.7	26-30	30-55	35-43	36.5-42	27-28
Freq. (GHz)	28	37	47	28	28	40	37	39	28
Core Area (mm^2)	1.54	1.84	0.81	2.2	0.54	0.96	2.08	0.95	0.25
Gain (dB)	25.5	18.5	17.1	17	16.1	23.4^{++}	29.9	38	15.9
P_{sat} (dBm)	25.2	27.5	24	26.2	25.5	23.7	25.2	26	23.2
DE_{sat}/PAE_{sat} (%)	20.5/15.3	NA/18	30*/26.8	30*/25.4	32.5/25.2	35*/26	NA/16.2	NA/26.6	NA/33.5
DE_{6dB}/PAE_{6dB} (%)	13.3/8.6	NA/15	24*/21.7	22*/19.7	25.4/20.4	22.5*/16.5*	NA	NA/10.4*	NA/15*
ITRS FoM (dB)	91.5	89.6	88.8	86.2	84.6	93.3	98.6	110.1	83.3
Modulation Scheme	64-QAM OFDM	64 QAM	64 QAM OFDM	64 QAM	64 QAM	16 QAM	64 QAM OFDM	64 QAM OFDM	256 QAM
Data rate (Gb/s)	12/6/2.4	2.4	12	4.5	1.5$^{\#}$	4	12	0.6	0.8
Modulation BW (MHz)	2000/1000/400	400	2000	750	250	1000	2000	100	100
EVM_{rms} (dB)	-25/-24.6/-25.5	-25.1	-25	-26.8	-25.2	-19.2	-25	-28.5*	-31.2
ACLR (dBc)	-33/-32/-35.3	-26.2	-30.5	-32.7	-27	-30	-30.7	-33*	-30
P_{avg} (dBm)	11.3/15.5/15.3	18.5	14.1	17.3	17.7	16.9	16	19.5	18.2
PAE_{avg} (%)	4/6/7.2 (DE_{avg})	10.9	13.7	13.9	17.5	24.6	4.1	8.3	17.6
DPD	No$^{\#}$/Yes/Yes (AI-DPD)	No	No	No	No	Yes	No	Yes	No
Output Config.	SE	DE	DE	SE	SE	SE	SE	SE	SE
VSWR	3:1 @28 GHz	NA	NA	NA	NA	NA	3:1 @37 to 40 GHz	NA	NA
Gain Deviation (dB)	1	NA	NA	NA	NA	NA	0.7	NA	NA
P_{1dB} Deviation (dB)	0.8	NA	NA	NA	NA	NA	0.79	NA	NA
AM-PM_{max} (°)	-18	NA	NA	NA	NA	NA	2.8	NA	NA
Modulation Scheme	64-QAM OFDM (28 GHz)	NA	NA	NA	NA	NA	NA	NA	NA
Modulation BW (MHz)	50	NA	NA	NA	NA	NA	NA	NA	NA
EVM Deviation (dB)	7 (AI-DPD)	NA	NA	NA	NA	NA	NA	NA	NA

NA - Not Available. SE - Single-ended. DE - Differential-ended. $^{\#}$limited by equipment. *Graphically estimated. $^{+}$Nominal voltage of the technology. $^{++}$Gain at P_{sat}.
ITRS FoM = P_{sat}(dBm) + Gain(dB) + $10log_{10}(PAE_{max}[\%])$ + $20log_{10}(f_c[\text{GHz}])$ [133].

VSWR, thanks to QHC included, in the compact output network.

With assistance from DPD, the proposed PA can meet the linearity requirement for a 1 GHz 64-QAM OFDM signal at an average power of 15.5 dBm. The proposed PA preserves its required linearity and improves its average power while achieving the required EVM of −21.9 dB across VSWR of 2. Meanwhile, the DPD needs to be trained only at 50 Ω,

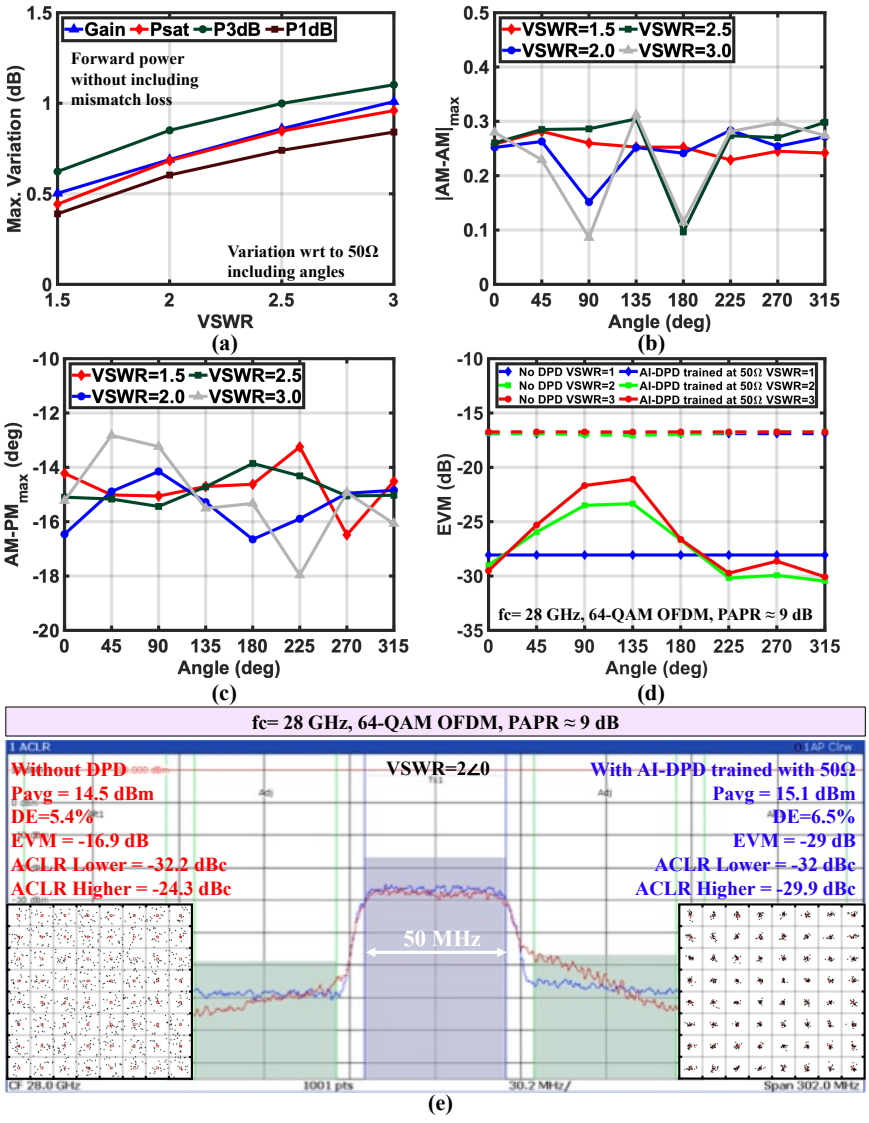


Fig. 5.26. (a) Gain/P_{1dB}/P_{3dB}/P_{sat} variation across VSWR, (b) maximum AM-AM error, (c) maximum AM-PM error across angles for different VSWR, (d) EVM versus VSWR angles for 50 MHz 64-QAM OFDM signal with and without AI-DPD trained at 50 Ω, (e) spectrum and constellation for VSWR = 2∠0 with and without AI-DPD trained at 50 Ω.

thus reducing training time, thanks to the VSWR resilience of the proposed PA.

5.8. SUMMARY

A mm-wave 4x2-way Doherty PA has been implemented that features a high P_{out} and gain. The design procedure for implementing the output network has been thoroughly explained. The proposed PA is fabricated using 40 nm CMOS technology, occupying a core area of 1.54 mm^2. The realized front-end operating at 28 GHz demonstrates a power gain of 25.5 dB, a peak power of 25.2 dBm, and a DE of 20.5 %/15.3 % at PBO levels of 0 dB/6 dB. It attains an EVM and ACLR of −25 dB/−32 dBc for a 1000 MHz 64-OFDM signal with a P_{avg} of 11.5 dBm and a 4 % DE_{avg}. For an 800 MHz 256-QAM OFDM signal, the proposed PA achieves EVM/ACLR of −30 dB/−39 dBc with a P_{avg}/DE_{avg} of 8.3 dBm/2 %. It is also resilient to VSWR variations, keeping gain and P_{1dB} deviation less than 1 dB and 0.8 dB, respectively. With the help of AI-DPD, the proposed PA can achieve a P_{avg} of 15.3 dBm for a 400 MHz 64-QAM OFDM signal, thus improving the DE_{avg}. These results make it a promising choice for adoption in 5G mm-wave TXs or phased arrays.

6

Conclusion & Future Work

This chapter presents the outcomes of the thesis, compares them with the state-of-the-art, and highlights the key takeaways from the dissertation. Additionally, it offers recommendations for future research.

6.1. THESIS CONTRIBUTIONS

This dissertation presents novel PA architectures, addressing the critical key performance indicators (KPIs) required for mm-wave phased array TX, including high output power, high average efficiency, linearity, wide modulation bandwidth, high gain, and resilience to VSWR. These designs aim to leverage the mm-wave spectrum to enable multi-gigabit data rates while addressing practical implementation challenges.

Chapter 3 - The study explores linear N-way Doherty architecture and evaluates trade-offs when scaling to higher-order Doherty configurations, particularly in terms of P_{out}, DE at peak, and PBO, and VSWR resilience. The analysis reveals that beyond a 3-way Doherty configuration, the improvement in average efficiency diminishes when transmitting signals with a 12 dB PAPR, such as OFDM 64-QAM. The 3-way Doherty PA emerges as an optimal candidate, offering higher P_{out} than a 2-way Doherty PA while requiring fewer components than higher-order configurations. However, the limited modulation bandwidth of the 3-way Doherty PA is a drawback.

Chapter 4 - To address the RF bandwidth limitation, a novel output network was developed, featuring three baluns, one inductor, and four capacitors. This balun-first 3-way Doherty PA, fabricated in 40 nm CMOS, operates at 26 GHz and achieves a power gain of 20 dB, a P_{sat} of 20.7 dBm, and DE levels of 39 %, 24.7 %, and 18.1 % at 0 dB, 6 dB, and 9.5 dB PBO, respectively. For a 400 MHz 64-QAM OFDM signal, the PA demonstrates an EVM of −24.9 dB and an ACLR of −28.9 dBc at a P_{avg} of 9.4 dBm and 14 % average efficiency. However, experiments indicate efficiency improvements are limited at deep PBO, due to finite loss from the device's drain-source capacitance (C_{ds}) and channel resistance, especially of the main PA. This effect becomes more pronounced with higher-order linear Doherty designs, as the deep PBO impedance ($N \times R_{opt}$) combines in parallel with these losses, further diminishing back-off efficiency.

Chapter 5 - To achieve higher P_{sat} (close to 0.5 W) and enhanced efficiency at back-off, a novel architecture combining four 2-way Doherty PAs with QHCs was introduced. This design integrates three power-combining techniques: 2-way Doherty combining, isolated combining using QHCs, and non-isolated combining in the current domain. Fabricated in 40 nm CMOS, the PA operates at 28 GHz with a power gain of 25.5 dB, a P_{sat} of 25.2 dBm, and DE levels of 20.5 % and 15.3 % at 0 dB and 6 dB back-off, respectively.

Analysis shows that Doherty PAs exhibit higher nonlinearity compared to traditional class-B PAs, primarily due to AM-PM distortion caused by nonlinear C_{ds}, further amplified by load modulation. This nonlinearity is more severe in higher-order Doherty configurations. Experimental results reveal that incorporating AI-DPD significantly improves performance. For a 1000 MHz 64-QAM OFDM signal, the PA with AI-DPD achieves an EVM of −24.6 dB, ACLR of −32 dBc, P_{avg} of 15.5 dBm, and DE_{avg} of 6 %. Without AI-DPD, the PA achieves an EVM of −25 dB, ACLR of −32 dBc, P_{avg} of 11.5 dBm, and DE_{avg} of 4 %. The QHCs enhance the PA's VSWR resilience, maintaining gain and P_{out} deviations within 1 dB and 0.8 dB, respectively, at P_{1dB} across varying load conditions. This allows an AI-DPD trained at 50 Ω to function effectively under different VSWR conditions while staying within the EVM limit.

6.2. COMPARISON WITH STATE-OF-THE-ART

The experimental results of the balun-first 3-way Doherty PA and the 4 × 2-way Doherty PA are summarized in Fig. 6.1. Using the PA survey in [35], state-of-the-art PAs operating between 20–50 GHz are considered. The CW and modulated results of the proposed output networks are compared with state-of-the-art PAs in Figs. 6.2 and 6.3.

The proposed PA achieves one of the highest gains and P_{sat}, with a DE_{avg} performance comparable to the state-of-the-art. However, peak efficiency falls short of leading designs, leaving room for further optimization. In conclusion, while the proposed architectures demonstrate significant advancements, particularly with AI-DPD assistance, opportunities exist to further improve efficiency and bandwidth to meet the demands of future mm-wave systems.

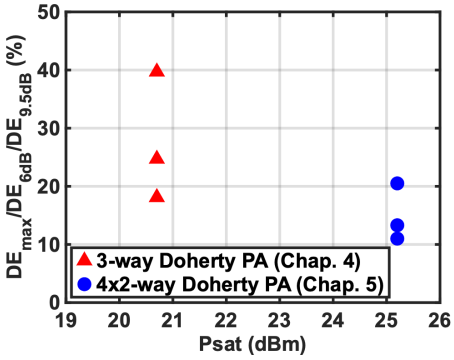


Fig. 6.1. Efficiency versus P_{sat} at 0/6/9.5 dB PBO for the two prototypes presented in the thesis.

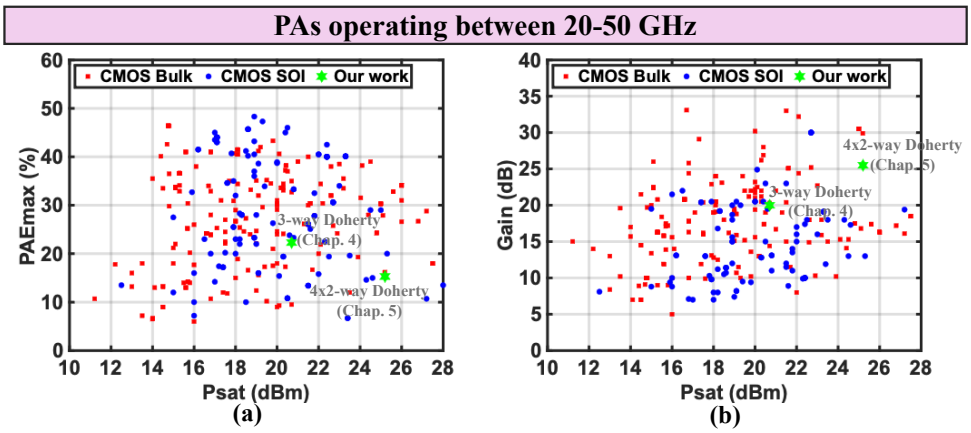


Fig. 6.2. (a) Efficiency versus P_{sat}, and (b) gain versus P_{sat} compared with CMOS PAs operating between 20-50 GHz.

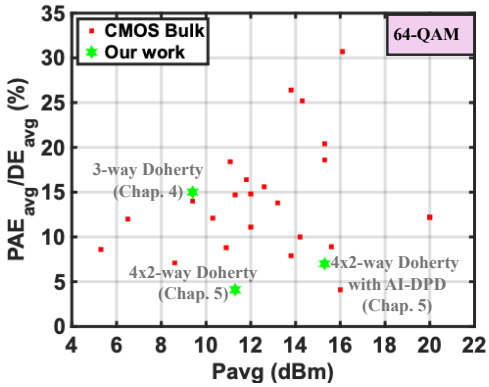


Fig. 6.3. Average efficiency versus P_{avg} compared with CMOS PAs operating between 20-50 GHz.

6.3. THESIS KEY POINTS

From the dissertation, we can conclude the following:

- **Efficiency limitations beyond linear 3-way Doherty:** For an OFDM signal with a PAPR of 12 dB, increasing the order of Doherty PAs beyond three does not improve average efficiency, even with ideal components.

- **Increased output network loss:** Moving from an N-way to an $N+1$-way Doherty PA increases the number of lumped components (inductors and capacitors) by 2, leading to greater output network losses.

- **Back-off efficiency challenges:** Higher-order linear symmetrical N-way Doherty PAs, with their higher impedance ($N \times R_{opt}$), fail to achieve the intended back-off efficiency due to practical limitations such as lossy C_{ds} and finite channel resistance, particularly in the main PA due to its high load modulation.

- **Enhancing back-off efficiency:** The linear N-way Doherty PA simplifies scaling by reusing device sizes but suffers from high load modulation and shunt losses. Back-off efficiency can be improved by adopting asymmetrical Doherty designs with smaller main PAs or by using Doherty schemes with early current saturation for the main and peaking devices in deep PBO. However, these approaches are generally more difficult to linearize due to the early current saturation, requiring heavy DPD for linearity. Additionally, using a higher V_{DD} and more advanced technologies to reduce parasitics helps to improve efficiency.

- **Bandwidth enhancement technique for N-way Doherty:** Bandwidth can be increased by combining high-pass (HP) and LP networks in the transmission lines (TLs) and applying transformations such as the Norton transformation for a compact layout. For the 3-way Doherty, a combination of HP and LP TLs provides superior bandwidth, while for the 2-way Doherty, HP TLs are preferred so the shunt inductor can also serve as the dc feed without adding extra components.

- **Nonlinearity due to AM-PM distortion:** AM-PM distortion significantly contributes to the nonlinearity of Doherty PAs. This arises primarily from load modulation, which causes fluctuations in the phase of the main PA voltage ($\angle V_{main}$) and exacerbates the nonlinearities of device parameters such as g_m, C_{gd}, and C_{gs}. This effect is more pronounced in Doherty PAs compared to traditional class B/AB PAs.
- **Nonlinearity in higher-order designs:** Higher-order N-way Doherty PAs exhibit greater nonlinearity due to the increased impedance transformations required.
- **Optimal power combining:** Achieving a desired P_{out} is best accomplished by combining Doherty with isolated and non-isolated power combining techniques, rather than relying on a single method, which also improves VSWR resilience.
- **Distortion trade-offs in Doherty PAs:** While Doherty PAs enhance efficiency, they inherently suffer from AM-AM and AM-PM distortions. These distortions reduce the P_{avg} because maintaining a certain EVM often requires operating at deep back-off.
- **Linear PAs and EVM performance:** In contrast, linear PAs, although lacking in efficiency enhancement compared to Doherty PAs using early current saturation, excel in EVM performance. This allows them to achieve the required EVM at higher average power, resulting in relatively higher average efficiency.
- **Role of DPD:** digital pre-distortion (DPD) can improve the linearity of Doherty PAs without requiring significant back-off, enabling them to meet EVM requirements and enhance efficiency. However, DPD incurs additional power consumption, which reduces overall system efficiency.
- **Final insights:** While mm-wave Doherty PAs excel in back-off efficiency, linear PAs may offer better overall system performance when low EVM is crucial due to their simpler, low-loss output networks and superior linearity. To maximize transmitter system efficiency, pairing Doherty PAs with DPD is essential, despite the power overhead introduced by DPD.

6.4. RECOMMENDATIONS FOR FUTURE RESEARCH

This dissertation focused entirely on parallel N-way Doherty PAs. However, the insights gained can also be extended to series Doherty architectures. Among N-way series Doherty designs, the 2-way series Doherty emerges as an optimal choice. The schematic of a 2-way series Doherty PA is shown in Fig. 6.4(b) and compared with the 2-way parallel Doherty PA in Fig. 6.4(a). Both designs include a TL, with their respective Z_0 indicated. The current, voltage, and impedance profiles for both the main and peak-1 PAs are illustrated in Fig. 6.4(a)/(b).

For the 2-way series Doherty, the impedance of the main PA varies from R_L to $R_L/2$, while for the 2-way parallel Doherty, it varies from $4R_L$ to $2R_L$. The value of R_L is 3.15 Ω for the 2-way parallel Doherty and 12.62 Ω for the 2-way series Doherty, both designed to achieve a P_{out} of 22 dBm. From Chapter 4, it was observed that R_{Loss}, particularly in

the main PA of parallel Doherty designs, can significantly reduce back-off efficiency. A similar effect is present in series Doherty due to comparable back-off impedance. However, because R_L is higher in the series Doherty, the impedance transformation required to match the antenna impedance (50 Ω) is smaller, inherently improving bandwidth.

Although series Doherty designs require a balun, it can be integrated into the output network, enabling a compact and low-loss implementation [95]. The push-pull architecture used in series Doherty offers additional benefits, such as higher P_{out} and improved device stability through cross-coupled capacitors. To further enhance P_{out}, the series Doherty architecture can be combined with isolated and non-isolated power-combining techniques, as shown in Fig. 6.5. For instance, two Doherty networks on the left can be combined using a QHC, with a similar configuration on the right. Finally, non-isolated power combining can integrate the outputs. This floor plan minimizes the long interconnects presented in the 4 × 2-way parallel Doherty PA (discussed in Chapter 5), improving passive efficiency.

The primary reason for using four 2-way Doherty PAs in Chapter 5 on the same side was to facilitate easier RF input distribution to the PAs with lower loss. To address this in the series Doherty, local oscillator (LO) distribution can be performed at a lower frequency, reducing distribution losses. A frequency multiplier can then be placed near each 2-way series Doherty PA to reach the desired frequency. For instance, LO distribution could occur at 10 GHz, with a multiplier of 3 positioned near the series Doherty

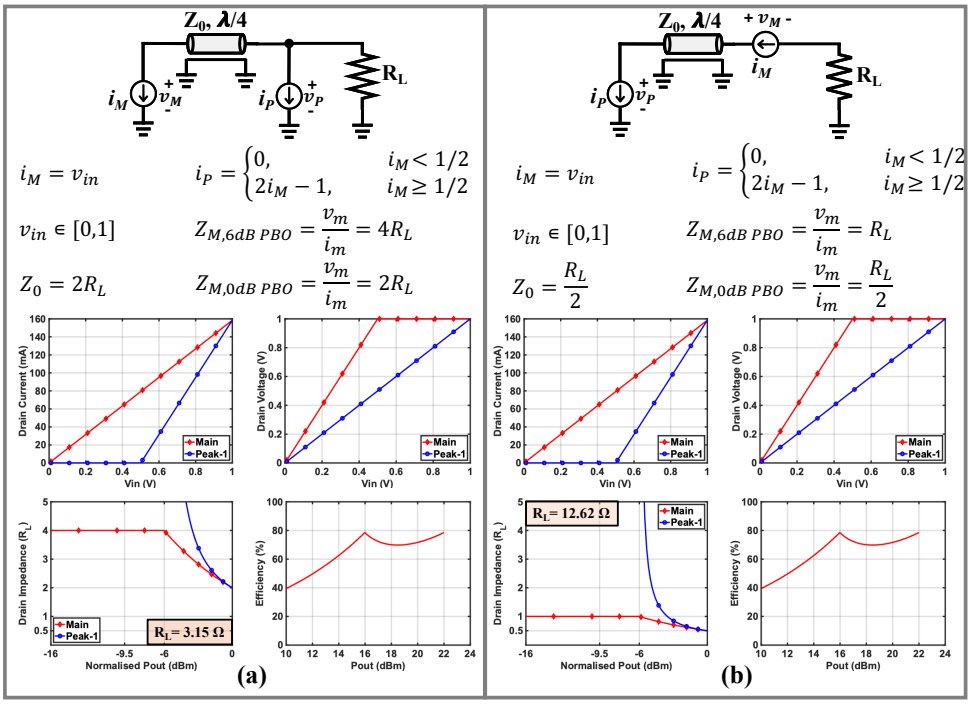


Fig. 6.4. (a) 2-way parallel Doherty and (b) 2-way series Doherty schematics designed to achieve P_{out} = 22 dBm.

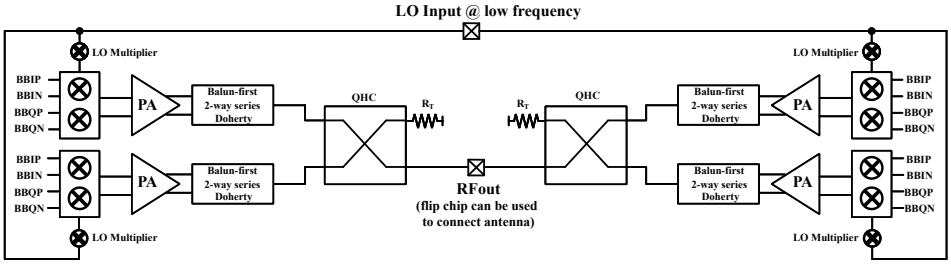


Fig. 6.5. Proposed TX architecture.

PA. The RF output can be centrally located, and the flip-chip technique can be used to connect the antennas [134, 135], further reducing unwanted interconnects.

Future work could focus on implementing a complete 5G TX chain, including the I/Q mixer and baseband signal generation. The phase alignment of the signals from each Doherty PA for coherent combining can be achieved by interchanging baseband (BBIP, BBIN, BBQP, BBQN) and LO (0°/90°) signals within the I/Q mixer.

One potential approach to mitigating output impedance limitations is to increase the gate length of the devices. This improves breakdown voltage and raises the intrinsic output resistance (r_{out}), which can be beneficial for PA robustness. At the same time, the associated trade-offs in gain, efficiency, and parasitics open opportunities for future work in device optimization, hybrid device structures, or circuit techniques that preserve high-frequency performance while leveraging the benefits of longer gates.

In CMOS 40 nm technology, generating around 0.5 W of output power requires combining 6–8 parallel devices. K-port network synthesis provides a promising solution for efficiently combining these outputs with low loss and relatively few components. However, the layout complexity of interconnecting multiple devices introduces new challenges in terms of resistive losses, parasitic effects, and coupling. These challenges highlight directions for future research, particularly in advanced layout optimization, electromagnetic -aware design, and innovative power-combining schemes that can maintain efficiency while scaling output power.

Appendices

A

Design of 2-way Doherty PA

Fig. A.1(b) shows the 2-way Doherty structure using quarter-wavelength TLs. Their characteristic impedances (Z_{13}, and Z_{23}) can be determined by analyzing the circuit's KVL and KCL at the back-off conditions (K_1) and its full (maximum) power. At the first back-off point (K_1), the following conditions are inferred for voltages of the main PA ($V_{m@K_1}$), currents of main PA ($I_{m@K_1}$), and peak-1 PA ($I_{p1@K_1}$):

$$\begin{aligned} V_{m@K_1} &= V_{max} = V_{DD} \\ I_{p1@K_1} &= 0 \\ I_{m@K_1} &= I_{m@F} \cdot K_1 \end{aligned} \tag{A.1}$$

At its maximum power, the following conditions are assumed for voltages of the main PA ($V_{m@F}$), and peak-1 PA ($V_{p1@F}$):

$$V_{m@F} = V_{p1@F} = V_{max} = V_{DD} \tag{A.2}$$

The back-off points can be defined as

$$\begin{aligned} K_1^2 &= \frac{P_{m@K_1}}{P_{total@max}} \\ \text{where, } P_{total@max} &= P_{m@max} + P_{p1@max} \end{aligned} \tag{A.3}$$

Using the (A.1), (A.2), and (A.3), we can calculate ratios of the maximum current carried by main, and peak-1 PAs.

$$\begin{aligned} I_{m@max} : I_{p1@max} &= [K_1 : (1 - K_1)] \cdot I_{max} \\ \text{where, } I_{max} &= I_{m@max} + I_{p1@max} \end{aligned} \tag{A.4}$$

The optimum impedance that a single PA requires to deliver given P_{sat} is:

$$Ropt_{max} = \frac{V_{DD}^2}{2 \cdot P_{sat}} = \frac{V_{DD}}{I_{max}} \tag{A.5}$$

At peak power, the optimum impedances seen by the main, and peak-1 PAs are given by

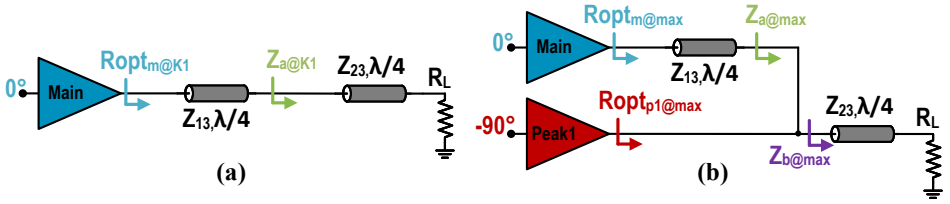


Fig. A.1. 2-way Doherty network at (a) back-off K_1, and (b) peak power.

(A.6), and (A.7).

$$Ropt_{\mathrm{m@max}} = \frac{V_{\mathrm{DD}}}{I_{\mathrm{m@max}}} = \frac{V_{\mathrm{DD}}}{I_{\mathrm{max}} \cdot K_1} = \frac{Ropt_{\mathrm{max}}}{K_1} \tag{A.6}$$

$$Ropt_{\mathrm{p1@max}} = \frac{V_{\mathrm{DD}}}{I_{\mathrm{p1@max}}} = \frac{Ropt_{\mathrm{max}}}{(1-K_1)} \tag{A.7}$$

At back-off K_1, the impedance seen by the main PA can be obtained by using (A.6) and (A.1).

$$Ropt_{\mathrm{m@K_1}} = \frac{V_{\mathrm{m@K_1}}}{I_{\mathrm{m@K_1}}} = \frac{V_{\mathrm{DD}}}{I_{\mathrm{m@max}} \cdot K_1} = \frac{Ropt_{max}}{K_1^2} \tag{A.8}$$

From the schematic in Fig. A.1(a), we can get the following equation:

$$(\frac{Z_{23}}{Z_{13}})^2 = \frac{R_L}{Ropt_{\mathrm{m@K_1}}} = \frac{R_L \cdot K_1^2}{Ropt_{max}} \tag{A.9}$$

The impedance seen by each PA (main, and peak-1) is given by (A.6), and (A.7). From the schematic in Fig. A.1(b), we can obtain the following equation.

$$Z_{23}^2 = R_L \cdot Z_{b@max} \tag{A.10}$$

$$Z_{13}^2 = Ropt_{\mathrm{m@max}} \cdot Z_{a@max} \tag{A.11}$$

$$\frac{1}{Z_{\mathrm{a@max}}} + \frac{1}{Ropt_{\mathrm{p1@max}}} = \frac{1}{Z_{\mathrm{b@max}}} \tag{A.12}$$

Using (A.10), (A.11), and (A.12) can be simplified into

$$\frac{Ropt_{\mathrm{m@max}}}{Z_{13}^2} + \frac{1}{Ropt_{\mathrm{p1@max}}} = \frac{R_L}{Z_{23}^2} \tag{A.13}$$

In this regard, using ((A.9), (A.13), (A.6) and (A.7)), the generalized equations for the characteristic impedance of the two TLs (Z_{13}, and Z_{23}) can be calculated in terms of $Ropt_{\mathrm{max}}$, V_{DD}, R_{L}, and K_1 (A.14).

$$\begin{aligned} Z_{13} &= \frac{Ropt_{\mathrm{max}}}{K_1} \\ Z_{23} &= \sqrt{Ropt_{\mathrm{max}} \cdot R_L} \end{aligned} \tag{A.14}$$

A

The equations for a symmetrical 2-way Doherty, along with their corresponding back-off point ($K_1 = 0.5$) is given below:

$$\begin{aligned} Z_{13} &= 2Ropt_{\max} \\ Z_{23} &= \sqrt{Ropt_{\max} \cdot R_L} \end{aligned} \tag{A.15}$$

Fig. 2.18(a)/(b)/(c) present the voltage, current, and impedance profiles for the main and peak PAs in a symmetrical 2-way Doherty PA. The efficiency curve for the symmetrical 2-way Doherty PA is illustrated in Fig. 2.18(d).

B

Application of Enhanced Bandwidth Technique to 4-Way Doherty PA

In this appendix, the EBW technique introduced in Section 4.3.1 is applied to the 4-way Doherty PA, as illustrated in Fig. B.1(a). Additionally, alternating low-pass (LP) and high-pass (HP) models are employed for the TLs to evaluate their impact on bandwidth. Variations in the 4-way Doherty architecture are depicted in Fig. B.1(b).

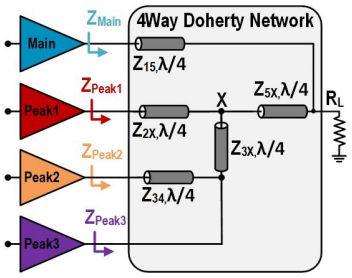
In Version #1, the HP model is applied to all TLs, alongside the lumped-element equivalence shown in Fig. 4.3. Version #2 incorporates the EBW technique on the Z_{15} TL. Versions #3, #4, #5, and #6 are created by alternating between LP and HP models for the Z_{2X}, Z_{34}, Z_{3X} and Z_{5X} TLs.

All simulations are performed using an ideal PA model with a QF of 25/15 for the capacitors and inductors. Fig. B.1(c) presents the drain efficiency (DE) versus output power (P_{out}) at 30 GHz for the different versions. Among these, Versions #3 and #5 emerge as the top performers.

Further results, as shown in Fig. B.2, reveal that version #5 in Fig. B.1(b) outperforms all other versions across frequencies at 12/9.5/4/0 dB PBO. The analysis in Section 4.3.2 indicates that both HP-LP and LP-HP configurations exhibit relatively flat phase responses across frequencies when compared to HP-HP and LP-LP configurations.

Among all the evaluated versions, Version #5 demonstrates superior performance in terms of DE and bandwidth, as highlighted in Fig. B.1(c) and Fig. B.2. This performance can be attributed to its balanced use of LP and HP models for the TLs (Z_{2X}, Z_{34}, Z_{3X} and Z_{5X}) and the application of the EBW technique on the Z_{15} TL. Additionally, Version #5 features a hybrid LP-HP configuration within the peak PAs, reducing phase variation in the equivalent passive network compared to other versions. The placement of an LP structure adjacent to the active power devices helps absorb parasitic C_{ds}.

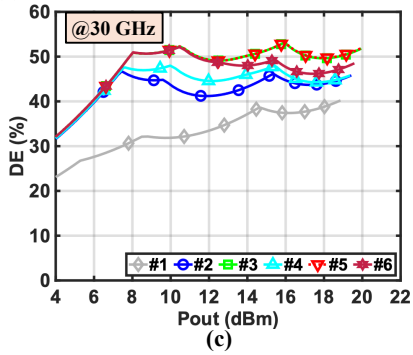
Moreover, the application of the EBW technique results in reduced inductor values, enabling smoother layout implementation and decreased sensitivity to QF effects.



(a)

TL	Z_{15}	Z_{2X}	Z_{34}	Z_{3X}	Z_{5X}
#1	HP	HP	HP	HP	HP
#2	EBW	HP	HP	HP	HP
#3	EBW	LP	LP	LP	HP
#4	EBW	LP	LP	LP	LP
#5	EBW	LP	LP	HP	HP
#6	EBW	LP	HP	HP	HP

(b)



(c)

Fig. B.1. (a) Schematics of 4-way Doherty PA, (b) variations in the 4-way Doherty architecture, and (c) DE vs P_{out} at 30 GHz.

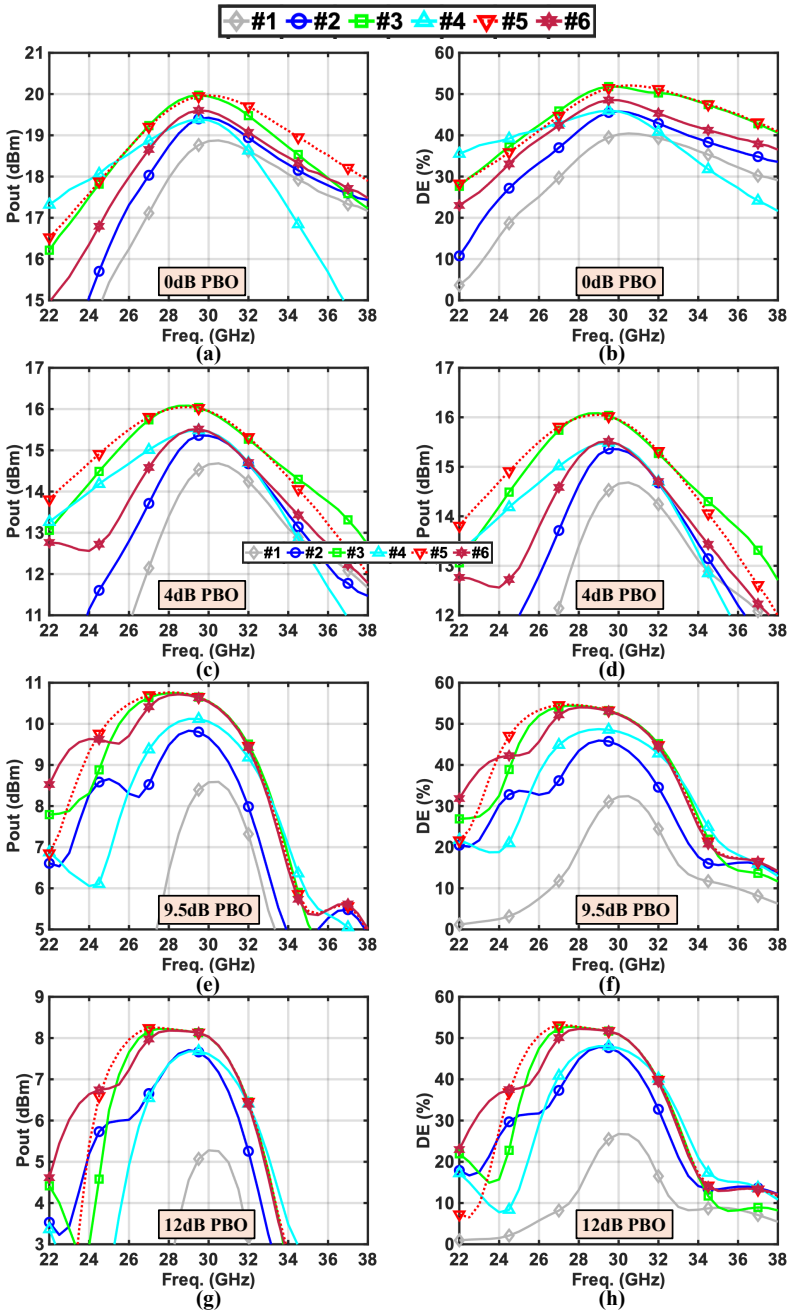


Fig. B.2. (a) P_{out} across frequency at 12 dB PBO, (b) DE across frequency at 12 dB PBO, (c) P_{out} across frequency at 9.5 dB PBO, (d) DE across frequency at 9.5 dB PBO, (e) P_{out} across frequency at 4 dB, (f) DE across frequency at 4 dB PBO, (g) P_{out} across frequency at 0 dB PBO and (h) DE across frequency at 0 dB PBO using QF of 25/15 for capacitors and inductors.

C

Supplementary Material for Linearity Analysis of N-way Doherty

C.1. EVM Analysis

Using the amplitude-to-amplitude (AM-AM) and amplitude-to-phase (AM-PM) transfer characteristics shown in Fig. C.1, the EVM can be calculated, as explained in this appendix. The input QAM signal can be modeled as:

$$V_{in} = \rho \exp^{j\theta} \tag{C.1}$$

where θ is in radians. From the AM-AM and AM-PM transfer curves, we can determine the gain error (α) and phase error (β). For a given V_{in}, we calculate α and multiply it with ρ to obtain the magnitude of V_{out}. Similarly, we compute β and add it to θ to determine the phase of V_{out} (see (C.2)):

$$V_{out} = \rho \cdot \alpha \exp^{j(\theta+\beta)} \tag{C.2}$$

where θ and β are in radians.

Now that we have both V_{in} and V_{out}, we can calculate the EVM. To understand the impact of AM-AM and AM-PM distortions on EVM and spectral purity, we consider three cases, explained below.

C.1.1. Case 1: Ideal AM–AM and Non-Ideal AM–PM

In this case, the ideal AM-AM characteristic (dotted brown line) shown in Fig. C.1(a) is considered for both the standalone class B PA and the N-way Doherty PAs. This implies that the gain error (α) is equal to 1. Only the phase error (β) is calculated, based on the AM-PM characteristics shown in Fig. C.1(b) for the class B PA and N-way Doherty PAs. The equation for V_{out} is given below:

$$V_{in} = \rho \exp^{j(\theta+\beta)} \tag{C.3}$$

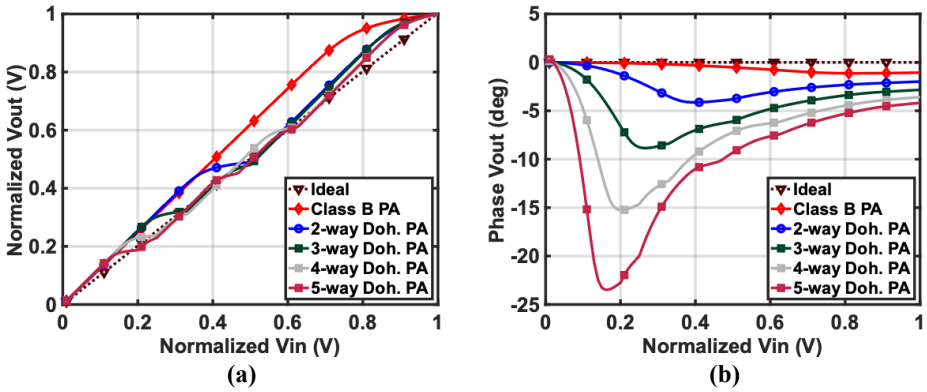


Fig. C.1. (a) AM-AM, and (b) AM-PM of ideal device without nonlinear C_{ds}, N-way Doherty PA with nonlinear C_{ds} and standalone class B PA with nonlinear C_{ds}.

A 500 MHz 64-QAM signal is used to calculate the EVM, assuming ideal AM-AM and non-ideal AM-PM characteristics for both class B and N-way Doherty PAs. From Fig. C.2, it is observed that the EVM degrades when moving from the class B PA to Doherty PAs. Furthermore, higher-order Doherty PAs exhibit worse EVM compared to lower-order configurations. This degradation is attributed to the larger impedance transformation (from NR_{opt} to R_{opt}) in N-way Doherty PAs, as explained in (5.7). The output spectrum for the class B PA and N-way Doherty PAs, considering ideal AM-AM and non-ideal AM-PM characteristics (from Fig. C.1(b)), is shown in Fig. C.3.

C.1.2. CASE 2: IDEAL AM–PM AND NON-IDEAL AM–AM

In this case, the ideal AM–PM characteristic (dotted brown line) shown in Fig. C.1(b) is considered for both the standalone class B PA and the N-way Doherty PAs. This implies that the phase error (β) is zero. Only the gain error (α) is calculated, based on the AM-AM characteristic shown in Fig. C.1(a) for both the class B PA and the N-way Doherty PAs. The equation for V_{out} is given by:

$$V_{in} = \rho \cdot \alpha \exp^{j\theta} \tag{C.4}$$

A 500 MHz 64-QAM signal is used to calculate the EVM, assuming ideal AM-PM and non-ideal AM-AM characteristics. From Fig. C.4, it is observed that the EVM degrades when moving from the class B PA to Doherty PAs. However, in this case, higher-order Doherty PAs show improved EVM compared to lower-order ones. This improvement is due to the smoother AM-AM curves in higher-order Doherty configurations, which avoid sudden jumps or kinks (refer to Fig. C.1(a)). The output spectrum for the class B PA and N-way Doherty PAs under these conditions is also shown in Fig. C.5.

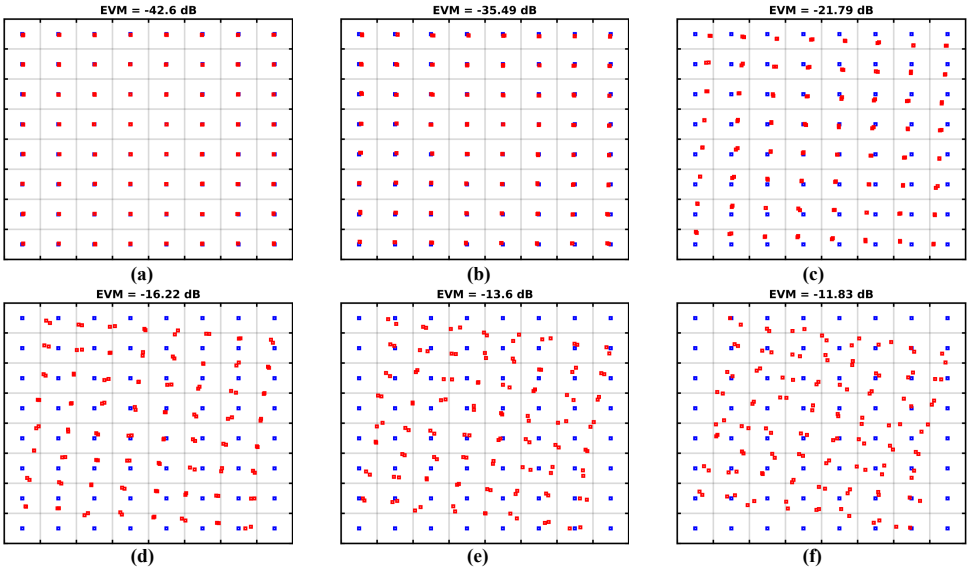


Fig. C.2. (a) Constellation using ideal AM-PM, (b) class B AM-PM, (c) 2-way Doherty AM-PM, (d) 3-way Doherty AM-PM, (e) 4-way Doherty AM-PM, and (f) 5-way Doherty AM-PM.

C.1.3. CASE 3: NON-IDEAL AM–AM AND NON-IDEAL AM–PM

In this case, both the AM-AM (refer to Fig. C.1(a)) and AM-PM (refer to Fig. C.1(b)) characteristics are considered for the standalone class B PA and the N-way Doherty PAs. This means that both the gain error (α) and the phase error (β) are present. The equation for V_{out} is given in (C.2)

A 500 MHz 64-QAM signal is used to calculate the EVM, taking into account both AM-AM and AM-PM distortions for the class B and N-way Doherty PAs. From Fig. C.6, it is observed that the EVM degrades as we move from the class B PA to Doherty PAs. Furthermore, higher-order Doherty configurations exhibit worse EVM compared to lower-order ones. It is also evident that AM-PM distortion contributes more significantly to EVM degradation than AM-AM distortion. The output spectrum for the class B PA and N-way Doherty PAs under these conditions is shown in Fig. C.7.

C.2. TEST WITH TRANSISTOR

Now, the 2-/3-way Doherty output networks shown in Fig. 5.2(a)/(b) are tested using a 40 nm CMOS transistor. The output network is considered ideal, and an inductance L_{ds} is added to resonate out the C_{ds} at a center frequency of 30 GHz. A cascode configuration with a supply voltage of 2 V is employed. The cascode stage consists of five unit cells, each with a transistor aspect ratio of 2 µm/40 nm and 40 fingers. The common-source transistor in the PA comprises eight unit cells, each with 50 fingers and a width of 1 µm.

The 2-way combiner uses the same output network and device sizing as the 2-way Doherty, but with the peak PA always turned on. Fig. C.8(a)/(b) show the AM-AM and

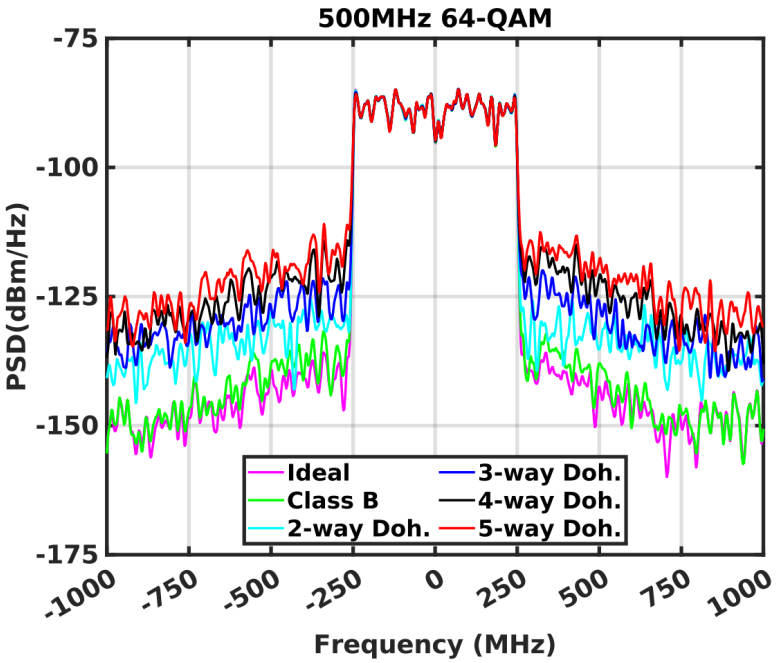


Fig. C.3. Spectrum of class B and 2-/3-/4-/5-way Doherty considering only AM-PM.

AM-PM characteristics of the 2-/3-way Doherty PAs, respectively. AM-PM distortion increases with higher-order Doherty configurations, which aligns with theoretical expectations.

Additionally, in real devices, parameters such as transconductance (g_m), gate-drain capacitance (C_{gd}), and gate-source capacitance (C_{gs}) depend on the gate input voltage and are inherently nonlinear. As a result, load modulation exacerbates these nonlinearities, further increasing the overall distortion in Doherty PAs. Therefore, AM-PM degradation is more pronounced with a real transistor compared to an ideal device with only nonlinear C_{ds}.

Fig. C.9(a)/(b) show the maximum |AM-AM| error and |AM-PM| error errors across frequency. It is observed that the 2-way power combiner has the lowest error, followed by the 2-/3-way Doherty configurations.

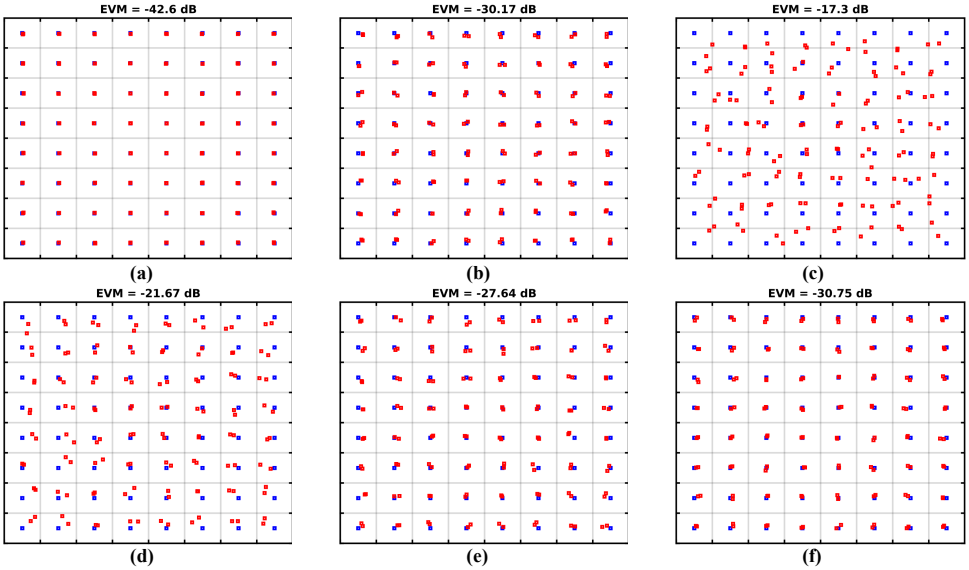


Fig. C.4. (a) Constellation using ideal AM-AM, (b) class B AM-AM, (c) 2-way Doherty AM-AM, (d) 3-way Doherty AM-AM, (e) 4-way Doherty AM-AM, and (f) 5-way Doherty AM-AM.

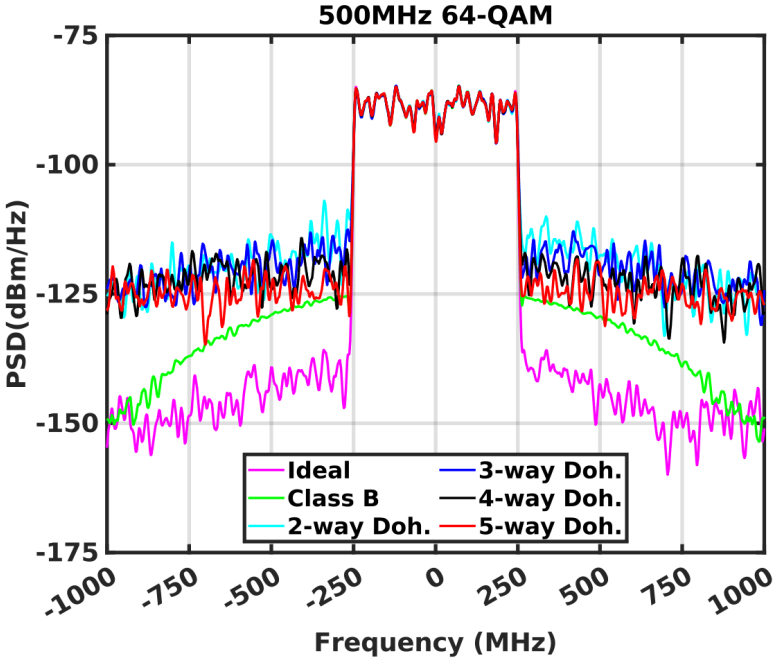


Fig. C.5. Spectrum of class B and 2-/3-/4-/5-way Doherty considering only AM-AM.

C

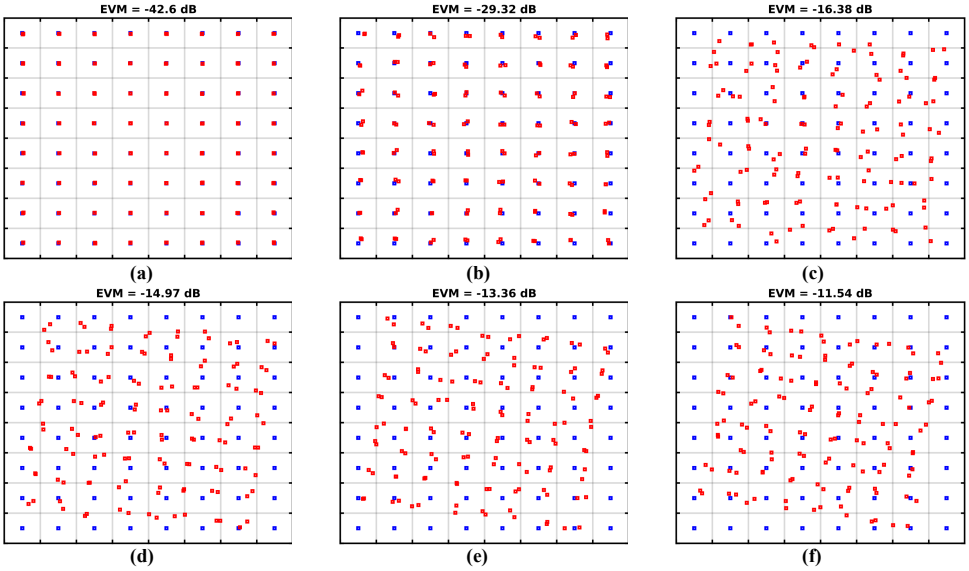


Fig. C.6. (a) Constellation using ideal AM-AM and AM-PM, (b) class B, (c) 2-way Doherty, (d) 3-way Doherty, (e) 4-way Doherty, and (f) 5-way Doherty.

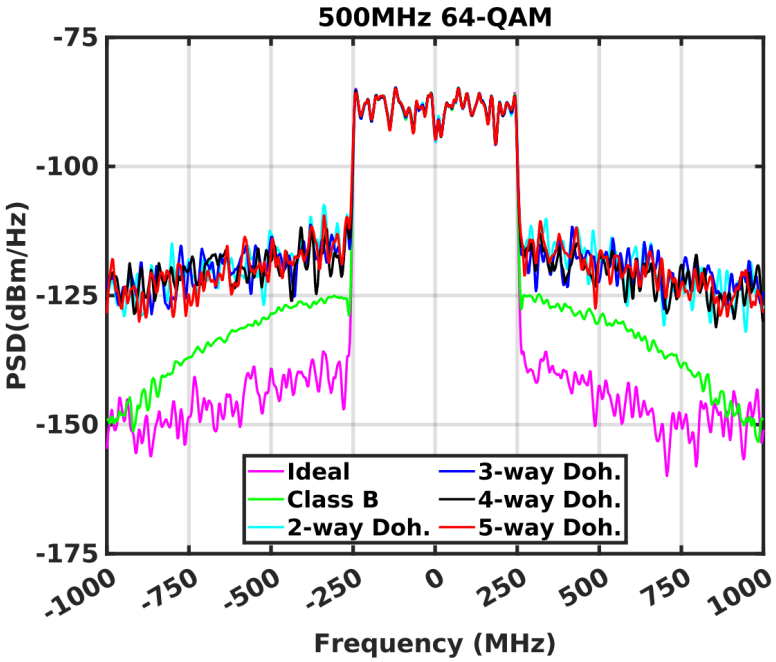


Fig. C.7. Spectrum of class B and 2-/3-/4-/5-way Doherty considering both AM-AM and AM-PM.

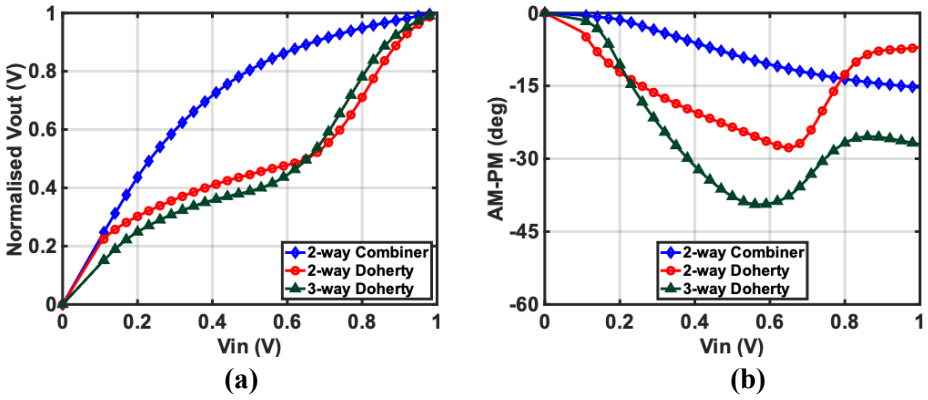


Fig. C.8. (a) AM-AM, and (b) AM-PM of 2-/3-way Doherty PAs and 2-way combiner with ideal output network and CMOS 40 nm transistors.

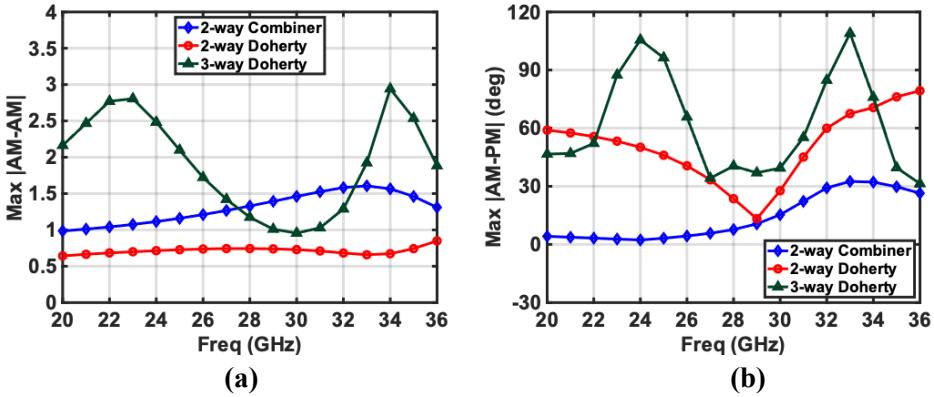


Fig. C.9. (a) Maximum |AM-AM|, and (b) maximum |AM-PM| of 2-/3-way Doherty PAs and 2-way combiner with ideal output network and CMOS 40 nm transistors.

D

Artificial Intelligence Digital Pre-Distortion

The linearization of Doherty PAs typically relies on DPD to approximate the inverse function of the PA. However, conventional DPD methods face challenges in achieving satisfactory linearization performance as modulation bandwidth increases, primarily due to growing memory effects [136].

To address these challenges, this study introduces an off-chip, deep RNN-based AI-DPD framework that employs a GRU regressor for PA modeling and DPD learning [130]. The general implementation of the AI-DPD consists of three processes: data acquisition, algorithm training, and implementation. In this study, the ideal baseband input is generated in MATLAB, passes through the Doherty PA setup, and then the signal is down-converted and digitized by a spectrum analyzer (R&S FSW43). Baseband input and output signals are collected from the proposed mm-wave 4×2-way Doherty PA. To ensure sufficient coverage of adjacent channels and effectively mitigate spurious leakage, the sampling rate must be at least 3–4 times the baseband bandwidth. The algorithm training step relies on the open-source platform OpenDPD offered by [130]. The OpenDPD training process consists of two steps, as illustrated in Fig. D.1.

1. **Step 1**: The acquired baseband PA input and output signals are used to train a GRU-based PA model, denoted as π_{PA}. The training minimizes the discrepancy between the outputs of π_{PA} and the physical PA.

2. **Step 2**: Once training for the GRU-based PA model is complete, the model coefficients of π_{PA} are copied and frozen to prevent further updates. In this step, another GRU-based DPD model, denoted as π_{DPD}, is cascaded with the frozen π_{PA}. Both models share the same GRU-based architecture. The cascaded model is trained using gradient descent to emulate a linear PA with a gain G. This allows π_{DPD} to effectively learn the inverse function of π_{PA} while accounting for memory effects, leveraging the RNN's capability to model time-sequential data.

After obtaining satisfying linearization performance on OpenDPD platform, the algorithm is frozen to generate the predistorted signal $u[t]$ as shown in Fig. D.1. The off-line

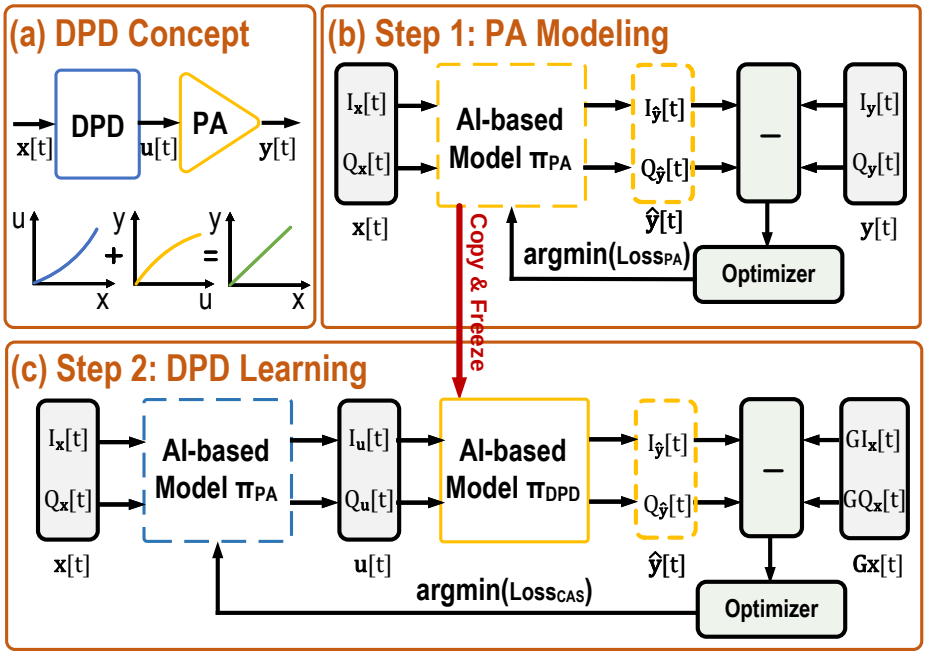


Fig. D.1. (a) Basic Concept of DPD (b) Step 1 of OpenDPD training process: PA Modeling (c) Step 2 of OpenDPD training process: DPD Learning.

deployment utilizes this predistorted signal $u[t]$ as Doherty PA input to test the experimental linearization performance.

D.1. PERFORMANCE ENHANCEMENT OF 4X2-WAY DOHERTY PA USING AI-DPD

A 400 MHz, 64-QAM OFDM signal with a carrier frequency of 28 GHz is applied to the proposed PA. The baseband input and output signals are collected from a 4 × 2-way Doherty PA, with approximately 30 iterations performed to generate the training dataset. This dataset is subsequently used to train the AI-DPD algorithm, which is designed to linearize the PA and enhance its performance.

Fig. D.2 presents the modulated measurements of the 4 × 2-way Doherty PA, both with and without the application of AI-DPD. The AI-DPD model is trained at each power level to optimize linearization across the operating range. As shown in the Fig. D.2, the AI-DPD significantly improves the EVM and ACLR across various power levels.

The output power (P_{out}) required to achieve an EVM of −25 dB increases by at least 5 dB, enabling the Doherty PA to operate closer to saturation. This contributes to achieving a higher average efficiency. Furthermore, the ACLR remains below −35 dBc across all power levels with the assistance of AI-DPD, demonstrating its effectiveness in maintain-

ing spectral compliance and minimizing signal distortion.

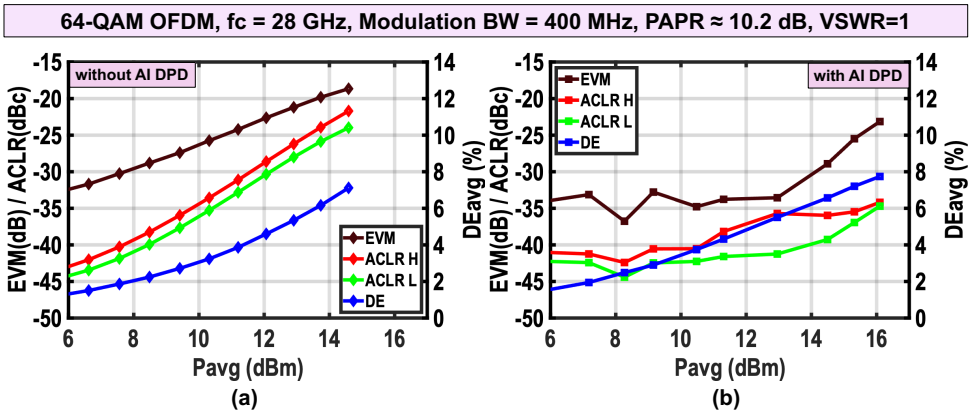


Fig. D.2. EVM/ACLR/DE_{avg} versus P_{avg} for a 400 MHz 64-QAM OFDM signal: (a) With AI-DPD and (b) Without AI-DPD on the 4 × 2-way Doherty PA.

E

PCB Design for Testing and Measurement

This appendix details the printed circuit board (PCB) design of the power board and daughter board, which are used for measuring both chips — the balun-first 3-way Doherty PA and the 4 × 2-way Doherty PA — developed in this dissertation. Since the measurements are performed using probes on a bare die, separating the power board from the daughter board is advantageous. This separation allows the daughter board to be positioned on the vacuum chuck of the probe station, minimizing vibrations and ensuring more stable measurements.

E.1. Measurement boards for balun-first 3-way Doherty PA

E.1.1. Power Board

The power board is designed to generate the required V_{DD} supply and biasing voltages for the main, peak-1, and peak-2 power amplifiers (PAs), drivers (DRVs), and pre-drivers (PDRVs). Its schematic is shown in Figs. E.1 and E.2. To simplify the setup and ensure a common ground, a single 5 V supply is used instead of multiple power supplies.

A LMS1587 low dropout (LDO) regulator (capable of delivering 3 A) converts 5 V to 3.3 V. From this 3.3 V, the V_{DD} supply for the main, peak-1, and peak-2 PAs, DRVs, and PDRVs is derived. Each V_{DD} supply chain includes an additional LDO (ADP1715), a CMOS linear adjustable regulator, which generates 0.8–1.2 V. A potentiometer is used with this LDO to provide adjustable voltage control.

To monitor the current drawn by each amplifier, INA21x current-shunt monitors (also known as current-sense amplifiers) are used. These precision current-measurement devices determine the drain efficiency (DE) and power-added efficiency (PAE) by measuring the voltage difference across a known resistor. The INA212, for example, has a gain of 1000 V/V. The measured voltage, available at jumper (J2), is digitized and read into a PC via a universal serial bus (USB) interface and analog to digital converter (ADC) module (Fig. E.3).

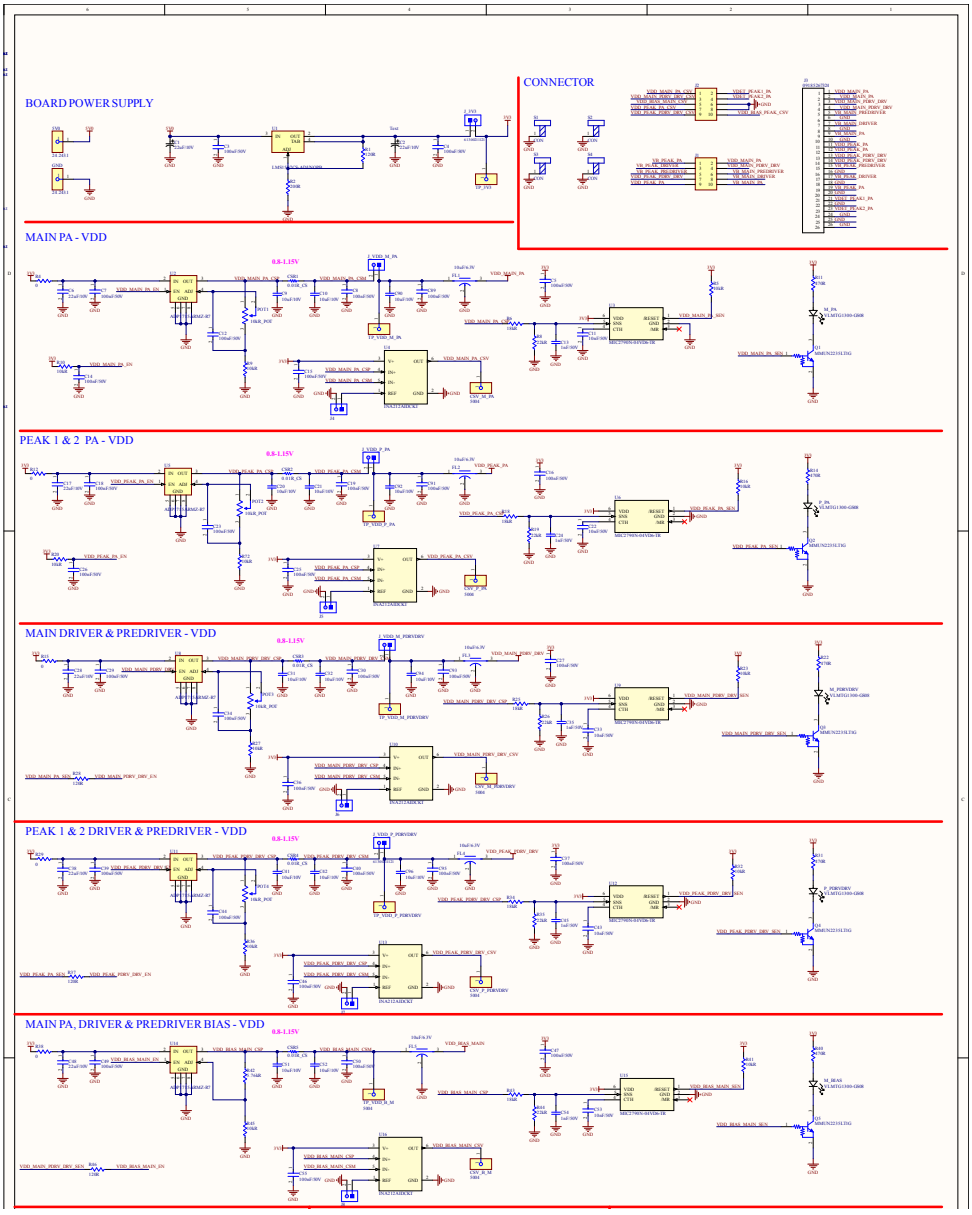


Fig. E.1. Schematics of power board for balun first 3-way Doherty PA (part-1).

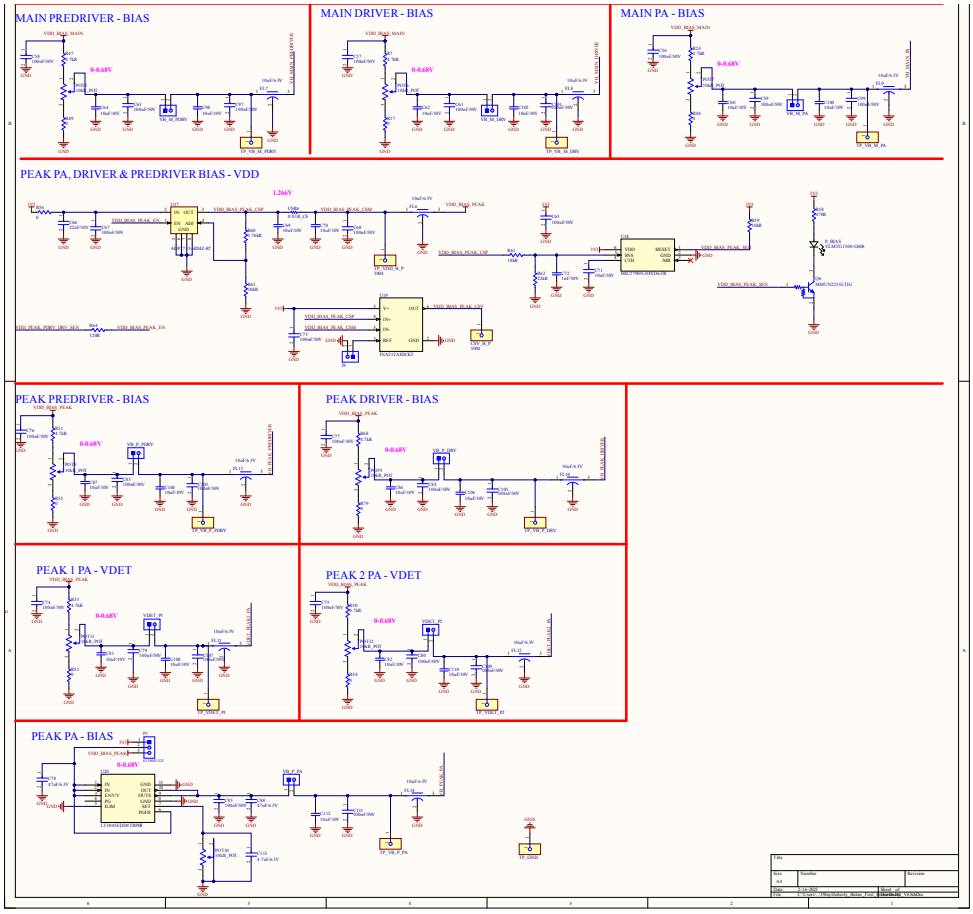


Fig. E.2. Schematics of power board for balun first 3-way Doherty PA (part-2).

A MIC2790N-04VD6-TR voltage supervisor IC ensures proper power sequencing. The V_{DD} for the PA is turned on first, followed by the DRV and PDRV supplies, and finally, the biasing voltages. An light-emitting diode (LED) (VLMTG1300-GS08) indicates when a specified voltage is active.

The biasing circuits for the main PA, main DRV, main PDRV, peak DRV, and peak PDRV use potentiometers to generate voltages in the range of 0–0.68 V. However, the biasing circuit for the peak PA is different—it uses an LT3045EDD LDO to generate 0–0.68 V, ensuring a highly stable voltage source with low impedance to the chip.

The top view and isometric view of the PCB are shown in Fig. E.4(a)/(b), respectively. Jumpers are strategically placed for easier testing and debugging. All voltages and ground connections are routed to a 26-pin jumper (J3), which connects to the daughter board via a flat ribbon cable.

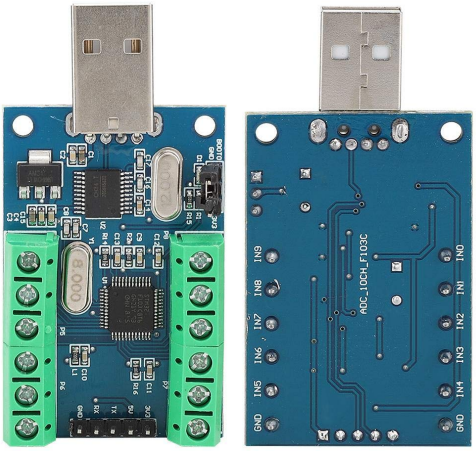
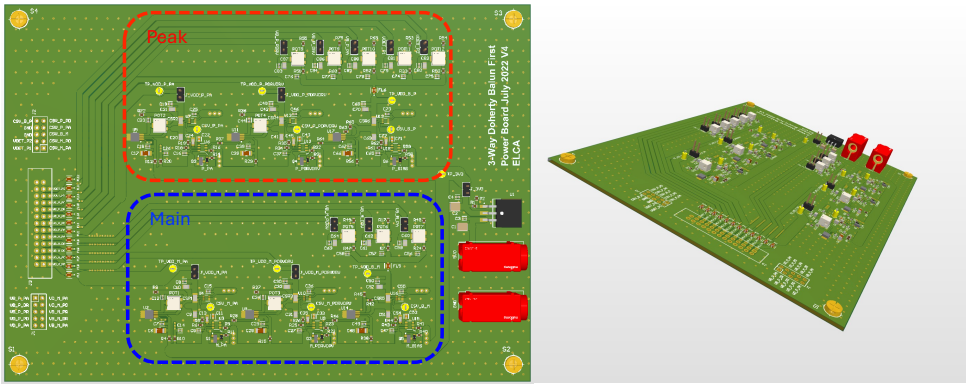


Fig. E.3. STM3210 ADC module.

E.1.2. DAUGHTER BOARD

The schematic of the daughter board is shown in Fig. E.5. It includes decoupling capacitors and a jumper that connects to the power board via a flat ribbon cable. The PCB consists of four layers, where Layers 2 and 4 serve as ground planes to improve signal integrity and reduce electromagnetic interference. Layer 1 is used for signal routing, while Layer 3 distributes different V_{DD} supplies to the amplifiers in the chip.

To ensure power stability and minimize noise, decoupling capacitors of various values are placed in parallel to filter a wide range of frequencies. Large capacitors, such as 10 µF or 47 µF, handle low-frequency noise and provide bulk energy storage, while medium capacitors, like 0.1 µF, filter mid-range frequencies. Small capacitors, such as 10 nF or 1 nF,



(a) **(b)**

Fig. E.4. (a) Top view, and (b) isometric view of the power board PCB for the balun first 3-way Doherty PA.

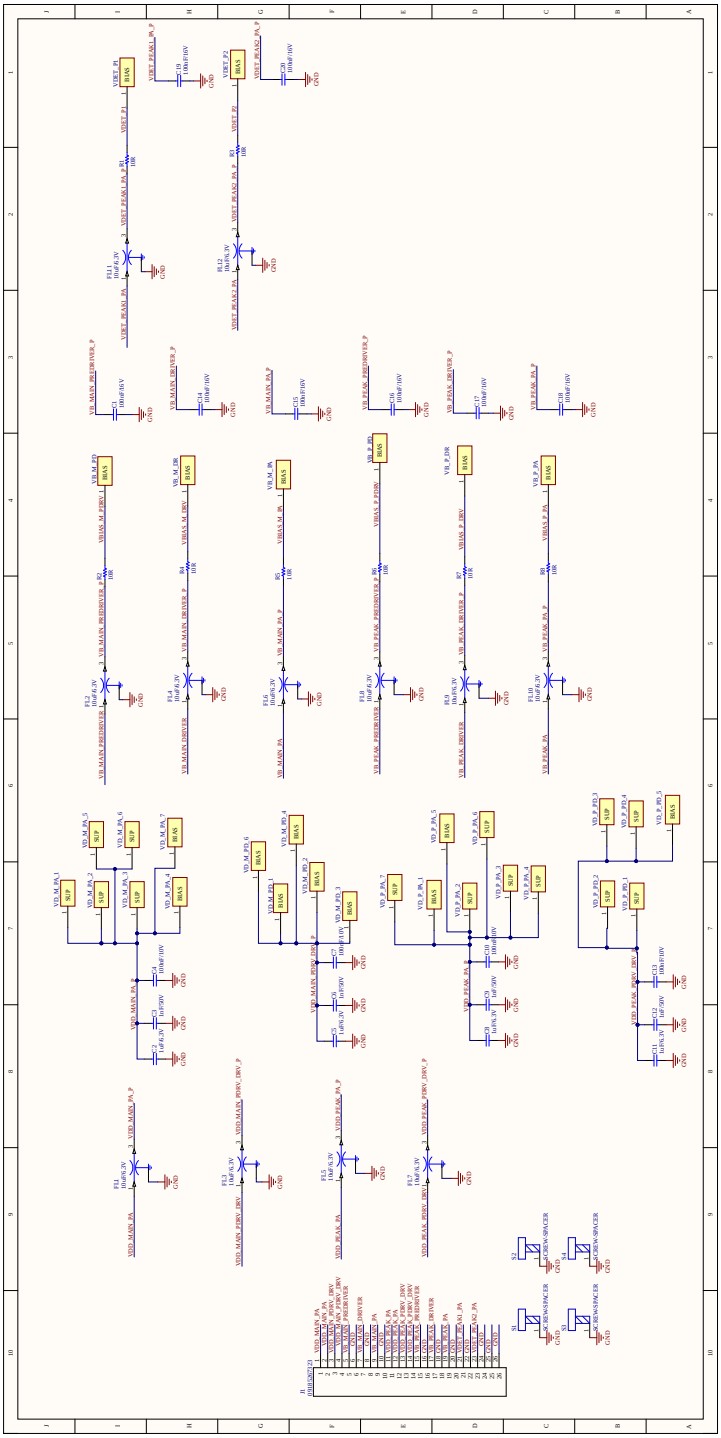


Fig. E.5. Schematic of the daughter board PCB for the balun first 3-way Doherty PA.

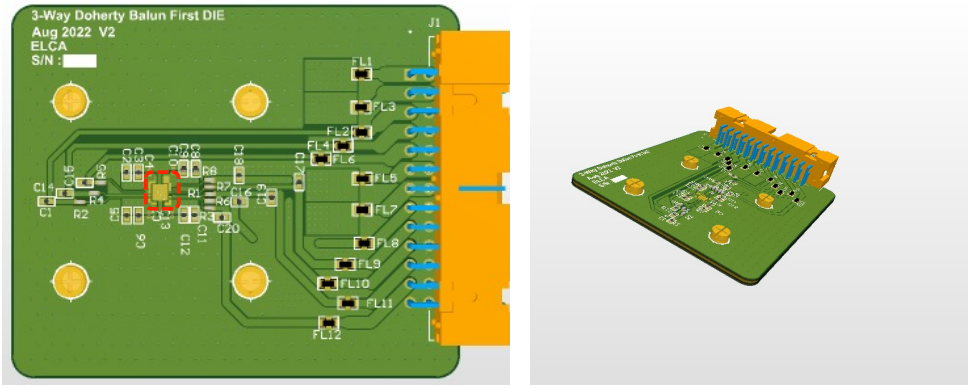


Fig. E.6. (a) Top view, and (b) isometric view of the daughter board PCB for the balun first 3-way Doherty PA.

are effective at high frequencies due to their lower impedance at those ranges. Since no single capacitor can effectively filter all frequencies due to parasitic inductance and resistance, smaller capacitors with lower inductance are included to respond quickly to high-frequency noise. Using multiple capacitor values also enhances stability and transient response, ensuring that sudden current demands are met without voltage drops or spikes that could disrupt sensitive components. These capacitors are placed as close as possible to the power pins of the ICs to minimize inductive effects and maintain power integrity across the board.

The top and isometric views of the daughter board PCB for the balun-first 3-way Doherty PA are shown in Fig. E.6(a)/(b). The bare die is glued to the designated location in Fig. E.6(a) and then wire bonded. To ensure proper placement on the vacuum chuck of the probe station, the daughter board requires a stand at the bottom. Without this, screws and through-hole components would create an uneven base, preventing the PCB from sitting flat on the vacuum chuck.

E.2. MEASUREMENT BOARDS FOR 4 × 2-WAY DOHERTY PA

E.2.1. POWER BOARD

The power board follows a similar design to the previous version, with the key differences being the inclusion of additional voltage domains and the use of a 50-pin connector. The schematic is shown in Figs. E.7 to E.9, while the top view of the PCB is presented in Fig. E.10.

E.2.2. DAUGHTER BOARD

The schematic of the daughter board for measuring the 4 × 2-way Doherty PA is shown in Fig. E.11 and the corresponding PCB layout is presented in Fig. E.12

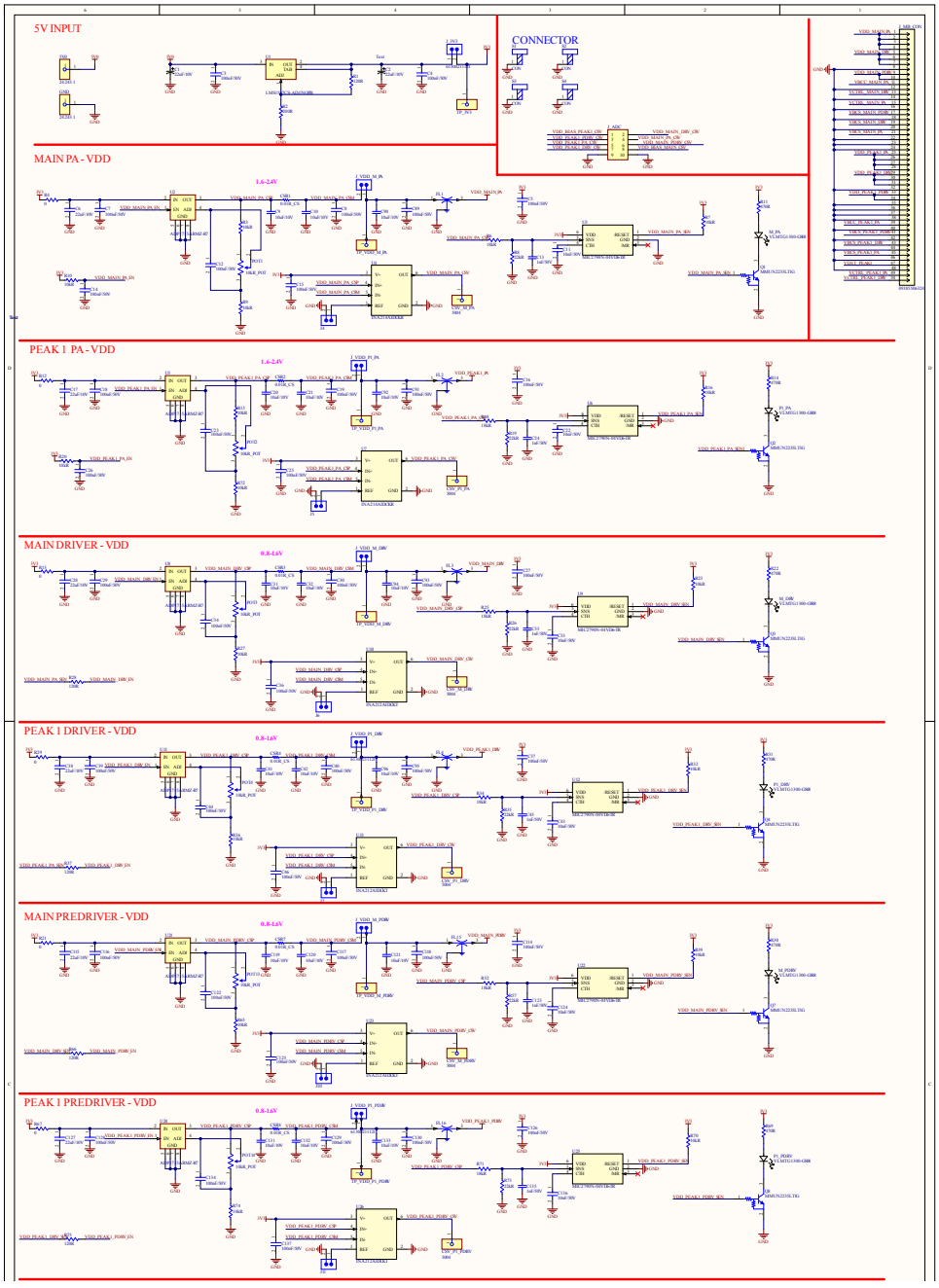


Fig. E.7. Schematic of the power board for the 4 × 2-way Doherty PA (part-1).

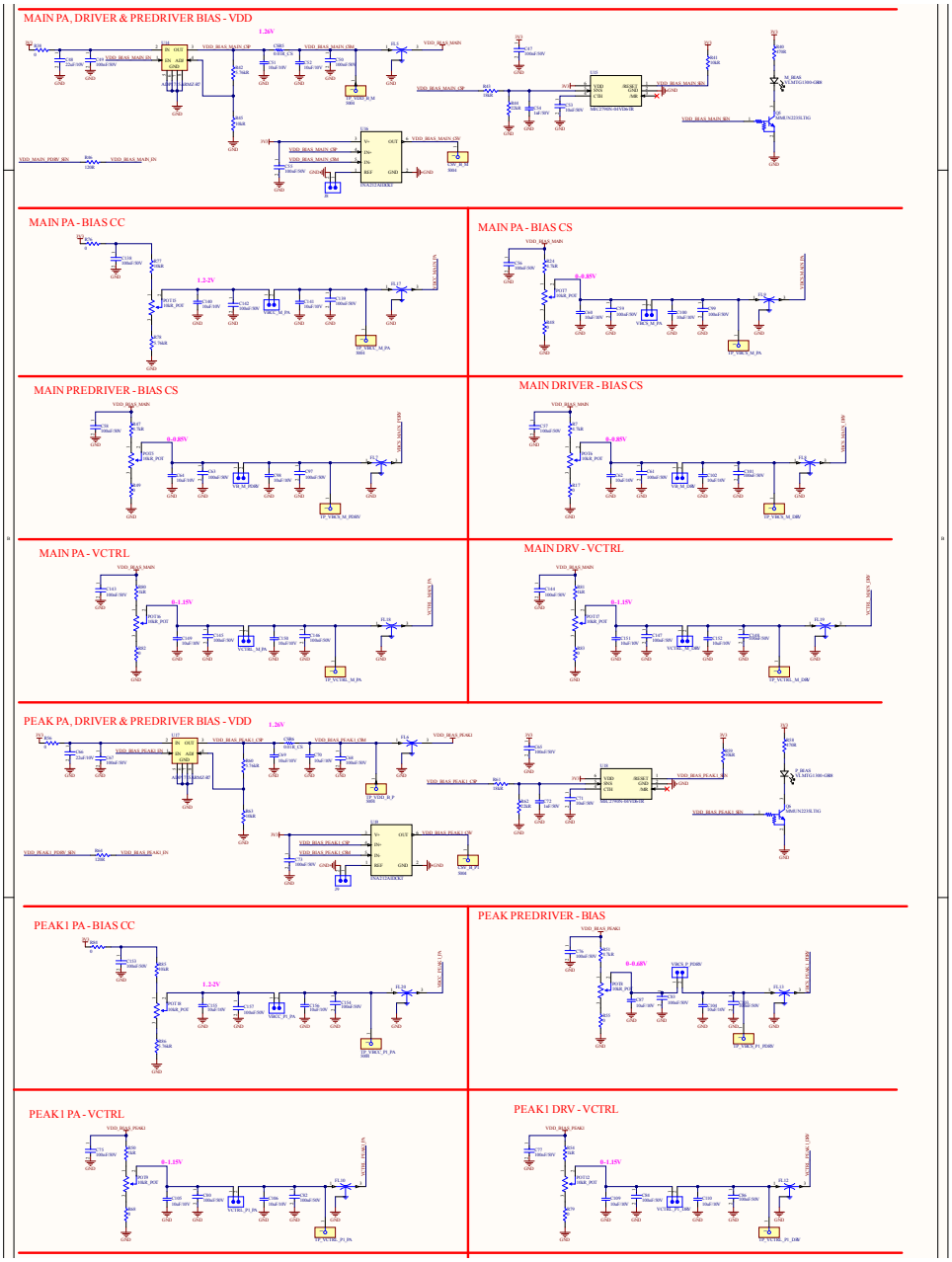


Fig. E.8. Schematic of the power board for the 4 × 2-way Doherty PA (part-2).

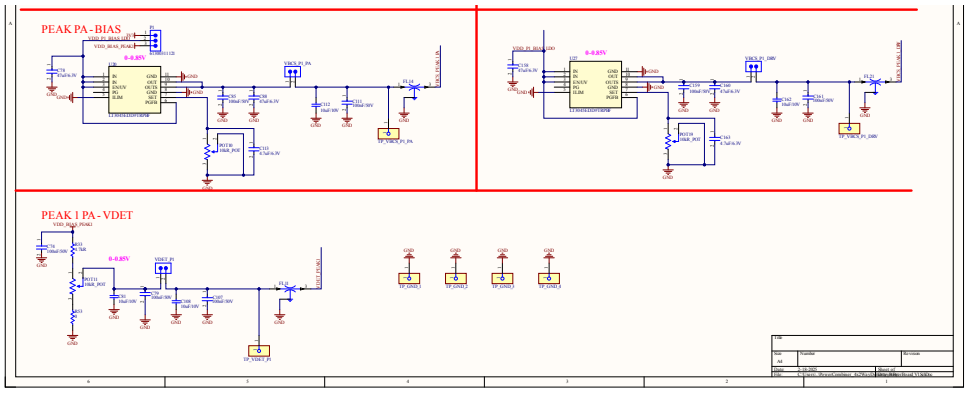


Fig. E.9. Schematic of the power board for the 4 × 2-way Doherty PA (part-3).

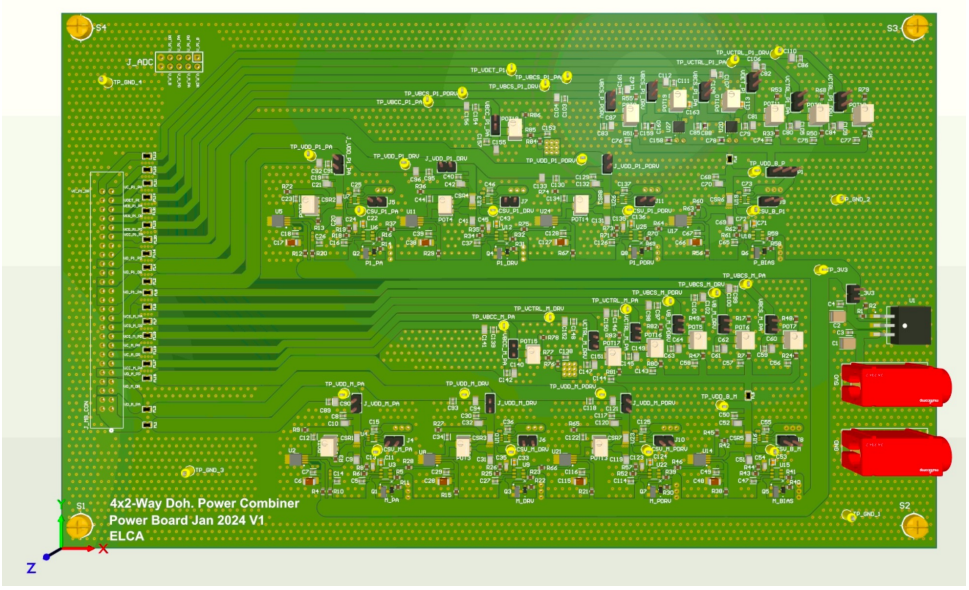


Fig. E.10. Power board PCB for the 4 × 2-way Doherty PA.

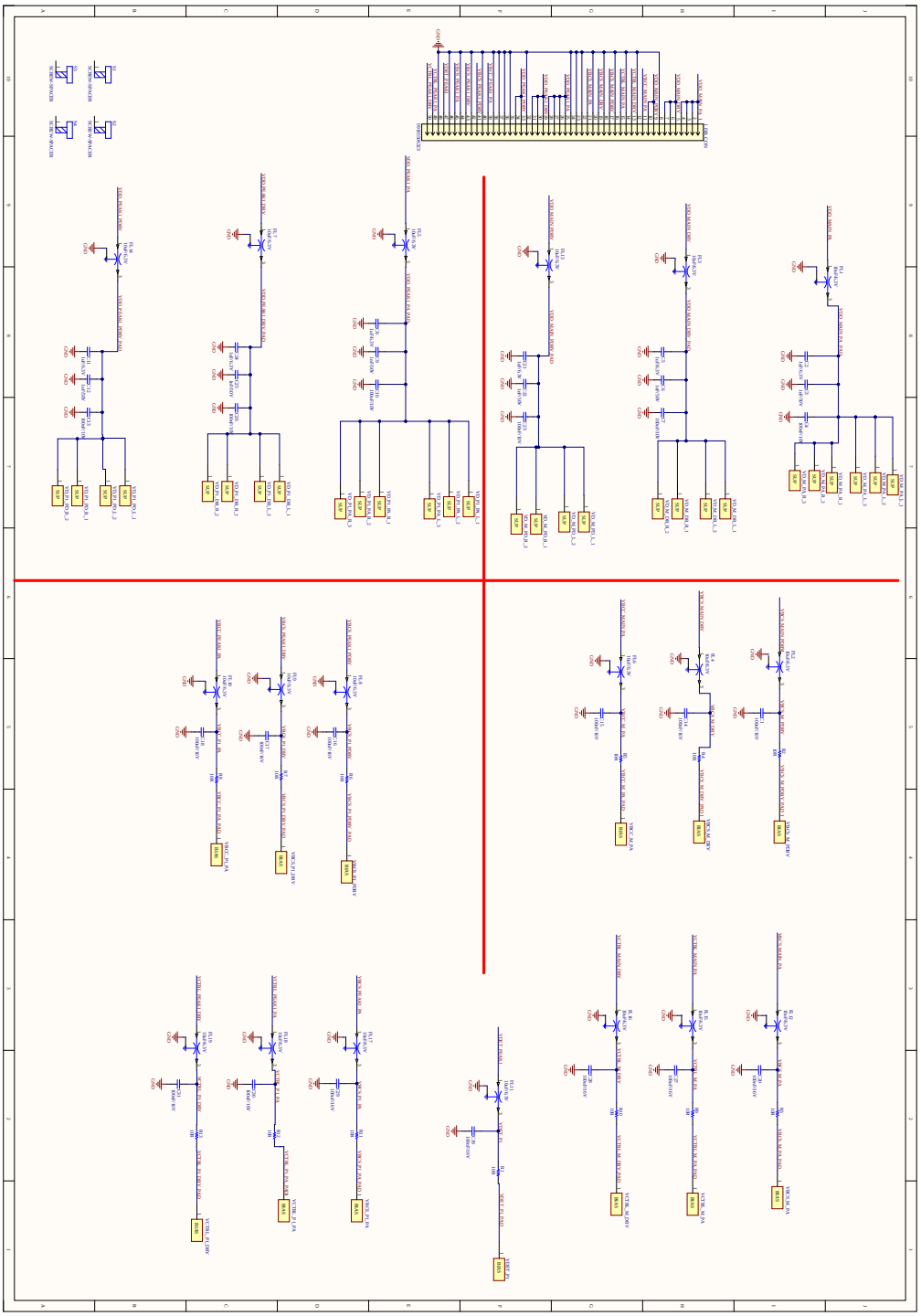


Fig. E.11. Schematic of the daughter board for the 4 × 2-way Doherty PA.

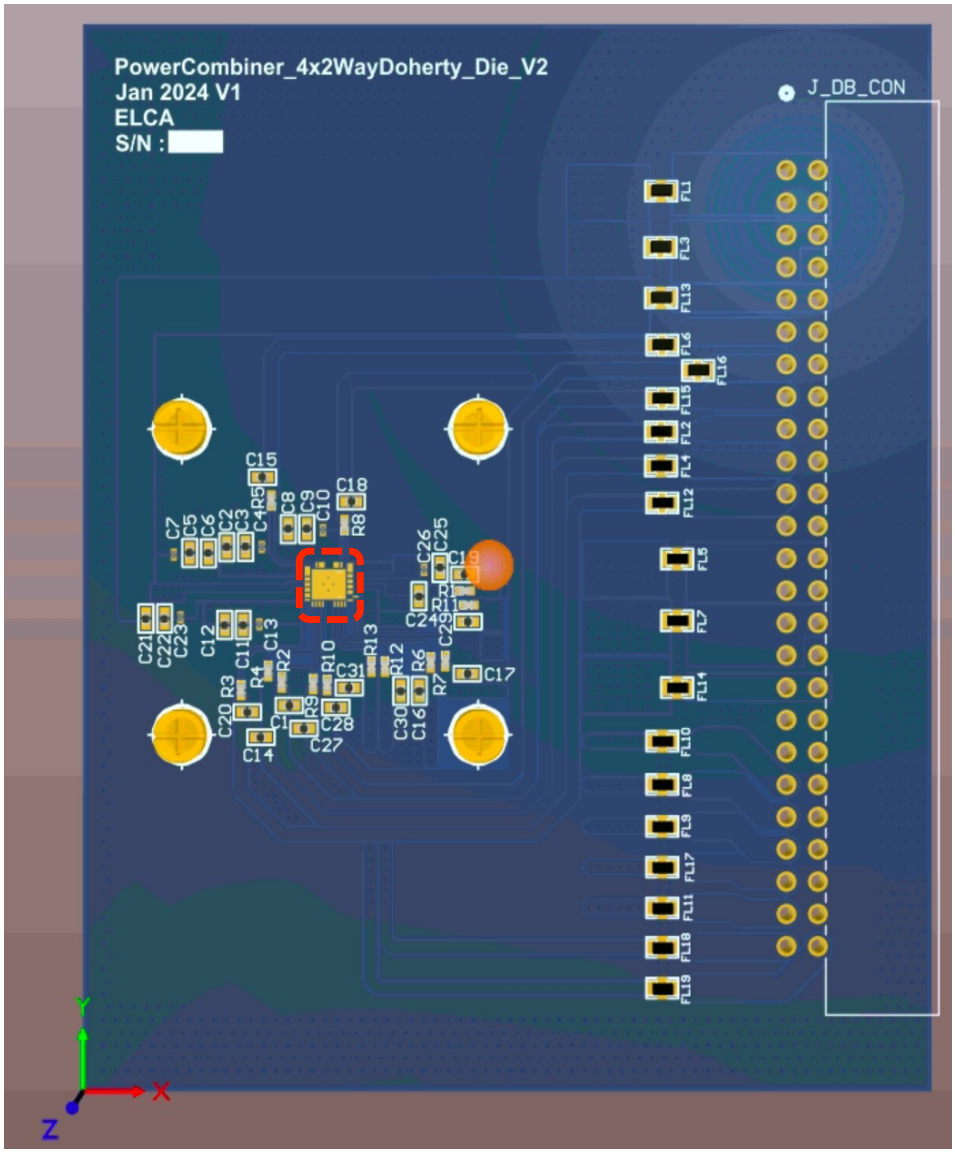


Fig. E.12. Daughter board PCB for the 4 × 2-way Doherty PA.

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List of Publications

Journal Articles

1. **A. K. Kumaran**, Y. Wu, M. Pashaeifar, H. Nachouane, C. Gao, L. Cornelis Nicolaas de Vreede, and M. S. Alavi. "A 4xTwo-Way mm-Wave Doherty CMOS PA". in: *IEEE Trans. Microw. Theory Tech.* 73.10 (2025), pp. 7482–7499. DOI: 10.1109/TMTT.2025.3569155.

2. **A. K. Kumaran**, M. Pashaeifar, M. Alexanderson, L. C. N. d. Vreede, and M. S. Alavi. "A Single-Supply Balun-First Three-Way mm-Wave Doherty PA". in: *IEEE Trans. Microw. Theory Tech.* 72.5 (2024), pp. 2757–2772. DOI: 10.1109/TMTT.2024.3365697

3. M. Pashaeifar, **A. Kumar Kumaran**, L. C. N. de Vreede, and M. S. Alavi. "A Chain-Weaver Balanced Power Amplifier With an Embedded Impedance/Power Sensor". In: *IEEE J. Solid-State Circuits* 59.12 (2024), pp. 3938–3951. DOI: 10.1109/JSSC.2024.3453213

Conference Proceedings

1. **A. K. Kumaran**, M. Pashaeifar, H. M. Nemati, L. C. de Vreede, and M. S. Alavi. "A 26GHz Balun-First Three-Way Doherty PA in 40nm CMOS with 20.7 dBm Psat and 20dB Power Gain". In: *2023 IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*. 2023, pp. 189–192. DOI: 10.1109/RFIC54547.2023.10186161

2. **A. K. Kumaran**, H. M. Nemati, L. C. De Vreede, and M. S. Alavi. "Compact N-Way Doherty Power Combiners for mm-wave 5G Transmitters". In: *2022 IEEE Int. Symp. on Circuits and Syst. (ISCAS)*. 2022, pp. 438–442. DOI: 10.1109/ISCAS48785.2022.9937619

3. **A. K. Kumaran**, M. Pashaeifar, M. D'Avino, L. C. N. de Vreede, and M. S. Alavi. "On-Chip Output Stage Design for a Continuous Class-F Power Amplifier". In: *2021 IEEE Int. Symp. on Circuits and Syst. (ISCAS)*. 2021, pp. 1–5. DOI: 10.1109/ISCAS51556.2021.9401788

4. M. Pashaeifar, **A. K. Kumaran**, L. C. De Vreede, and M. S. Alavi. "32.7 A 25.2dBm PSAT, 35-to-43GHz VSWR-Resilient Chain-Weaver Eight-Way Balanced PA with an Embedded Impedance /Power Sensor". In: *2024 IEEE Int. Solid-State Circuits Conf. (ISSCC)*. vol. 67. 2024, pp. 532–534. DOI: 10.1109/ISSCC49657.2024.10454427

5. M. Pashaeifar, **A. K. Kumaran**, M. Beikmirza, L. C. de Vreede, and M. S. Alavi. "A 24-to-32GHz series-Doherty PA with two-step impedance inverting power combiner achieving 20.4dBm Psat and 38%/34% PAE at Psat/6dB PBO for 5G applications". In: *2021 IEEE Asian Solid-State Circuits Conf. (A-SSCC)*. 2021, pp. 1–3. DOI: 10.1109/A-SSCC53895.2021.9634772

SUMMARY

The ever-increasing demand for data transmission, driven by the need to support global economic growth, is being addressed by fifth-generation (5G) networks. 5G offers several advantages over previous cellular generations, including low network latency, enhanced link robustness, improved mobility, energy efficiency, and superior spectral efficiency. These advancements are expected to have a transformative impact on industries worldwide by creating new job opportunities and boosting productivity.

To achieve multi-Gbit/s data transmission and low-latency line-of-sight links, 5G systems utilize the millimeter-wave (mm-wave) spectrum and advanced modulation schemes such as quadrature amplitude modulation (QAM). The mm-wave spectrum supports large modulation bandwidths that enable higher data rates but suffer from increased signal attenuation. Similarly, spectrally efficient higher-order modulation schemes like QAM improve data rates but require higher signal-to-noise ratio (SNR). By combining mm-wave spectrum usage with complex modulation schemes and phased arrays, 5G networks achieve high-speed, low-latency performance. However, this also imposes stringent requirements on output power (P_{out}), error vector magnitude (EVM), and adjacent channel leakage ratio (ACLR). Additionally, orthogonal frequency-division multiplexing (OFDM) is used in 5G for its high spectral efficiency, immunity to frequency-selective fading, and power efficiency. However, it introduces high peak-to-average power ratio (PAPR) that necessitate efficiency at both peak power and power back-off (PBO) in transmitters (TXs).

Chapter 2 examines the fundamental performance metrics in power amplifier (PA) design, which serves as a critical bottleneck in mm-wave 5G systems. It reviews various PA classes, explores challenges associated with mm-wave operation, and discusses existing solutions. The chapter also introduces design equations for a 2-way Doherty PA and evaluates its operation and performance. While N-way Doherty PAs show promise for achieving required power levels and improving average efficiency in complementary metal-oxide-semiconductor (CMOS) technology, they face limitations such as narrow bandwidth, low gain, nonlinearity, and sensitivity to voltage standing wave ratio (VSWR). These challenges make mm-wave N-way Doherty PAs an active area of research.

Chapter 3 presents a systematic design process for 3-/4-/5-way Doherty networks using transmission lines (TLs) and lumped elements, which can also be extended to N-way configurations. These power combiners are designed and compared using both lossless and lossy components with a quality factor (QF) of 15/25 for inductors/capacitors at 30 GHz, while their PAs are modeled as ideal current sources. Based on this analysis, it reveals that the 3-way network is the most efficient and practical candidate for mm-wave frequencies, requiring fewer components and offering comparable performance to the 4-way configuration.

Chapter 4 introduces a single-supply balun-first 3-way parallel Doherty PA designed

for mm-wave 5G applications. This design incorporates a bandwidth enhancement technique to broaden the operational frequency range, improve broadband PBO efficiency, and reduce impedance mismatches. Realized in 40 nm CMOS bulk technology with a core area of 0.77 mm^2, the prototype achieves a P_{sat}/peak gain of over 20 dBm/16 dB and demonstrates a drain efficiency (DE) of 15 %/22 %/33 % at 9.5 dB/6 dB /0 dB PBO across a 24–30 GHz band. It supports 64-QAM OFDM signals with an EVM/ACLR of −24.3 dB/ −30.1 dBc at 9.4 dBm average output power (P_{avg}) and achieves promising results with 1024-QAM signals. However, the 3-way Doherty PAs show efficiency limitations compared to 2-way Doherty PAs at 9.5 dB PBO due to finite QF of the drain-source capacitance (C_{ds}), device channel resistance, and higher passive losses of the output network.

Chapter 5 describes a 4 × 2-way Doherty PA designed for mm-wave 5G applications. Featuring an advanced output combiner with four differential 2-way Doherty networks, two quadrature hybrid couplers (QHCs), and a balun, this design enhances P_{out} and PBO efficiency. Realized in 40 nm CMOS bulk technology with a core area of 1.54 mm^2, the prototype achieves a P_{sat}/peak gain of 25.2 dBm/25.5 dB and a DE of 17.5 %/10 % at 0 dB/6 dB PBO across a 26–32 GHz band. It delivers exceptional EVM/ACLR performance for both 64-QAM and 1024-QAM OFDM signals and demonstrates resilience to VSWR variations. By incorporating artificial intelligence digital pre-distortion (AI-DPD), the PA achieves a P_{avg} of 15.3 dBm for 400 MHz 64-QAM signals, making it a strong candidate for 5G mm-wave TXs or phased arrays.

Chapter 6 summarizes the findings of the thesis, compares them with the state-of-the-art, and highlights key conclusions. It also suggests future research directions, such as a novel floor plan for the TX chain. This includes the use of four 2-way series Doherty PAs to achieve high output power and improved PBO efficiency. Additionally, flip-chip integration is proposed to position antenna connection pads centrally, reducing interconnect parasitics and unwanted losses.

SAMENVATTING

De steeds toenemende vraag naar gegevensoverdracht, gedreven door de noodzaak om de wereldwijde economische groei te ondersteunen, wordt aangepakt door netwerken van de vijfde generatie (5G). 5G biedt verschillende voordelen ten opzichte van eerdere mobiele generaties, waaronder lage netwerklatentie, verbeterde linkrobuustheid, verbeterde mobiliteit, energie-efficiëntie en superieure spectrale efficiëntie. Deze ontwikkelingen zullen naar verwachting een transformerende impact hebben op industrieën wereldwijd door nieuwe banen te creëren en de productiviteit te verhogen.

Om multi-Gbit/s datatransmissie en line-of-sight-verbindingen met lage latentie te bereiken, maken 5G-systemen gebruik van het millimetergolfspectrum (mm-wave) en geavanceerde modulatieschema's zoals kwadratuuramplitudemodulatie (QAM). Het mm-wavespectrum ondersteunt grote modulatiebandbreedtes die hogere datasnelheden mogelijk maken, maar lijden aan verhoogde signaalverzwakking. Op dezelfde manier verbeteren spectraal efficiënte hogere-orde modulatieschema's zoals QAM datasnelheden, maar vereisen ze een hogere signaal-ruisverhouding (SNR). Door het gebruik van mm-wavespectrum te combineren met complexe modulatieschema's en gefaseerde arrays, bereiken 5G-netwerken hogesnelheidsprestaties met lage latentie. Dit stelt echter ook strenge eisen aan het uitgangsvermogen (Pout), de grootte van de foutvector (EVM) en de aangrenzende kanaallekverhouding (ACLR). Daarnaast wordt orthogonale frequentieverdelingmultiplexing (OFDM) in 5G gebruikt vanwege de hoge spectrale efficiëntie, immuniteit tegen frequentieselectieve vervaging en energie-efficiëntie. Het introduceert echter wel een hoge piek-gemiddelde vermogensverhouding (PAPR) die efficiëntie vereist bij zowel piekvermogen als vermogensafname (PBO) in zenders (TXs).

Hoofdstuk 2 onderzoekt de fundamentele prestatiemetingen in het ontwerp van vermogensversterkers (PAs), die een kritiek knelpunt vormen in mm-wave 5G-systemen. Het bespreekt verschillende PA-klassen, onderzoekt uitdagingen die verband houden met mm-wave-werking en bespreekt bestaande oplossingen. Het hoofdstuk introduceert ook ontwerpvergelijkingen voor een 2-weg Doherty PA en evalueert de werking en prestaties ervan. Hoewel N-way Doherty PAs veelbelovend zijn voor het bereiken van vereiste vermogensniveaus en het verbeteren van de gemiddelde efficiëntie in complementaire metaaloxide-halfgeleider (CMOS)-technologie, hebben ze te maken met beperkingen zoals smalle bandbreedte, lage versterking, niet-lineariteit en gevoeligheid voor spanningsstaande golfverhouding (VSWR). Deze uitdagingen maken mm-wave N-way Doherty PAs een actief onderzoeksgebied.

Hoofdstuk 3 presenteert een systematisch ontwerpproces voor 3-/4-/5-weg Doherty-netwerken met behulp van transmissielijnen (TLs) en samengevoegde elementen, die ook kunnen worden uitgebreid naar N-wegconfiguraties. Deze vermogenscombinatoren zijn ontworpen en vergeleken met behulp van zowel verliesloze als verliesgevende componenten met een kwaliteitsfactor (QF) van 15/25 voor inductoren/condensatoren op

30 GHz, terwijl hun PAs zijn gemodelleerd als ideale stroombronnen. Op basis van deze analyse blijkt dat het 3-wegnetwerk de meest efficiënte en praktische kandidaat is voor mm-golffrequenties, waarbij minder componenten nodig zijn en vergelijkbare prestaties worden geboden als de 4-wegconfiguratie.

Hoofdstuk 4 introduceert een single-supply balun-first 3-way parallel Doherty PA ontworpen voor mm-wave 5G-toepassingen. Dit ontwerp omvat een bandbreedteverbeteringstechniek om het operationele frequentiebereik te verbreden, de efficiëntie van breedband-PBO te verbeteren en impedantiemismatches te verminderen. Gerealiseerd in 40 nm CMOS-bulktechnologie met een kernoppervlak van 0.77 mm^2, bereikt het prototype een Psat/piekversterking van meer dan 20 dBm/16 dB en toont een drain efficiency (DE) van 15 %/22 %/33 % bij 9.5 dB/6 dB/0 dB PBO over een 24-30 GHz-band. Het ondersteunt 64-QAM OFDM-signalen met een EVM/ACLR van −24.3 dB/−30.1 dBc bij 9.4 dBm gemiddeld uitgangsvermogen (Pavg) en behaalt veelbelovende resultaten met 1024-QAM-signalen. De 3-weg Doherty PAs vertonen echter efficiëntiebeperkingen vergeleken met 2-weg Doherty PAs bij 9.5 dB PBO vanwege de eindige QF van de drain-sourcecapaciteit (Cds), de kanaalweerstand van het apparaat en hogere passieve verliezen van het uitgangsnetwerk.

Hoofdstuk 5 beschrijft een 4 × 2-weg Doherty PA die is ontworpen voor mm-wave 5G-toepassingen. Met een geavanceerde outputcombiner met vier differentiële 2-weg Doherty-netwerken, twee kwadratuurhybridekoppelingen (QHCs) en een balun verbetert dit ontwerp de Pout- en PBO-efficiëntie. Gerealiseerd in 40 nm CMOS-bulktechnologie met een kernoppervlak van 1.54 mm^2, bereikt het prototype een Psat/piekversterking van 25.2 dBm/25.5 dB en een DE van 17.5 %/10 % bij 0 dB/6 dB PBO over een 26-32 GHz-band. Het levert uitzonderlijke EVM/ACLR-prestaties voor zowel 64-QAM- als 1024-QAM OFDM-signalen en toont veerkracht tegen VSWR-variaties. Door het integreren van kunstmatige intelligentie digitale pre-distortion (AI-DPD) behaalt de PA een Pavg van 15.3 dBm voor 400 MHz 64-QAM-signalen, wat het een sterke kandidaat maakt voor 5G mm-wave TXs of gefaseerde arrays.

Hoofdstuk 6 vat de bevindingen van het proefschrift samen, vergelijkt ze met de stand van de techniek en benadrukt belangrijke conclusies. Het suggereert ook toekomstige onderzoeksrichtingen, zoals een nieuw plattegrondplan voor de TX-keten. Dit omvat het gebruik van vier 2-weg series Doherty PAs om een hoog uitgangsvermogen en verbeterde PBO-efficiëntie te bereiken. Bovendien wordt flip-chip-integratie voorgesteld om antenneverbindingspads centraal te positioneren, waardoor interconnect-parasieten en ongewenste verliezen worden verminderd.

ACRONYMS

Γ reflection coefficient

$\mathbf{C_{ds}}$ drain-source capacitance

$\mathbf{C_{gd}}$ gate-drain capacitance

$\mathbf{C_{gs}}$ gate-source capacitance

$\mathbf{DE_{avg}}$ average drain efficiency

$\mathbf{DE_{sat}}$ saturated drain efficiency

$\mathbf{f_T}$ cut-off frequency

$\mathbf{F_{max}}$ maximum oscillation frequency

$\mathbf{PAE_{sat}}$ saturated power-added efficiency

$\mathbf{P_{1dB}}$ output power at 1dB compression

$\mathbf{P_{avg}}$ average output power

$\mathbf{P_{out}}$ output power

$\mathbf{P_{sat}}$ saturated output power

$\mathbf{R_L}$ load

$\mathbf{R_{opt}}$ optimum impedance

$\mathbf{V_{DD}}$ supply source

$\mathbf{V_{det}}$ turn-on voltage

$\mathbf{Z_0}$ characteristic impedance

g_m transconductance

V_{in} input voltage

V_{TH} threshold voltage

3GPP 3rd Generation Partnership Project

5G fifth-generation

ac alternating current

ACLR adjacent channel leakage ratio

ADC analog to digital converter

ADS Advanced Design System

AI-DPD artificial intelligence digital pre-distortion

AM-AM amplitude-to-amplitude

AM-PM amplitude-to-phase

AWG arbitrary waveform generator

balun balanced-to-unbalanced

BER bit error rate

BiCMOS Bipolar CMOS

BPA balanced PA

BPSK binary phase shift keying

CCF continuous class F

CMOS complementary metal-oxide-semiconductor

CSP control signal power

CW continuous wave

DAC digital-to-analog converter

DAT distributed active transformer

dc direct current

DE drain efficiency

DPD digital pre-distortion

DRV driver

DSP digital signal processing

DUC direct up-conversion

EBW enhanced bandwidth

ECCF extended continuous class F

EIRP equivalent isotropically radiated power

EM electromagnetic

ET envelope tracking

EVM error vector magnitude

FD-SOI fully depleted silicon-on-insulator

GaAs gallium arsenide

GaN gallium nitride

GRU gated recurrent unit

HEMT high-electron-mobility transistor

HP high-pass

I/Q in-phase/quadrature

IC integrated circuit

IL insertion loss

IMD inter-modulation distortion

KCL Kirchhoff's Current Law

KPI key performance indicator

KVL Kirchhoff's Voltage Law

LDO low dropout

LED light-emitting diode

LMBA load-modulated balanced amplifier

LO local oscillator

LOFT local oscillator feedthrough

LP low-pass

LPF low-pass filter

MIMO multiple-input multiple-output

mm-wave millimeter-wave

mMIMO massive multiple-input multiple-output

MOSFET metal-oxide-semiconductor field-effect transistor

NR new radio

OFDM orthogonal frequency-division multiplexing

PA power amplifier

PAE power-added efficiency

PAPR peak-to-average power ratio

PBO power back-off

PCB printed circuit board

PDF probability distribution function

PDRV pre-driver

PE passive efficiency

pHEMT pseudomorphic high-electron-mobility transistor

PN phase noise

QAM quadrature amplitude modulation

QF quality factor

QHC quadrature hybrid coupler

QN quantization noise

QPSK quadrature phase shift keying

QTL quarter-wave transmission line

RF radio frequency

RNN recurrent neural network

SC single carrier

SE single-ended

SFDR spurious free dynamic range

SiGe silicon germanium

SNR signal-to-noise ratio

SoC system on chip

SOI silicon-on-insulator

TL transmission line

TX transmitter

USB universal serial bus

VCO voltage controlled oscillator

VSWR voltage standing wave ratio

WiFi Wireless Fidelity

ZCS zero-current switching

ZVS zero-voltage switching

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About the Author

Anil Kumar Kumaran received the B.Tech. degree in Electronics and Communication Engineering from Amrita Vishwa Vidyapeetham, Coimbatore, India, in May 2015, and the M.Sc. degree in Microelectronics from Delft University of Technology, Delft, the Netherlands, in August 2020. He worked as a Validation Engineer at Texas Instruments India before joining the ELCA research group at Delft University of Technology for his master's studies. He subsequently pursued his Ph.D. research in the same group. His research focused primarily on the design of linear and efficient mm-wave power amplifiers for 5G cellular applications. He is currently working at SiTime B.V., the Netherlands.

Propositions

accompanying the dissertation

HIGH-POWER, EFFICIENT, AND WIDEBAND FRONT-ENDS FOR 5G TRANSMITTERS

by

Anil Kumar Kumaran

1. Mm-wave power amplifiers operating with ≈12 dB peak-to-average power ratio signals do not benefit in energy efficiency when adopting (a linear) Doherty-order beyond three (Chapter 3), due to increased impact of power combiner losses, and the limited output resistance of mm-wave semiconductor devices (Chapter 4).

   This proposition pertains to this dissertation

2. At mm-wave frequencies, Doherty PAs must employ high-pass or low-pass transmission -line models due to size constraints. Since higher-order Doherty architectures inherently exhibit reduced bandwidth, combining both models can effectively enhance bandwidth (Chapter 4).

   This proposition pertains to this dissertation

3. The wildly varying AM-PM transfer of a higher-order Doherty, caused by its complex load modulation and impedance transformations, limits its achievable spectral purity and EVM, making the linearization of such a higher-order Doherty increasingly more challenging and costly (Chapter 5).

   This proposition pertains to this dissertation

4. Although mm-wave Doherty PAs offer excellent back-off efficiency, linear PAs achieve better system performance under strict EVM demands. Integrating digital predistortion (DPD) is therefore indispensable to balance efficiency and linearity (Chapter 5).

   This proposition pertains to this dissertation

5. Physical activity, PlayStation break, and vacations stimulate the creativity essential for research, making them vital components of a productive PhD journey rather than distractions.

6. In mm-wave chip measurement, the real challenge isn't taking the measurement but setting it up, something PhD candidates, and supervisors often forget.

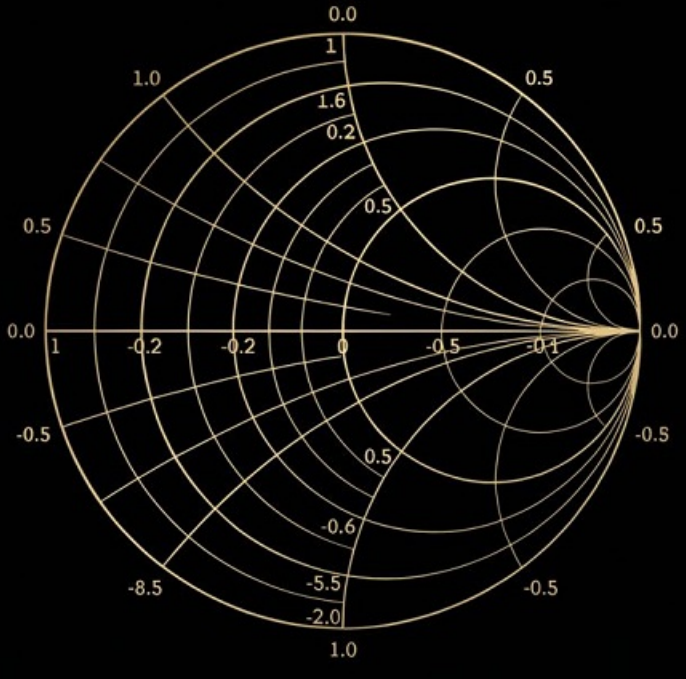
7. A PhD is not a test of technical brilliance, but of resilience, enduring failure, uncertainty, and the ever-evolving expectations of your supervisor.

8. A PhD may appear to be a solitary pursuit, but every journey is unique, and no one completes it without the support of family, friends, colleagues, and the often-overlooked technicians.

9. In research, ideas and results matter, but papers are won or lost through how well the story is sold, and that story begins with clear, insightful figures.

10. Completing measurements and thesis writing within four years is key; believing you can finish them after starting a job is a comforting illusion that many PhDs and supervisors share.

These propositions are regarded as opposable and defendable, and have been approved as such by the promotor Dr. S.M. Alavi and the promotor Prof. dr. ing. L.C.N. de Vreede.



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