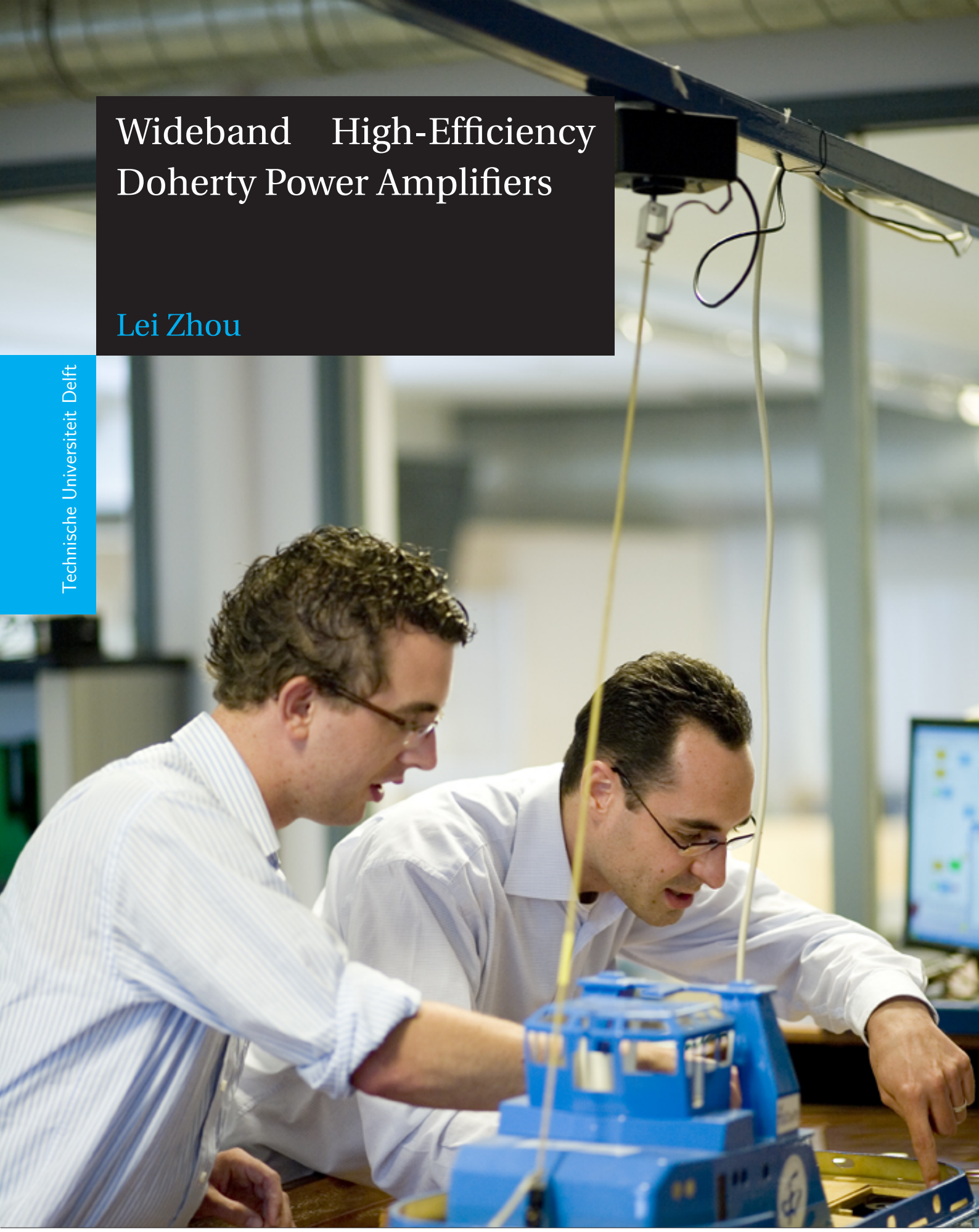
Wideband High-Efficiency Doherty Power Amplifiers

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TU Delft Delft University of Technology

Challenge the future

WIDEBAND HIGH-EFFICIENCY DOHERTY POWER AMPLIFIERS

by

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in partial fulfillment of the requirements for the degree of

Master of Science
in Electrical Engineering, Microelectronics

at the Delft University of Technology,
to be defended on Wednesday, June 29, 2016 at 15:00.

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This thesis is confidential and cannot be made public until December 31, 2017.

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ABSTRACT

Doherty power amplifier (PA) has been widely used in base station and broadcast appliations due to its simple structure and high efficiency at power back-off. Conventionally, the Doherty PA for linearity consideration tends to employ transconductance-based power amplifiers as the main and peak branch amplifiers, which have a lower peak efficiency compared with their switch-mode counterparts. In this work, we intend to enhance the efficiency of the conventional Doherty PA by employing a modified version of the load-insensitive switch-mode Class E power amplifier. Since the amplitude of the output in the Class E PA is not controled by the input drive, linear amplification of the modulated signal can not normally be obtained. To solve this problem, a novel digital polar architecture is introduced where the modulated signal is split into a digital amplitude component to control the effective on-resistance of the acive devices and a digital phase component which can be linearly amplified by the switch-mode power amplifier.

Another hot issue in the Doherty PA design is the operating bandwidth. Practical implementations of Doherty PA only provide limited RF bandwidth, especially at high power level because of the use of traditional narrowband device matching network and the bandwidth restrictions related to the Doherty load modulation network (or power combining network). In terms of the bandwidth limitations caused by the Doherty load modulation network, first a detailed analysis of the frequency behavior of an ideal 2-way symmetrical DPA is presented and it turns out that the behaviour of the conventional quarter wavelength transmission line (QWTL) impedance inverter in combination with the resulting harmonic terminations versus frequency contributes the most to the narrowband behaviour. For this reason, three new impedance inverters are introduced. It works out that the one with $\lambda/2$ open-circuited impedance inverter stands out due to its simplicitity, symmetry and wide impedance modulation bandwidth. Next to overcome the bandwidth restrictions caused by the Class E device matching network, a broadband parallel-circuit differential Class E is proposed where a balun is employed to convert the differential signal to a single-ended one. The first approach we explored to implement a balun is based on bondwires. Because of the high-quality factor of bondwires, this kind of baluns can potentially provide significant benefits in terms of low losses and form factors. Here, three different topologies are investigated. Compared with the symmetrical parallel-to-parallel single-turn topology, strctures that are based on parallel-to-series connection can provide larger impedance transforma-

tion ratio, but at the cost of lower coupling coefficient and therefore more serious amplitude and phase imbalance.

An alternative balun implementation depends upon transmission line coupling. In this thesis, a compensated Marchand balun employing re-entrant type coupled lines is proposed, which has been verified theoretically and practically to achieve low-loss and broadband balanced balun impelentations. Combining this with the broadband impedance inverter, excellent DPA wideband performance can be achieved.

The last part of this report is intended to provide a detailed design and implementation considerations of the digital envelope modulator (on-chip) and the load network (off-chip) in the proposed digitally-controlled Doherty PA. First, a broadband digitally-controlled Class-E power amplifier is given. The schematic-level Simulation results show a maximum output power of 20dBm, and a high efficiency which is up to 80% from 2.0 GHz to 2.8GHz in the case of 0.6 supply voltage. Then, a Doherty PA is simulated on the basis of this Class E power amplifier. According to simulation results, a maximum output power of 22dBm with the efficiency above 70% at both full power and 6dB power back-off. Currently this amplifier type is under construction in the SEEDCOM project.

Lei Zhou
Delft, June 2016

ACKNOWLEDGEMENT

Completion of this thesis project is an unforgettable journey in my life. I would like to take the opportunity to acknowledge to all the people who supported me along the way.

First and foremost, I would like to express my deep-felt gratitude to my supervisor Prof. Dr. Leo de Vreede, who provides me the opportunity to do such an interesting research on Doherty power amplifier, for his outstanding guidance, continuous support, valuable discussion, constant inspiration and never ending patience throughout my master project.

I am also deeply grateful to the senior colleagues involved in the SEEDCOM project, Morteza Alavi, Mohsen Hashemi, Yiyu Shen for their patience during endless discussions, and useful advice based on their rich knowledge and experience. My thanks also go to Atef Akhnoukh and Marco Pelk for helping me with the chip design and PCB layout.

In addition, I would like to thank Jawad Qureshi, Mustafa Acar, Fred van Rijs and John Gajadharsing at Ampleon for sponsoring this project and the valuable discussions during the progress of the project.

Last but not the least, I owe my loving thanks to my parents in China, my friends in the Netherlands. They supported me very much during my study abroad. Their encouragements have strengthened my confidence to face the difficulties during my master program.

Lei Zhou
Delft, June 2016

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1

INTRODUCTION

1.1. MOTIVATION

The past few years have witnessed an explosive growth of cellular network sectors due to the increase in the numbers of mobile subcribers and multimedia applications, leaving behind significant economic and environmental issues. According to[1], the Information and Communications Technologies (ICT) is responsible for about 2% of the greenhouse gas emissions worldwide. Among the total carbon dioxide emissions of ICT devices, mobile sectors accounts for 43% in 2007 and it is forecasted to rise to 51% by the year 2020[2]. With respect to the economics of the sector, it is indicated that ICT currently consumes 600 TWh (Terawatt hours) of electrical energy and this consumption is expected to increase to 1,700 TWh by 2030[3]. The above-mentioned statistics have motivated researchers to develop techniques to reduce the energy consumption of cellular networks.

According to[4, 5], the radio access equipment at the base stations contributes approximately 75-80% of all mobile network energy expenditure. However, the overall efficiency of a base station, which relates to the conversion of DC power to the RF power, lies between only 12% to 15%[6]. Thus, improving the energy efficiency of base stations is vital. In addition to high efficiency, next generation base stations should also be wideband to support multiple communication standards/bands (like the third generation mobile network, and the fourth generation standards)[6]

Figure 1.1 depicts the block diagram of a modern high power base-station. As the final stage in the transmit chain, the power amplifier (PA) is typically the most power hungry component. According to[4, 5], the power amplifier is directly responsible for almost 65-

70% and indirectly (in regard to power supplies and air cooling) up to about 85-90% of the total power consumption in the base station. Obviously, improving the efficiency of the power amplifier block is one of the most effective methods to decrease the overall energy consumption of wireless communications. Furthermore, the ever-increasing peak-to-average power ratio (PAPR) of wireless communication signals in 3G and 4G system results in stringent linearity requirements as well as power efficiency degradation in the power amplifier (PA). Therefore, more attention should be paid to the power amplifiers with respect to the energy efficiency and linearity.

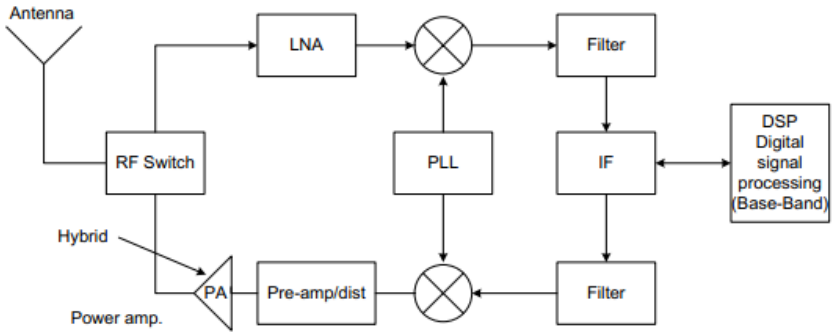


Figure 1.1: Wireless Base Station

Several techniques, such as Doherty, outphasing, dynamic load line, envelope tracking and envelope elimination and restoration (EER) have been introduced to enhance the average efficiency of PAs by improving the ratio of output power versus DC power over the transistors of the output stage. Among these techniques, the Doherty power amplifier (DPA), with simple circuit configuration, high back-off efficiency and proven linearizability, has been widely deployed in the base stations of the third generation wireless communications systems.

1.2. THESIS GOAL

Despite of the efficiency enhancement at back-off levels, DPA is a narrow band technique. The output power combiner network is often considered as the constraining factor for the RF bandwidth. For high power level DPA, the optimum load impedance is very low, resulting in an even more narrow bandwidth. In addition, both the main and peak branch amplifiers employed in a Doherty architecture are transconductance-based PAs for instance Class-B PAs, which have good linearity but low efficiency compared to the switch-mode PAs like Class-D and Class-E. Since the current improvement in the digital signal processing (DSP) technology enables the digital pre-distortion hardware to be directly embedded in the transmitter, consequently, more researches on DPA recently are focused on achiev-

ing wider bandwidth [7] and increasing efficiency rather than improving linearity.

Within this project, we aim to explore a new solution for Doherty PA with wider bandwidth and higher efficiency no matter in terms of peak efficiency or average efficiency at both power back-off and full power.

1.3. THESIS STRUCTURE

This thesis is organized as follows. Chapter 2 presents the basic concept of power amplifiers followed by an overview of different PA classes. With the need of high voltage device operation, an overview of the reliability issues for CMOS technology is discussed.

Chapter 3 discusses the operation principles of a symmetrical two-way Doherty PA and introduces the concept of digital polar Doherty PA to allow the employment of the Class E switch-mode power amplifiers for higher peak efficiency.

Chapter 4 intends to find out a wideband solution for the proposed Class E based Doherty PA. First, Class E power amplifier, can be made broadband using the differential "parallel-circuit" topology. With respect to the load modulation network, the impedance inverter turns out to be the key bandwidth limiting factor and three new impedance inverters are introduced for wideband operation.

Chapter 5 and Chapter 6 focus on the implementation of baluns, which play a critical role in a differential DPA. The possibility of a bondwire-based balun based on magnetic coupling is analyzed in Chapter 5. In this case, the imbalance between the fundamental signals, which greatly depends upon the symmetry of the structure turns out to be a big issue. Chapter 6 describes an alternative implementation of balun, which is the Marchand balun based on the transmission line coupling. To overcome the stringent dimensional requirements for tight coupling in circuit fabrication, the re-entrant type coupled lines are adopted with a compensation line to improve the imbalance caused by the unequal even-mode and odd-mode phase velocities, which is one of the key contributions of this work.

Chapter 7 first gives the design details of a differential digitally-controlled Class E PA using tsmc CMOS 40nm transistor and re-entrant type coupled lines. In this design, the techniques introduced in Chapter 3, Chapter 4 and Chapter 6 are utilized to obtain a wideband performance. Then we shift to the implementation of digital polar doherty PA, where both the main amplifiers and peak amplifiers employ the differential Class E PA. Combined with the open-circuit $\lambda/2$ TL compensated impedance inverter, the overall DPA exhibites

wider bandwidth and enhanced efficiency.

2

POWER AMPLIFIER FUNDAMENTALS

This chapter provides background information of RF power amplifiers. It starts with a brief introduction of the main performance metrics. Then an overview of different classes of power amplifiers is presented with particular attention attached to Class-E because their usage in our proposed design. Finally, a discussion of the most important reliability concerns is given in terms of CMOS power amplifiers.

2.1. POWER AMPLIFIER BASICS

Power amplifier (PA) is a key element in a transmitter that converts a low power radio-frequency (RF) signal into a larger signal of significant power to drive the antenna. In the following, the main performance parameters charactering a power amplifier are presented including the output power, power gain, efficiency, and linearity.

2.1.1. OUTPUT POWER

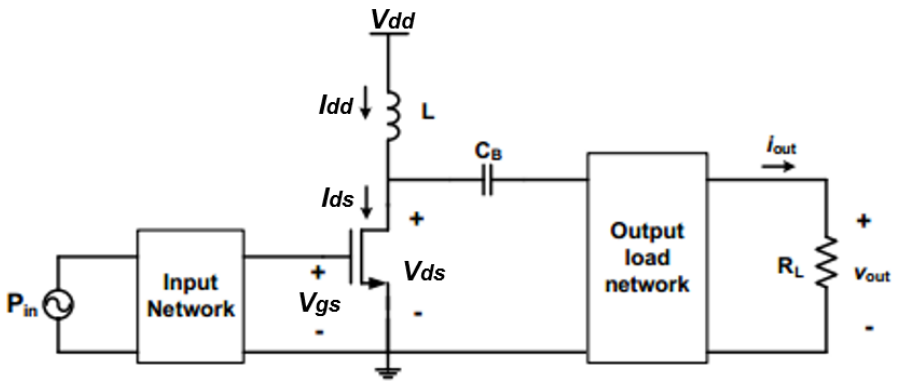


Figure 2.1: Block diagram of power amplifier

The output power is defined as the power delivered by the active device and flowing into the load R_L considering the basic circuit of Fig 2.1. The instaneous output power is defined as

$$p_{out}(t) = v_{out}(t) \cdot i_{out}(t) \tag{2.1}$$

The average output power P_{out} is given by

$$P_{out} = \frac{1}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} p_{out}(\tau) d\tau \tag{2.2}$$

In most cases, only the power at the fundamental frequency is desired and the harmonic power needs to be filtered at the output. Therefore, it is more meaningful to define a fundamental average output power P_{out,f_0}, which equals to the output power at the fundamental frequency only

$$P_{out,f_0} = \frac{V_{out}^2}{2R_L} = \frac{V_{out,rms}^2}{R_L} \tag{2.3}$$

with V_{out} the amplitude or peak value of the sinusoidal output voltage at frequency f_0 and $V_{out,rms}$ the rms value of V_{out}.

According to Equation 2.3, the output power delivered to a real load R_L by a PA is proportional to the square of the output voltage amplitude. And the output voltage amplitude in rms can be expressed as $V_{out,rms} = \overline{v_{pk}} \cdot V_{dd}$, where $\overline{v_{pk}}$ is the proportionality factor and it is determined by the amplifier class of operation. Thus, the output power can be given in terms of the proportionality factor as

$$P_{out,f_0} = K_P \frac{V_{dd}^2}{R_L} \tag{2.4}$$

Thus K_P can be viewed as the the normalized output power level with respect to the supply voltage for a given load. This general quantitative definition of output power is helpful for the direct comparisons between all the amplifier classes in the .

However, K_P (P_{out}) only describes how much output power will be generated from a given supply voltage, it does not state anything about the reliablity of the PAs. For this reason, the maximum output power ($P_{out,max}$) which measures the deliverable output power with the transistor operating under the technology's maximum reliability limits is considered as well. This power level is normalized with respect to the maximum voltage ($V_{ds,max}$) at the transistor's terminal and the load resistor R_L. The normalization factor is defined as k_P and it is given by

$$k_P = \frac{P_{out,max}}{V_{ds,max}^2 \cdot \frac{1}{R_L}} \tag{2.5}$$

Notice that both K_P and k_P are directly related through

$$k_P = \frac{K_P}{v_{pk}^2} \tag{2.6}$$

where v_{pk} is the normalized (with respect to the supply voltage) peak voltage at the drain terminal.

2.1.2. POWER GAIN

The power gain of a PA, usually expressed in dB, is defined as the ratio of the output power to its input power.

$$G_p = 10\log_{10}(\frac{P_{out}}{P_{in}}) \tag{2.7}$$

2.1.3. EFFICIENCY

Efficiency is an important design parameter which provides information on how well DC power is converted to RF power. First, the DC power consumption P_{DC} is calculated as

$$P_{dc} = V_{dd} \cdot I_{dc} \tag{2.8}$$

with I_{dc} the dc component of Fourier Series expansion of $i_{dd}(t)$. The drain or collector efficiency η is defined as

$$\eta = \frac{P_{out}}{P_{dc}} \tag{2.9}$$

The Power Added Efficiency (PAE) takes into account the RF input power P_{in} and it can be expressed as

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} = \eta(1 - \frac{1}{G_p}) \tag{2.10}$$

If the power gain is sufficiently high, the PAE becomes equal to the drain efficiency.

2.1.4. LINEARITY

Most new communication systems (EDGE, W-CDMA, W-LAN) in recent years have varying envelope signals. To amplify these signals correctly, the power amplifier must thus have sufficient amplitude linearity. The nonlinearity of a PA can be characterized by their AM-AM distortion and AM-PM distortion. Various ways can be used to qualify the linearity of a power amplifier, including the third-order intercept point (IP3), adjacent channel power ratio (ACPR), 1dB compression point, and harmonics suppression.

The 1dB compression point (P_{1dB}) of a power amplifier indicates the output power level that causes the gain to drop by 1dB from its small signal value. The third-order intercept point (IP3) is the point where the third-order term as extrapolated from small-signal conditions crosses the extrapolated power of the fundamental. ACPR is defined as the ratio of power in a bandwidth away from the main signal (the distortion product) to the power in a bandwidth within the main signal.

2.2. PA CLASSIFICATION

Power amplifiers can be categorized into two major groups: transconductance (gm)-based PAs (or linear PAs) and switch-mode PAs (or nonlinear PAs). Generally, the first group of PA (gm-based) works as a dependent current source while the second group operates as a switch toggling between two opposite states: ON (or low-impedance) and OFF (or high-impedance).

This section presents a brief description of the familiar lettered classification of PAs (Class A, B, C, D, E, F, etc.) refering to amplifiers belonging to one of the two groups. Particular attention is given to Class-E power amplifiers because their usage in our proposed design.

2.2.1. GM-BASED PAS

Class A, AB, B and C PAs are the well-known gm-based PAs. In addition, Class-F PAs can also be considered as gm-based PAs when the active device operates as a transconductor. The Class-F PAs belong to switch-mode PAs only when it is driven very hard.

CLASS A, AB, B, C PAS

Class A, AB, B, C PAs can be distinguished by the conduction angle of drain current, which is defined as the portion of a period during which the transistor is carrying current. The simplified gm-based power amplifier topology is shown in Figure 2.1. The inductor L is assumed to allow only a DC current. The output matching network provides optimum fundamental impedance and allows harmonics control. The transistor behaves as a voltage-controlled current source whose conduction angle changes with different biasing conditions.

Class A: For Class-A PAs, the biasing point is chosen to enable the transistor to operate in linear region over the entire RF cycle, thus, the conduction angle is 360°. Class-A PAs are considered to be the most linear but the theoretical maximum efficiency of this type of power amplifier is as low as 50%.

Class B: For Class-B PAs, the biasing point is set at the threshold voltage of the transistor, thus its conduction angle is 180°. Compared to Class-A PAs, Class-B PAs have worse linearity and better efficiency. The theoretical maximum efficiency of Class-B PAs achieves 78.5%.

Class AB: For Class-AB PAs, the conduction angle varies between 180°and 360° depending on the biasing point. As a result, Class-AB represents a compromise between Class-A and Class-B in terms of linearity and effiency. Thus the efficiency for this class of operation is between 50 and 78.5%.

Class C: For Class-C PAs, the biasing point is below the threshold voltage of the transistor and hence its conduction angle is below 180°. The Class C PAs have the greatest efficiency but the poorest linearity compared to the other conventional linear power amplifies. In theory, a drain effiency of 100% can be achieved, however, in this case, the output power is reduced to 0. As a result, tradeoff between efficiency and output power must be made.

Figure 2.2 presents a generalized current waveform incorporating all conventional linear PA classes, where α is the conduction angle, I_q is the quiescent bias current, I_{pk} is the current amplitude and I_{max} is the peak value of the drain current. The drain current waveform of the transistor $i_d(\theta)$ can be expressed as

$$i_d(\theta) = \begin{cases} I_q + I_{pk}\cos(\theta) & \text{if } -\alpha/2 \le \theta \le \alpha/2, \\ 0 & \text{if } -\pi < \theta < -\alpha/2 \quad or \quad \alpha/2 < \theta < \pi. \end{cases} \tag{2.11}$$

where

$$\cos(\frac{\alpha}{2}) = -\frac{I_q}{I_{pk}} \quad \text{and} \quad I_{pk} = Imax - I_q$$

So

$$i_d(\theta) = \frac{I_{max}}{1-\cos(\alpha/2)}(\cos\theta - \cos(\alpha/2)) \quad if -\alpha/2 \le \theta \le \alpha/2 \tag{2.12}$$

Using Fourier decomposition, we can calculate the related DC current as well as the fundamental and harmonic current components. First, the DC component is

$$I_{dc} = \frac{I_{max}}{2\pi}\frac{2\sin(\alpha/2) - \alpha\cos(\alpha/2)}{1-\cos(\alpha/2)} \tag{2.13}$$

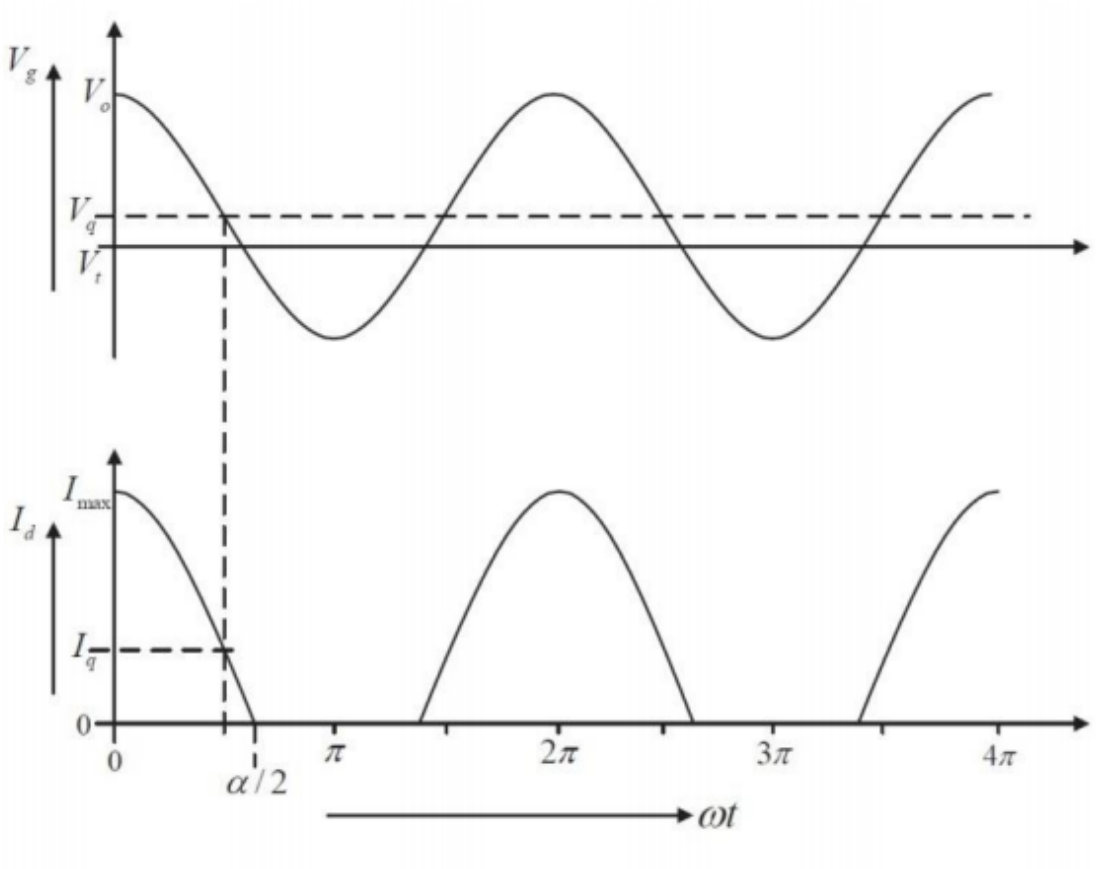


Figure 2.2: Input voltage and output current waveforms of a linear power amplifier

The fundamental component is

$$I_1 = \frac{I_{max}}{2\pi}\frac{\alpha - \sin(\alpha/2)}{1-\cos(\alpha/2)} \tag{2.14}$$

The magnitude of n_{th} component ($n \geq 2$) is

$$I_n = \int_{-\alpha/2}^{\alpha/2} \frac{I_{max}}{1-\cos(\alpha/2)} \cdot (\cos\theta - \cos(\theta/2)) \cdot \cos(n\theta)\, d\theta \tag{2.15}$$

If the fundamental load impedance is set to make the drain voltage of the device have a maximum $2V_{DD}$ peak-to-peak value, we can get maximum output power. This matching technique is called loadline matching and the optimum load impedance can be expressed as

$$R_{opt} = \frac{V_1}{I_1} = \frac{V_{dd}}{I_1} = V_{dd} \cdot \frac{2\pi}{I_{max}} \cdot \frac{1-\cos(\alpha/2)}{\alpha - \sin\alpha} \tag{2.16}$$

The RF fundamental output power can be calculated as

$$P_{out} = \frac{1}{2} V_{dd} I_1 = \frac{V_{dd} I_{max}}{4\pi} \cdot \frac{\alpha - \sin\alpha}{1-\cos(\alpha/2)} \tag{2.17}$$

And and the DC power supply is given by

$$P_{dc} = V_{dd} I_{dc} \tag{2.18}$$

Therefore the drain efficiency can be expressed as

$$\eta = \frac{P_{out}}{P_{dc}} = \frac{1}{2}\frac{V_{dd} I_1}{V_{dd} I_{dc}} = \frac{1}{2} \cdot \frac{\alpha - \sin\alpha}{2\sin(\alpha/2) - \alpha\cos(\alpha/2)} \tag{2.19}$$

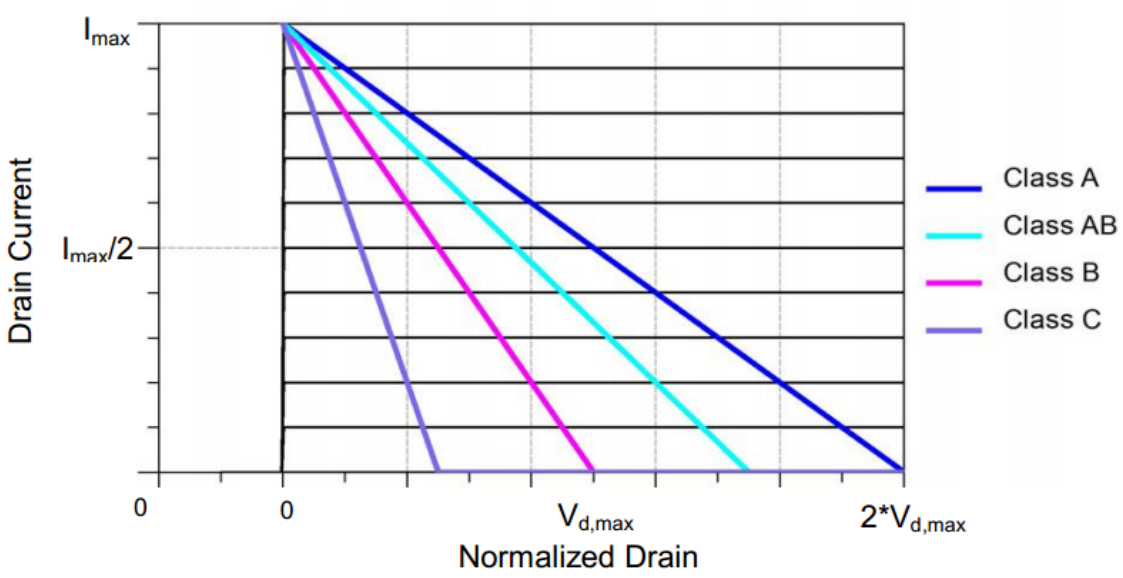


Figure 2.3: Loadline for different classes of conventional PAs [6]

Figure 2.3 shows the loadline for different conventional PA classes while Figure 2.4 presents the output power, DC input power as well as efficiency as a function of conduction angle, from which conclusions above can be verified. As depicted in Figure 2.4, between Class A and Class B operation, the fundamental RF output power is approximately constant, showing a slight increase in the middle Class AB stage over Class A. The Class B condition delivers the same power as Class A but with a dc supply reduced by a factor of $\pi/2$ compared to Class A, giving an ideal efficiency of $\pi/4$. Class AB is a compromise between Class A and Class B in terms of efficiency. Class C owns very high efficiency, but its output power is sharply reduced as a function of a shorter conduction angle.

CLASS-F POWER AMPLIFIERS

Class F boosts both efficiency and output power by using harmonic resonators in the output network to shape the drain waveforms. The voltage waveform includes one or more

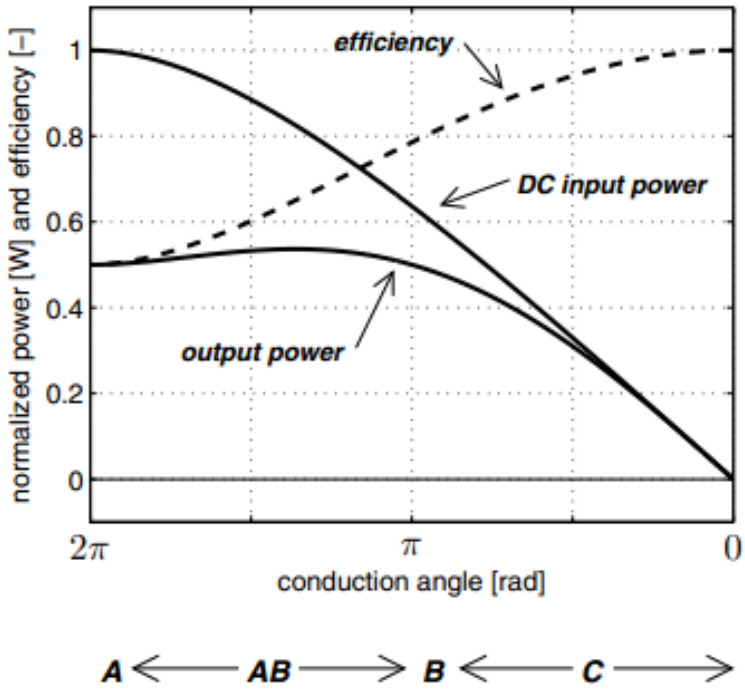


Figure 2.4: Output power, DC power consumption and efficiency versus conduction angle

odd harmonics and approximates a square wave, while the current includes even harmonics and approximates a half sine wave. In this way, the voltage-current overlap is therefore reduced. The inverse Class F, or class F^{-1}, which is derived from the Class F, has a half-sinusoidal wave drain voltage and a square wave drain current on the contrary.

An ideal Class F amplifier requires the control of an infinite number of harmonics, which can be realized by using a $\lambda/4$ transmission line as shown in Figure 2.5. This type of Class-F power amplifiers was initially proposed to be applied at very high frequencies where it is difficult to implement the load networks with only lumped elements and the parasitic device output (lead or package) inductor is sufficiently small. The Class F power amplifier topology presented in Figure 2.5(a) makes use of a series quarter-wave transmission line and a parallel-tuned resonant circuit to provide a short circuit at the drain for even harmonics and an open circuit for odd harmonics with resistive load at the fundamental. While in Figure 2.5(b), a shunt transmission line is added between the dc power supply and device collector to provide open circuit for odd harmonics and short circuit for even harmonics at the drain.

Although the Class F and the inverse Class F amplifiers look attractive at first sight, they are difficult to realize because of the output parasitics of the active device and the related

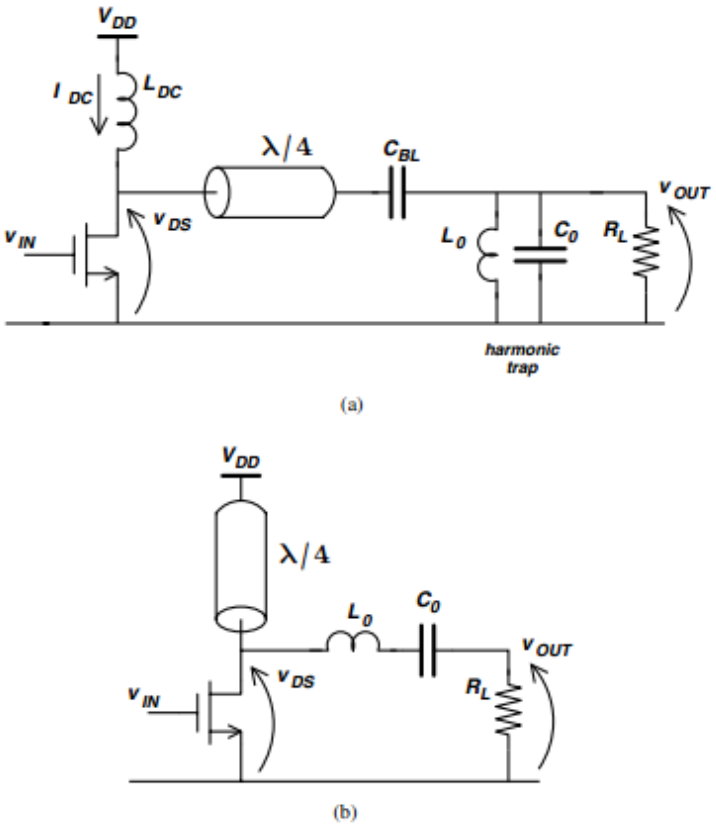


Figure 2.5: Class F power amplifier with $\lambda/4$ transimission linee [8]

complex load network to compensate for those. Realization involving a $\lambda/4$ transmission line as depicted in Figure 2.5 is able to control infinite number of harmonics, but it increases the required area to implement the amplifier, thus making the (ideal) Class F amplifier less attractive if one strives for a high level of integration. On the other hand, more than three harmonics is difficult to control, resulting in a reduction of the maximum obtainable efficiency from 100%. From [8], the (theoretical) efficiency is 92% if both the third and fifth harmonic peaking are included and this value will decrease to 88% if only the third harmonic is used. In addition, as mentioned, the drain-source parasitic capacitance of the active device at RF becomes significant, which provides a low-impedance path for the higher harmonics, and the squaring will be less pronounced, again reducing the benefit of Class F. Therefore, it is necessary to resonate it out to present the required impedances at the internal current generator plane. All these will result in a narrow band operation of Class F power amplifiers, restricting their potential for integration within wideband or multiband transceivers.

2.2.2. SWITCH-MODE PAS

In a switch-mode PA, the transistor is driven by a large input signal in such a way that it goes from the triode region to the cut-off region rapidly, thus the transistor operates as a switch instead of a current source. The switch behaviour minimizes the overlapping of non-zero drain voltage and non-zero drain current waveforms and therefore yields a higher efficiency. Compared to conventional gm-based PAs, switch-mode PAs can achieve higher efficiency. But the price paid for efficiency enhancement is the degradation in linearity. Switch-mode PAs are considered non-linear as there is no relationship between the output signal and the input signal in terms of amplitude as long as the input signal is high enough to keep the transistor in the triode region. However, this 'non-linearity' only refers to the amplitude, since phase linearity is still present.

CLASS-D POWER AMPLIFIERS

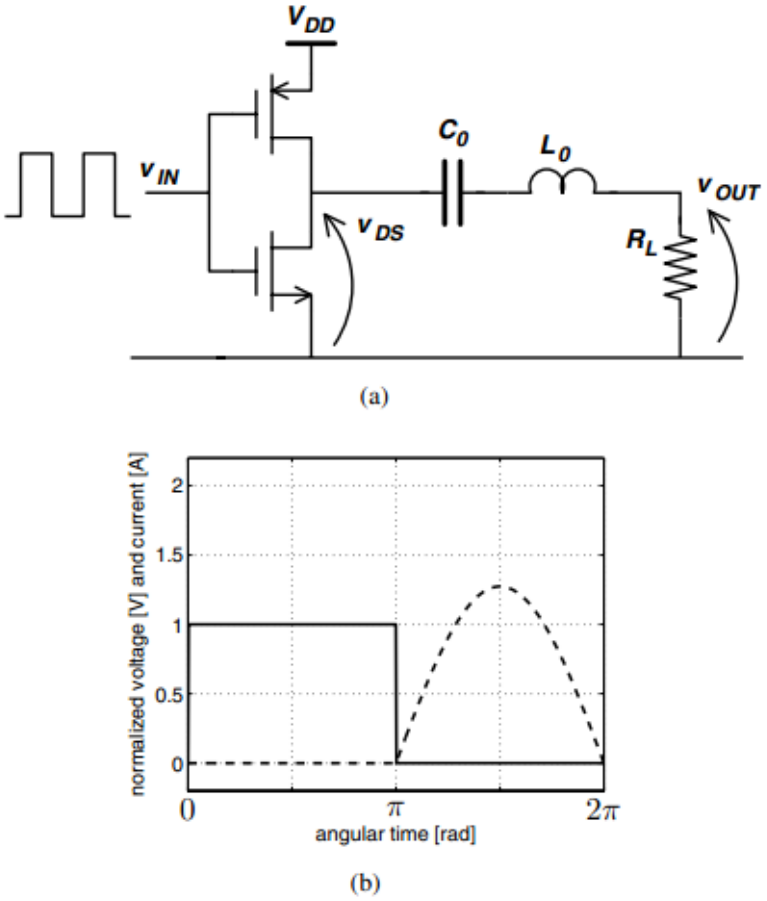


Figure 2.6: Class D power amplifier: (a) schematic and (b) normalized drain voltage (solid line) and drain current (dashed line).[8]

Class-D power amplifier generally consists of two active devices to generate square drain–voltage (or current) waveforms and a tuned circuit in the load match network to re-

move the harmonics of the rectangular waveform, generating a sinusoidal output. Figure 2.6 shows the basic schematic of a Class D Complementary Voltage Switching power amplifier. When M1 is switched on, M2 is switched off and vice versa. Ideally, there is no voltage across the switch when conducting and no current through them when off, thus no power dissipates on the switches and all the power is delivered to the load. In the output load network, the combination of L_0 and C_0 is resonant at the fundamental frequency to suppress all harmonics. The theoretical efficienct of Class-D is 100%. However, charging and discharging the drain-to-source capacitance per RF cycle causes power dissipation that is directly proportional to the drain voltage and frequency of operation. Consequently, the use of Class-D is generally limited to low frequencies.

CLASS-E POWER AMPLIFIERS

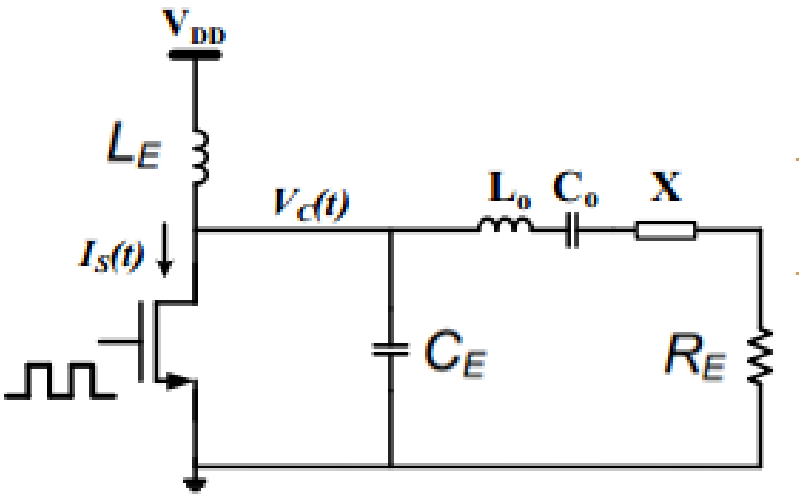
Class E power amplifier, first introduced by Sokal in 1975[9], is another well-known switch-mode amplifier. The basic Class E schematic and its equivalent model are shown in Figure 2.7 where the transistor is employed here as an ON/OFF switch (R_{on} and R_{off} are the switch resistance for ON-state and OFF-state respectively). The load network generally consists of a shunt capacitor C_E, a DC feed inductor L_E, a series-tuned filter (L_0 and C_0), and an extra reactance X. Note that the shunt capacitance C_E is a combination of the transistor output capacitance and the load network capacitance. For higher operating frequencies, C_E can be entirely supplied by the transistor parasitic output capacitance, which is a huge advantage especially in CMOS since power losses due to the discharge of the output capacitance of the transistor are avoided in theory.

Class-E power amplifiers can be categorized into two main groups, “optimum” and “sub-optimum” depending on its loading condition, which is expressed as follows:

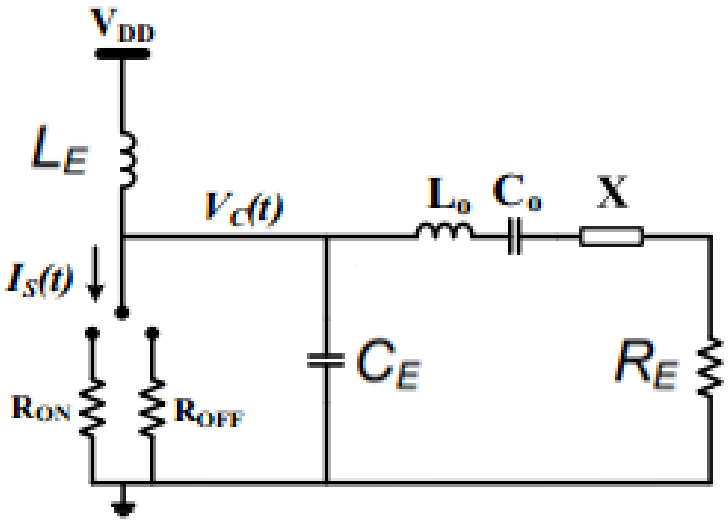
$$V_C(t)\Big|_{t=\frac{2\pi}{\omega}} = \alpha V_{DD} \tag{2.20}$$

$$\frac{dV_C(t)}{dt}\Big|_{t=\frac{2\pi}{\omega}} = k\omega V_{DD} \tag{2.21}$$

with αV_{DD} the voltage of $V_C(t)$ at the moment the switch is closed and $\omega V_{DD} k$ the slope of $V_C(t)$ at the moment the switch is closed. For the well-known "optimum" mode, both the voltage and the voltage-derivative are simutaneously zero ($\alpha = 0$ and $k = 0$)[10, 11]. For the so-called "sub-optimum" mode [12], either the voltage or the voltage-derivative are non-zero ($\alpha \neq 0$ or $k \neq 0$). Among the "sub-optimum" mode, two particular case, called “variable-voltage” and “variable-slope” are of interest as well. For variable-voltage mode[13], $\alpha \neq 0$ $k = 0$, while for Variable-Slope operation, $\alpha = 0$ and $k \neq 0$ [14]. However, only the first condition is responsible for the ideal efficiency of 100% while the second is



(a)



(b)

Figure 2.7: Class-E amplifier. (a)Basic circuit. (b)Equivalent circuit.

useful in practice as it reduces the sensitivity of the circuit to the spread of component values[9].

The design of Class E power amplifier is straight forward with the generalized analytical model proposed in [15] where a useful design set $K_E = \{K_L, K_C, K_P, K_X\}$ shown in Table 2.3 was made use of to relate certain technology and design parameters (see Table 2.1) as well as some user defined operating condition (see Table 2.2) to circuit element val-

Table 2.1: Technology and design related parameters

Symbol	parameter description
V_{DD}	Supply voltage[V]
ω	Operating frequency[rad/s]
$m_{on} = \omega C R_{on}$	A technology-frequency paramater[rad]
$m_{off} = \omega C R_{off}$	A technology-frequency paramater[rad]

Table 2.2: User defined parameters

Symbol	parameter description
α	Variable-voltage defining parameter
k	Variable-slope defining parameter
d	Duty-cycle defining paramater (duty cycle = $d \cdot 50\%$)
$q = \frac{1}{\omega\sqrt{LC}}$	Ratio between LC tuning frequency and operating frequency

Table 2.3: Design set K_E

Design set K_E
$K_L = \omega L / R_L$
$K_C = \omega C R_L$
$K_P = P_{out} R_L / V_{DD}^2$
$K_X = X / R_L$

ues (e.g. L_E, C_E, X, R_E) as well as to the PA performance (P_{out} and η). The design set K_E can be viewed as a function of many parameters including α, k, d, q, m_{on}, m_{off}, ω and V_{DD}. Infinite solutions exist due to the freedom in the values of dc-feed inductor (q), the switch duty-cycle (d), the variable-voltage (α) and variable-slope (k). Once these parameters are selected there is a solution for design set K_E and therefore the circuit elements (e.g. L_E, C_E, X, R_E) can be readily found for a given output power P_{out} as follows:

$$R_E = \frac{K_C}{\omega \cdot C_E} \tag{2.22}$$

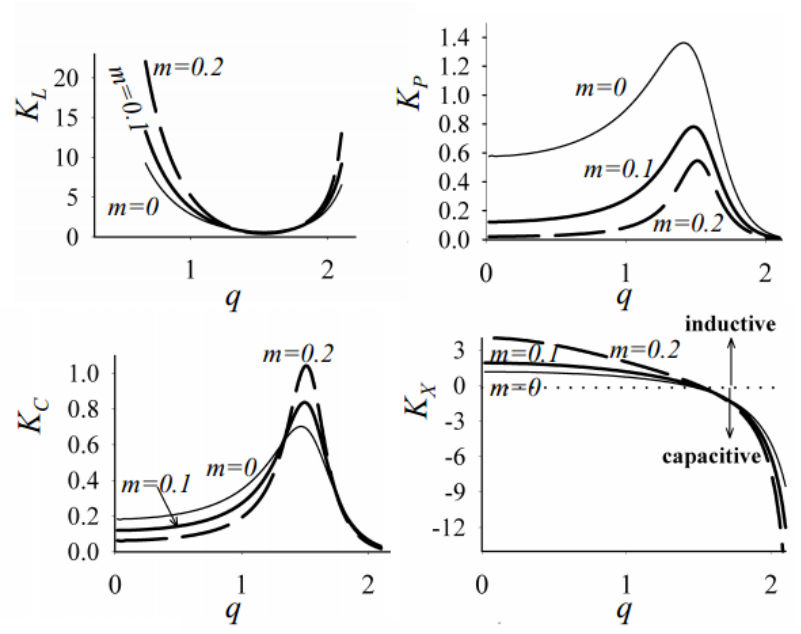
$$V_{DD} = \sqrt{\frac{P_{out} \cdot R_E}{K_P}} \tag{2.23}$$

$$L_E = R_E \cdot \frac{K_L}{\omega} \tag{2.24}$$

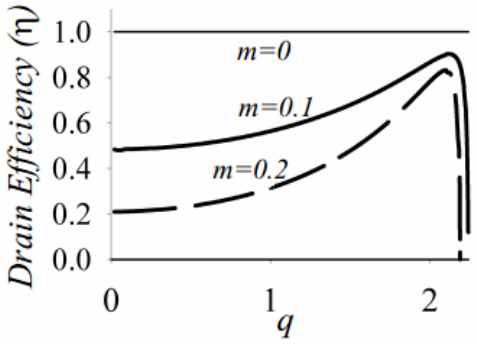
$$X = R_E \cdot K_X \tag{2.25}$$

Figure 2.8 shows the design set K_E and drain efficiency η for the optimum Class E with varying m ($m_{on} = m$, $m_{off} = \infty$ in this case) and q values and a fixed duty cycle which is assumed to be 50% ($d = 1$). q, in theory, can take any positive real number. However, as it

can be seen in Figure 2.8, K_C, K_P and η approach zero for $q > 2$. Thus, the useful range of the analytical solution for optimum Class E with $d = 1$ can be assumed to be restricted to 0< q <2. In addition, we can observe from Figure 2.8 that K_P and η drops as m_{on} increases. Therefore a smaller parameter m is prefered for the desired high efficiency and large power Class E PA.



(a)



(b)

Figure 2.8: (a) Design set K_E and (b) drain efficiency (η) as a function of q for $m_{on} = m$ =0, 0.1, 0.2 and $m_{off} = \infty$ [11].

Table 2.4 [16] summarizes the results for three distinctive cases of interest: the RF-choke, the parallel-circuit and the load-insensitive class-E amplifiers when $d = 1$ and $m = 0$. The classical "RF-choke" class-E PA [9, 10] results when $q = 0$ and $L_E = \infty$. When $q \approx 1.3$, the class-E PA becomes “load-insensitive” [16, 17] to allow for large variation in the load resistor R_E and this feature can be favorably exploited in PAs using load-modulation tech-

nique for higher average efficiency. Further details about this feature can be found in Chapter 3. The "parallel-circuit" class-E PA [18] corresponds to the case when $q = 1.41$ and hence $Z_{Eparallel} = R_L || j\omega L$ since $X = 0$ for $q = 1.41$. It provides the maximum output power for a given supply voltage and loading resistance. In addition, with proper choice of load match network, we can realize a broadband design with parallel Class E power amplifiers, this feature will be detailed discussed in Chapter 4. In addition, it can be observed from Table 2.4 that the peak voltage V_c and peak current I_s are very weak functions of q and roughly about 3.6 and 2.7 times the supply voltage and current respectively.

Table 2.4: Design equations for different Class E power amplifier

Design details	RF-choke	Parallel Circuit	Load-insensitive
q	0	1.412	1.3
K_L	∞	0.732	1.01
K_C	0.184	0.685	0.585
K_X	1.152	0	0.26
K_P	0.577	1.365	1.29
k_P	0.046	0.103	0.100
$V_{c,pk}/V_{DD}$	3.562	3.647	3.6
$I_{s,pk}/I_{DD}$	2.862	2.647	2.7
f_{max}	$\frac{I_{ds,max}}{56 \cdot C_E \cdot V_{DD}}$	$\frac{I_{ds,max}}{33 \cdot C_E \cdot V_{DD}}$	$\frac{I_{ds,max}}{37 \cdot C_E \cdot V_{DD}}$

Next we move to the sub-optimum mode. Designing a Class E in sub-optimum mode has advantages. As mentioned before, if the correct input parameters and circuit element values in Figure 2.7 are chosen by satisfying the following conditions (see Equation (2.26) and (2.27)), the Class E PA will operate in voltage-variable mode. Figure 2.9 depicts the typical time-domain drain-to-source voltage and switch current for the so-called voltage-variable Class E PA with different voltage-variable parameter $\alpha = 0, 0.5, 1, 2$ while assuming that $m_{on} = 0.01$, $m_{off} = 1000$,$d = 1$. The design details for these 4 Class E PAs are listed in Table 2.5. Obviously, larger values of α result in lower efficiency η and smaller output power factor K_P due to the ON switching losses. But η and K_P do not drop very rapidly as α increases from 0 up to 1. Additionally, it can be observed that the peak voltage decreases with the increase of α, implying that a safety design can be achieved in variable-voltage Class E trade-off with a small loss in drain efficiency and output power.

$$V_C(t)\Big|_{t=\frac{2\pi}{\omega}} = \alpha V_{DD} \tag{2.26}$$

$$\frac{dV_C(t)}{dt}\Big|_{t=\frac{2\pi}{\omega}} = 0 \tag{2.27}$$

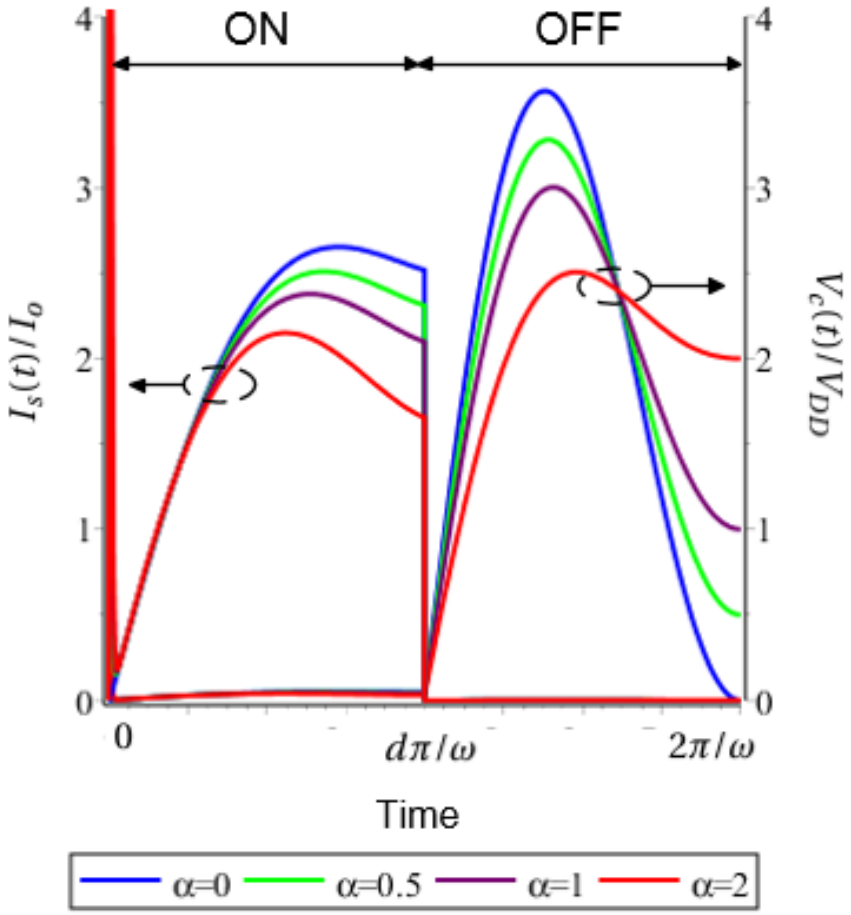


Figure 2.9: Normalized switch voltage and switch current of voltage-variable Class E PA with turn-on voltage of $\alpha = 0, 0.5, 1, 2$

Table 2.5: Design details for Class E PA with different values of variable-voltage defining parameter α

Design Details	Class E_0	Class $E_{0.5}$	Class E_1	Class E_2
(m_{on}, m_{off})	(0.01,1000)	(0.01,1000)	(0.01,1000)	(0.01,1000)
(q, d)	(1.4,1)	(1.4,1)	(1.4,1)	(1.4,1)
α	0	0.5	1	2
K_L	0.725	0.821	0.933	1.377
K_C	0.692	0.621	0.538	0.364
K_X	0.0186	-0.143	-0.377	-0.912
K_P	1.271	1.126	0.927	0.527
k_P	0.103	0.102	0.100	0.083
η	95.4%	94.8%	92.1%	80.5%
$V_{c,pk}/V_{DD}$	3.624	3.326	3.041	2.526
$I_{s,pk}/I_{DD}$	2.602	2.445	2.321	2.141

If the correct input parameters and the circuit element values are chosen, the circuit properly operates as a variable-slope Class-E PA by satisfying the following conditions (2.28) and (2.29). The variable-slope Class E has the advantage of allowing higher switch sizes

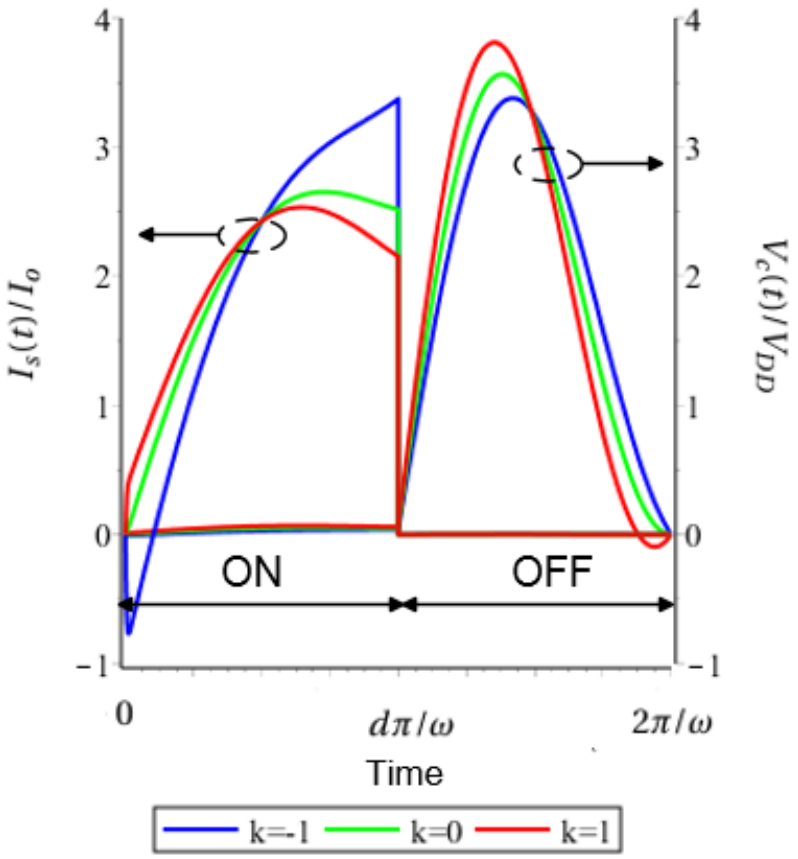


Figure 2.10: Normalized switch voltage and switch current of voltage-slope Class E PA with turn-on voltage of $k = -1, 0, 1$

Table 2.6: Design details for Class E PA with different values of variable-slope defining parameter k

Design Details	Class E_{-1}	Class E_0	Class E_1
(m_{on}, m_{off})	(0.01,1000)	(0.01,1000)	(0.01,1000)
(q, d)	(1.4,1)	(1.4,1)	(1.4,1)
k	-1	0	1
K_L	0.480	0.725	1.00
K_C	1.045	0.692	0.502
K_X	-0.267	0.0186	0.205
K_P	1.164	1.271	1.270
k_P	0.100	0.103	0.084
η	96.6%	95.4%	92.1%
$V_{c,pk}/V_{DD}$	3.414	3.624	3.898
$I_{s,pk}/I_{DD}$	3.345	2.602	2.451

(higher K_C) with the benefit of enhanced drain efficiency for negative variable-slope parameter (i.e. k=-1). When the value of k goes to positive, it does not seem attractive any

more since the peak voltage increases and the drain efficiency decreases.

$$V_C(t)\Big|_{t=\frac{2\pi}{\omega}} = 0 \tag{2.28}$$

$$\frac{dV_C(t)}{dt}\Big|_{t=\frac{2\pi}{\omega}} = k\omega V_{DD} \tag{2.29}$$

2.3. CONCLUSIONS

Linearity, efficiency and output power are among the important considerations for PA designs. This section mainly presents a discussion of these properties for different classes of power amplifiers. Class A, B, C, and F are among the gm-based PAs which have much better linearity but lower efficiency compared with their swith-mode counterparts including Class D and Class E. Table 2.7 summarizes a few basic PA properties including ideal drain efficiency η, normalized output power K_P and maximum power factor k_P for different classes. It can be observed from K_P that if the active devices are not constrained by the reliability issues, then the parallel-circuit Class E will yield the highest output power for a given supply voltage and load. But if the active devices are limited by the reliability issues, then the highest output power is achieved by the Class D operation for a given reliable supply voltage and load, as expressed by k_P. And the reliable constrains of CMOS technology will be discussed in the next section.

Table 2.7: Summary of ideal drain efficiency η, normalized output power K_P and power capacibility k_P for different PA classes

PA operation class	Peak efficiency η	Output power factor K_P	Maximum power factor k_P
Class A	50.0%	0.500	0.125
Class B	78.5%	0.500	0.125
Class C	78.5%–100%	< 0.500	<0.125
Class F_3	88.4%	0.6328	0.1582
Class F_5	92.0%	0.6866	0.1717
Class D	100%	0.2026	0.2026
RF-choke Class E	100%	0.5768	0.0455
Parallel-circuit Class E	100%	1.365	0.1036
Load-insensitive Class E	100%	1.290	0.1029

2.4. CMOS TECHNOLOGY AND RELIABILITY

Although CMOS technology has merits of low cost and high integration potential, it is challenging to design a CMOS power amplifier because of the intrinsic drawbacks of standard

CMOS processes from RF perspectives: limited quality factor (Q) of integrated passives, the lossy substrate and low breakdown voltage. In this section, importance is attached to the reliability challenges related to the low breakdown voltages in CMOS transistors. For this reason, four well-known degradation mechanisms including gate oxide breakdown, hot carrier degradation, punch through and drain-bulk break-down are discussed.

2.4.1. GATE OXIDE BREAKDOWN

Gate oxide breakdown is a catastrophic failure as a result of the application of a high voltage over the gate-oxide of a MOS device. Once it occured, a conductive path is formed from the gate to the substrate, resulting in permanent damage to the gate oxide. The breakdown limit is inversely proportional to the oxide thickness and thus it becomes smaller as the gate oxide thickness is reduced in each process generation. As shown in Figure 2.11, the

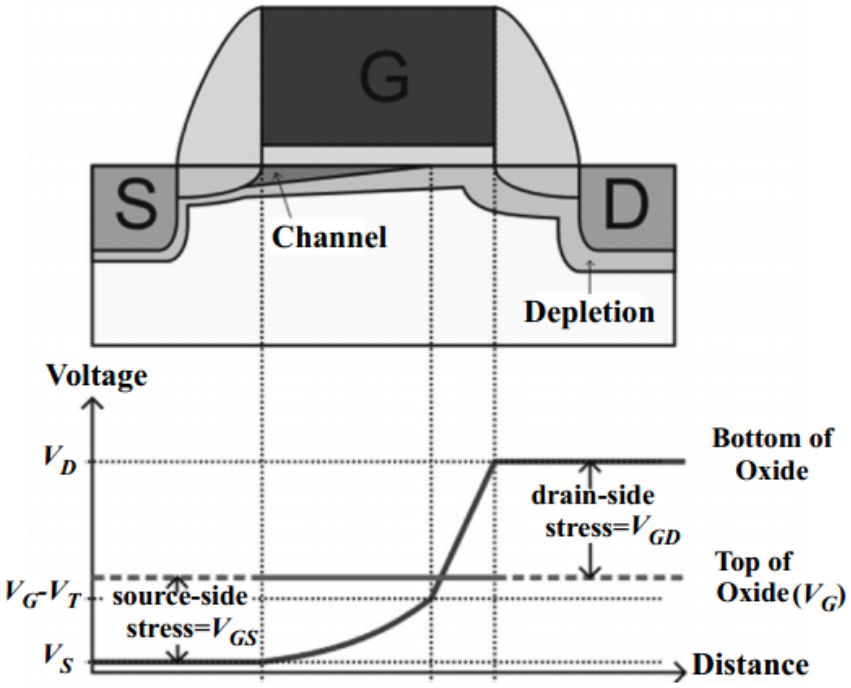


Figure 2.11: Gate oxide breakdown in a MOS transistor [19]

channel voltage varies from the source to drain. Consequently, the oxide stress, the voltage difference between the top of the oxide and the bottom of the oxide is a function of position. The highest stress areas occur at the source and drain oxide edges and therefore from a design point of view, we must make sure that the gate-source and the gate-drain voltages (V_{GS} and V_{GD}) never exceed the breakdown limit [19].

Although oxide breakdown is often assumed to occur instantly at a predetermined break-

down limit. In fact the failure is a probabilistic event, with increasing probability as voltage, stress time, or oxide area are increased [19]. Generally, the Oxide breakdown process occurs in two steps [20]:a gradual field-induced defect accumulation followed by thermal runway and permanent damage of oxide. It can be characterized by the Mean Time to Failure (MTTF) to anticipate the time for the defect dencity to reach a critical level that triggers the thermal runway [20]. This thermal runway process rapidly leads to a short across the oxide and hence permanently destroying the device. Though the intrinsic breakdown electrical field for SiO_2 is around 1.1V/nm, the maximum practical voltage ratings in typical CMOS are usually lower [20]. According to [20], oxide lifetime is sufficient if the electrical field is restricted to 0.55V/m. For instance, for a 40nm CMOS process, the maximum rated gate voltage is 1.1V and 2.5V respectively for thin-oxide (2.4nm) and thick-oxide (5.7nm) device, which corresponds to oxide field of less than 0.5V/nm for both cases.

2.4.2. HOT-CARRIER DEGRADATION

For a short channel device under a large drain-to-source voltage, the lateral field can be extremely high, consequently carriers flowing from source to drain may gain high energies. Before arriving at the drain terminal, some of these hot carriers collide with the lattice, resulting in impact ionization and potential avalanche multiplication. In addition, this may generate surface defects, which will cause the reduction of the carrier mobility in the channel. Morever, trapped charge can be created in the gate oxide or oxide/silicon interface due to the collision, shifting the local threshold voltage. This damage usually occurs in the drain region where the electric field is very high, ending up with the damage to manifest itself as an increase in on-resistance and knee voltage, reducing the power amplifier performance. Different from the gate oxide breakdown, the hot carrier degradation is not intrin-sically catastrophic. Instead, it causes a gradual degradation in the device performance over a period of time [19].

Since hot carriers are only generated in the simutaleous presence of a high drain-source voltage and a substantial drain current, the hot carrier degradation can be elimilated by avoiding channel current when drain voltage is high. This happens ordinarily in a switch-mode amplifier (e.g. Class-E poweramplifiers), where the transistor conducts current at a low voltage and vice versa, thus making switch-mode power amplifiers less prone to hot carrier degradation. However, hot carrier degradation can be a serious issue in linear power amplifiers [19].

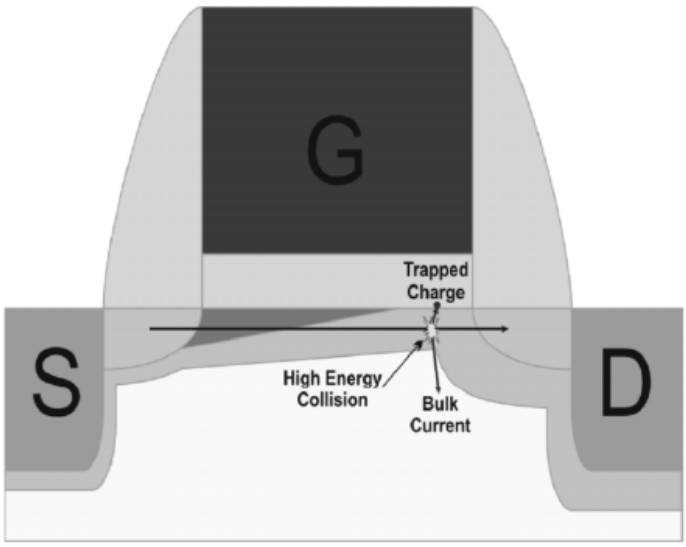


Figure 2.12: Hot carrier degradation in a MOS transistor [19]

2.4.3. PUNCH THROUGH

when a large enough gate bias is applied to create a inversion channel, the drain-to-source current of a MOS transistor flows close to the surface. If the gate bias is absent, very little current flows since the drain-bulk and the source-bulk diodes are effectively connected back-to-back with opposite polarities. When larger voltages are applied to the drain, the drain-bulk depletion region extends further to accommodate the electric potential drop. This depletion region will eventually extend all the way to meet the depletion region of the source-bulk junction, therefore diminishing the potential barrier that stops the direct flow of current between the drain and the source, as depicted in Figure 2.13(a). This punch-though process results in a current flow that can occur even in the absence of any significant gate bias (Figure 2.13(b)). In practice there is no need for the depletion regions to touch. Even when they approach each other, the potential barrier height drops, increasing current from one side to the other. Punch-though is exacerbated by smaller channel length, and larger drain-to-source voltage. The significance of punch-through reduces rapidly with increasing channel length [19].

Punch-through is not intrinsically destructive, although the simultaneous occupance of high voltage and high current can easily result in thermal failure if sustained. However, the process can generate its own hot carriers, potentially causing similar reliability issues as previously discussed. From a design perspective, punch-through can be dealt with by making sure that of a single transistor remains at all times below a certain pre-specified value for any given channel length [19].

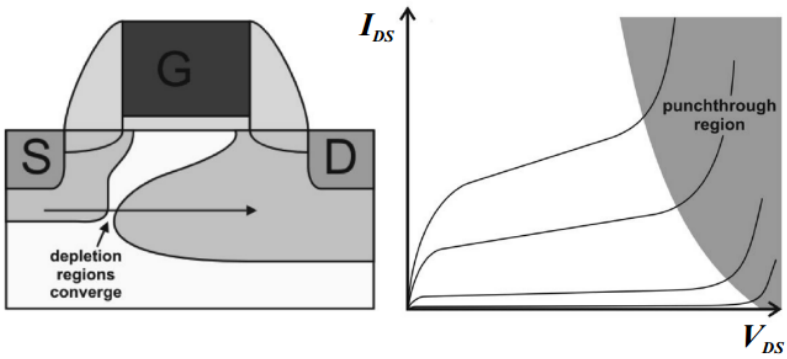


Figure 2.13: Punch-through in a MOS transistor [19]

2.4.4. DRAIN-BULK BREAKDOWN

The bulk in a standard CMOS process is connected to a fixed electrical potential and the drain-bulk diode experiences a reverse bias directly proportional to the absolute drain voltage. This diode has a reverse breakdown voltage primarily determined by the doping of the bulk (the lightly doped side). Thereby, it is significant to make sure that the drain-bulk voltage does not exceed this breakdown voltage in addition to maintaining smaller than its critical level. Fortunately, this breakdown voltage is relatively high in recent CMOS processes (e.g. 10 V in 65 nm CMOS).

2.4.5. AC OXIDE BREAKDOWN LIMIT

Among the previously discussed four MOS transistor life-time determining mechanisms, the gate-oxide breakdown has the most disastrous effect for switch-mode power amplifiers, especially at the gate-drain node (V_{GD}). For RF power amplifiers, the active device experience a high voltage across the gate-oxide only for a portion of the operation cycle, thus the exact limit to prevent oxide breakdown seems difficult to determine. Typically gate oxide breakdown has been investigated under DC conditions, where large field is applied to accelerate the breakdown so as to predict the maximum voltage for safe operation [21]. However, it turns out that the active devices exhibit different breakdown limits under high frequency conditions. According to [22], the gate oxide lifetime increased by ten times if the transistor is subjected to AC instead of DC stressing. Unfortunately AC oxide breakdown testing is not included in the standard characterization in production CMOS at this moment [20].

Due to the lack of an AC oxide breakdown standardization, different maximum limits

for the supply voltage from several authors are used even for the same power amplifier class. For instance, [23] employed $1.1 \times V_{DD,nom}$ in 65nm CMOS, [20] chose $1.7 \times V_{DD,nom}$ in 0.35um CMOS while [24] preferred $2.0 \times V_{DD,nom}$ in 0.25um CMOS for a Class E power amplifier. The first two authers followed the same DC conservative limit aiming to restrict the electric field to about 0.6V/nm while the third auther employed the limit of 1V/nm, which is close to the intrinsic breakdown field (1.1V/nm) for SiO_2. Note that a difference of 70% exists in the electric field limit employed by these three authors.

The difference between AC and DC stressing reported in [22] provides an insight into the relative reliability of PAs with different voltage waveforms [20]. [21] concluded that the maximum RF voltage peaking for safe operation is much larger than the conventional DC limit by experimentally from the observation that the physical mechanism of oxide breakdown is triggered by the rms value of the oxide field instead of its maximum. However, most designers tend to employ the most conservative DC limits due to the lack of a commom consensus with respect to the AC oxide breakdown limit.

2.5. CONCLUSIONS

After an introduction of the main performance metrics in PAs. An overview of different classes of power amplifiers is presented with particular attention attached to Class E because their usage in our proposed design. It has been proved that if the active devices are not constrained by the reliability issues, then the parallel-circuit Class E will yield the highest output power for a given supply voltage and load. However, the high peak drain voltage, which is up to 3.6 times the supply voltage, poses a serious challenges for CMOS Class E implementing. In addition to decreasing the supply voltage , designing a Class E circuit in sub-optimum mode also benefits a reliable operation, which will be further discussed in Chapter 7.

3

TOWARDS ENHANCED EFFICIENCY: A NOVEL CLASS E BASED DIGITAL POLAR DOHERTY PA

Modern wireless communication systems employing complex digital modulation signals (e.g. W-CDMA and LTE/LTE-A) that can provide high data rates over restricted bandwidths tend to have high peak-to-average ratios (PAR). In order to linearly amplify these signals, the amplifier is often operated at a back-off region, resulting in a poor average efficiency. How to improve the average efficiency of the power amplifiers thus becomes a hot research issue. Among the various efficiency enhancement techniques, Doherty power amplifier has attracted a lot of research interest because of its enhance efficiency at power back-off (PBO).

This chapter, first reviews the basic operation of the Doherty PA. Conventionlly, the linear power amplifiers are employed in the branch amplifiers of a Doherty architecture. However, switch-mode PAs are potentially more efficient than their linear PA counterparts. Thus, a novel Doherty based on digitally-controlled Class E power amplifier is proposed for higher peak efficiency.

3.1. CONVENTIONAL DOHERTY PAS

The Doherty power amplier (DPA), first proposed in 1936 [25], is primarily an efficiency enhancement or power conservation technique. Traditionally, DPA, as shown in Figure 3.1, is implemented with two identical devices, namely the carrier or main and the peak or

auxiliary PA. Both ampliers with their outputs are combined by a quarterwave transformer forming a parallel combination. The quarterwave transformer acts as an impedance inverter, causing the resistive impedance seen by the main PA to drop as the current of peak PA increases. In this chapter, the theory of the DPA will be explained in detail. In addition, methods to extend the bandwidth of DPA is presented.

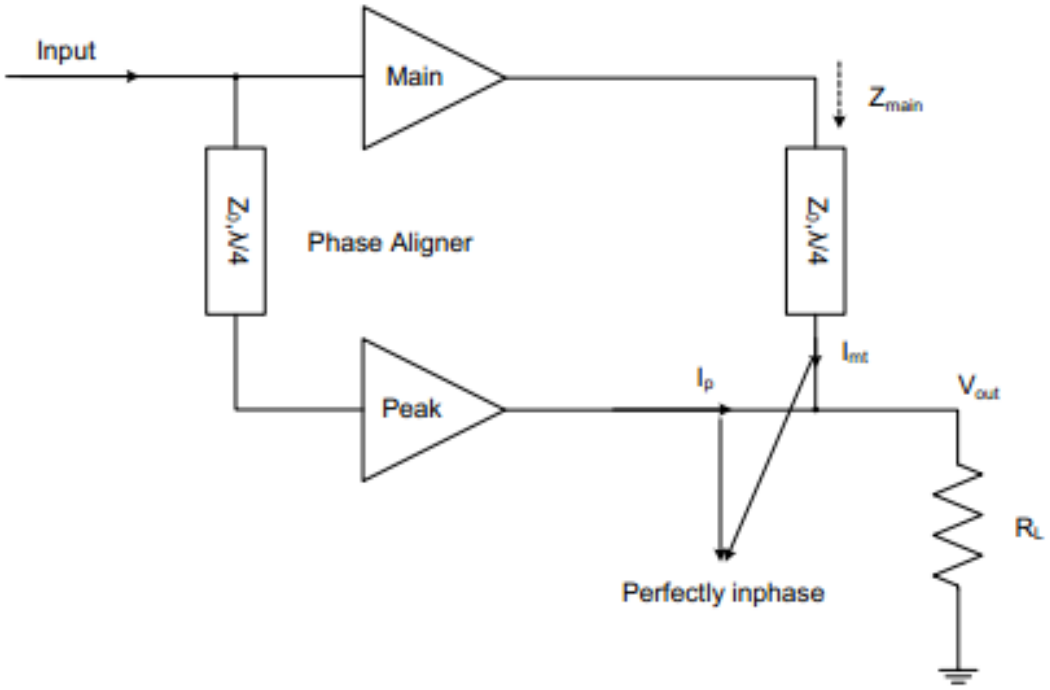


Figure 3.1: Basic Configuration of DPA

3.1.1. THE THEORY OF DOHERTY PAS

In order to analyze the DPA in Figure 3.1 mathematically, the two amplifiers are replaced by two ideal current source and thus we obtain the equivalent schematic shown in Figure 3.2. At low power level, where the input power is lower than the threshold of the peak amplifier, only the main amplifier is active. The impedance inverter transforms the load impedance to a higher value to boost the voltage swing across the drain of the main amplifier, thus yielding a higher efficiency. When the input power exceeds the threshold of the peaking amplifier, the peak amplifier starts to work, current generated from the peaking amplifier increases the voltage across the load impedance. Consequently, the impedance seen at the output of the impedance inverter is effectively larger than the actual component value. Through the impedance inverter, the impedance seen by the main amplifier will be pulled down and its output power can continue to increase with the increase of input power. This is what we called as load-pull technique. With the further increase of input power, the

output power increases until it reaches the peak power capability.

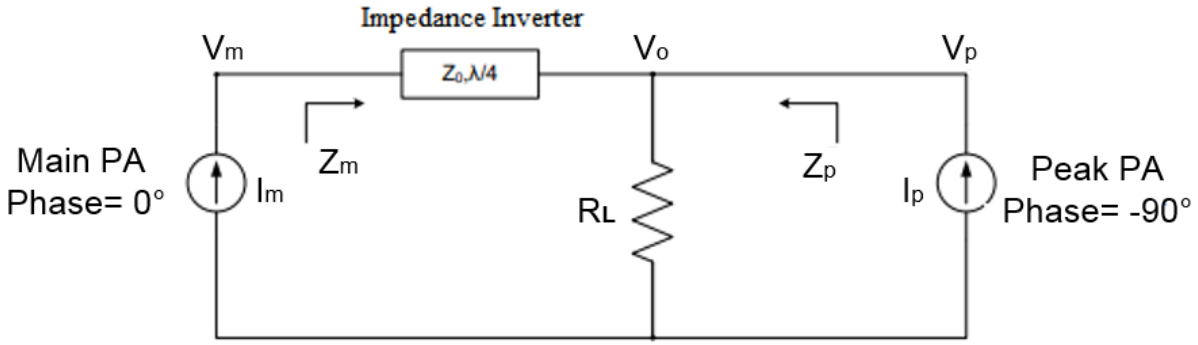


Figure 3.2: Equivalent circuit of a two-way symmetrical DPA

As shown in Figure 3.2, Z_0 is the characteristic impedance of the QWTL impedance inverter. V_m and I_m are the fundamental drain voltage and current of the main amplifier, while V_p and I_p are the fundamental drain voltage and current of the peak amplifier, respectively. V_o is the fundamental output voltage. Note that the current flowing out the main amplifier is delayed by the QWTL, therefore a phase lag of 90° is introduced in I_p to compensate the phase shift. Substitute I_p with $-jI_p$ and the two-port network of the impedance inverter can be expressed as (note $V_p = V_o$)

$$\begin{bmatrix} V_m \\ I_m \end{bmatrix} = \begin{bmatrix} 0 & jZ_0 \\ \frac{j}{Z_0} & 0 \end{bmatrix} \begin{bmatrix} V_o \\ \frac{V_p}{R_L} + jI_p \end{bmatrix} \tag{3.1}$$

From equation (3.1) the Z-matrix can be derived

$$\begin{bmatrix} V_m \\ V_p \end{bmatrix} = \begin{bmatrix} \frac{Z_0^2}{R_L} & -jZ_0 \\ -jZ_0 & 0 \end{bmatrix} \begin{bmatrix} I_m \\ -jI_p \end{bmatrix} \tag{3.2}$$

Derived from equation (3.2), the impedance seen from the drain of the main and peak amplifiers can be expressed as:

$$Z_m = \frac{V_m}{I_m} = \frac{Z_0^2}{R_L} - Z_0 \frac{I_p}{I_m} \tag{3.3}$$

$$Z_p = \frac{V_p}{I_p} = Z_0 \frac{I_m}{I_p} \tag{3.4}$$

From equation (3.1), the voltages of the main and peaking PA can be expressed as

$$V_m = Z_0(I_m(\frac{Z_0}{R_L}) - I_p) \tag{3.5}$$

$$V_p = V_o = -jZ_0 I_m \tag{3.6}$$

According to Equation (3.3) and (3.4), it is obvious that each current source experiences a load modulation due to another current source. In addition, equation (3.5) shows that the current I_p can be designed to keep the main amplifier voltage at the maximum level over a specified power range for high efficiency.

In the following discussion, a back-off parameter α is introduced and the peak amplifier starts to generate current I_p when $V_{in} \geq \alpha V_{in,max}$. V_{in} is the gate drive for both devices and $V_{in,max}$ is the maximum value that V_{in} can achieve. Since the current of both devices are controlled by their driving voltage, the main and peak devices are assumed to have the following transfer characteristics.

$$I_m = \begin{cases} 0 & \text{if } V_{in} < 0, \\ G_m V_{in} & \text{if } 0 \leq V_{in} \leq V_{in,max}, \\ G_m V_{in,max} & \text{if } V_{in} > V_{in,max}. \end{cases} \tag{3.7}$$

$$I_p = \begin{cases} 0 & \text{if } V_{in} < \alpha V_{in,max}, \\ G_p(V_{in} - \alpha V_{in,max}) & \text{if } \alpha V_{in,max} \leq V_{in} \leq V_{in,max}, \\ G_p(1-\alpha) V_{in,max} & \text{if } V_{in} > V_{in,max}. \end{cases} \tag{3.8}$$

where G_m and G_p are the transconductance of the main and peak amplifier.

Below the back-off point ($V_{in} < \alpha V_{in,max}$), the peak amplifier is off ($I_p = 0$) and only the main amplifier is turn-on. From equation 3.3 and 3.5, we can have:

$$Z_m = \frac{Z_0^2}{R_L} \tag{3.9}$$

$$V_m = I_m \frac{Z_0^2}{R_L} \tag{3.10}$$

At the back-off point ($V_{in} = \alpha V_{in,max}$), the main device becomes saturated with its drain voltage reaching its peak amplitude, which is equivalent to the drain bias voltage V_{dc}.

$$V_m = G_m V_{in} \frac{Z_0^2}{R_L} = G_m \cdot \alpha V_{in,max} \cdot \frac{Z_0^2}{R_L} = V_{dc} \tag{3.11}$$

Beyond the back off point ($V_{in} > \alpha V_{in,max}$), the peak amplifier starts to work. Due to load modulation, the drain voltage of main amplifier maintains constant so as to guarantee

a rail-to-rail swing to achieve high efficiency.

$$V_m = I_m Z_m = I_m(\frac{Z_0^2}{R_L} - Z_0\frac{I_p}{I_m}) = V_{dc} \tag{3.12}$$

$$V_p = I_p Z_p = I_p(Z_0\frac{I_m}{I_p}) = I_m Z_0 \tag{3.13}$$

At full output power point ($V_{in} = V_{in,max}$), both amplifiers experience full swing at the drain, whose amplitude is equal to the supply voltage V_{dc}.

$$V_{m,full} = G_m V_{in,max}(\frac{Z_0^2}{R_L} - Z_0\frac{G_p(1-\alpha)}{G_m}) = V_{dc} \tag{3.14}$$

$$V_{p,full} = G_p(1-\alpha)V_{in,max}Z_0\frac{G_m}{G_p(1-\alpha)} = V_{dc} \tag{3.15}$$

By solving equation (3.12)(3.14)(3.15), the current and transconductance ratio of the main and peak device can be figured out as follows

$$\frac{Z_0}{R_L} = \frac{G_p}{G_m} = \frac{1}{\alpha} \tag{3.16}$$

$$\frac{I_{m,max}}{I_{p,max}} = \frac{\alpha}{1-\alpha} \tag{3.17}$$

3.1.2. IDEAL DOHERTY PA PERFORMANCE

The analysis in the previous subsection shows that in DPA operation, the effective transconductance ratio of the main and peak amplifier should be α, if we want to utilize their full current capacity. In this section, Equations (3.18) and (3.19) show the possibility to control the drive voltage of both amplifiers to guarantee the same device property and the full output capacity utilization of DPA.

$$V_{in,m} = V_{in} \tag{3.18}$$

$$V_{in,p} = \begin{cases} 0 & \text{if } V_{in} < \alpha V_{in,max}, \\ \frac{1}{\alpha}(V_{in} - \alpha V_{in,max}) & \text{if } \alpha V_{in,max} \le V_{in} \le V_{in,max}. \end{cases} \tag{3.19}$$

This approach is called as mixed-signal drive and has been proven to be useful in [6, 26–29]. Assuming the models are all linear (then we have $G_m = G_p$), the biasing point is also set at the value that the main device is working in linear region. If Z_0 and R_L satisfies the relation $Z_0 = R_L/\alpha$, the characteristic of this DPA can be described using the following equations.

BRANCH AMPLIFIER CURRENT

First, the drain current for the main amplifier can be expressed as

$$I_m = G_m V_{in} \tag{3.20}$$

And the drain current for the peak amplifier beyond the back-off point can be calculated as

$$I_p = \frac{G_m}{\alpha}(V_{in} - \frac{V_{in,max}}{\alpha}) \tag{3.21}$$

When $\alpha = 0.5$, we can obtain the normalized drain current shown in Figure 3.3.

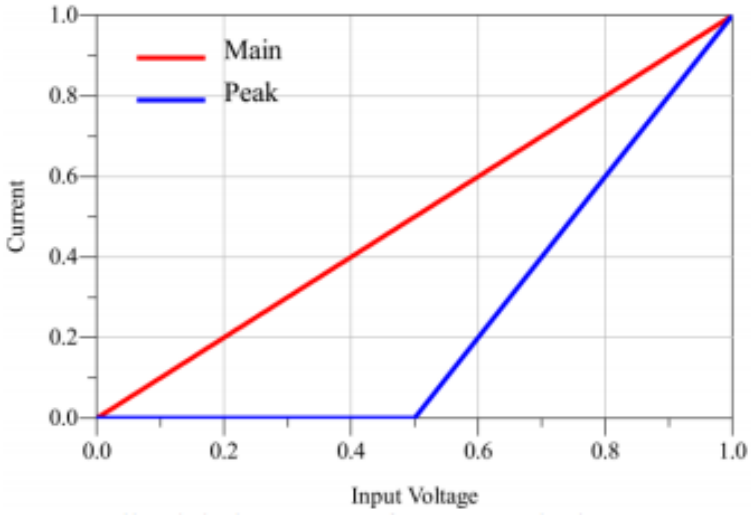


Figure 3.3: Normalized drain current of a symmetrical two way DPA

BRANCH AMPLIFIER VOLTAGE

Below the back-off point ($V_{in} < \alpha V_{in,max}$), the peak amplifier is off (I_p=0). We can calculate the voltage of the main amplifier from equation (3.5) and (3.20)as

$$V_m = I_m \frac{Z_0^2}{R_L} = (\frac{G_m Z_0}{\alpha}) \cdot V_{in} \tag{3.22}$$

At the back-off point ($V_{in} = \alpha V_{in,max}$), we have

$$V_m = (G_m Z_0) \cdot V_{in,max} = V_{dc} \tag{3.23}$$

Beyond the back-off point ($V_{in} > \alpha V_{in,max}$), the peak amplifier starts to work and through load modulation, the voltage of the main amplifier remains constant. Hence from Equation

3.5, 3.20 and 3.21, we can get

$$V_m = Z_0(I_m(\frac{Z_0}{R_L}) - I_p) = V_{dc} \tag{3.24}$$

$$V_p = V_o = I_m Z_0 = (G_m Z_0) \cdot V_{in} \tag{3.25}$$

When $\alpha = 0.5$, the normalized voltage of the main and peak amplifiers is depicted in Figure 3.4.

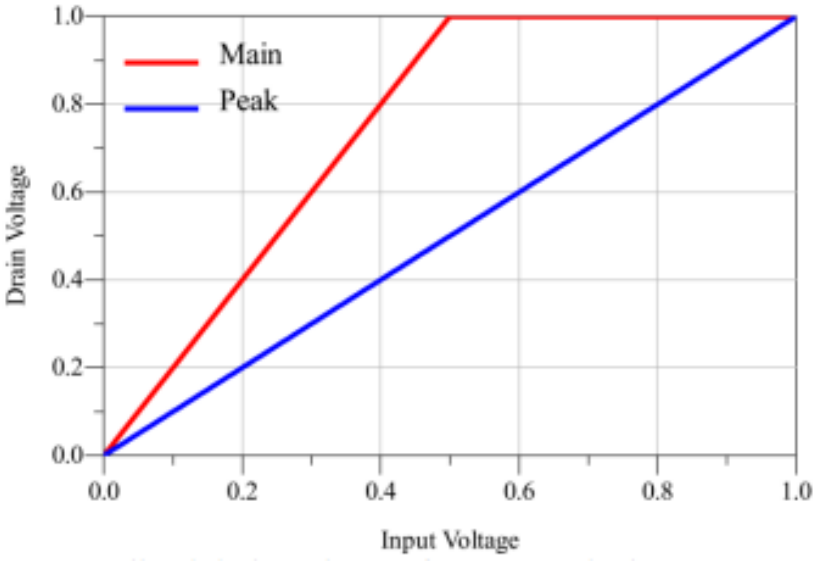


Figure 3.4: Normalized drain voltage of a symmetrical two way DPA

BRANCH AMPLIFIER IMPEDANCE

From equation (3.3),(3.16) and (3.9), the impedance seen by the main amplifier can be expressed as

$$Z_m = \begin{cases} \frac{Z_0}{\alpha} & \text{if } V_{in} < \alpha V_{in,max}, \\ \frac{Z_0}{\alpha} - \frac{(V_{in} - \alpha V_{in,max}) Z_0}{\alpha V_{in}} & \text{if } \alpha V_{in_max} \leq V_{in} \leq V_{in,max}. \end{cases} \tag{3.26}$$

From equation (3.4) and (3.16), the impedance seen by the peak amplifier can be calculated as

$$Z_p = \begin{cases} \infty & \text{if } V_{in} < \alpha V_{in,max}, \\ \frac{\alpha V_{in} Z_0}{V_{in} - \alpha V_{in,max}} & \text{if } \alpha V_{in_max} \leq V_{in} \leq V_{in,max}, \end{cases} \tag{3.27}$$

When $\alpha = 0.5$, we can obtain the normalized impedance seen by the main and peak amplifiers in Figure 3.5.

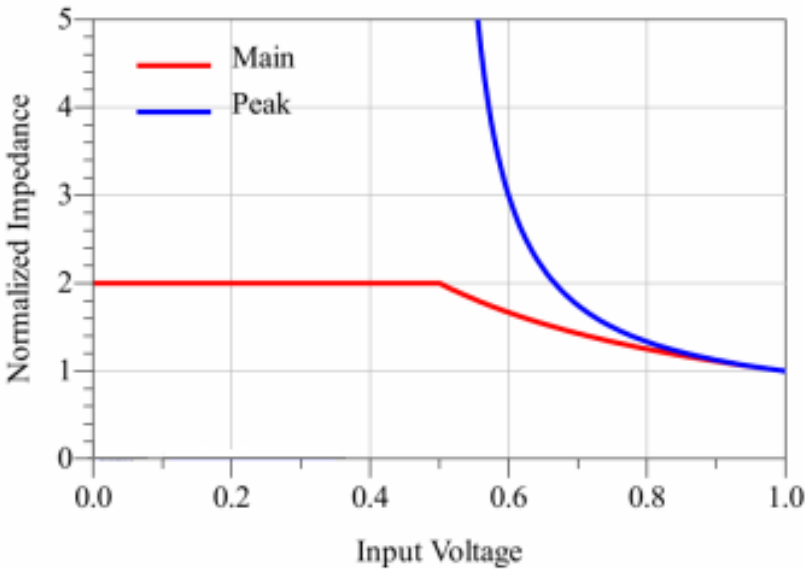


Figure 3.5: Normalized impedance of a symmetrical two way DPA

OUTPUT POWER

Assuming that both the main and peak amplifier are working at class B mode. From the discussion in chapter 2 we know that:

$$I_{dc} = \frac{2}{\pi} I_1 \tag{3.28}$$

where I_1 means the magnitude of the corresponding fundamental component. Below the back-off point ($V_{in} < \alpha V_{in,max}$), the peak amplifier is off (I_p=0) and only the main amplifier works. Thus

$$P_{out} = P_{main} = \frac{V_o^2}{2R_L} \tag{3.29}$$

From Equation 3.5, 3.6 and 3.16, the magnitude seen by the main amplifier I_m can be expressed in terms of V_0 as

$$I_m = \frac{\alpha V_{dc} V_o}{R_L} \tag{3.30}$$

Thus the DC power can be calculated as

$$P_{dc} = V_{dc} I_{dc} = \frac{2}{\pi} \frac{\alpha V_{dc} V_o}{R_L} \tag{3.31}$$

After the back-off point ($V_{in} > \alpha V_{in,max}$), the peak amplifier starts to operate, therefore

$$\begin{aligned} P_{out} &= P_{main} + P_{peak} \\ &= \frac{1}{2} I_m^2 \left(\frac{Z_0^2}{R_L - Z_0 \frac{I_p}{I_m}}\right) + \frac{1}{2} I_p^2 \left(Z_0 \frac{I_m}{I_p}\right) \\ &= \frac{1}{2} I_m^2 \frac{Z_0^2}{R_L} \end{aligned} \tag{3.32}$$

which means DPA shows a linear power amplification characteristic.

$$P_{dc} = V_{dc} I_{dc} = \frac{2}{\pi} V_{dc} (I_m + I_p) = \frac{2}{\pi} \frac{V_{dc}}{R_L} (\alpha V_o + V_o - \alpha V_{dc}) \tag{3.33}$$

When $\alpha = 0.5$, the output power of the symmetrical two way DPA can be presented in Figure 3.6.

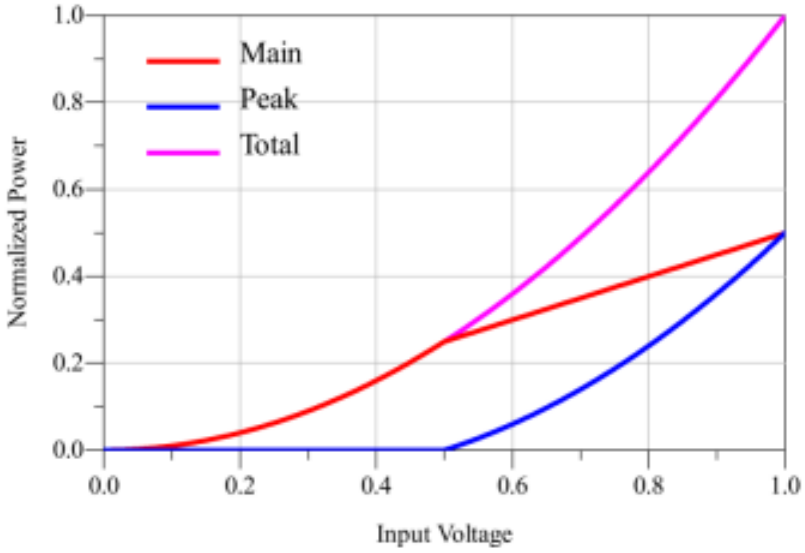


Figure 3.6: Output power of a symmetrical two way DPA

EFFICIENCY

Below the back-off point ($V_{in} < \alpha V_{in,max}$),

$$\eta = \frac{\pi}{4} \frac{V_o}{\alpha V_{dc}} \tag{3.34}$$

Beyond the back-off point ($V_{in} > \alpha V_{in,max}$),

$$\eta = \frac{\pi}{4} \frac{(\frac{V_o}{V_{dc}})^2}{(\frac{V_o}{V_{dc}})(\alpha + 1) - \alpha} \tag{3.35}$$

When $\alpha = 0.5$, the efficiency performance of the symmetrical two way DPA can be depicted in Figure 3.7.

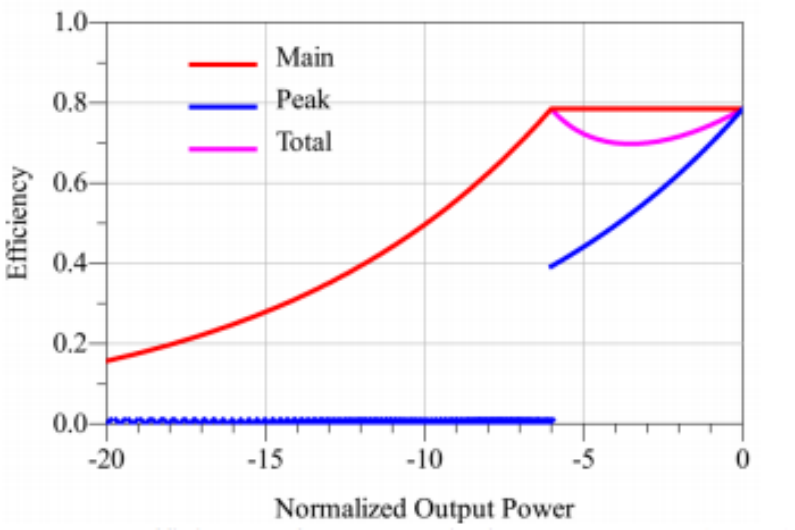


Figure 3.7: Efficiency of a symmetrical two way DPA

3.2. A NOVEL DOHERTY PA BASED ON DIGITALLY-CONTROLLED CLASS E

Switching power amplifiers (e.g. Class D and E) have higher efficiency compared with their linear counterparts (Classes A/AB/B/C etc.), thus employing high efficient switch-mode PAs, for instance Class E, in a Doherty power amplifier is a promising solution to higher peak efficiency. However, the switched-mode power amplifiers are non-linear in terms of amplitude, thus they cannot be directly applied in systems which employ spectrally efficient modulation. But these amplifiers are able to process constant-envelope input signals (with varying frequency or phase) since the switched-mode power amplifiers exihibite linearity in phase. Based on this property, a digital polar Doherty PA based on Class E topology is proposed in this design.

3.2.1. INTRODUCTION TO DIRECT DIGITAL POLAR MODULATION

Before moving to digital polar modulation, let us first review the principle of polar modulation. Generally speaking, in a typical polar modulator, a phase-modulated (PM) signal with constant envelope is amplified to the desired power level, whilst amplitude modulation (AM) is reconstructed only at the circuit output stage through the PA supply modulation. Because the non-linear envelope is conveyed by supply modulation, a non-linear switching PA (class-D, class-E, class-F and etc) can be employed to amplify the constant-envelope

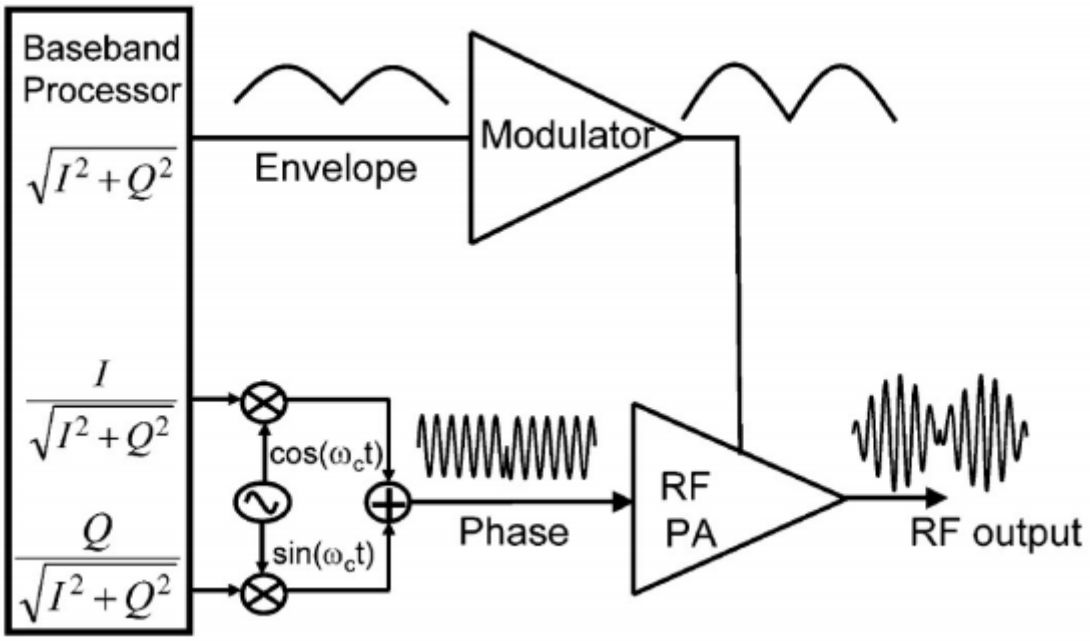


Figure 3.8: A typical polar modulated transmitter architecture [30]

and phase-modulated signal at its input, resulting in higher efficiency compared to its linear counterpart (Classes A/AB/B/C etc.). However, this analog polar modulation system as shown in Fig 3.8 exhibits certain disadvantages. First, the bandwidth requirement for the supply modulator may be much more (3-10x) than the corresponding BB (baseband) signal bandwidth due to bandwidth expansion from Cartesian to polar conversion [31]. In addition, their phase and amplitude paths exploit heterogeneous circuits whose delays must be accurately aligned in order to avoid spectral distortion at the final recombining stage, otherwise it will yield spectral re-growth [32]. Last but not the least, the conventional analog-intensive transmitters do not benefit significantly from technology scaling. Although transistor size shrinks every generation, the passives do not scale well with technology [33]. Here, a polar TX with direct digital amplitude modulation [34–38] has been proposed to address these issues.

Instead of depending on a high-bandwidth supply modulator to convey the nonlinear envelope as in a traditional analog-intensive polar TX, a direct digitally modulated polar TX achieves the amplitude modulation by turning on and off a large array of unit PA cells in the digital envelope modulator as illustrated in Figure 3.9. With this method, the digital modulation is applied directly to the PA , which is different from a conventional TX where the digital modulation first acts on the baseband DAC and is then fed to the PA through several intermediate stages. Consequently, the baseband DAC and the up-conversion mixer in a conventional Cartesian TX are no longer required on the amplitude path of the digital

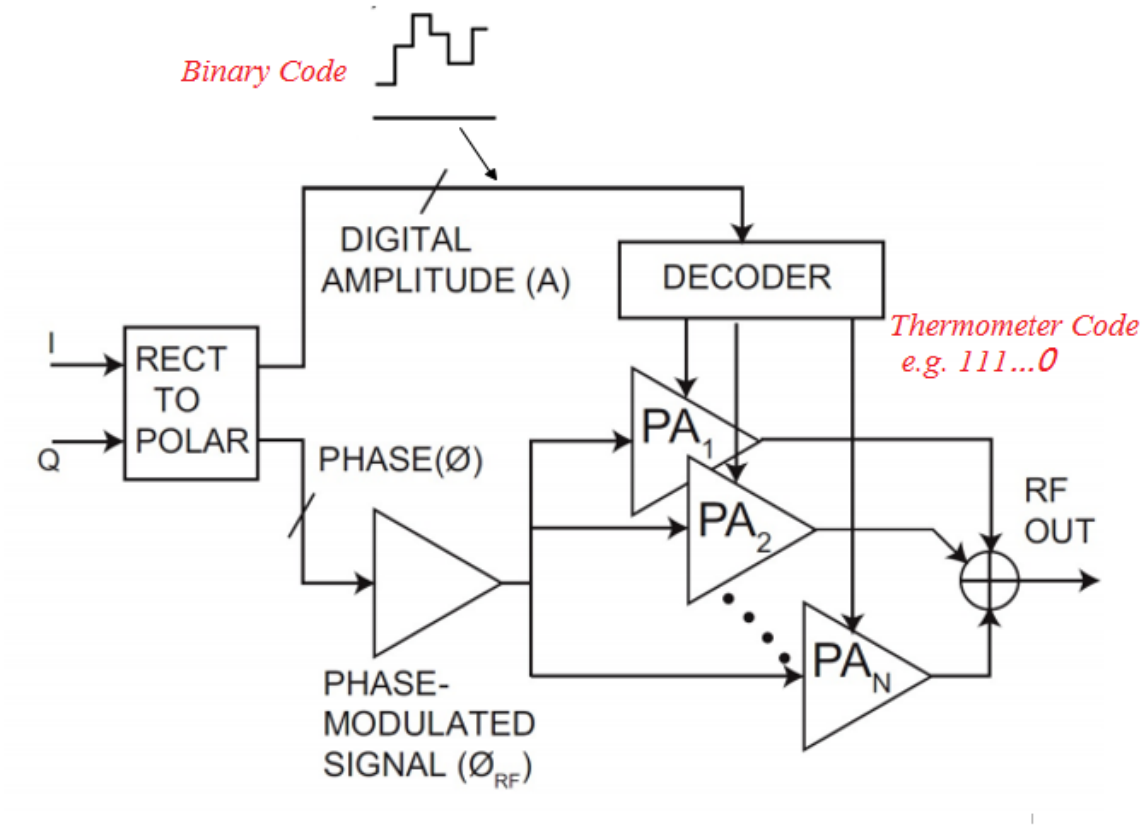


Figure 3.9: A polar TX with direct digital amplitude modulation [37]

polar TX system, which results in the decrease of the overall TX power consumption. Moreover, the predistortion can be applied more efficiently and accurately because the amplitude modulation and predistortion are directly applied to the final PA stage without going through the DAC, the filter, the up-conversion mixer, and the PA driver as in a conventional TX chain. Last but not the least, since the PA cell in a direct digitally modulated polar TX is also driven by a constant-envelope RF signal, the PA can be implemented using high-efficiency switch-mode classes, for example, Class E PAs for high peak efficiency [38].

3.2.2. DIGITAL DOHERTY PAS USING CLASS E BRANCH AMPLIFIER

Doherty PA employing switch-mode Clas E amplifiers for both main and peak branch amplifiers are feasible once the digital polar modulation technique is employed. Additional benefit of the digital polar Doherty scheme is the accurate control it provides over the turn-on and gain of the peaking amplifier relative to the main amplifier.

As discussed in the previous section, the desired Doherty PA operation highly depends

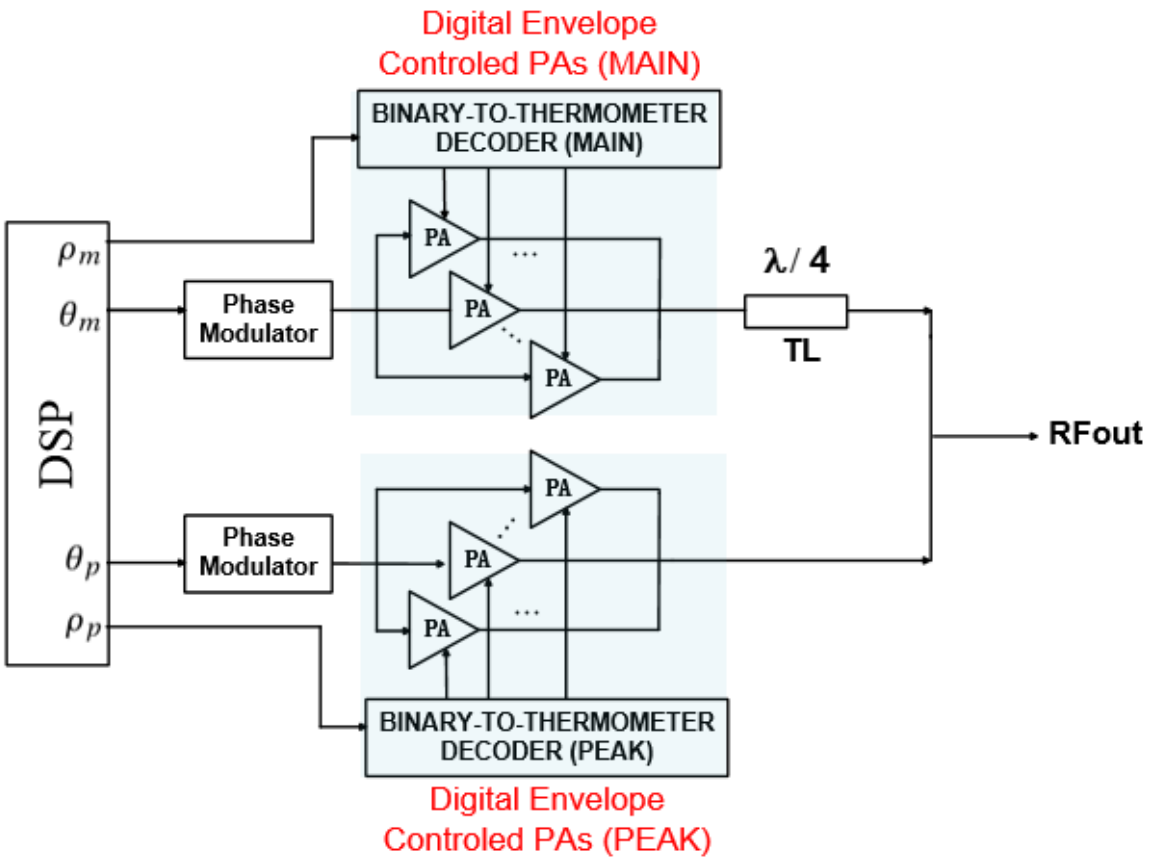


Figure 3.10: System schematic for the proposed digital polar Doherty PA

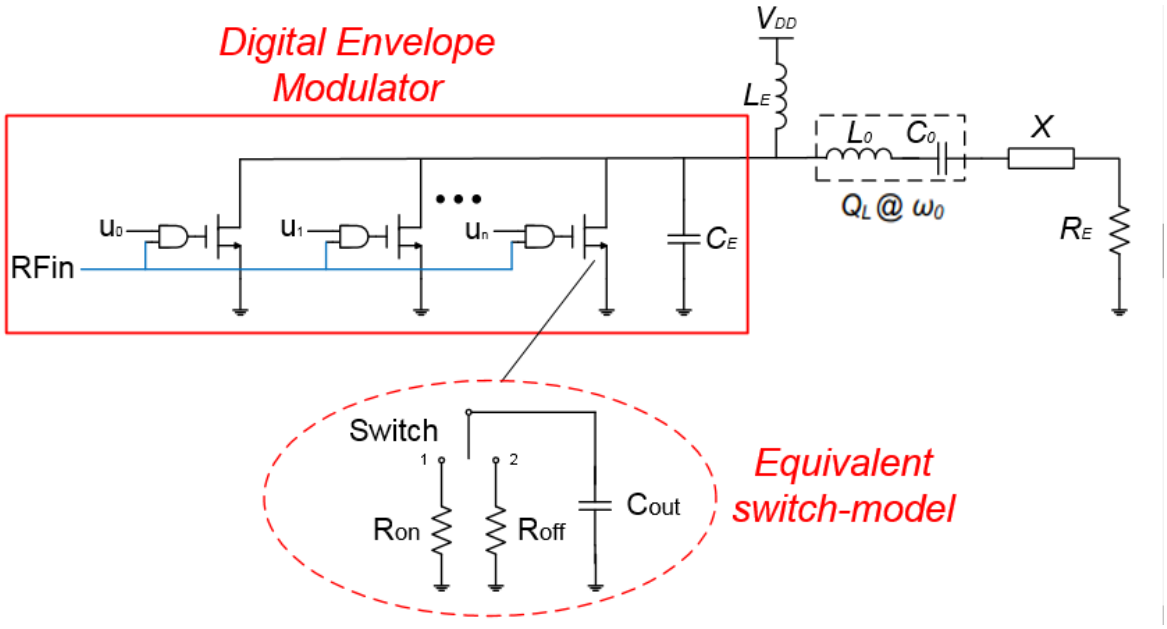
on the cooperation between the two branch PAs, especially the turning-on point and the transconductance of the peak PA with respect to the main PA. It is challenging to satisfy these in analog Doherty PAs. Biasing the auxiliary PA with a smaller conduction angle compared with the main PA is a conventional approach to mimic the Doherty PA operation. Additional analog techniques including uneven input power splitting, asymmetrical main and auxiliary amplifiers, and dynamic biasing have been reported to improve the analog Doherty PA performance. Most techniques, nevertheless, rely on dedicated tuning and lack the flexibility for in-field adjustment. Consequently, achieving desired cooperation between the two branch amplifiers remains elusive in practice. A digital polar architecture for Doherty PAs can address this issue [39].

Figure 3.10 depicts the system-level schematic of the proposed digital polar Doherty PA. Different from analog Doherty PAs, in the digital polar Doherty PA, both main and auxiliary PAs are digitally controlled by the envelope signal. Consequently, the auxiliary PA turning-on point and the two PAs'gain/transconductance relationship can be precisely controlled using the digital settings. This leads to a fundamentally improved Doherty operation and

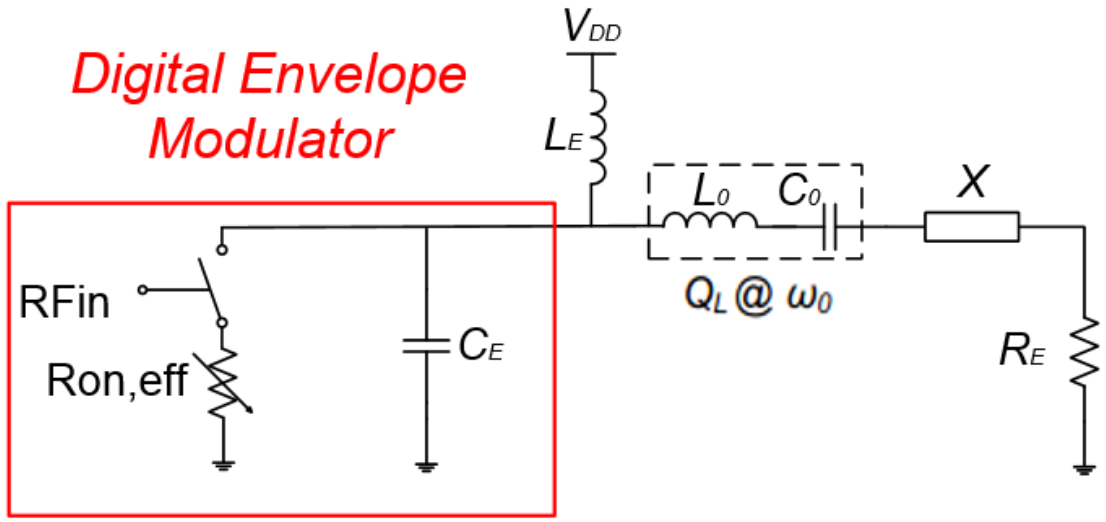
hence enhanced PBO efficiency compared with analog Doherty PAs.

This section presents the discussion of the basic principle as well as the efficiency performance for the proposed Doherty PA.

BASIC PRINCIPLE



(a)



(b)

Figure 3.11: (a) Simplified schematic (b) Equivalent schematic for digitally-controlled Class E

Let us start with the digital controlled Class-E PA to explain the basic operation of the proposed digitally-controled Class E based Doherty PAs. For a class-E PA, the transistor

operates as a switch, and its output power is determined by the load resistor and supply voltage, rather than its input power. Thus, amplitude modulation in this case can not be realized by directly applying a amplitude-varying signal at the input as in linear power amplifiers. However, we can ultilise the on-resistance of the active devices (Ron) to make a difference. Figure 3.11 (a) depicts a simplified schematic of digital controlled Class E PA, where a great number of unit cells (Each unit cell is composed of an AND gate and a large transistor) are connected in parallel. As memtioned in the subsection, the signal in a digital polar modulator is directly decomposed into a digital amplitude component and a phase component. After the decoder (Fig 3.8), the binary digital amplitude signal is converted into a thermometer signal to control the on/off a large array of unit cells. When the thermometer code applied to the AND gate of unit cell is high, the PA transistor starts to operate in respond to the phase signal. When the thermometer code applied to the AND gate of unit cell is low, the phase signal fails to reach the input of the PA transistor and therefore the transistor does not work. With this method, the number of ON transistors are varying according to the digital amplitude signal. Figure 3.11 (b) presents the equivalent circuit for this digital controlled Class E PA as shown in Figure 3.11 (a), where the array of unit cells are represented by an ideal switch in series with a resistor $R_{on,eff}$. The resistor $R_{on,eff}$ modeling the on-resistance of the switch is amplitude controlled and the value in the case of identical transistors can be expressed as

$$R_{on,eff} = R_{on}/n \tag{3.36}$$

where R_{on} is the on-resistance of a single transistor, and n is the number of working (or ON)transistors. And the capacitor C_{out} includes all capacitance at the transistor output. The LC bandpass filter is tuned to the switching frequency of the amplifier serveing as an open impedance for all harmonics so that it achieves significant harmonic suppression. With the digital approach to control the effective $R_{on,eff}$, the output power can change depending on the input. And the nonlinearity relationship between the input and output can be reduced or eliminated with the help of Pre-distortion.

Figure 3.12 presents the comparisons of output power and efficiency changes according to the input between the conventional analogue approach and the novel digital approach. The conventional analogue approach (varying input amplitude) fails to react to the input amplitude in a effective way while the digital approach (varying the on-resistance of switch arrays) achieves succefully amplitude modulation. Therefore, by turning on a dynamically varying number of unit elements to control the effective Ron, the output power can change in respond to the input, thus a Class-E based Doherty PA is feasible.

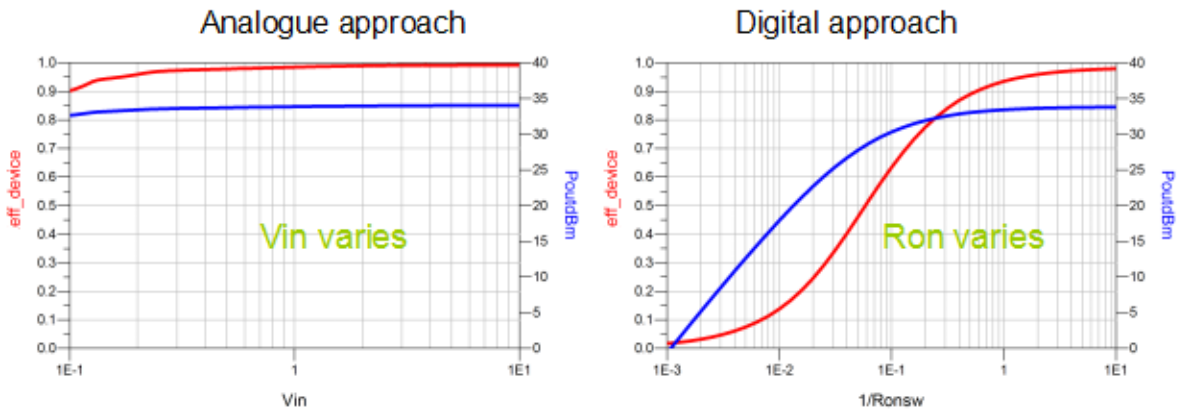


Figure 3.12: Comparisons of Output power and efficiency performance for Class E using analogue and digital approach

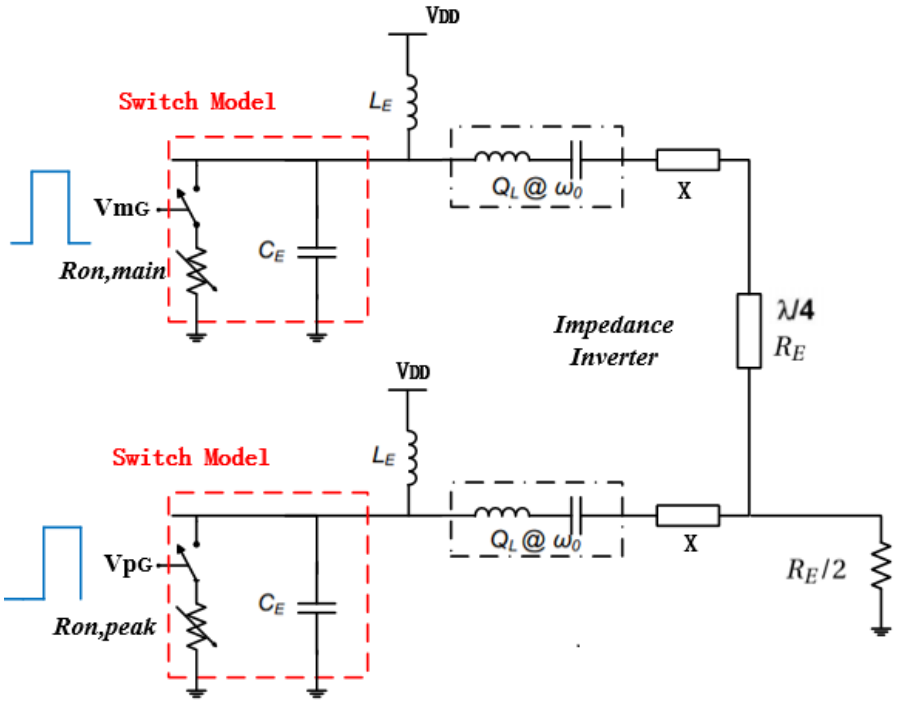


Figure 3.13: Basic schematic for Class E based digital DPA

Figure 3.13 shows the equivalent circuit of the proposed Digital Doherty PA employing the class-E topology, where the transistor arrays are replaced by the same switch model as in Figure 3.11 and $R_{on,main}$ represents the on-resistance of the switch in the main path while $R_{on,peak}$ represents the on-resistance of the switch in the peak path. Assuming that both $R_{on,main}$ and $R_{on,peak}$ vary from 1000 to 0.1. We can obtain the efficiency-output power characteristics as shown in Figure 3.14. At the very beginning, the input power is quite small, thus the peak amplifier does not work and $R_{on,peak}$ of the peak amplifier is in its maximum 1000 ohm. With the increase of the input power, $R_{on,main}$ of the main

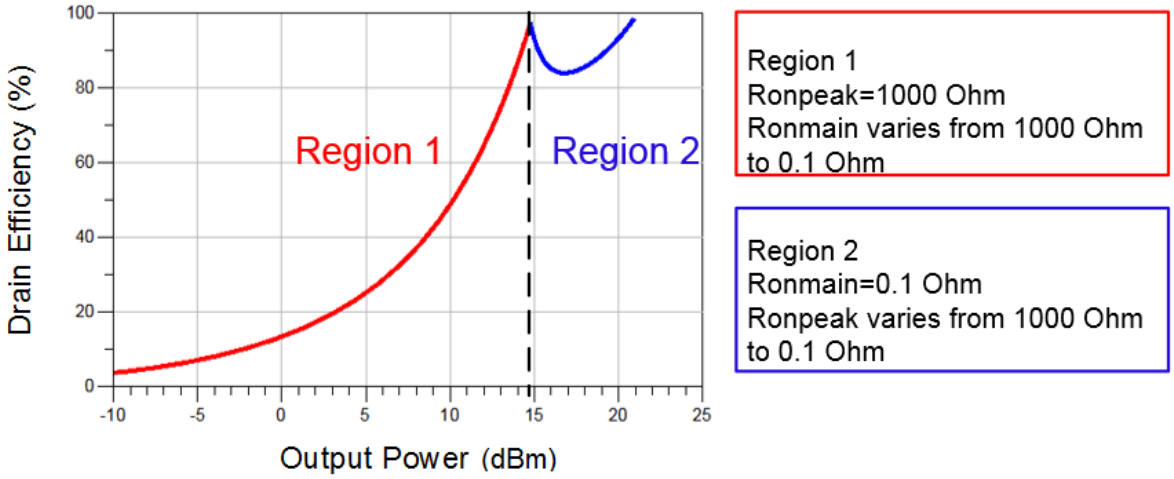


Figure 3.14: Efficiency output power characteristics for segmented Class E based digital DPA

branch ranges from 1000-0.1, which results in the increase of output power and efficiency. When the on-resistor of the main amplifier reaches its minimum value 0.1, the efficiency we get is 96.9%, which is close to the theoretical 100%. Then $R_{on,peak}$ of the peak amplifier decreases from 1000 to 0.1 with further increase of input, another efficiency peak reaches when on-resistor of the peak amplifier is also 0.1 and it delivers 98% efficiency. In addition, the output power difference between these two efficiency peak point is about 6dB. Compared with the conventional DPA, it is obvious that the digital controlled class-E based DPA can potentially achieve both high peak efficiency and enhanced PBO efficiency.

LOAD-INSENSITIVE CLASS E PAS FOR DOHERTY

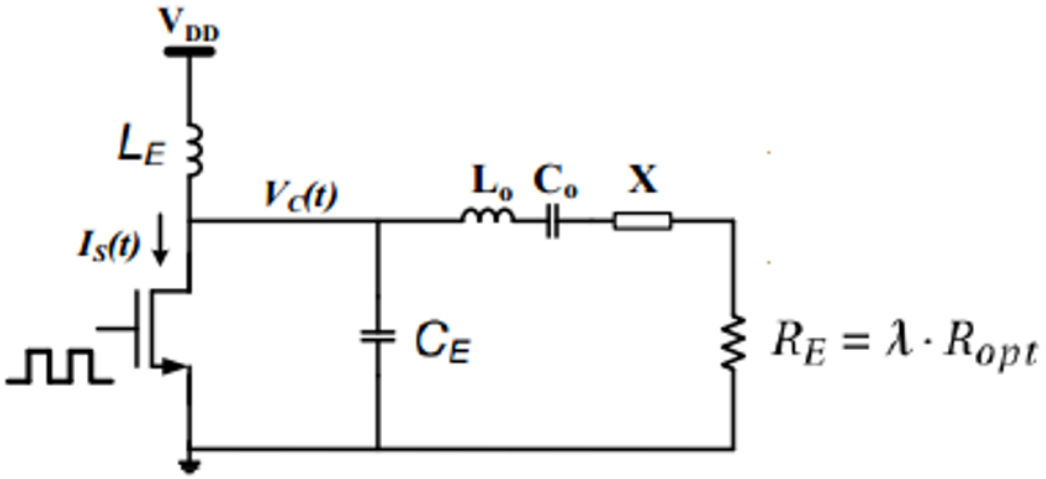


Figure 3.15: Generic class-E PA schematic with load modulation.
R_E is the optimum load and λ is the outphasing load-modulation factor.

Doherty PA is a well-known load-modulation technique. For a symmetrical two-way

Doherty PA, the normalized impedance seen by the main amplifier decreases from 2 to 1 while the normalized impedance seen by the peak amplifier decreases from infinite to 1 as the input voltage changes, as depicted in Figure 3.5. In order to handle the high dynamic load modulation without compromising its performance, Doherty PA tends to employ "load-insensitive" branch amplifiers. Thus in this specific case (Class E based doherty PA), "load-insensitive" switch-mode Class E is benefical for the average efficiency.

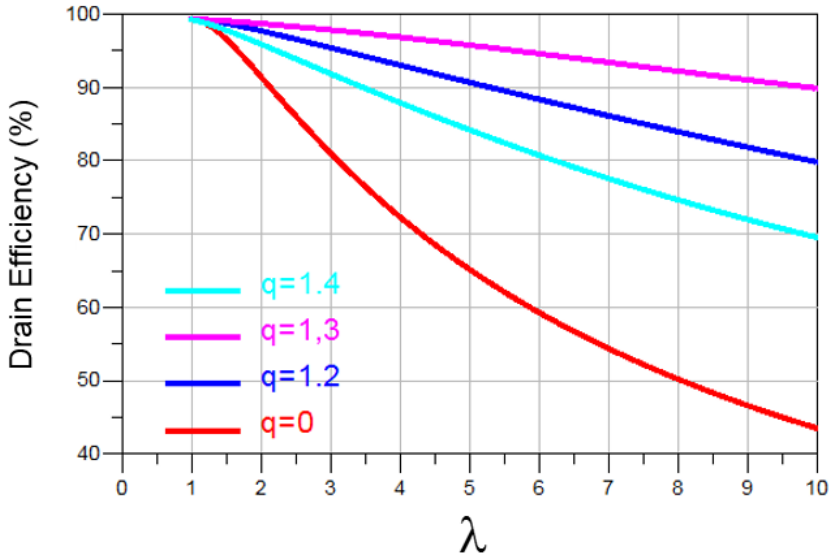


Figure 3.16: Simulated drain efficiency versus load-modulation factor for Class-E PAs with $Q_L = 10$

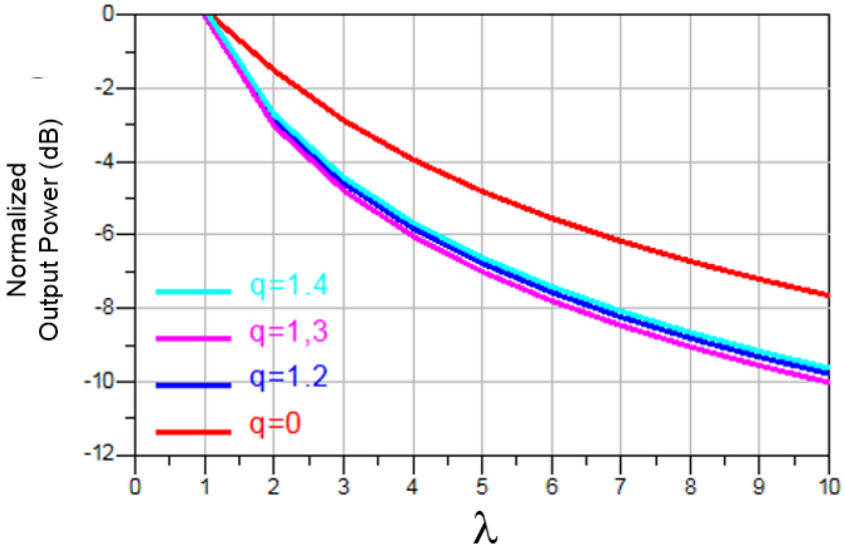
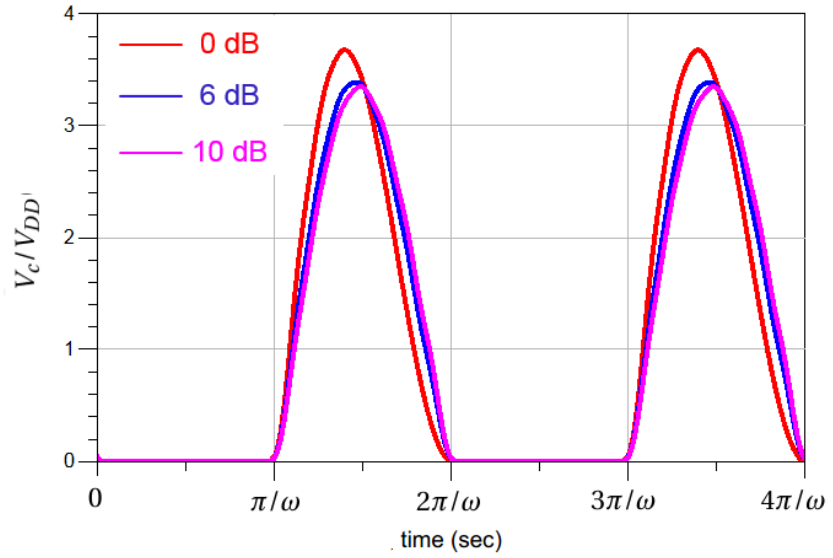


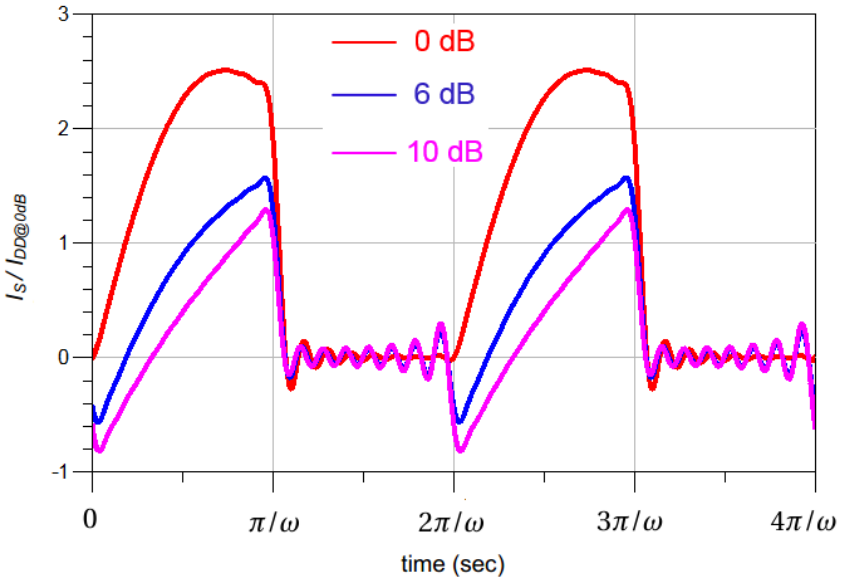
Figure 3.17: Simulated output power versus load-modulation factor for Class-E PAs with $Q_L = 10$

The concept of "load-insensitive" Class E, first proposed in [17] can be explained using the generic schematic in Figure 3.15, where the active device is assumed as an ideal switch.

To simplify the analysis, the load of this Class E PA in a Doherty topology is considered to be ohmic and to change according to $R_E = \lambda \cdot R_{opt}$, where R_{opt} is the optimum load determined by the optimum Class E loading condition and λ is the Doherty load-modulation factor. In addition, the quality factor Q_L of the series LC bandpass filter (BPF) is defined for the optimum R_{opt}.



(a)



(b)

Figure 3.18: (a) Normalized voltage and (b) normalized current waveforms at the intrinsic switch of the load-insensitive class-E PA ($Q_L = 10$) at 0, 6, and 10 dB back-off power (i.e.,λ=1, 4, and 10, respectively).

The simulation reults for drain efficiency and output power of the Class E power amplifier in Figure 3.15 are plotted in Figure 3.16 and Figure 3.17, respectively. It can be observed that the load-insensitive Class E PA ($q = 1.3$) indeed maintains its high efficiency

for large load modulation range compared to the other class-E amplifier implementations using different q values. The reason can be explained by refering to Figure 3.18 [16]. It can be observed in Figure 3.18 that when the load resistance varies from its nominal ($\lambda = 1$) to a much higher value ($\lambda >> 1$),the turn-on voltage-slope changes from zero to a negative value while still keeping its turn-on voltage close to zero (i.e., it enters into variable-slope operation). Because the voltage at turn-on point maintains close to zero, meanwhile the peak current through the switch reduces with back-off at the same turn-on moment, there is no overlapping between the voltage and current waveforms and the resulting efficiency will be preserved for the varying load conditions that will occur in a Doherty PA [16].

To verify the above assumption, the effect of design parameter q on the efficiency performance of a Doherty amplifier is investigated. There are two extreme case in the proposed Doherty PA, as depicted in Figure 3.13. One is at back-off level where all the PA unit cells in the main path are turned on, the resulting $R_{on,main}$ is in its minimum value and the fundamental load impedance seen by the main PAs are calculated as $\frac{R_E^2}{R_E/2}$ because of the $\lambda/4$ QWTL impedance inverter. The other one is at full power level where the peak PAs are also included and it delivers the same current to the load as the main PAs, thus the main PAs and the peak PAs see the same fundamental impedance given by R_E. First, we investigate how the efficiency-output power characteristics change when the branch Class E PA is designed refering to different matching condition. In this test, the load resistor R_E remains the same, but the circuit element including the output capacitor C_E and DC-feed inductance L_E changes according to the equations as follows

$$L_E = \lambda \cdot \frac{K_L R_E}{\omega} \tag{3.37}$$

$$C_E = \frac{1}{\lambda} \cdot \frac{K_L}{\omega R_E} \tag{3.38}$$

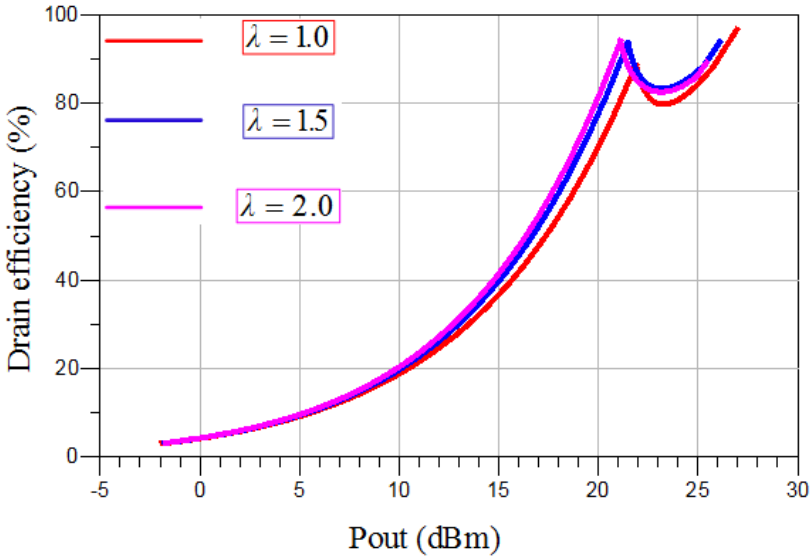
where λ is defined as the normalized impedance (with respect to R_E) seen by the main PA and it ranges between 1 and 2 for the symmetrical Doherty PA in Figure 3.13. The simulation results in Figure 3.19 indicate that Class E designed refering to $\lambda = 1.5$ has larger average efficiency compared to Class E designed referring to $\lambda = 2.0$ and higher achievable output compared to Class E designed refering to $\lambda = 1.0$.

Next, the Class E circuit is designed for $\lambda = 1.5$ and the efficiency-output power characteristics with different q is plotted in Figure 3.20. It can be observed that Class E PA with finite dc-feed inductance ($q = 1.3, 1.4$) is more tolerance of the load modulation than that with infinite dc-feed inductance ($q = 0$). Note that $q = 1.3$ indeed provides large efficiency in respond to the change output power, but when q deviates a little from 1.3, the resulting

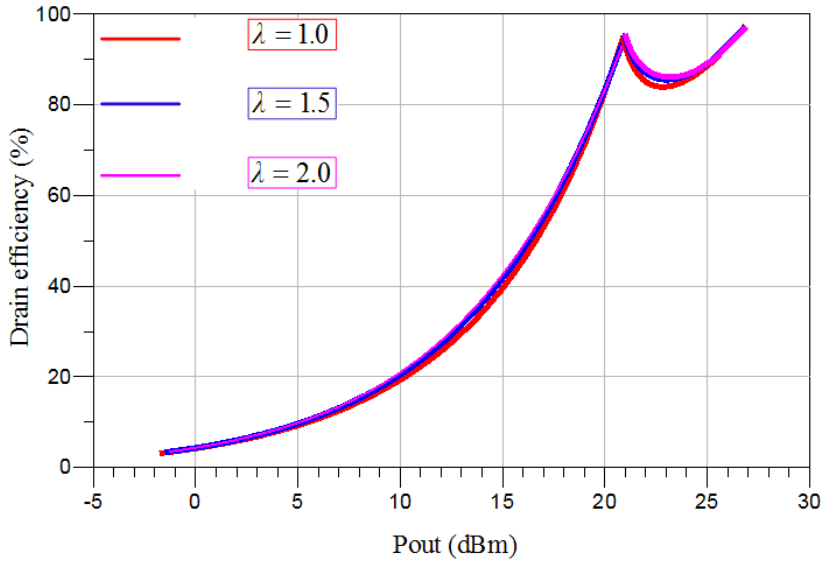
efficiency-output power characteristics are still excellent.

3.3. CONCLUSIONS

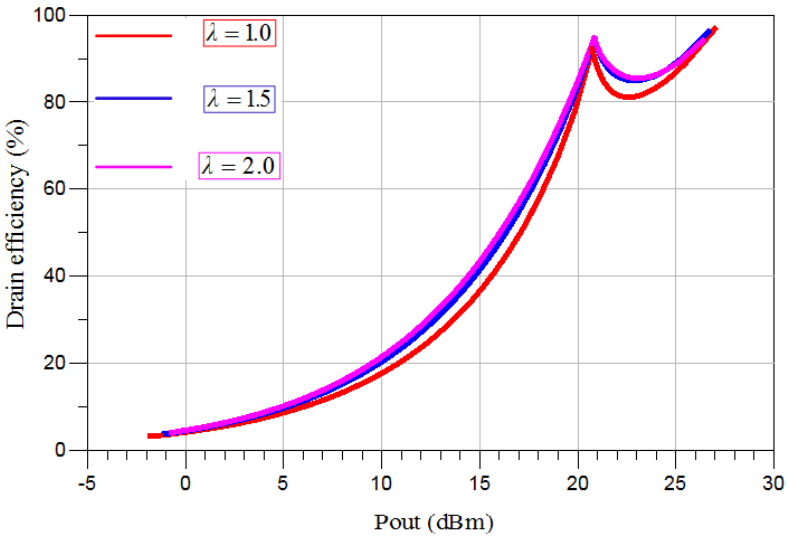
This chapter begins with the theory and performance analysis of a conventional Doherty PA. If the branch amplifier is biased at Class B, there are two efficiency peaks in the simulated DPA, both deliver 78.5% maximum efficiency. To further improve the efficiency performance of a Doherty PA, swith-mode Class E amplifiers with up to 100% theoretical drain efficiency are employed to implement the branch amplifiers instead of their linear counterparts. Since Class E PAs fail to relate the amplitude of input to output when turned on , they cannot be directly applied in systems which employ spectrally efficient amplitude modulation. But they can be used in a context of constant-envelope input signal (fixed amplitude with only varying frequency or phase) as the switched-mode power amplifiers exihibite linearity in phase. A direct digital polar modulation technique is therefore proposed. By turning on a discrete number of unit PA elements to control the effective on-resistance, amplitude modulation can be achieved. More details of the basic operation of the proposed Class E based digital polar Doherty PA can be found in subsection 3.2.3. Finally, the efficiency-output power characteristics are investigated with different design parameter q and different matching impedance. It can be observed from the simulation results that the efficiency performance of parallel circuit Class E and load-insensitive Class E is more tolerant of the change of output power, especially at the backoff region between the two peaks. In addition, it's better to design the branch amplifier according to the $\lambda = 1.5$, a comprise between full power level and back-off level.



(a) RF-choke Class E



(b) Load-insensitive Class E



(c) Parallel-Circuit Class E

Figure 3.19: Efficiency output power characteristics for digital Doherty PAs employing (a) RF-choke Class E, (b) Load-insensitive Class E (c) Parallel-circuit Class when $\lambda = 1.0, 1.5, 2.0$

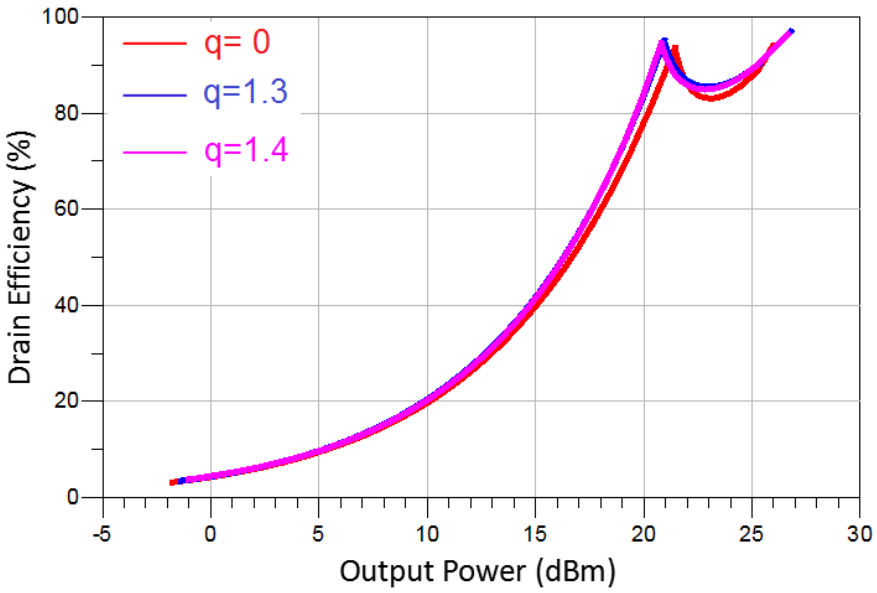


Figure 3.20: Efficiency output power characteristics for Class E based digital DPA with different design parameter q

4

TOWARDS EXTENDED OPERATION BANDWIDTH: A NOVEL POWER COMBINING NETWORK FOR DIFFENTIAL OPERATION

Doherty power amplifier is a cost-effective efficiency-enhancement technique that is widely used in cellular base station transmitters. However, practical implementations of DPAs only provide limited RF bandwidth, especially at high power level, which limits its applications in the wideband/multiband base stations. Therefore, techniques that can improve the efficiency bandwidth performance become another hot research interest for Doherty PAs. In this chapter, we intend to find a wideband solution for the proposed Class E based digital polar Doherty PA. For this reason, the frequency analysis of the conventional Doherty PA is firstly investigated and techniques that can improve the bandwidth of efficiency are discussed. In addition, the implementation of a broadband Class E is given in detail.

4.1. WIDEBAND ANALYSIS FOR CONVENTIONAL DOHERTY PAS

Conventional Doherty power amplifier is narrowband in nature due to the output capacitance of the active devices and the quarter wave transmission line (QWTL) impedance inverter [40, 41]. In this section, the factors that affect bandwidth behavior of the conventional DPA are discussed in detail with techniques that can overcome these restrictions.

4.1.1. DOHERTY PA BANDWIDTH FOR IDEAL DEVICES

The diagram of a symmetrical two-way Doherty Power Amplifier (DPA) in its basic form is shown in Fig 4.1, where the main and peak current sources are connected by a transmission

line (TL) impedance inverter which has an electrical length of $\lambda/4$ at the center frequency of the design. The output current from the peak device should be exactly in phase with the current flowing out from the impedance inverter. Thus, a phase lag of θ should be introduced in peak current to compensate the phase shift. θ can be expressed as $(\frac{f}{f_0}) \cdot \frac{\pi}{2}$ with f_0 the center frequency and f the operation frequency.

Optimum wideband operation of the DPA would require the TL to be a perfect impedance inverter over the whole desired frequency range. However, it is impossible without changing the physical properties of the TL, since the electrical length of the TL increases linearly with frequency. Hence the TL forming the inverter will imposes bandwidth restrictions to the DPA operation.

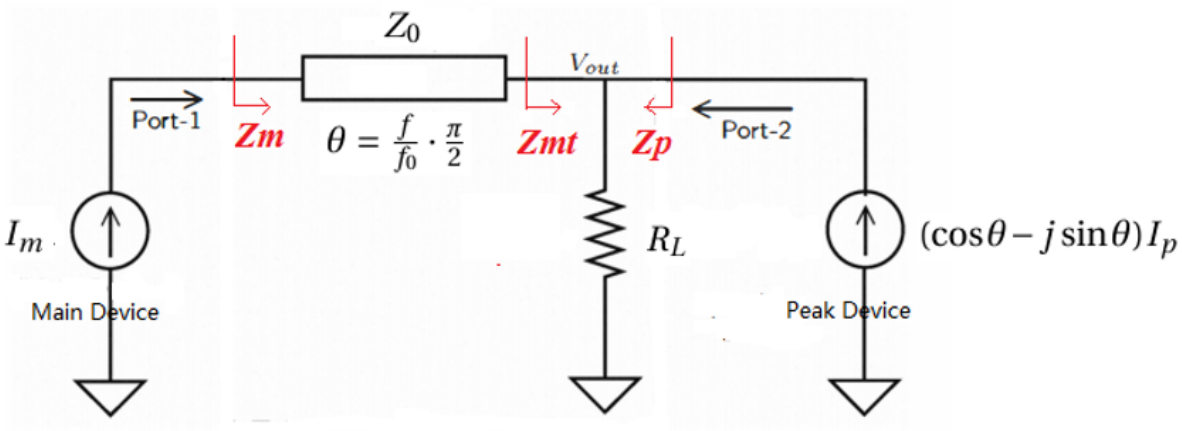


Figure 4.1: Basic schematic of a symmetrical two way DPA.

Figure 4.2 presents how efficiency changes at different frequencies with different input signal power levels for the ideal Doherty PA in Figure 4.1 on the condition that both main and peak PA are operated at Class B with all harmonics shorted. Obviously, the DPA efficiency bandwidth increases with the increse of input signal amplitude. When the input drive corresponds to the full voltage swing at the output, there is no bandwidth limitation at all and the DPA delivers 78.5% efficiency over the whole frequency range. In addition, the efficiency of the main amplifier is more frequency-sensitive than that of the peak amplifier. And the narrowest DPA efficiency bandwidth is found when the peak amplifier is off. Therefore more attention is paid to the bandwidth behaviour at power back-off.

An analysis of the load impedance at different input power levels is performed below.

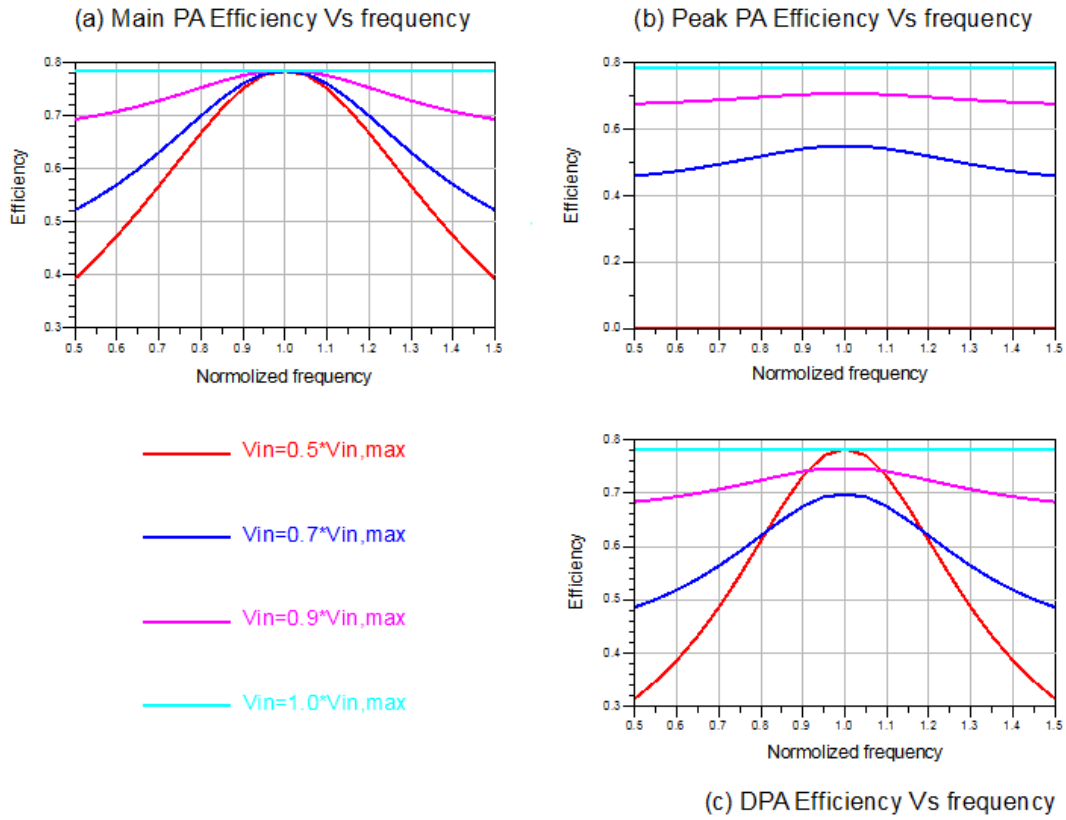


Figure 4.2: Efficiency bandwidth performance of a symmetrical Doherty PA based on Class B

The impedance seen by the main device and peak device can be expressed as

$$Z_m = Z_0 \frac{1 + I_p/I_m + j(Z_0/R_L - I_p/I_m)\tan\theta}{Z_0/R_L + j\tan\theta} \tag{4.1}$$

$$Z_p = Z_0 \frac{I_m}{I_p} \frac{1 + (I_p/I_m)\cos\theta(\cos\theta - j\sin\theta)}{(j\sin\theta + (Z_0/R_L)\cos\theta)(\cos\theta - j\sin\theta)} \tag{4.2}$$

Below the back off point, the peak device does not work, meaning that $I_p = 0$. Therefore,

$$Z_m = Z_0 \frac{R_L + jZ_0\tan\theta}{Z_0 + jR_L\tan\theta} \tag{4.3}$$

$$Z_p = \infty \tag{4.4}$$

The electrical length of the QWTL can be expressed in terms of center frequency as

$$\theta = \frac{2\pi}{\lambda}\frac{\lambda_0}{4} = \frac{\pi}{2}\frac{f}{f_0} \tag{4.5}$$

Then the impedance observed by the main power amplifier at 6dB back-off is

$$Z_m = \frac{Z_0^2}{R_L} \cdot \alpha \cdot \frac{\alpha + \alpha \tan^2(\frac{\pi}{2} \cdot \frac{f}{f_0}) - j(\alpha^2 - 1)\tan(\frac{\pi}{2} \cdot \frac{f}{f_0})}{1 + \alpha^2 \tan^2(\frac{\pi}{2} \cdot \frac{f}{f_0})} \cdot \tag{4.6}$$

with $\alpha = R_L/Z_0$. From Equation (4.6), it can be seen that the optimum load impedance Z_0^2/R_L could only be satisfied at center frequency. As the frequency changes, the real part of the fundamental impedance becomes smaller, degenerating the output power and lowering the efficiency.

Beyond the back off point, the peak amplifier starts to work. According to the Doherty operation analysis in Chapter 3, we have $I_p/I_m = (1-\alpha)/\alpha$. Thus the impedances seen by the main amplifier and the peak amplifier are given by

$$Z_m = Z_0 \tag{4.7}$$

$$Z_p = Z_0 \frac{\alpha}{1-\alpha} \tag{4.8}$$

Obviously, both the main and peak amplifiers at full power see a frequency-independent impedance.

If bandwidth is defined where the efficiency is within 10% of its maximum value, it is obvious that Doherty operation in its most elementary implementation allows an efficiency bandwidth of 28% at 6dB power back-off point, while having no bandwidth restrictions at 0dB power back-off (full power) from Figure 4.2. In view of this, a wideband impedance inverter should be applied if we want to improve the DPA bandwidth.

4.1.2. DOHERTY PA BANDWIDTH FOR REAL DEVICES

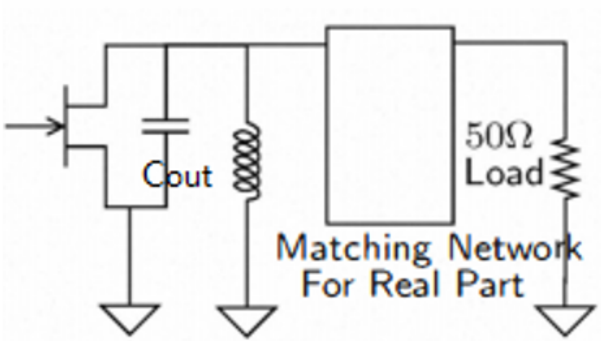


Figure 4.3: Matching topology typically applied in load modulated PAs [41].

In addition to the impedance inverter, the output capacitance of the active devices has

been proved to play a very decisive role in defining the maximum bandwidth of the DPA in [40] and [41]. The maximum bandwidth of DPA can be achieved if the PA devices are matched using wideband impedance matching techniques, which is traditionally realized by matching the output of the PA devices as a complex impedance. But From [41] and [6], it is better for DPA applications to match the PA devices as admittance because of load modulation. This is usually done by first tuning out the output capacitance by a parallel inductor, and then matching the real part of the output admittance (see Fig 4.3). However, the parallel LC network at the output of the PA device will have a band pass characteristic and therefore not only limits the bandwidth of the PA devices, but also the bandwidth of the total DPA. The efficiency degradation of the PA devices, when deviating from the center frequency of the design, can be represented as

$$\eta = cos(tan^{-1}(2\pi C_{out} R_{opt}(1 - f_n^2))) \tag{4.9}$$

where $f_n = \frac{f}{f_c}$ means the normolized frequency with respect to the center frequency (f_c) of the design and R_{opt} is the output load which is usually equal to the optimum load of the PA device for maximum performance. It can be concluded from equation (4.9) that the efficiency degradation depends on the output capacitance and optimum loading of the PA device which is characterized by a given technology. The efficiency-frequency characteristics of the DPA with devices NXP's LDMOS Gen 7 and Cree Inc. GaN are presented in Figure 4.4. Note that output capacitance of GaN from Cree is almost half the capacitance of the LDMOS devices for the same output power level. This reduced output capacitance results in a better starting point to achieve a large high-efficiency bandwidth.

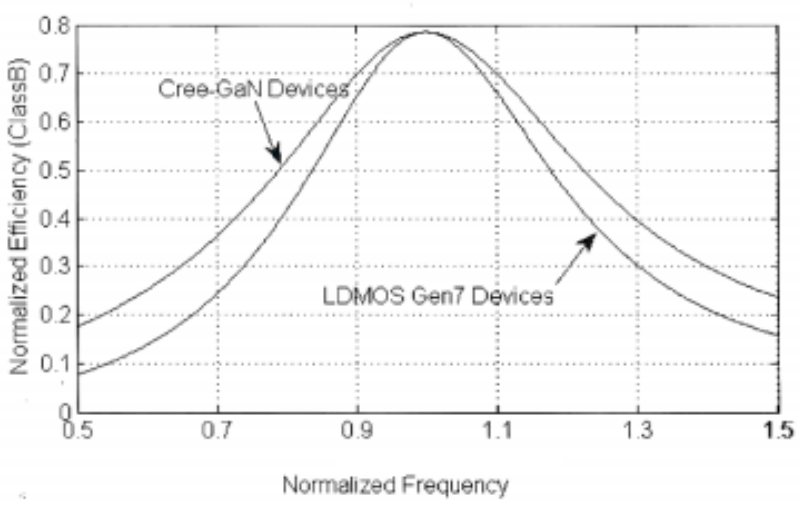


Figure 4.4: Efficiency vs. bandwidth of a symmetrical two-way DPA for different FET technologies [6]

4.1.3. COMPENSATION FOR OUTPUT CAPACITANCE

It can be concluded from the previous section that by compensating the output capacitances of the active device in a more wide-band manner, the overall bandwidth of the DPA can be significantly improved. An attractive technique to do this is to absorb the output capacitance along-with the connecting bond-wires in the TL forming the impedance inverter, consequently, the bandwidth is only limited by the behaviour of quasi lumped transmission line impedance inverter rather than the parallel LC resonator at the output of the devices [40].

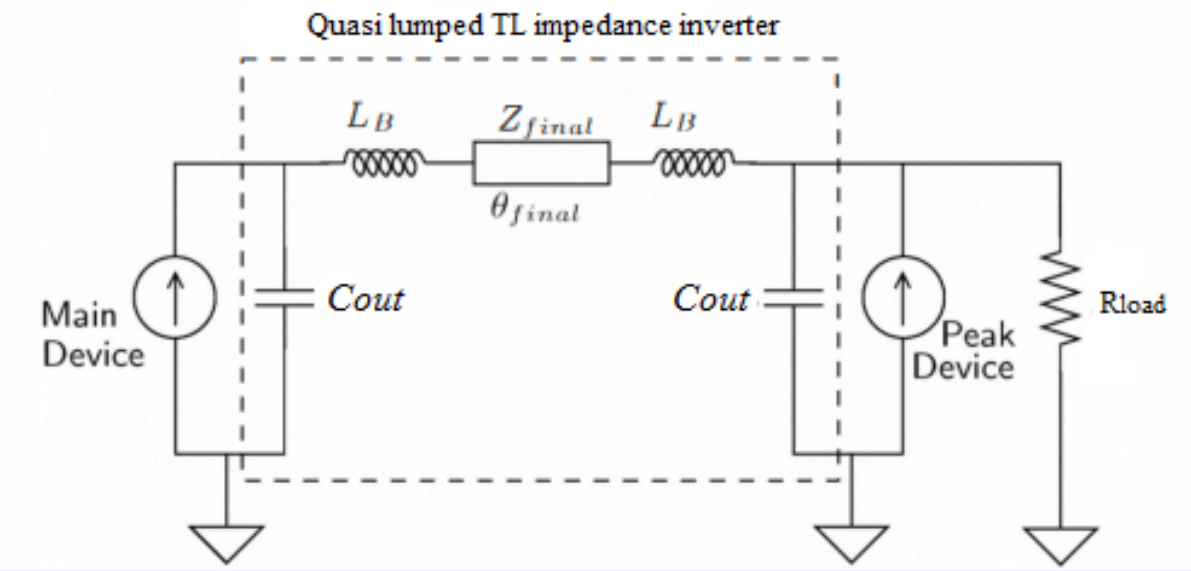


Figure 4.5: Simplified schematic of a DPA absorbing the device output capacitance and bond-wires into the quasi-lumped transmission line impedance inverter [6].

Figure 4.5 shows the simplified DPA schematic including the output capacitance and the connecting bondwires. Note that C_{out} along with the bond-wire L_B and TL form the new impedance inverter, called the quasi-lumped TL impedance inverter. If the length and characteristic impedance of the connecting transmission line in this quasi-lumped impedance inverter are adjusted in a proper way, it will act as an impedance inverter at the center frequency.

A quick analysis of this quasi-lumped transmission line is carried out below to evaluate the usability and limitation of this concept[6, 29, 41]. First, the bond-wire inductances are neglected for simplicity. Then the electrical length and characteristic impedance of the transmission line needed to absorb the output capacitance of the active devices in the quasi-lumped inverter can be calculated as

$$\theta_t = cos^{-1}(\omega C_{out} Z_0) \tag{4.10}$$

$$Z_t = \frac{Z_0}{sin(\theta_t)} \tag{4.11}$$

Where, Z_0 is the characteristic impedance of the original full $\lambda/4$ impedance inverter. Equation (4.10) also indicates the maximum output capacitance the quasi-lumped transmission line can absorb since θ_t should be smaller than 90 degree, which for a particular frequency ω is given by

$$C_{out} < \frac{1}{\omega Z_0} \tag{4.12}$$

Or we can see the frequency restriction:

$$\omega < \frac{1}{C_{out} Z_0} \tag{4.13}$$

Once the inductance of bond-wires are included, the electrical length and impedance in

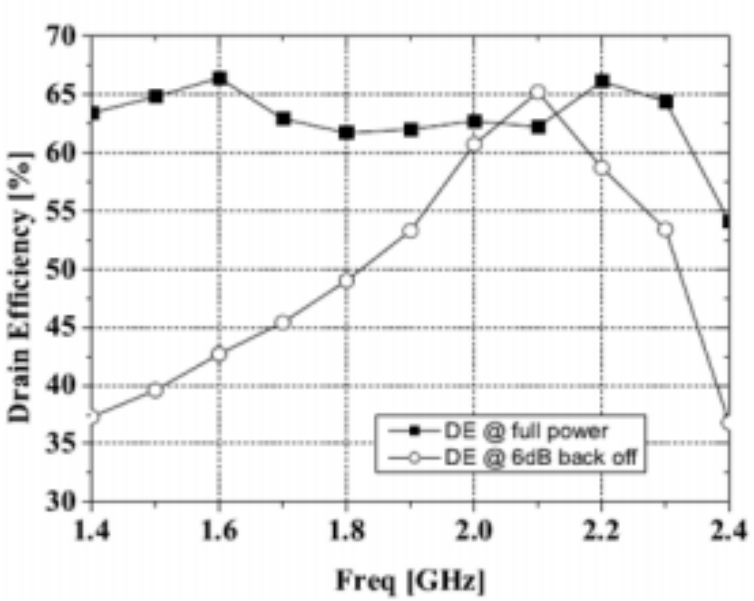


Figure 4.6: Drain efficiency of a 20W DPA with compensation of output capacitance [41].

the final realization turn out to be:

$$\theta_f = tan^{-1}(\frac{Z_t}{\omega L_B}) \tag{4.14}$$

$$Z_f = Z_t \frac{sin(\theta_t)}{sin(\theta_f)} \tag{4.15}$$

Improved efficiency bandwidth performance is given in Figure 4.6 [41]. As we can see, the efficiency is maintained high at full power while at the back-off region, there is no efficiency enhancement. If the efficiency at back off region can be improved at lower frequency band,

better DPA efficiency bandwidth characteristics can be obtained.

4.1.4. WIDEBAND IMPEDANCE INVERTERS

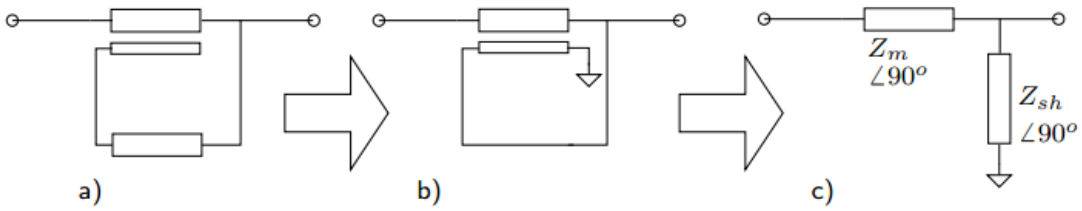


Figure 4.7: a) Wideband impedance inverter b) Wideband impedance inverter after removing the 90 degrees feedback line. c) Equivalent of the wideband impedance inverter by assuming that the coupling factor is zero [29].

It can be found in the previous subsection that although the bandwidth of the DPA at full power is significantly enhanced by absorbing the output capacitance of the devices together with the bondwire inductance into the quasi-lumped impedance inverter, the bandwidth at 6dB back-off power is not improved. This section shows that if a wideband impedance inverter is used, the bandwidth of the DPA at back-off region can be increased. Here are three candidates as we called: coupled-line impedance inverter, short-circuit $\lambda/4$ TL compensated impedance inverter and open-circuit $\lambda/2$ TL compensated impedance inverter, which can be used to more or less improve the DPA bandwidth.

Coupled lines can be applied as wideband impedance inverter from literature [42–44]. The coupled line impedance inverter, proposed by Jordon Sveshtarov [45], is based on a combination of a coupled line section (CLS) with a single transmission line (TL), as illustrated in Figure 4.7(a), where the electrical length of the coupled line and the feedback TL are both 90 degrees. This configuration has wideband impedance inversion properties that can be utilized to improve the bandwidth of the DPA [29]. A much simpler structure for wideband impedance inverter is derived from the coupled line structure by Xiaobo Deng [29] by assuming that the coupling coefficient for the coupled lines is 0 (see Figure 4.7). This is what we call short-circuit $\lambda/4$ compensated impedance inverter. Another creative idea to improve the wideband behaviour at back-off power is to add an additional $\lambda/2$ TL compensation line to the load end of the QWTL [46] as shown in the Fig 4.8 (d). Here we call it open-circuit $\lambda/2$ TL compensated impedance inverter. In order to verify it, the impedance transformation effect comparison between four different impedance inverters, namely the conventional QWTL, coupled-line impedance inverter, short-circuit $\lambda/4$ TL compensated impedance inverter and open-circuit $\lambda/2$ TL compensated impedance inverter can be per-

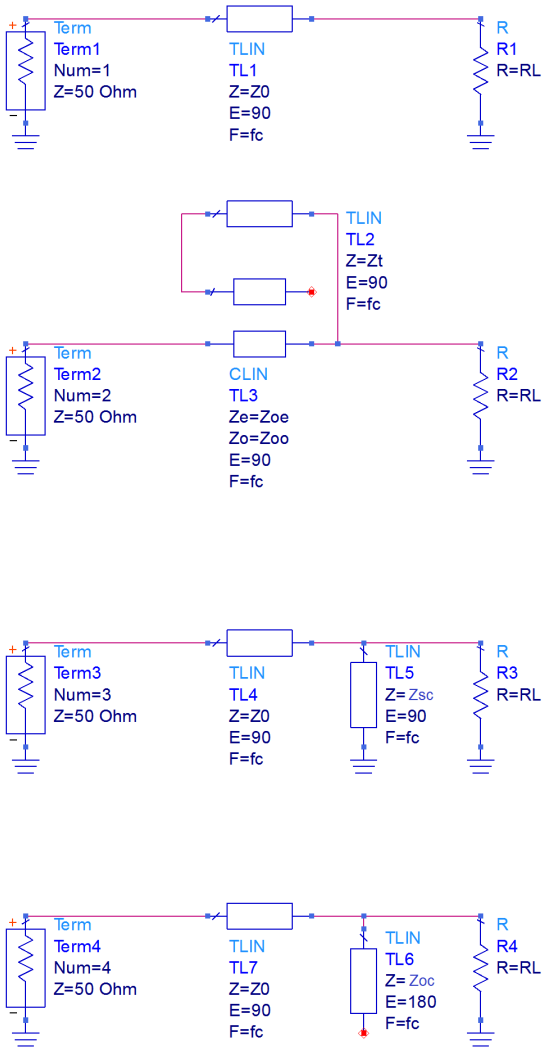


Figure 4.8: Impedance transformation effects comparison schematic of 4 different impedance inverters at power back-off level (Up to down: QWTL, coupled line, short-circuit $\lambda/4$ TL Compensated and open-circuit $\lambda/2$ TL Compensated impedance inverters)

Table 4.1: A set of impedance inverter parameters

QWTL Impedance inverter	Z_0	1 Ω
Coupled line Impedance inverter	Z_{0e}	1.78 Ω
	Z_{0o}	0.83 Ω
	Z_t	1.557 Ω
Short-circuit $\lambda/4$ TL Compensated Impedance Inverter	Z_0	1 Ω
	Z_{sc}	1 Ω
Open-circuit $\lambda/4$ TL Compensated Impedance Inverter	Z_0	1 Ω
	Z_{oc}	1 Ω

formed. The schematic is shown in Figure 4.8, where different load impedances (R_L) correspond to different power levels in the DPA. Since it is confirmed in the previous subsection that the narrowest DPA bandwidth is observed at 6dB back off for a symmetrical Doherty PA, the following analysis focuses on the impedance transformation bandwidth in this condition. Assuming the normalized optimum load R_{opt} for a device is 1Ω, for an ideal symmetrical Doherty PA, which means the back off ratio α is 0.5, the characteristic impedance Z_0 of the QWTL must be 1Ω and the load impedance R_L must be 0.5Ω to mimic the 6dB power back-off situation. Thus, the impedance seen by the main amplifier is $Z_0^2/R_L = 2\Omega$. More details about the component values in Figure 4.8 are listed in Table 4.1.

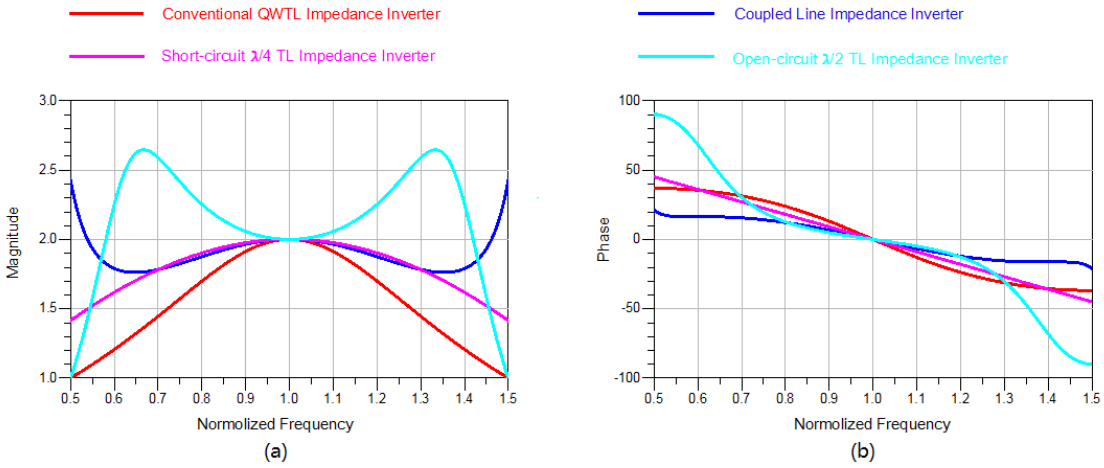


Figure 4.9: a) Magnitude b) phase of the normalized input impedance of different wideband impedance inverters Vs Frequency when $R_L = 0.5$

Figure 4.9 depicts the impedance seen by the main amplifier at back-off power level. It is apparent that all the four impedance inverters have the same responses at central frequency f_c. In addition, we can observe that the magnitude and phase variation of the three wideband impedance inverter is slower than that of the conventional QWTL, meaning an improved inversion bandwidth compared with the QWTL at power back-off. Morever, it can be note that except for the open-circuit $\lambda/2$ TL compensated impedance inverter, both the coupled-line impedance inverter and the short-circuit $\lambda/4$ TL compensated impedance inverter see an impedance decrease around the center frequency which is the same as the QWTL. If the transformation bandwidth is defined within 5% impedance variation (from 2.0Ω to 1.9Ω or from 2.0Ω to 2.1Ω), then for the QWTL, it is from $0.89f_c$ to $1.11f_c$, or a relative bandwidth of 22%. For the coupled line impedance inverters, the transformation bandwidth is from $0.82f_c$ to $1.18f_c$, or a relative bandwidth of 36%. For the short-circuited and open-circuit $\lambda/2$ TL compensated impedance inverter, it is from $0.80f_c$ to $1.20f_c$ and from $0.87f_c$ to $1.13f_c$, respectively. The relative bandwidth improves to 36% and 26%. Note

that the addition of the open-circuit $\lambda/2$ TL is different from the other three impedance inverters since it results in a wider load-modulation bandwidth along-with more ohmic loading conditions for the main PA in the frequency range from $0.80f_c$ to $1.20f_c$. At band edges the load-modulation factor even approaches a value which is a little larger than 2.5.

The simplified schematics for the symmetrical Doherty PAs employing these 4 different impedance inverters (see Figure 4.8) are plotted from Figure 4.10 to Figure 4.13, where the ideal device can be modeled as a current source, and the transfer characteristics described in Section 3.1 when $\alpha = 0.5$ are adopted here to ensure a symmetrical Doherty operation.

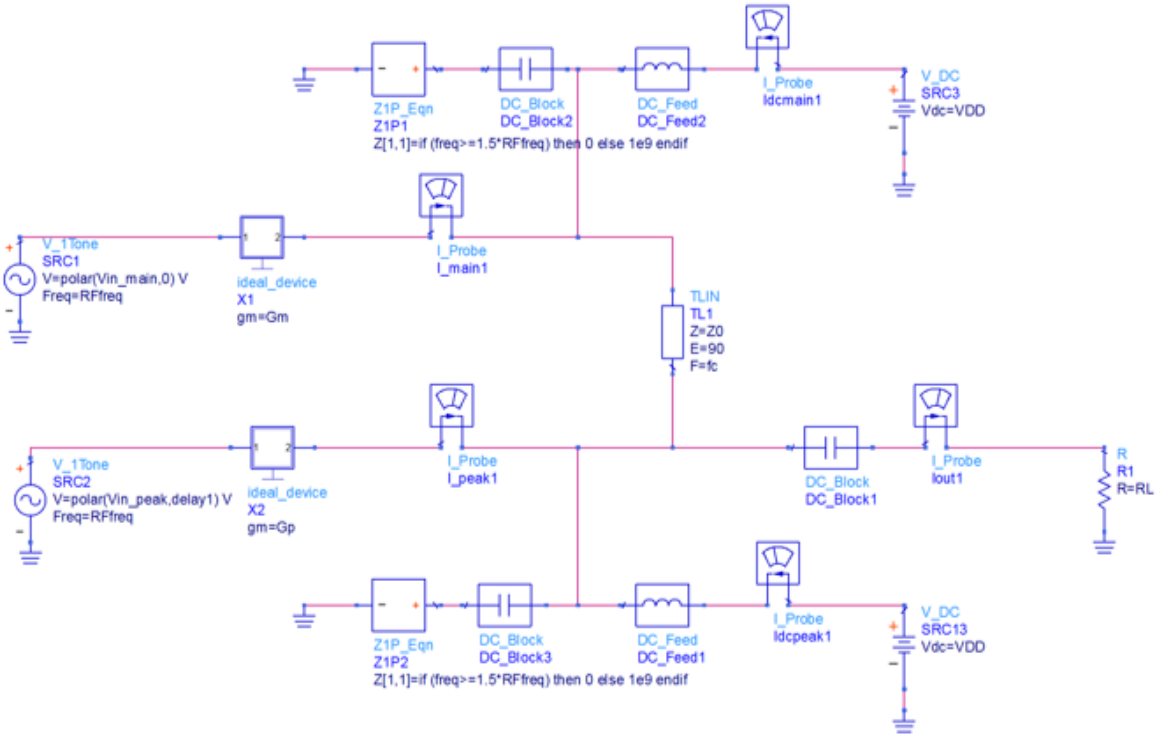


Figure 4.10: Simplified schematics for Symmetrical two-way Doherty PAs employing the conventional QWTL inverter (Case 1).

In addition, all higher harmonics are short circuited by the component $Z1P_Eqn$ to ensure a Class B operation for both the main and peak amplifiers. The phase of the main current source is fixed as 0 while the phase of the peak current source is set to $-90° \cdot f/f_c$ to make sure that the output current from the peak amplifier is exactly in phase with the current flowing out from the impedance inverter. Assuming that RL is set to be 0.5Ω and the characteristic impedance for the TL in the case of the conventional QWTL is set to 1Ω while the wideband impedance inverter parameters are chosen in such a way that it provides a wide-band input impedance of $Z_0^2/R_L = 2\Omega$ at full power.

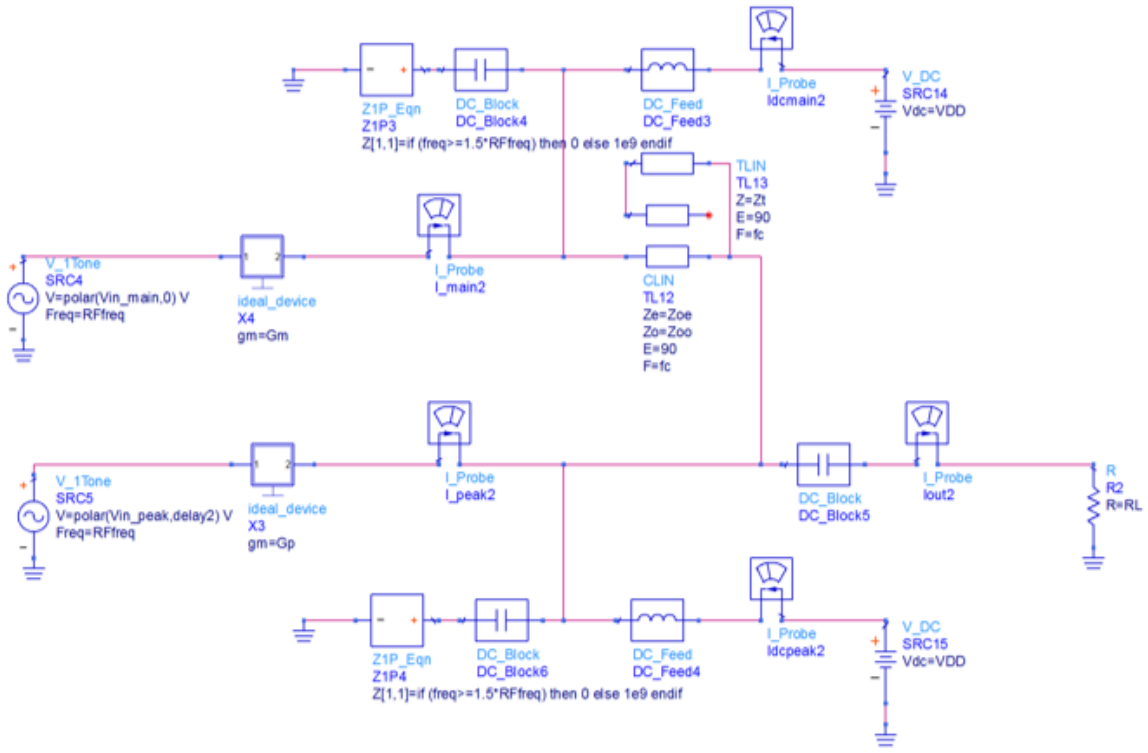


Figure 4.11: Simplified schematics for Symmetrical two-way Doherty PAs employing the coupled-line impedance inverter (Case 2).

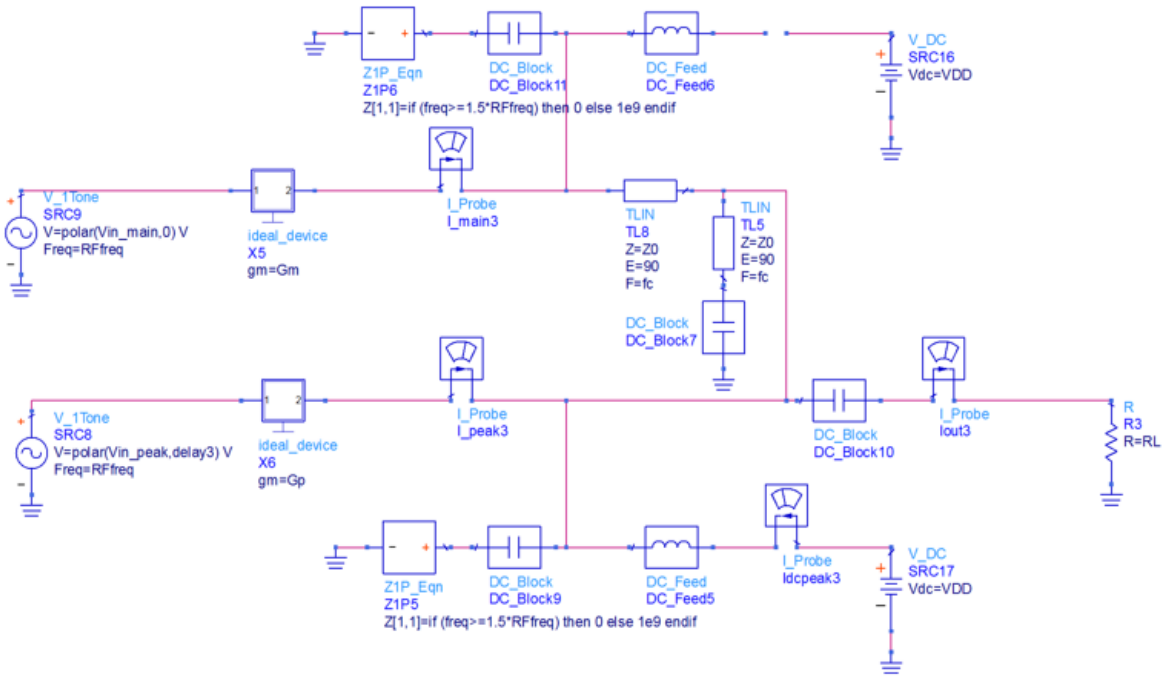


Figure 4.12: Simplified schematics for Symmetrical two-way Doherty PAs employing the short-circuit $\lambda/4$ TL Compensated impedance inverter (Case 3).

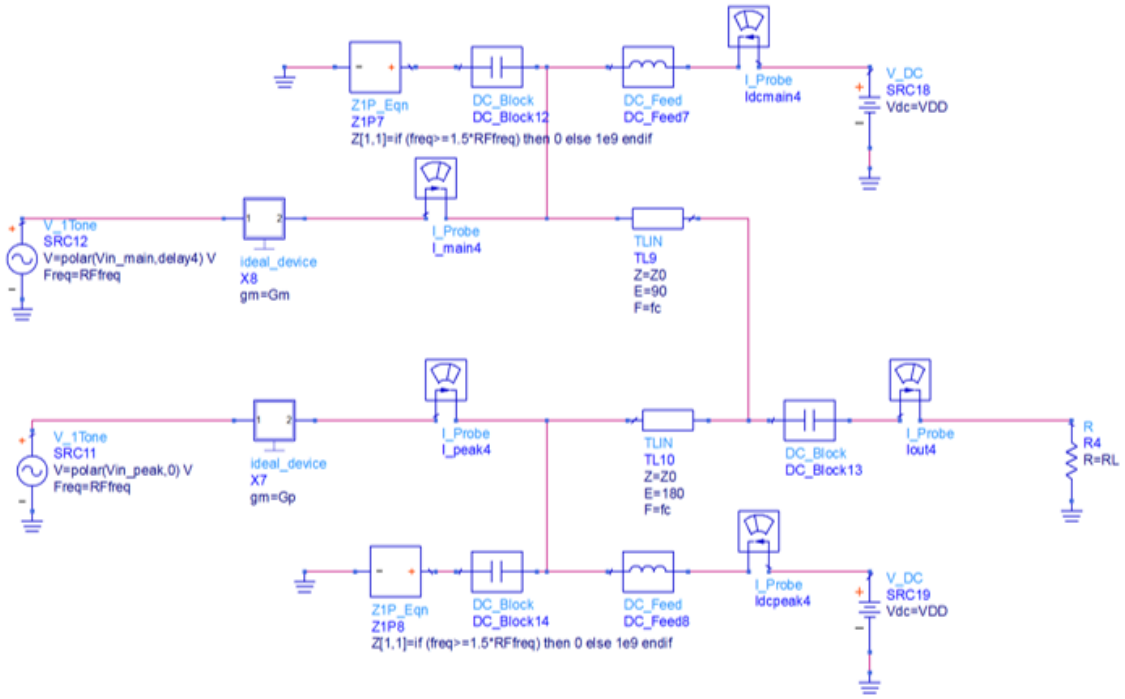


Figure 4.13: Simplified schematics for Symmetrical two-way Doherty PAs employing the open-circuit $\lambda/2$ TL Compensated impedance inverter (Case 4)

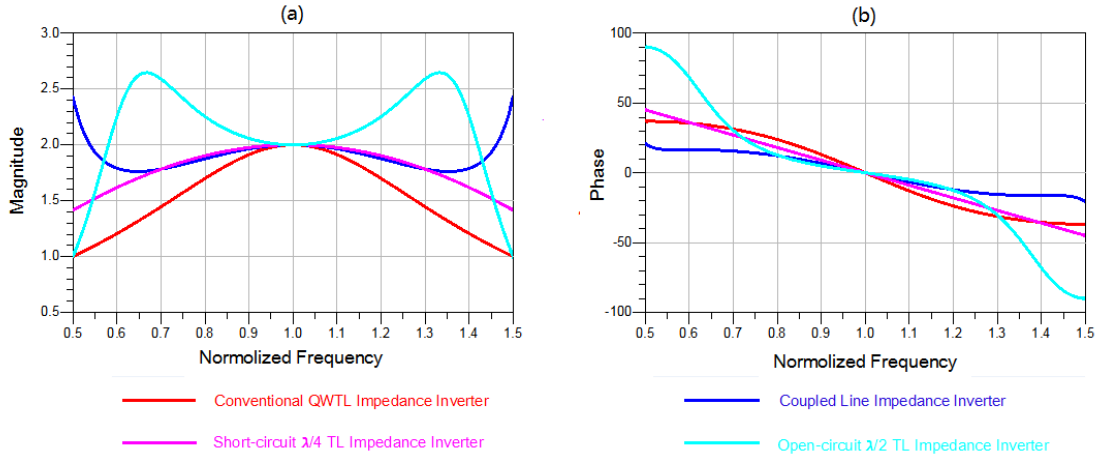


Figure 4.14: a) Magnitude b) phase of the impedance seen by the main PAs in the schematic shown in Figures from 4.10 to 4.13 at 6dB back-off ($V_{in} = 0.5 * V_{inmax}$)

First,we examine the impedance seen by main PA at two extreme case, namely the 6dB power back-off and full power (see Figure 4.14 and Figure 4.15). The simulation results shown in Figure 4.14 matches well with that in Figure 4.9, which further verifies the conclusion above. From Figure 4.15, it can be observed that the transformance bandwidth at full power for the open-circuit $\lambda/2$ TL compensated impedance inverter is a copy of that for the QWTL, while for the other two wideband inverters, it degrades. The impedance

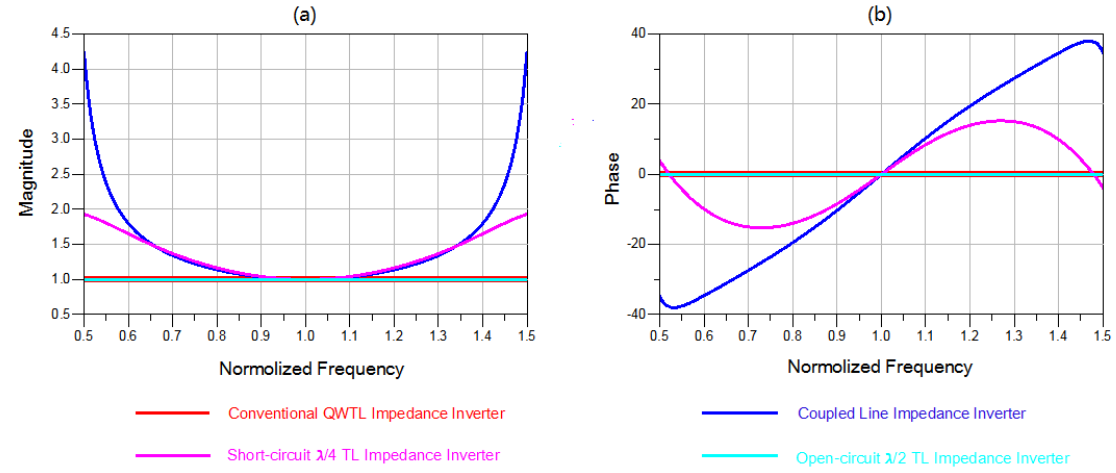


Figure 4.15: a) Magnitude b) phase of the impedance seen by the main PAs in the schematic shown in Figures from 4.10 to 4.13 at full power ($V_{in} = 1.0 * V_{inmax}$)

offered by the other two wideband impedance inverters is larger than the desired value when the frequency deviates from the central frequency. The transformation bandwidth at 5% impedance increase (from 1Ω to 1.05Ω) decreases to 22% and 18% for the coupled-line impedance inverter and the short-circuit $\lambda/4$ TL compensated impedance inverter, respectively. The performance is summarized in Table 4.2.

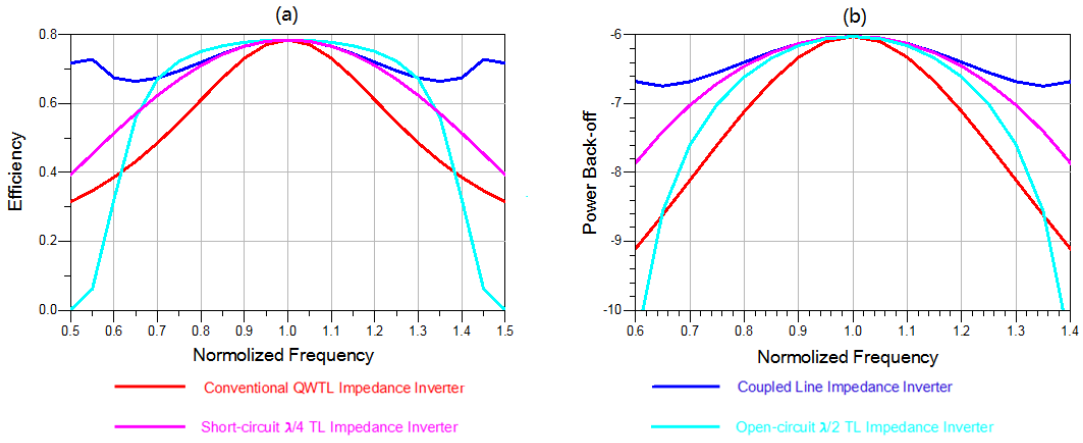


Figure 4.16: a) Efficiency b) Power back-off Vs Frequency for Doherty PAs as depicted in Figures from 4.10 to 4.13 at 6dB back-off ($V_{in} = 0.5 * V_{inmax}$)

The effciency and output power bandwidth analysis of Doherty PAs employing wideband impedance inverter is performed using ADS with the simplified schematics as depicted in Figure 4.10, 4.11, 4.12, 4.13. If the 10% efficiency drop bandwidth criterion is used again, the efficiency bandwidth of DPAs at 6dB back-off and at full power with different impedance inverters can be read from Figure 4.16 and 4.17 respectively. The performance

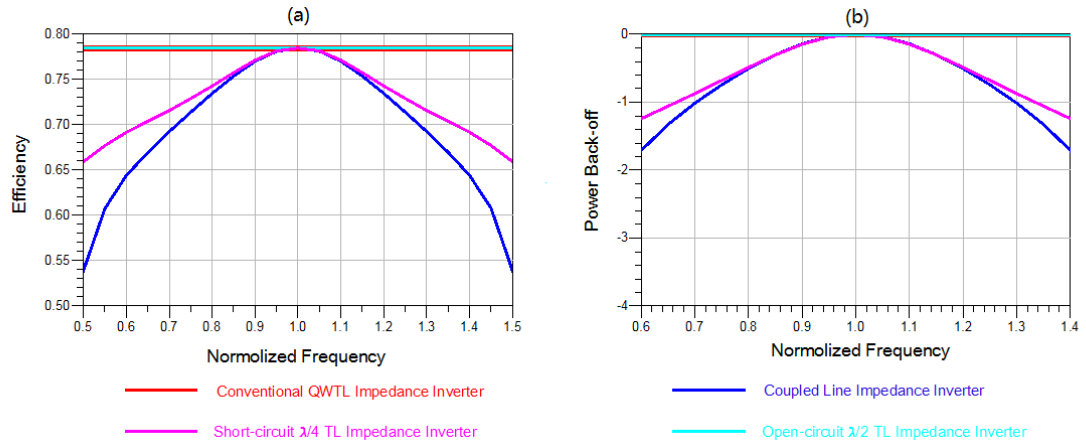


Figure 4.17: a) Efficiency b) Power back-off Vs Frequency for Doherty PAs as depicted in Figures from 4.10 to 4.13 at full power ($V_{in} = 1.0 * V_{inmax}$)

Table 4.2: Impedance transformation bandwidth seen by the main PA at 6dB back off ($V_{in} = 0.5 * V_{inmax}$) and full power level ($V_{in} = 1.0 * V_{inmax}$) (Note that the impedance phase bandwidth is defined as the phase difference when the frequency deviates +/- 0.2 with respect to the center frequency)

	Mag(Z_m)		Phase(Z_m)	
	@6dB back-off	@full power	@6dB back-off	@full power
Case 1	22%	100%	23.7°	0°
Case 2	36%	24%	12.2°	9.53°
Case 3	40%	22%	18.0°	14.1°
Case 4	26%	100%	12.7°	0°

is summarized in Table 4.3. First, the three wideband impedance inverters can obviously improve the efficiency bandwidth at 6dB back off within the frequency range from $0.7 f_c$ to $1.3 f_c$. When it comes to the wideband efficiency and output power behaviour at full power as depicted in Figure 4.17, first it can be observed that the same as the QWTL, there is no bandwidth limitation for the open-circuit $\lambda/2$ TL compensated impedance inverter. However, the efficiency and output power bandwidth deteriorate for the other two wideband impedance inverters when compared with the QWTL. This can be explained with the help of the impedance simulation results at full power as plotted in Figure 4.15. Obviously, the impedance seen by the main PA at the device end of open-circuit $\lambda/2$ TL compensated impedance inverter is the same as that for a QWTL, while for the coupled line and the short-circuit $\lambda/4$ TL compensated impedance inverters, the impedances are larger than that of the QWTL. At central frequency, the main amplifier drain voltage swing reaches its maximum when the drive voltage V_{in} equals V_{inmax}. When frequency deviates, the loading impedance is larger than the optimum impedance, the drain voltage will be clipped, leading to a limited current and output power. We can observe from the efficiency versus output power at $1.2 f_c$ (see Figure 4.18) that both coupled line and compensated impedance

inverters can improve the back off efficiency of DPA. However, their peak output power will decrease because of the non-optimum impedance value in this situation. Though the efficiency bandwidth is narrow for coupled line and the short-circuit $\lambda/4$ TL compensated impedance inverters compared with the QWTL at power back-off, still the overall DPA efficiency performance will be improved, since most of the time the DPA operates in the back off region.

Table 4.3: Efficiency and output power bandwidth of the Doherty PA employing different impedance inverters at 6dB back off ($V_{in} = 0.5 * V_{inmax}$) and full power level ($V_{in} = 1.0 * V_{inmax}$) (Note that the effiency bandwidth is defined as 10% efficiency drop while output power bandwidth is defined as 1dB power drop)

	Efficiency		Output Power	
	@6dB back-off	@full power	@6dB back-off	@full power
Case 1	26%	100%	38%	100%
Case 2	48%	56%	100%	60%
Case 3	42%	72%	60%	66%
Case 4	54%	100%	50%	100%

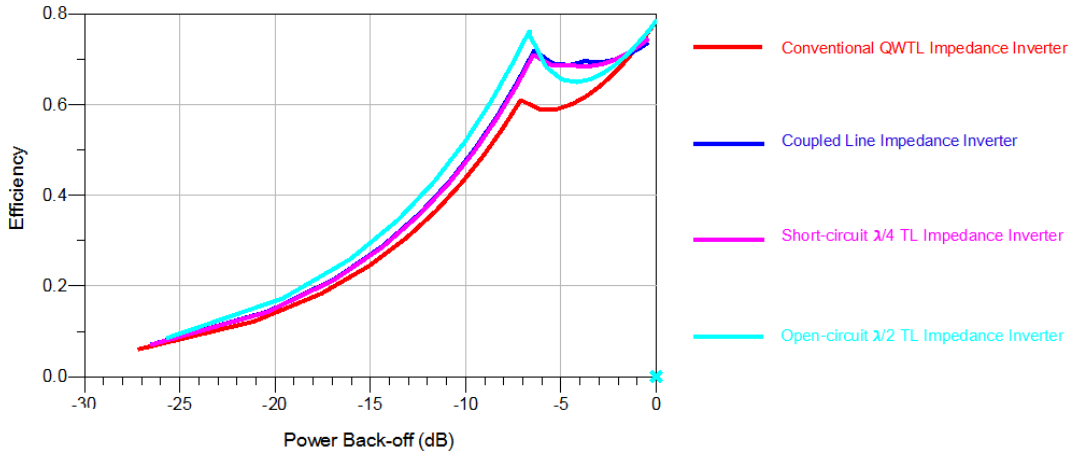


Figure 4.18: Eff Vs Output Power @ $1.2 f_c$

From the discussion we can conclude that the best choice for impedance inverter is the open-circuit $\lambda/2$ TL compensated impedance inverter because it boosts the efficiency at power back-off without sacrificing the performance at full power.

4.1.5. CONCLUSIONS

The bandwidth limitations of a symmetrical two-way Doherty amplifiers have been evaluated. For a Doherty PA with ideal devices and a QWTL inverter, the bandwidth varies with

input power level and is narrowest at back off with a relative bandwidth of 28% while having no bandwidth restrictions at full power. In addition to the impedance inverter, the narrowband behavior in practical DPAs is also caused by the output capacitances of the PA devices. A technique is presented to absorb the output capacitance of the PA devices along with the bondwire inductance in QWTL, forming a quasi-lumped impedance inverter. In this way, the bandwidth of the DPA is only limited by the quasi-lumped impedance inverter.

Three new impedance inverters are proposed, namely coupled-line impedance inverter, short-circuit $\lambda/4$ TL compensated impedance inverter and open-circuit $\lambda/2$ TL compensated impedance inverter, through which higher average efficiency over a significant frequency range could be obtained with a phase delay between main and peak PA proportional to the frequency to follow the phase change with frequency of the QWTL. But for the coupled line impedance inverter, short-circuit $\lambda/4$ TL compensated impedance inverter, the improvement is at the expense of the power capability and the bandwidth degradation at full power level. The open-circuit $\lambda/2$ TL compensated impedance inverter, however, has no bandwidth restriction at full power level if the impedance of the compensation line is chosen to be equal to the optimum loading impedance of the peaking device and proper input phase relations are enforced. In addition, The corresponding efficiency at power backoff indicates a fractional efficiency bandwidth of more than 60% compared with that for the conventional QWTL. Consequently, a wideband conventional Doherty PA can be expected using this open-circuit $\lambda/2$ compensation TL along-with the improved power combiner.

4.2. WIDEBAND CLASS E PA DESIGN

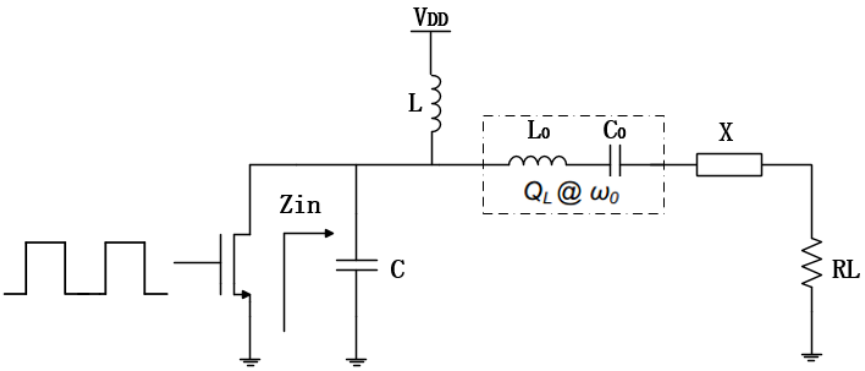


Figure 4.19: Basic schematic for Class-E Power Amplifiers

A general schematic for Class E power amplifier is plotted in Figure 4.19, where the load network consists of a parallel capacitance C, a parallel DC feed inductance L, a series fundamentally tuned circuit, a series reactance X which can be capacitive as well as inductive and a load resistance. In a common case, the shunt capacitor C can represent the intrinsic

device output capacitance and external circuit capacitance added by the load network.

When the DC feed inductance L is made infinite, the Class E is called RF-choke Class E. In this situation, both the shunt susceptance ($B = \omega \cdot C_{out}$) and the load reactance($Z_{E,load} = j\omega L_0 + 1/j\omega C_0 + jX$) will change when deviating from the design frequency, causing violation from the optimum loading condition. B is simply proportional to the frequency while $Z_{E,load}$ not only depends on the frequency, but also the quality factor Q_L of the LC tuned circuit. For bandwidth consideration, a lower value of Q_L is prefered since the efficiency bandwidth of RF-choke Class E is inversely proportional to the quality factor Q_L. However, for efficiency consideration, Class E power amplifier requires a high Q_L factor to selectively pass the fundamental frequency over the band of interest and suppress the harmonic components. This section we are trying to find out solutions that can overcome the bandwidth limitations of the traditional Class E.

4.2.1. PARALLEL-CIRCUIT CLASS E WITH REACTANCE-COMPENSATION TECHNIQUE

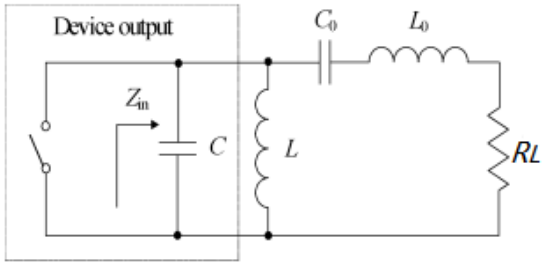
In this subsection, a parallel-circuit Class E RF power amplifier using reactance-compensation technique[47, 48] is proposed to relax the tradeoff between efficiency and bandwidth in Class E PAs.

THEORY OF REACTANCE COMPENSATION

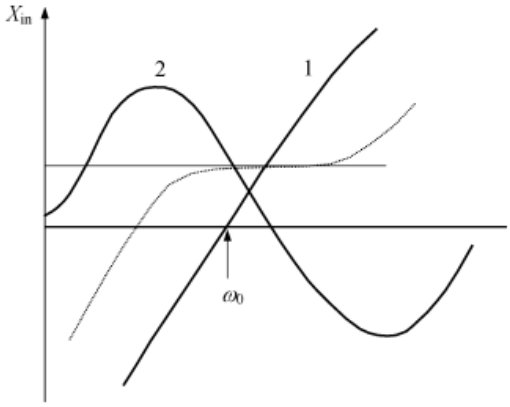
To explain the theory of the reactance compensation circuit technique, which is given in [49] for a load network with lumped parameters, a simplified equivalent load network is considered with a series resonant circuit tuned on the fundamental and a shunt circuit providing a constant load phase angle relative to the device output terminals, as shown in Figure 4.20(a). It can be observed from Figure 4.20(b), where $X_{in} = Im(Z_{in})$, the reactance of the series and shunt resonant circuits vary with frequencies, exhibiting an increase in the case of a series circuit (Curve 1) and a decrease in the case of a loaded parallel circuit (Curve 2) near the resonant frequency ω_0, which means that the slope of the series circuit is positive while the slope of the shunt circuit reactance is negative around central frequency. With a proper choice of the circuit elements, a constant load angle over a very large frequency bandwidth is established. This technique can be directly applied to a parallel circuit Class E power amplifier because its circuit configuration exactly matches with the reactance-compensation circuit, which is discussed in detail in the following subsection.

CONCEPTUAL ANALYSIS OF PARALLEL CIRCUIT WITH REACTANCE COMPENSATION

As discussed in Chapter 2, the design parameter q for an ideal parallel circuit Class E power amplifier equals 1.412 and the corresponding K set parameters is $K_L = 0.732$, $K_C = 0.685$, $K_P =$



(a) Schematic



(b) Principle ($X_{in} = Im(Z_{in})$)

Figure 4.20: Reactance Compensation

1.365, $K_X = 0$. Then the circuit elements shown in Figure 4.19 can be calculated as

$$R_L = \frac{V_{DD}^2 \cdot K_p(q)}{P_{out}} = 1.365\frac{V_{DD}^2}{P_{out}} \tag{4.16}$$

$$L = R_L\frac{K_L(q)}{\omega} = 0.732\frac{R_L}{\omega_0} \tag{4.17}$$

$$C = \frac{K_C(q)}{\omega \cdot R_L} = 0.685\frac{1}{\omega_0 R_L} \tag{4.18}$$

$$X = R_L\frac{K_X(q)}{\omega \cdot C} = 0 \tag{4.19}$$

With X=0, the resulting drain load impedance (see Figure 4.19) composed of shunt capacitance, dc-feed inductance and RLC tuned network, has the same structure with that shown in Figure 4.20. The admittance of load network ($Y_{in} = 1/Z_{in}$)as a function of frequency is given as

$$Y_{in}(\omega) = j\omega C + \frac{1}{j\omega L} + \frac{1}{R_L + j(\omega L_0 - 1/\omega_0 C_0)} \tag{4.20}$$

where $\omega_0 = 1/\sqrt{L_0 C_0}$. In order to provide a constant phase angle of the load network over the maximum frequency bandwidth, the parameters of the series resonant circuit $L_0 C_0$

must be chosen so as to satisfy the relation below.

$$\left.\frac{dB(\omega)}{d\omega}\right|_{\omega=\omega_0} = 0 \tag{4.21}$$

where $B(\omega) = Im(Y_{in}(\omega))$. Solving Equation (4.21), we can obtain

$$C + \frac{1}{\omega_0^2 L} = \frac{2}{\omega_0^2 C_0 R_L^2} = \frac{2L_0}{R_L^2} \tag{4.22}$$

As the final result, the series capacitance C_0 and inductance L_0 can be calculated from

$$L_0 = 1.026\frac{R_L}{\omega} \quad C_0 = \frac{1}{\omega_0^2 L_0} \tag{4.23}$$

Thus the quality factor Q_L @ ω_0 for the series tuned network is obtained.

$$Q_L = \frac{\omega_0 L_0}{R_L} = 1.026 \tag{4.24}$$

FREQUENCY ANALYSIS OF PARALLEL-CIRCUIT CLASS E WITH REACTANCE COMPENSATION

It has been proved theoretically in the previous subsection that the parallel Class E with reactance compensation can achieve a broadband operation. In this part, the performance of Class E power amplifier as a function of frequency is investigated with different load quality factor Q_L and different design parameter q to further verify this conclusion.

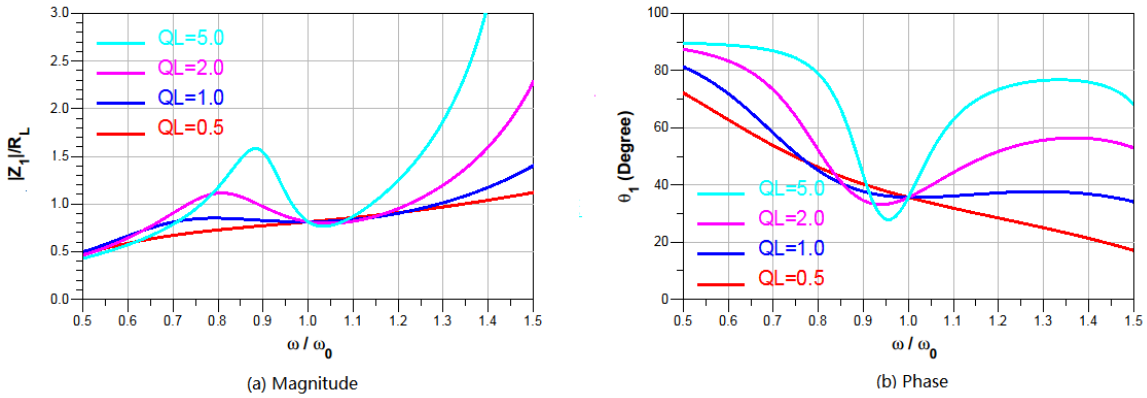


Figure 4.21: a) Magnitude and b) Phase of the normalized drain load impedance at fundamental as a function of frequency for different load quality factor Q_L

First the effects of loaded quality factor Q_0 is investigated with $q = 1.412$. One important reason for this choice ($q = 1.412$) is that it corresponds to the maximum output power according to [15]. The magnitudes and phase angles of the normalized drain load impedance at fundamental and second harmonic frequencies with varying load quality factor Q_L are

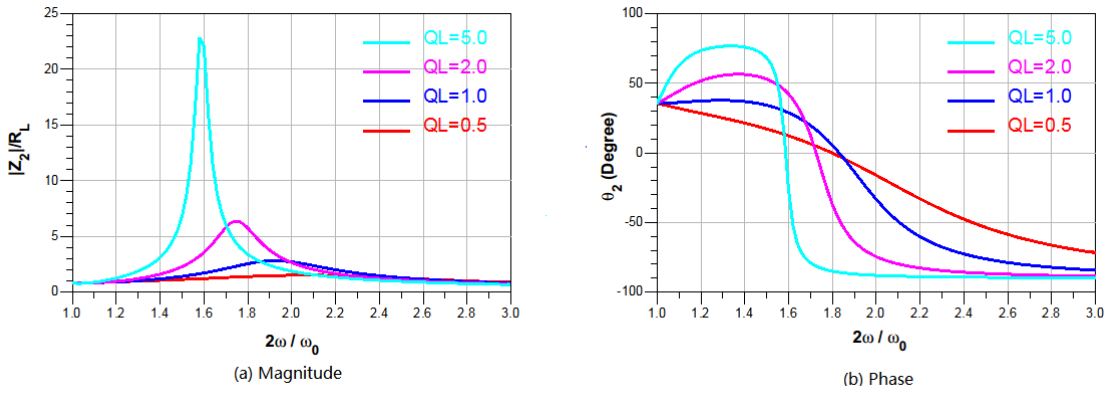


Figure 4.22: a) Magnitude and b) Phase of the normalized drain load impedance at second harmonic as a function of frequency for different load quality factor Q_L

plotted in Figure 4.21 and Figure 4.22 respectively. In addition, the variation of efficiency, K_P which corresponds to the output power as a function of frequency with different Q_L values is presented in Figure 4.23. It can be observed that the magnitude and phase angle of the drain load impedance is more tolerant of frequency variations for low Q_L values than for high Q_L values. The smallest magnitude and phase variations for fundamental components occur when $Q_L = 1$. We can see that with $Q_L = 1$, the magnitude and load phase angle is almost flat from $0.8\omega_0$ to $1.2\omega_0$, which is consistent with the results from Equation (4.15) and (4.24) in the previous subsection. However, for $Q_L = 1$ the load phase angle for second harmonic components deviates from the required value of $-90°$ and increases significantly as the frequency decreases, leading to the drain efficiency drop at low frequency. Contrary to the case of $Q_L = 1$, for $Q_L = 5$, the magnitude and phase exhibit the largest variations for fundamental components, which results in a sharp decrease of the output power between $0.8\omega_0$ and $1.2\omega_0$ and limited efficiency bandwidth. However, the load phase angle θ_2 is near $-90°$ from $0.85\omega_0$, which satisfies the required load phase angle at second harmonic frequency, giving high efficiency in band.

In conclusion, the bandwidth in terms of drain efficiency and output power is wider for low Q_L values than for high Q_L values. The large loaded quality factor Q_L can improve the peak drain efficiency, but reduce the usable bandwidth due to the significant variation of load phase angle in the band.

Next the effects of the design parameter q is examined with $Q_L = 1$. Since the DC feed inductance is a function of q, the variations of q can then be modeled by scaling the DC feed inductance. The magnitudes and phase angles of the normalized drain load impedance at fundamental and second harmonic frequencies with varying q are plotted in Figure 4.24 and Figure 4.25 respectively. And the variation of drain efficiency, output power represented by K_P as a function of frequency with varying q is presented in Figure 4.26. Note

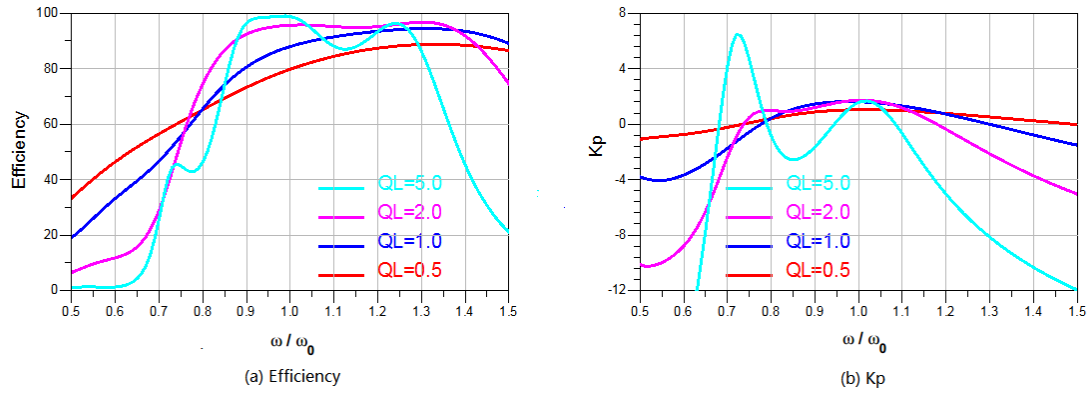


Figure 4.23: Effects of finite load quality factor Q_L on the wideband operation a) Drain Efficiency and b) K_P

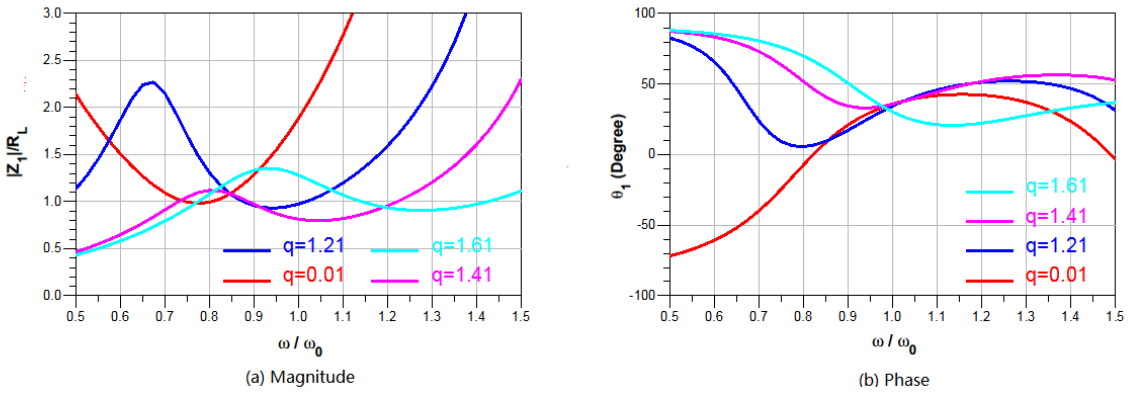


Figure 4.24: a) Magnitude and b) Phase of the normalized impedance at fundamental component as a function of frequency for different q

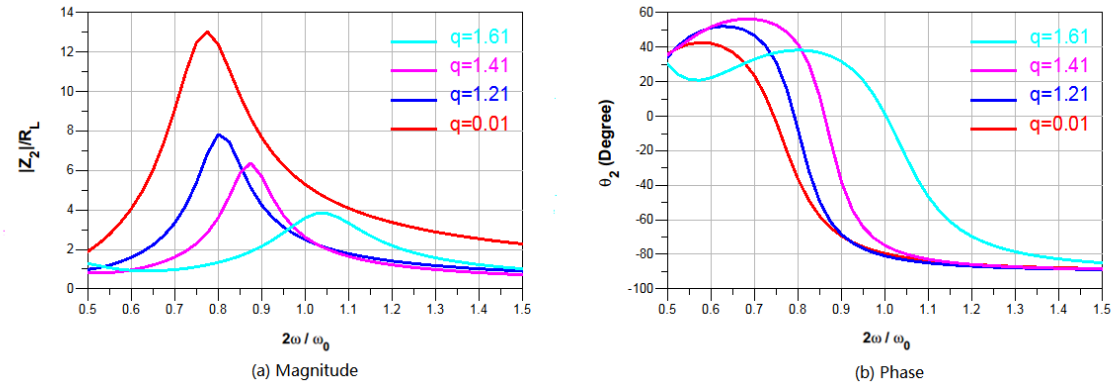


Figure 4.25: a) Magnitude and b) Phase of the normalized impedance at second harnonic as a function of frequency for different q

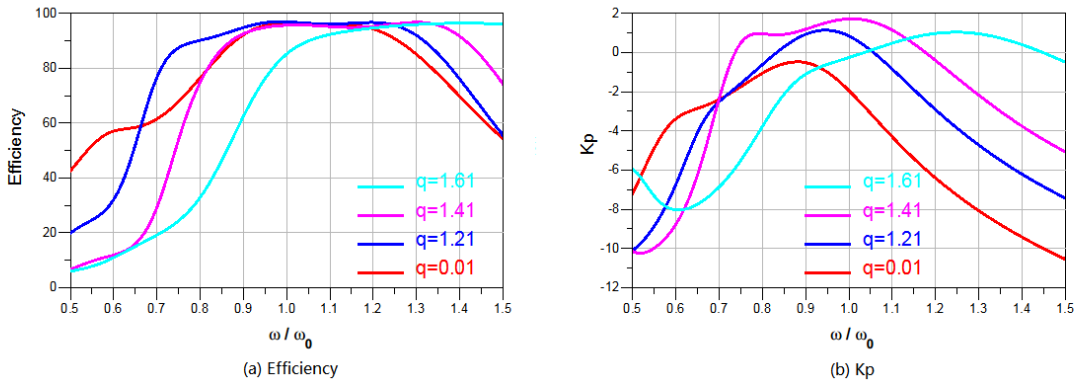


Figure 4.26: Effects of finite DC feed inductance on the wideband operation a) Drain Efficiency and b) K_P

that $q = 0.01$ here corresponds to the RF-choke Class E power amplifier where the DC feed inductance is infinite while the other three values for q correspond to Class E power amplifier with finite DC feed inductance.

It is apparent from Figure 4.24 that as q increases, the center frequency moves to higher frequency and the variations of magnitude and phase angle of finite dc-feed inductance (q=1.61) is smaller than that of infinite dc-feed inductance (q=0.01), therefore the bandwidth in terms of drain efficiency and output power is enhanced. As can be seen from Figure 4.26, if the efficiency bandwidth is defined within 20% drop, the bandwidth is 42.9% for $q = 0.01$ while it is 56.1% for $q = 1.41$. Thus the bandwidth is improved by 30.7% via finite dc-feed inductance. In addition, the bandwidth of 1dB output power flatness is 29.2% for $q = 0.01$ while it is 39.2% for $q = 1.41$. Meanwhile, K_P for $q = 1.41$ is over 3dB larger than that for infinite dc-feed inductance.

From the above results, one can conclude that parallel circuit Class E power amplifier with reactance compensation is a good option which can provide the bandwidth of 40% or more.

4.2.2. SINGLE-ENDED VERSUS DIFFERENTIAL

Compared with a single-ended design, the differential design has many advantages. First, this topology features a virtual ground, which makes it robust against parasitic inductance from the bondwires and leads to a good cancellation of the even harmonics. Furthermore, the push-pull combination scheme has a 4:1 load-line impedance benefit in an equal power comparison to a simple single-ended or parallel device connection. Therefore, a lower load impedance transformation ratio can be used for the matching network, which

leads to lower output currents and lower losses in the matching network.

From the previous discussion, we can figure out that the load quality factor is of great significance to the broadband characteristics of Class E PAs. Generally, lower Q_L values can provide a wider bandwidth in terms of drain efficiency and output power, but at the expense of reduced achievable peak drain efficiency due to the dramatical variation of the load phase from the required value of $-90°$ at second harnonic. This section shows that if a differential topology is used instead of the previous single-ended one, we can obtain the required load phase for second harmonic components over a large frequency range without changing the impedance characteristics for fundamental components, thus further improving the efficiency and output bandwidth for Class E power amplifiers.

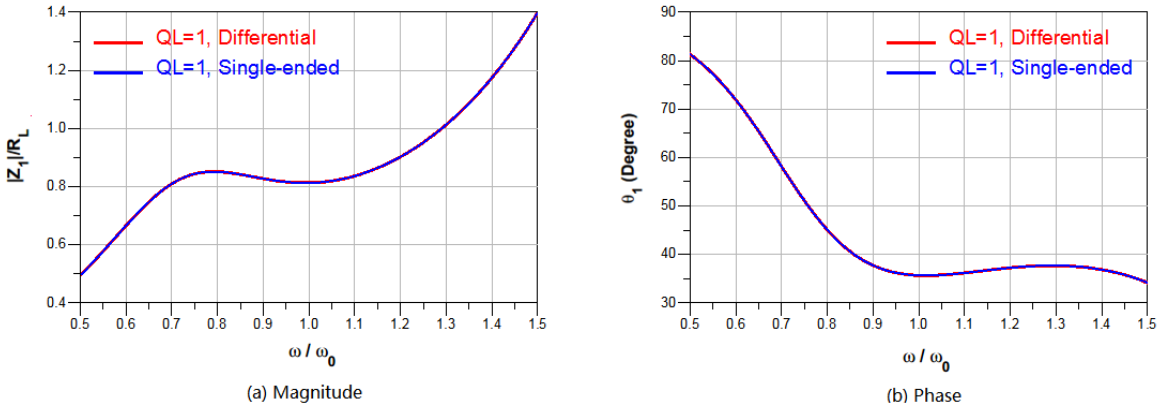


Figure 4.27: Comparisons of a) Magnitude and b) Phase of the normalized drain load impedance at fundamental as a function of frequency between a differential and single-ended Class E amplifier

In order to investigate this opportunity, a comparison between the single-ended and the corresponding differential Class E amplifier is given in terms of drain load impedance, efficiency and output power. The load quality factor Q_L is set to 1 for smallest impedance variations at fundamental. Figure 4.27 and Figure 4.28 present the drain load impedance as a function of frequency for fundamental components and second harmonic components respectively. As is shown in Figure 4.27, the curve for the differential case overlaps with the curve for the single-ended case, meaning that differential operation does not change the load impedance characteristics at fundamental. Then consider the second harmonic impedance characteristics in Figure 4.28, it can be observed that for the single-ended case, the load phase angle θ_2 from $0.73\omega_0$ to $1.5\omega_0$ deviates from the required value of $-90°$ and the phase increases as the frequency decrease while for the differential case the phase angle maintains $-90°$ from $0.73\omega_0$ to $1.5\omega_0$ with significantly improved magnitude at low fre-

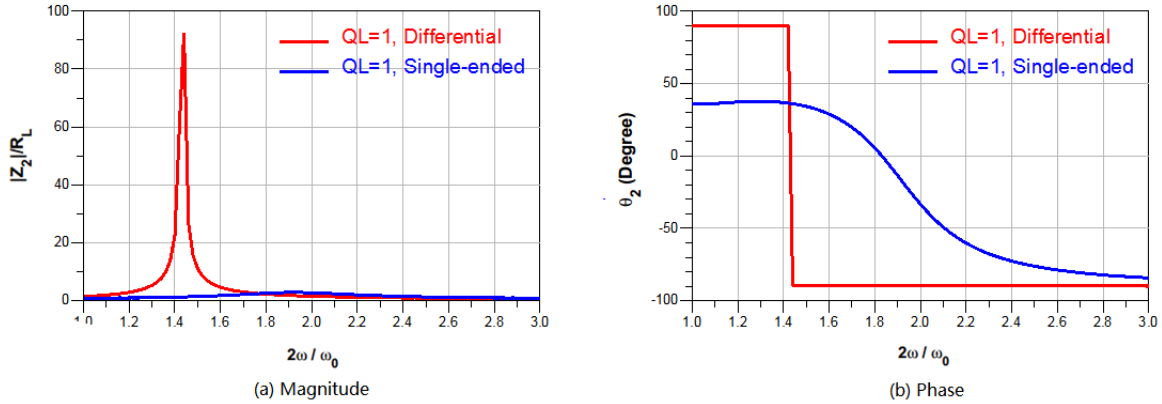


Figure 4.28: Comparisons of a) Magnitude and b) Phase of the normalized drain load impedance at second harmonic as a function of frequency between a differential and single-ended Class E amplifier

quencies.

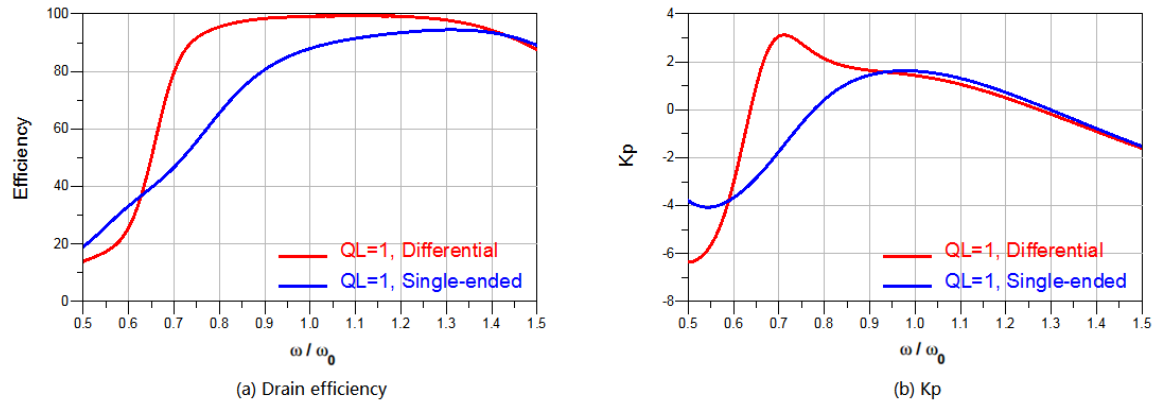


Figure 4.29: Effects of differential topology on the wideband operation of a parallel circuit Class E compared to the single-ended one a) Drain efficiency and b) K_P

From the discussion in the previous subsection, we find the phase deviation from $-90°$ will result in low peak efficiency in band, which limits the design of simultaneous high efficiency and broadband Class E with low load quality factor Q_L. With enhanced impedance characteristics at second harmonic frequencies, the differential operation can overcome this issue. This assumption is proved with the results in Figure 4.29, where the wideband performance comparisons between the single-ended parallel circuit Class E and the corresponding differential Class E in terms of drain efficiency and K_P are given. First, it can be found that the differential Class E amplifier provides a wider efficiency bandwidth and a higher in-band peak efficiency compared with the single-ended Class E. In addition, we can observe that there is little change in output power at high frequencies between the single-ended case and the differential case. At lower frequencies, the output power drops

more sharply for the differential case because of its dramatic phase variations (from −90° to 90°) as frequency decreases. Morever, the peak output power for the differential case is larger due to the significant improved magnitude peak for second harmonic frequencies. In addition to the suppression of even harmonics, there are several benefits of differential topology as mentioned in the beginning of this subsection: the differential output power is twice the single ended output power, insensitivity to ground inductance and low substrate current losses.

4.2.3. CONCLUSIONS

Both the load quality factor Q_L and the design parameter q are of great significance for the broadband charateristics of a Class E amplifier. In general, the finite dc-feed inductance (large q) can provide improved bandwidth in terms of drain efficiency and output power compared with the infinite dc-feed inductance (small q). In addition, a smaller Q_L value can significantly improve the efficiency and output power bandwidth, but reduce the peak efficiency in band because the load phase angle θ_2 for a small Q_L value will deviate dramatically from the required value of −90°, especially at lower frequencies. With a differential operation to supress the even harmonics, the non-ideal second harmonic impedance characteristics can be greatly enhanced, consequently improving the drain efficiency. Thus a high efficiency broadband can be realized using differential parallel-circuit Class E with reactance compensation.

4.3. CONCLUSIONS

Obviously, the broadband characteristics of the branch Class E amplifier, and the power combining network (mainly the impedance inverter) are the two main factors limiting the the bandwidth of the proposed Doherty PAs. Thus, for a wide band design, there are two issues to be solved. First, the branch amplifier is required to be wideband. This issue can be solved by using differential parallel-circuit Class E amplifier with a low load quality factor for the LC bandpass filter, which has the potential to realize high efficiency and large bandwidth simultaneously. The other is to achieve an optimum fundamental load modulation over a wide bandwidth and therefore a wideband impedance inverter is in need. For this reason, the so-called open-circuit $\lambda/2$ TL compensated impedance inverter is given and this topology has been confirmed to be able to provide a wideband load modulation. Details of the design will be discussed in Chapter 7.

5

WIDEBAND BALUN DESIGN CASE 1: BONDWIRE BASED

A balun is a type of transformer used to convert a balanced impedance (differential signal) to an unbalanced impedance (single-ended signal) and vice versa. Hence, baluns are essential components in realizing balanced mixers, push-pull amplifiers, and antenna feeding networks. Generally, the balun is either based on magnetic coupling or transmission line coupling. In this chapter, we focus on the magnetic coupling balun.

Conventionally, a magnetic transformer is implemented as a planer monolithic component, but due to the low quality factor it is limited for high-power applications. To overcome the drawback of monolithic transformers, a novel transformer structure ultilising the characteristics of bondwires is proposed. Bondwires are typically thought of as lumped electrical parasitic elements (normally inductive) which will deteriorate circuit performance in many semiconductor devices. However, in RF power transistors, bondwires are a very attractive alternative for the implementation of high-quality magnetic components such as inductors and transformers. Compared with conventional silicon monolithic implementation, they have many advantages such as lower resistance and almost no substrate losses, as well as lower parasitic capacitances (and hence higher resonance frequencies).

This chapter starts with a review of bondwire characteristics. Based on this background information, a study focusing on the design and modeling of bondwire-based transformers is carried out. Here, a novel parallel-to-series connection bondwire-based transformer is presented, which differs from the conventional series (multi-turn) and parallel connection of inductive bondwire loops that has been described in previous works. The last part

presents the design and simulation results of baluns which are implemented by simply combining two bondwire-based transformers.

5.1. BONDWIRES CHARACTERISTICS

Wire bonding is a highly mature, cost-efficient interconnect technique, intended to create electrical interconnections between integrated circuits and their packages. This technique makes use of thin metal wires, typically made of aluminum or gold with diameters ranging from 25μm to 250μm to provide mechanical and electrical attachment to bonding pads on chips and in packages using a wire-bonding tool which is automated for mass production or for accurate prototyping. The two main wire-bonding process technologies are ultrasonic wedge-wedge (normally used for aluminum wires connecting to aluminum or gold pads) and thermosonic ball-stitch (normally used for gold wires to different pad materials) bonding.

A bondwire exhibits self inductance along with mutual inductance to neighbouring conductors. Here analytical formulas for self- and mutual inductance of wires along with the current handling capacibility are given to provide design guidelines of bondwire-based transformers in the next section.

5.1.1. INDUCTANCE FOR ROUND-WIRE CONDUCTORS

There are numerous approximate formulas and methods in literature available for the calculation of the self and mutual inductance of a closed loop through the application of the Biot–Savart law or Neumann's equation [50, 51]. Since bondwires form non-closed loops, the concept of partial inductance was introduced. This means that complex shaped loops can be segmented into smaller linear pieces such that its total inductance is the algebraic sum of the individual partial inductances of those pieces.

The inductive characteristics of a bondwire are determined by several geometric parameters, including the shape of the wires, number of wires, spacing between wires, and wire radius. For simplicity, the idealized case of a couple of identical parallel round-wire conductors as illustrated in Figure 5.1 is considered to provide a basic understanding of the main parameters influencing inductance in bondwires. As shown in Figure 5.1, the conductor radius is r_w, the center-to-center conductor distance is d, and the conductor height above a large return ground plane is h. According to [16, 52, 53], the self-inductance and mutual-inductance per-unit-length of each of the two wires in the figure (assumed infinitely long) at high frequencies are given independent of their interconnection (i.e. independent on the relative current direction between both wires):

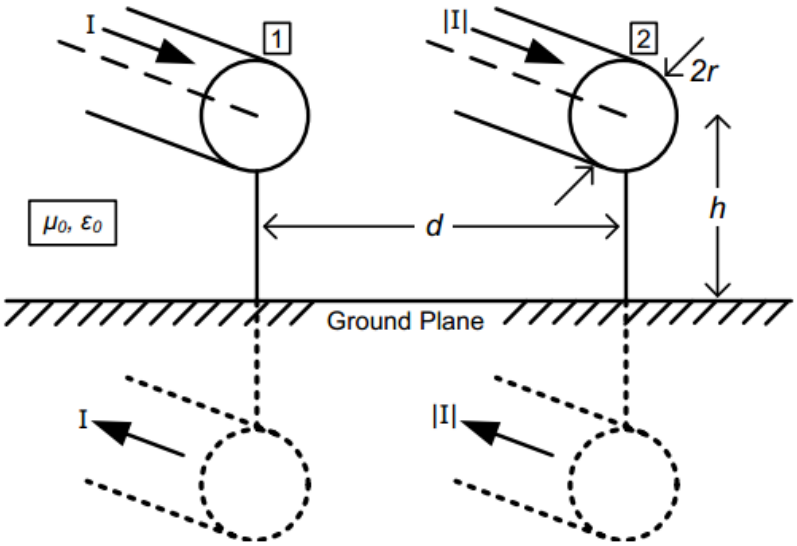


Figure 5.1: Diagram illustrating the currents and geometries of two straight and round-wire coupled conductors.

$$L'_{11} = L'_{22} = \frac{\mu_0}{2\pi}\cosh^{-1}(\frac{h}{r_w}) = \frac{\mu_0}{2\pi}\ln(\frac{h}{r_w}) \tag{5.1}$$

$$M'_{12} = \frac{\mu_0}{2\pi}\ln(1+(\frac{h}{r_w})^2) \tag{5.2}$$

If the currents in the conductors shown in Figure 5.1 are equal and in the same direction, the total inductance is given by the parallel of the individual equivalent inductances according to

$$L'_{eq} = \frac{L'_{11} + M'_{12}}{2} \tag{5.3}$$

And if more conductors are joined in parallel, there will be a mutual-inductance between every pair, making the total inductance equation more complex by including the expanded mutual-inductance terms (which are not equal due to the different distances) divided by the number of wires.

The above three simple expressions for the case of parallel conductors show general trends of the inductance of (sets or arrays of) bondwires. It is easy to find out from Equation (5.1) and (5.2) that a smaller wire radius will contribute to a larger self-inductance and mutual-inductance of the bondwires. For a given wire radius, the same result can be accomplished by raising the area of the loop via the length of the wire and its height from the ground plane. In addition, we can observe from Equation (5.2) that the mutual inductance is reversely proportional to the spacing distance between adjacent bondwires. Another way

to increase the mutual inductance is to include more bondwires in parallel. Equation (5.3), however, indicates that the equivalent inductance of several bondwires in parallel do not scale linearly with their number due to their magnetic coupling. Note that the derivation of Equation (5.1) and (5.2) is based on the assumption of uniform current distribution along the peripheries of the wires. This assumption restricts the accuracy of those expressions when the separation of the wires between ground or between them is not large compared to the radius.

Obviously, the inductance expressions in Equation (5.1) and (5.2) lack the ability to precisely define the three-dimensional nature of the bondwires because of the concepts such as the average height of the bondwire arc above the ground plane for complex loop shapes. In addition, these equations suffer from severe limitations when analyzing high frequency circuits where the distributed nature of the bondwire, radiation and non-uniform current densities due to proximity effects become important or cannot be neglected. Consequently, it is necessary to depend on more accurate full-wave 3D electromagnetic simulation tools to account for the characteristics of bondwires after a basic understanding of geometrical characteristics of bondwire inductance as described previously. Three of the most popular techniques that have been used to simulate bondwire include the finite-difference time-domain method, the method-of-moments (MoM), and the finite-element method (FEM). Among the three techniques, we have focused on the FEM in ADS due to its greater versatility and accuracy and it will be adopted for the design and modeling of bondwire-based components in the next sections.

5.1.2. LOSSES AND CURRENT-HANDLING OF BONDWIRES

Additional importance consideration when employing bondwires is the current-handling of bondwires related to the losses. There exist two main types of losses for bondwires, namely ohmic loss and Eddy current loss. Compared with monolithic inductors, the losses associated to Eddy currents are much lower for bondwires due to the much larger separation from the ground. At low frequencies the ohmic loss dominates and its value is simply related to the DC resistance of the conductors which is determined by their material properties and their physical dimensions. At high frequencies the current density becomes non-uniform due to eddy currents which cause skin effect. The skin effect decreases the effective cross-section area of the conductors and thus the AC resistance increases. Since the skin depth δ at frequency ω is given by

$$\delta = 1/\sqrt{\pi \cdot f \cdot \mu \cdot \sigma} \tag{5.4}$$

Then the AC resistance per-unit-length R'_{AC} can be calculated as

$$R'_{AC} = \frac{1}{\pi\sigma(r_w^2 - (r_w - \sigma)^2)} \approx \frac{1}{2\pi \cdot \sigma \cdot r_w \cdot \delta} \tag{5.5}$$

where σ is the conductivity of the material and r_w is the radius of a single round-wire conductor. For example, for 50μm-diameter aluminium and gold wires at 2.1 GHz, the resulting R'_{AC} is about 102 and 110 $m\Omega/mm$ per wire, respectively [16].

When current is flowing through the conductor, the losses due to R'_{AC} are converted into heat. If significant current is passing through the conductor wire, the temperature rise could be significant enough to fuse the conductor. The current level at which the wire can melt is known as fusing current and sets a hard limit for the current-handling capability for the wires. For instance, a 5 mm-long and 50 μm-diameter AlMg wire has a fusing current of about 0.7 A at 1.8 GHz, while gold wires can support about 25% higher currents [16]. Even though parallel connection of wires will reduce losses and increase the current-handling capability, conservative limits are recommended to avoid this failure mechanism.

5.2. BONDWIRE BASED TRANSFORMER

Bondwires are quite popolar for the implementation of high-quality magnetic components in matching networks for high-power applications due to their excellent inductive properties, low losses and high current-handling capabilities. In addition, bondwires have sufficiently high resonance frequencies that allows operation up to a few gigaherz while still allowing the use of a lumped equivalent model approximation. In this section, we start with the design and modeling of bondwires(array) to better support the design of the bondwire-based transformer.

5.2.1. DESIGN AND MODELING OF BONDWIRES

In ADS, the geometrical characteristics of a bondwire can be described with the 5-point JEDEC model in Figure 5.2, where five independent parameters (three distance parameters D, H_1 and H_2, and two positive angles α and β) are introduced to define the bondwire shape. As long as their shapes are well-known, bondwire arrays can be accurately simulated using FEM in ADS.

Generally, the lumped equivalent circuit of a bondwire is given in terms of a pi-network that consists of a series inductance L, a series resistance R and two shunt capacitances C_1 and C_2 (see the inner pi-network in Figure 5.3(a). The external and surrounding capacitors C_{d1} and C_{d2} represent parasitic capacitance due to artificial ports in the simulation

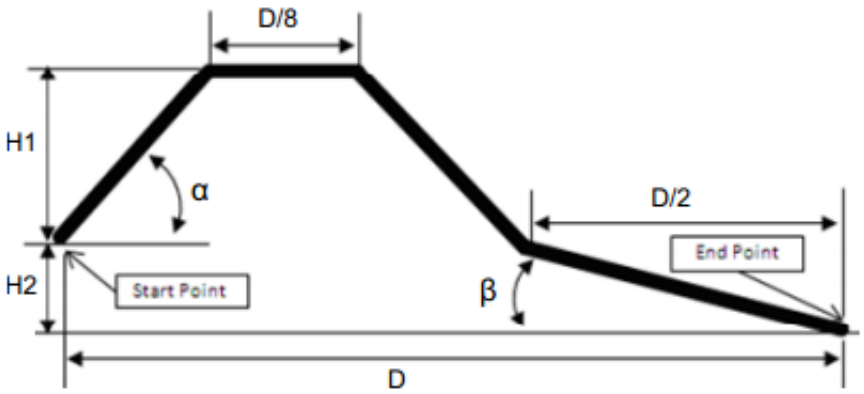


Figure 5.2: 5-point JEDEC model in ADS

bench if any. To get the accurate value of the bondwire capacitance, ports $1'-2'$ need to be de-embedded, which can be done by seperately performing two simulations: one with the entire structure and its ports (Y_{all}) and the other with only the ports (Y_{par}). Then we can obtain the desirable Y-parameters of the inner bondwire structure (Y_{DUT}), given by $Y_{DUT} = Y_{all} - Y_{par}$ [32]. With the resulting Y_{DUT}, the equivalent circuit elements can be easily derived using the following expressions

$$L = \frac{-im(Y_{12})}{\omega} \tag{5.6}$$

$$R = re(Y_{12}) \tag{5.7}$$

$$C_1 = \frac{im(Y_{11} + Y_{12})}{\omega} \tag{5.8}$$

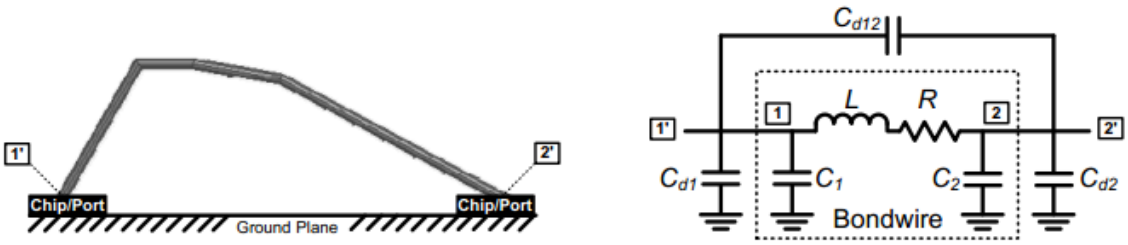
$$C_2 = \frac{im(Y_{22} + Y_{12})}{\omega} \tag{5.9}$$

Then the quality factor is given by

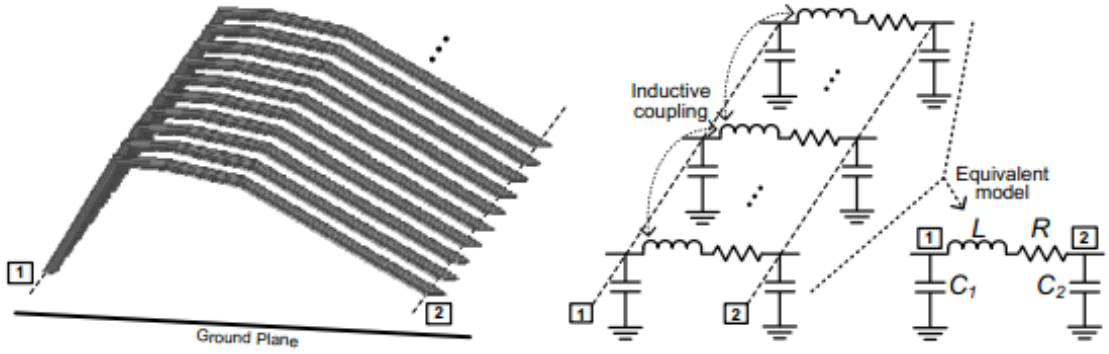
$$Q_L = \frac{\omega L}{R} = \frac{-im(Y_{12})}{re(Y_{12})} \tag{5.10}$$

A Single bondwire is rarely employed in power transistors. Instead, large numbers of bondwires are included in parallel to form an array as illustrated in Figure 5.3(b). Note that the capacitance from ports $1-2$ are negligible for simplicity. The parallel connection results in the inductance decreasing and capacitance increasing as the number of wires in the array increases.

With the background above, the geometrical characteristics of bondwires can be investigated. As can be concluded from the discussion in the previous subsection, the inductance of a bondwire basically depends on the geometry of the loop formed with the



(a) Lateral view of a single bondwire and the lumped equivalent circuit



(b) Lateral view of an array of bondwires and the lumped equivalent circuit

Figure 5.3: Compact model of 2-port bondwire inductor structures: a) before and b) after de-embedding

ground, its cross-section area and other conductors nearby which could be coupled. Variables such as the wire material and wire diameter are normally fixed for a given bonding process. Therefore, for the design of a bondwire-based inductor, parameters including the number of parallel bondwires (BW_N), bondwire pitch (BW_P), bondwire length (BW_L) and bondwire height (BW_H) can be ultilised to achieve different inductance values. How the bondwire characteristics including bondwire length (BW_L), bondwire height (including height between the bond pad and ground (SUB) and height between the bond pad and the top of the bondwire loop (BW_H)), bondwire pitch (BW_P) and the number of parallel bondwires (BW_N) affect the inductance of a bondwire array has been detailly investigated in [54] with computational electromagnetic techniques (HFSS) as depicted in Figure 7.38 and Table 5.1. To summarize, increasing the value of BW_L and BW_H will result in a large inductance value, as discussed in Section 5.1 with the idealized case of a couple of identical parallel round-wire conductors over ground. This inductance will drop as more bondwires are connected in parallel or the wires are placed further to one another. Note that the total inductance is not directly proportional to $1/BW_N$. In reality, as the original bondwire number becomes larger, doubling it (from 2 to 4 or from 4 to 8) leads to a smaller effect on decreasing the total inductance. In addition, it can be observed from Table 5.1 that the a

thicker substrate will result in a larger inductance.

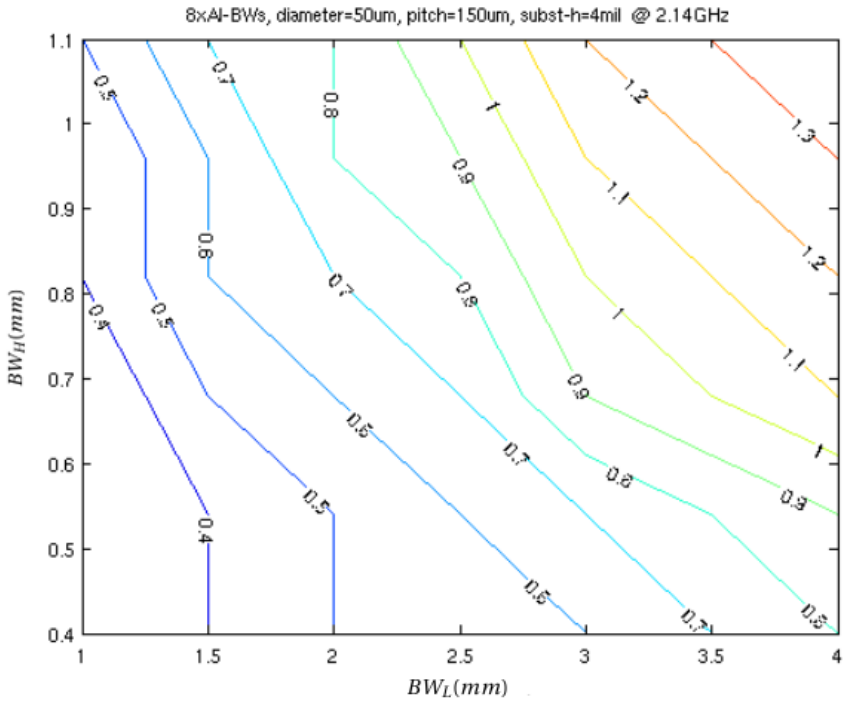


Figure 5.4: Example of an inductance design chart simulated by HFSS with different bondwire length (BW_L) and bondwire height (BW_H)[54].

Table 5.1: Bondwire inductances with different pad-to-ground height (or substrate thickness), different pitch and different bondwire numbers (In this case, PCB material is Roger 4350b, $BW_L = 2mm$, $BW_H = 0.4mm$) [54]

$BW_P@SUB$ \ BW_N	2	4	8
150um @ 4mile	1.1 nH	0.7 nH	0.5 nH
300um @ 4mile	1.0 nH	0.5 nH	0.3 nH
300um @ 10mile	1.1 nH	0.7 nH	0.4 nH

5.2.2. DESIGN AND MODELING OF BONDWIRE TRANSFORMERS

As expected from Equation (5.2), the loops of two arrays of bondwires in close proximity will be magnetically coupled, thus it can be advantageously ultilised to implement a transformer. There exist two different topologies for bondwire-based transformers in previous literatures, namely the series connected topology (or multi-turn) [55] and parallel connected topology (or single-turn) [56]. Either of these two structures will resemble an ordinary 2-port transformer if one end of each bondwire array is grounded, for example either by a large capacitor (AC ground) or by a metallic bar (DC ground).

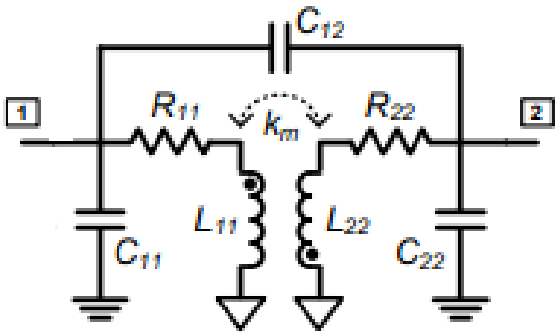


Figure 5.5: compact model of 2-port bondwire transformers.

Generally speaking, a transformer with a high coupling factor, a large quality factor and a great turn ratio is desirable. In order to extract the electrical properties of a transformer, a two-port transformer model shown in Figure 5.5 is assumed (the dot con-vention used indicates the direction where the currents are flowing into on each side). L_{11} and L_{22} are the primary and secondary self-inductances. k_m is the magnetic coupling coefficient. The ohmic losses in the bonding wires are modeled by the series resistances R_{11} and R_{22}, while C_{11} and C_{22} represent the parasitic capacitances. Finally, C_{12} is the port-to-port capacitance. At low frequencies, the inductive behavior dominates and the parasitic capacitance C_{11}, C_{22} and C_{12} can be neglected. From measured Z-parameters, the self inductance and quality factor can be simply extracted as the following:

$$L_{11} = \frac{Z_{11}}{\omega} \tag{5.11}$$

$$L_{22} = \frac{Z_{22}}{\omega} \tag{5.12}$$

$$Q_{L1} = \frac{imZ_{11}}{re(Z_{11})} \tag{5.13}$$

$$Q_{L2} = \frac{imZ_{22}}{re(Z_{22})} \tag{5.14}$$

The coupling coefficient $k_m$and turn ratio N can be calculated as

$$k_m = \sqrt{\frac{im(Z_{12}) \cdot im(Z_{21})}{im(Z_{11}) \cdot im(Z_{22})}} \tag{5.15}$$

$$N = \sqrt{\frac{L_{22}}{L_{11}}} \tag{5.16}$$

At higher frequencies, however, the capacitances will cause resonance, modifying the relatively flat behavior of the magnetic quantities simply extracted such as its self and mutual

inductances, quality factor, and coupling coefficient.In the following discussion, 4 different designs for the bondwire-based transformer are listed, each with its advantages and disadvantages.

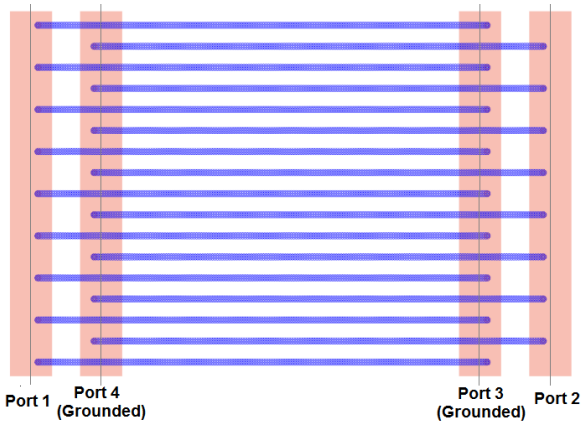


Figure 5.6: Bondwire transformer Case1: Parallel-to-parallel connection

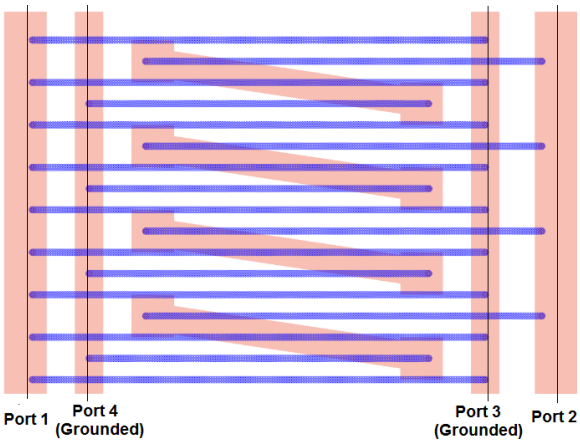


Figure 5.7: Bondwire transformer Case2: Parallel-to-parallel connection (two-steps)

The first prototype (Case 1), as described in Figure 5.6, is a symmetric single-turn transformer with 9 parallel bondwires in primary and 8 parallel bondwires in secondary windings. Fig 5.10 shows the extracted parameters for the simple parallel-to-parallel transformer (Case 1) . It can be observed that this transformer can realize a high coupling coefficient (above 0.7), a high self-resonant frequency (about 11.35GHz) and a low turn ratio (below 1). The second transformer (Case 2), as shown in Figure 5.7, differs from the first prototype in the secondary windings, where two bondwires are connected in series by the trace instead of a single bondwire. Fig 5.11 shows the extracted parameters for the transformer in Figure 5.7. The coupling factor of this transformer (Complex parallel-to-parallel) can also be above 0.7. What's more, it has a larger turn ratio which is above 1. The only drawback is that the self-resonant frequency is much lower (about 6.85GHz).

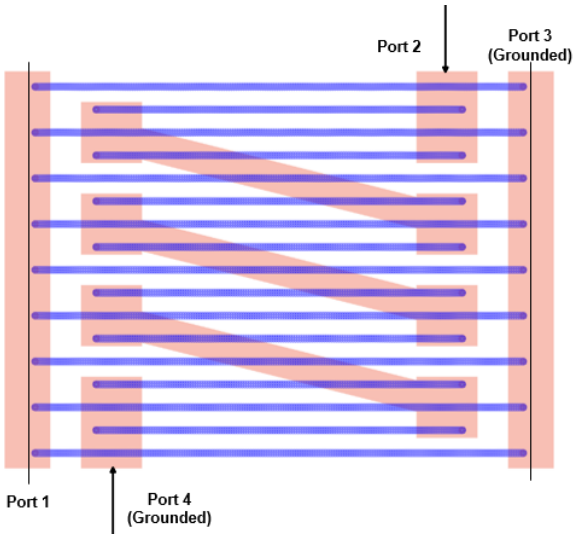


Figure 5.8: Bondwire transformers: a) coupled bondwire arrays, and b) compact model of 2-port bondwire transformers.

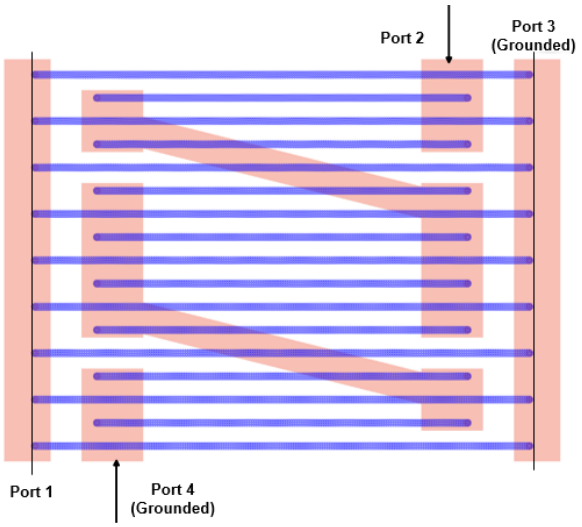
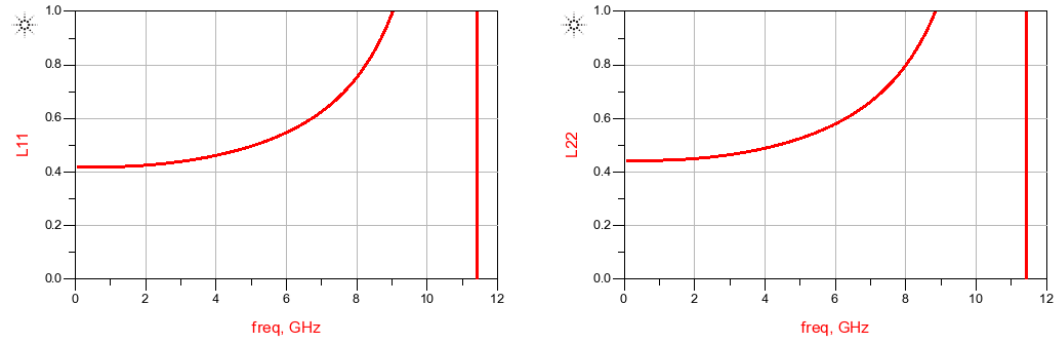


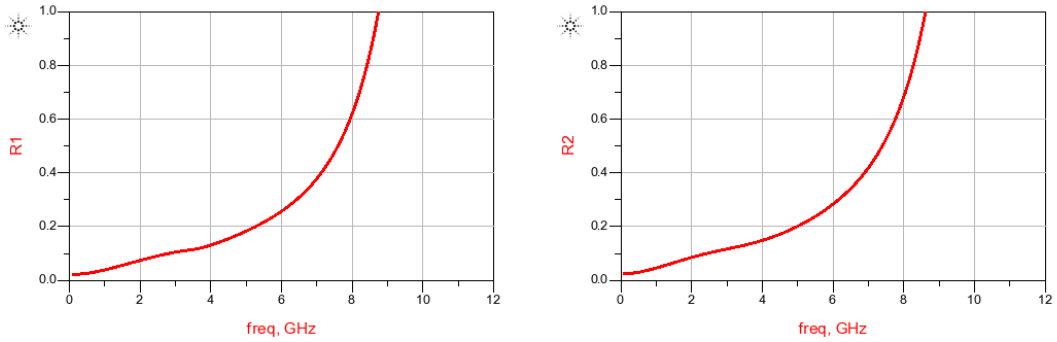
Figure 5.9: Bondwire transformers: a) coupled bondwire arrays, and b) compact model of 2-port bondwire transformers.

The third prototype (Case 3) and the forth prototype (Case 4) as depicted in Figure 5.8 and 5.9, are based on the parallel-to-series connection where 9 parallel bondwires forms the primary windings and several bondwire sets connected in series form the secondary windings. Fig 5.12 shows the extracted parameters for the transformer in Figure 5.8. We can observed that this transformer (parallel-to-series) can realize a high coupling coefficient which is above 0.6, a high turn ratio which is above 2 but it ends up with a low self-resonant frequency (about 4.68GHz). The transformer in 5.9 increses the self-inductance from 4.68GHz to 6.16GHz at the cost of the slightly decreased turn ratio.

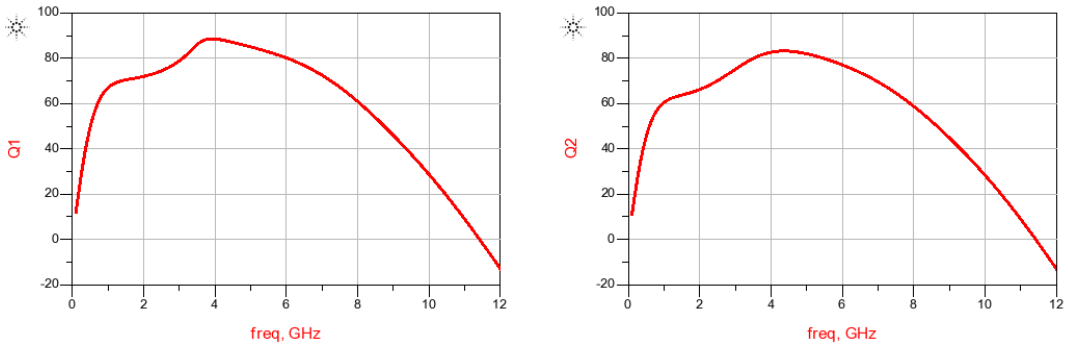
Table 5.2 summarizes the performance of the 4 transformer designs. In all, the parallel-to-parallel topology has a higher self-resonant frequency and a larger coupling coefficient,



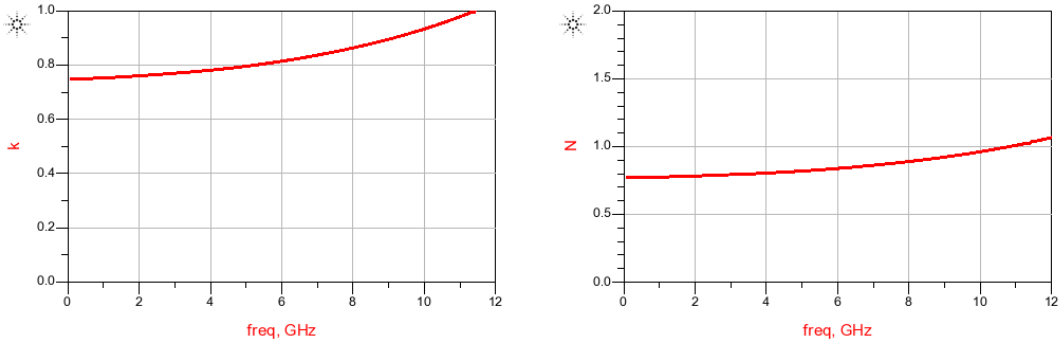
(a) Self-inductance



(b) Series resistance

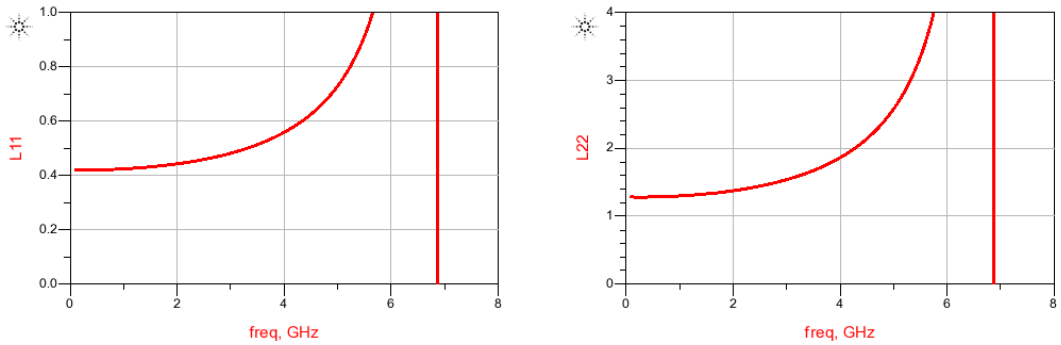


(c) Quality factor

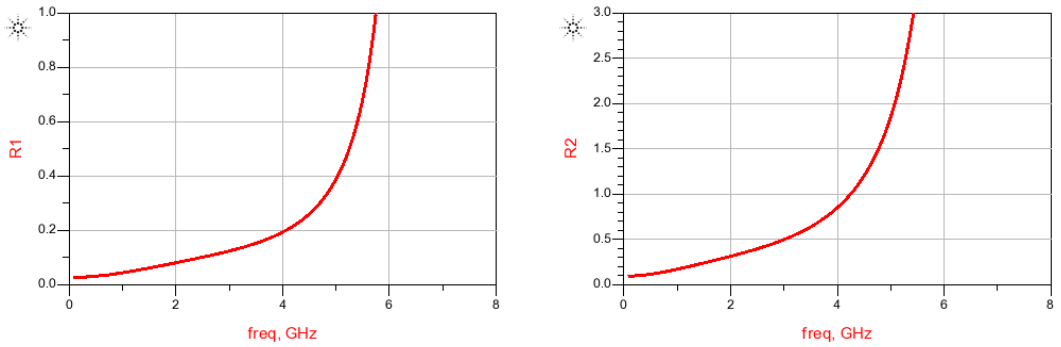


(d) Coupling factor k and effective turn ratio

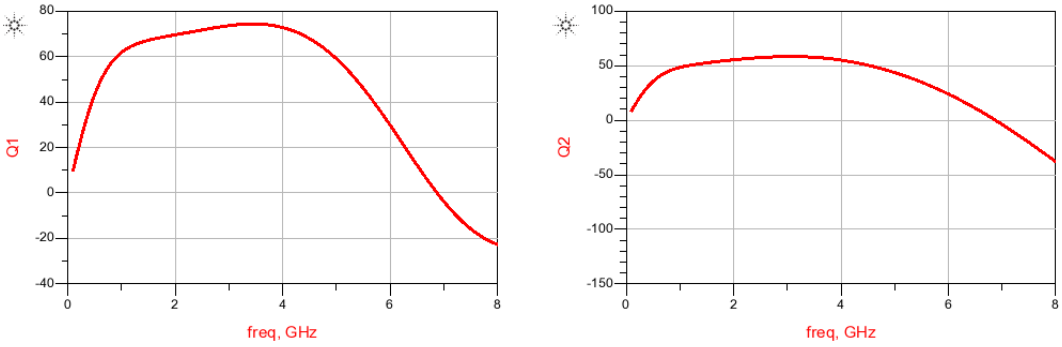
Figure 5.10: Simulated results for the Case 1 parallel-to-parallel bondwire-based transformer a) Self inductance and b) Series resistance c) Quality factor d)Coupling factor and effective turn-ratio



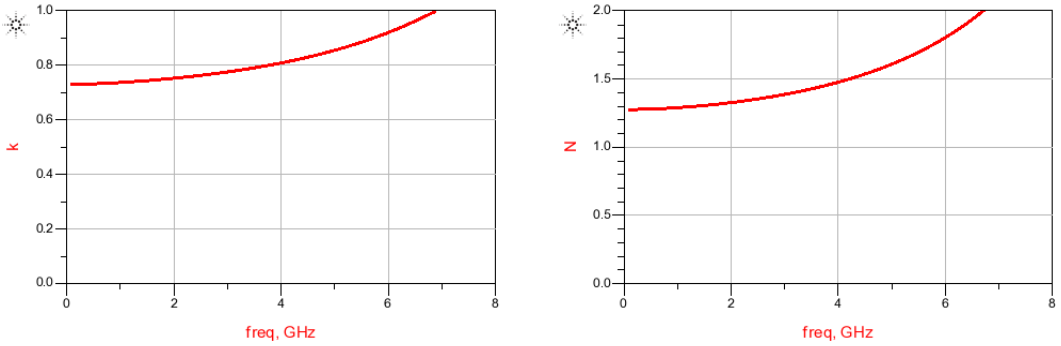
(a) Self-inductance



(b) Series resistance

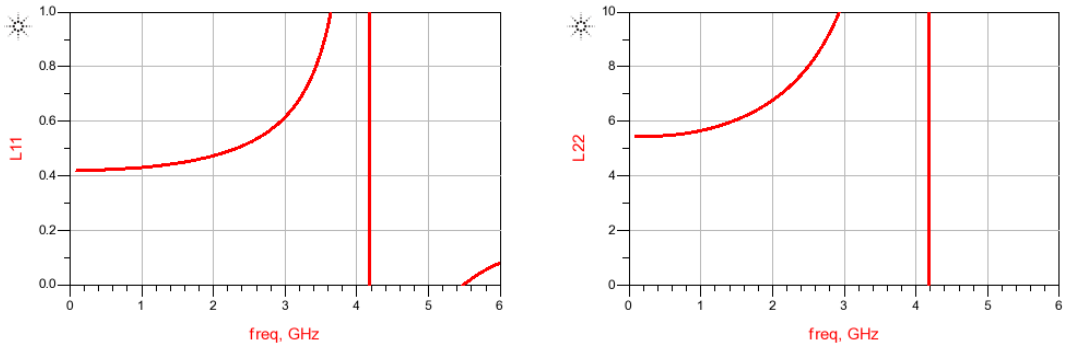


(c) Quality factor

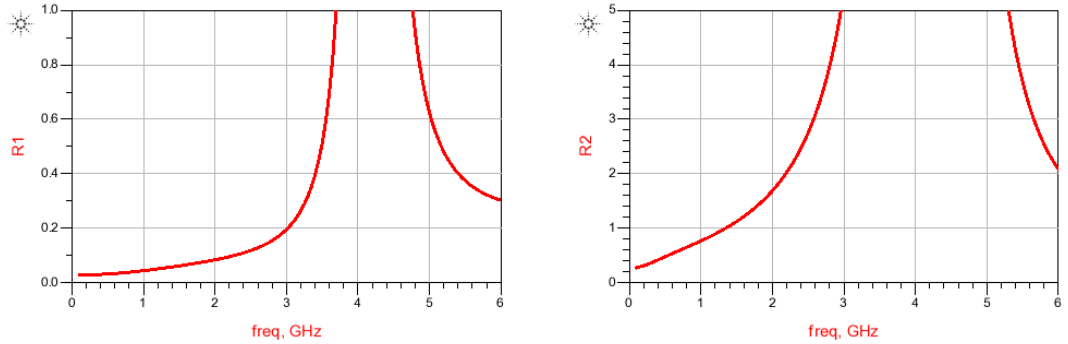


(d) Coupling factor k and effective turn ratio

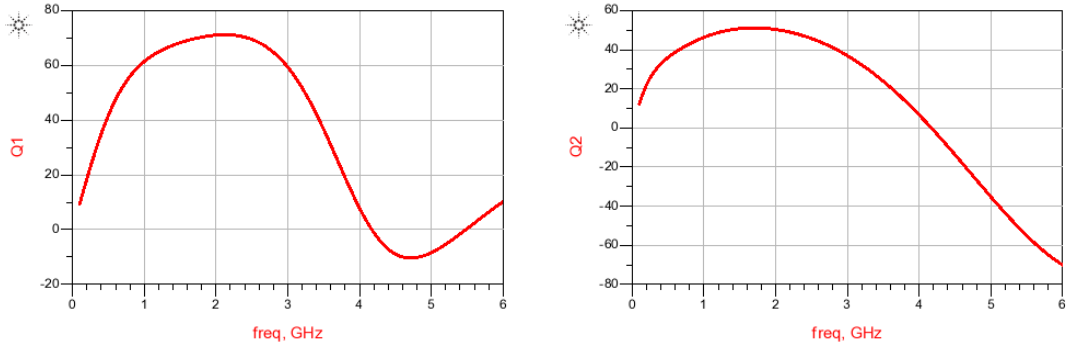
Figure 5.11: Simulated results for the Case 2 complex parallel-to-parallel bondwire-based transformer a) Self inductance and b) Series resistance c) Quality factor d)Coupling factor and effective turn-ratio



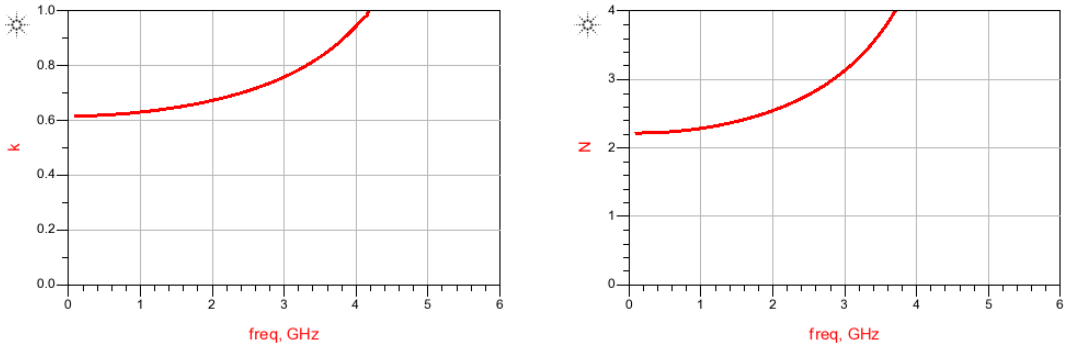
(a) Self-inductance



(b) Series resistance

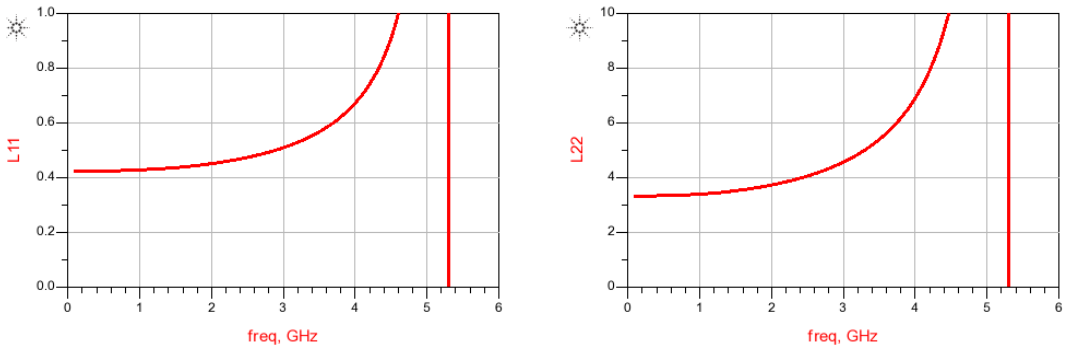


(c) Quality factor

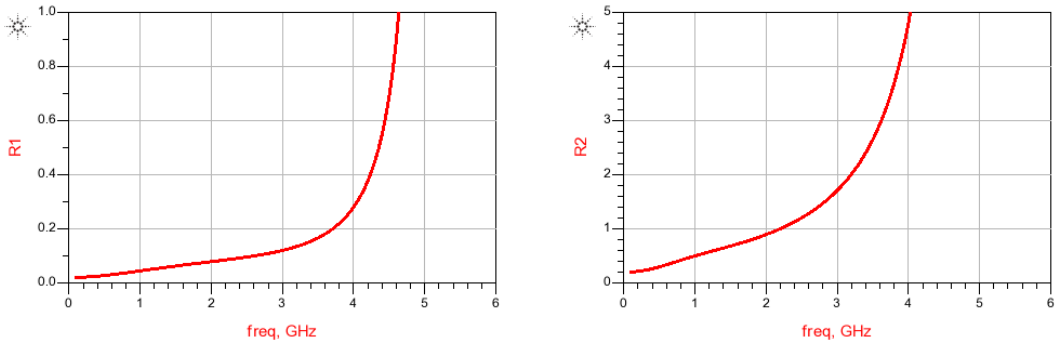


(d) Coupling factor k and effective turn ratio

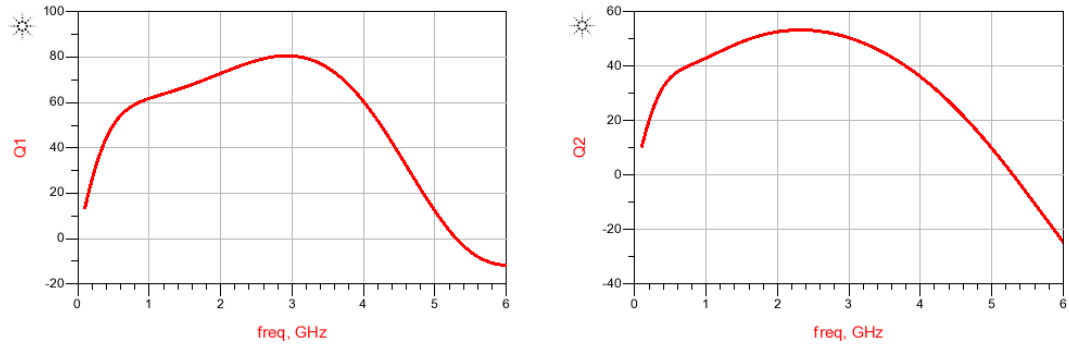
Figure 5.12: Simulated results for the Case 3 parallel-to-series bondwire-based transformer a) Self inductance and b) Series resistance c) Quality factor d)Coupling factor and effective turn-ratio



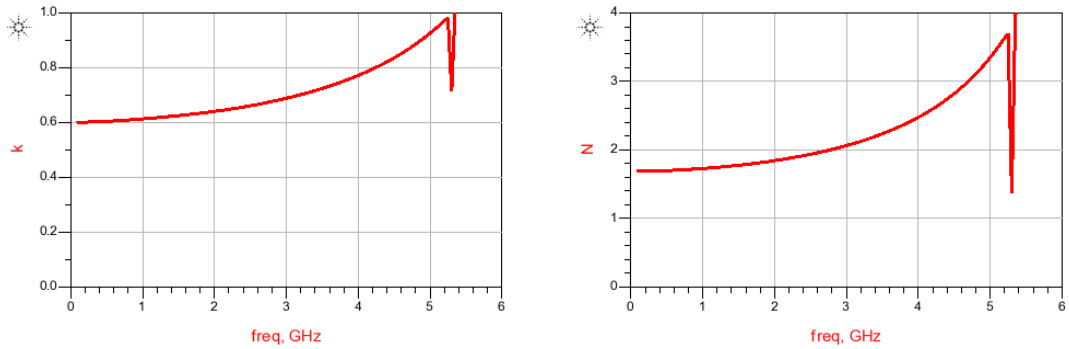
(a) Self-inductance



(b) Series resistance



(c) Quality factor



(d) Coupling factor k and effective turn ratio

Figure 5.13: Simulated results for the Case 4 parallel-to-series bondwire-based transformer a) Self inductance and b) Series resistance c) Quality factor d)Coupling factor and effective turn-ratio

but its turn-ratio is not suffciently high. On the contrary, the parallel-to-series topology contributes to a large turn-ratio but it is limited to lower frequency application.

Table 5.2: Summary of the 4 transformer design in terms of self-inductance (L_{11}, L_{22}), quality factor (Q_1, Q_2), coupling coefficient (k_m) and effective turn-ratio (N) at 2.4 GHz and self-resonant frequency f_{max}

Design / Performance	Case 1	Case 2	Case 3	Case 4
L_{11} (nH)	0.430	0.455	0.510	0.468
L_{22} (nH)	0.455	1.428	7.711	3.98
Q_1	73.8	71.3	70.3	73.5
Q_2	69.2	57.1	47.0	53.3
k_m	0.764	0.761	0.701	0.656
N	0.786	1.350	2.725	1.912
f_{max} (GHz)	11.45	6.90	4.20	5.35

5.3. WIDEBAND BALUN DESIGN USING BONDWIRE-BASED TRANSFORMER

Magnetic coupling between bonding wires can also be advantageously used to transform a differential signal to a single-ended signal by combining two bondwire-based transformers. Because bonding wires are very good conductors, this differential to single-ended signal transformation can be performed with minimal signal loss. Moreover, since bonding wires are already part of an integrated circuit package, both system cost and board resources are minimized. Based on the transformer design in the previous section, 3 different balun topologies (see Figure 5.18, 5.20 and Figure 5.22) are given here which correspond to the transformer designs Case 1, Case 2 and Case 4 in the previous section. The simulation setup is depicted in Figure 5.14 where the balun input (Port 1 and port 2)is differentially driven. In addition, a parallel capacitor is inserted at the input and a series capacitor is added at the output to resonant out the inductive parts of the two terminals. The simulated results in terms of the insertion loss (dB(S12)) and return loss (dB(S11)) for the three balun designs are given in Figure 5.15, showing a low-loss property over a wide bandwidth.

Next, we make use of the simulation setup shown in Figure 5.16 to investigate the am-

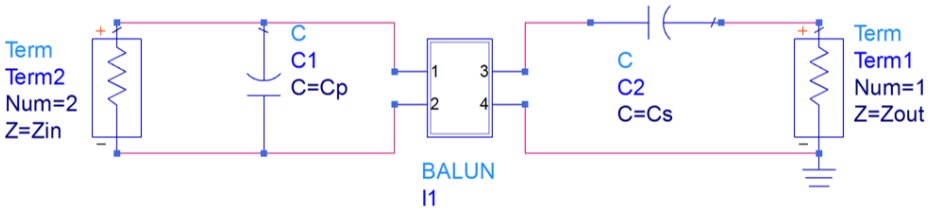
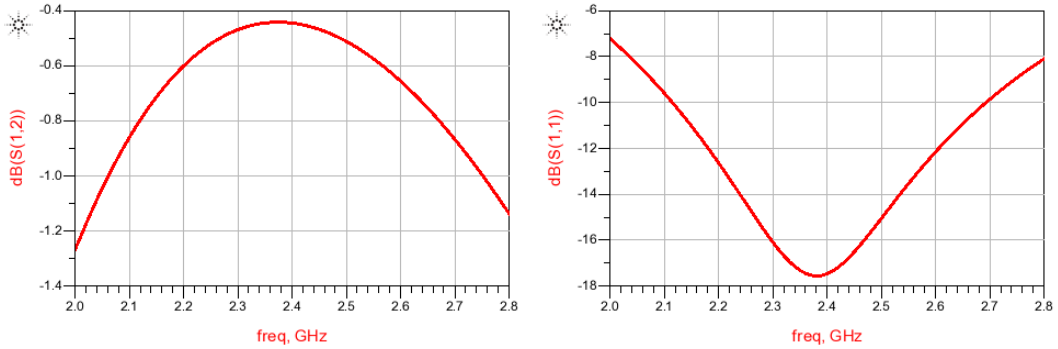


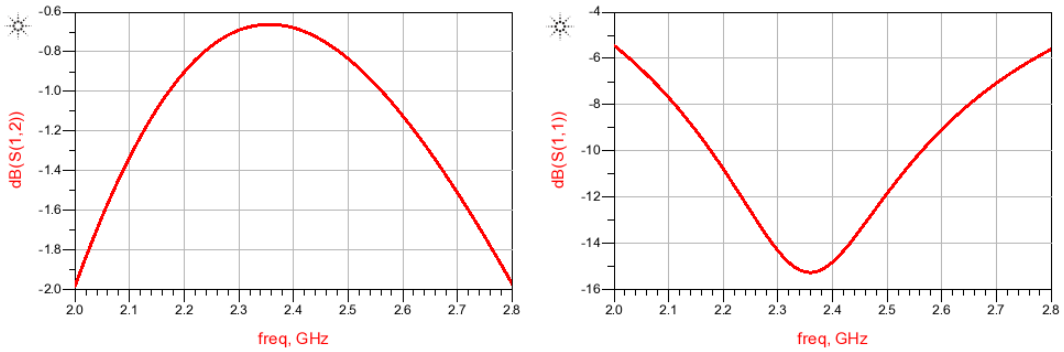
Figure 5.14: 2-port S-parameter simulation setup for the three different balun designs

Table 5.3: Setup schematic design details for the 3 different balun topologies

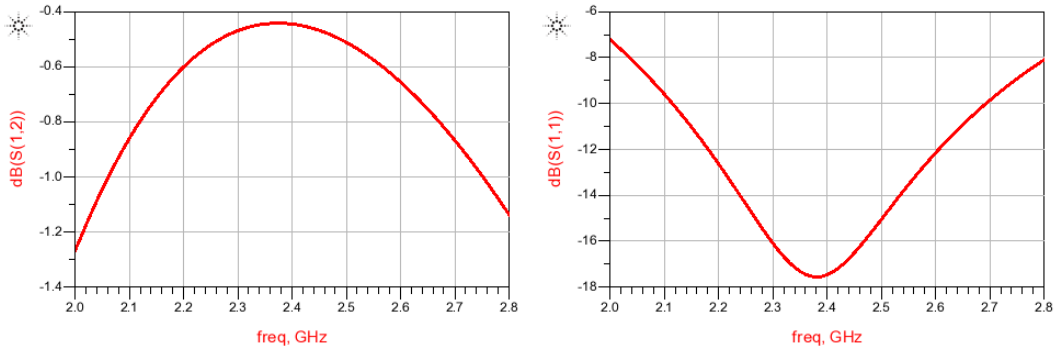
Design / Details	Case 1	Case 2	Case 3
C_P (pF)	4.75	4.02	2.90
C_S (pF)	6.00	2.15	0.47
Z_{in} (Ω)	10	10	10
Z_{out} (Ω)	4.5	13.5	50.0



(a) Case 1



(b) case2



(c) Case 3

Figure 5.15: Simulated results in terms of the insertion loss and return loss for the three different balun designs

plitude and phase imbalunce for the three balun designs. The first prototype employs

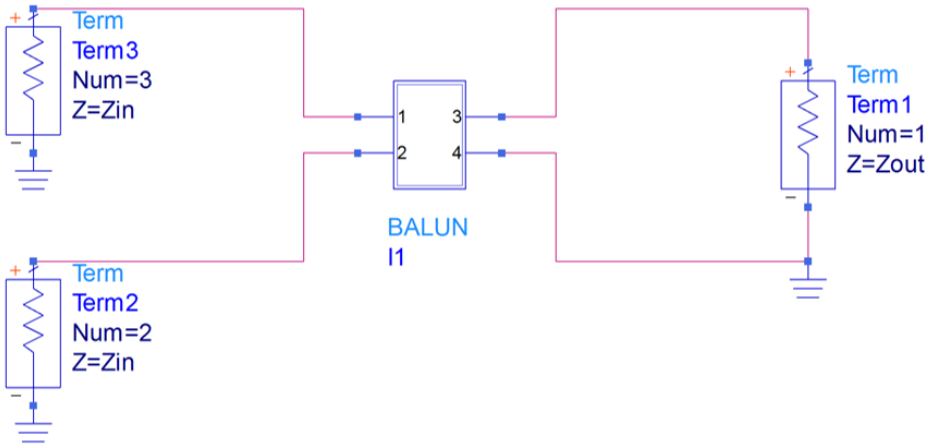
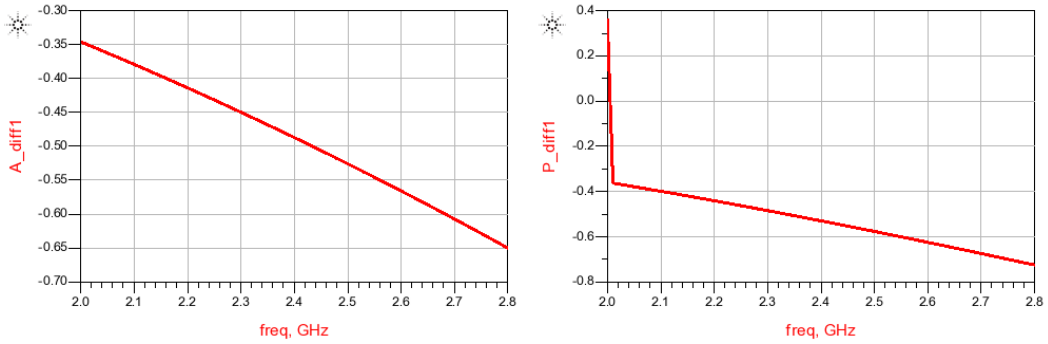
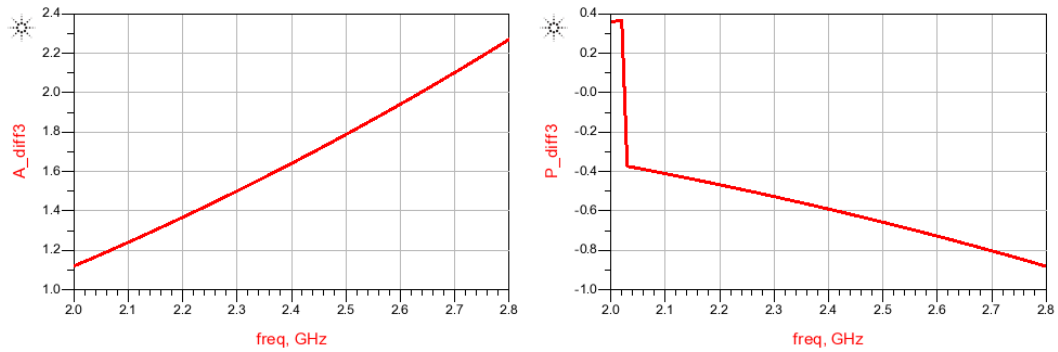


Figure 5.16: 3-port S-parameter simulation setup for the three different balun designs

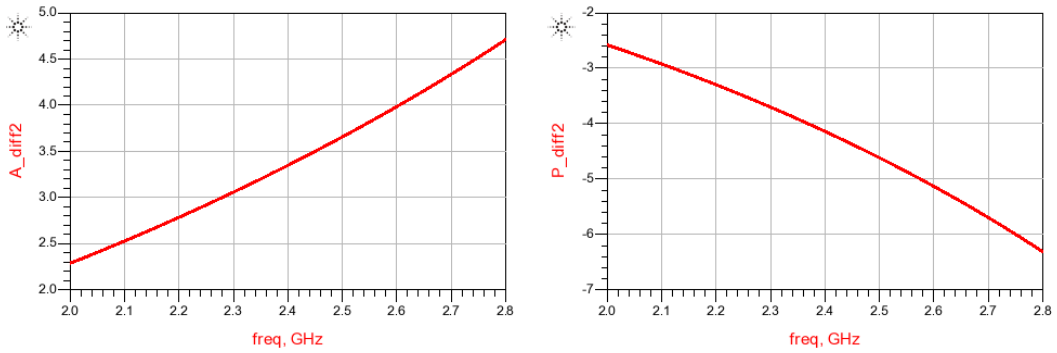
two symmetrical parallel-to-parallel connected transformers (see Figure 5.6(a)). The corresponding 3-port S-parameter is plotted in Figure 5.17 (a). Apparently, in the frequency range from 2.0 GHz to 2.8 GHz, the amplitude difference is better than -0.7dB, meanwhile the phase difference is better than 0.8 deg, exhibiting a well-balanced impedance transformation. However, for this balun topology, the transformation ratio is smaller than 1, which is not ideal for high-power PAs. The idea of the balun shown in Figure 5.20 is originally from the transformer as depicted in Figure 5.7. This topology can provide a larger impedance transformation ratio but as can be predicted from Figure 5.17(b), it results in a quite unbalanced behaviour with 1.1-2.3 dB amplitude difference and -1-0.4 deg phase difference from 2.0 GHz to 2.8 GHz, due to the large paratistic capacitance (Note that the substrate is as thin as 4 miles) in the secondary windings. The last design presented here is based on the transformer shown in Figure 5.9. It can provide the largest impedance transformation ratio but the imbalance issue is even more serious in this case. Since this imperfect is mainly due to the paracitics of the thin substrate, increasing the thickness of the substrate will undoubtedly help improve the balance, but it also leads to the decrease of coupling coefficient. To sum up, the designs employing a complex parallel-to-parallel connection (Case 2) and a parallel-to-series connection (Case 3) are more suited for a high power PA because of the larger turn-ratio compared with the symmetrical parallel-to-parallel based balun topology, but more efforts are needed to solve the imbalance problem. Another challenge to implement a bondwire-based balun is due to the large variations in bondwire shapes (such as bondwire length and bondwire height), since wire bonding is a mechanical process that cannot be as tightly controlled as a photolithographic processes. This may result in a significant difference between the practical design and simulation results.



(a) Case 1



(b) case2



(c) Case 3

Figure 5.17: Simulated results in terms of amplitude and phase difference for the three different balun designs employing the setup in Figure 5.16

5.4. CONCLUSIONS

Transformers employing bondwires can potentially provide significant benefits in terms of low losses because of their relatively high Q (on the order of 50). Instead of the symmetrical parallel-to-parallel single-turn transformer, the practical demonstration focuses on the novel parallel-to-series transformers and they have been confirmed to simultaneously achieve high turn ratio and coupling coefficient using 3D EM simulations (FEM) in ADS. However, it comes to difficulty when combining two transformers to form a balun because of the significant amplitude and phase imbalance caused by the parasitics between the in-

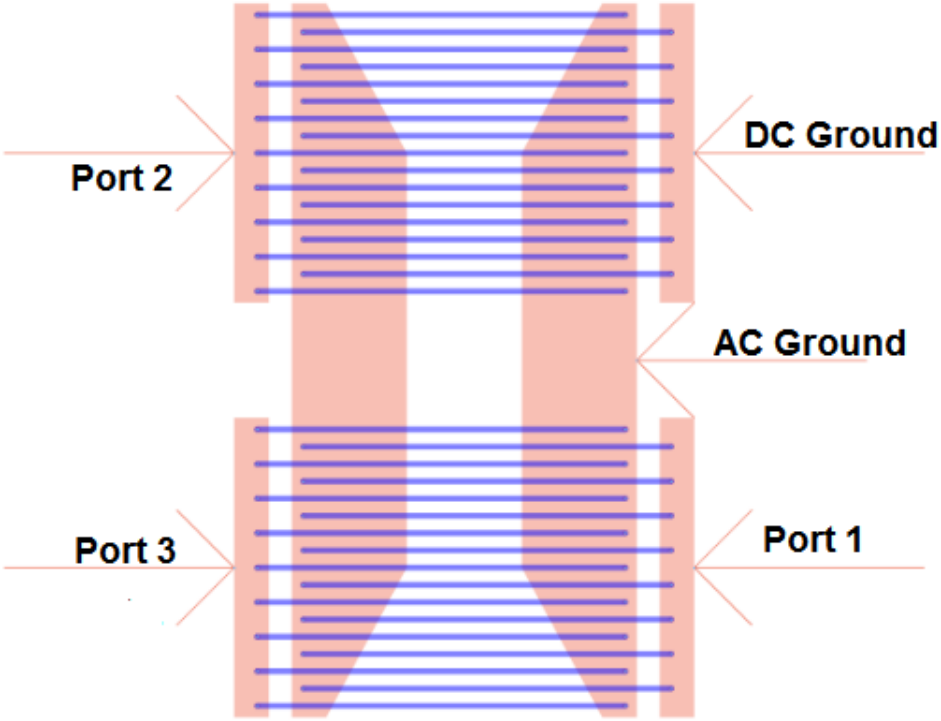


Figure 5.18: Bondwire balun Case1: based on the symmetrical single-turn parallel-to-parallel connection in Figure5.6

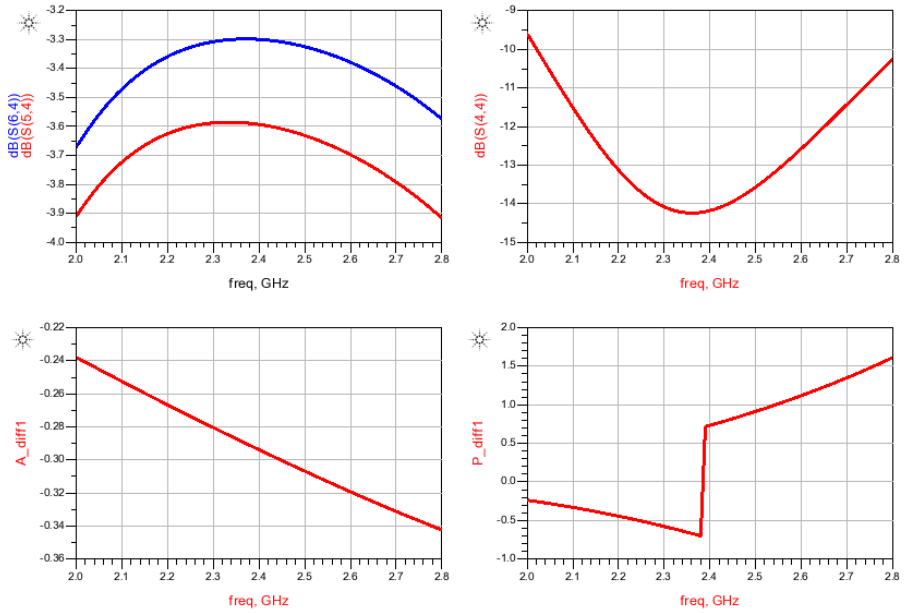


Figure 5.19: Simulation results for bondwire balun Case1: based on the symmetrical single-turn parallel-to-parallel connection in Figure5.6

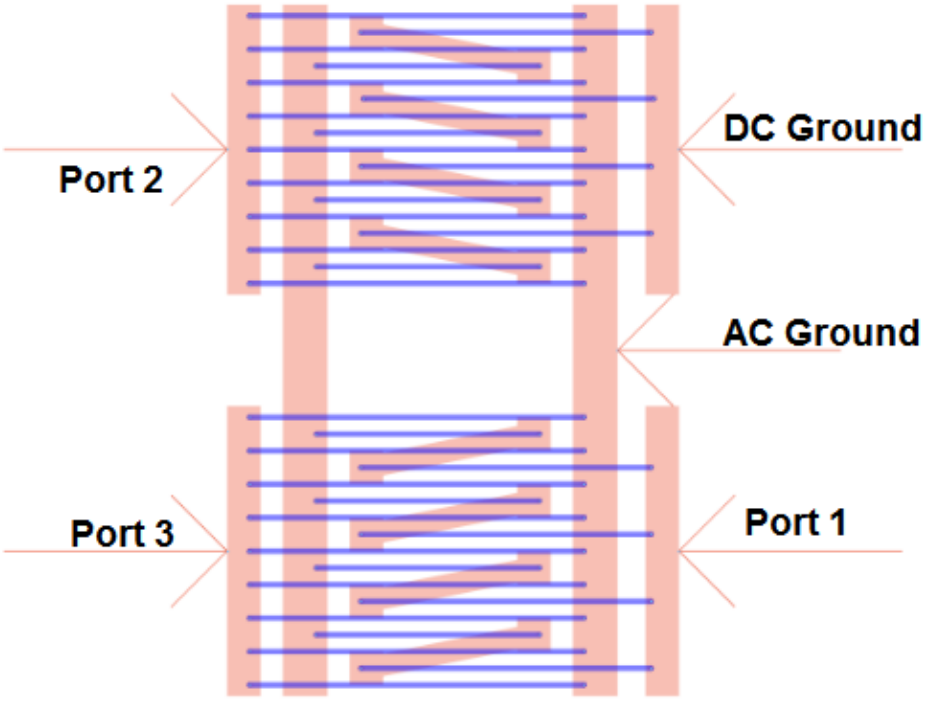


Figure 5.20: Bondwire balun Case2: based on the complex parallel-to-parallel connection in Figure5.7

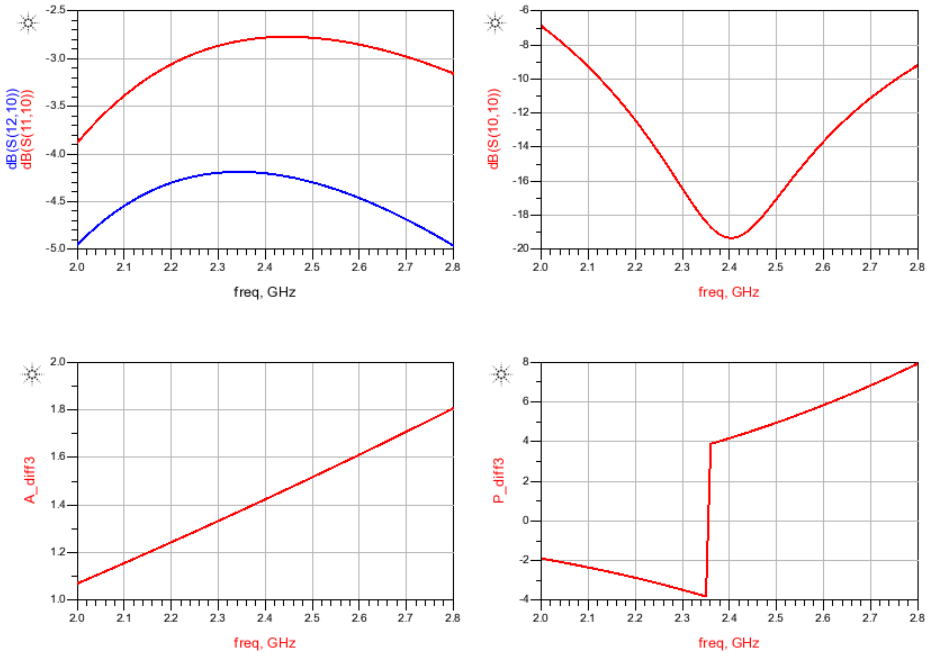


Figure 5.21: Simulation results for bondwire balun Case2: based on the complex parallel-to-parallel connection in Figure5.7

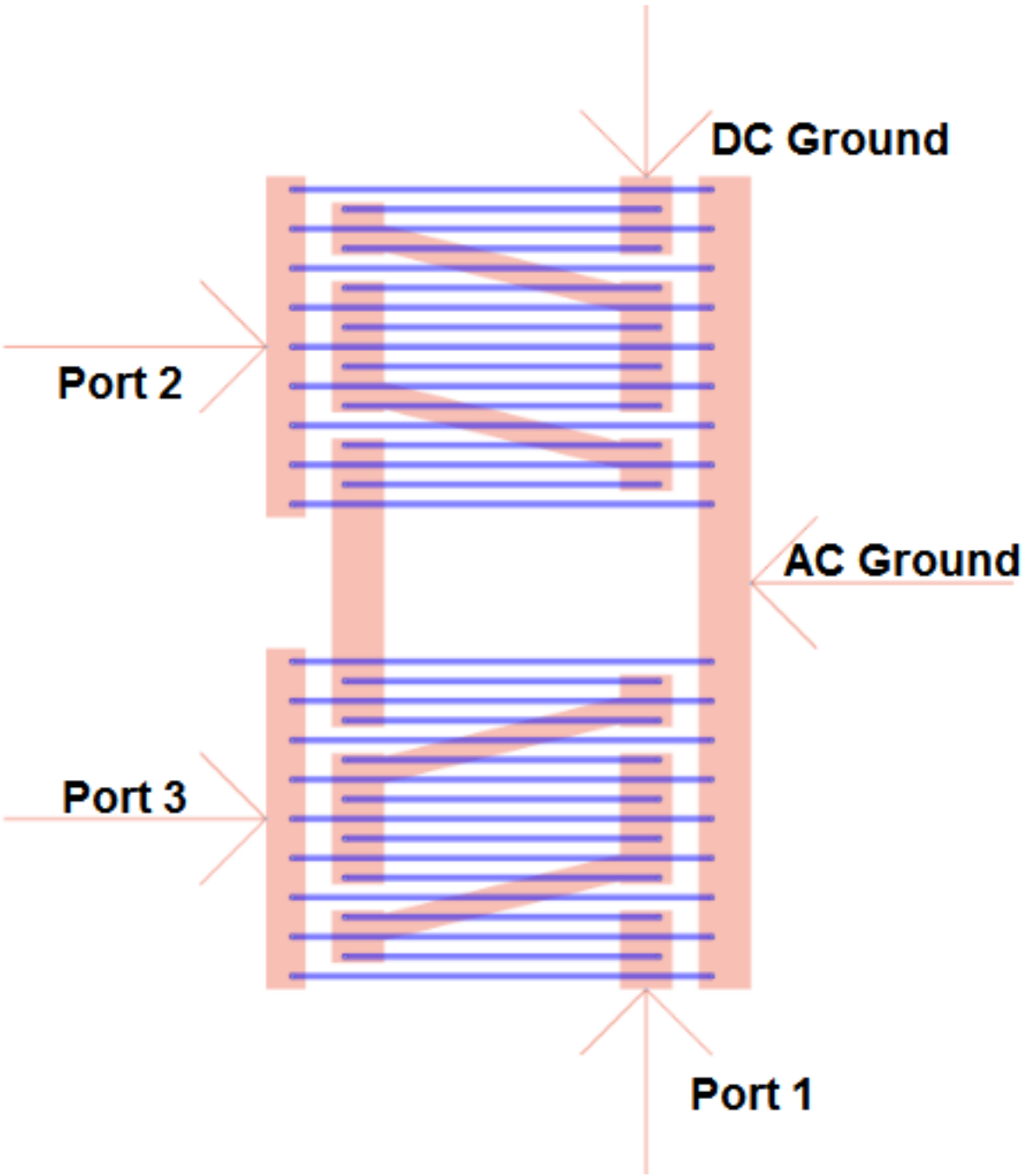


Figure 5.22: Bondwire balun Case3: based on the parallel-to-series connection in Figure**??**

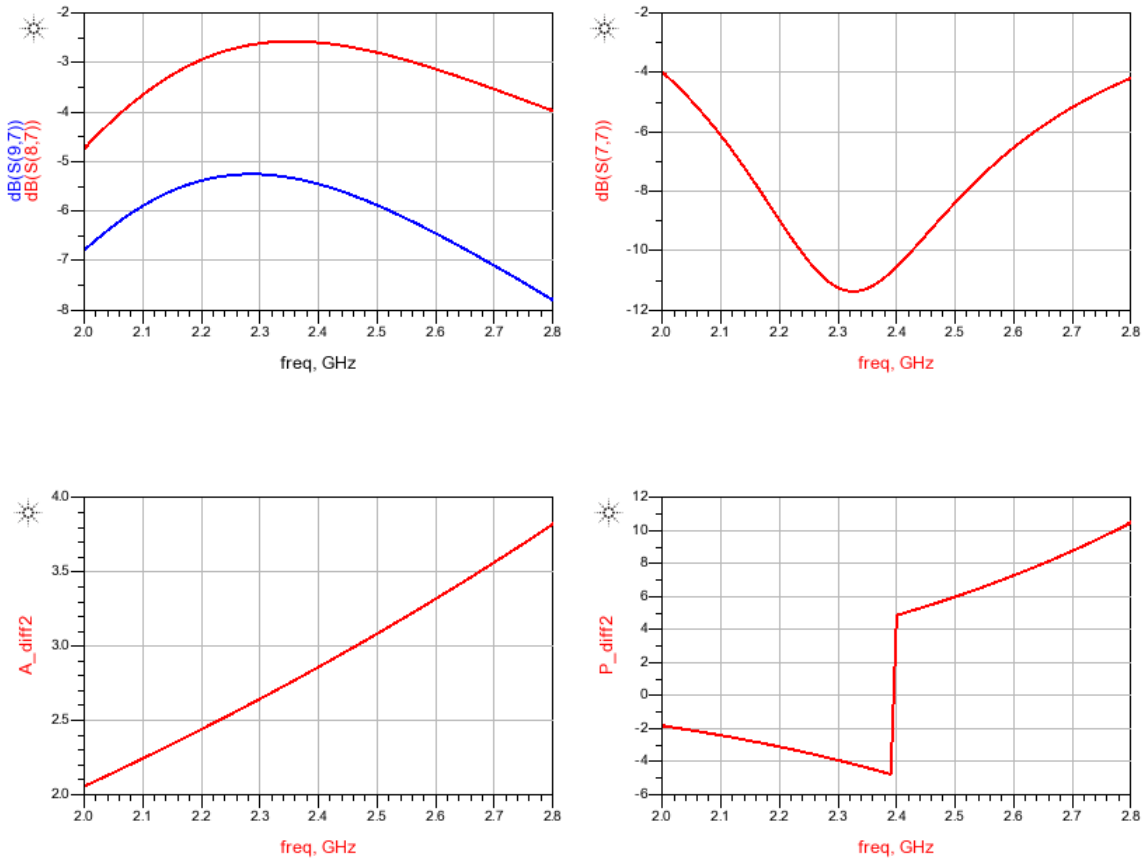


Figure 5.23: Simulation results for bondwire balun Case1:based on the parallel-to-series connection in Figure**??**

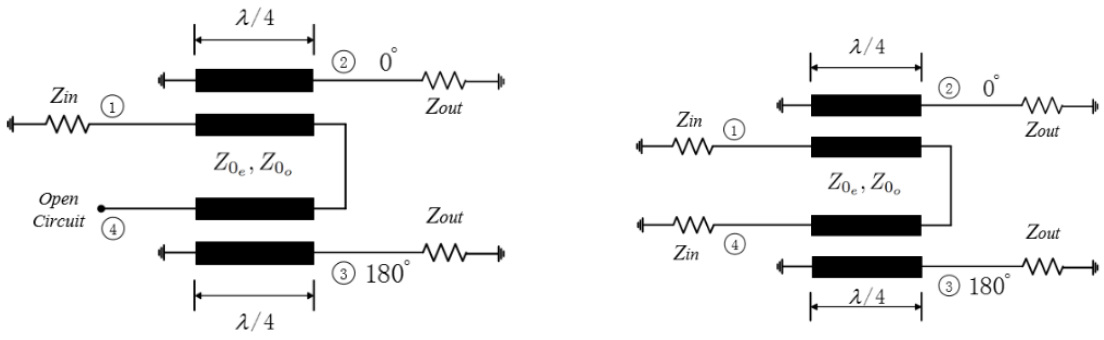
terconnect trace and the thin substrate. Therefore, more efforts are required to improve the balance.

6

WIDEBAND BALUN DESIGN CASE 2: COUPLED LINE BASED

In addition to magnetic coupling, transmission line coupling can also be ultilised to implement a balun. Within this chapter, we will continue to explore wideband balun structures. A large number of transmission line based balun configurations have been reported in literature [57–61]. Among them, the planar Marchand balun is perhaps one of the most attractive topology because of its relatively wider bandwidth of amplitude and phase balance and ease of implementation. In this chapter, a novel planar Marchand balun using re-entrant coupled lines is presented.

6.1. INTRODUCTION TO CONVENTIONAL PLANAR MARCHAND BALUN



(a) Circuit configuration

(b) Corresponding symmetrical four-port network for even- and odd- mode analysis

Figure 6.1: Conventional Marchand balun

The conventional planar Marchand balun consists of two symmetrical $\lambda/4$ coupled lines with open and short circuited terminations at specified ports, as clearly depicted in Figure 6.1 (a). It provides balanced outputs to load terminations (Z_{out}) from unbalanced input impedance (Z_{in}). Note that the impedances Z_{in} and Z_{out} are usually different, meaning that in addition to converting an unbalanced impedance to a balanced impedance, the balun can also perform impedance transformation.

6.1.1. SYMMETRICAL COUPLED LINE CHARACTERISTICS

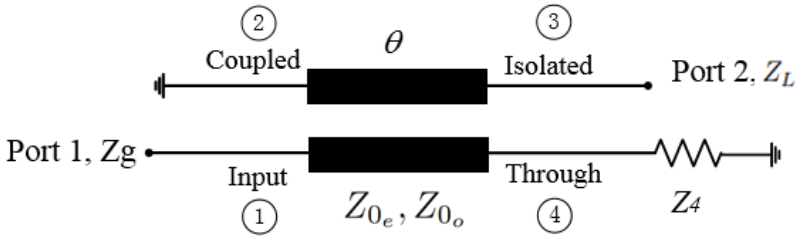


Figure 6.2: Four-port coupled transmission line section reduced to a two-port with the coupled port short-circuited and the through port terminated with load Z_4

Before looking into the even- and odd-mode circuits, it is instructive to have a understanding of the coupled line section, which as implicitly depicted in Figure 6.1 is symmetrical in a homogeneous medium. From [44], the impedance matrix for the four-port coupled line section can be derived as

$$Z_{11} = Z_{22} = Z_{33} = Z_{44} = -\frac{j}{2}(Z_{0e} + Z_{0o})\cot\theta \tag{6.1}$$

$$Z_{12} = Z_{21} = Z_{34} = Z_{43} = -\frac{j}{2}(Z_{0e} - Z_{0o})\cot\theta \tag{6.2}$$

$$Z_{13} = Z_{31} = Z_{24} = Z_{42} = -\frac{j}{2}(Z_{0e} - Z_{0o})\csc\theta \tag{6.3}$$

$$Z_{14} = Z_{41} = Z_{23} = Z_{32} = -\frac{j}{2}(Z_{0e} + Z_{0o})\csc\theta \tag{6.4}$$

where Z_{0e} and Z_{0o} represent the even- and odd-mode impedances and θ is the electrical length. In Figure 6.2, the four-port coupled line section is reduced to a two-port network with an open-circuited terminal at the coupled port and an arbitrary impedance Z_4 at through port.

If $Z_4 = \infty$ (open circuit), the corresponding two-port Z'-matrix can be expressed as

$$Z'_{11} = Z_{11} - \frac{Z_{12}Z_{21}}{Z_{22}} \tag{6.5}$$

$$Z'_{12} = Z'_{21} = Z_{13} - \frac{Z_{23}Z_{12}}{Z_{22}} = 0 \tag{6.6}$$

$$Z'_{22} = Z_{33} - \frac{Z_{23}Z_{32}}{Z_{22}} \tag{6.7}$$

In this specific case Z'_{12}=Z'_{21}=0, which means a perfect transmission stop ($T = 0$) that is frequency independent for all values of θ.
If $Z_4 = 0$ (short circuit), the corresponding two-port Z'-matrix can be given as

$$Z'_{11} = Z'_{22} = Z_{11} + \frac{-Z_{11}(Z_{12}^2 + Z_{14}^2) + 2Z_{12}Z_{13}Z_{14}}{Z_{11}^2 - Z_{13}^2} \tag{6.8}$$

$$Z'_{12} = Z'_{12} = Z_{13} + \frac{Z_{13}(Z_{12}^2 + Z_{14}^2) - 2Z_{11}Z_{12}Z_{14}}{Z_{11}^2 - Z_{13}^2} \tag{6.9}$$

Finally, the input impedance for this two-port network(Figure 6.2) can be calculated as

$$Z_{IN} = Z'_{11} - \frac{Z'_{12}Z'_{21}}{Z'_{22} + Z_L} \tag{6.10}$$

6.1.2. EVEN- AND ODD- MODE ANALYSIS

With the port assignments defined in Figure 6.1, the ideal balun behaviour can be described using S-parameters:

$$S_{21} = -S_{31} \tag{6.11}$$

$$S_{11} = 0 \tag{6.12}$$

To analyse the Marchand balun configuration, the well-known even- and odd-mode analysis method is ultilised. With this method, the balun can be seen as a symmetric four-port network where the open-circuited terminal is replaced by a load Z_{in}, as shown in Figure 6.1 (b). This facilitates the decomposition of the network into even- and odd-mode circuits as depicted in Fig 6.3 (a) and (b), respectively. According to [62], Equation 6.12 and 6.11 will be satisfied when the transmission and reflection coefficients in the even- and odd-mode circuits are given as follows. To satisfy Equation 6.11

$$\frac{T_{even}(1 - \Gamma_{odd}\Gamma)}{2 - \Gamma(\Gamma_{even} + \Gamma_{odd})} = 0 \tag{6.13}$$

$$\frac{\Gamma_{even} + \Gamma_{odd} - 2\Gamma_{even}\Gamma_{odd}\Gamma}{2 - \Gamma(\Gamma_{even} + \Gamma_{odd})} = 0 \tag{6.14}$$

Where Γ_{even} and Γ_{odd} are the input reflection coefficients of the even- and odd-mode circuits, while T_{even} and T_{odd} are the transmission coefficients. Γ is the reflection coefficient

of port 4. Provided the denominators in Equation 6.13 are not zero, we have

$$T_{even} = 0 \tag{6.15}$$

For the conventional Marchand balun, port 4 is open circuited, meaning that $\Gamma = 1$, thus Equation 6.14 can be expressed in terms of Z_{even}, Z_{odd} and Z_{in} as

$$Z_{even} + Z_{odd} = 2Z_{in} \tag{6.16}$$

where Z_{even} and Z_{odd} are the impedances seen into the even and odd mode circuits, respectively. From Equation (6.15), it can be concluded that to achieve perfect amplitude and phase balance, the balun has to present a transmission stop in the even-mode circuit. In addition, Equation (6.16) shows that, to achieve perfect matching at the balun input in the open-circuit case, the sum of the even-and odd-mode impedances must be twice of the input impedance.

The even-mode circuit of the conventional Marchand balun is shown in Figure 6.3 (a), where the through port is open-circuited (Z_4=0). From the previous discussion, this topology indeed provides a frequency-independent transmission stop. Therefore, condition (6.15) is fulfilled and perfect amplitude and phase balance is achieved at all frequencies. By combining Equation (6.1), (6.2),(6.5), (6.6), (6.7) and (6.10) the resulting even-mode impedance at center frequency ($\theta = 90°$) can be calculated as

$$Z_{even} = Z'_{11} = -\frac{j(Z_+^2 - Z_-^2)}{2Z_+}\cot\theta = 0 \tag{6.17}$$

with the notation $Z_+ = Z_{0e} + Z_{0o}$,$Z_- = Z_{0e} - Z_{0o}$.

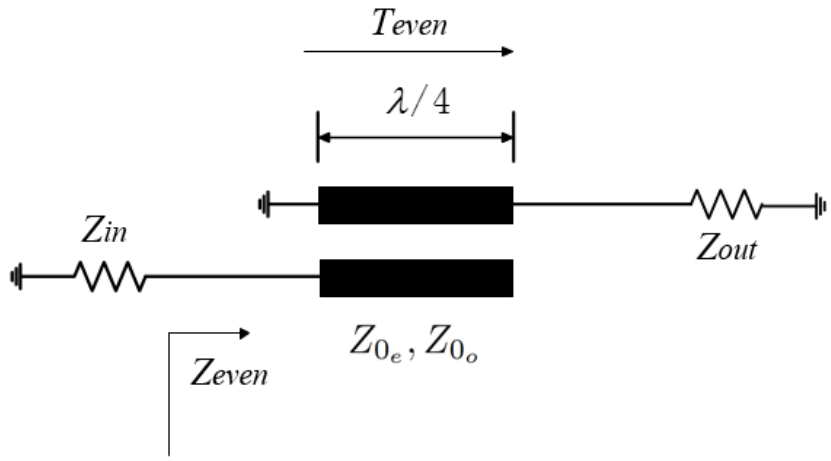
Figure 6.3(b) presents the corresponding odd-mode circuits, where the through port is short-circuited ($Z_4 = 0$). From Equation (6.1), (6.2),(6.3), (6.4), (6.8), (6.9) and (6.10), the odd-mode impedance at center frequency ($\theta = 90°$) can be calculated as

$$Z_{odd} = \frac{(Z_+^2 - Z_-^2)^2}{4Z_-^2 Z_{out}} \tag{6.18}$$

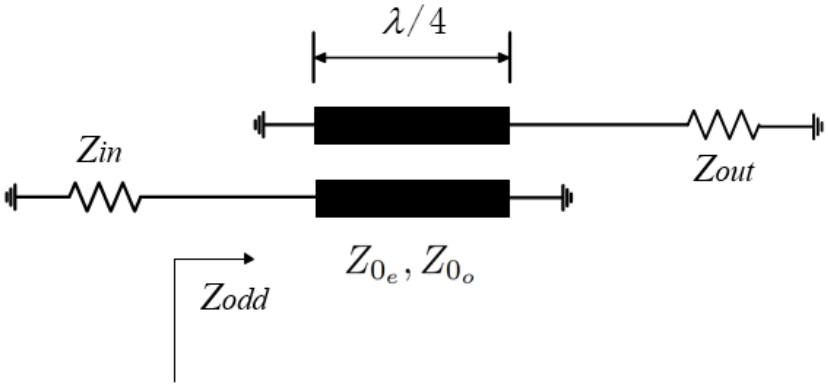
By inserting Equation (6.17) and (6.18) into (6.16), we can obtain

$$\frac{(Z_+^2 - Z_-^2)^2}{4Z_-^2 Z_{out}}\cos\theta = 2Z_{in} \tag{6.19}$$

Thus, in order to achieve perfect matching at the input of the balun, the even- and odd-



(a) Even-mode



(b) Odd-mode

Figure 6.3: (a) Even-mode circuit and (b) odd-mode circuit of the conventional Marchand balun in Figure 6.1

mode impedance should satisfy the following condition

$$\frac{Z_{0e}^2 Z_{0o}^2}{(Z_{0e}-Z_{0o})^2} = \frac{Z_{in}Z_{out}}{2} \tag{6.20}$$

With $Y_{0e} = 1/Z_{0e}$, $Y_{0o} = 1/Z_{0o}$, $Y_{in} = 1/Z_{in}$ and $Y_{out} = 1/Z_{out}$, the condition can also be espressed as

$$Y_{0o} - Y_{0e} = \sqrt{2 \cdot Y_{in}Y_{out}} \tag{6.21}$$

Based on Equation (6.21), the desired relation between Z_{0e} and Z_{0o} for different combinations of the input and output port impedances Z_{in} and Z_{out} is plotted in Figure 6.4. It should be noted that for a given set of balun impedances at the input and output port, there exist infinite solutions of even- and odd-mode impedances Z_{0e} and Z_{0o} to satisfy Equation (6.21). For example, when $Z_{in} = 50\Omega, Z_{out} = 25\Omega$, the corresponding odd-mode

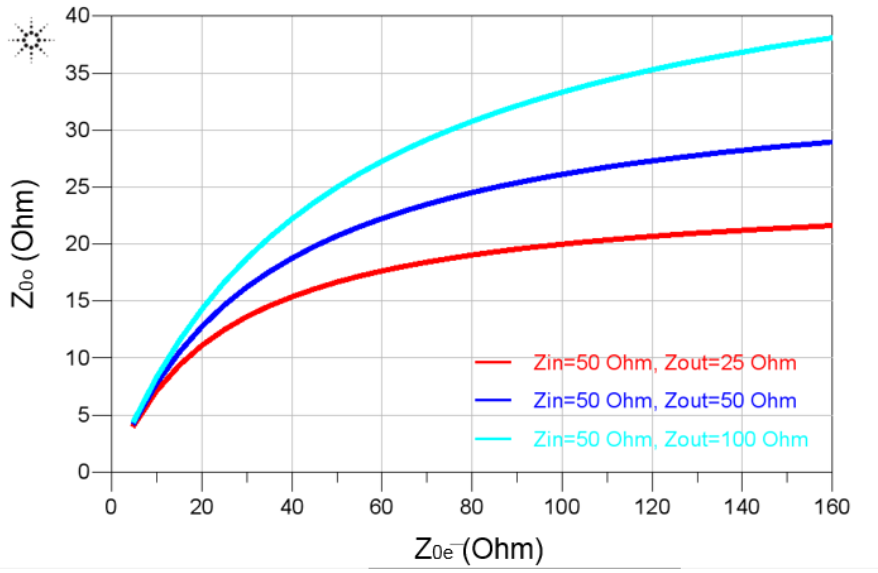


Figure 6.4: Solution of odd-mode impedance (Z_{0o}) versus even-mode impedance (Z_{0e}) for different combinations of unbalanced and balanced port impedances

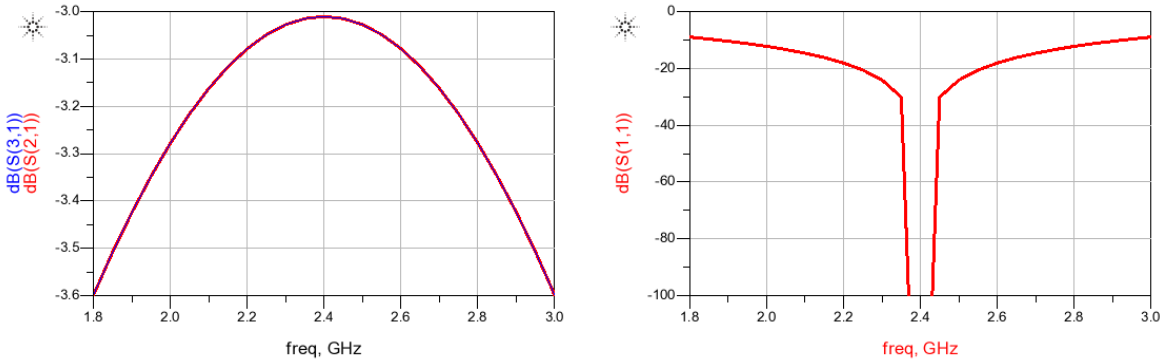


Figure 6.5: Simulated S-parameter for the conventional Marchand Balun when $Z_{in} = 50\Omega$, $Z_{out} = 25\Omega$

impedance Z_{0o} for $Z_{0e} = 100\Omega$ is 20Ω. The simulated S-parameters for this case are plotted in Figure 6.5, indicating a perfect match between the two balanced ports and an impedance match at the input port. Figure 6.6 presents the simulated $|S21|$ for different combinations of even-mode and odd-mode impedances with the port definition in Figure 6.1 (a) when $Z_{in} = Z_{out} = 50\Omega$. It can be observed that a larger even-mode impedance (or a larger coupling factor $k = Z_{0e}/Z_{0o}$ will result in a wider bandwidth. Thus for the implementation of a broadband Marchand balun, a tight coupling with high even-mode impedance is in need.

6.2. COUPLED LINE CONFIGURATION

A planar marchand balun tends to employ microstrip lines, striplines, coplanar waveguides to implement the coupled line section. The single-layer edge-coupled microstrip (see Fig-

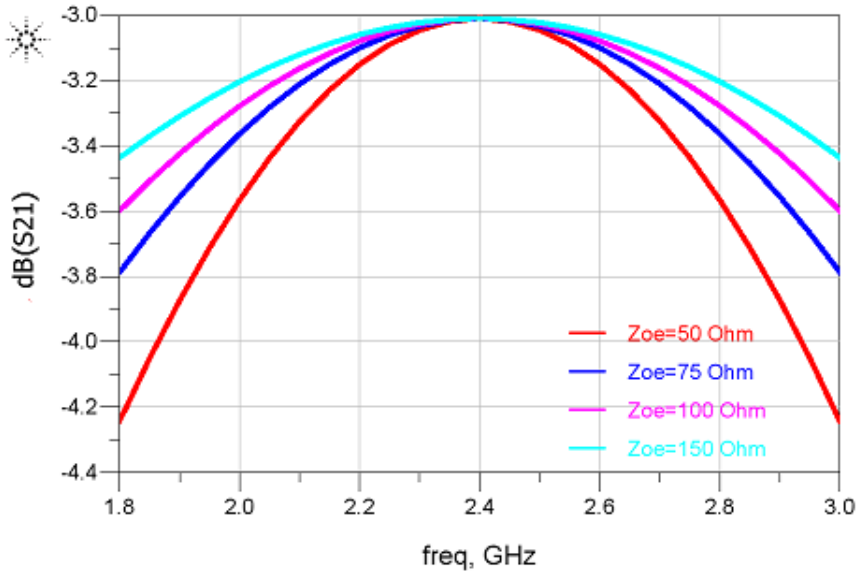
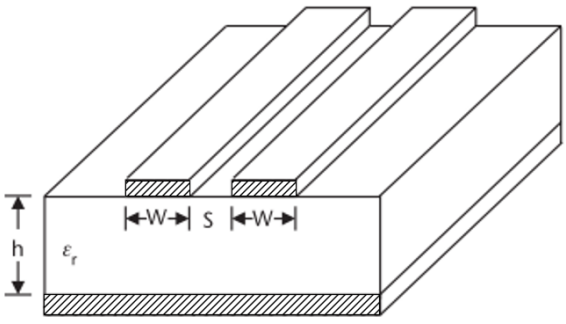
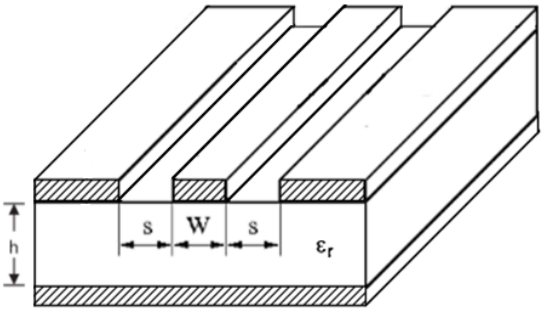


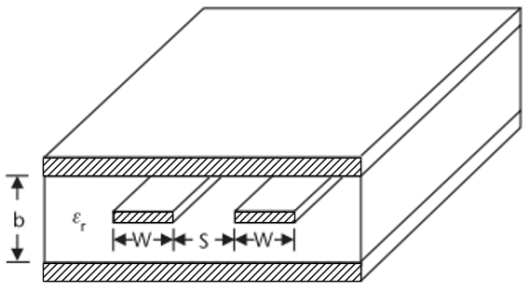
Figure 6.6: Simulated $|S21|$ for different combinations of even-mode and odd-mode impedances



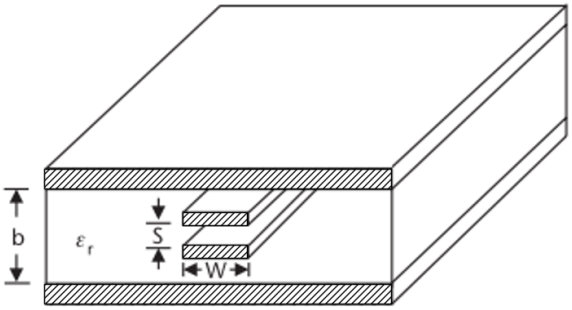
(a) Edge-coupled Microstrip lines



(b) Coplanar Waveguide



(c) Edge-coupled striplines



(d) Broadside-coupled striplines

Figure 6.7: Coupled Line Structures

ure 6.7(a))and coplanar waveguide (see Figure 6.7(b)) are easier to fabricate, but it's difficult to obtain a strong coupling because of the limits on gap fabrication. Multilayered edge-coupled (see Figure 6.7(c) or broadside-coupled lines (see Figure 6.7(d), on the other contrary, has the potential to achieve tight coupling, but they are high in cost or complex in structure. Therefore, it will be very benefiAcial if baluns can be implemented using simple microstrip couple lines. The re-entrant mode coupled lines, which were first described by S. B. Cohn in [64], have been used to resolve these problems and to achieve tight coupling without strict requirements in circuit fabrications.

6.2.1. BASIC CONCEPT OF RE-ENTRANT COUPLED LINES

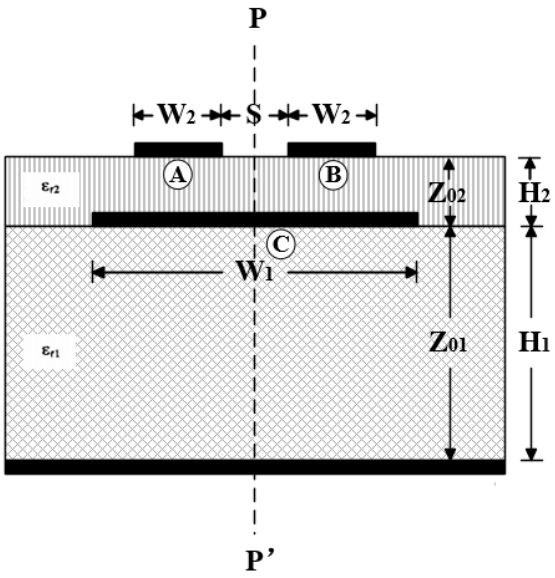
Figure 6.8 (a) presents a general re-entrant type coupled line configuration. It is also a multilayer configuration that consists of three conductors in which two conductors (conductors A and B) are deposited on the top surface of a two-layered dielectric substrate and a third conductor (conductors C) that is floating is sandwiched between the two dielectric layers. With proper dielectric constant and reasonable dielectric layer thickness between conductors A-C (or B-C) and C-ground, the expected tight coupling coefficient can be achieved.

The basic concept [59] of this re-entrant type coupled lines presented in Figure 6.8 (a) can be explained in terms of even- and odd-mode by placing a magnetic and an electric walls at the plane of symmetry P–P', respectively. In the case of even-mode excitation, the symmetry plane P–P' acts as a magnetic wall (open circuit) and bisects the coupler's cross section as shown in Figure 6.8 (b). Since the width of conductor C becomes half of its original value, the effective characteristic impedance of conductor C with respect to ground doubles. It should be noted that there are two different propagation modes for the even-mode excitation, one exists between transmission lines A–C (or B-C) (having characteristic impedance of Z_{02}), the other one exists between the floating conductor C and ground (having characteristic impedance of $2Z_{01}$). The even-mode impedance, which can be assumed as the series connection between these two modes, can be expressed as

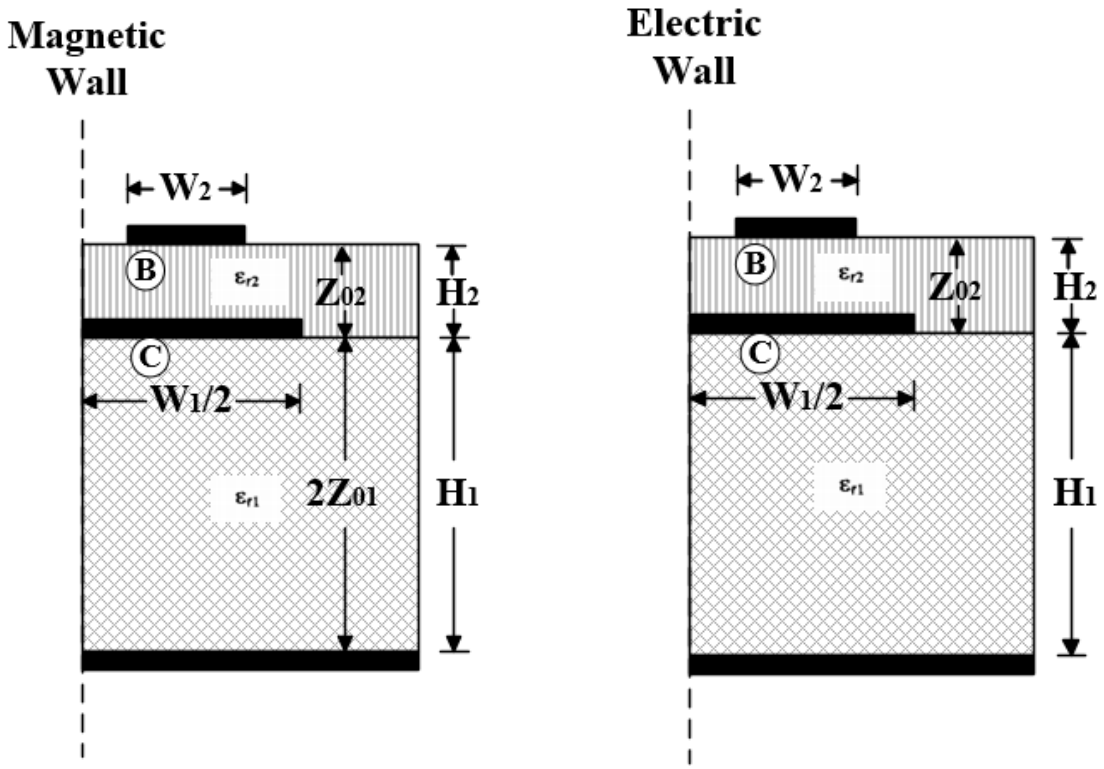
$$Z_{0e} = Z_{02} + 2Z_{01} \tag{6.22}$$

However, in the case of odd-mode excitation, the symmetry plane behaves as an electric wall (short circuit). The floating conductor C works like a virtual ground and the odd-mode signal only exists between transmission lines A–C (or B-C). Then the odd-mode impedance of the coupled structure is given by

$$Z_{0o} = Z_{02} \tag{6.23}$$



(a) Edge-coupled Microstrip lines



(b) Even-mode

(c) Odd-mode

Figure 6.8: (a) Microstrip re-entrant mode coupler cross section (b) Even- and odd-mode excitations [59]

Therefore, the coupling coefficient and the termination impedance in this case can be cal-

culated as

$$k = \frac{Z_{0e} - Z_{0o}}{Z_{0e} + Z_{0o}} = \frac{Z_{01}}{Z_{01} + Z_{02}} = \frac{1}{1 + Z_{02}/Z_{01}} \tag{6.24}$$

$$Z_0 = \sqrt{Z_{0e} Z_{0o}} \tag{6.25}$$

It can be observed from Equation (6.24) that the coupling coefficient of the re-entrant type coupled lines mostly depends on the Z_{02}/Z_{01} ratio rather than the spacing between the conductors A and B, thus relaxing the dimensional requirements in circuit fabrication. Generally, a small Z_{02}/Z_{01} ratio is prefered for tight coupling coefficient. This can be easily realized by controlling the parameters ε_{r1}, ε_{r2} and H_1, H_2. If the substrate layer between conductor A (B) and C has a larger dielectric constant but a smaller thickness when compared with the the substrate between conductor C and ground ($\varepsilon_{r1} < \varepsilon_{r2}$, $H_1 > H_2$), a strong coupling coefficient can be achieved.

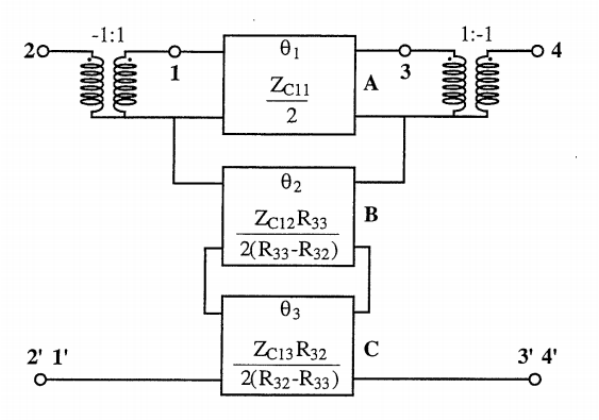
6.2.2. DESIGN AND MODELING OF RE-ENTRANT COUPLED LINES

The planar re-entrant type coupled lines (see Figure 6.8)(a) can be modeled as presented in Figure 6.9(a) according to [65]. In the equivalent circuit, transmission line section A corresponds to the "odd" mode, where the voltages at the two top conductors are out of phase ($R_{21} = -1$) and the middle conductor works as a virtual ground ($R_{21} = 0$). The other two transmission line sections B and C correspond to "even" modes where the voltages at the two top conductors are equal ($R_{22} = R_{23} = 1$). In one of these two "even" modes (say mode B), all the three conductors retain almost equal potential , meaning that ($R_{32} = 1$) while in the other "even" mode (mode C), the middle conductor has much lower potential ($R_{32} << 1$) [65]. Obviously, the two "even" modes of the three coupled lines in the re-entrant type coupler are connected in series. If these two "even" modes put together, this equivalent circuit for planar re-entrant type couplers in Figure 6.8(a) can be compared with the equivalent circuit for symmetrical two coupled lines shown in Figure 6.8(b) [65].

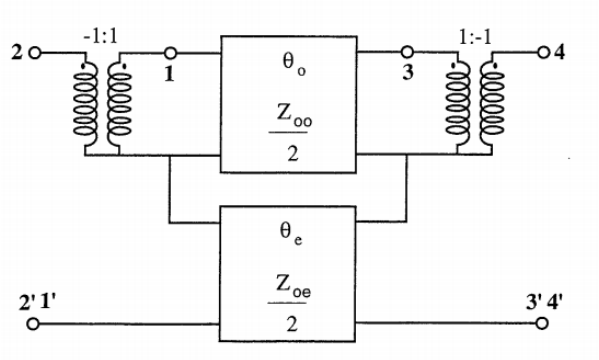
Multilayer re-entrant coupled line configuration makes use of broadside coupling thus allowing much greater freedom in terms of size requirements, but it adds up difficulties to design because a multilayer structure is inhomogeneous in character and there are no simple design expressions available for determining the physical dimensions. However, based on the network model in Figure 6.8, the design procedure can be summarized as follows [65]:

1. Calculate the even- (Z_{0e}) and odd- (Z_{0o}) mode impedances for a corresponding symmetrical two-line coupler according to the specified coupling coefficient and termination impedance.

2. Since $Z_{02} = Z_{0o}$, calculate the physical dimensions of the top-layer structure such as ε_{r2}, H_2 and W_2 by assuming a large separation S between the two conductors A and B.



(a) Re-entrant type three-coupled lines



(b) Symmetrical two-coupled lines

Figure 6.9: Equivalent network model for (a)Re-entrant type three-coupled lines and (b) Symmetrical two-coupled lines [65]

3. Calculate Z_{01} by $Z_{01} = (Z_{0e} - Z_{02})/2$ and determine the physical dimensions of the bottom-layer structure such as ε_{r1}, H_1 and W_1.
4. Optimize the coupler in terms of the structure's physical dimensions by fine-tuning the above calculated dimensions using EM simulators.

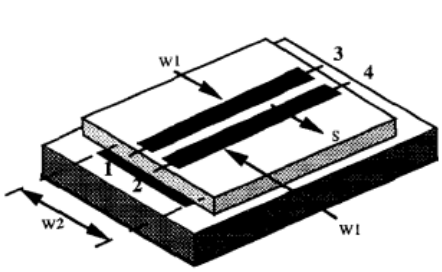
As an example, the substrate is designed with $\varepsilon_{r1} = 3, \varepsilon_{r2} = 10.2$, $H_1 = 0.13mm, H_2 = 0.75mm$, $W_1 = 3.2mm$ and $W_2 = 1.5mm$. The electrical length can be adjusted by the physical length of conductors. Figure 6.10 (a) shows the layout for the re-entrant coupled line while Figure 6.10 (b) gives the equivalent model (CLINP) used in ADS for schematic-level simulations. Io order to extract the parameters Z_{0o} and Z_{0e} and θ_e (K_e, even-mode effective dielectricity) and θ_o (K_o, odd-mode effective dielectricity) for the component CLINP, S-parameter of this four-port network is used. The resulting parameters values are listed in Table 6.1.

Figure 6.11 plots the S-parameter comparisons between the layout (using FEM for calcu-

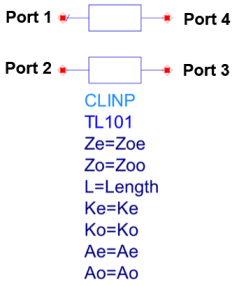
Table 6.1: Parameter values in the equivalent model as shown Figure 6.10(b) when $\varepsilon_{r1} = 3, \varepsilon_{r2} = 10.2$, $H_1 = 0.13mm, H_2 = 0.75mm$, $W_1 = 3.2mm$ and $W_2 = 1.5mm$.

Z_{0e}	Z_{0o}	K_e	K_o
70.73	7.28	3.35	8.85

lation) and its equivalent schematic-level replacement CLINP. In the frequency range from 2.0 GHz to 2.8 GHz, the differences between the two simulation results are always smaller than 0.1 dB, thus it is feasible to model this re-entrant coupled line with the component CLINP to simplify the design.



(a) Re-entrant coupled line layout



(b) Re-entrant coupled line schematic model

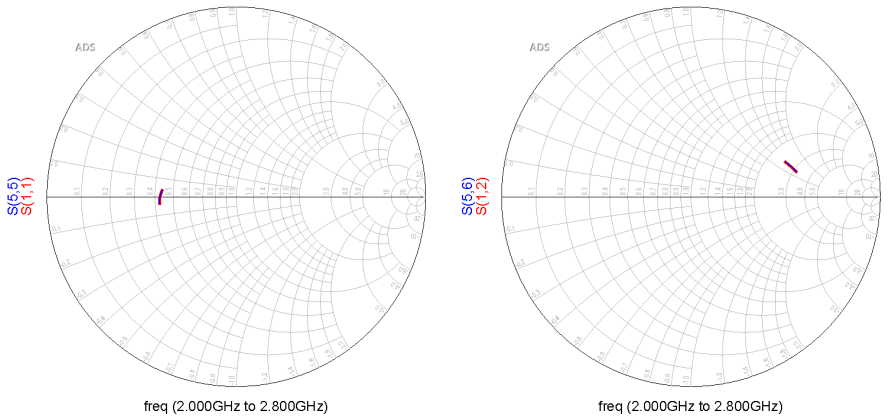
Figure 6.10: (a)layout and (b)schematic model of the re-entrant typed coupled lines

6.3. MARCHAND BALUN USING RE-ENTRANT COUPLED LINES

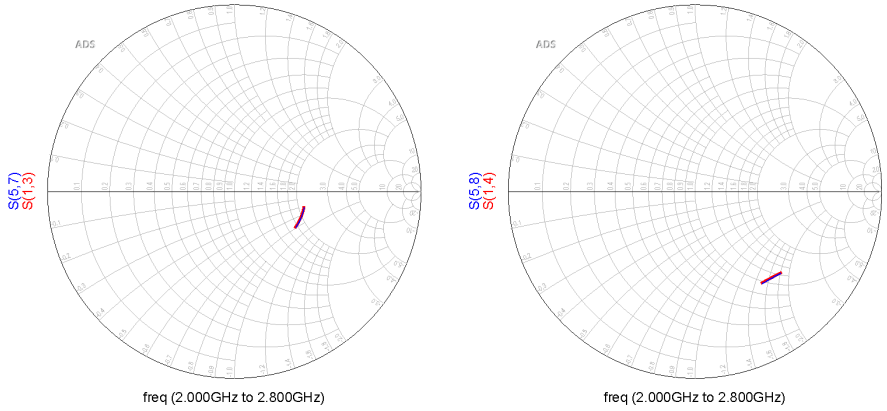
From the discussion in the previous section, we know that the re-entrant type coupled lines can provide tight coupling without stringent dimensional requirements in circuit fabrication. However, directly employing the coupled lines in the Marchand balun will lead to imperfect conversion from the unbalanced signal into the balanced signal because of the unequal even- and odd- phase velocities. To address this issue, a compensation technique [66] is adopted to improve the imbalance of the Marchand balun. A detailed discussion of the ideal balun condition in the case of a compensated Marchand balun is performed in this work.

6.3.1. BASIC PRINCIPLES

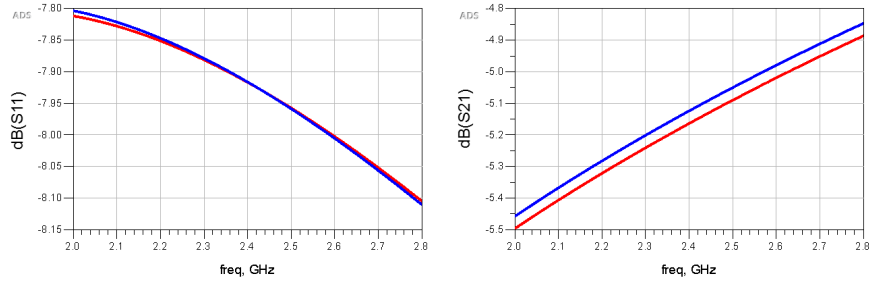
Figure 6.12 (b) plots the structure of the proposed balun composed by two re-entrant type coupled lines and an extra compensation transmission line, where θ_e and θ_o are the even- and odd-mode electrical lengths of the coupled lines, Z_{0e} and Z_{0o} are the even- and odd-mode characteristic impedances of the coupled lines and θ_c and Z_c are the electrical length and the characteristic impedances of the compensation line. The corresponding symmetrical four-port network is shown in Figure 6.13(a), which facilitates the decomposition of the network into even-mode (see Figure 6.13 (b)) and odd-mode half circuits (see Figure



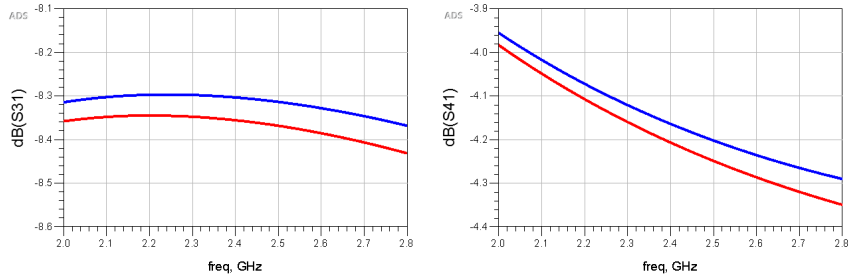
(a)



(b)



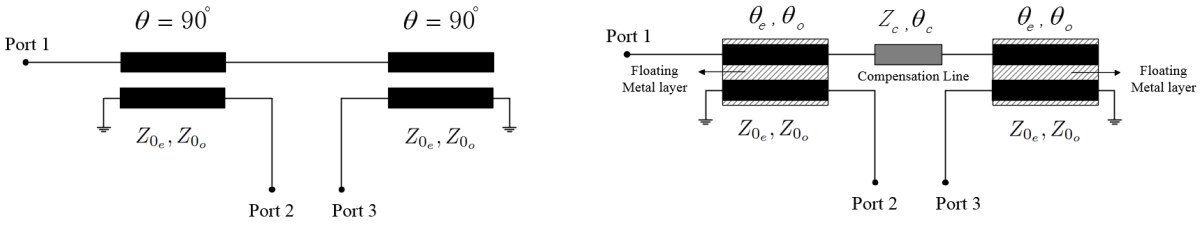
(c)



(d)

Figure 6.11: Comparisons of S-parameter between the re-entrant coupled line and its equivalent model

6.13 (c)).



(a) the conventional Marchand balun

(b) the proposed Marchand balun consisting of two re-entrant coupled line sections with compensation

Figure 6.12: Configurations of (a) the conventional Marchand balun and (b) the proposed Marchand balun consisting of two re-entrant coupled line sections with compensation.

In the following discussion, the re-entrant type coupler is approximately equivalent to a symmetrical two-line coupler in an inhomogeneous medium. Thus the impedance matrix for the four-port open-circuited coupled lines in terms of the even- and odd-mode impedances Z_{0e} and Z_{0o} and even- and odd-mode electrical lengths θ_e and θ_o can be expressed as

$$Z_{11} = Z_{22} = Z_{33} = Z_{44} = -\frac{j}{2}(Z_{0e}\cot\theta_e + Z_{0o}\cot\theta_o) \tag{6.26}$$

$$Z_{12} = Z_{21} = Z_{34} = Z_{43} = -\frac{j}{2}(Z_{0e}\cot\theta_e - Z_{0o}\cot\theta_o) \tag{6.27}$$

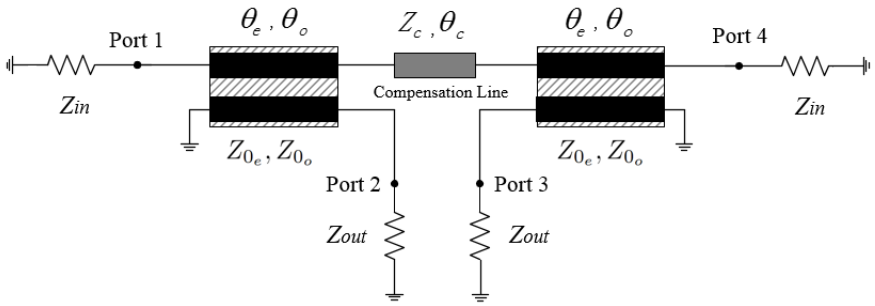
$$Z_{13} = Z_{31} = Z_{24} = Z_{42} = -\frac{j}{2}(Z_{0e}\csc\theta_e - Z_{0o}\csc\theta_o) \tag{6.28}$$

$$Z_{14} = Z_{41} = Z_{23} = Z_{32} = -\frac{j}{2}(Z_{0e}\csc\theta_e + Z_{0o}\csc\theta_o) \tag{6.29}$$

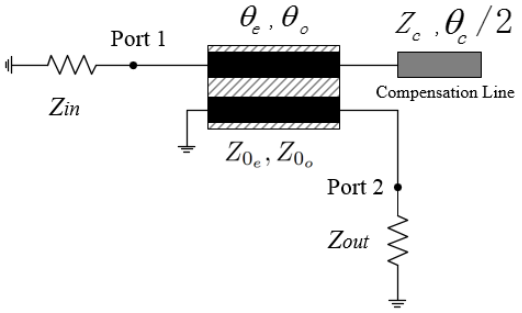
As discussed before, the requirement of balanced balun behavior with the port definition shown in Figure 6.12 (b) is given by $T_{even} = 0$. This condition in the even mode circuits can be expressed as $Z_1 2^{even} = 0$. Figure 6.13 (b) presents the even mode circuit of the modified Marchand balun . According to [44], the two-port Z-parameters for a coupled line section loaded at the coupled and through port with short circuit and Z_4 respectively is derived as

$$Z'_{11} = Z_{11} + \frac{-Z_{11}(Z_{12}^2 + Z_{14}^2) + 2Z_{12}Z_{13}Z_{14} - Z_4 Z_{12}^2}{Z_{11}(Z_{11} + Z_4) - Z_{13}^2} \tag{6.30}$$

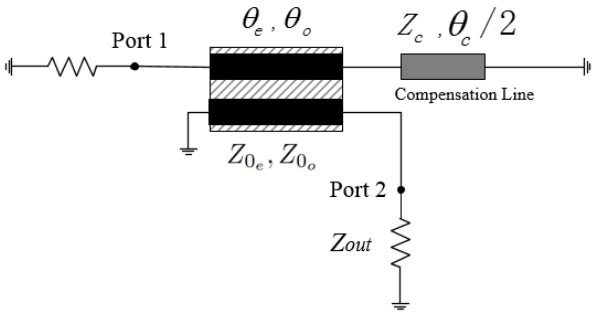
$$Z'_{12} = Z'_{21} = Z_{13} + \frac{Z_{13}(Z_{12}^2 + Z_{14}^2) - 2Z_{11}Z_{12}Z_{14} - Z_4 Z_{12}Z_{14}}{Z_{11}(Z_{11} + Z_4) - Z_{13}^2} \tag{6.31}$$



(a) Symmetrical four-port Network for the proposed Marchand balun



(b) Even-mode



(c) Odd-mode

Figure 6.13: Circuit schematic of (a)Symmetrical four-port Network for the proposed Marchand balun (b) Even-mode (c)Odd-mode.

$$Z'_{22} = Z_{11} + \frac{-Z_{11}(Z_{12}^2 + Z_{14}^2) + 2Z_{12}Z_{13}Z_{14} - Z_4 Z_{14}^2}{Z_{11}(Z_{11} + Z_4) - Z_{13}^2} \tag{6.32}$$

The requirement of perfect amplitude and phase balance is fulfilled if $Z'_{12} = Z'_{21} = 0$, which from Equation (6.31) can be satisfied with

$$Z_4 = \frac{Z_{13}(-Z_{11}^2 - Z_{12}^2 + Z_{13}^2 - Z_{14}^2) + 2Z_{11}Z_{12}Z_{14}}{Z_{11}Z_{13} - Z_{12}Z_{14}} \tag{6.33}$$

Substituting Equation (6.26), (6.27), (6.28) and (6.29) into Equation (6.33), we can get

$$Z_4 = \frac{Z_{0o}\csc\theta_e - Z_{0e}\csc\theta_o}{\csc\theta_e\cot\theta_o - \csc\theta_o\cot\theta_e} \tag{6.34}$$

Note that in this case, Z_4 is realized by an open-terminated transmission line with the characteristic impedance equal to Z_c and the electrical length equal to $\theta_c/2$. It can be calculated by $Z_4 = Z_c\cot(\frac{\theta_c}{2})$. Consequently, the balanced condition of the proposed Marchand balun can be expressed as

$$Z_{cm}\cot(\frac{\theta_{cm}}{2}) = \frac{Z_{0o}\csc\theta_e - Z_{0e}\csc\theta_o}{\csc\theta_e\cot\theta_o - \csc\theta_o\cot\theta_e} \tag{6.35}$$

If $\theta_e = \theta_o$ (meaning that the phase velocities for even-mode and odd-mode are equal), there is no imbalance in this balun network, which is in agreement with the conclusion for the conventional Marchand balun in the previous subsection. If $\theta_e \neq \theta_o$ (meaning that the phase velocities for even-mode is different from that of odd-mode), the balun is not balanced at all and the imbalance (the right-hand of Equation (6.35)) can be assumed as a function of the parameters of the coupled lines Z_{0e}, Z_{0o}, θ_e, θ_o. The left-hand of Equation (6.35) is influenced by the parameters of the compensation transmission line Z_{cm}, θ_{cm}. When the parameters of the coupled lines are determined, there are infinite solutions of compensation line parameters Z_{cm} and E_{cm} to satisfy the balanced equation. For instance, the coupled line section are decided as $Z_{0e} = 100\Omega$, $Z_{0o} = 7.5\Omega$, $\theta_e = 49°$, $\theta_o = 90°$, thus the left-side of Equation (6.35) equals 102.8 Ω. The relationship between the electrical length (E_c) and the characteristic impedance (Z_c) of the compensation line in this situation is plotted in Figure 6.14. With this figure, the designers can easily choose the suitable solution according to reality(die area and layout rule).

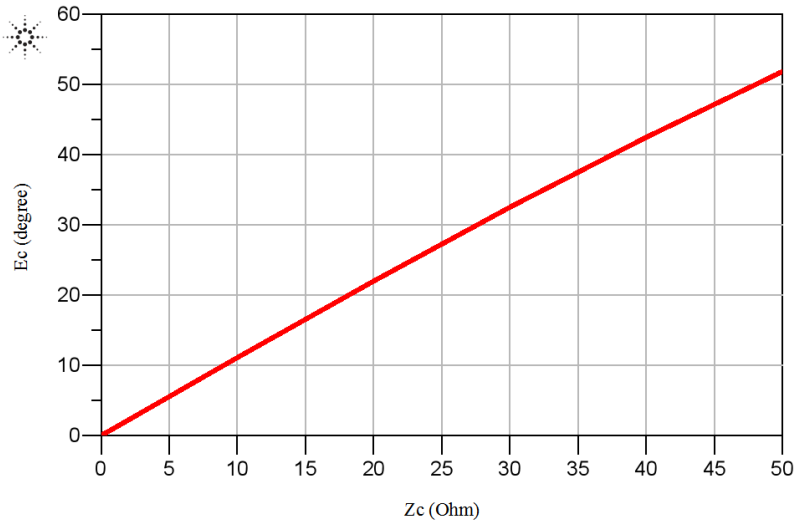


Figure 6.14: The electrical length E_c Vs characteristic impedance Z_c of the compensation line when $Z_{com} = 102.8\Omega$

Another requirement for an ideal balun is $Z_{even} + Z_{odd} = 2 \cdot Z_{in}^*$ to ensure an impedance match at the input port. For the even-mode schematic (see Figure 6.13(b)), we have $Z'_{12} = Z'_{21} = 0$, thus the even-mode impedance is given by

$$Z_{even} = Z'_{11}\Big|_{Z_4 = -jZ_c\cot(\theta_c/2)} \tag{6.36}$$

The calculation of odd-mode impedance is more complex. First, we need to obtain the

2-port Z-matrix Z'_{11}, Z'_{12}, Z'_{21}, Z'_{22} under the condition that $Z_4 = jZ_c\tan(\theta_c/2)$. Then the corresonding odd-mode impedance can be calculated according to Equation (6.10).

$$Z_{odd} = Z'_{11} + \frac{Z'_{12}Z'_{21}}{Z'_{22} + Z_{out}}\Big|_{Z_4 = jZ_c\tan(\theta_c/2)} \tag{6.37}$$

$$Z_{even} + Z_{odd} = 2 \cdot Z^*_{in} \tag{6.38}$$

By solving Equation (6.38), the relation of the input and output impedance can be figured out in terms of the coupled line parameters such as Z_{0e}, Z_{0o}, θ_e, θ_o, L_{cp} and compensation line parameters, namely Z_{cm} and E_{cm}, which can help designers to choose the suitable solution for input impedance match.

6.3.2. DESIGN PROCEDURE AND EXAMPLES

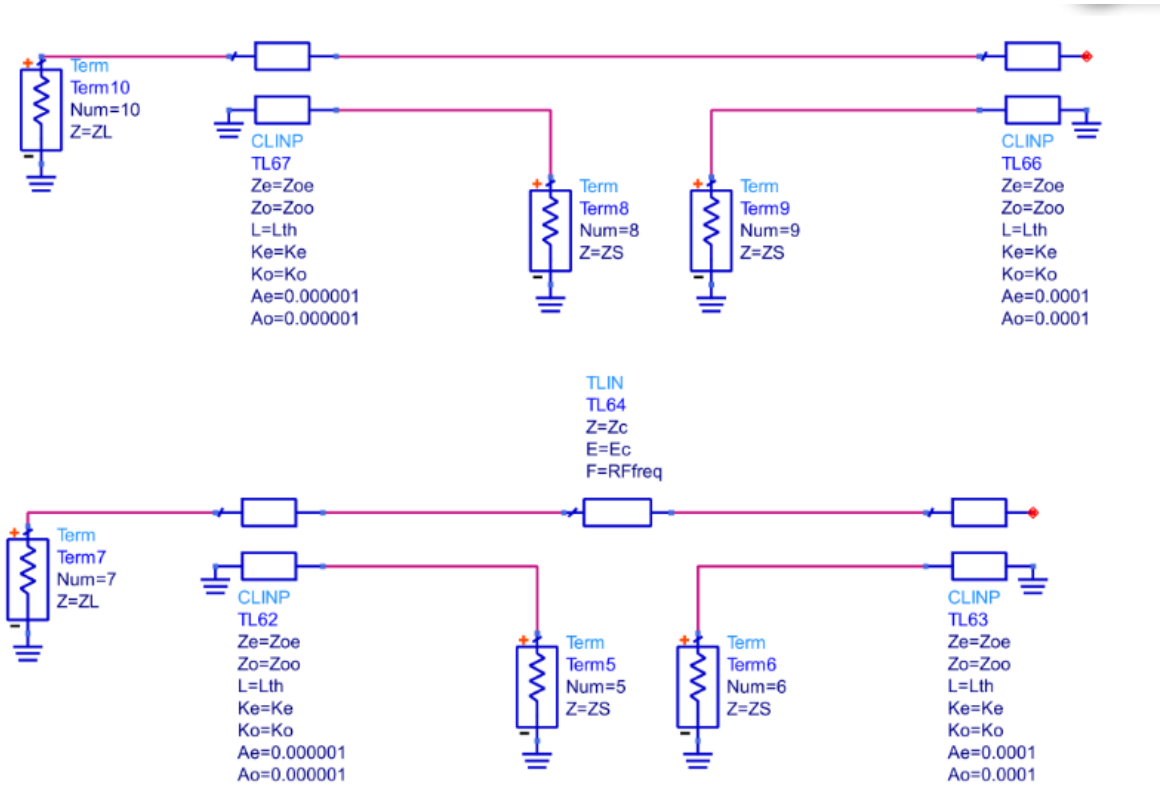


Figure 6.15: Schematic of the conventional Marchand balun (Top) and the proposed compensated one (Bottom)

Figure 6.15 presents the schematic for the compensated Marchand balun and the one without the compensation line. Based on a study of the ideal balun condition in the proposed compensated Marchand balun, a general design procesure is developed as follow.

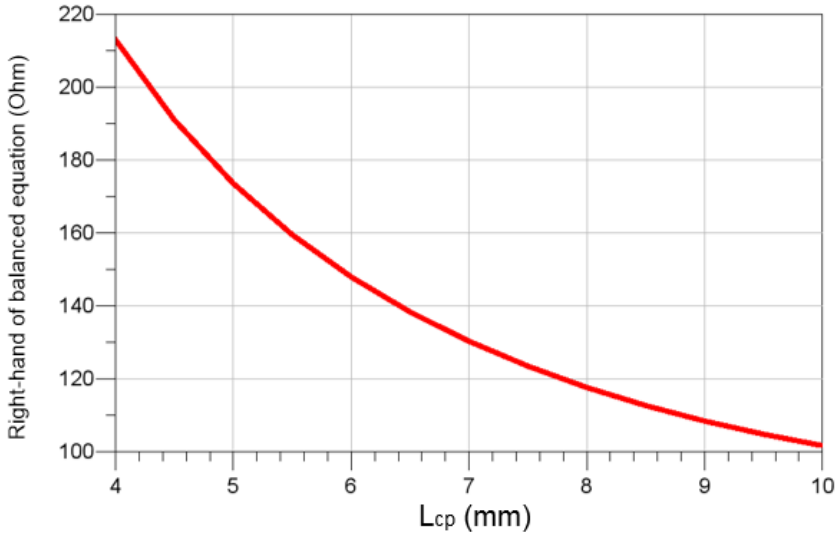


Figure 6.16: Z_{com} Vs the physical length of the coupled line section

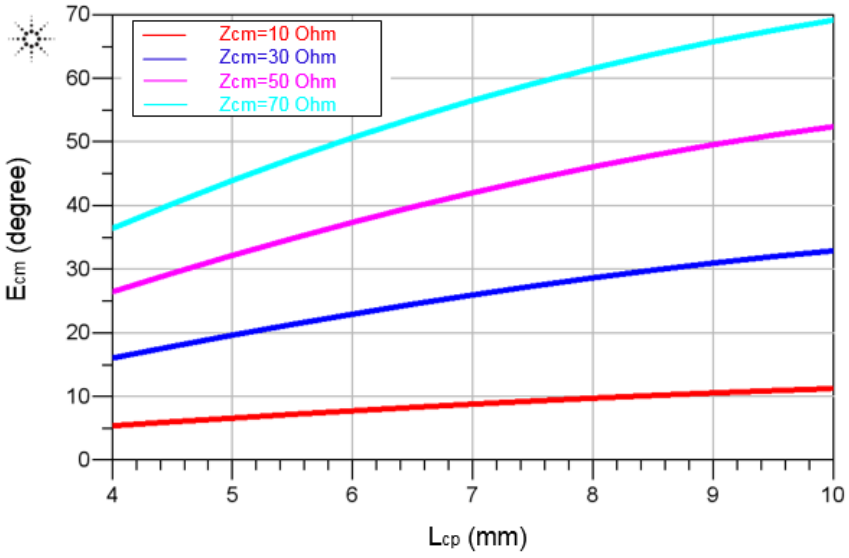


Figure 6.17: The electrical length of the compensated line E_{cm} versus the physical length of the coupled line section L_{cm} with different characteristic impedance Z_c from 10 Ohm to 70 Ohm

The first step to design the compensated Marchand balun is to determine Z_{0e}, Z_{0o}, K_e, and K_o of the coupled lines. This can be done by adjusting the parameters including ε_{r1}, H_1, W_1 and ε_{r2}, H_2, W_2 as described in the section 6.2. If $Z_{0e} = 100\Omega$, $Z_{0o} = 7.5\Omega$ and $K_e = 3$, $K_o = 10.2$, the right-hand of Equation (6.35) will be influenced only by the physical length of the coupled lines L_{cp}, as shown in Figure 6.16. The left-hand of Equation (6.35), however, is a function of compensation line parameters (Z_{cm} and E_{cm}). Figure 6.17 illustrates the

relationship between the electrical length of the compensated line E_{cm} versus the physical length of the coupled line section L_{cp} with different characteristic impedance Z_{cm}.

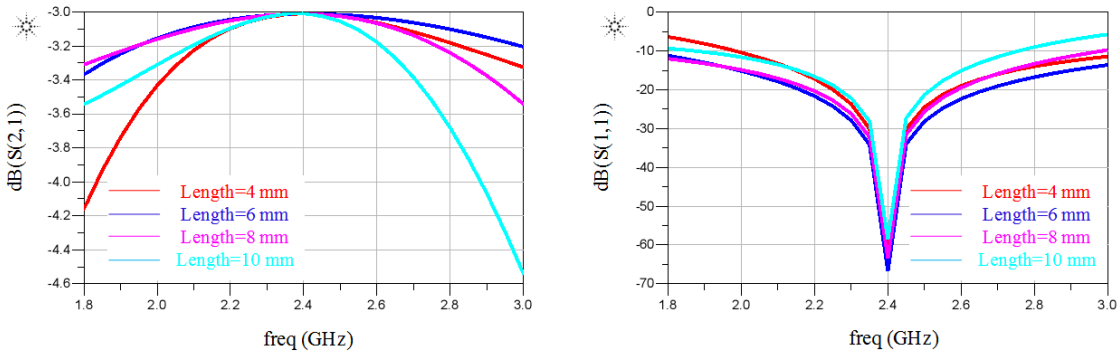


Figure 6.18: Simulated S-parameter of the compensated Marchand balun for different physical length of the coupled line section when Zc is determined

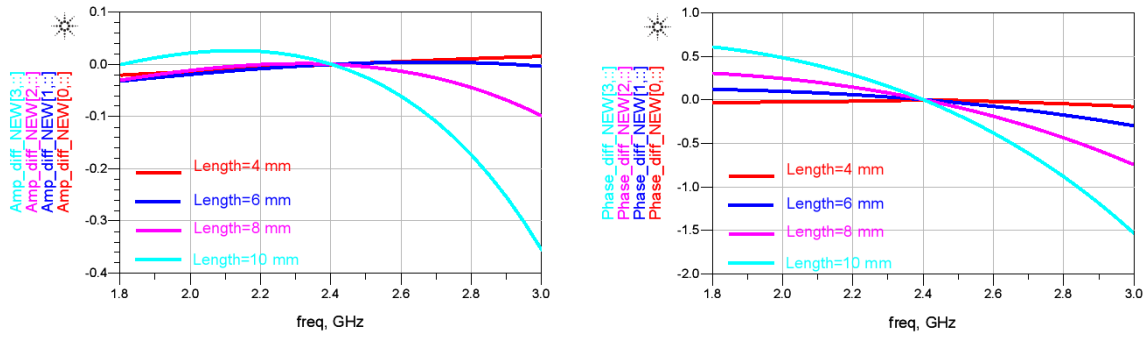


Figure 6.19: Simulated amplitude and phase imbalance of the compensated Marchand balun for different physical length of the coupled line section when Zc is determined

The second step is to determine the physical length of coupled line section (L_{cp}) as well as the compensation line parameters ((E_{cm}) and (Z_{cm})). Consider die area and layout rule to select the suitable width for the compensation line and thus Z_{cm} is determined. Assuming Z_{cm} = 30Ω, the relation between the electrical length of the compensated line versus the physical length of the coupled line section plotted in Figure 6.17. In order to choose from the various solution of coupled line Length and compensation line length, we investigate the wideband S-parameter performance with different coupled line length. As shown in Figure 6.18, the results corresponding to Length=6mm and Length=8mm have wider bandwidths than the other two cases (Length=4mm and Length=10mm). For the ampli-

tude and phase imbalance in Figure 6.19, these two cases (Length=6mm and Length=8mm) show advantage as well. With proper choice of the coupled line physical length (in this situation, Length=7 mm), an optimized wideband performance for the Marchand balun is obtained as shown in Figure 6.20. The resulting amplitude imbalance is within 0.1 dB and the phase imbalance is within 0.5°. In addition, significant improvement can be found in amplitude difference and phase difference compared with the case without the compensation line. Therefore, the proposed compensated Marchand balun employing re-entrant type coupled lines has the potential to realize a broadband balanced balun when the topology parameters are properly determined.

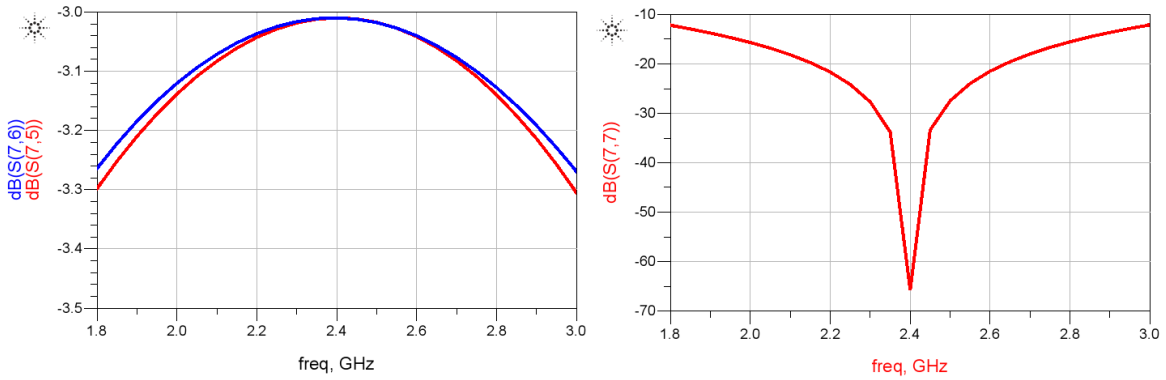


Figure 6.20: Simulated S-parameter of the compensated Marchand balun after optimization

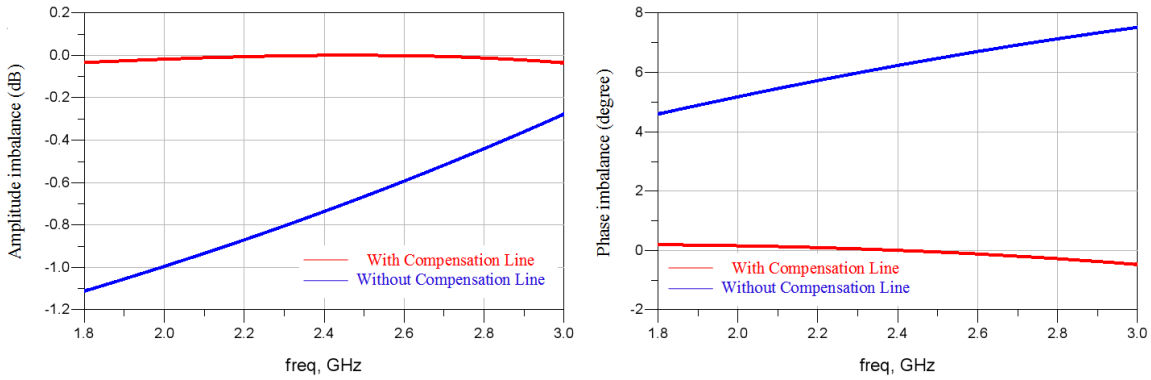


Figure 6.21: Simulated amplitude and phase imbalance of the compensated Marchand balun after optimization

6.3.3. PRACTICAL IMPLEMENTATION

In this part, we begin with a schematic-level design to figure out the design details. Here, the re-entrant type coupled line is designed with $\varepsilon_{r1} = 3, \varepsilon_{r2} = 10.2$, $H_1 = 0.13mm, H_2 =$

$0.75mm$, $W_1 = 3.2mm$ and $W_2 = 1.5mm$. As discussed in Section 6.2.2, we have $Z_{0e} = 70.73$, $Z_{0e} = 7.28$ and $K_e = 3.35$, $K_o = 8.85$. Following the design procesure described in Section 6.3.2, a broadband compensated Marchand balun can be made with the design details in Table 6.2. Figure 6.22 and Figure 6.23 give the simulated S-parameter and the amplitude and phase difference. It can be observed that this schematic-level design does provide a balanced impedance transformation over a wide bandwidth.

Table 6.2: Design details for the compensated Marchand balun as shown Figure 6.10(b) when $\varepsilon_{r1} = 3, \varepsilon_{r2} = 10.2$, $H_1 = 0.13mm, H_2 = 0.75mm$, $W_1 = 3.2mm$ and $W_2 = 1.5mm$.

Z_{0e}	Z_{0o}	K_e	K_o	L_{cp}	E_{cm}	Z_{cm}	Z_S	Z_L
70.73Ω	7.28 Ω	3.35	8.85	6.6 mm	27.2 deg	31Ω	7.5Ω	27.3Ω

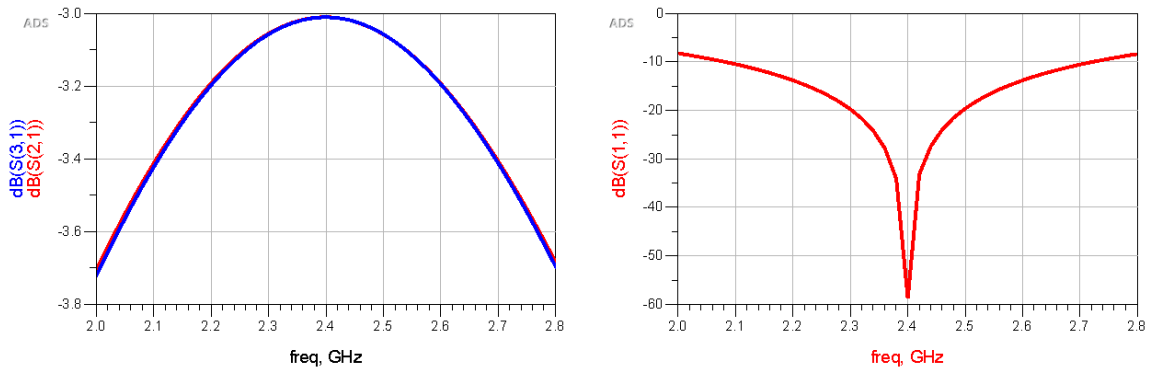


Figure 6.22: Simulated S-parameter of the compensated Marchand balun after optimization

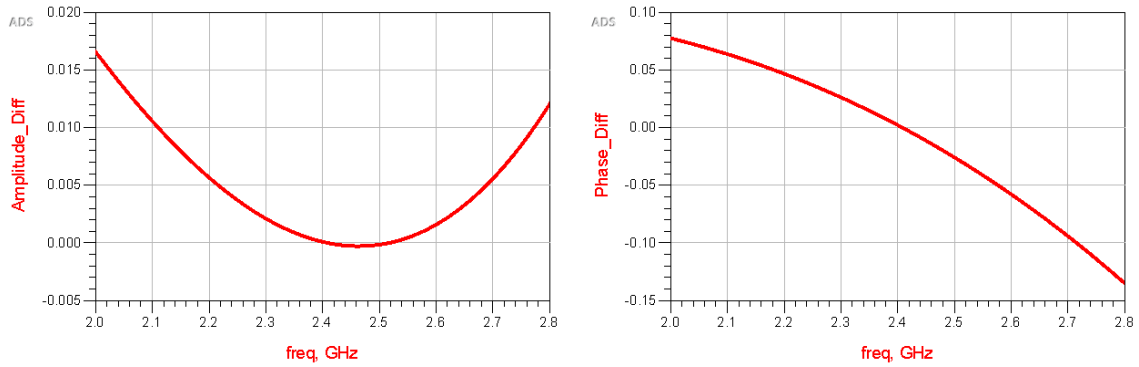


Figure 6.23: Simulated amplitude and phase imbalance of the compensated Marchand balun after optimization

Next we move to the practical design. Since the dimensions for the coupled line section is known, we only need to calculate the size of the compensation line according to Z_{cm} and E_{cm}. The layout of the practical Marchand balun is given in Figure 6.24 with an explaination of the structure. Figure 6.25 shows the simulation setup. Note that a parallel capacitor

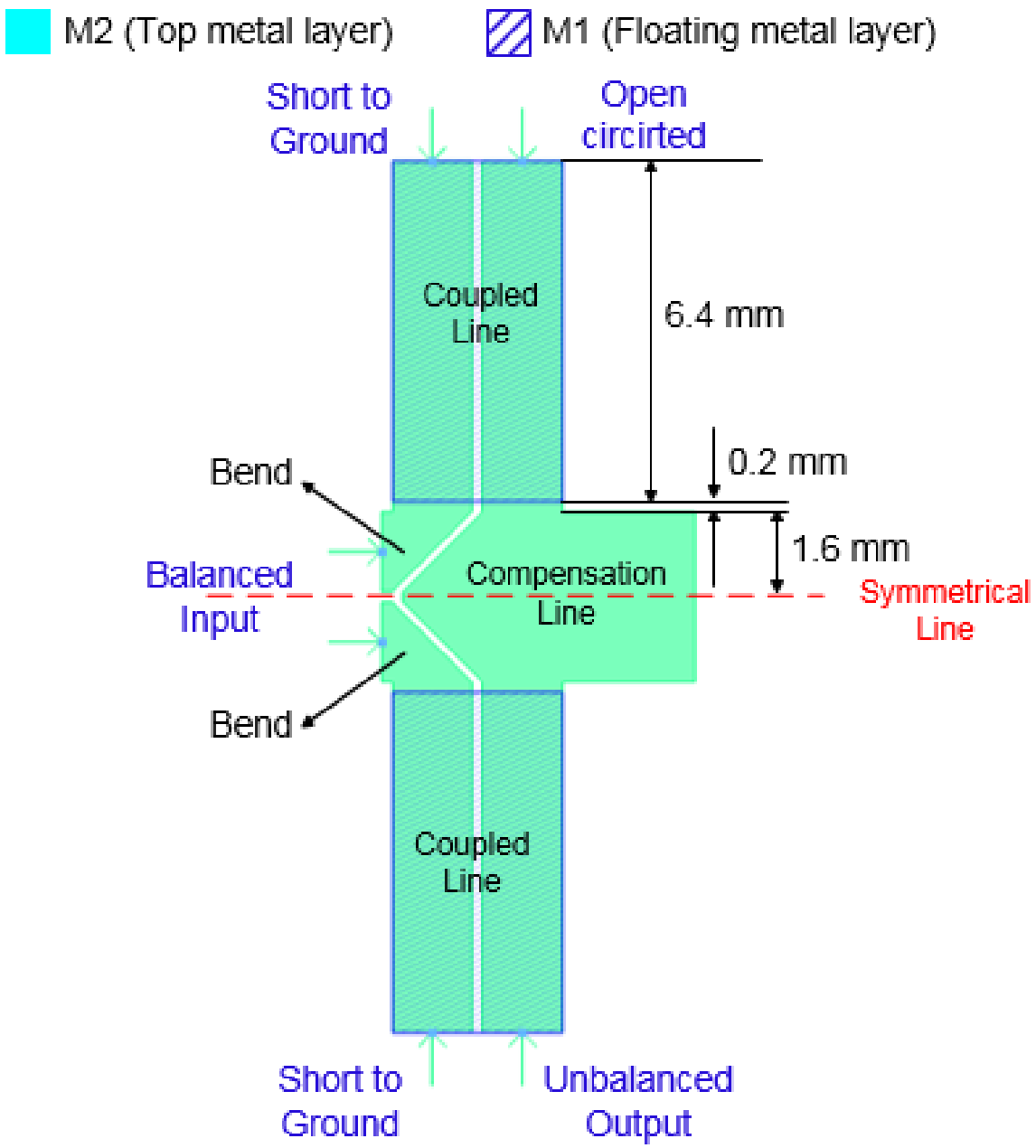


Figure 6.24: Compensated Marchand balun structure

is added between the balanced input ports to compensate for the inductance introduced by the microstrip bend, forming a LC lowpass impedance transformer. In this case, A finite element method (FEM) in ADS is employed for calculating the S-parameter of the Marchand balun at layout-level with ideal ground. The simulated S-parameter is given in Figure 6.26. We can observe that in the frequency range from 2.0 GHz to 2.8 GHz,$|S_{21}|$ and $|S_{31}|$ are better than -4.8dB. In addition, $|S_{11}|$ is better than -6.5 dB with a peaking of -26dB at center frequency 2.4GHz, indicating an excellent input match at port 1. The amplitude and phase

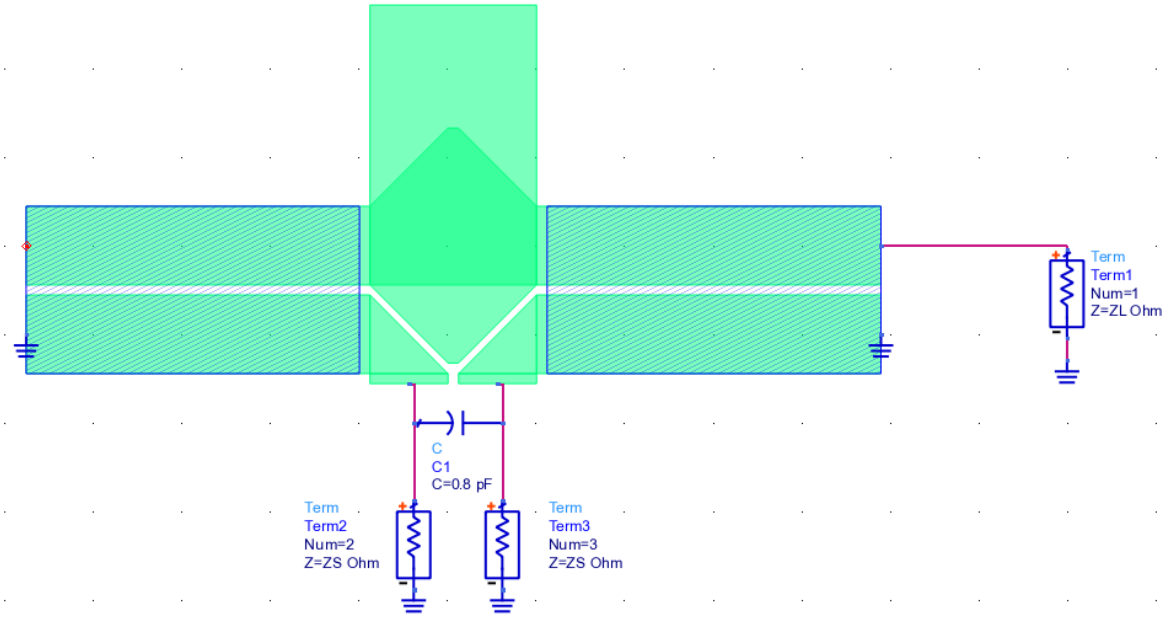


Figure 6.25: S-parameter simulation setup circuit for the practical Marchand balun with ideal ground

difference is depicted in Figure 6.27. Obviously, the amplitude difference is within 0.3dB from 2.0 GHz to 2.8 GHz, meanwhile the phase difference varies from 0.8 deg to 1.2 deg, exhibiting a well-balanced impedance transformation. Thus the compensated Marchand balun employing re-entrant coupled lines is feasible for implementing a balanced and low-loss balun with a large impedance transformation ratio.

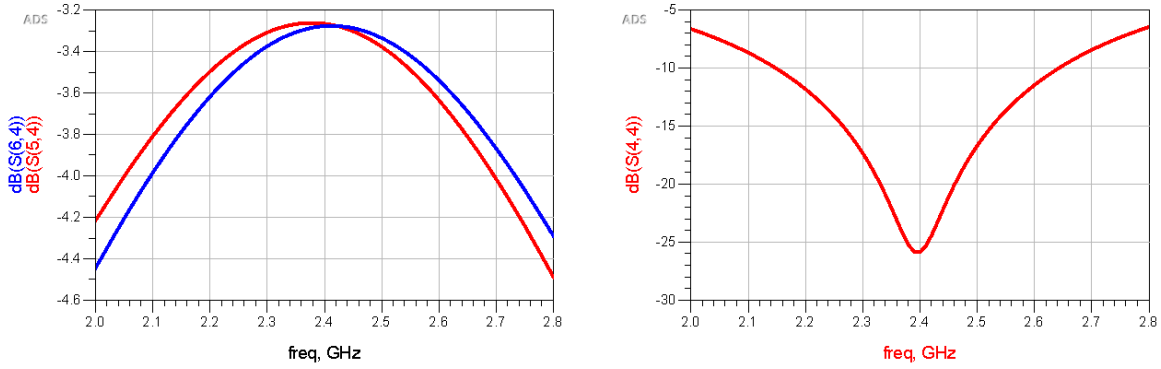


Figure 6.26: Simulated S-parameter of the compensated Marchand balun after optimization

6.4. CONCLUSIONS

In this chapter, a compensated Marchand balun employing re-entrant type coupled lines are discussed. It starts with a study of the conventional Marchand balun. Through analysis, it is shown that a large even-mode and odd-mode impedance ratio (or a tight coupling)

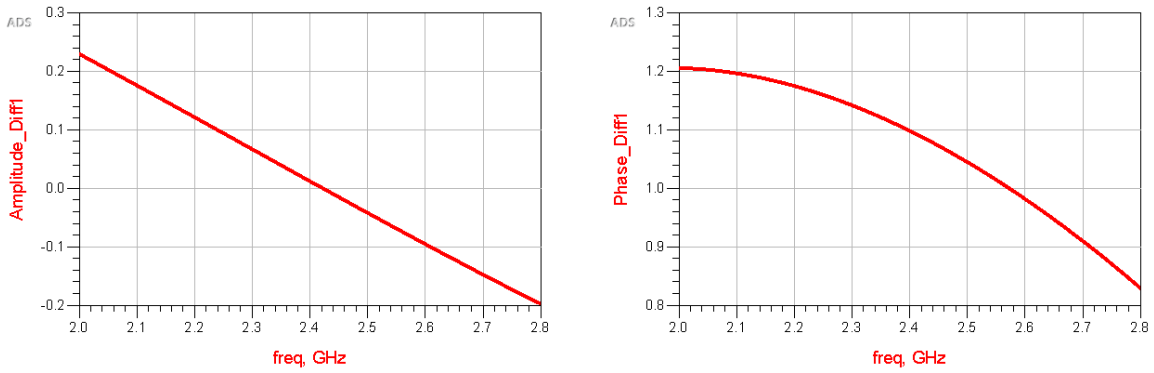


Figure 6.27: Simulated amplitude and phase imbalance of the compensated Marchand balun after optimization

is benefical for a wideband design. Then we investigate different structures of coupled lines. Among them, the re-entrant type coupled lines stand out because of their potential to achieve tight coupling without strict requirements in circuit fabrications. However, the employment of re-entrant type coupled lines introduces new problems due to their unequal even-mode and odd-mode phase velocities. To solve this problem, a compensated Marchand balun is given. Both the theory analysis and simulation results demonstrate that the amplitude and phase differences are greatly improved with a compensation line. Note that the practical design in this chapter ultilise ideal ground to better match the schematic-level design. Non-ideality of ground will be considered in the following chapter when designing the load network for PAs.

7

DIGITALLY-CONTROLLED POWER AMPLIFIER DESIGN CONSIDERATIONS AND EXAMPLES

This chapter provides detailed design and implementation consideration of the digital envelope modulator (on-chip) and the load network (off-chip). It starts with a review of the basic principle behind the proposed digitally-controlled power amplifier and a short study of the utilized 40nm CMOS technology. Following this review, a simplified block diagram of the proposed PA is given. The implementation of the digital envelope modulator, especially the MSB unitcell is explained in details. After the introduction of an equivalent transistor-level modeling of the digital envelope modulator, we investige the digitally-controlled Class E power amplifier configured in a differential topology with ideal and lossless passives to further verify the conclusions in Chapter 3 and to prepare for the practical design. A broadband digitally-controlled Class-E power amplifier is given in the following with emphasis laid on the design of the output matching network where the previously introduced Marchand balun based on re-entrant type coupled lines are applied. Then, a Doherty PA is built on the basis of this Class E power amplifier.

7.1. REVIEW OF THE DIGITALLY-CONTROLLED CLASS E PA

To better understand the design and implementation detailes that will be given in the following, it is instructive to briefly review the operation principle behind the digitally-controlled Class E power amplifier which has been discussed in Chapter 3. Instead of the typical supply voltage modulation, a novel on-resistance modulation is applied in the proposed digital-controlled Class E PA. With reference to Figure 7.1, the thermometer-coded (or unary-coded) amplitude signal u_x is multiplied with the phase modulated RF signal (RF_{in}) in the digital domain, utilizing AND gates. When the control voltages u_x is high, the

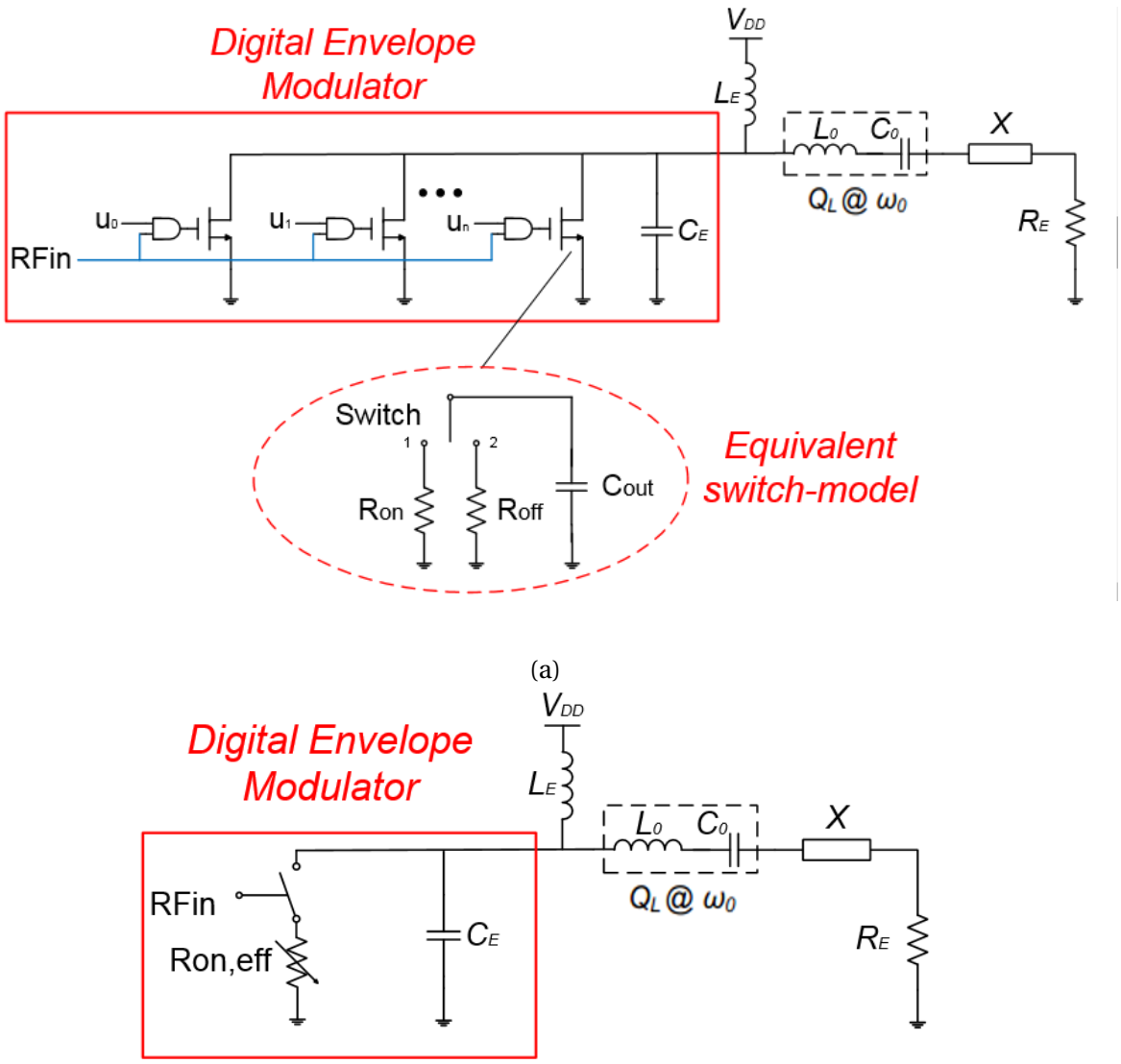
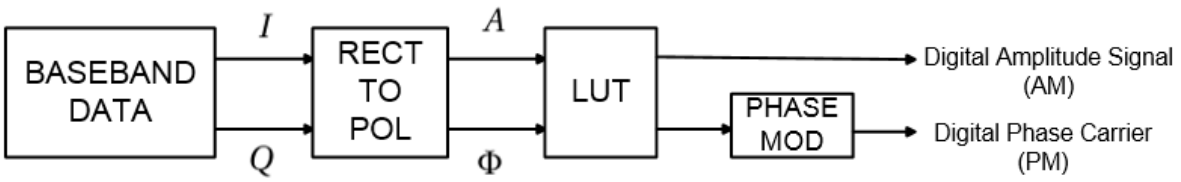


Figure 7.1: Digital Controlled Class E power amplifier
(a) Simplified schematic (b) Conceptual equivalent circuit (switch-model based)

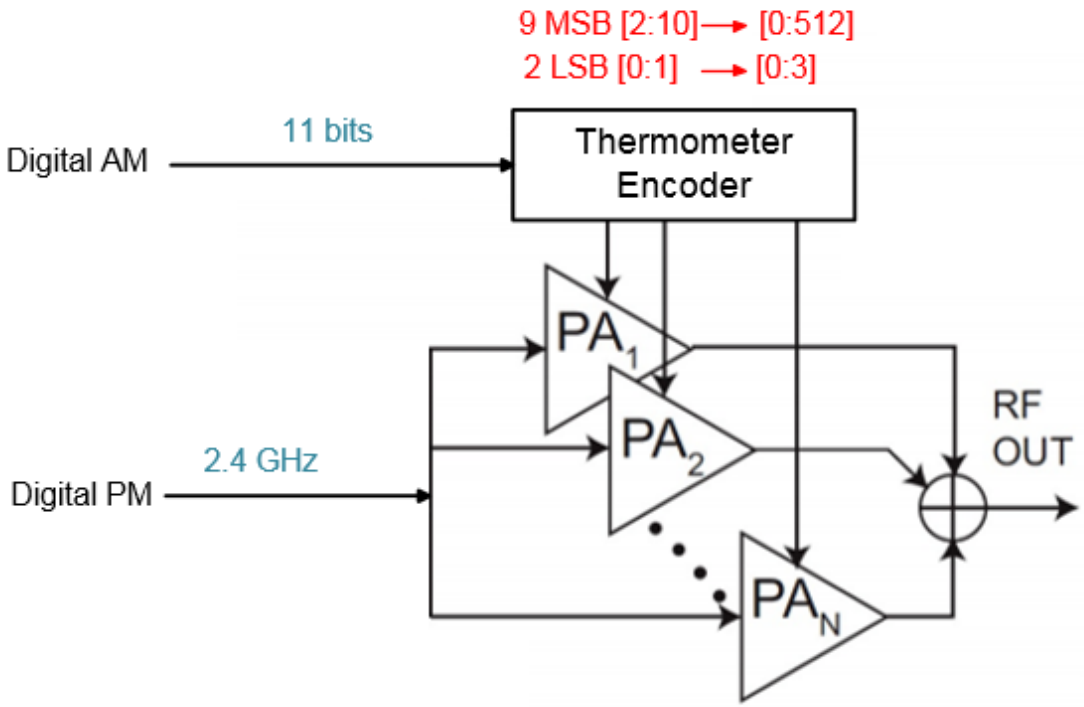
transistor starts to operate in respond to the phase-modulated signal. When the control voltages u_x is low, the gate voltage of the NMOS transistor is forced to be zero, therefore the transistor does not work. With this method, the number of "ON" transistors and the effective on-resistance are varying according to the digital amplitude signal.

Figure 7.1 (b) shows the conceptual model for the digitally-controlled Class E power amplifier where the NMOS transistors are replaced by a resistive switch. This model is ultilised in Chapter 3 for simplicity.

7.2. SYSTEM DESIGN CONSIDERATIONS



(a) Digital AM/PM generation



(b) PA stage

Figure 7.2: Block diagram of a digitally-modulated polar PA.

A block diagram of the complete system developed so far is shown in Figure7.2. It is divided into two parts, one is the generation of the required digital AM and PM signal, the other one is the implementation of the PA stage. In this thesis project, we focus on the implementation of PA stage.

As shown in Figure7.2, the digital envelope modulator is driven by a PM signal and a 11-bit AM signal in digital domain. The 11-bit binary AM signal is converted to thermometer code to properly turn on and off the unit cells (mainly composed of a PA transistor and an AND gate) according to the envelope magnitude. However, the use of the pure thermome-

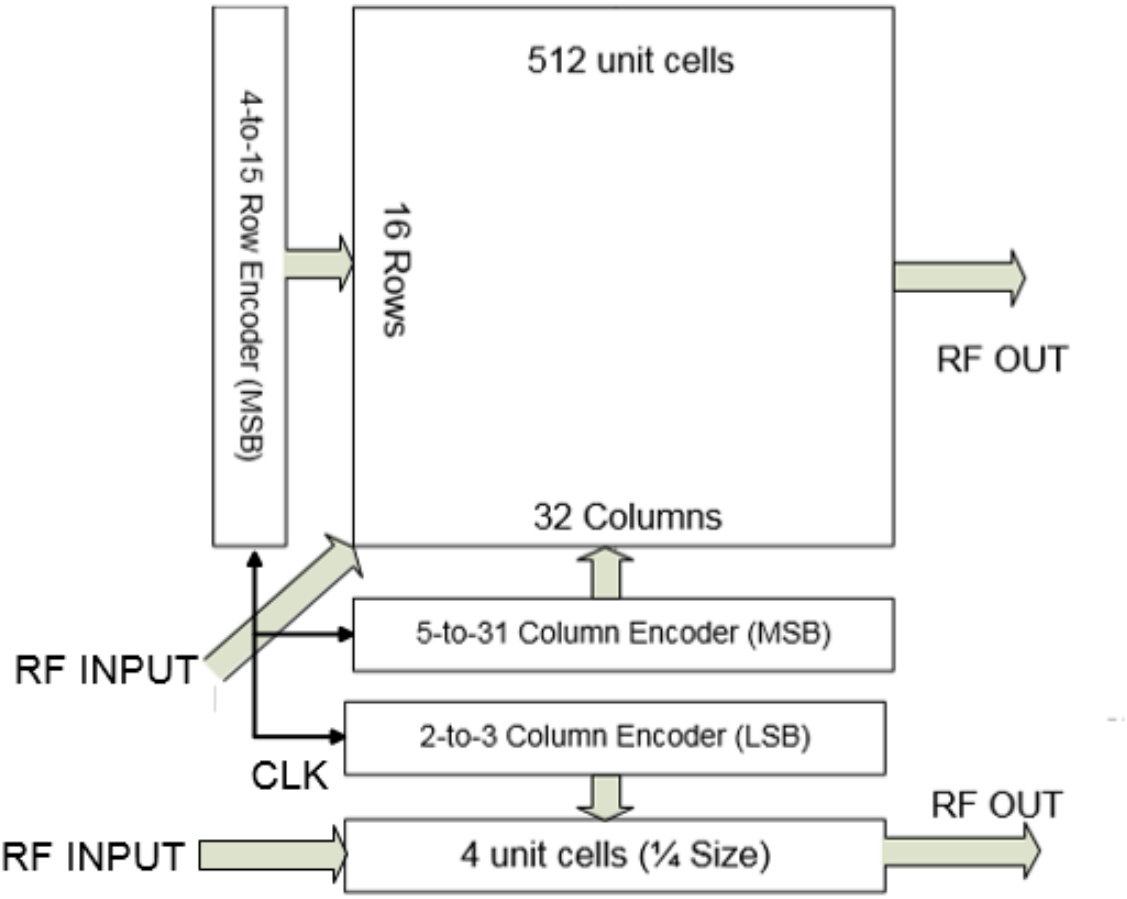
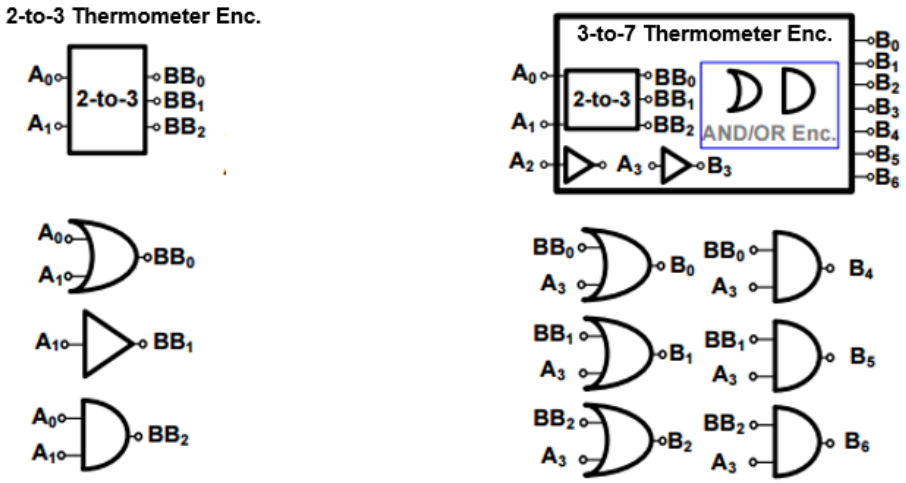


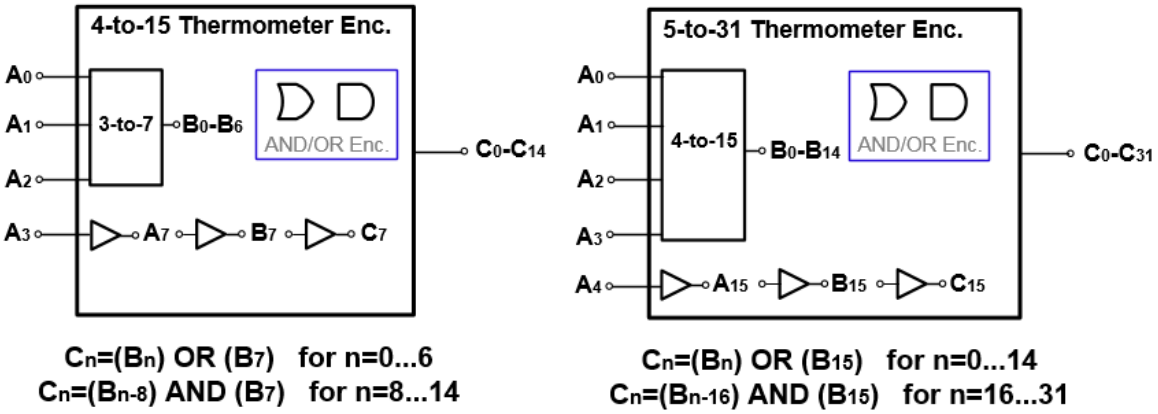
Figure 7.3: 11 bits digitally-modulated PA floorplan

ter code leads to the increase of the complexity of the encoders, the chip area, interconnect parasitics, and power consumption. For this reason, a segmented approach is adopted here.

As shown in Figure 7.3, the segmentation is selected such that 9 bits are used for the MSB and 2 bits for the LSB of the binary input. Thus, the digital PA implementation requires 512 MSB and 4 LSB units. The 512 MSB unit cells further split into 16 rows (4 bits) and 32 columns (5 bits). Based on this arrangement, a 2-3 (for LSB) and a 4-to-15 (for MSB Row) and a 5-to-31(for MSB Column) binary-to-thermometer encoders are employed. And all of them are re-clocked to prevent glitches. The binary-to-ther-mometer decoder is a custom digital circuit, implemented using static CMOS logic, digital buffers as shown in Figure 7.4. The implementation of digital envelope modulator will be given in the following sections.



(a) 2-to-3 and 3-to-7



(b) 4-to-15 and 5-to-31

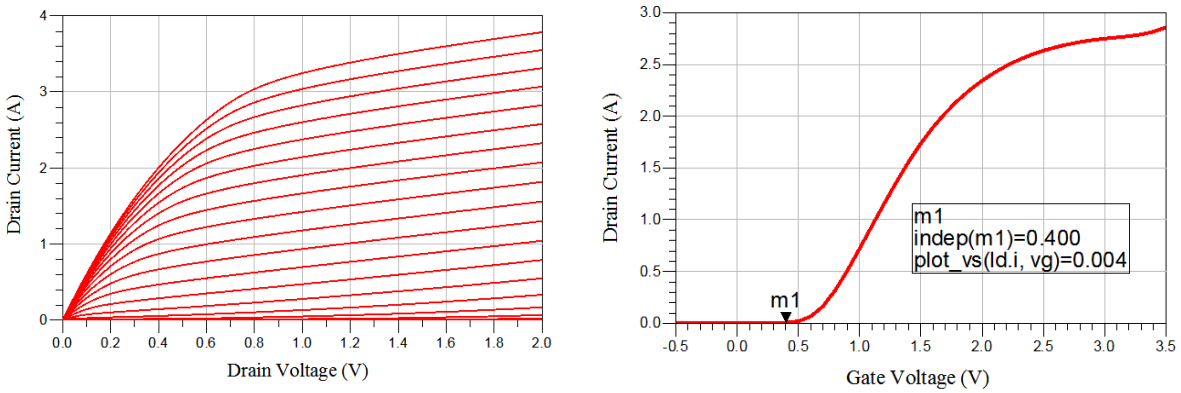
Figure 7.4: Thermometer encoders [32]

7.3. CMOS DEVICE CHARACTERISTICS

Before moving to the implementation details of the digital envelope modulator, it is necessary to look into the characteristics of the CMOS devices in advance. For one thing, transistor sizing in digit circuits are related to the input power and chip area. For another, transistor technology parameters, such as the ON-resistance, OFF-resistance, and the total output capacitance seen into drain node, are of great importance for a Class E power amplifier design.

In this project, the standard 1.1V thin-oxide transistor from TSMC 40nm low-power CMOS technology is employed. The technology is optimized for low power consumption of

digital circuits. By importing the 40nm NMOS transistor model in Cadence Spectre to ADS, we can simulate of the characteristics of the devices in ADS. The simulation setup is shown in Figure 7.6. First, we look into the DC transfer characteristic of this device. As shown in Figure 7.5, the threshold voltage is about 0.4V when V_{ds}=0.6V.



(a) Output characteristic (b) DC transfer characteristic

Figure 7.5: DC characteristic of TSMC 40nm NMOS transistor

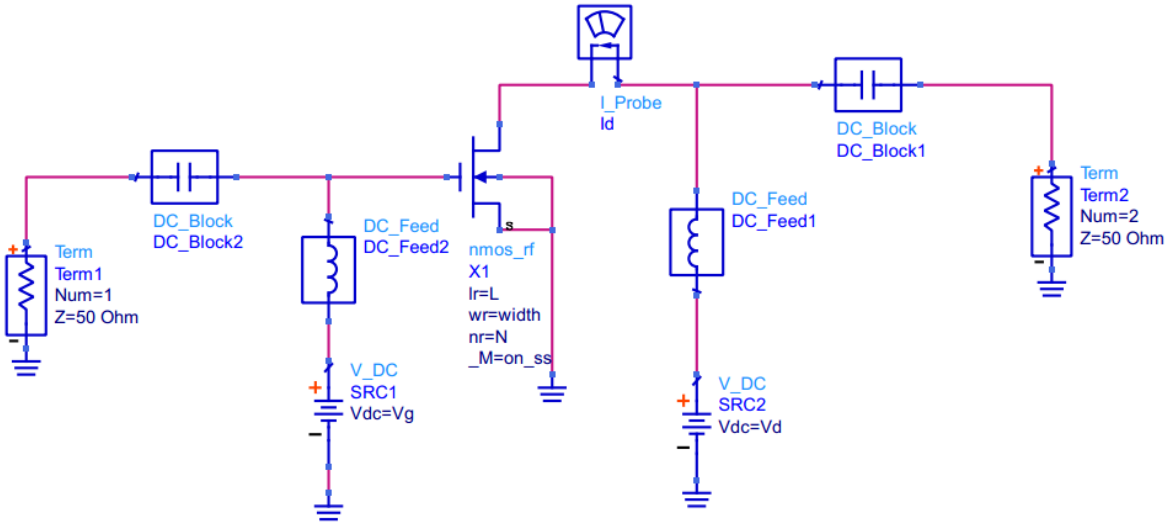


Figure 7.6: Simulation setup for the extraction of R_{on} and C_d

Next we aim to extract the parameters such as on-resistance R_{on} and output capacitance C_d. R_{on} is obtained from DC simulations by $R_{on} = V_d/I_d$, where V_d is the drain-to-source voltage and I_d is the drain current. C_{out} is derived from S-parameter simulations by calculating $C_{out} = im(Y_{22})/(2\pi f)$. Figure 7.7 shows the simulation results of R_{on} as a function of drain-to-source voltage V_d for different gate voltage V_g. The condition for deep triode region is $V_d << 2(V_g - V_{th})$, as a consequence, the lowest on-resistance R_{on} appears

for values of V_d close to zero and values of V_g close to the peak. To ensure a reliable operation, the maximum value for V_g is 1.1V, the drain voltage is chosen with a medium value 0.5V (V_d can range from 0 to 1.1V), then we can obtain the relation of R_{on} versus the width of transistor as plotted in Figure 7.8. Obviously, R_{on} is inversely proportional to the transistor width.

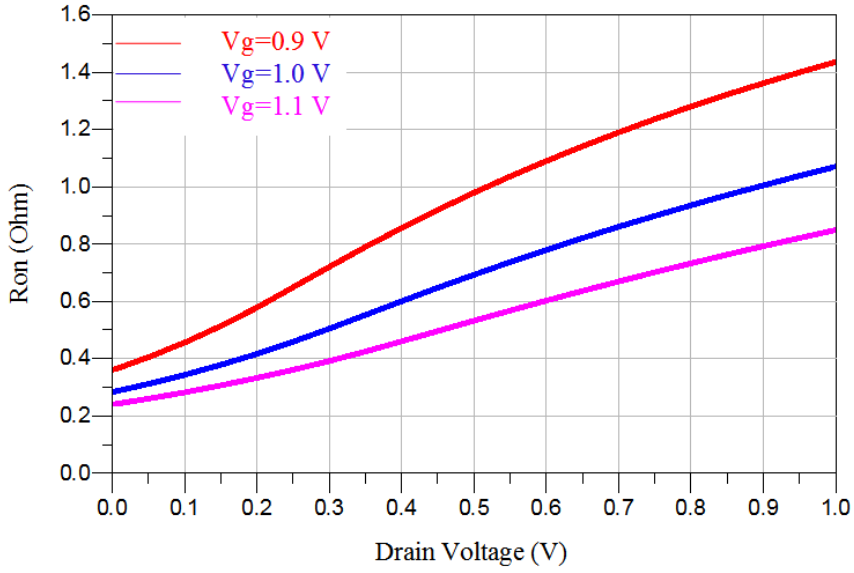


Figure 7.7: R_{on} as a function of drain voltage V_d for different gate voltage V_g

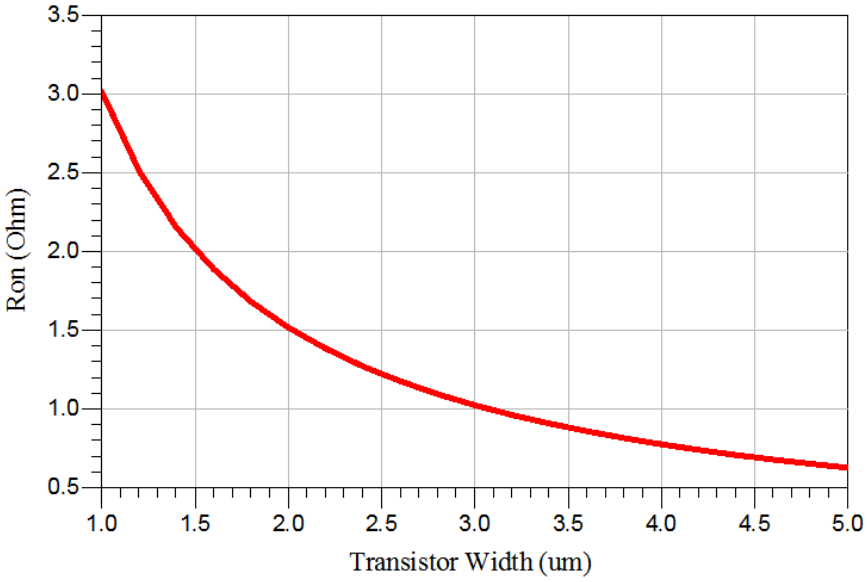


Figure 7.8: R_{on} as a function of transistor width assuming that $V_d = 0.5V$ and $V_g = 1.0V$

The drain parasitic capacitance including the drain-to-source and drain-subtrate paracitic capacitances is a function of biasing condition as well as the layout implementation. Since

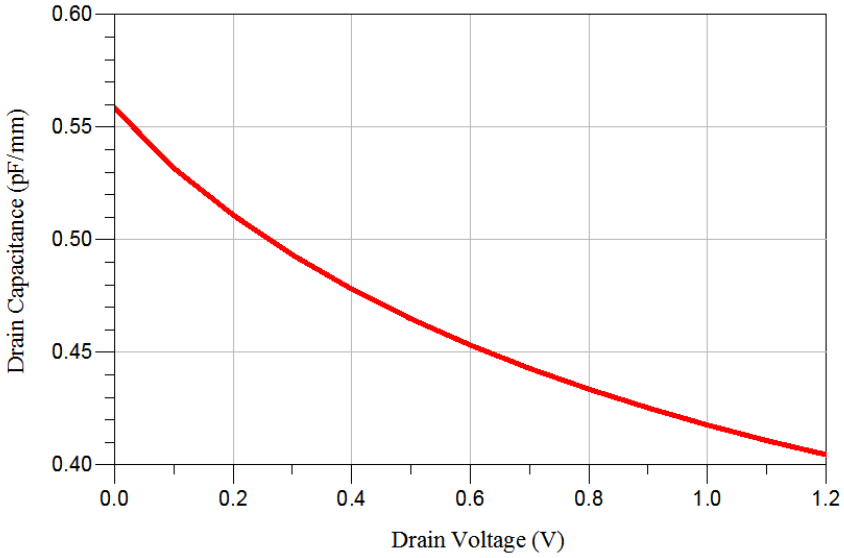


Figure 7.9: C_d as a function of V_d assuming that the W=5um and M=512

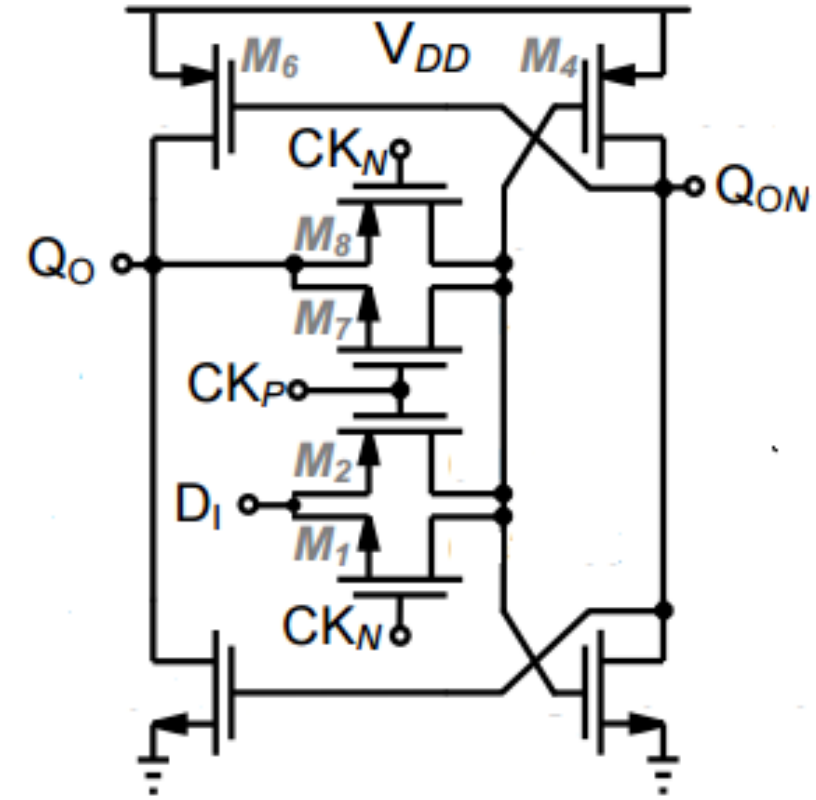
the characterization of drain capacitance C_d is meaningful when the transistor is OFF, C_d is investigated when $V_g = 0$. Figure 7.9 shows the simulation results of drain capacitance per mm of gate width, given as a function of drain voltage V_d. It can be observed that the drain capacitance is inversely proportional to the drain voltage V_d.

For optimum Class E PAs, R_{on} is taken at its minimum value while C_d comes from a standard average over the range of drain voltage V_d in the OFF-state. Since C_d is proportional to the transistor gate width ($C_d \propto W$) and R_{on} is inversely proportional to the transistor gate width ($R_{on} \propto 1/W$), the product $R_{on} \cdot C_d$ is constant and technology defined. Generally speaking, a larger switch device will lead to a more efficient amplifier, since the ratio between R_{on} and the effective load R_L will decrease, thus increasing the efficiency. In addition to efficiency enhancement, a larger device will lower the effects of mismatch. After certain point, the increase of the switch size no longer benefits since other issues related to power dissipation will start to dominate. This is because such large transistors would lead to a large input capacitance, thus a high power is required to drive the array. In this design, the PA transistor width is chosen to be 5um as a result of a compromise among mismatch between the transistors, input capacitance and R_{on}.

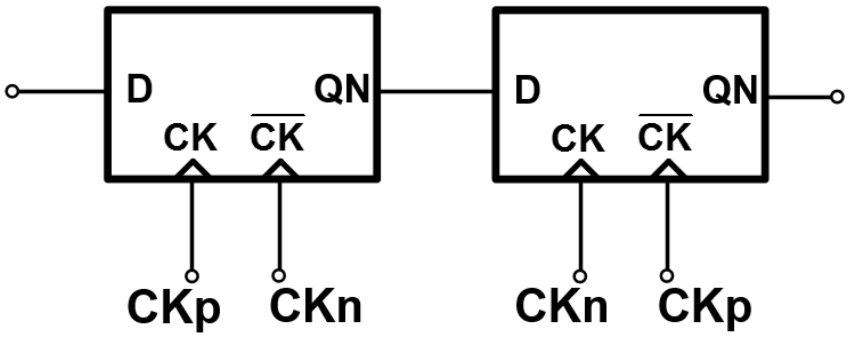
7.4. IMPLEMENTATION OF DIGITAL ENVELOPE MODULATOR

In this section, the digital envelope modulator is explained in more detail. First, a large number of the flip-flops are employed before and after the binary-to-thermometer encoder for synchronizing all unit cells to the clock, in order to reduce undesirable harmonic distortion related to early-late arrival of input data of each unit cell.

The flip-flop is master/slave edge triggered and comprises two cascaded multiplexer



(a)



(b)

Figure 7.10: (a)multiplexer based latch including last data buffer; (b)master/slave edge triggered flip-flop

based latches, as shown in Figure 7.10. In the sense mode of operation, the input clocks CKP /CKN are low/high and consequently, the input data (DI) passes through the “lower” pass-gate logic of M1/M2 and is subsequently buffered by the cascaded inverters of M3/M4 and M5/M6. It signifies that the path between DI and QO is transparent. In the store mode, on the other hand, CKP /CKN are high/low, thus the “top” pass-gate logic of M7/M8 is transparent, and the “lower” one is opaque. As a result, the two inverters of M3/M4 and

M5/M6 are cross-coupled with each other and latch the digital input signal. All transistors of flip-flop circuit are implemented with the most minimal possible aspect ratio in 40 nm CMOS, i.e., W/L = 0.12µm/0.04µm to minimize area and power consumption.

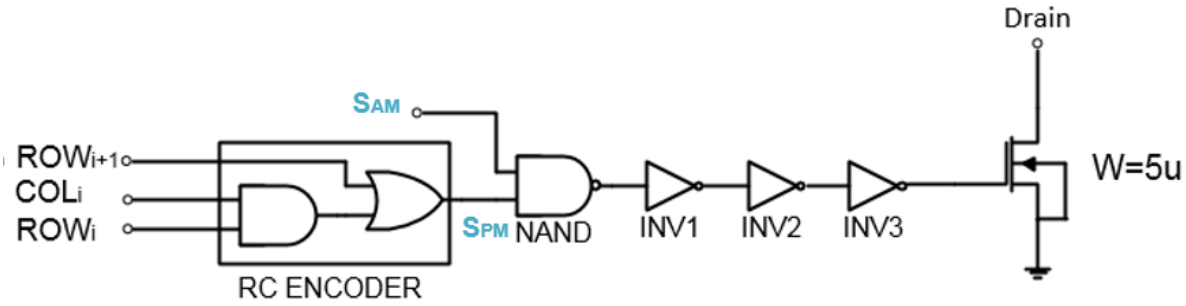


Figure 7.11: MSB unit cells

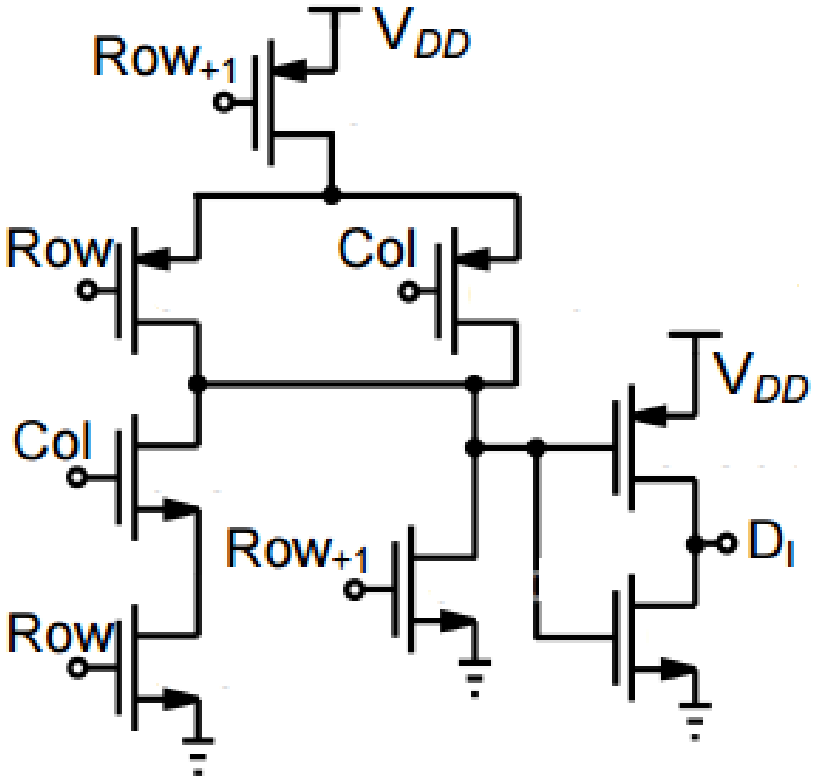


Figure 7.12: AND-OR gate based decoder

Next, a comprehensive description of the MSB unit cell is given. The schematic of the MSB unit-cell is illustrated in Figure 7.11. It consists of an AND-OR gate for decoding row-

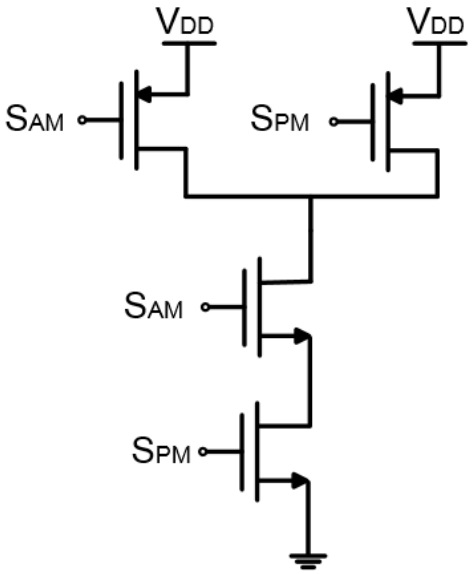


Figure 7.13: NAND gate

and column-data, an NAND gate, an inverter-chain and the PA transistor. The AND-OR decoder is given in Figure 7.12. The output of decoder is given as $OUT = Row_{+1}//(Row\&Col)$ and it is fed into the NAND gate, which is implemented with a custom design as depicted in Figure 7.13 to determine whether this unit cell should be activated. Note that both the ROW/COL decoder and the NAND gates employ transistors in its most minimal possible aspect ratio in 40 nm CMOS, i.e., W/L = 0.12µm/0.04µm. In the end, an inverter chain made up of three inverters (see Figure7.14) are inserted to drive the large size of the PA transistor with the transistor size listed in Table 7.1. Figure 7.15 presents the layout for the MSB unit cell.

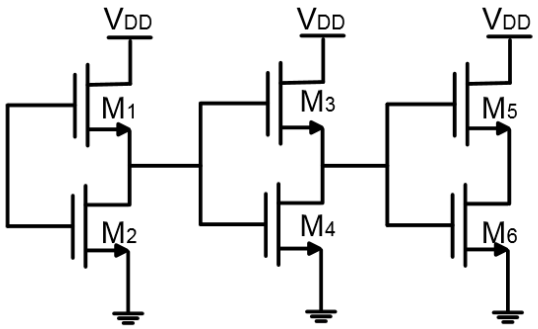


Figure 7.14: Inverter chain

The LSB unit cell is of the same circuit structure but the size of PA transistor is 1/4 of that in the MSB unit cell and the same trend goes for the inverter chain.

Table 7.1: Transistor size for the inverter chain in Figure 7.14

Device	M_1	M_2	M_3	M_3	M_5	M_5
L(um)	0.04	0.04	0.04	0.04	0.04	0.04
W(um)	0.12	0.24	0.29	0.58	0.70	1.40

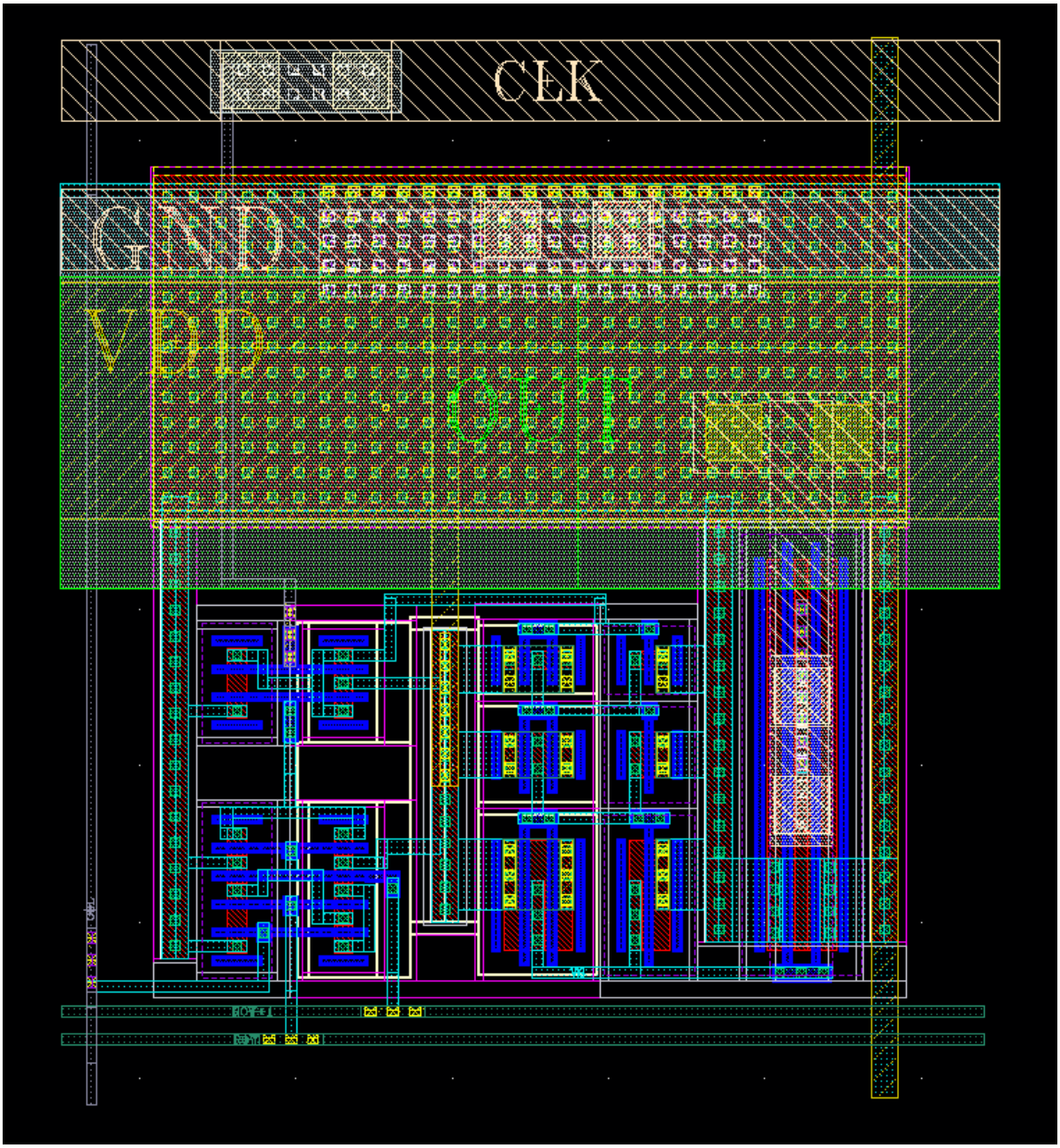


Figure 7.15: MSB unit cell layout

7.5. STUDY OF A DIGITALLY-CONTROLLED CLASS E WITH LOSSLESS PASSIVES

The digital envelope modulator, as discussed in previous section, can be implemented by properly turning on and off a large array of PA transistors ultilising AND gates. In chapter

3, we propose a conceptual equivalent model which is composed of an ideal switch and a series vatiable resistor to model the digital envelope modulator. In this section, a more accurate transistor-level equivalent circuit is employed. Based on this model, we studied the performance of a differential digitally-controlled Class E with lossless passives.

7.5.1. DIGITAL ENVELOPE MODULATOR MODELING AND CHARACTERISTICS

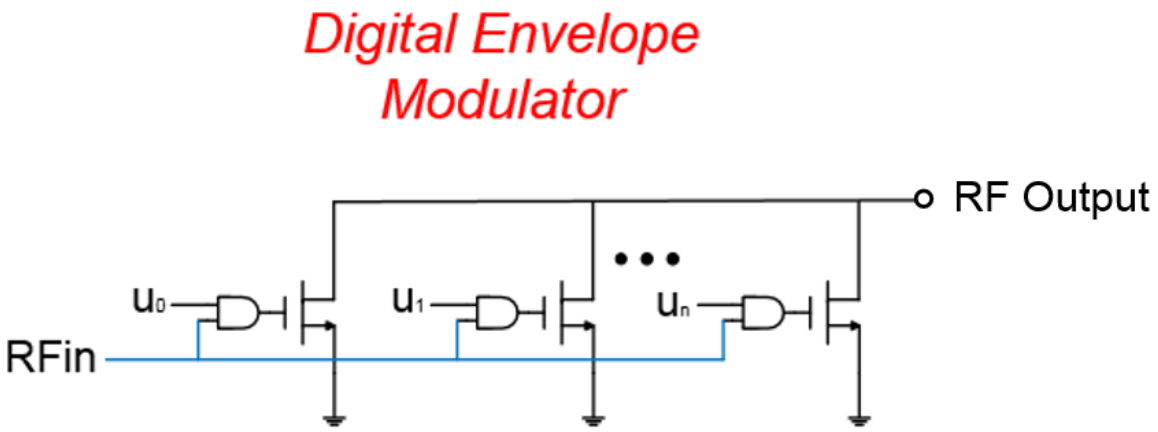


Figure 7.16: Basic schematic for digital envelope modulator

The proposed transistor-level equivalent circuit, as depicted in Figure 7.16, is composed of two parallel-connected (at drain terminal) transistors, one with its input connected to the driving source represents the "on" part and the number of parallel devices is represented by a parameter on_ss, the other with its input connected to ground represents the “off ” part and the number of parallel devices is given by a parameter off_ss, as depicted in Figure 7.17. The sum of these two parts is fixed by the resolution, meaning that once the resolution is determined, $on_ss + off_ss = constant$. In this case, a 9-bit resolution is chosen as a result of a compromise between the quantization noise and chip area according to the system simulation results in the seedcom project, Consequently, the overall number of transistors is 512 and the number of working (“ON”) transistors on_ss can range from 1-512 according to the digital amplitude signal.

This section studies the possibilities of high efficient and high power Class E power amplifier with standard devices in 40nm CMOS. As demonstrated in Section 2.2, the design set K_E as well as the drain efficiency are determined by the transistor technology parameters (namely the ON-resistance, OFF-resistance, and the total output capacitance seen into drain node). Thus in the first part of the significance section, a discussion of device model and characteristics is given. Based on it, simulation for a differential digitally-controlled

Class E power amplifier is performed to provide guidance for the practical design and implementation.

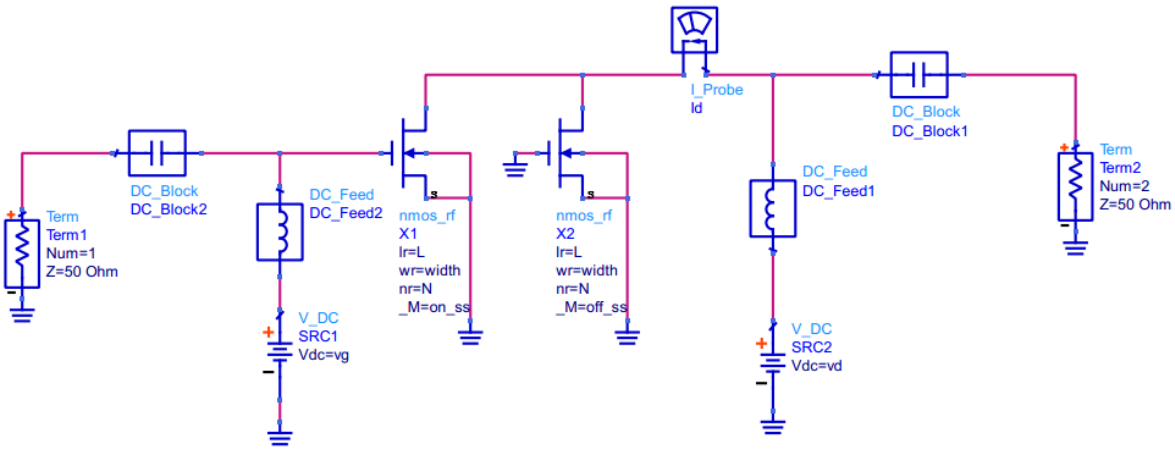


Figure 7.17: Simulation setup for the extraction of R_{on} and C_d for the segmented devices

The transistor-level model for the digital envelope modulator, as shown in Figure 7.1, consists of two parallel transistors, one gate is connected to the driving source while the other gate is connected to ground. In order to extract the transistor technology parameters for this digital envelope modulator, the simulation setup presented in Figure 7.17 are employed. If all the transistors are "OFF" ($on_ss = 512$), the minimum value for the measured off-state resistance R_off is equal to 383.7 $K\Omega$. If all the transistors are "ON" ($on_switch = 512$), the resulting on-resistance R_{on} ($V_g = 1.1V$) and drain capacitance C_d ($V_g = 0$) as a function of drain-to-source voltage V_d are plotted in Figure 7.18 and 7.19.

As shown in Figure 7.18 and 7.19, the drain capacitance C_d and on-resistance R_{on} for switching device arrays are bias dependent. However, a single equivalent lumped value is desired for each parameter to design a Class E PA. Instead of considering the probability density function of the dynamic load line of the switching devices, a more pragmatic method has been employed here for quantitative analysis. With this method, the on-resistance R_{on} is chosen at its minimum value and the drain capacitance C_d is derived from a standard average over drain-to-source voltage V_d range in the OFF state ($V_g = 0$). Thus the values for R_{on} and C_d in this situation are 0.225 Ω and 2.33 pF respectively.

Next the effect of the number of "ON" transistors on the parameters R_{on} and C_d is investigated. Assuming $V_d \approx 0$, Figure 7.20 shows the relation between the effective on-resistance R_{on} and the number of "ON" transistors on_ss, where the gate width is chosen to be 5um to obtain a small R_on. Obviously, the value of R_{on} is proportional to the number

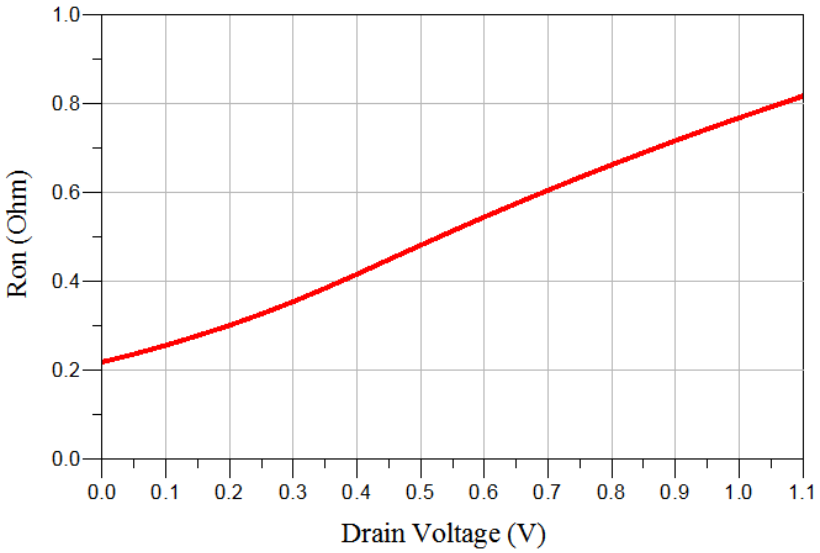


Figure 7.18: R_{on} as a function of drain-to-source voltage V_d when $on_switch = 512$

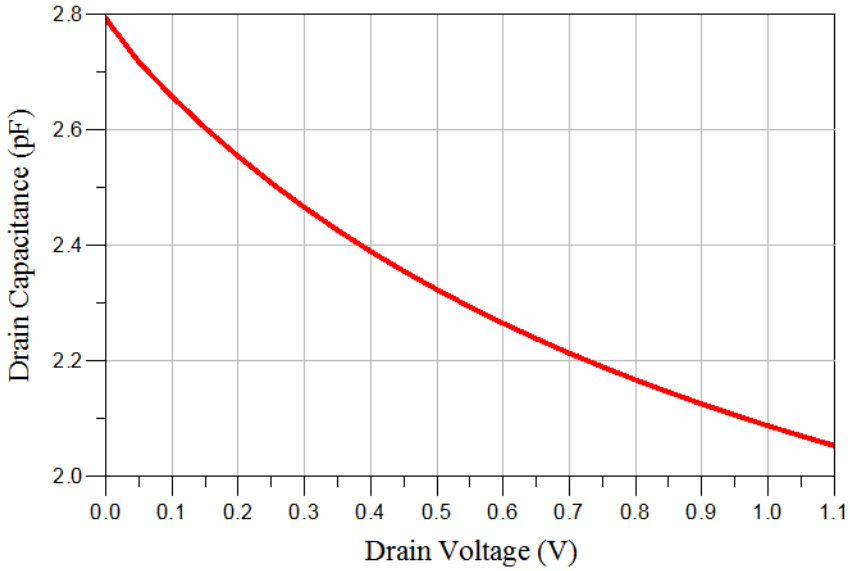


Figure 7.19: C_d as a function of drain-to-source voltage V_d when $on_switch = 512$

of "ON" transistors and when on_ss increases from 1 to 512, the resulting R_{on} decreases from 111.6 Ω to 0.225 Ω. Drain capacitance as a function of on_ss with $V_g = 0V$ is plotted in Figure 7.21. In this figure, C_d is constant in spite of the change of on_ss. In conclusion, the simulation results for R_{on} and C_d as a function of on_switch agree with the description of the digital-controlled Class E in subsection 3.2.2.

A differential Class-E power amplifier is given in Figure 7.22, where the equivalent model for the digital envelope modulator is employed. The load network before the balun for a single Class E consists of a shunting capacitor, a finite DC-feed inductance and a series-tuned output circuit, which may have a residual reactance as shown in Figure 7.22. Note

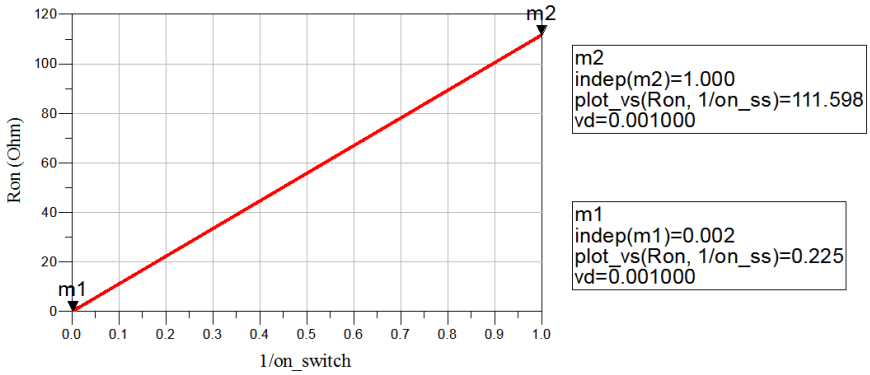


Figure 7.20: R_{on} as a function of 1/on_switch where on_switch means the number of ON transistors

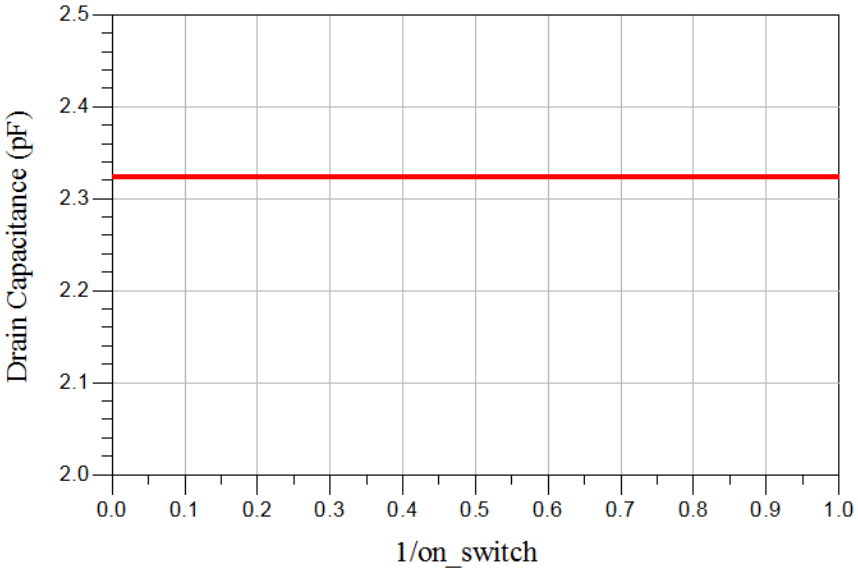


Figure 7.21: Drain capacitance per mm of gate width as a function of 1/on_switch where on_switch means the number of ON transistors

that the capacitor C_P shunting the transistor is due to the layout parasitics and the load network paracitics.

7.5.2. GENERAL DESIGN PROCEDURE

The detailed steps are described as follows.

Step 1: Calculate the technology paramete $m_{on} = \omega C R_{on}$ and $m_{off} = \omega C R_{off}$

The on-resistance and off-resistance for the digital envelope modulator employed in Figure 7.22 are 0.23 Ω and 383.7 $k\Omega$ according to the previous subsection. And the simulated average output capacitance is 2.4 pF. Thus the technology parameters $m_{on} = \omega C R_{on}$ and $m_{off} = \omega C R_{off}$ at 2.4GHz are in the order of $10^{-}3$ and 10^4, respectively. It should be notica-

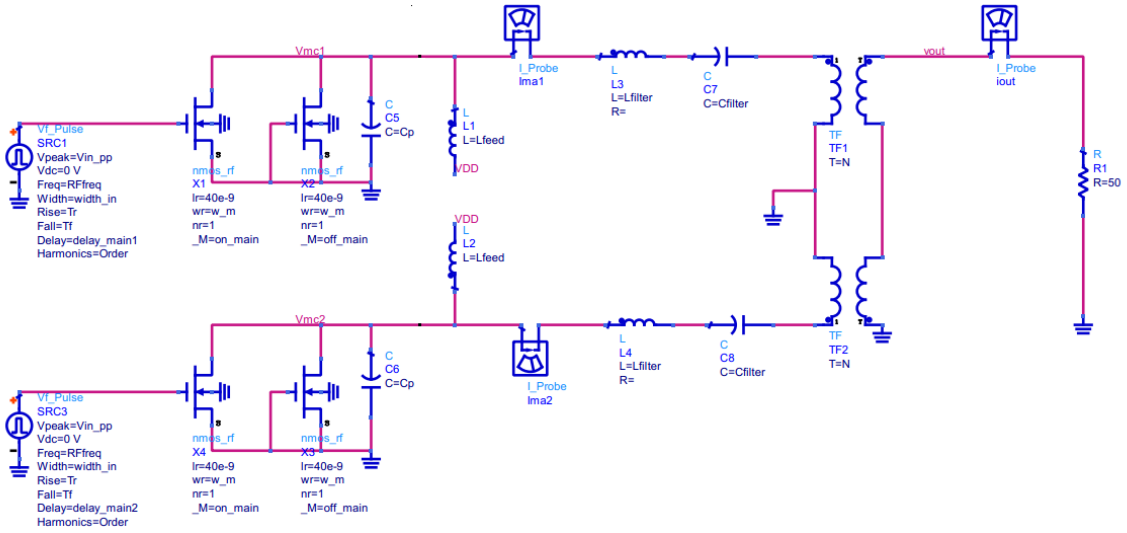


Figure 7.22: Schematic for a differential digitally-controlled Class E power amplifier with lossless passives

ble that the value for m_{on} is somehow optimisic since they are obtained from ideal models through simulation (not layout extracted views or real measurements). In practice, layout devices will have extra paracitic capacitance which in Figure 7.22 is represented by a shunting capacitor C_P and hence m_{on} will increase significantly. Assuming that C_P equals 3 pF. The total output capacitance C_E, due to the intrinsic transistor capacitance (2.4 pF) and the layout paracitics (3 pF) is 5.4 pF, thus $m_{on} = 0.02$.

Step2: Calculate the design set K_E in Maple based upon the input parameters input parameters (m_{on}, m_{off}, d, ω, V_{DD}, q, α, and k) by the analytical approach in [15]
As demonstrated in Section 2.2, the design set K_E is a function of many input parameters (m_{on}, m_{off}, d, ω, V_{DD}, q, α, and k). Among these parameters, m_{on} and m_off are technology limited. $\omega = 1$ and $V_{DD} = 1$ for a general case. The other parameters including q, α, and k are user defined and they can be tuned to meet a specific requirement in terms of efficiency, output power, and drain voltage and current waveforms. Usually, α and k are set to zero at the beginning so that the amplifier will operate at optimum Class-E condition (zero-voltage switching and zero-slope switching). Then one can sweep q to obtain the design set K_E.

Step 3: Calculate the supply voltage V_{DD}, load resistance R_E and passive components based upon the design set K_E, loaded quality factor Q_0 and desired output power.

With a given output capacitance C_E and desired output power P_{out}, the component values (e.g., DC feed inductance L_{feed}, series tuned filter L_{filter} and C_{filter}, turn ratio N

and supply voltage V_{DD}) for the Class E PA circuit in Figure 7.22 can be calculated based upon the design set K_E as follows.

$$R_E = \frac{K_C}{\omega C_E} \tag{7.1}$$

$$N = \sqrt{\frac{25}{R_E}} \tag{7.2}$$

$$V_{DD} = \sqrt{\frac{R_E P_{out}}{K_P}} \tag{7.3}$$

$$L_{feed} = R_E \frac{K_L}{\omega} \tag{7.4}$$

For this case ($K_X > 0$)

$$L_{filter} = R_E \frac{K_X + Q_L}{\omega} \tag{7.5}$$

$$C_{filter} = \frac{1}{\omega R_E Q_L} \tag{7.6}$$

For this case ($K_X < 0$)

$$L_{filter} = R_E \frac{K_X}{\omega} \tag{7.7}$$

$$C_{filter} = \frac{1}{\omega R_E (Q_L - K_X)} \tag{7.8}$$

7.5.3. RELIABILITY STUDY RELATED TO OXIDE BREAKDOWN

Oxide breakdown, as discussed in Section 2.3, has always been the predominant effect for CMOS PAs. To ensure a reliable operation, both V_{GS} and V_{GD} should not exceed the limit voltage. For a switch-mode Class E PA, the transistor only conducts half duty-cycle. And the drain voltage becomes 0 when the transistor is "ON", while the gate-voltage is typically 0 when the transistor is "OFF". Thus being reliable in a Class E PA means that both the amplitude of the input signal (applied to the gate) and the drain peak voltage must stay below the upper limit. With a resonable input voltage (0-1.1 squre wave), we only need to pay attention to the drain voltage. In this part, a study of the drain-to-source waveform is given to explore a reliable Class E operation with large output power and high efficiency.

To begin with, we assume that the amplifier operates at maximum output power mode ($q = 1.42$) with zero switching voltage ($\alpha = 0$) and zero switching slope ($k = 0$). The derived design set K_E based upon the input parameters (see Table 7.2)by the analytical approach in [15] is listed in Table 7.3.

Since the device output capacitance C_E is fixed so that the load resistance R_E can be

Table 7.2: Input parameters for analytical model

$\omega = 1$	$m_{on} = 0.02$	$m_{off} = 13480$
$q = 1.42$	$\alpha = 0$	$k = 0$
$d = 1$	$V_{DD} = 1$	$Q_0 = 2$

Table 7.3: Results of design set K_E based upon the parameters in Table 7.2

$K_L = 0.703$	$K_C = 0.705$	$K_P = 1.189$	$K_X = 0.015$

Table 7.4: Design details based on the design set K_E in Table 7.3 and the corresponding simulated results

$N = 1.7$	$V_{DD} = 0.34V$	$C_P = 3pF$
$Lfeed = 0.4nH$	$L_{filter} = 1.12nH$	$C_{filter} = 3.95pF$
$P_{out} = 14.97dBm$	$\eta_D = 90.2\%$	$V_{DS,peak}/V_{DD} = 3.56$

found from K_C, then the supply voltage will be known via K_P for a presdertermined P_{out} value. Obviously, a larger supply voltage results in a higher output power. However, Class E power amplifier is very vulnerable to oxide breakdown because the peak drain voltage generated by this topology can approach up to 3.6 times the supply voltage. For this reason, special care should be taken when determing the supply voltage. It is known that the reliable gate-drain voltage for 40nm CMOS standard thin-oxide transistors is 1.1-1.2V. Using the DC conservative limit, the supply voltage should be lower than 0.4V to ensure a safe operation.

Figure 7.23 depicts the simulated drain-to-source voltage with circuit component values in Table 7.4. In this example, the peak drain voltage is limited below 1.2V by applying a small supply voltage (0.34V), but the output power decreased to 14.97dBm at the same time. To reduce the peak drain voltage and improve reliable operation, the variable-voltage operation ($\alpha \neq 0$ and $k = 0$) seems a good choice since this operation can obtain lower peak drain voltage as described in Section 2.2. This decrease of peak drain voltage, on the other hand, can relax the limitation for the supply voltage thus improving the output power. When $\alpha = 1$, the corresponding design set K_E are listed in Table 7.6. In this case, the supply voltage can increase to 0.40V to ensure a reliable operation. Figure 7.7. the peak drain voltage decreases from $3.56V_{DD}$ to $2.97V_{DD}$. The degradation of drain efficiency is only 2%.

Table 7.5: Input parameters for Class E analytical model

$\omega = 1$	$m_{on} = 0.02$	$m_{off} = 13480$
$q = 1.42$	$\alpha = 1$	$k = 0$
$d = 1$	$V_{DD} = 1$	$Q_0 = 2$

It should be noted that the discussion above is following the DC conservative limit. But

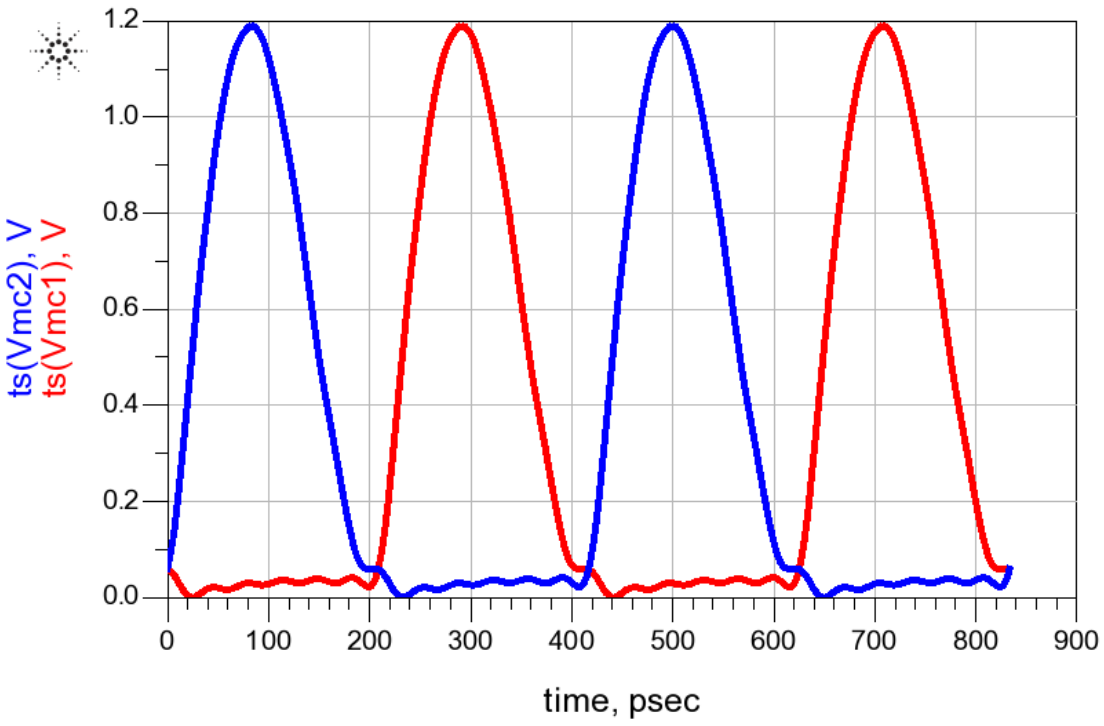


Figure 7.23: Simulated drain-to-source voltage for a optimum Class E ($\alpha = 0$) with circuit component values in Table 7.4

Table 7.6: Results of design set K_E based upon the parameters in Table 7.5

$K_L = 0.929$	$K_C = 0.534$	$K_P = 0.853$	$K_X = -0.392$

Table 7.7: Design details based on the design set K_E in Table 7.6 and the corresponding simulated results

$N = 2.0$	$V_{DD} = 0.40V$	$C_P = 3pF$
$Lfeed = 0.4nH$	$L_{filter} = 0.85nH$	$C_{filter} = 4.32pF$
$P_{out} = 16.02dBm$	$\eta_D = 88.2\%$	$V_{DS,peak}/V_{DD} = 2.97$

according to the study of AC oxide breakdown limit in Section 2.3, the maximum RF voltage peaks for reliable device operation in a switch-mode PA should be much larger than the DC limits since the physical mechanism of oxide breakdown is triggered by the rms values rather than the peak values. For this reason, a larger supply voltage of 0.6 is selected. The other component values except for the supply voltage remains, as presented in Table 7.25. Figure 7.25 shows the resulting drain-to-source voltage. In this case the peak voltage can approach 1.84V in the half "OFF" cycle. And the output power can be as large as 19.81 dBm as a consequence of the increased supply voltage with only 2.5% decrease in the drain efficiency.

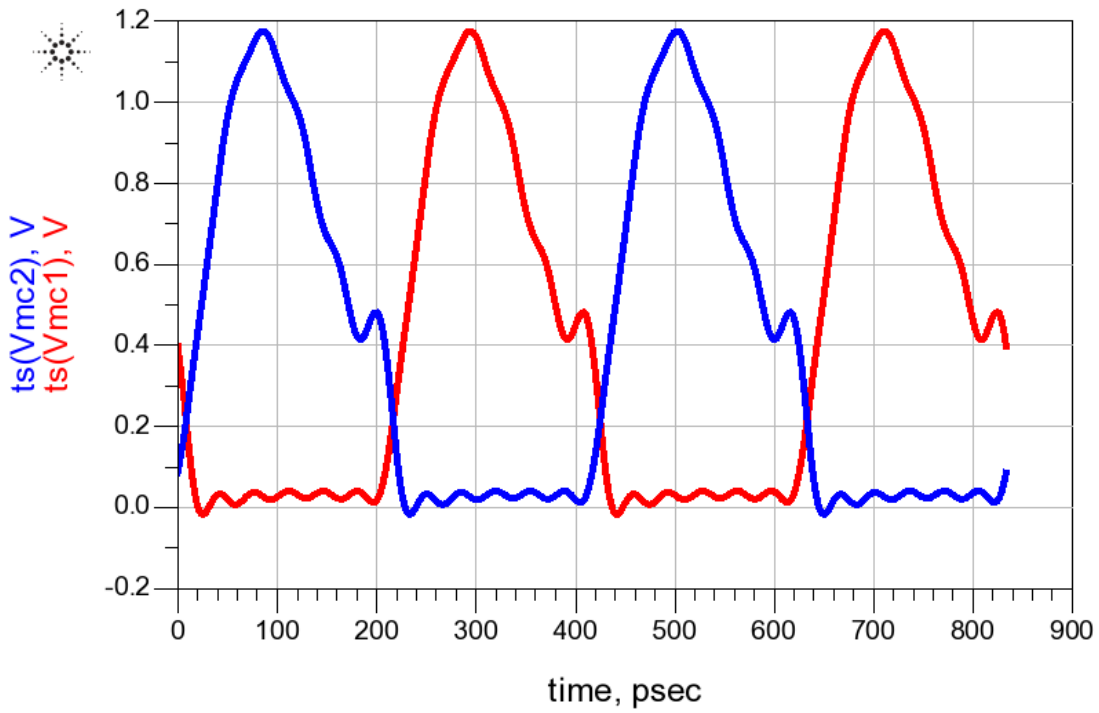


Figure 7.24: Simulated drain-to-source voltage for a suboptimum Class E ($\alpha = 1$)with circuit component values in Table 7.7

Table 7.8: Design details based on the design set K_E in Table 7.6 and the corresponding simulated results

$N = 2.0$	$V_{DD} = 0.60V$	$C_P = 3pF$
$Lfeed = 0.4nH$	$L_{filter} = 0.85nH$	$C_{filter} = 4.32pF$
$P_{out} = 19.81dBm$	$\eta_D = 87.7\%$	$V_{DS,peak}/V_{DD} = 2.97$

7.5.4. AM-AM AND AM-PM TRANSFER CHARACTERISTICS

As explained before, a digitally-controlled Class E power amplifier works based on the on-resistance modulation. By selectively turning on and off a plurality of RF amplifier transistors in a digital manner, the effective on-resistance are varying, resulting in the change of output power and effciency. In this part, we investigate the transfer characteristics in the digitally-controlled Class E PA as shown in Figure 7.22.

Figure 7.26 shows the magnitude and Phase of the output voltage (normalized with respect to the supply voltage) at fundamental as a function of the number of "ON" devices (on_{ss}). Obviously, the magnitude and the output voltage increases as on_{ss} varies from 1 to 512. However, the phase decreases slightly with the same trend. The corresponding output power and drain efficiency is given in Figure 7.27. It can be observed that both the output power and drain efficiency rise as a result of increased (on_{ss}). These results verify the feasibility of the proposed digitally-controlled Class E power amplifier based on a transistor

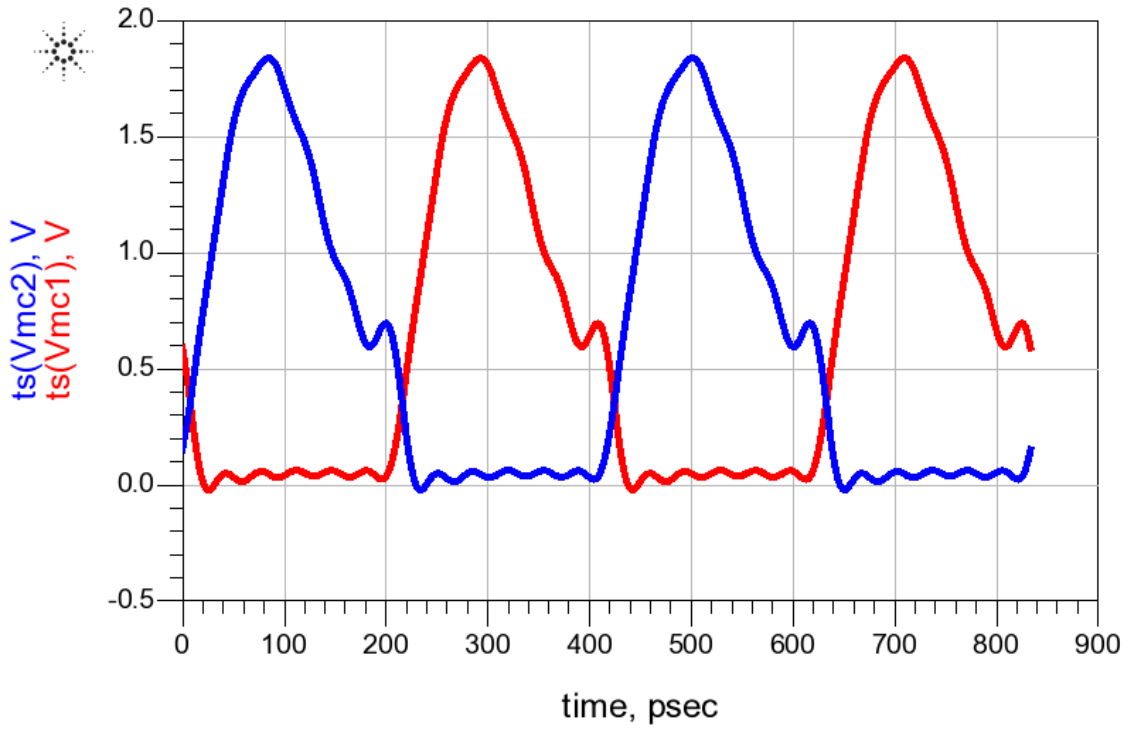


Figure 7.25: Simulated drain-to-source voltage for a suboptimum Class E ($\alpha = 1$)with a larger supply voltage 0.6V.

level. (Chapter 3 based on a conceptual model).

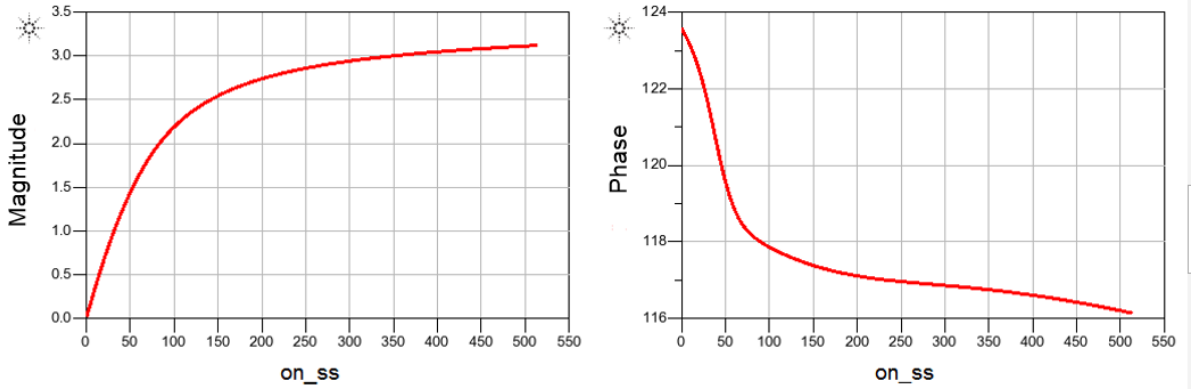


Figure 7.26: (a) Magnitude (b) Phase of the output voltage at fundamental as a function of the number of "ON" devices (on_ss)

7.6. DIGITALLY-CONTROLLED CLASS E PA DESIGN

As discussed in Subsection 3.2.2, Class E PA can be made digital by controling the array of parallel transistors according to the digital envelope signal. In this project, the key is at-

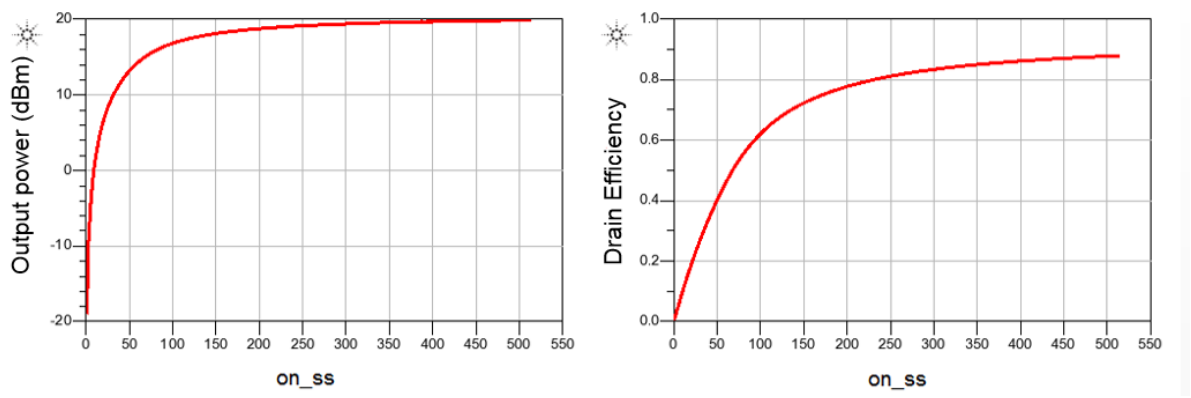


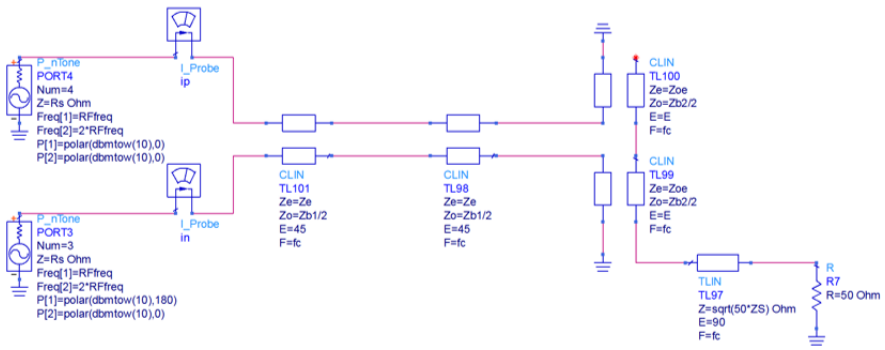
Figure 7.27: (a) Output power (b) Drain efficiency of the digitally-controled Class E power amplifier as a function of the number of "ON" devices (on_ss)

tached to the design and implementation of PA stages. Since the model of the digital controled active devices has been given in the previous section, this section will focous on the design and implementation of the output matching network of this digital-domain Class E amplifier.

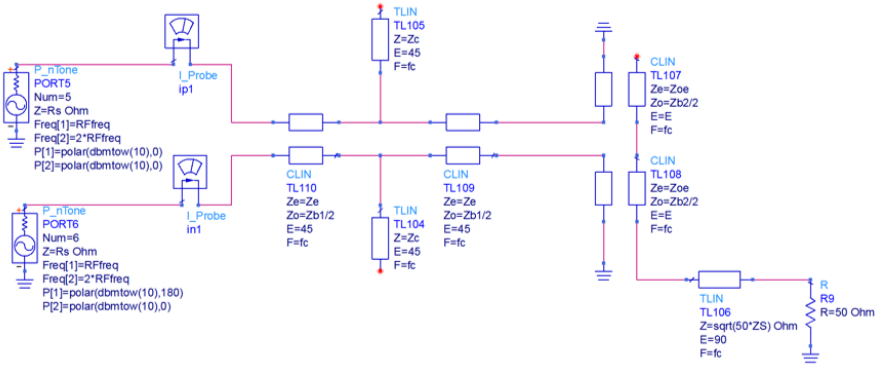
The desired broadband performance are achived by employing the so-called "Class E with parallel-circuit" loading condition in a differential topology. This is because parallel-circuit Class E with finite DC feed inductance and zero extra teactance X, as described in Subsection 4.2, is simpler and more wideband in nature compared with the traditional RF-choke Class E. In addition, it provides larger output power for a given supply and loading resistance. The balun in this case is implemented using the previously proposed compensated Marchand balun, which has been proved in Chapter 6 to have a wide bandwidth.

7.6.1. DESIGN OF OUTPUT MATCHING NETWORK USING SYMMETRICAL AND HOMOGENEOUS COUPLED LINES

Generally, the load network of Class E power amplifier should provide open for all higher harmonics. In practice, correct impedances are required only at the fundamental and second harmonic since the third and higher harmonics are of relatively small amplitudes. Begining with a simpler type of coupled lines, namely, symmetrical coupled lines in a homogeneous dielectric medium, two types of load network in Figure 7.28 are presented for the differential Class E PA. The marchand balun is employed here to convert the differential signal to a single-ended one. An additional $\lambda/4$ transmission line coming after the marchand balun matches the single-ended impedance to the standard 50 Ω. Morever, coupled lines composed of two $\lambda/8$ coupled line section is inserted in front of the Marchand balun to transform the balanced impedance to a smaller value for higher output power.



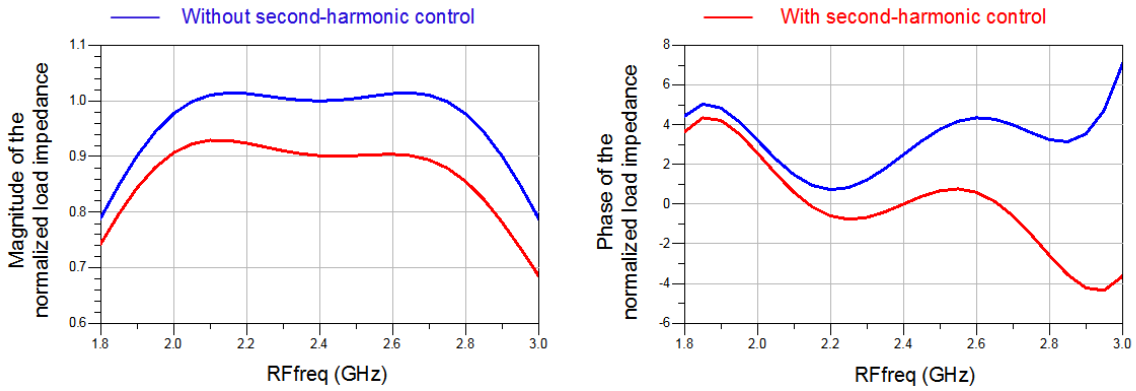
(a) Without even-harmonics control



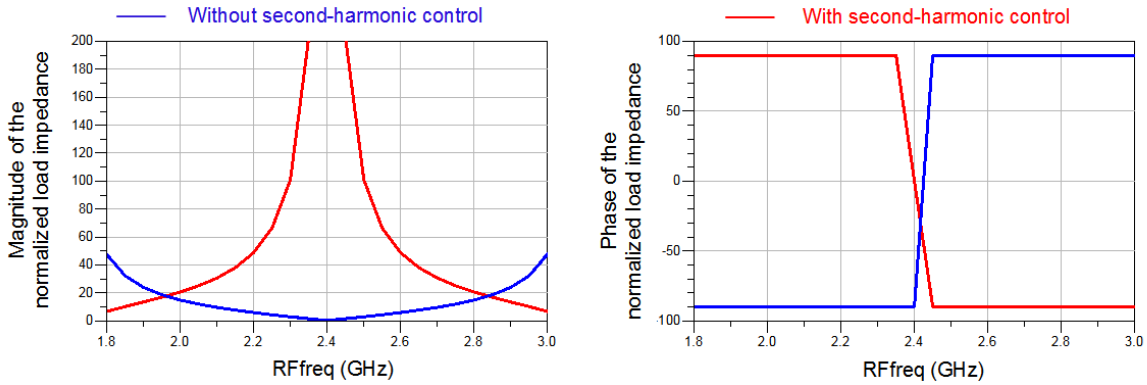
(b) With even-harmonics control

Figure 7.28: Differential load network using symmetrical and homogeneous coupled lines

The only difference between these two load networks is that in Figure 7.28 (b) an open-circuited $\lambda/8$ transmission line is added between the two $\lambda/8$ coupled line section. The reason of this addition is easy to seek by refering to Figure 7.29, where a comparison of input impedances at fundamental and second-harmonic are given for these two structures. First, the fundamental impedance (see Figure 7.29 (a)) slightly reduces by including the even-harmonic control. When it comes to the second-harmonic impedance (see Figure 7.29 (b)), the two cases are quite different. It can be observed that without the open-circuited $\lambda/8$ transmission line, the second-harmonic impedance is approximated to zero around the center frequency, which conflicts with the loading condition for conventional Class E. With the open-circuited $\lambda/8$ transmission line, the magnitude of second-harmonic impedance significantly increases to an infinitely large value. This is because the open-circuited $\lambda/8$ transmission line provides a short-circuited impedance for even-mode signals at the right-end of the first $\lambda/8$ coupled lines and this short termination for even-mode signals is transformed to an open condition at the reference plane of the active device.



(a) fundamental load impedance



(b) second-harmonic load impedance

Figure 7.29: Simulated results for load impedance in Figure 7.28

7.6.2. DESIGN OF OUTPUT MATCHING NETWORK USING RE-ENTRANT COUPLED LINES

Table 7.9: Summary of the typical design parameters for the re-entrant type coupled lines

Design	Material	Thickness	Trace Width
Substrate Layer 1	Rogers 3003 ($\epsilon_{r1} = 3.0$)	$H_1 = 0.75mm$	$W_1 = 3.2mm$
Substrate Layer 2	Rogers 3010 ($\epsilon_{r2} = 10.2$)	$H_2 = 0.13mm$	$W_2 = 1.5mm$

In this design, the coupled lines are implemented using the re-entrant type structure as depicted in Figure 6.8 to overcome the stringent dimensional requirements for tight coupling in circuit fabrication. Typical design parameterd for the re-entrant type coupled lines are listed in Table 7.9, resulting in 74Ω even-mode impedance and 8.2Ω odd-mode impedance.

Figure 7.31 presents the layout for the Class E load network using the re-entrant type coupled lines. The compensated Marchand balun can be designed following the general

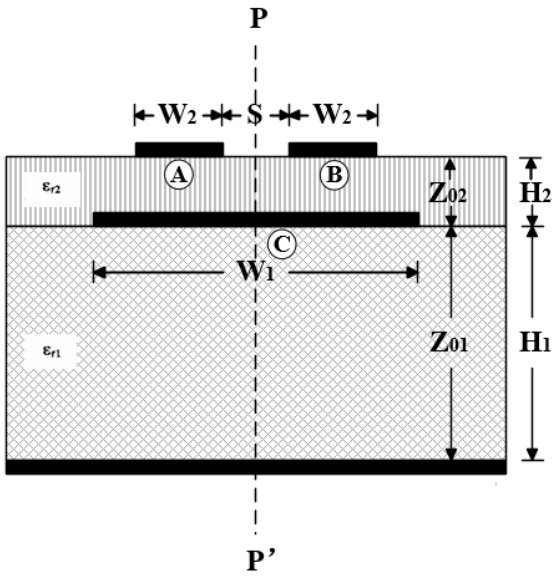


Figure 7.30: Microstrip re-entrant-type coupled lines

procedure discussed in Chapter 5, where the initial length of the coupled line section is determined by the characteristics impedance and electrical length of the compensation line. Then optimize the design to include the non-ideal load of specific ports, especially the non-ideal ground. Another key point of the Class E load network is the harmonic control circuit, especially for the second-harmonic component. Instead of inserting an open-circuited $\lambda/8$ transmission line, the required even-mode harmonic short in the re-entrant coupled lines can be realized by simply adding a conductive via from the floating middle-layer conductor to ground at the position (from left to right) where the electrical length for the second harmonic $2f_0$ (f_0 is the operating frequency) equals $\lambda/4$. Because of the coupling between the three conductors (See Figure 7.30), the top metals are forced ground for even-mode signals. Since it is difficult to form blind vias (for example, the via from the middle layer to ground), an island with a through via from the top metal layer to the ground metalization (see Figure 7.31) is created at the specific position where the electrical length for the second harmonic $2f_0$ equals $\lambda/4$.

Simulation results of the fundamental and second-harmonic impedance for the load network in Figure 7.31 are plotted in Figure 7.32. Compared to the case with a floating island (simulation results for this case are shown in Figure 7.33), the one with the island connected to ground not only provides larger second-harmonic impedance, but also improves the imbalance in both amplitude and phase for the differential to single-ended conversion.

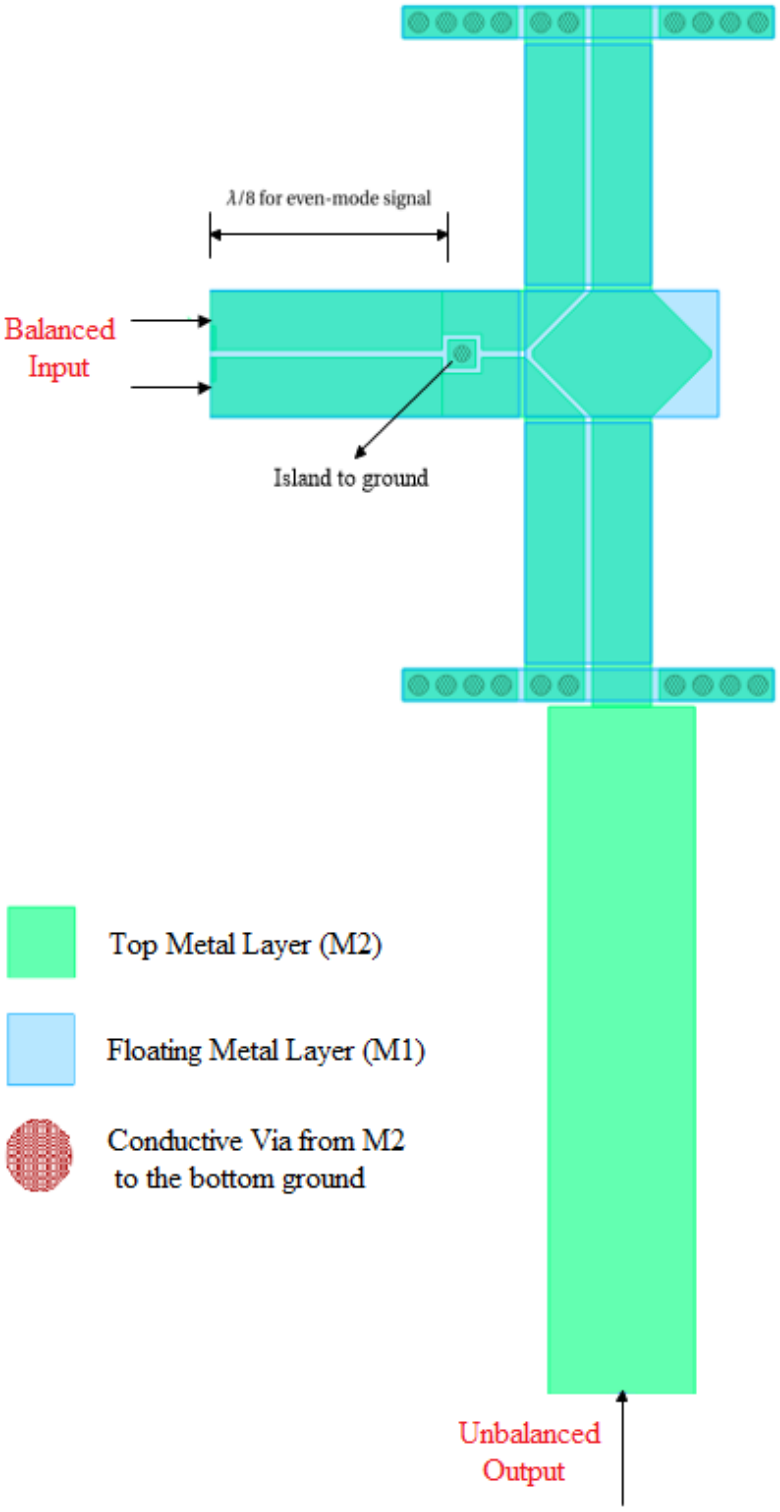
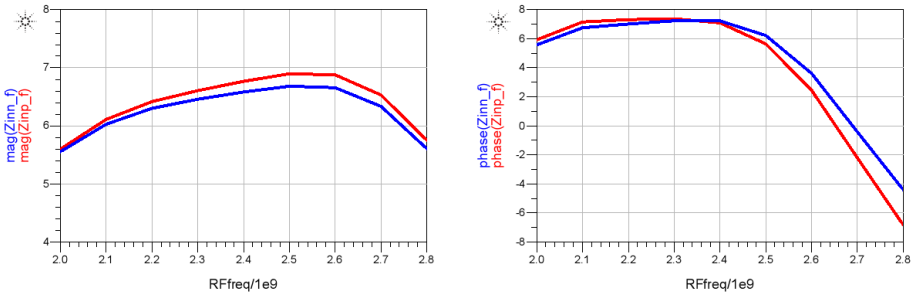


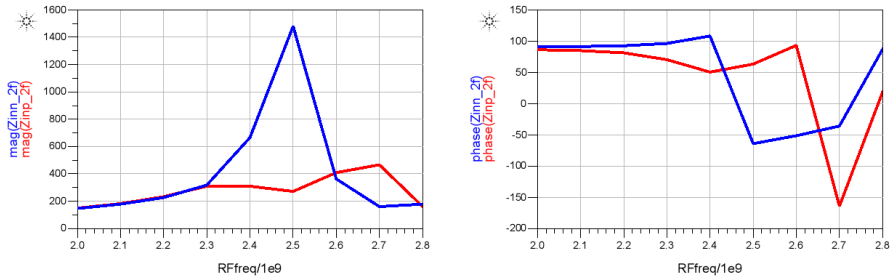
Figure 7.31: Layout for the Class E load network

7.6.3. SIMULATION RESULTS

Figure 7.34 shows the schematic for the differential parallel-circuit Class E power amplifier with practical balun design. Note that other passive components are lossless and the values

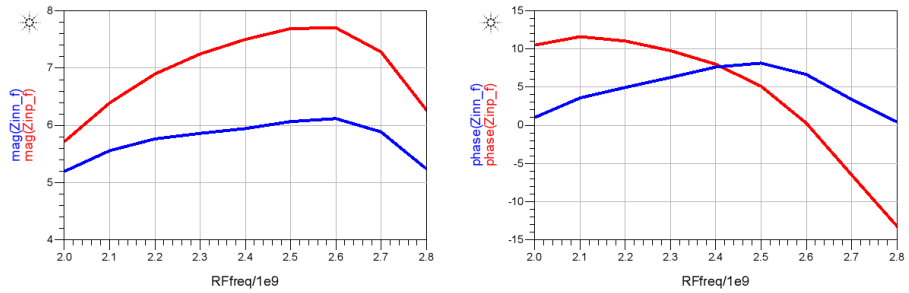


(a) fundamental impedance

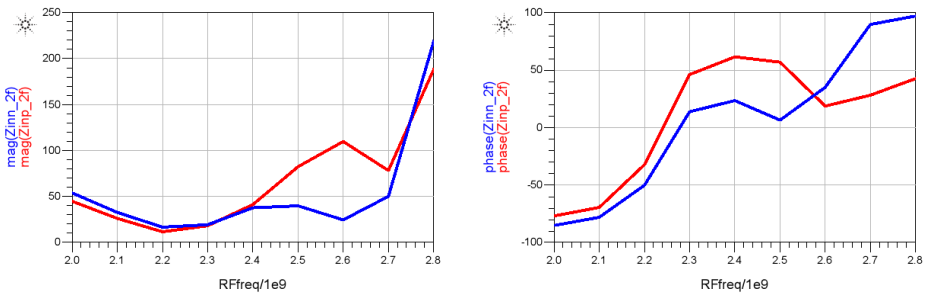


(b) second-harmonic impedance

Figure 7.32: (a) Fundametal (b) Second-harmonic impedance for the load network shown in Figure 7.31 with the island connected to ground



(a) fundamental impedance



(b) second-harmonic impedance

Figure 7.33: (a) Fundametal (b) Second-harmonic impedance for the load network shown in Figure 7.31 with a floating island

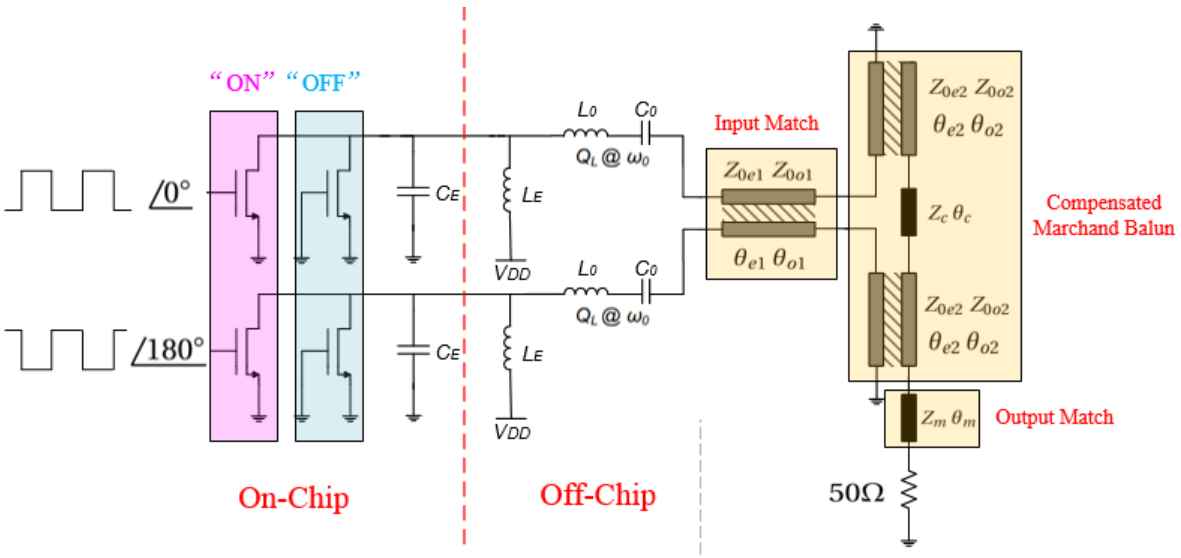


Figure 7.34: Simplified differential parallel-circuit Class E using re-entrant type coupled lines

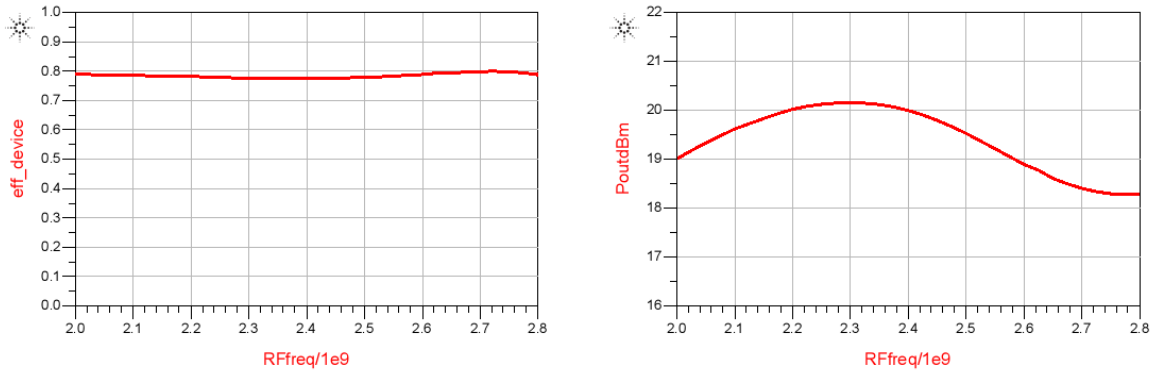


Figure 7.35: Wideband efficiency and output power performance for the Class E in Figure 7.34

are set the same with that in Figure 7.22. The resulting efficiency and output power in the frequency range from 2.0GHz to 2.8GHz are plotted in Figure 7.35. It can be observed that the efficiency in the specific frequency range is quite close to 80%. The maximum output power, limited by the low breakdown voltage of the transistors, are 20.2dBm but the variation due to the frequency change is within 2dB.

7.6.4. PRACTICAL IMPLEMENTATION OF OFF-CHIP MATCHING NETWORK

The output matching network is implemented off-chip and bondwires are used to provide interconnects from the device die to the off-chip part (on PCB). As shown in Figure 7.36, four bondwire sets are needed to connect the bias line, the matching networks as well as the PCB ground to the device die. In detail, L_s represents the bondwires from the source of

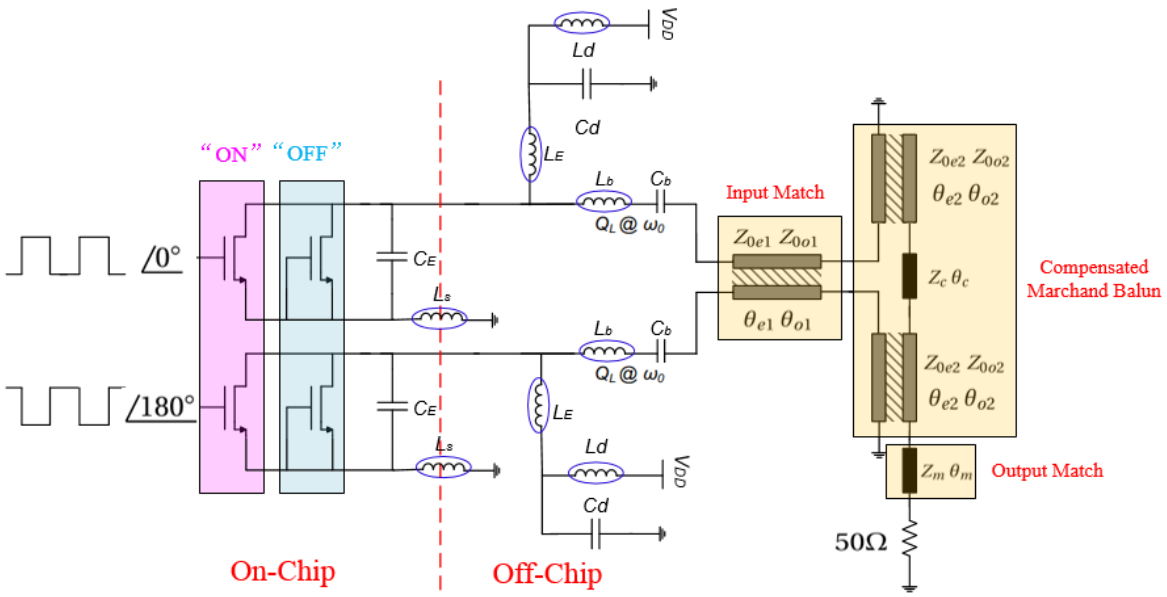


Figure 7.36: Schematic for the broadband Class E PA

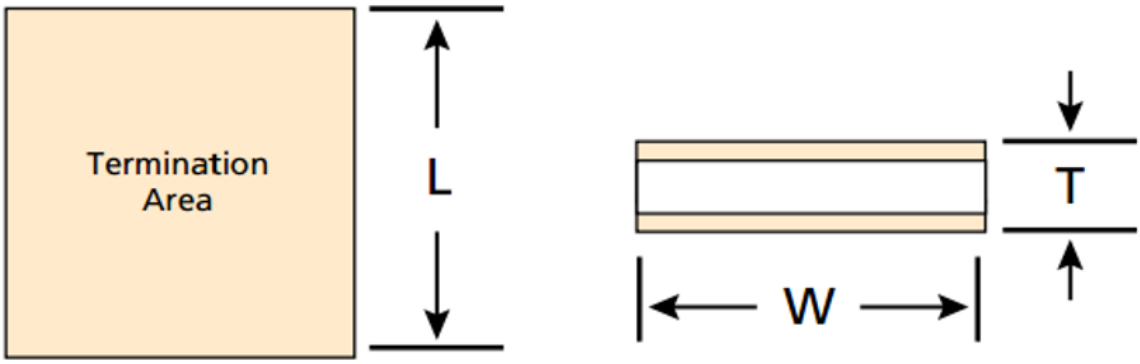


Figure 7.37: SLC chip capacitor

the transistors to the PCB ground, L_b indicates the bondwires from the drain of the transistors to the load network. By combining it with a series capacitor C_b, the LC bandpass filter is formed. The DC-feed inductance L_E, is also implemented using bondwires and it is connected to the bias line with bondwires represented by L_d at DC while at AC, it is shorted to ground with a DC-block capacitor C_d. Figure 7.38 shows details of bondwires from the device die to PCB. Note that the capacitors C_b and C_d in this case are implemented using the wire bondable SLC (Single-layer ceramic) chip capacitor as shown in Figure 7.37, where the thickness depends on the capacitance value.

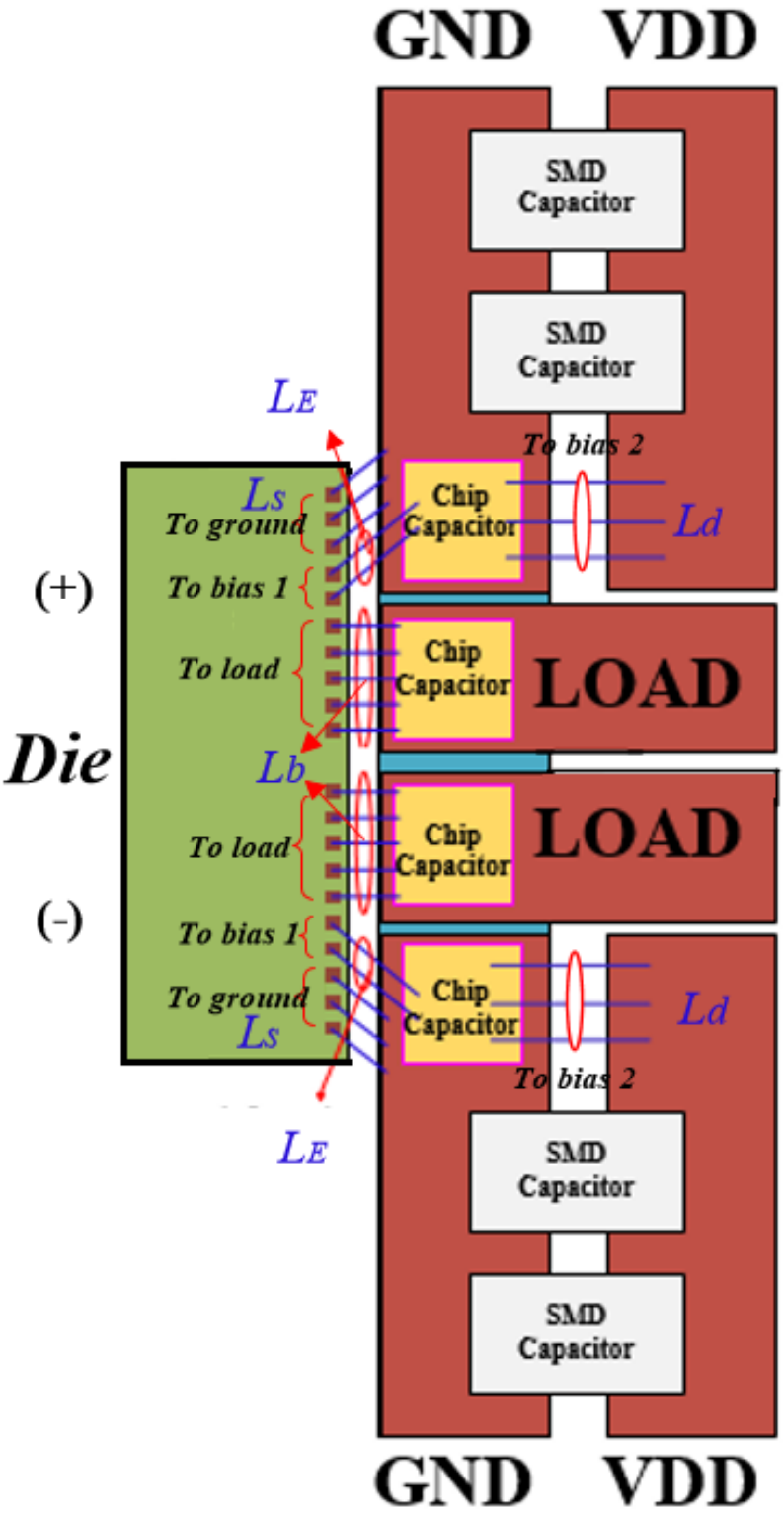


Figure 7.38: Details of bondwires from the device die to PCB

7.7. DOHERTY PA DESIGN EMPLOYING DIGITALLY-CONTROLLED CLASS E

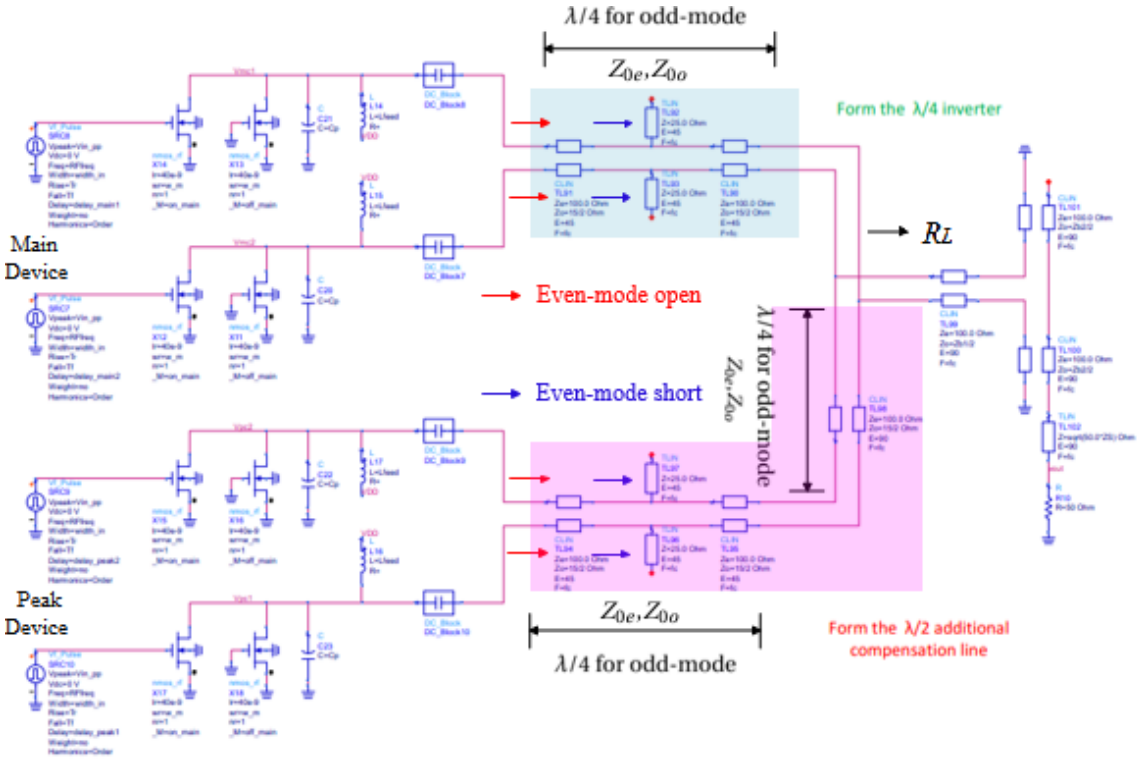
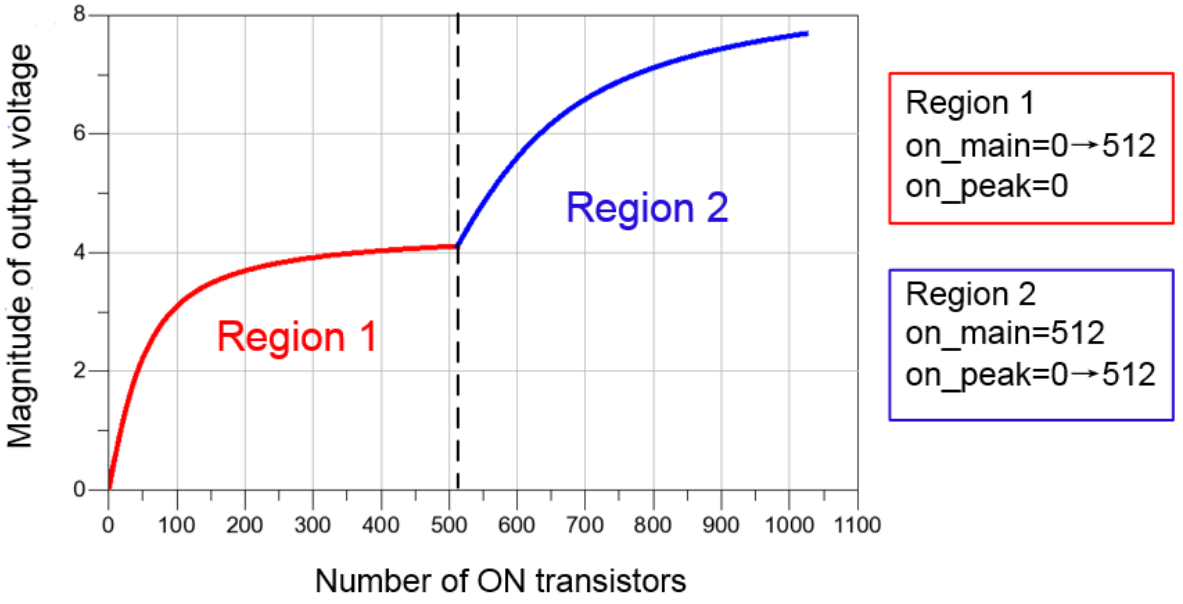


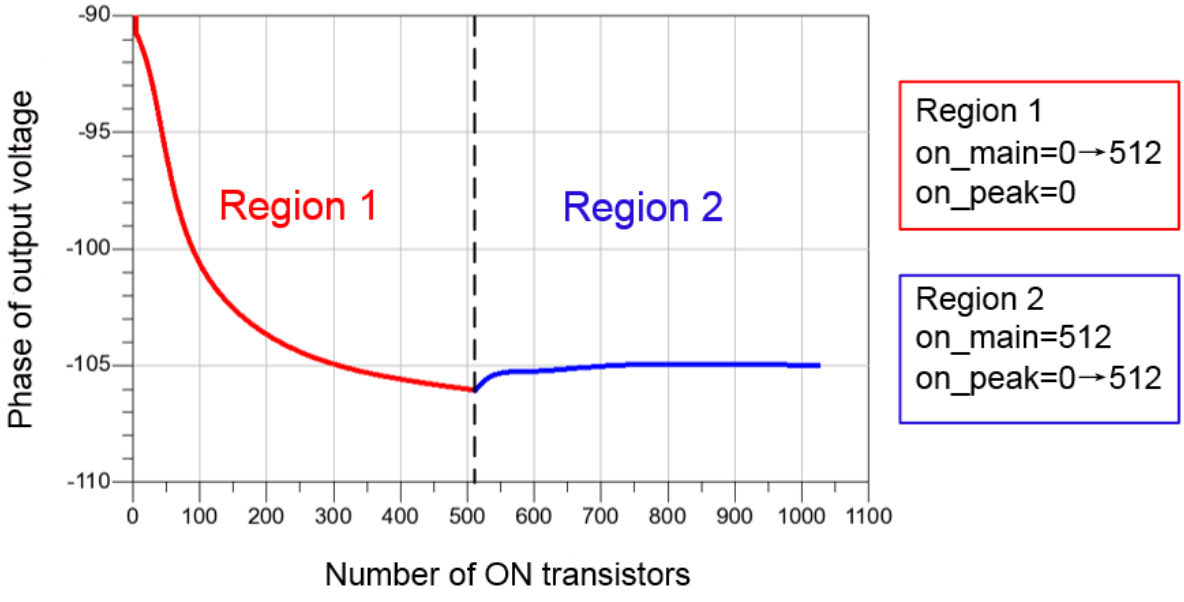
Figure 7.39: Simplified schematic for the proposed Doherty PA using symmetrical coupled lines in a homogeneous medium

In this project, a Doherty PA employong digitally-controled Class E is proposed for enhanced efficiency and extended bandwidth. In terms of efficiency, the digital polar architecture is ultilised here to allow the employment of switch-mode Class E power amplifiers. In addition, the use of a differential parallel-circuit Class E together with a wideband impedance inverter can boost the bandwidth. The simplified schematic for the proposed Doherty PA is shown in Figure 7.39, where the Marchand balun is employed to convert the differential signal to a single-ended one after the parallel combining of the main and peak path. In detail, the coupled lines before the parallel combining in the output matching network for the main device will form the $\lambda/4$ impedance inverter, simutaleously the additional $\lambda/8$ transmission line together with the first $\lambda/8$ coupled lines will provide open for the second-harmonic components. For the peak devices, an additional $\lambda/4$ coupled lines are inserted before the parallel combining, forming the $\lambda/2$ compendation line to boost the load impedance in a wideband fashion at power back-off as we discussed in Chapter 4. In order to ensure the Doherty operation, $Z_{0o} = 2 * R_L$ under the condition that Z_{0e} is large enough, where R_L is the balanced impedance seen from the input of the Marchand balun

and Z_{0e},Z_{0o} are the even-mode and odd-mode impedance of the coupled lines. Note that the coupled lines in this figure are set to be symmetrical on a homogeneous medium for simplicity.



(a) AM



(b) PM

Figure 7.40: Amplitude and phase transfer characteristics for the Class E based Doherty PA in Figure 7.34 at center frequency $f_0 = 2.4GHz$
(Note that the output voltage is normalized with respect to the supply voltage)

Figure 7.40 gives the input (Number of "ON" transistors in total)-output (magnitude

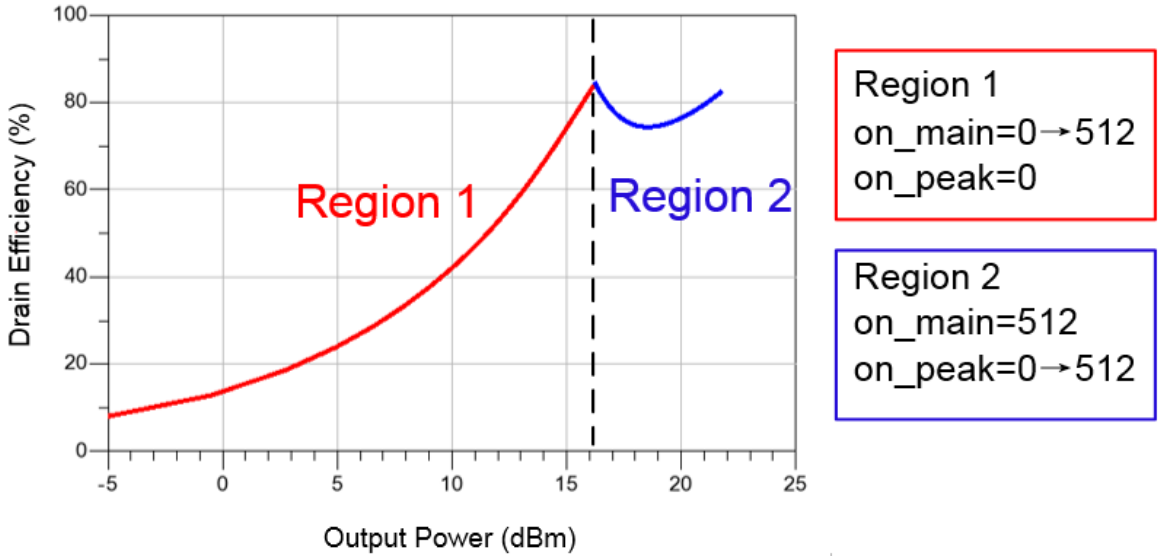


Figure 7.41: Characteristics of efficiency and output power performance for the Class E based Doherty PA in Figure 7.34 at center frequency $f_0 = 2.4GHz$

and phase of the normalized output voltage) transfer characteristics at the center frequency 2.4 GHz. For the red curve, the active devices in the peak branch are entirely off, while the number of "ON" active devices in the main branch ranges from 0 to 512. For the blue curve, the active devices in the main branch are entirely "ON", while the number of "ON" active devices in the peak branch ranges from 0 to 512. Obviously, both the magnitude and phase of the output voltage vary as a function of the number of "ON" transistors, thus verifying the discussion of a digitally-controlled Class-E Doherty PA in Section 3.2. Though the relation between the input and output as shown in Figure 7.40 is quite nonlinear, it can be greatly improved with the aid of pre-distortion circuitry. Figure 7.41 shows the resulting efficiency-output characteristics at the center frequency. There are two efficiency peaks, one is at back-off (the active devices in the main branch are entirely on, while the active devices in the peak branch are entirely off), the other one is at full-power (the active devices in both the main branch and the peak branch are entirely on). The following discussion focuses on these two states to look into the wideband behaviour of this Doherty PA. According to the simulation results in Figure 7.42, a maximum output power of 22dBm with the efficiency above 80% at both full power and 6dB power back-off from 2.1 GHz to 2.7GHz. In addition, both the efficiency and output power for these two states (namely back-off and full power) do not see large variations for the entire frequency range7.39.

7.7.1. IMPLEMENTATION OF OUTPUT MATCHING NETWORK

Figure 7.43 shows the layout of the output matching network (without DC-feed inductance L_E and output capacitance C_E) for the proposed Doherty PA. The same re-entrant type

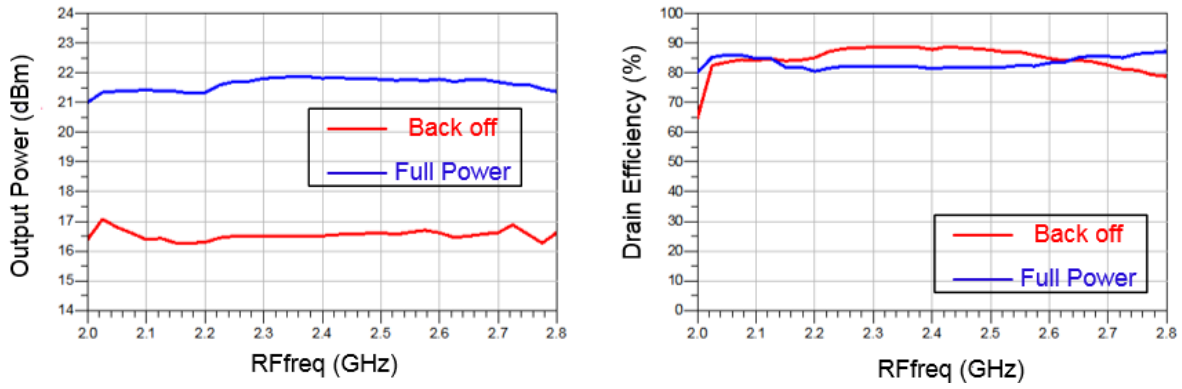


Figure 7.42: Wideband output power and efficiency performance for the Doherty PA shown in Figure 7.39

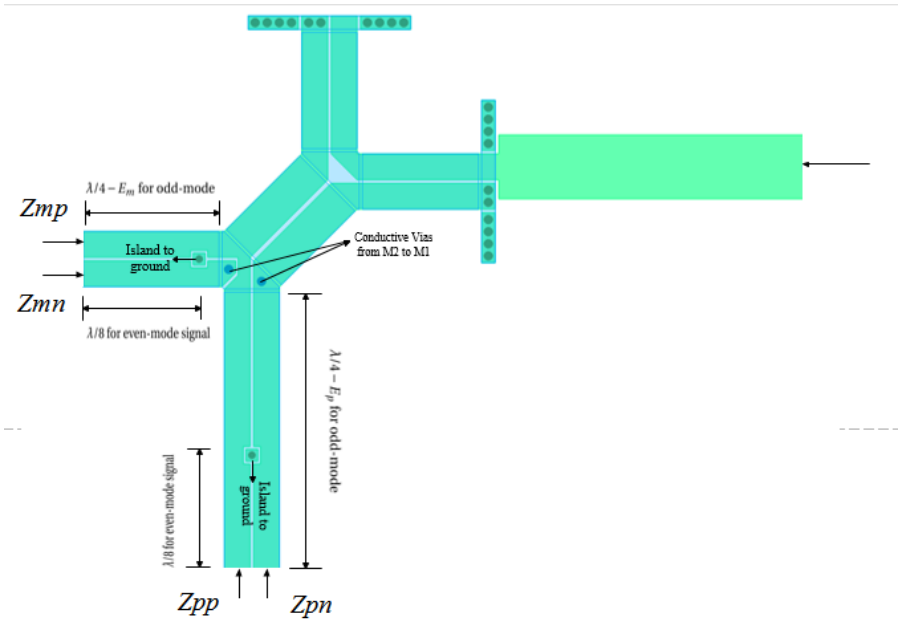
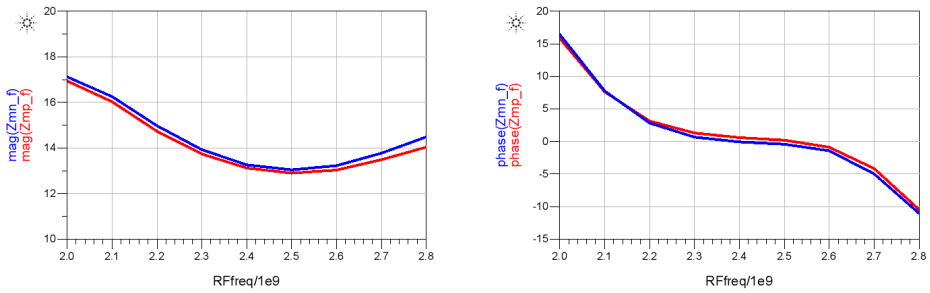


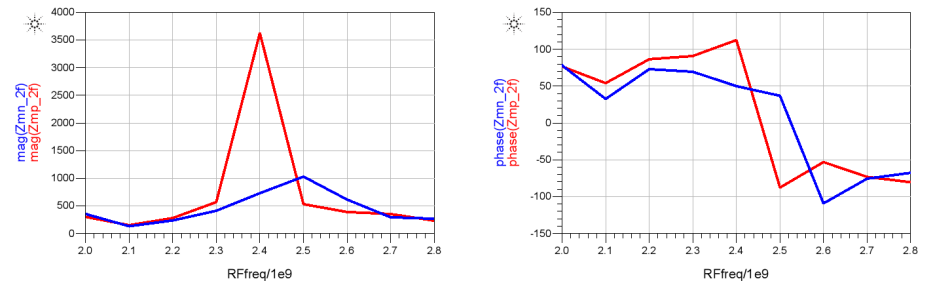
Figure 7.43: Layout of the load network for the proposed Doherty PA using differential Class E topology

coupled lines as in the case of the differential Class E PA are employed here instead of the symmetrical homogeneous coupled lines. In addition, the same trick (the ground island) for the even-harmonic control is applied here. Figure 7.44, Figure 7.45 and Figure 7.46 show the fundamental and second-harmonic impedance at back-off and full power for the Doherty load network in Figure 7.43. Benefiting from the Marchand balun and the ground island, the fundamental impedance imbalance between the differential inputs are quite small for all the listed cases. In addition, we can observe that the second-harmonic impedance is much larger compared to its fundamental value. At back-off (see Figure 7.44), we can obsered that the input impedance for the main branch at the center frequency 2.4 GHz is about 13 Ω and this value decreases to about half of 13 Ω at full power for both the main and peak branch, which is in aggrement with the impedance characteristics for a

symmetrical two-way Doherty PA.

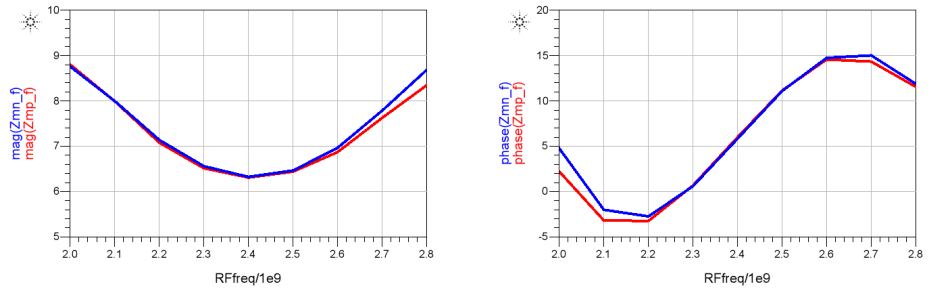


(a) fundamental impedance

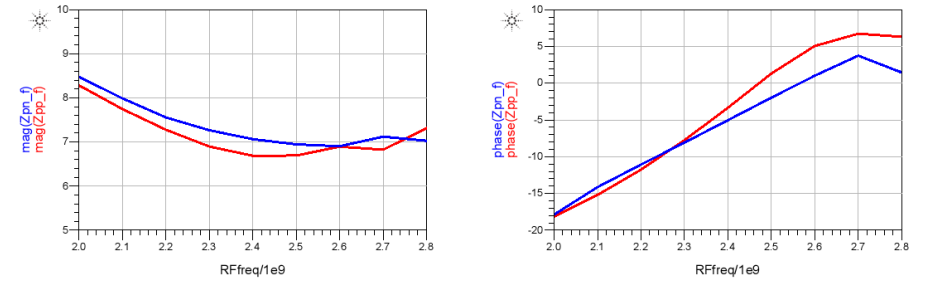


(b) second-harmonic impedance

Figure 7.44: (a) Fundametal (b) Second-harmonic impedance seen by the main PA at power back-off

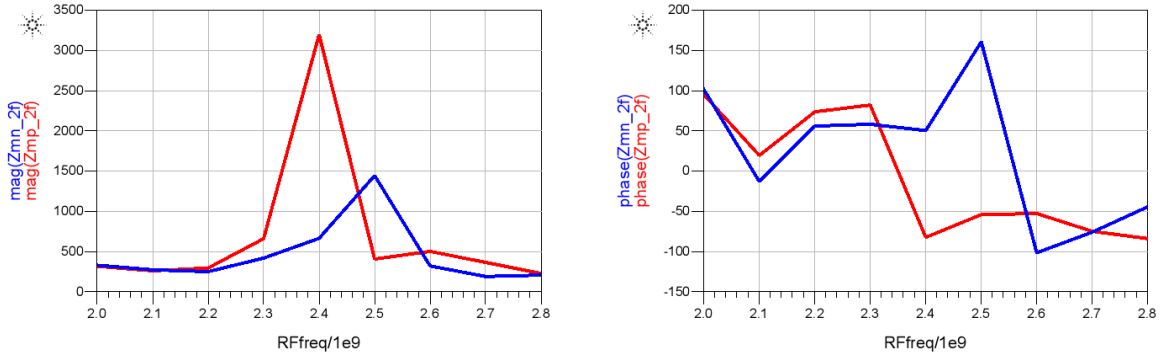


(a) fundamental impedance seen by main amplifier

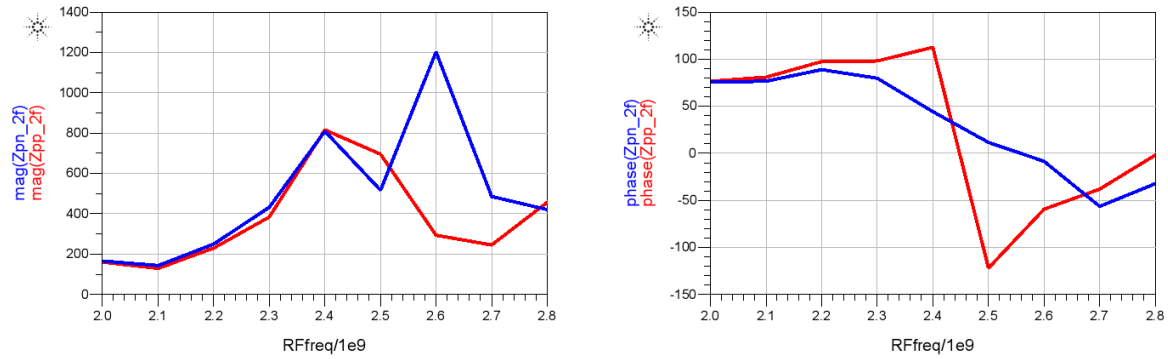


(b) second-harmonic impedance seen by peak amplifier

Figure 7.45: Fundametal impedance seen by (a) the main PA and (b) the peak PA at full power



(a) second-harmonic impedance seen by main amplifier



(b) second-harmonic impedance seen by peak amplifier

Figure 7.46: Second-harmonic impedance seen by (a) the main PA and (b) the peak PA at full power

7.7.2. SIMULATION RESULTS

Employing this load network (see Figure 7.43) in the schematic depicted in Figure 7.39, we can get the efficiency-output power characteristic in Figure 7.48 at 2.4 GHz and the wideband behaviour in Figure 7.49. According to the simulation results, this design can even achieve 70% efficiency at 6dB back-off and full power with a maximum 22 dBm ouput power for full power. Note that the simulation results above is based on ideal ground, loss-less interconnect bondwire inductors and parallel capacitors.

7.8. CONCLUSIONS

Within this chapter, a detailed design and implementation considerations is provided of the digital envelope modulator (on-chip) and the load network (off-chip) in the proposed digitally-controlled Doherty PA. For the digitally-controlled Class-E power amplifier, the transistor-level simulation results show a maximum output power of 20dBm, and a high efficiency which is up to 80% from 2.0 GHz to 2.8GHz in the case of 0.6 supply voltage.

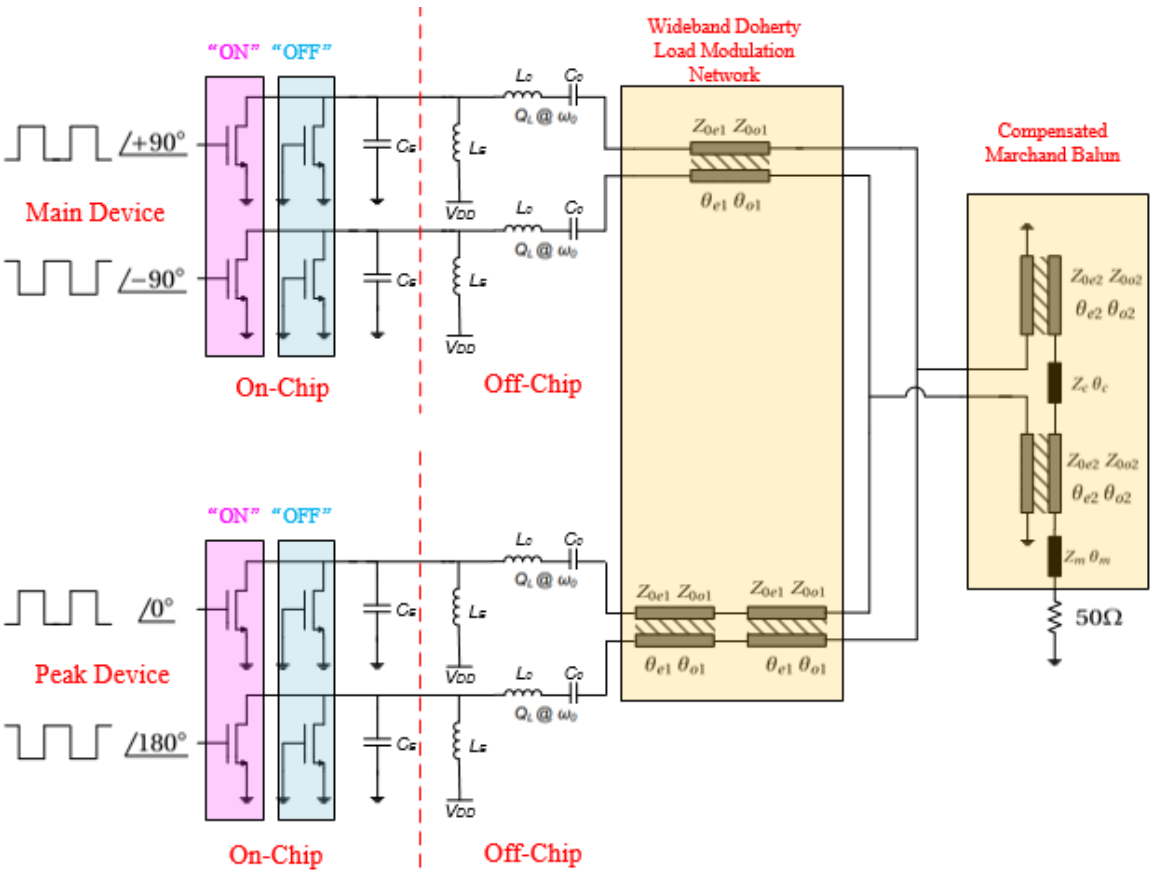


Figure 7.47: Simplified schematic for the proposed Doherty PA using differential Class E topology and re-entrant type coupled lines

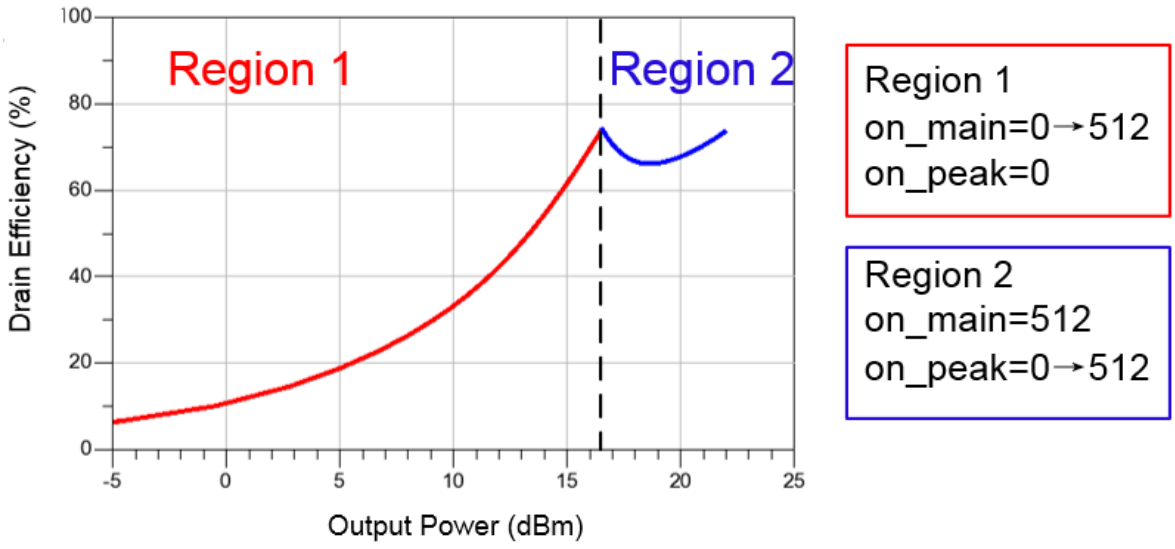


Figure 7.48: Characteristics of efficiency and output power performance for the Class E based Doherty PA in Figure 7.34 at center frequency $f_0 = 2.4GHz$

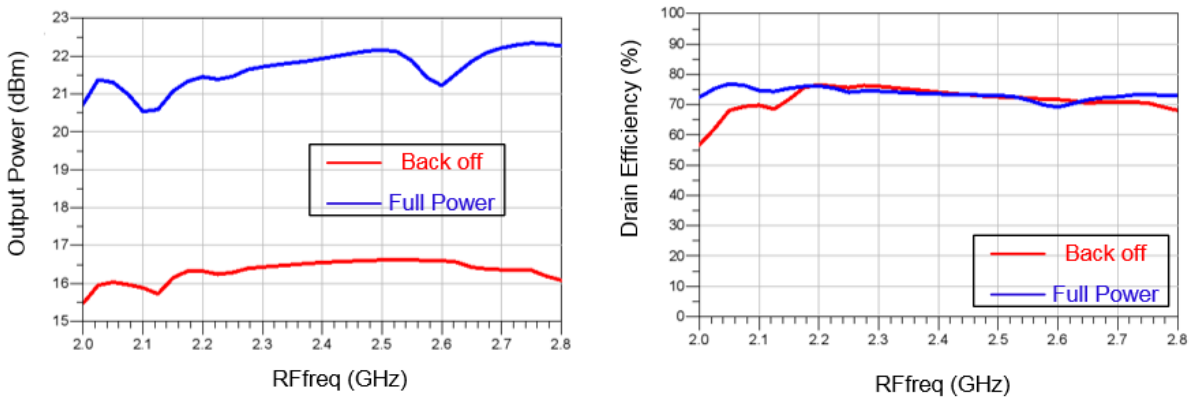


Figure 7.49: Wideband efficiency and output power performance for the Class E in Figure 7.34

Then, a Doherty PA is built on the basis of this Class E power amplifier. According to simulation results, a maximum output power of 22dBm with the efficiency above 70% at both full power and 6dB power back-off.

8

CONCLUSIONS AND RECOMMENDATIONS

8.1. CONCLUSIONS

Within this project, we aim to explore a new solution for Doherty PA with wide bandwidth and higher efficiency.

Prior to providing the solution how to achieve higher transmitter efficiency in the future, we first give an overview of different PA classes and the basic operation of the Doherty PAs. In general, linear power amplifiers, including Class A, AB, B and C are less efficient compared to their switch-mode counterparts (Class D and Class E). Thus a Doherty PA employing switch-mode Class E PAs instead of the conventional linear PAs can potentially provide a higher efficiency. Since Class E is very nonlinear in terms of the amplitude but linear in terms of phase, a novel digital polar architecture is introduced where the modulated signal is first split into a digital amplitude component to properly turn on and off the PA transistors arrays to control the effective on-resistance of the acive devices and a digital phase component (constant-envelope) which can be linearly amplified by the switch-mode power amplifier.

Wide bandwidth operation is achieved by two steps. The first step is to overcome the bandwidth limitations caused by the Doherty power combining network. After a study of the wideband frequency behavior for ideal two-way Doherty Power, it has been proven that the fundamental bandwidth limitation of a conventional DPA is its impedance inverter. For these reason, three different wideband impedance inverters are introduced, namely coupled-line impedance inverter, short-circuit $\lambda/4$ TL compensated impedance inverter and open-circuit $\lambda/2$ TL compensated impedance inverter, through which higher

average efficiency over a significant frequency range can be obtained. For the coupled line impedance inverter and short-circuit $\lambda/4$ TL compensated impedance inverter, the achieved improvement is at the expense of power capability and the bandwidth degradation at full power level. The open-circuit $\lambda/2$ TL compensated impedance inverter, however, has no bandwidth restriction at full power level if the impedance of the compensation line is chosen to be equal to the optimum loading impedance of the peaking device and proper input phase relations are enforced.

The second step is to find a broadband solution for the Class E device matching network. To address this issue, a differential parallel-circuit Class E PA is proposed where the balun plays a significant role in the entire load network. The first approach we explored to implement a balun is based on bondwire coupling, which can potentially provide significant benefits in terms of low losses because of their relatively high Q (on the order of 50) and large form factor. In chapter 5, a novel parallel-to-series connection bondwire-based transformer is proposed to allow simutaleous high coupling coefficient and large impedance transformation ratio. Unfortunately, when simply combining two transformers to form a balun, problems arise due to the significant amplitude and phase imbalance caused by the parasitics between the interconnect trace and the substrate. Alternatively, transmission line coupling can also be ultilised to implement a balun. In chapter 6, a compensated Marchand balun employing re-entrant type coupled lines is proposed. It starts with a study of the conventional Marchand balun. Based on this study, we know that a large even-mode and odd-mode impedance ratio (or a tight coupling) is benefical for a wideband design. Since the re-entrant type coupled lines can provide tight coupling without stringent dimensional requirements in circuit fabrication, they are employed here to implement a broadband balun. However, the employment of re-entrant type coupled lines introduces new problems due to their unequal even-mode and odd-mode phase velocities. To solve this problem, a compensated Marchand balun is given. Both the theory analysis and simulation results demonstrate that the amplitude and phase differences are greatly improved with a compensation line. A patent application based on this work is in preparation.

Chapter 7 provides detailed design and implementation considerations of the digital envelope modulator (on-chip) and the load network (off-chip) in the proposed digitally-controlled Doherty PA. It starts with the design of a broadband digitally-controlled Class-E power amplifier. According to the transistor-level simulation results, a maximum output power of 20dBm, and a high efficiency which is up to 80% from 2.0 GHz to 2.8GHz in the case of 0.6 supply voltage. Following this, a CMOS Doherty PA is developed on the basis

of the Class E power amplifier. The schematic-level simulation results show a maximum output power of 22dBm with the efficiency above 70% at both full power and 6dB power back-off.

8.2. FUTURE WORK

Several aspects of this project can be further extended to improve the performance ofthe DPA . Here several topics are listed that related to DPA design.

8.2.1. TOWARDS HIGH-POWER PAS

In this thesis, the standard 1.1V thin-oxide transistor from TSMC 40nm low-power CMOS technology is employed. Due to the low breakdown voltage, the supply voltage is restricted to ensure a safe operation, leading to a small output power. To allow a larger supply voltage, there are two ways. One is to increase the breakdown voltage by using high voltage MOS transistors instead, the other is to employ the cascoding topologye as shown in Figure 8.1 where the gate of the bottom transistor is driven directly with an RF input signal while the gates of the top transistor are AC grounded. Based on this cascoding topology, we can simply the digital envelope modulator as depicted in Figure 8.2. Instead of using an AND gate to combine the amplitude- and phase-modulated signals, the RF input signal (phase-modulated signal) is applied directly to the bottom transistors. By switching on or off the cascode voltages bx the on-resistance can be modulated.

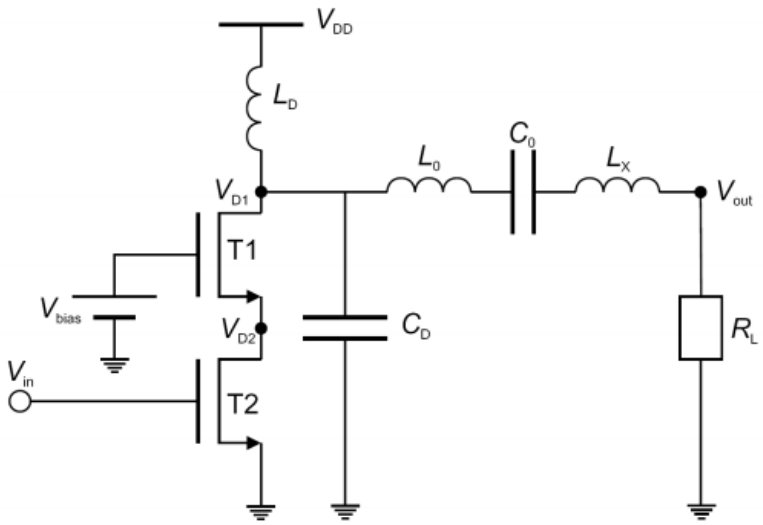


Figure 8.1: General schematic of a cascoded Class E PA [67].

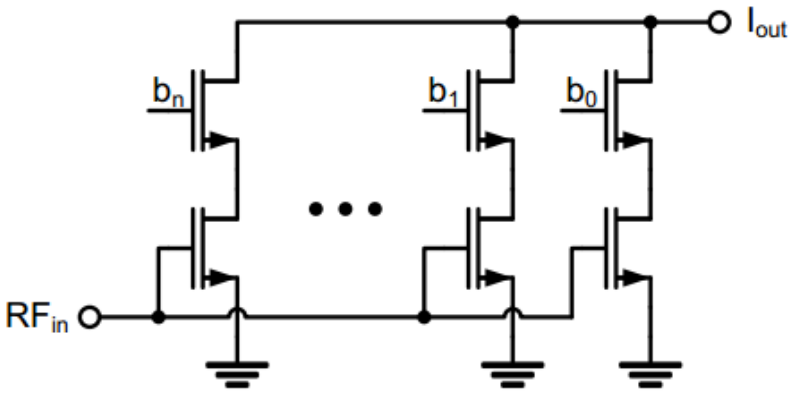


Figure 8.2: Digital envelope modulator based on cascaded devices

8.2.2. TOWARDS HIGHLY BALANCED BONDWIRE-BASED BALUNS

In chapter 5, one can observe that the amplitude and phase imbalance for the novel parallel-to-series connected baluns are not very good compared with the parallel-to-parallel single-turn topology. This is due to the large paracitic capacitance between the interconnect trace and the thin substrate. To improve at this point, a thicker substrate should be employed.

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