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Multistage Complex-Impedance Matching Network Analysis and Optimization

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***Abstract*—Some systems like RF energy harvesters have power transfer efficiency as one of the most important specifications. Therefore, the efficiency of the matching network, which affects the entire system's efficiency, plays an important role. When the impedance transformation factor between the antenna and its load is high, the matching network efficiency is decreased. In this paper we present the efficiency analysis and optimization of multistage matching networks at a single frequency using lumped components. Considering complex source and load impedances at each stage of the network, we show that it is possible to obtain better results than prior art.**

I. Introduction

Impedance matching networks are applied, for example, in communication circuits [1]–[3], DC-DC converters [4] and rectifiers [5]. They are employed to assure maximum power transfer when the impedance of the power source is not equal to the conjugate of the load impedance. Such networks are two-port circuits placed between source and load and that make them "see" their respective conjugate impedances.

Most analyses of matching networks assume no losses and power efficiency is not the goal [1]–[3]. But in some applications, like wireless energy harvesting and transfer, the power conversion efficiency is the most important goal and the energy losses in the matching network cannot be neglected. To realize a more efficient matching network, in some cases, a combination of several L-matches may be used [3], [6]. In [6], a method for obtaining high efficiency matching networks is presented, but only purely real impedances are considered. Not including complex impedances may discard the most efficient network from the solution space.

In this paper we propose a method to obtain efficient multistage matching networks considering complex load and source impedances at each stage of the network. To do that, we analyze, in Section II, the efficiency of the basic matching network, the L-match [1], for the general case of complex source and load impedances. In Section III, we define the efficiency of the multistage matching network and optimize it for maximum efficiency. In Section IV, we apply this optimization technique to some design examples. We conclude the paper in Section V.

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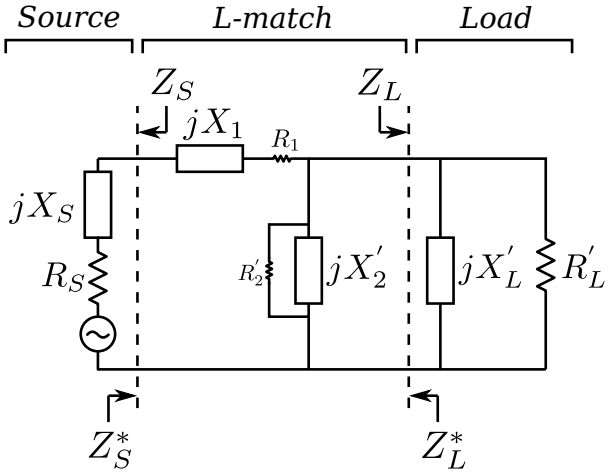

Fig. 1. Lossy L-match network matching complex impedances

II. Efficiency Analysis

In order to analyze the efficiency of a multistage matching network, we first analyze its basic building block, the L-match, which is shown in Fig. 1. In this circuit, the reactances X_1 and X_2 represent the inductors or capacitors used to transform the impedance and the resistances R_1 and R_2 represent their losses. Note that, throughout this paper, the prime symbol denotes the equivalent parallel values of the components at the frequency of interest, as $jX_L^{'} /\!/ R_L^{'}$ in Fig. 1 is the equivalent of $Z_L = R_L + jX_L$.

For high efficiency matching networks we may state, initially, that the resistors R_1 and R_2 are small enough so that they have negligible influence on the matching. We know that the transformation quality factor of the network must be equal to the series and shunt legs' quality factor when the impedances are matched [2]. For complex load and source impedances, as in Fig. 1, the quality factor is

$$Q = \sqrt{\frac{R_L'}{R_S} - 1} = \frac{|X_1 + X_S|}{R_S} = \frac{R_L'}{|X_2 /\!/ X_L'|}. \tag{1}$$

The input and output power are given by

$$P_{in} = I_S^2 R_S, \tag{2}$$

$$P_{out} = \frac{V_L^2}{R_L'}, \tag{3}$$

in which I_S is the RMS current on the series leg and V_L is the RMS voltage on the shunt leg. We can calculate the parasitic

resistors losses:

$$P_{loss,1} = I_S^2 R_1 = \frac{Q}{Q_1}\left|\frac{X_1}{X_1+X_S}\right| P_{in}, \tag{4}$$

$$P_{loss,2} = \frac{V_L^2}{R_2'} = \frac{Q}{Q_2}\left|\frac{X_2+X_L}{X_L}\right| P_{out}, \tag{5}$$

in which Q_1 and Q_2 are the quality factor of the components used in the L-match. The output power is equal to the input power minus the losses on the parasitic resistances:

$$P_{in} = P_{out} + P_{loss,1} + P_{loss,2}. \tag{6}$$

Knowing that the efficiency η is the ratio between output and input power and substituting (4) and (5) in (6), we get

$$\eta = \frac{P_{out}}{P_{in}} = \frac{1-\frac{Q}{Q_1}\left|\frac{X_1}{X_1+X_S}\right|}{1+\frac{Q}{Q_2}\left|\frac{X_2+X_L}{X_L}\right|} \tag{7}$$

Because the equations were defined for the up-converting L-match (Fig. 1), the impedances can be matched and (7) is valid when $R_L^{'} > R_S$. When this is not the case, we may swap Z_L and Z_S. This is the equivalent of using a down-converting L-match. With that in mind, (7) can be applied for any impedance transformation.

Equation (7) is similar to the one presented in [6], but we include the reactances of source and load to it. This addition is important to obtain better efficiencies in multistage networks as will be explained in the next section.

III. Maximizing Efficiency for Multiple-stage Matching

Using two or more L-matches to match the impedance, as shown in Fig. 2, may increase the efficiency. The multistage matching network gradually transforms the impedance while reducing the Q of each stage and balancing their losses. To do that, we must select the correct intermediary impedances $Z_{s,n}$ of the network. Doing this, the bandwidth of the matching network tends to increase because the Q is decreasing as the impedance changes from load to source in smaller steps [2].

The efficiency of a multistage matching network with N stages is defined by

$$\eta = \prod_{n=1}^{N} \eta_n(Z_{S,n}, Z_{L,n}), \tag{8}$$

in which η_n is calculated through (7) and its parameters are obtained with the selected source and load impedances of the n-th stage.

When the impedances are matched, the network presents $Z_{L,n} = Z_{S,n+1}^*$ at each section [3]. Therefore, we must only find the vector $Z_{S,n}$ with size $N-1$ that optimizes η, in which N is the desired number of L-match stages. Notice that $Z_{S,0} = Z_S$ is the source impedance and $Z_{S,N} = Z_L^*$ is the conjugate of the load impedance. We may find the best vector $Z_{S,n}$ by means of numerical optimization using (1)-(8) with specified Z_S, Z_L and quality factor of the components used in the matching network.

To optimize the network we use MATLAB's *Globalsearch* class [7], [8] with the *fmincon* local solver [9]. We need to apply a global optimization algorithm because this problem presents several local maxima. While using the *fmincon* solver it is important to set the solution constraints correctly. These are set as nonlinear constraints, checking if the vector of section impedances can be realized by the desired (up-converting or down-converting) L-match.

Running the optimization for several values of N, we find that there is a minimum number of stages N_{min} that produces the maximum achievable efficiency. Increasing N beyond $N > N_{min}$ does not decrease the efficiency because we consider intermediate complex impedances and the values of $X_{1,n}$ ($X_{2,n}$) can be equal to zero (infinity), which produces effectively the same network for greater values of N. The value of N_{min} increases with the impedance transformation, but it also depends on the imaginary part of the impedances, which may limit the number of stages.

A. Approximations

In order to reduce the computation time, we may apply some heuristics to simplify (8). For example, suppose that we want to match a capacitive load ($X_L < 0$) to an inductive or resistive antenna ($X_S \geq 0$), which is a common scenario. The best way to match is by using L-matches with series inductors and parallel capacitors (which can be seen from (1) and (7)). As a first, yet realistic, approximation, we may consider all quality factors constant for any value of inductance and capacitance, i.e., Q_1 is always equal to Q_{ind} and Q_2 to Q_{cap}. When using capacitors with Q_{cap} much greater than the inductors' Q_{ind}, we can approximate the efficiency equation to

$$\begin{aligned}\eta &= \prod_{n=1}^{N}\left(1-\frac{Q_n}{Q_{ind}}\left|\frac{X_{1,n}}{X_{1,n}+X_{S,n}}\right|\right)\\ &= \prod_{n=1}^{N}\left(1-\frac{|Q_n - Q_{S,n}|}{Q_{ind}}\right),\end{aligned} \tag{9}$$

in which $Q_{S,n} = |X_{S,n}|/R_{S,n}$ is the quality factor of the source impedance of each stage.

As a second approximation, we may consider only high efficiency networks, i.e., when the negative term in (9) is much smaller than 1. In this case, we may further approximate the equation to:

$$\eta \simeq 1 - \frac{1}{Q_{ind}}\sum_{n=1}^{N}|Q_n - Q_{S,n}|. \tag{10}$$

When using the *fmincon* solver to optimize (10), it is necessary to update the solution constraints to check whether the vector of section impedances can be matched by L-matches composed of a series inductor and a parallel capacitor.

B. Low-efficiency matching networks

When the efficiency of the matching network is low, the approximations above will not apply. Furthermore, (7) is not valid anymore because the parasitic resistances are now

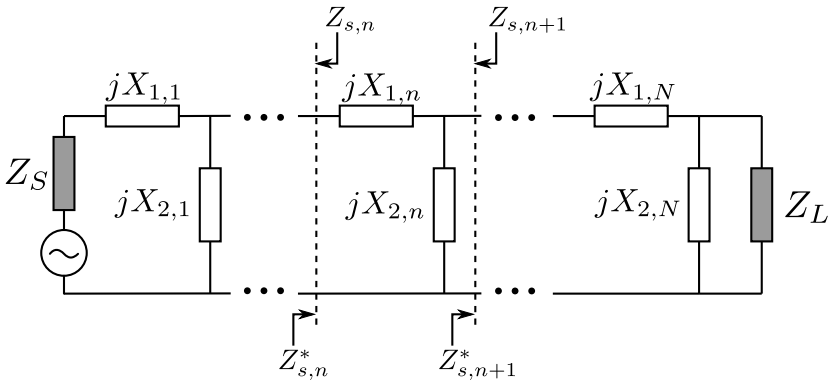

Fig. 2. Multistage impedance matching network

influencing the matching and consequently changing the current through the components and their losses. The efficiency equation for the L-match that uses series inductors is

$$\eta_n = 1 - \frac{|Q_n - Q_{S,n}|}{Q_{ind}} \frac{4R_{S,n}^2}{(2R_{S,n} + R_{1,n})^2} - |\Gamma_n|^2, \qquad (11)$$

in which $R_{1,n} = X_{1,n}/Q_{ind}$ is the inductor series resistance and Γ_n is the updated reflection coefficient, given by

$$\Gamma_n = \frac{R_{1,n}}{2R_{S,n} + R_{1,n}}. \qquad (12)$$

Note that (11) considers that the losses take the matching network away from the matched condition ($\Gamma_n \neq 0$) instead of properly matching source to load considering the losses. Despite the increased complexity of the calculations, optimizing this equation can be a better idea when dealing with lossy components or high impedance transformations, because the matched state may not present the best efficiency [10].

C. Simulations

Setting the source impedance to $50\,\Omega$, we apply the optimization for a large range of the real load impedances from $200\,\Omega$ to $50\,\mathrm{k}\Omega$. For this test, we consider the inductors to have a quality factor equal to 80 and the quality factor of the capacitors to be infinite. We simulate the matching network obtained through optimization and compare its efficiency to the one calculated through the high-efficiency approximation. The results are presented in Fig. 3 along with the minimum number of stages that produces the maximum efficiency N_{min}. As expected, the value of N_{min} and the difference between calculated and simulated efficiency increases with R_L (as the impedance transformation increases).

The variation of efficiency with number of stages for the case of $Z_S = 50\,\Omega$ and $Z_L = 25\,\mathrm{k}\Omega$ is presented in Fig. 4. The efficiency increases with N, but for bigger values of N its increase may not justify the use of more components. For example, from $N = 6$ ($\eta = 91.85\%$) to $N = 7$ ($\eta = 91.98\%$), the increment in efficiency is only 0.13%. At $N = 1$, for which the efficiency is lower, we can observe that the approximation result presents a larger error, but for bigger N the error is reduced (down to 0.34% for $N = 7$). Fig. 4 shows that it is possible to obtain much higher efficiencies by

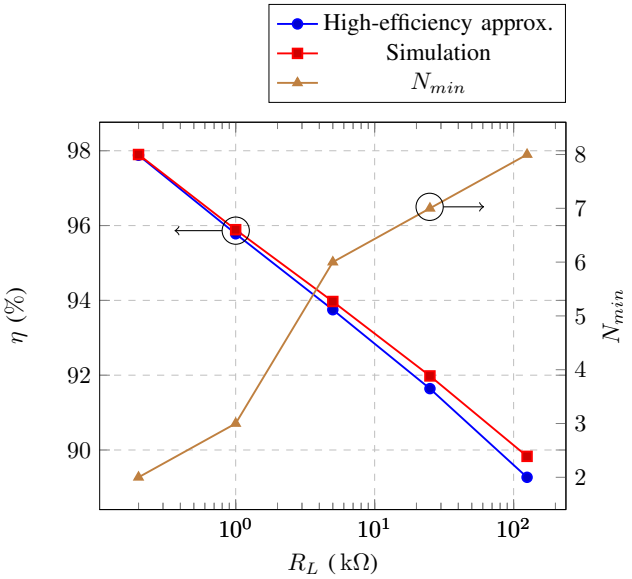

Fig. 3. Comparison of simulation and approximation results along with number of stages to obtain maximum efficiency

using a multistage network while optimizing its intermediate impedances, when compared to a single stage network.

In Fig. 4 we also show how the 3-dB bandwidth varies with the number of stages. In this analysis we consider the frequency of interest equal to 1 GHz. Due to the reduction of impedance transformation between each stage, the bandwidth increases from 45 MHz, for $N = 1$, to 379 MHz, for $N = 7$.

D. Comparison with previous art

In Fig. 5 we show the intermediate impedances of the matching network designed using the method presented in [6], which uses only real intermediate impedances, and using the method proposed in this work. We compare the methods in one case in which we have only real source and load impedances ($Z_S = 10\,\Omega$ and $Z_L = 3\,\mathrm{k}\Omega$) and in another case in which we have complex source and load impedances ($Z_S = 10 + j50\,\Omega$ and $Z_L = 2770 - j3772\,\Omega$). The impedance levels of the second case can be found in the problem of matching a rectifier to an inductive antenna.

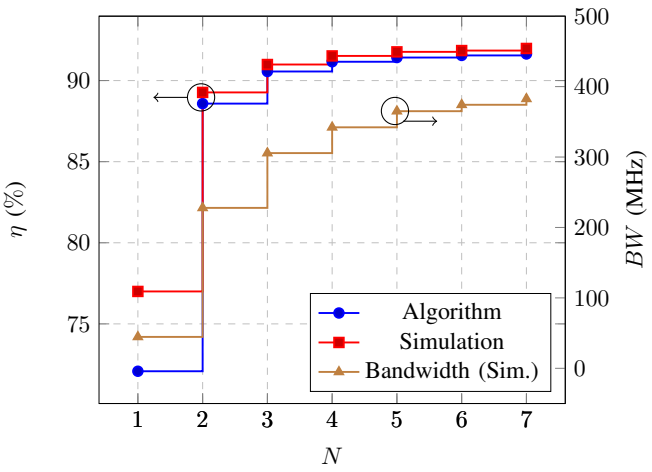

Fig. 4. Efficiency and bandwidth of matching networks varying the number of stages for $Z_s = 50\,\Omega$ and $Z_l = 25\,\mathrm{k}\Omega$

In the first case, for which the impedance transformations are shown in Fig. 5(a)-5(b), our method presents a reduction of 5% in losses (as the efficiency increases from 91.45% to 91.88%) for $N = 3$. The work in [6] does not introduce a guideline to match complex impedances. Thus, for the second case, we make the matching network absorb the imaginary part of the load and source impedances while applying the method that considers real impedances, which is possible for $N = 2$ or less. In this case we obtain a reduction of 1.8% of the losses (as the efficiency increases from 93.97% to 94.08%) by using intermediate complex impedances with the same number of stages. In Figs. 5(c)-5(d), the Smith charts are normalized to $500\,\Omega$ to facilitate the visualization. Increasing the number of stages to $N = 6$, we obtain a 95.93% efficiency with the proposed method. When increasing the number of stages with the previous method [6], a drop in efficiency occurs. All the results above are computed from simulations.

IV. Design Examples

In this section, we apply the proposed method to two practical examples. In the first one, we match a rectifier to an electrically small loop antenna. And in the second example, we use the method to assist us in selecting the best rectifier-matching combination considering a fixed antenna impedance. In both examples, we consider the operating frequency to be $403.5\,\mathrm{MHz}$, which is the central frequency of the Medical Implanted Communication Service (MICS) band. We optimize the networks using (11), the low-efficiency equation, because the large impedance transformations in these cases produce low-efficiency matching networks that are not well described by (10). The rectifiers in these examples are designed in a standard CMOS $0.18\,\mu\mathrm{m}$ technology.

A. Matching a rectifier to an electrically small loop antenna

Fig. 6 presents the power conversion chain used in this example. We use an electrically small loop antenna as the power source. Its diameter is equal to $2\,\mathrm{cm}$ and its impedance is equal to $6.5 + j116\,\Omega$. A differential-drive rectifier [11] does

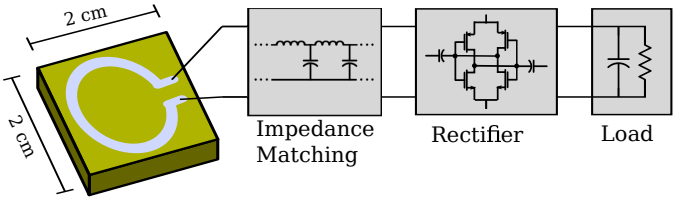

Fig. 6. Block diagram of the power conversion chain using an electrically small antenna

the RF-DC conversion and its load is set to the optimum value at the input power $P_{in} = -28\,\mathrm{dBm}$.

We compare two approaches to design the impedance matching network: one in which the network will be integrated together with the rectifier on a single chip and the other in which the network will be off-chip. The difference between both cases is the location of the pads (as its parasitic capacitance affects the source or load impedance) and the quality factor of the inductors. For both cases we consider only L-matches formed by a series inductor and a parallel capacitor, as shown in Figure 6.

For the off-chip matching network, the rectifier input impedance, considering the pads' parasitic capacitance, is $122 - j3270\,\Omega$. Supposing that we will use inductors that have $Q = 80$, we now have all the necessary data to run the optimization algorithm. The results show that the optimum matching network has 2 stages and an efficiency equal to 76.6%.

For optimizing the on-chip matching network we must embed the pad parasitics into the antenna impedance, which results in a $7 + j120\,\Omega$ source. Without the pads parasitics, the rectifier input impedance is now $4.3 - j22.7\,\mathrm{k}\Omega$. Considering integrated inductors with $Q = 8$, the optimization results in a matching network with 3 stages and an efficiency equal to 52.6%. By iteratively running the algorithm through increasing values of Q, we find that for $Q \geq 21$ we obtain higher efficiency than when we use an off-chip matching network with $Q = 80$. Since it is difficult to obtain such large values of Q for integrated inductors, the best solution in this case is to use off-chip impedance matching.

It is important to notice that the losses in the matching network will require a higher available power P_{av} at the antenna interface in order to provide the defined $P_{in} = -28\,\mathrm{dBm}$ at the rectifier input. A change of P_{in} produces a change of the rectifier input impedance and, consequently, a change of the matching network efficiency. Thus the available power must be set to $P_{av} = P_{in}/\eta_{match}$.

B. Choosing the best rectifier-matching combination

While selecting the transistors' width on a differential-drive rectifier, using small values may increase the efficiency as shown in Tab. I. This happens because the input voltage amplitude increases when the equivalent series capacitance decreases, making the series resistance of the switches smaller (counteracting the width reduction effect on it). However, the matching network efficiency will be reduced because the impedance transformation increases as the transistor width

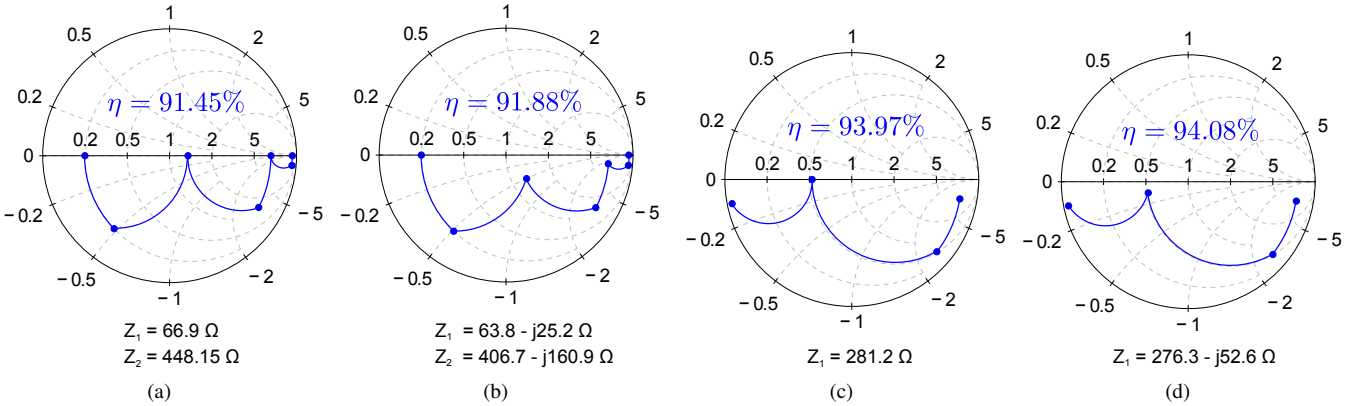

Fig. 5. Comparison of the method presented in [6] (a, c) with the proposed method (b, d) for two cases: matching real impedances (a, b) and matching complex impedances (c, d). Impedance values of intermediary nodes (between L-matches) are shown below the Smith charts

TABLE I
COMPARISON OF POWER CONVERSION CHAINS FOR VARIOUS RECTIFIER TRANSISTOR WIDTHS

W_n (μm)	η_{rect} (%)	Z_L (Ω)	η_{match} (%)	η_{total} (%)
1.5	71.1	$68 - j2860$	62.4	44.3
3	68.6	$74.4 - j2731$	65.7	45.1
6	62.7	$74.3 - j2506$	67.8	42.5
12	50.5	$64.5 - j2167$	68.0	34.3

becomes smaller. Therefore, there is a transistor width that will present the best rectifier-matching combination. For our case, this happens when the width of NMOS transistors W_n equals $3\,\mu$m as can be seen in Tab. I.

The data in the table was obtained using an antenna impedance $Z_s = 50\,\Omega$ and input power $P_{in} = -28\,\text{dBm}$. The widths of the PMOS transistors are set as $W_p = 2.7W_n$. We consider the matching network to be off-chip using inductors with $Q = 80$. We also consider the parasitic capacitance of the pads in simulations to find the rectifier input impedance Z_L and efficiency η_{rect}. For those impedance values, all matching networks have best efficiency when the number of stages $N = 2$.

It is important to notice that the values for the number of stages selected for each example above are set to their respective optimum value N_{min}. By increasing the number of stages and running the optimization the result becomes effectively the same as obtained for $N = N_{min}$, as explained in Section III.

V. CONCLUSION

The efficiency analysis of an L-match and of a generic matching network formed by several L-matches were presented, both considering complex load and source impedances. Based on these analyses, we developed a design method based on numerical optimization, which takes as input the source and load impedances and the quality factor of the components. Comparisons of the estimation and simulation results validated the method. We have shown that it is possible to obtain better results than the previous state-of-the-art method. In cases when there is little flexibility in selecting the source impedance or when the impedance transformation is high, our matching method is especially useful. The method is limited by the global optimizer algorithm used, since there are many local maxima for the efficiency. It is also important to notice that even if we have better efficiency when increasing the number of stages of the matching network, it may not be the best solution for some cases due to the increase of the number of components and thereby the cost and area, and the extra losses due to the physical implementation of these additional stages may even reduce the total efficiency.

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