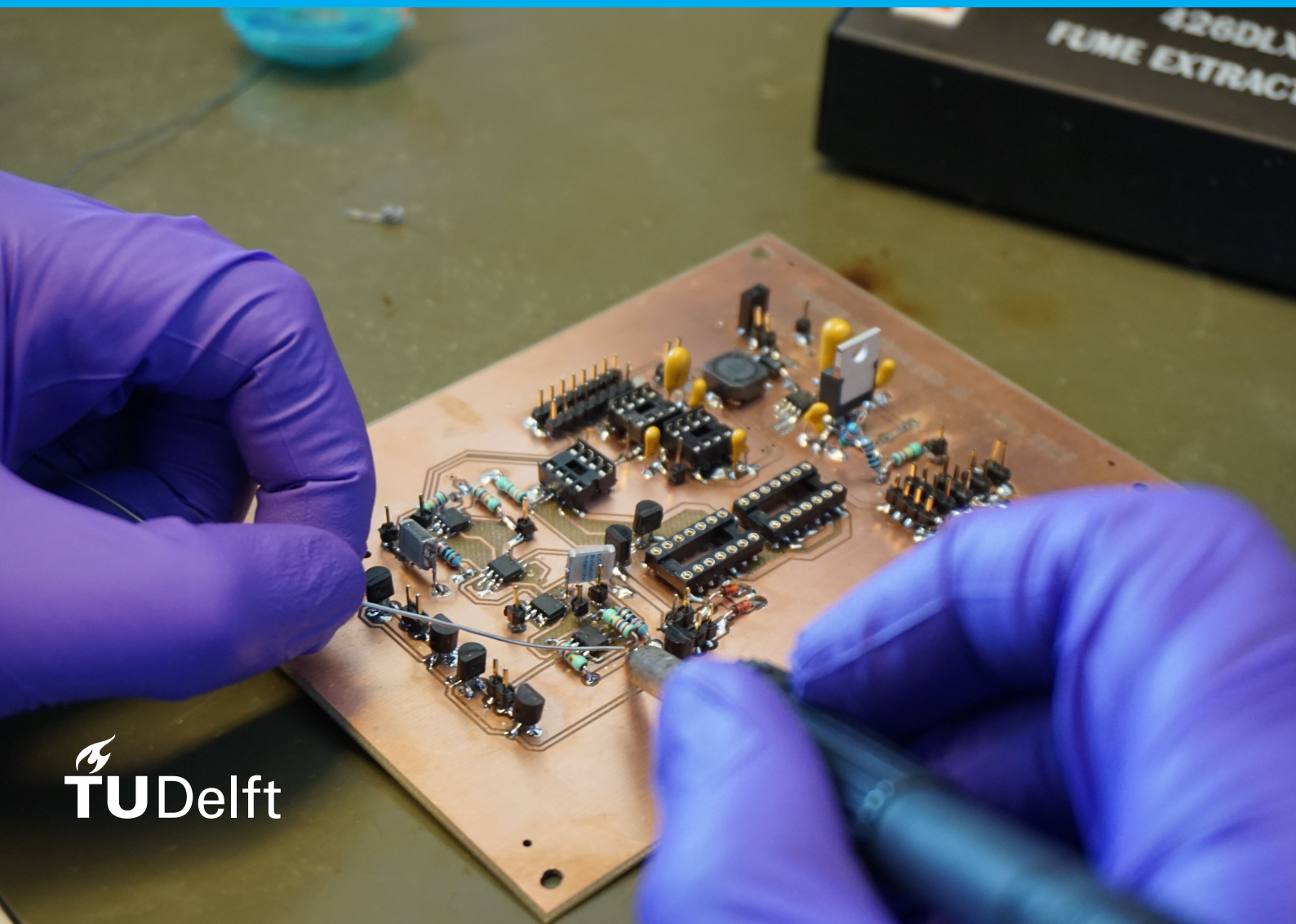
Bachelor Thesis

Arbitrary Waveform Generator

for a High Frequency Arbitrary Waveform Neural Stimulator

T.V.A. Salden & S.J.H. Verkleij

REValUE Project



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Arbitrary Waveform Generator for a High Frequency Arbitrary Waveform Neural Stimulator

by

T.V.A. Salden & S.J.H. Verkleij

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Abstract

The goal of this Bachelor graduation project is to make an electrical stimulator that can be used to help people empty their urinary bladder. Patients that are unable to relax the urethral sphincter are most commonly treated by mechanically emptying the bladder or by sacral root stimulation where the roots are selectively cut.

The stimulator to be made must send a high-frequency signal that cancels the blocking of the urethral sphincter. This method should be able to empty the bladder without the use of mechanical devices or selectively cutting nerves.

The whole project is divided into three parts: Control and Interface, Arbitrary Waveform Generator and Safety Module. These parts have been performed by three different subgroups. In this report, the Arbitrary Waveform Generator is discussed. The other parts are explained in the respective reports [1, 2].

The requirements for this waveform are to generate a biphasic pulse with frequencies ranging from 1 to 15 kHz. The amplitude range of this pulse should be adjustable between 0 and 10 mA and the pulse width and interphase delay should be fully adjustable. In order to generate this signal, a power management system was necessary. In addition to the power management system, the LPC1343 microcontroller was chosen to control the system. One of its functions is to control a DAC by communication using the SPI protocol. The DAC can linearly control the output voltages between 0 and the offered reference voltage, in this case 3.3 V by sending 10 bits of data. Using a voltage to current converter, made by the Interface and Control subgroup, the output voltage is converted to a current between 0 and 10 mA [1]. Three additional signals from the microcontroller operate an H-bridge. This is a switching circuit that is able to direct the generated current through a load. Using a timer and four interrupt moments, the three signals are generated that can make a cathodic pulse, anodic pulse and can disconnect the current source.

The chosen DAC has a close to ideal behavior. Therefore, the conversion from the microcontroller to the voltage to current converter is very precise. The H-bridge works best at low frequencies. At 1 kHz, around 2% of a total pulse of 127.2 μs is needed to reach 63% of the cathodic or anodic amplitude. At high frequencies, the time increases. At 15 kHz, 24% of a total pulse of 8.4 μs is needed to reach the amplitude.

Preface

The graduation project marks the end of a three-year bachelor Electrical Engineering. While progressing through the program, a lot of theoretical and a little practical knowledge has been passed on to the students. From the first encounter with Ohm's law to complex electromagnetic computations and from a first measurement with an oscilloscope to designing a game on a chip, the knowledge increased and a intuition for anything related to electricity was born.

This knowledge and intuition connects electrical engineers by the way they think about designing or working with circuits. There is, however a third facet that is really important to the engineers, which is experience. Only with experience, engineers can reproduce or combine circuits they have seen in the past or understand complex systems without having to compute every part of it.

As a final test, students from Electrical Engineering that are filled with a lot of theoretical knowledge, have to perform the very practically aimed bachelor graduation project. After completion, they do not only have theoretical knowledge and intuition, but also have gained a little experience. Equipped with this combination, they graduate the program.

However, as Wouter Serdijn, the supervisor of our project told us, the more you learn, the more you know what you don't know.

Throughout this project, this became especially apparent, since there were a lot of new topics to learn about. Therefore, we like to thank our supervisor, Wouter Serdijn, for giving us good feedback, advice and new ways to think about the designs.

In addition, we want to thank Bertil Blok for the very interesting project proposal, the time he put into it for us and the feedback he gave on our work.

Next, we like to thank Ali Kaichouhi for technical help during the project and the secretary Marion de Vlieger for being the contact of the department for us.

We like to thank Gerard Baquer for providing us with a lot of insight in the problem and stimulation parameters. As a master student working on simulations of the same subject, he was able to make us understand what parameters were important.

Lastly, we would like to thank the other two subgroups for working together at this project. Sometimes the borders of the different groups faded, but the collaboration was optimal. Every day at 8:45 everyone was present and driven to continue working. It was a very educational period and we are very satisfied with the project.

T.V.A. Salden & S.J.H. Verkleij
Delft, June 2018

Contents

1 Introduction

This project is done in cooperation with two other groups [1, 2], all groups concern the same problem but work on different sub modules for this project. Therefore, the project introduction, problem definition and project objective found in the theses are the same.

1.1. Introduction to the REValUE Project

Millions of people have difficulty in emptying their urinary bladder [3]. Well-known causes are Spinal-Cord Injury (SCI) and Multiple Sclerosis (MS), but many more non-neurological patients suffer from similar problems without an obvious cause. Normally, the urethral sphincter is continuously contracted and only a few times per day relaxed during voiding. This relaxation is controlled by a switch in the brainstem [4]. When the brainstem switch is not activated, there is no relaxation of the sphincter and, thus, no voiding and the sphincter remains contracted and closed. Patients in retention cannot void because they are unable to activate the brainstem switch.

1.1.1. Problem Definition

The most common treatment is to mechanically empty the bladder with intermittent self catheterization or an indwelling catheter as there is no treatment to restore the voiding function [5]. Using a catheter results in infections, pain and excessive healthcare costs [6]. Electrical stimulation to improve bladder function has been utilized with varying success [7]. The Bindley system has been implanted which uses sacral root stimulation where the roots are selectively cut. This method is irreversible and causes total absence of erections. The rhizotomy and implantation take more than five hours of surgery and both urologists and neurosurgeons are necessary for the operation.

Sacral nerve stimulation is an often used technique for bladder voiding in patients without SCI [8]. This method only needs percutaneous access to the nerves, significant reducing the surgery time. The downside of this method is that the urethra is still closed, resulting in a high bladder pressure and an increased chance that urine flows back into the kidneys.

1.1.2. Project Objective

In this project, a high frequency stimulator is developed. The high frequency signal cancels the blocking of the urethral sphincter. A study has shown effective emptying of the bladder of cats by blocking the pudendal nerves [9]. Besides high frequency stimulation, the project is aimed to develop a low frequency stimulator as well, to stimulate the ventral roots, causing bladder contraction.

For this goal, a Bachelor Graduation Project group from Electrical Engineering was formed. The objective of this group was to develop a high frequency, arbitrary-waveform, neural stimulation device that offers efficacious, yet safe, stimulation of the pudendal nerves. This can

be used to focus on relaxing the urethral sphincter by reversible, bilateral, high frequency blocking of the pudendal nerves to enable voiding. After emptying the urinary bladder, the blockage is stopped and the sphincter resumes its normal closure function during continence.

This group of six people is divided in teams of two. The first team focuses on the interface and the control of the device. The second team develops the waveform generator circuit and a third team makes the safety system of the waveform generator.

1.1.3. State-of-the-art Arbitrary Waveform Neural Stimulator Analysis

The state of the art neural stimulators are integrated circuits because they have restrictions on the power and the size of the device. Most arbitrary waveform generators are however made with discrete components [10]. Furthermore, most state-of-the-art neural stimulators have been made for testing and implementation on small animals and not for humans [10, 11]. When there are no power and size limitations the arbitrary waveform generators are often implemented using a current controlled stimulation [10].

Most state-of-the-art stimulators are based on low frequency stimulation (1-100 Hz). Low frequency stimulation can produce neural response, while high frequency stimulation results the blockage of these neural responses [12]. High frequency stimulators do exist for other applications than pudendal nerve stimulation, which this project is focussed on [13]. The stimulator designed in this project will stimulate at both high and low frequency, which does not exist currently.

At the start of the research, the Medtronic 3625 Test Stimulator has been used for arbitrary low frequency bladder stimulation in the hospital. The Test Stimulator is a voltage controlled device and has the following characteristics: amplitude range 0-10 V with a $\pm$0.5 V accuracy and a variable pulse width between 50-1000 μs [14].

1.2. Arbitrary Waveform Generators State-of-the-art

There are many present-day medical procedures that rely on electrical stimulation. Due to a lot of research in this field, a lot of different manners of injecting charge into the body have been tested. Usually, a repeating charge, voltage or current steered pattern is used to generate or block an action potential. The most often used waveform for stimulation is a rectangular pulse [15–22]. Other generators use Gaussian or sinusoidal waveforms for more power efficient stimulation [12, 23–26]. Using these non-constant stimulation waveforms makes some aspects of the system more complicated, such as the charge balancing system.

The waveform is not the only parameter that can be altered. There are different modes of operation of which the most interesting for this project are monopolar and bipolar. Monopolar stimulation uses the devices' metal case as the return electrode, while bipolar uses one of the other electrodes on the lead as the return electrode. Bipolar stimulation is more focused than monopolar stimulation and reduces the size of artifacts [27]. Both modes are effective, however in some cases, the bipolar configuration is much more efficacious [26].

Another alteration can be found in the usage of monophasic or biphasic stimulation. Monophasic stimulation waveforms only send out cathodic pulses and are only used for low frequency stimulation [20, 25, 26]. Biphasic stimulation usually starts with a cathodic pulse which is followed by an anodic pulse to cancel the charge accumulated during the cathodic phase. Biphasic stimulation is used for low frequency [17, 18, 28, 29] as well as high frequency stimulation [16, 21, 25, 29, 30]. Monophasic stimulation waveforms are more efficacious than biphasic waveforms, since the second stimulation phase can (partially) cancel the effect of the first stimulus [31]. However, monophasic pulsing causes the greatest shift of the electrode potential during pulsing away from the equilibrium potential, thus causes the most accumulation of unrecoverable charge and lead to irreversible electrochemical processes and

thus causing damage to the tissue and electrode [20].

It has been found that low frequency stimulation can produce neural response, while high frequency stimulation results the blockage of these neural responses [12]. The border between high and low frequency is usually considered to be 100 Hz [26, 27]. The typical frequency range for high-frequency stimulation of the pudendal nerve is from 1 to 10 kHz [26], while also other ranges such as 1 to 30 kHz [12] and 6 to 10 kHz [25] are used.

Injecting charge into the body can be charge, current or voltage steered. In many cases, a current controlled signal is preferred because more exact knowledge of charge applied [18, 22]. Using voltage controlled stimulation, the injected charge and stimulation intensity will depend on the load [31]. The main advantage of voltage driven is the 2x-3x higher energy efficiency of the stimulator [32]. Also, charge steered stimulators based on switched-capacitor techniques have been proposed [33], which combines the power efficiency of voltage-controlled simulators and safety and controllability of current-controlled stimulator in a simplified design to decrease the size and power requirements of the stimulator.

1.3. Thesis Outline

The outline of this thesis is as follows. Chapter 2 lists all requirements for this waveform generator. An overview of the entire neural stimulator and of the waveform generator is given in chapter 3. This chapter also includes a comparison between different topologies of the waveform generator.

The different subsystems are described in more detail in the later chapters. Chapter 4 describes the power management system. This includes the design, implementation and measurements. The selection of the microcontroller, together with a description of the code is included in chapter 5. Chapter 6 then describes the selection, implementation and measurements Digital to Analog Converter (DAC). The description about the H-bridge is included in chapter 7, which also includes tests of the entire system.

Chapter 8 includes the discussion on the research. The project is concluded in chapter 9 which also describes whether the designed system has met the requirements and which includes recommendations for future work.

2

Program of Requirements

The goal of the REValUE project is to deliver a testing device which can determine the optimal parameters for urinary stimulation. The program of requirements is divided into two parts. First, the general requirements are presented, which hold for the entire testing device. Section 2.2 lists the requirements for the arbitrary waveform generator subgroup. The general requirements are the same for all three subgroups, so they are included in the other two reports as well [1, 2].

2.1. General Requirements of the Project

The general requirements of the total system will not be further discussed in this report during the design steps, they are however always kept in mind during the design process. The following general requirements are set for the project:

- The device should have 2 identical connections for 2 extension cables which are connected to a lead. The lead has an array with 4 electrodes (Lead used is Medtronic Model 388928).
- The leads must be connected with an extension cable which should fit the connectors of the device.
- The device must be able to stimulate on all possible terminals of the lead.
- The device must support monopolar and bipolar stimulation.
- The device must operate outside the sterile field around the patient.
- The device must not cost more than €5,000.
- The device must not be larger than $0.5 \times 0.5 \times 0.3$ meters (length x width x height).
- The device must not weigh more than 10 kg.
- The components of the device must ensure a lifetime of at least 6 months.
- The device must be able to operate between 10° C and 40° C.
- The internal temperature of the device must be kept in a range where the device is still fully functioning (so where the device meets all specified requirements).
- The device must not create sounds which exceed 40 dB [34].
- The device must be made from commercial off-the-shelf components.

2.1.1. Output Quantity

A current waveform has to be available at the output. This is done either by the waveform generator or converted from a voltage waveform by a separate section later in the design.

2.1.2. Requirements to Apply Injected Charge

Primary requirement
The generated waveform must be current driven. The device must independently control the current through two (implantable) leads with both four electrodes. The current through all electrodes must be controlled independently in two different channels.

Secondary requirement
Besides a current driven waveform, the device must be able to generate a voltage driven waveform.

2.2. Requirements for Waveform Generation
The requirements for the arbitrary waveform generator are specified by the client and are listed here.

2.3. Functional Requirements
Functional requirements define the purpose of the arbitrary waveform generator and the tasks it is expected to perform. The requirements are split up into primary and secondary requirements. The primary requirements have the highest priority. When all primary goals are met, the secondary goals can be taken into account.

Primary Functional Requirements
Waveform
The waveform generator must be able to generate a biphasic block waveform.

Adjustable Parameters
The parameters of the biphasic waveform that must be adjustable are the

- frequency of the pulse;
- pulsewidth;
- interphase delay; and
- amplitude

as defined in Figure 2.1.

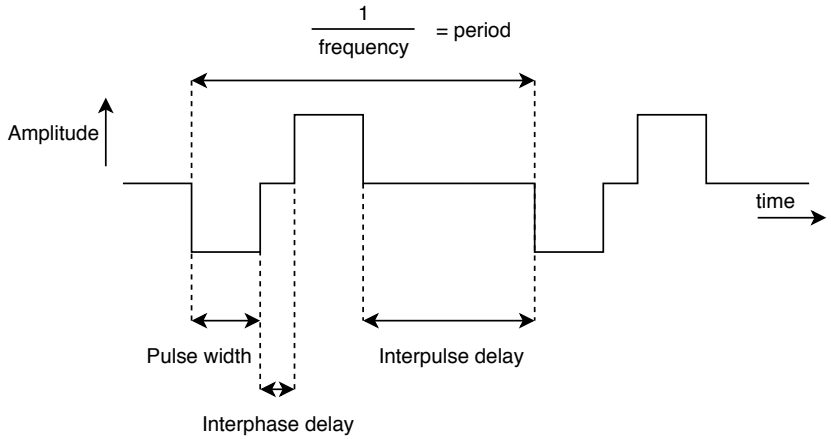


Figure 2.1: Adjustable parameters of the biphasic waveform.

Secondary Functional Requirements
Monophasic waveform
Besides a biphasic waveform, the device must be able to generate a monophasic waveform. In case of a monophasic waveform only the frequency, pulse width and amplitude must be adjustable.

Other types of waveforms
Besides a block waveform, the device must be able to generate different other types of waveforms. Research will be done to determine the required waveforms. The options for investigation are sinusoidal, exponential, delta pulse and sawtooth waveforms.

2.4. System Requirements
System requirements are specific technical requirements on the functioning and performance of the arbitrary waveform generator.

Primary System Requirements
High frequency stimulation
The frequency of the high frequency stimulation must be adjustable between 1 kHz and 15 kHz with linear increments of 1 kHz. The maximum deviation of the frequency must be ± 0.5 kHz.

Pulse width and interphase delay
The pulse width of the stimulation must be adjustable. The sum of the pulse width of the cathodic pulse, interphase delay and pulse width of the anodic pulse must not be longer than the period of the waveform. The pulse width and interphase delay should be adjustable independently.

Current amplitude
When the output of the waveform generator is a current driven waveform, the current amplitude must be adjustable. The range must be from 0 to 10 mA. The system has to be able to step through this amplitude range with steps of maximum 0.1 mA.

When the output of the waveform is a voltage driven waveform, it must be converted to a current waveform in a later stage with the same amplitude range as above.

Safety of the generated pulses
The device must leave less than 30 $\mu C/cm^2$ of charge in the body after each biphasic stimulation pulse.

Secondary System Requirements
Low frequency stimulation
Stimulation on low frequency is a secondary requirement. The output frequencies of this lower range must be between 5 and 20 Hz. In this range, the system must be able to make steps of 1 Hz.

Voltage amplitude
When making use of voltage driven stimulation, the voltage range must be from 0 to 10 V. The system has to be able to step through this amplitude range with steps of maximum 0.1 V.

3

System Decomposition

This chapter gives an overview of the entire neural stimulator, after which the system overview of the arbitrary waveform generator is explained in section 3.1. The detailed system overview of the entire neural stimulator is presented in section 3.2. The considered alternative topologies for the arbitrary waveform generator are discussed in section 3.3.

Figure 3.1 shows the high level block diagram of the entire neural stimulator. The neural stimulator is controlled by input signals, which are handled by the interface subsystem. The input signals are used by the waveform generator subsystem to generate the desired waveform. This is passed through to the safety module in order to check if the waveform is safe before stimulating the patient. The safety module gives feedback to the waveform generator and the interface when a not safe waveform is blocked. The waveform generator then stops the stimulation and the interface gives visual feedback. The settings of the stimulator are also shown as visual feedback.

The safe waveform is passed through from the safety module to the electrode switches. These switches are used to stimulate with the desired electrodes. The electrode switches are part of the interface and are therefore connected. The arbitrary waveform generator in the blue block together with the power management of the stimuator is described in this report.

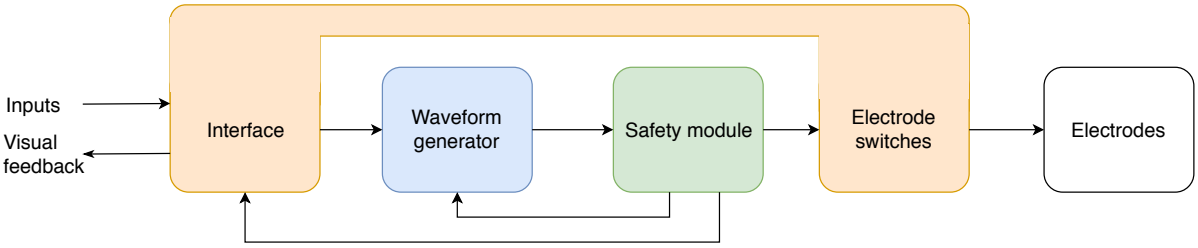


Figure 3.1: Block diagram of the entire neural stimulator.

3.1. System Overview of the Arbitrary Waveform Generator

An overview of the arbitrary waveform generator is shown in the block diagram of Figure 3.2. The device is powered by a 9 V battery. This voltage is regulated to a stable 3.3 V, 5 V, 6.5 V and 15 V to power all subsystems. The microcontroller uses the inputs of the interface subsystem to generate the waveform. A current with the desired amplitude is generated by using the DAC and the voltage to current converter. The latter one is made by the Interface and Control subgroup in order to have a better task division [1]. The constant current is then converted into a biphasic current by the H-bridge. Feedback from an error signal combiner is used to correct or stop the stimulation when necessary.

To guarantee safety of the stimulator, the device will be powered by a 9V battery rather than the 230 V power outlet. The voltage from the mains is dangerously high. If there is a shortage or other fault, the voltage over the electrodes could possibly be 230 V. Next to this, the mains voltage can be unpredictable in very rare cases, like during lighting storms. If this happens, the stimulator could behave unpredictable as well. In addition, the generated signal is sent through an independent safety system that checks if the device is operating using safe signal levels. A more detailed explanation of this system is made by the Safety Module subgroup [2].

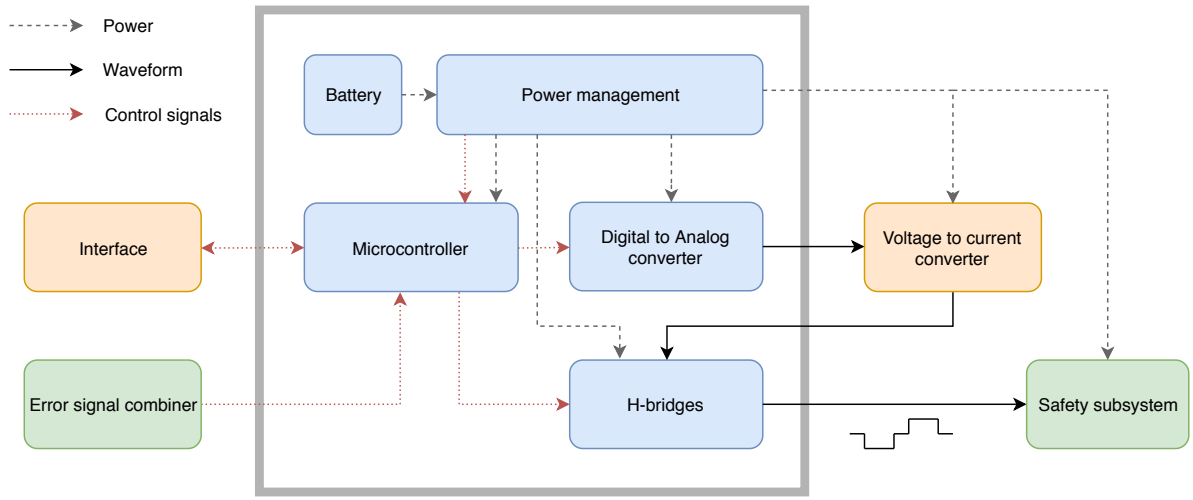


Figure 3.2: Block diagram of the arbitrary waveform generator subsystem.

3.2. System Overview of the Complete System

Figure 3.3 shows the detailed block diagram of the full neural stimulator. It can be seen that the power management provides the power for all subsystems. The colors of the blocks show which subgroup has the responsibility of designing which part of the device. The blue blocks are designed by the arbitrary waveform generator subgroup and described in this thesis. The orange blocks are designed by the interface and control subgroup [1]. The safety subgroup has the responsibility over the green blocks [2].

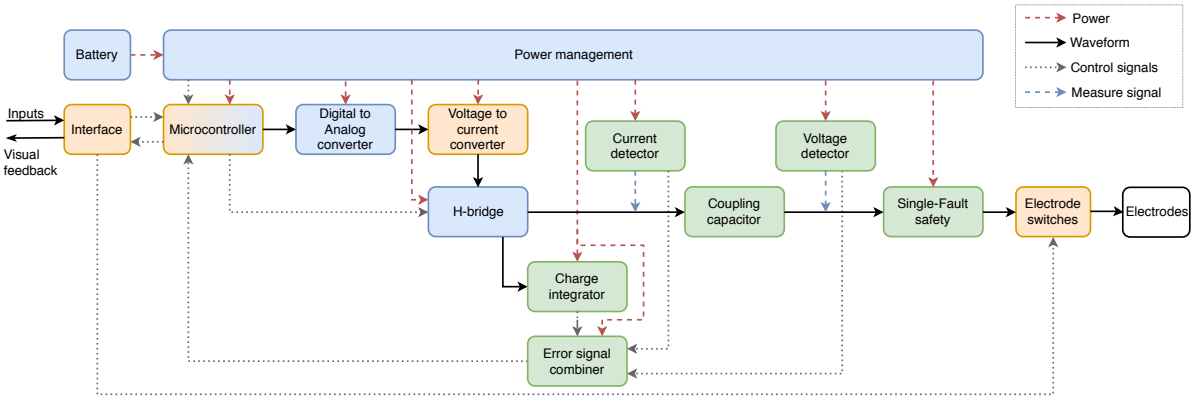


Figure 3.3: Block diagram of the complete neural stimulator. The blue blocks are designed by the arbitrary waveform generator subgroup. The orange blocks are designed by the interface and control subgroup [1]. The safety subgroup has the responsibility over the green blocks [2].

3.3. Comparison of Topologies to Generate a Biphasic Waveform

In section 3.1, the chosen topology to generate a biphasic waveform has already been highlighted. By using a DAC, a correct voltage level is generated. A voltage to current source transforms this voltage level to the correct stimulating current and an H-bridge creates a biphasic signal from this.

The reason a biphasic pulse is used is because during The negative part of the pulse (Cathodic), an action potential is either generated or blocked by injecting the negative charge close to the nerve. During The positive part of the pulse (Anodic), the charge balance is restored.

The previous discussed method of generating a biphasic pulse is not the only possibility. The order or approach of generation can be different. One method uses monostable multivibrators with adjustable pulse widths and a differential operational amplifier to generate a biphasic pulse [30]. Afterwards, this voltage based pulse needs to be converted to a current stimulation. A diagram of this generation can be seen in Figure 3.4. The advantage of this is that the pulses are easily created and switching time is always the same due to the differential operational amplifier. The disadvantage is that the voltage to current source should be quick enough and just as precise for positive currents as for negative currents.

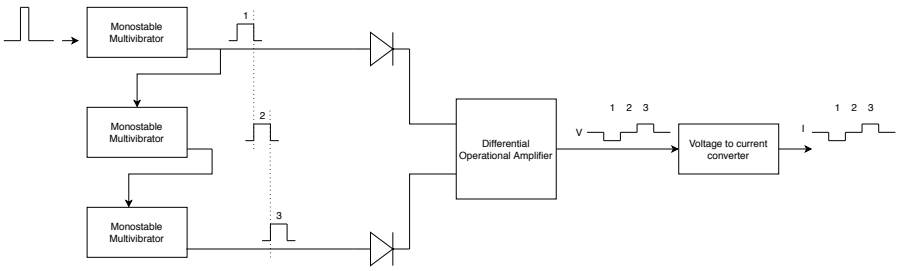


Figure 3.4: Biphasic signal generation using Monostable Multivibrators. After applying a pulse to the first multivibrator, the output stays high for a set amount of time. Once the output is low again, the second multivibrator is driven and will output its pulse. The same for the third multivibrator. A differential operational amplifier is able to make a negative voltage from the first multivibrator and a positive voltage from the second.

Instead of generating multiple signals like the last implementation, it is also possible to use two current sources to switch between for a positive and negative current [35]. The advantage is that the time duration of the pulses depend on the switches only, so they can be precisely driven from a microcontroller. The disadvantage is that the two current sources should be matched as closely as possible. Especially when using variable current sources. A basic circuit is shown in Figure 3.5.

A different approach of creating a pulse is by using two 555 timers. A 555-timer is a component that is very frequently used for the generation of pulse signals, PWM signals or other timer implementations. Since this component can make a pulse with a high precision, it is suitable as signal generator. Unfortunately, one 555-timer is not able to alter the pulse width and frequency of a generated wave independently. This can be solved if two timers are combined, one for the generation of frequency and one to manage the pulse width. The advantage of using this method is that the circuit is very precise and fast. The disadvantage is that for changing the frequency, a capacitor value on both the first and second timer need to be changed and the pulse width needs to be altered by changing a resistance.[15]

After considering the options, the decision was made to use only one current source. This ensures that the anodic and cathodic amplitude are the same or nearly the same. In addition, the usage of a constant current source provides a stable current output. When this signal is switched afterwards, the cathodic and anodic pulse have the same amplitude. A DAC can be used to set the amplitude of the current souce and an H-bridge is used to switch the signal

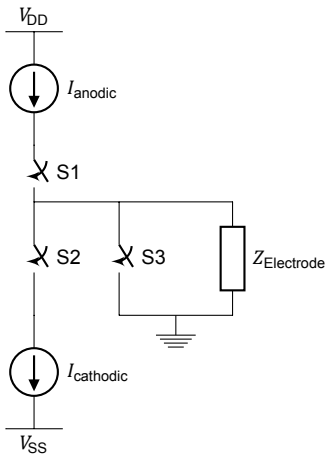


Figure 3.5: Biphasic generation using two current sources. By using switches S1 and S2, the direction of the current can either be set to an cathodic pulse or an anodic pulse. S3 is able to ground the electrode, making sure no current from the sources passes through the electrode.

between the cathodic pulse, anodic pulse and the interphase delay. When using the same type of transistors in the H-bridge, the different switching times in the stimulation are the same.

4 Power Management

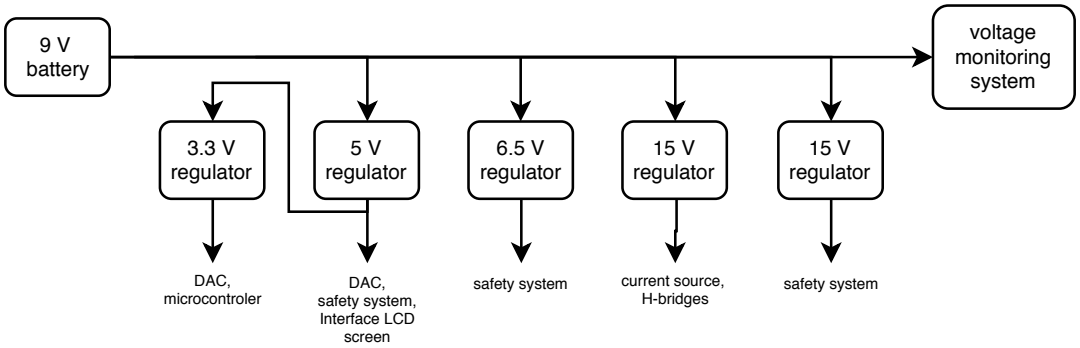


Figure 4.1: Block diagram of the power management system. The neural stimulator is powered by a 9 V battery, which is monitored by the microcontroller to detect when the battery is empty. The stimulator requires four different voltage levels which are provided by the voltage regulators. The 3.3 V regulator is powered by the 5 V regulator.

To provide the entire device with power, a Power Management System (PMS) is designed, made and tested. This chapter describes the requirements, implementation and measurements of this system as shown in Figure 4.1. The PMS will provide the power for the waveform generator as well as the interface, as described in [1], and the safety module, which is described in [2].

The waveform generator needs to be accurate in order to guarantee the required precision of the set stimulation parameters. This requires accurate voltage regulators for the supply voltage of each subsystem.

4.1. Requirements of the Voltage Regulators

The voltage of a battery drops over time, so a regulator is required to ensure a constant voltage. The different subsystems of the stimulator need different supply voltages. An overview of these is given in Table 4.1. There are no specific requirements on power usage and operation time. However, efficiency needs to be taken into account when designing the PMS.

4.2. Design

4.2.1. Battery and Voltage Monitoring System

To improve the safety of the stimulator, it is powered from a battery and not from the 230 V mains. A 9 V alkaline battery of type 6LR61, with a typical capacity 550 mAh is chosen for its compactness, high capacity and high voltage.

Table 4.1: Power budget of the entire system.

Voltage	Subsystem	Maximum current	Accurate voltage required
3.3 V	DAC	low, < 0.1 mA	Yes
	Microcontroller	58 mA	No
5 V	DAC	0.4 mA	No
	Safety system	55 mA	Yes
	Interface LCD screen	25 mA	No
6.5 V	Safety system	low, only used as reference voltage in comparator	Yes
15 V	Current source	21 mA	No
	Safety system	40 mA	No
	H-bridges	23 mA	No

To detect when the battery is empty, a voltage monitoring system is used. The battery voltage is connected to the analog input of the microcontroller. A voltage divider is added in between to make sure that the input voltage of the microcontroller stays under the maximum of 3.3 V. All regulators work down to a minimum battery voltage of 7 V. The voltage monitoring system will detect that the battery is almost empty from 7.5 V. Then there is still 0.5 V left to let the stimulator work for a bit longer. This prevents the stimulator from directly shutting down after a low battery voltage is detected.

The voltage divider uses a 287 kΩ resistor in series with a 105 kΩ resistor as shown in Figure 4.2. By using this ratio, the maximum voltage on the input of the microcontroller becomes $v_{\max} = 105\ \text{k}\Omega/(105\ \text{k}\Omega + 287\ \text{k}\Omega) \cdot 9\ \text{V} = 2.41\ \text{V}$, which is far under the maximum 3.3 V. The microcontroller turns on an LED on the interface when a voltage of 2.01 V or lower is sensed. This corresponds with a battery voltage of 7.5 V. After this, the device keeps working, until the microcontroller senses a voltage of 1.88 V or lower, corresponding to a battery voltage of 7 V. At that moment, the microcontroller will stop the stimulation.

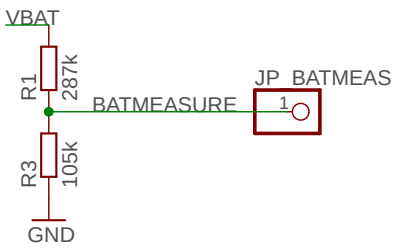


Figure 4.2: Schematic of the voltage divider to monitor the battery voltage.

4.2.2. Linear Regulators

Linear regulators work as voltage dividers where the internal resistance is varied to ensure a constant output voltage. These regulators provide a very stable output with a very low voltage ripple and noise. This makes them widely used for applications where a precise voltage is required. The power efficiency of linear regulators is relatively low, since the voltage difference between the input and output is converted into heat. The efficiency can be calculated as shown in Equation 4.1

$$\eta = \frac{P_{\text{out}}}{P_{\text{in}}}. \tag{4.1}$$

Converting from 9 V to 5 V for example only gives a power efficiency of 56%. Another downside of linear regulators is that the input voltage often needs to be 2 V higher than the output voltage, making the required input voltage for a 5 V linear regulator equal to 7 V. A low-dropout (LDO) regulator solves this problem by lowering the minimum input voltage significantly down to less than 100 mV [36].

4.2.3. Switching Regulators

A linear regulator is very power inefficient for big differences between the input and output voltage. This can be solved by using a switching regulator. A switching regulator can be used in different configurations, a boosting converter to step up the input voltage, a bucking converter to step down the voltage or a boosting/bucking converter to create lower as well as higher output voltages.

The efficiency of a switching regulator, in practical applications, is about 80% to 90% [36]. This is much higher than linear regulators, especially for a high voltage difference between the input and the output. The main disadvantage of switching regulator is the added harmonics because of the switching behavior. Besides that, switching regulators often require many external components which need to be accurately chosen.

The harmonics, or switching noise, of a switching regulator can be reduced by adding a Low Pass Filter (LPF) to the output. For high power applications, a switching regulator is a good option to reduce the power losses. For precision applications, a linear regulator is more often used to ensure a stable output. When both are important, a switching regulator followed by a linear regulator can be used. For output voltages higher than the input voltage, a switching regulator is the only possibility.

4.2.4. Chosen Voltage Regulators

To meet the requirements of Table 4.1, a combination of LDOs and switching regulators is chosen. Two different 5 V regulators are tested to determine which works the best. The first is an LDO, which gives a more constant output. The second one is a switching regulator to be more power efficient. The 3.3 V regulator needs to give an accurate voltage for the DAC and therefore needs to be a linear regulator. When this regulator would be directly connected to the 9 V battery, it would have a low efficiency, This is due to the fact that the input and output current of LDOs are almost the same, even though the voltage is different. Since the 3.3 V LDO needs to power the DAC and Microcontroller, 58 mA is the required output current. The LDO itself subtracts 15 μA from the input current, so the input current is about 58 mA as well. This means that the power in the LDO equals:

$$P_{in} = 9\ \text{V} \times 58\ \text{mA} = 522\ \text{mW} \tag{4.2}$$

The voltage on the output is 3.3 V. This means that the output power equals

$$P_{out} = 3.3\ \text{V} \times 58\ \text{mA} = 191\ \text{mW} \tag{4.3}$$

This means that the total efficiency of the LDO equals

$$\eta_{3.3\ \text{V}} = \frac{191\ \text{mW}}{522\ \text{mW}} = 37\%. \tag{4.4}$$

When the 3.3 V LDO regulator is connected to a very efficient 5 V regulator, the efficiency becomes a lot higher, since the input power only equals

$$P_{in} = 5\ \text{V} \times 58\ \text{mA} = 290\ \text{mW} \tag{4.5}$$

At the same time, the output power stays the same, so the efficency of lowering the voltage from 5 V to 3.3 V is

$$\eta_{3.3\ \text{V}} = \frac{191\ \text{mW}}{290\ \text{mW}} = 66\% \tag{4.6}$$

The 6.5 V regulator needs to give a very accurate voltage, therefore an LDO is chosen. There is no LDO available with a fixed 6.5 V output, therefore an adjustable LDO is selected. The 15 V regulator will only be used to power op amps, which can therefore be less accurate. The chosen voltage regulators are shown in Table 4.2. The 15 V boost switching regulator could only be found for a maximum output current of 50 mA, while 84 mA is needed. Therefore, two 15 V regulators are used to power two different subsystems which need a supply current of 44 mA and 40 mA.

Table 4.2: Chosen voltage regulators.

Name	Output voltage	Type	Maximum output current	Input voltage range
MAX604CPA+	3.3 V	Fixed output LDO	500 mA	4.3 V - 11.5 V
MAX603CPA+	5 V	Fixed output LDO	500 mA	6.0 V - 11.5 V
LM2594M-5.0	5 V	Buck (step-down) switching regulator	500 mA	7 V - 40 V
LP2951ACN	6.5 V	Adjustable output LDO	100 mA	6.88 V - 30 V
MAX633ACPA+	15 V	Boost (step-up) switching regulator	50 mA (two times)	2 V - 16.5 V

4.2.5. Capacitors

Capacitors are used to remove ripple from the input and output of the voltage regulators. This is essential in order to get a constant output voltage. There is a variety of capacitor types available, which all have their own advantages and disadvantages for this application. The main three capacitor types, aluminum electrolytic capacitors, tantalum capacitors and ceramic capacitors differ as described below [37].

- **Aluminum electrolytic capacitors** - These are polarized and can have large values of capacitance, typically between 1 and 47000 μF. These capacitors can have high working voltages up to 350 V and can handle a high ripple current. The main drawback is the poor performance at high frequencies. This type of capacitor also has a high leackage and a low tolerance.
- **Tantalum capacitors** - These capacitors are polarized as well. They have a high capacitance value in a small volume with a low leakage. Tantalum capacitors have a lower Equivalent Series Resistance (ESR) than aluminum electrolytic capacitors. The drawbacks are that this capacitor has a low ripple current capability and is very intolerant of reverse voltages or over voltages.
- **Ceramic capacitors** - This is a non-polarized type of capacitor with an even lower ESR. The values range from a few pF up to about 0.1 μF. It has a good performance at high frequencies and is widely used in both leaded and Surface Mounted Device (SMD) form.

Ceramic capacitors with a low ESR usually improve the transient response of the regulator. However, some regulators require tantalum capacitors with a higher ESR to stabilize the feedback loop [36].

4.3. Implementation of the Voltage Regulators

4.3.1. Regulator 3.3 V

The implementation of the 3.3 V LDO regulator is shown in the schematic of Figure 4.3. An input and output capacitor of 10 μF is chosen, based on recommendations from the data sheet. Tantalum capacitors are chosen for the low ESR.

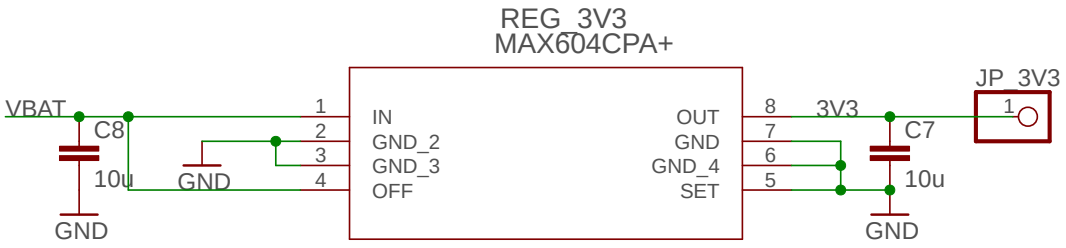


Figure 4.3: Schematic of the 3.3 V LDO regulator.

4.3.2. Regulator 5 V

Two different 5 V regulators are designed and tested, to ensure the best regulator for the final design. A switching regulator is tested since it has a high efficiency and an LDO regulator is tested because it has a high precision. When the switching regulator is used, the 5 V will be the input of the 3.3 V LDO. In case the 5 V LDO is used, the 3.3 V LDO will be connected to the battery directly.

LDO Regulator 5 V

The implementation of the 5 V LDO regulator is shown in the schematic of Figure 4.4. The external components are the same as for the 3.3 V LDO, which are two 10 μF tantalum capacitors.

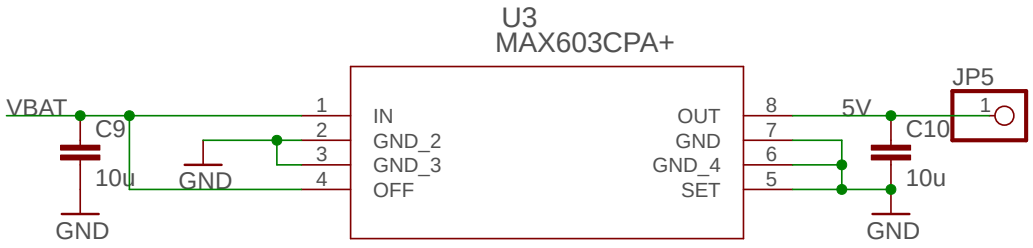


Figure 4.4: Schematic of the 5 V LDO regulator.

Switching Regulator 5 V

The implementation of the 5 V switching regulator is shown in the schematic of Figure 4.5. Both the input and output capacitors are chosen to be tantalum capacitors, in order to have a low ESR. The ESR of ceramic capacitors is even lower, but the required values are not available as ceramic capacitors. The inductor L1 requires to be 68 μH for the current and voltage of this application. Therefore the EPCOS (TDK) B82464G4683M000 inductor of 68 μH, which has a low resistance of only 130 mΩ, is selected.

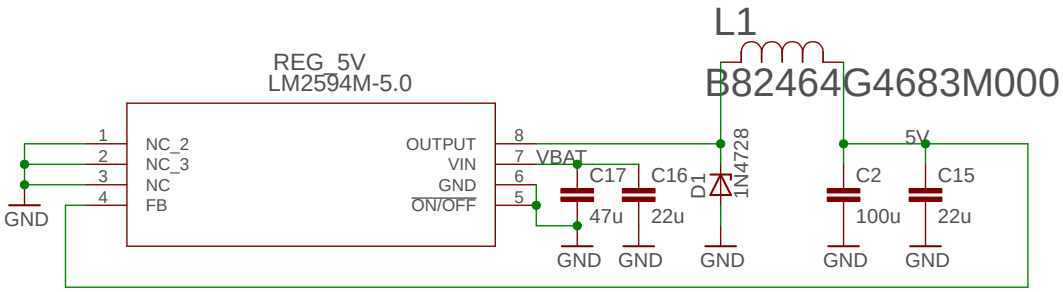


Figure 4.5: Schematic of the 5 V switching regulator.

4.3.3. Regulator 6.5 V

The LP2951ACN LDO with an adjustable output is used to generate a stable 6.5 V. The implementation if this regulator is shown in the schematic of Figure 4.6. This regulator uses a feedback controlled by a voltage divider connected to the output. The resistance of R5 is recommended to be 100 kΩ [38]. The required resistance of R6 is calculated by

$$V_{\text{out}} = V_{\text{ref}}\left(1 + \frac{R_6}{R_5}\right) + I_{\text{fb}}R_6 \tag{4.7}$$

where V_{ref} is the nominal 1.235 V reference voltage [1] and I_{fb} is the feedback pin bias current, nominally –20 nA [38]. R_6 is calculated to be 427 kΩ. In order to get an accurate 6.5 V output

[1] The 1.235 V reference voltage is a voltage level that is kept constant inside the voltage regulator Integrated Circuit (IC). It is used to compare the voltage on the feedback pin.

votlage, R6 is implemented as a trimmable potentiometer.

The input capacitor, C5, needs to be a tantalum, ceramic or aluminum electrolytic capacitor of minimum 1 μF. For this a 10 μF capacitor is used. Ceramic capacitors are not available with a value as high as this, therefore a tantalum capacitor with a low ESR is used. The same capacitor is used for C6. Since the 6.5 V regulator will be used as a V_{ref}, it is desired to reduce the output noise. One method to lower this noise is by increasing the capacitor. However, as described in the data sheet, this is not very effective [38]. A more effective method is to connect a capacitor between the output and the feedback pin. This capacitor needs to be 0.01 μF. A ceramic capacitor is chosen to assure a low ESR.

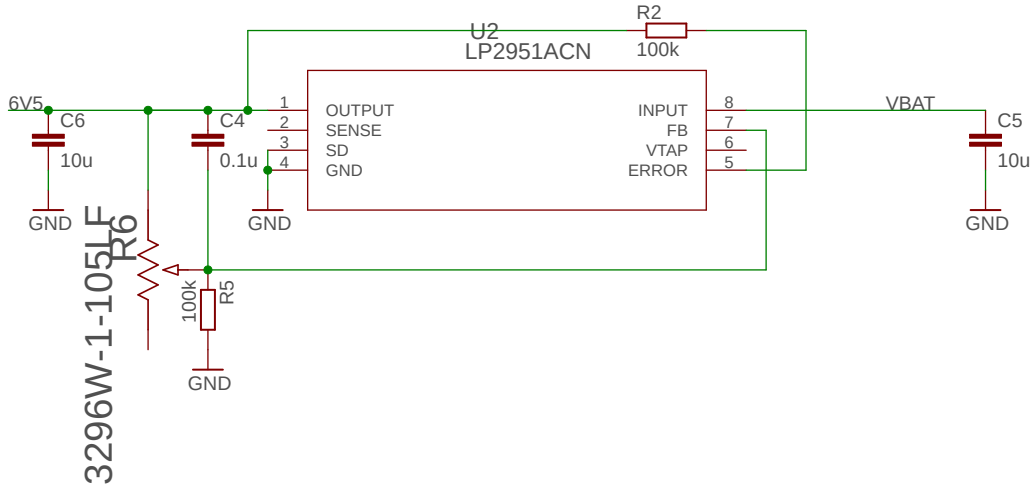


Figure 4.6: Schematic of the 6.5 V LDO regulator. The potentiometer R6 only has two pins connected to make it a trimmable resistor.

4.3.4. Regulator 15 V

Figure 4.7 shows the schematic of the 15 V switching regulator implementation. This regulator requires an inductor at the input and two capacitors at the output. According to the data sheet, the inductor needs to have a value of 500 μF with a resistance of about 0.5 Ω or less [39]. However, the closest available inductor of 470 μH with a resistance of 0.21 Ω is selected. The 100 μF capacitor needs to be an aluminum electrolytic capacitor and the 0.1 μF capacitor needs to be ceramic.

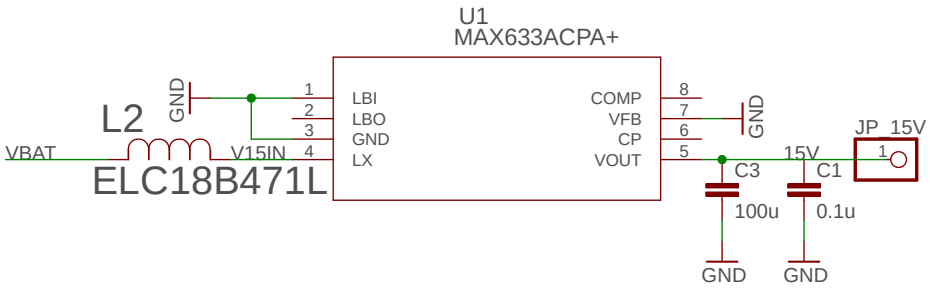


Figure 4.7: Schematic of the 15 V switching regulator.

4.4. Measurements

The regulators are tested to determine if they work as expected. All regulators are tested separately with different loads of 3 MΩ and 470 Ω. With the outcome of these tests, the decision is made to use the 5 V switching regulator rather than the 5 V LDO regulator. The power supply used for this test is the ISO-TECH IPS-4303. The DC voltages are measured by the

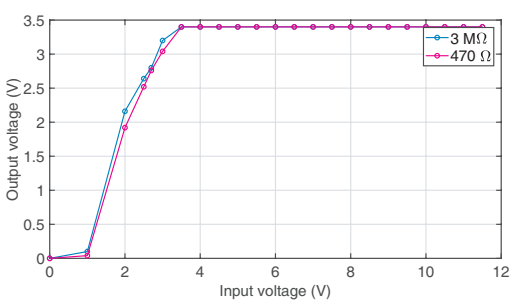
Extech EX210 multimeter and the used oscilloscope is the Tektronix TDS 2014C.

The 3.3 V and both 5 V regulators are tested on Printed Circuit Board (PCB) implementation. This is advantageous since a layout with short paths improves the accuracy of the output voltage.

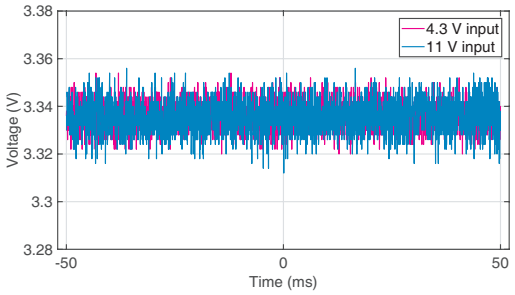
4.4.1. Regulator 3.3 V

The DC output voltage of the 3.3 V regulator is measured for the full range of available input voltages, from 0 V to the expected maximum input voltage of 11 V. As can be seen in Figure 4.8a, 3.5 V is the minimum input voltage to ensure a 3.3 V output voltage. Besides that, it can be seen that the output voltage is constant for voltage from 3.5 V to 11 V.

Figure 4.8b shows the output voltage over time for an input voltage of 4.3 V and 11 V. These are the minimum required input voltage for this regulator and the maximum expected input voltage. The 3.3 V regulator will be used as V_{ref} for the DAC which together with the voltage to current converter generates the stimulation current. The 3.3 V regulator therefore needs to be accurate enough. The required accuracy of the generated current is 0.1 mA for a maximum amplitude of 10 mA. This requires a relative accuracy of 1%. At a maximum V_{ref} of 3.3 V, this accuracy needs to be 33 mV. The maximum deviation from the average output voltage, as can be seen in Figure 4.8b, is 24 mV which is lower than the required 33 mV. The 3.3 V regulator therefore has the required accuracy.



(a) 3.3 V LDO regulator output voltage for different loads.



(b) 3.3 V LDO regulator output voltage for different input voltages.

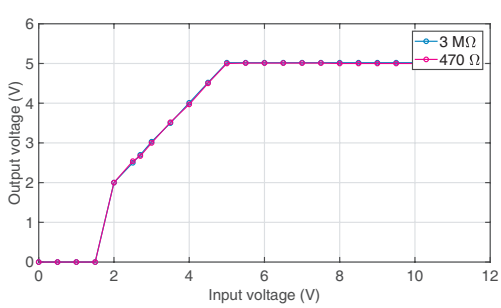
Figure 4.8: Measurement results of the output voltage of the 3.3 V LDO regulator.

4.4.2. Regulator 5 V

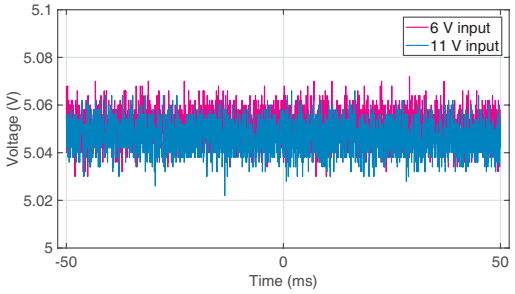
Both the 5 V LDO regulator and the 5 V switching regulator are measured, after which the switching regulator is chosen to have the best performance and efficiency combination.

LDO Regulator 5 V

Figure 4.9 shows the measurement results of the output voltage of the 5 V LDO regulator. The 5 V LDO regulator generates a constant 5 V output from an input voltage of only 5 V as can be seen in Figure 4.9a. An input voltage between 5 V and 11 V results in a constant output voltage. Figure 4.9b shows the output voltage over time for an input voltage of the minimum required input voltage for this regulator, 6 V, and the maximum expected input voltage of 11 V. The maximum peak to peak output voltage of the 5 V LDO regulator is measured to be 40 mV at an input voltage of 6 V and 44 mV at an input voltage of 11 V.



(a) 5 V LDO regulator output voltage for different loads.



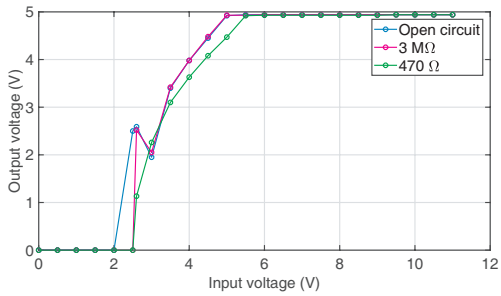
(b) 5 V LDO regulator output voltage for different input voltages.

Figure 4.9: Measurement results of the output voltage of the 5 V LDO regulator.

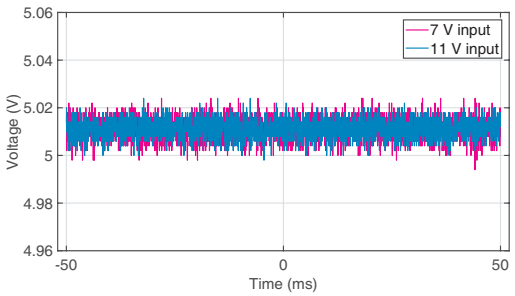
Switching Regulator 5 V

Figure 4.10 shows the measurement results of the output voltage of the 5 V switching regulator. The 5 V switching regulator generates a constant 5 V output from an input voltage of 5.5 V as can be seen in Figure 4.10a. A load with a high impedance allows the regulator to provide a 5 V output from an input of 5 V. An input voltage between 5.5 V and 11 V results in a constant output voltage. Figure 4.10b shows the output voltage over time for an input voltage of the minimum required input voltage for this regulator, 7 V, and the maximum expected input voltage of 11 V. The maximum peak to peak output voltage of the 5 V switching regulator is measured to be 30 mV at an input voltage of 7 V and 26 mV at an input voltage of 11 V.

It can also be seen that the output voltage for an input voltage of 2.5 V is higher than for 3 V. This is the case for a load of 3 MΩ as well as an open circuit. The reason for this is not found. It is however not important, since the regulator will only be used with an input voltage of 7 V or higher.



(a) 5 V switching regulator output voltage for different loads.



(b) 5 V switching regulator output voltage for different input voltages.

Figure 4.10: Measurement results of the output voltage of the 5 V switching regulator.

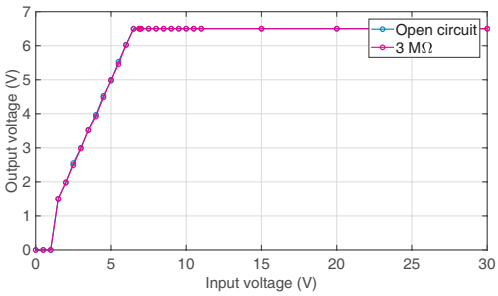
Decision on 5 V regulator

From the measurement results in Figure 4.9a and 4.10a it can be concluded that the switching regulator has less variation in the output voltage than the LDO regulator. It is also more power efficient, therefore this switching regulator is selected as the best option.

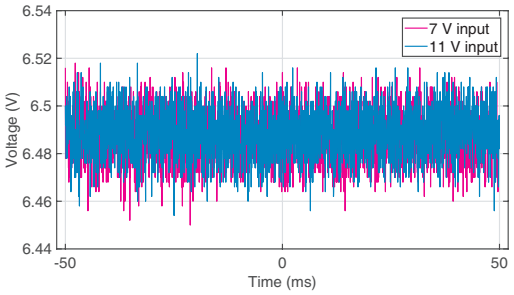
4.4.3. Regulator 6.5 V

The DC output voltage of the 6.5 V LDO regulator is measured for the full range of available input voltages, from 0 V to the maximum input voltage of 30 V. It is measured for a load of 3 MΩ and an open load since a current of less than 0.1 mA is expected. As can be seen in Figure 4.11a, 6.5 V is the minimum input voltage to ensure a 6.5 V output voltage. Besides that, it can be seen that the output voltage is constant for an input voltage from 6.5 V to 30 V.

Figure 4.11b shows the output voltage over time for an input voltage of 7 V and 11 V. The connected load is 3 MΩ. The maximum peak to peak voltage of the 6.5 V regulator is measured to be 37 mV at an input voltage of 7 V and 35 mV at an input voltage of 11 V.



(a) 6.5 V LDO regulator output voltage for different loads.



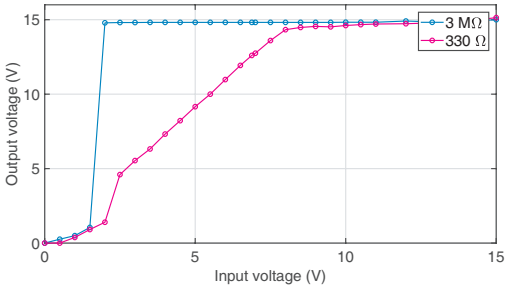
(b) 6.5V LDO regulator output voltage for different input voltages. The connected load is 3 MΩ.

Figure 4.11: Measurement results of the output voltage of the 6.5 V LDO regulator.

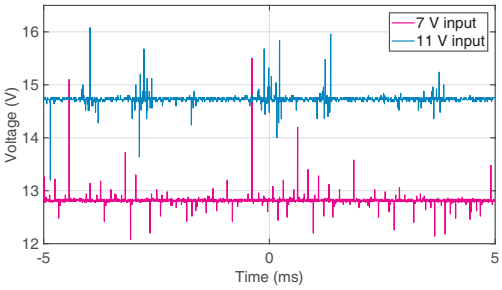
4.4.4. Regulator 15 V

The DC output voltage of the 15 V switching regulator is measured from 0 V to 15 V. It is measured for a load of 3 MΩ and a load of 330 Ω. The latter one corresponds to the maximum expected output current of 45 mA. As can be seen in Figure 4.12a, for a load of 330 Ω, an input voltage of 8 V or higher is required. This is significantly higher than the specified minimum input voltage of 2 V. A possible reason for this is that the measurements are done with a breadboard implementation of the regulator and the layout of the circuit can influence its performance. Besides that, a 470 μH inductor is used where a 500 μH initially was required.

Figure 4.11b shows the output voltage over time for an input voltage of 7 V and 11 V. The connected load is 330 Ω. The maximum peak to peak voltage of the 15 V regulator is measured to be 2.7 V at an input voltage of 7 V and 1.5 V at an input voltage of 11 V. This high noise voltage is caused by the switching behaviour of the regulator. This can possibly be reduced by a low pass filter, for which more research needs to be done.



(a) 15 V switching regulator output voltage for different loads.



(b) 15 V switching regulator output voltage for different input voltages. The connected load is 330 Ω.

Figure 4.12: Measurement results of the output voltage of the 15 V switching regulator.

5 Microcontroller

5.1. Requirements

The microcontroller has two main tasks in order to generate the biphasic stimulation pulse. The first one is to generate a specified voltage which will be converted into the correct current by the voltage to current converter. The second task is to generate the signals for the switches for the H-bridge, used to switch the orientation of the signal through the electrodes.

In addition, the microcontroller has to be able to read analog inputs from potentiometers that can alter the stimulation parameters. It has to react on error signals that may have to stop or correct the stimulation while the system is operating. It should control an LCD screen to display the set stimulation parameters and turn on LEDs to show the user the stimulation status. This means that the microcontroller needs enough input-output pins, an Analog to Digital Converter (ADC) to read potentiometer values and timers to control the H-bridge signal. For fast prototyping the microcontroller needs to include a development board. Table 5.1 sums up the requirements for the microcontroller by listing the requirements per part of the system.

Table 5.1: Microcontroller requirements for the different components in the device.

Component	Input/output pins	ADC's	Timers	Timer size
Power management	1	1	0	-
Interface potentiometers	4	4	0	-
Interface LCD	2	0	0	-
DAC (using timer)[1]	3	0	1	16-bit
H-bridge	3	0	1	32-bit
Safety module	2	0	0	-
Total system	**15**	**5**	**2**	**-**

5.2. Comparison of Microcontrollers

Table 5.2 shows the different properties of the considered microcontrollers, two of which have been used for stimulator purposes as well.

[1] The DAC uses a simplified version of the SPI protocol that is implemented with a timer and 1 fewer input/output pin.

Table 5.2: Comparison between microcontrollers.

	PIC12LF1822 [40]	**MC9S08SH8** [41]	**LPC1343**
Supply voltage	1.8 V to 5 V	2.7 V to 5.5 V	2 V to 3.6 V
Processor type	8-bit PIC	8-bit HCS08	32-bit ARM Cortex-M3
Clock frequency	32 MHz	40 MHz	72 MHz
Timers	two 8-bit, one 16-bit	one 8-bit, two 16-bit	two 16-bit, two 32-bit
ADC (amount and bits)	eight 10-bit	twelve 10-bit	eight 10-bit
Number of inputs/outputs	11	17	42
Frequency accuracy of the clock[2]	5%	2%	1%
Output rise time	typ. 15 ns (max. 32 ns)	typ. 40 ns	max. 5.0 ns
Output fall time	typ. 15 ns (max. 30 ns)	typ. 40 ns	max. 5.0 ns

Of the three microcontrollers, the LPC1343 has been chosen to use for the system. From the three in the table, it is the only one that is capable of driving a 32-bit timer. In addition to that, it has more than enough input/output ports, so extra ports were available if needed.

5.3. Software

The software part has been split up for the different subgroups. The interface subgroup created the main file, the communication with the LCD screen and reading and processing the values from the potentiometers [1]. The code for the H-bridge and DAC has been made by this subgroup and will be elaborated in this chapter. The different files can be shared on request. Contact information can be found in appendix A.1.

5.3.1. Digital to Analog Converter

The Digital to Analog Converter (DAC) uses the Serial Peripheral Interface (SPI) protocol to communicate with the microcontroller. This protocol officially uses four wires to communicate [42]:

- **SCK** (Serial Clock): A communication clock that is driven by the master.
- **SSEL** (Slave Select): A signal that is low if master is sending data.
- **MOSI** (Master Out Slave In): Data from the master to the slave.
- **MISO** (Master In Slave Out): Data from the slave to the master.

A typical data transfer starts when SSEL is pulled down by the master. A serial clock begins pulsing and in synchronisation with this clock, the master and slave can send and receive data. After the data has been sent, the clock stops and SSEL is set to 1 again by the master. A visual interpretation of the signals can be seen in Figure 5.1

[2] Frequency accuracy over entire temperature and voltage range.

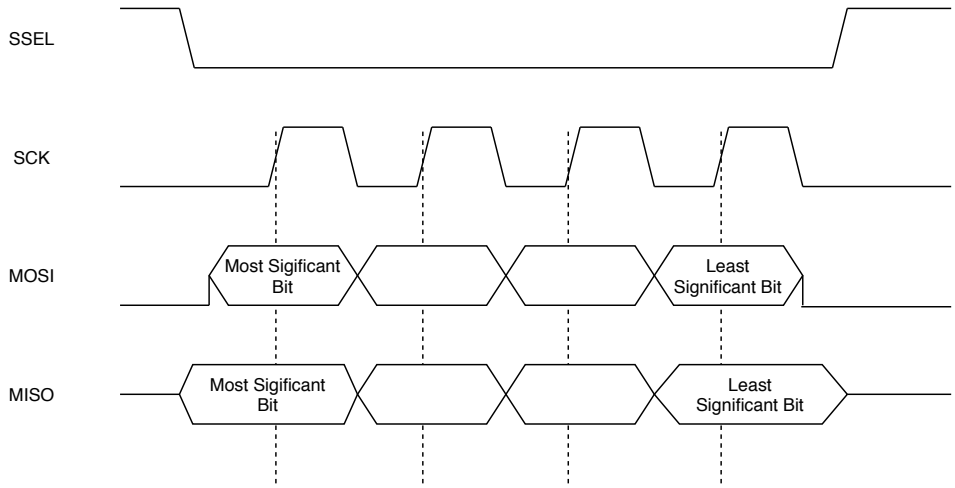


Figure 5.1: An example of a transmission using the SPI protocol.

Table 5.3: Operations of the DAC using the 16 bit word constructed from C2-C0, D9-D0 and S2-S0 and the function the device performs. X means either a 1 or a 0.

C2...C0	D9...D0	S2...S0	Function
X 0 0	10 bits data	000	Load input register; DAC register immediately updated (exit shutdown).
X 0 1	10 bits data	000	Load input register; DAC register unchanged.
X 1 0	XXXXXXXXXX	XXX	Update DAC register from input register (exit shutdown; recall previous state)
1 1 1	XXXXXXXXXX	XXX	Shutdown
0 1 1	XXXXXXXXXX	XXX	No operation

The chosen DAC, further discussed in chapter 6, cannot send data back to the microcontroller. Therefore, the MISO signal is not used. The DAC starts reading data when the serial clock has a first low-to-high transition. On the next low-to-high transitions, the next bits will be read until SSEL is high again. The communication is the same as in Figure 5.1, but without the MISO data line. The total transmission is 16 bits long. The first and last three are control signals. The possible operations with these control signals are summarized in Table 5.3. The data bits determine the output voltage of the device, where 0 is 0 V and 1023[3] equals a reference voltage, V_{ref} [43]. In order to send new data and update the DAC, the following format is used every communication cycle: 100 XXXXX XXXXX 000. Here, the X means either a 1 or a 0, corresponding to the 10 bits of data to be sent. The code starts a new transmission as soon as the previous transmission has ended. Whether the data for the DAC is changed is not regarded.

5.3.2. H-bridge

Next to the DAC, the microcontroller needs to create signals for the H-bridge as well. The H-bridge operates on three signals. If signal S1 or S2 is high, a current can flow through the H-bridge. S1 creates the cathodic pulse and S2 creates the anodic pulse. During the interpulse or interphase delay, signal S3 is high. This signal grounds the current source, so no current can flow through the H-bridge. In order to make these signals, one timer is used on the microcontroller. The period of this timer equals the stimulation period, afterwards, it resets. Using four interrupt moments, the correct times to switch the H-bridge can be

[3] 1023 is the maximum a 10 bit number can form

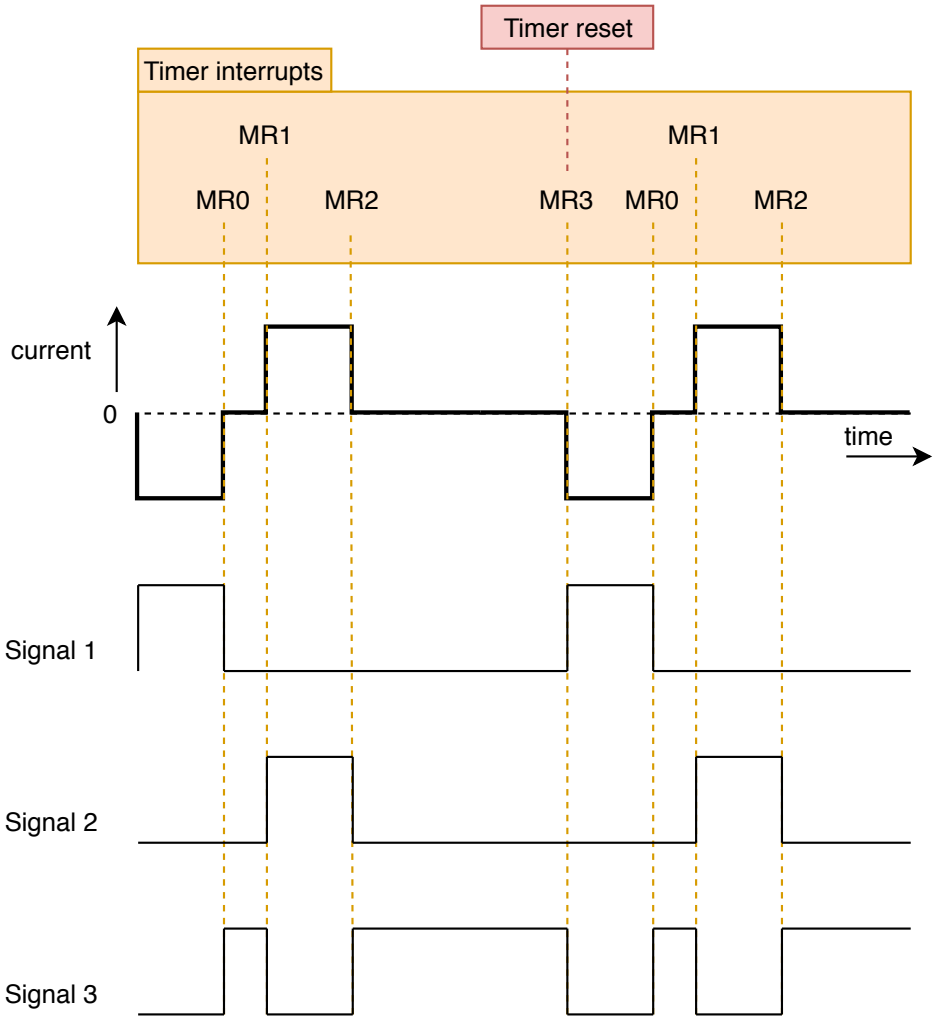


Figure 5.2: Interrupt moments and control signals for the generation of a biphasic signal.

determined as can be seen in Figure 5.2.

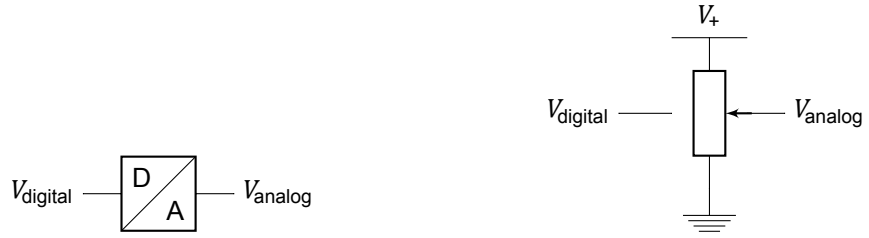
The way interrupts work is that the timer counts until the value of the interrupt is reached. At that moment, the code switches signals or resets the timer. MR3 is the interrupt that determines the frequency of the signal. Because the clock of the microcontroller runs at 72 MHz, the value of this interrupt should be MR3 = (72 MHz)/(Required frequency). When the interrupt is executed, the timer will be reset, starting from 0 again. MR0 is the pulse width of the two pulses. The value of MR1 is found by adding MR0 with the interphase delay. Likewise, the value of MR2 found by adding MR1 with the pulse width.

Every time one period is completed, the program checks if there are changes in parameters. If the parameters from the interface subgroup are unchanged, the timer continues with its next period. If the parameters did change, the interrupt timings are first set accordingly before the next period of the H-bridge is started.

6

Digital to Analog Converter

The voltage to current converter requires an accurate voltage in order to generate an accurate current. The generation of this voltage, using the microcontroller, can be done on several ways. The most common method is to use a DAC as shown in Figure 6.1a [10, 16, 40]. Another method is to use a digital potentiometer as shown in Figure 6.1b [44, 45]. When using a digital potentiometer, the accuracy is very important. However, potentiometers can have errors of up to 20% if not chosen carefully [10]. Commercial of the shelf DACs use a higher quiescent current than digital potentiometers, but that is no problem for this application.



(a) Digital to Analog Converter. (b) Digital potentiometer.

Figure 6.1: A DAC and digital potentiometer which can be used to generate the analog voltage for the current source.

6.1. Requirements

The maximum required stimulation current is 10 mA with an accuracy of 0.1 mA. This gives 100 steps in amplitude, which corresponds with 7 bits. However, to add an accuracy margin, a DAC with minimum 10 bits will be used. This results in a step size of 10 μA. The accuracy of the DAC must be as high as possible. The DAC should be controlled via a serial protocol from the microcontroller. This reduces the required output pins from the microcontroller, compared to a parallel connection. The data interface should be either SPI, Universal Asynchronous Receiver-Transmitter (UART) or Inter-Integrated Circuit (I^2C), since these are supported by the selected microcontroller.

6.2. Design

Different DACs are compared, which can be seen in Table 6.1. The main difference between these three are the maximum errors. MAX5354CPA+ is chosen for the low integral nonlinearity and low maximum gain error. The supply current of all three is almost the same and all very low, making it a less important point of comparison. The amplitude of the DAC output does not change very fast and will only be adjusted when the user adjusts the inputs of the neural stimulator. Therefore, the settling time and the slew rate are less important as well.

Table 6.1: Comparison between different DACs

	TLC5615CP	MAX5354CPA+	MAX5354MJA
Supply voltage	4.5-5.5V	4.5-5.5 V	4.5-5.5 V
Data interface	SPI	SPI	SPI
Bits	10	10	10
Integral nonlinearity	$\pm$1 LSB	$\pm$1 LSB	$\pm$2 LSB
Maximum gain error	$\pm$3 LSB	$\pm$2 LSB	$\pm$2 LSB
Supply current	typ. 230 μA (max. 350 μA)	typ. 240 μA (max. 400 μA)	typ. 240 μA (max. 400 μA)
Output settling time	12.5 μs	10 μs	10 μs
Voltage output slew rate	0.5 V/μs	0.6 V/μs	0.6 V/μs

The output voltage of the MAX5354CPA+ is calculated by

$$V_{\text{out}} = V_{\text{ref}}\left(\frac{\text{NB}}{1024}\right) \tag{6.1}$$

where NB is the numeric value of the DAC's binary input code. The reference voltage is the maximum output voltage, which is chosen to be 3.3 V. This voltage needs to be at least 1.4 V below the supply voltage of 5 V [46].

The selected DAC uses an SPI protocol to communicate with the microcontroller for which it uses three inputs:

- **$\overline{\text{CS}}$** (chip select): A signal that must be low to enable the DAC's serial interface. This pin is connected to the SSEL pin of the microcontroller.
- **DIN** (serial-data input): Data from the microcontroller. This pin is connected to the MOSI pin of the microcontroller.
- **SCLK** (serial clock): Communication clock, driven by the microcontroller and connected to the SCK pin.

6.3. Implementation

The schematic of the DAC is shown in Figure 6.2. The capacitor values are chosen based on recommendations of the data sheet [46]. For both capacitors of 4.7 μF and 0.1 μF, tantalum types are selected for a low ESR.

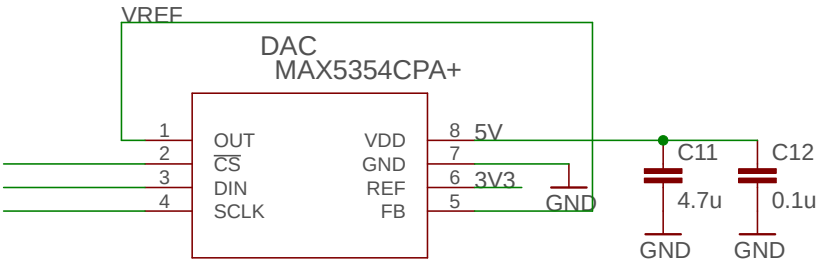
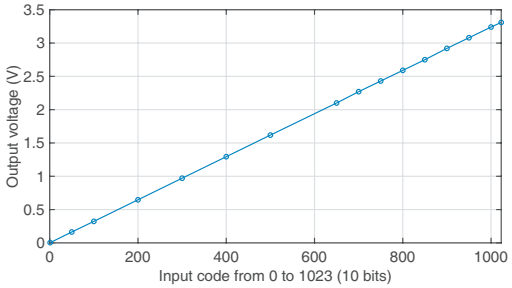


Figure 6.2: Schematic of the DAC. The $\overline{\text{CS}}$, DIN and SCLK pins are connected to the microcontroller.

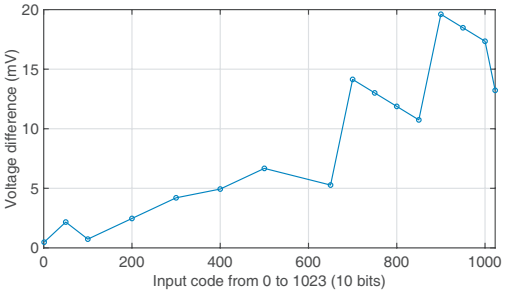
6.4. Measurements

The DAC is implemented on PCB after which it is measured in order to see if it meets the requirements. The measurements are done with the use of the ISO-TECH IPS-4303 power supply and the Extech EX210 multimeter. Figure 6.3a shows the output voltage of the DAC.

This output linearly increases from 0 V to 3.3 V. However, when looking at the difference between the measured and expected output voltages, as shown in Figure 6.3b, there is an error in the output voltage. The highest error, of 20 mV, occurs at an input code of 900. This is still lower than the required accuracy of 33 mV, as explained in subsection 4.4.1. The DAC therefore meets the requirement on accuracy.



(a) Output voltage of the DAC for different input codes for a reference voltage of V_{ref} = 3.3 V.

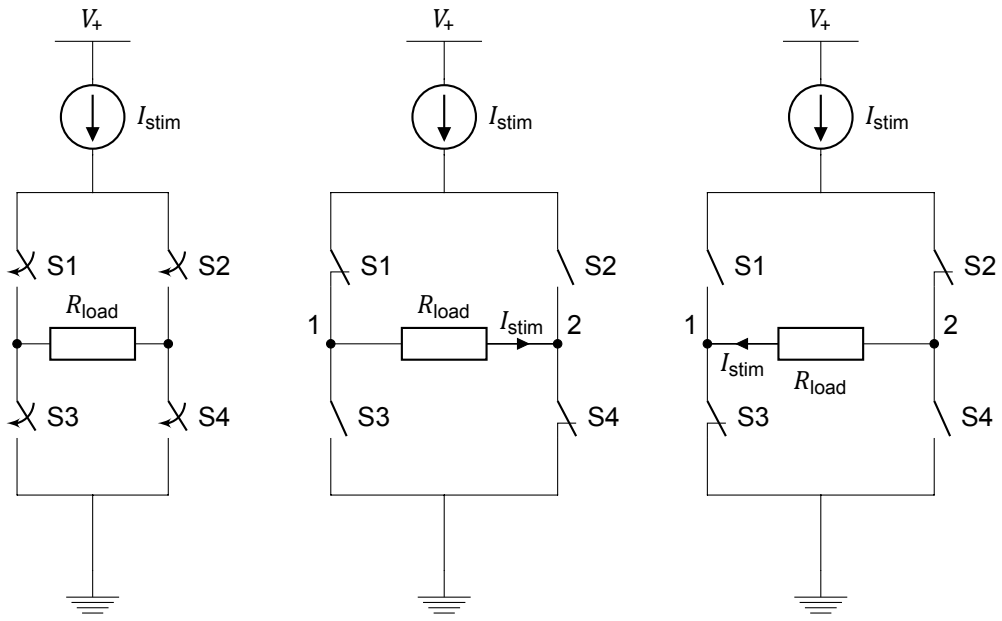


(b) Difference between measured and expected DAC output voltage for a reference voltage of V_{ref} = 3.3 V.

Figure 6.3: Measurement results of the output voltage of the DAC.

7 H-bridge

After a constant current has been made using a voltage to current converter, further discussed by the Interface and Control subgroup [1], it should be turned into a signal that has positive, neutral and negative phases, like displayed in Figure 2.1. One manner of creating this signal is by using a so called H-bridge. This design in its simplest form makes use of four switches, as shown in Figure 7.1a. If the switches are operated with the right timing, the current can travel through the load in two directions. Figure 7.1b shows how the current travels via one direction and Figure 7.1c displays how the switches should be closed for the current to travel in the other direction [47].



(a) Basic H-bridge design

(b) H-bridge with S1 and S4 closed

(c) H-bridge with S2 and S3 closed

Figure 7.1: Basic operation of an H-bridge. I_{stim} shows the direction of the current through R_{load}.

7.1. Requirements

The H-bridge has a few functional requirements that need to be resolved before it will work properly. First and foremost, the bridge needs to withstand the current of the signal that passes through. In addition it has to be able to handle the voltage differences on the source, gate and drain during operation.

(a) An NMOS transistor. (b) A PMOS transistor.

Figure 7.2: The two different MOSFETs.

Another important functional requirement is that it needs to be controlled by the microcontroller. This device has outputs that are either 0 V or 3.3 V. These logical signals need to be sufficient to switch the direction of the generated current.

Next to these functional requirements, the H-bridge needs to influence the signal as little as possible to keep the stimulation as close to the desired parameters as possible. Aside from this, other components of the system should not be damaged by the H-bridge.

7.2. Design

In order to open and close the switches introduced in Figure 7.1, signals from the microcontroler will be sent. This means that the switches need to be voltage controlled and capable of keeping up with the 15 kHz frequency.

7.2.1. Circuit Design

Transistors are the solution for these switches, Metal Oxide Semiconductor Field Effect Transistor (MOSFET) in particular. When applying a voltage on the gate of a MOSFET, a conducting channel between the emitter and the collector appears. This functions as a voltage controlled current source. When using an enhancement mode MOSFET, however, it behaves as a switch that is normally opened and can be closed by applying a voltage on Gate-to-source voltage (V_{GS}). The advantage of a MOSFET over for example a bipolar transistor is that no current flows through the gate, affecting the signal through the transistor as little as possible.

Figure 7.2a and 7.2b show the two different MOSFETs that exist; an N-channel MOSFET (NMOS) and a P-channel MOSFET (PMOS). These devices operate on the same principle. In order to create a conducting channel from drain to source for an NMOS, a positive V_{GS} is needed. This is opposed to the PMOS, where a negative V_{GS} is needed to create a conducting channel between source and drain.
When implementing MOSFETs in the H-bridge, switches S3 and S4, from Figure 7.1 can be easily replaced with NMOS transistors. If the source of the two transistors are connected to the ground, a positive voltage on the gate will create the conducting channel, thus effectively closing the switch. If switches S1 and S2 are implemented in the same way using a NMOS, a problem arises [48]. The sources of these transistors would be connected to node 1 and 2 in the figures. Because of the switching, these nodes are not always defined at the same voltage. When switch S1 and S4 are closed, node 2 is connected to ground. If switch S2 and S3 are closed, node 1 is connected to ground. This means that applying a 3.3V positive voltage on the gate of the transistors will not always guarantee surpassing the threshold voltage and therefore closing the switch.

This can be solved by using PMOS transistors, along with a driver circuit. The gate on the PMOS transistors should be constantly the same as the input voltage, except when the switch needs to be closed. Then, the voltage needs to be less than the input voltage. Because the input volage is better defined, this is a safer way of operating the H-bridge.

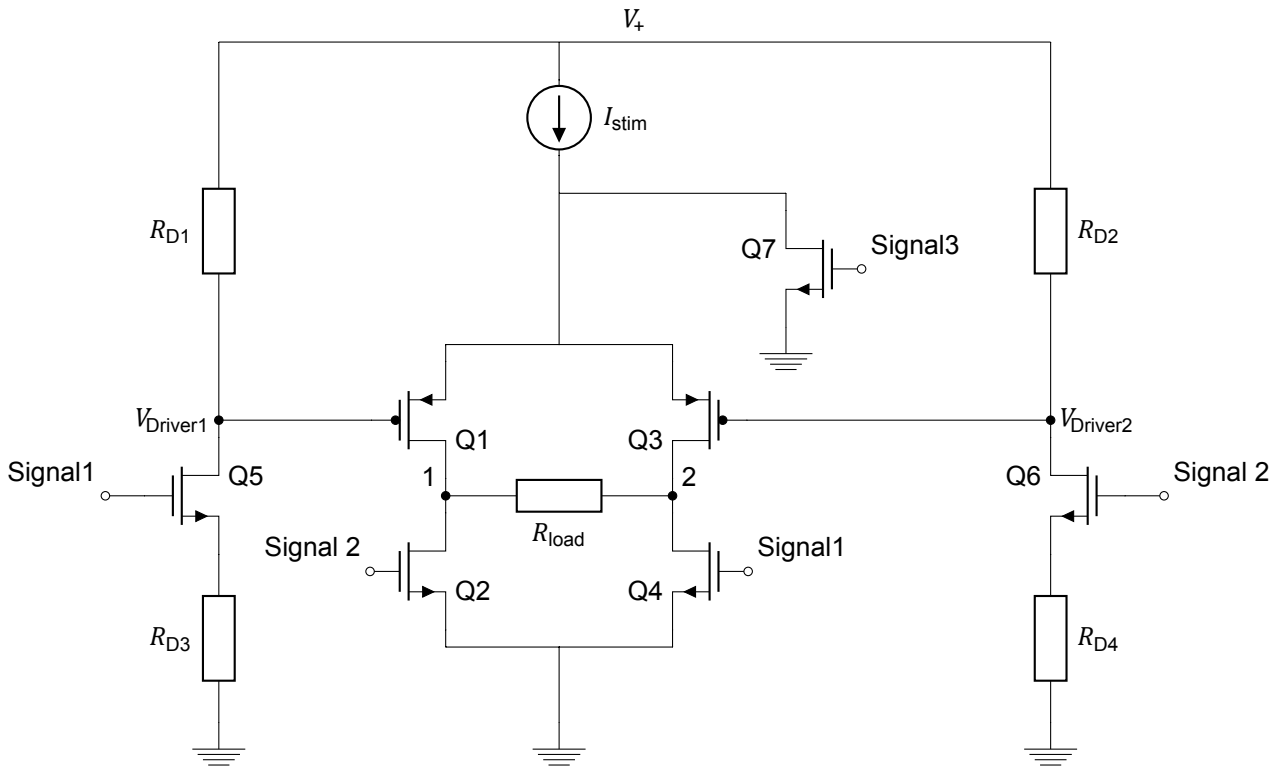


Figure 7.3: The implementation of the H-bridge using driver circuits based on voltage dividers and NMOS transistors.

Figure 7.3 shows the circuit with MOSFETs and a driver implementation for the top PMOS transistors. When Signal 1 is a logic high, the voltage on V_{Driver1} is lower than the input voltage, due to the voltage division of Equation 7.1

$$V_{\text{Driver1}} = \frac{R_{D3}}{R_{D1} + R_{D3}} \cdot V_+ \tag{7.1}$$

This negative voltage relative to V_+ will create a conducting channel in the PMOS transistor, Q1. At the bottom, Q4 is connected to Signal 1 and is conducting as well due to the positive voltage relative to ground. The other transistors will not generate conducting channels, since the gate voltage of the Q3 equals V_+ and of Q2 is 0 V. When Signal 2 is high, the opposite happens, reversing the current through R_{load}. If both Signal 1 and Signal 2 are high, all transistors conduct, effectively shorting R_{load}. In order to generate the full biphasic signal, Signal 1 and Signal 2 need to turn on and off in te pattern shown in Figure 7.4

A different implementation of a driver circuit would be to omit the second resistor, R_{D3} and R_{D4}. The result of this is that V_{Driver1} either equals V_+ or 0 V. Even though this means that the PMOS starts conducting with a lower supply voltage, there is also the risk that the maximum gate-to-source voltage is surpassed. By using a voltage division, the maximum gate-to-source voltage can be controlled for a known input voltage range.

Another addition in Figure 7.3 is that the current source can be shorted by using an NMOS together with Signal 3. This has been added to ensure that the current source will not try to generate current through the high impedance of the closed transistors. Because the current source will generate a maximum of 10 mA, a resistor limiting the current is not necessary. Signal 3 has to be high when Signal 1 and Signal 2 are low.

7.2.2. Component Selection

The circuit as shown in Figure 7.3 is able to operate like intended. However, correct components still have to be decided on. Transistors Q2, Q4, Q5 and Q6 are directly driven by the

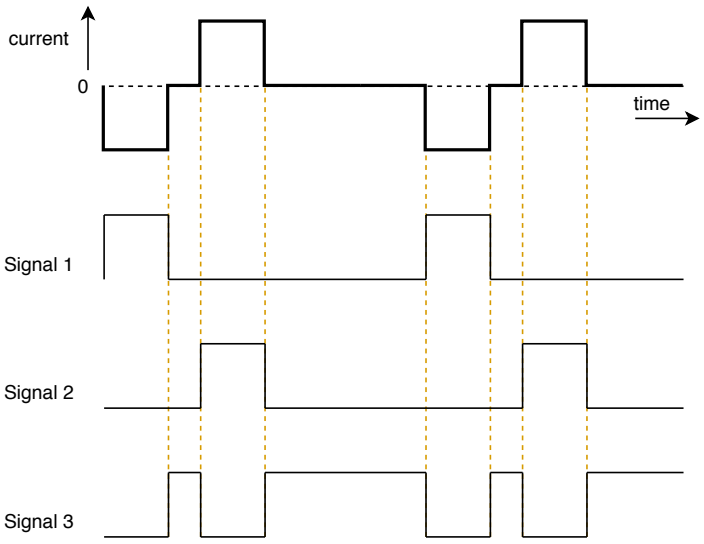


Figure 7.4: The driving signals needed for a biphasic pulse. Signal 1 creates a cathodic pulse, Signal 2 an anodic pulse and Signal 3 grounds the current source, disconnecting it from the H-bridge.

microcontroller. Therefore, the V_{GS} threshold should be lower than the 3.3 V that the microcontroller outputs.

The transistors in the H-bridge should have similar switching times and threshold voltages. This is to ensure that the Anodic and Cathodic pulses have the same set-up times and delays. For this reason, the Dual N and P Channel transistors inside the DMHC3025LSD have been used [49]. Not only does this component have 2 of the same NMOS and 2 of the same PMOS devices at once, but due to the integration, the components will be at the same temperature during operation, matching the operation times at all temperatures. The threshold voltage for the NMOS transistors equals 1 to 2 V and for the PMOS transistors -1 to -2 V. In addition to this, the transistors are rated for use until 30 V drain-source voltage and ± 20 V gate-to-source voltage.

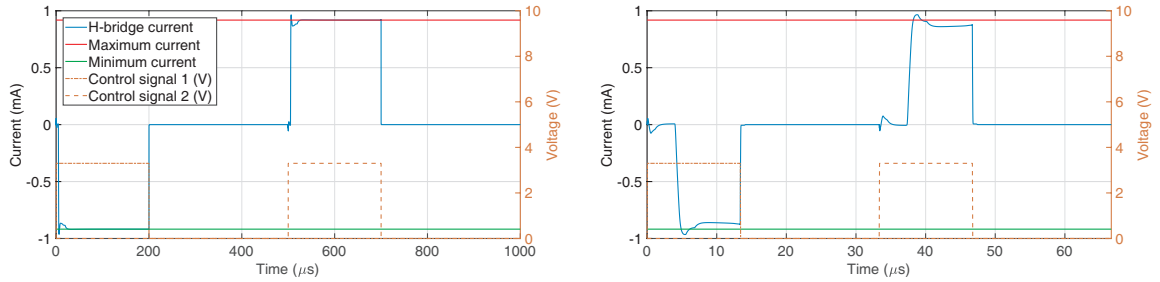
For the same reasons, the NMOS driver transistors Q5 and Q6 also share a DMHC3025LSD package. The PMOS transistor gates and sources in that package are connected to V_+, disabling the transistor.

The current source of the stimulator can deliver a maximum of 15 V [1], since $V_+ = 15$ V. This means that in order to turn on the PMOS transistors, a maximum of $15 - 2 = 13$ V should be presented to the gates, preferably lower.

A similar requirement holds for the NMOS in the driver, Q5 and Q6. Because the gate-to-source voltage should at least be 2 V, the source should not exceed 1.3 V, since the gate receives a logic signal that is either 0 V or 3.3 V. The source voltage is roughly equal to V_{Driver} when the transistor is on, due to R_{D3} and R_{D4}.

The minimum current that the stimulator has to deliver is 0.1 mA, as stated in the Program of Requirements (chapter 2). The minimum impedance for the tissue can be under 100 Ω at high frequencies [50]. This means that the voltage over the electrode will be less than $0.1\ \text{mA} \cdot 100\ \Omega = 10$ mV. It is not possible for the driver circuit to present a voltage that is 2 V lower than this, so the current source will generate a higher voltage until the PMOS starts conducting. Then, a voltage drop that equals the extra generated voltage will be present over the drain and source of that PMOS.

As becomes apparent, the exact values of the resistors are not important to the operation



(a) Simulation of the H-bridge output current at 1 kHz frequency.

(b) Simulation of the H-bridge output current at 15 kHz frequency.

Figure 7.5: Output of a simulation of the H-bridge topology of figure 7.3 through a 1 kΩ load.

of the H-bridge, as long as the voltage division between them results in a voltage lower than 1.3 V, abiding the requirement for the NMOS. The chosen values of R_{D1} and R_{D3} are 27.4 kΩ. Because transistors Q4 and Q5 are placed on the same chip, the sources are connected to each other. Therefore, only one resistor is needed instead of R_{D3} and R_{D4}. This resistor, $R_{Dbottom}$ in Figure 7.8, was chosen to be 1 $k\Omega$. This means that $V_{\text{Driver}} = (R_{D4})/(R_{D1}+R_{D4}) \cdot V_{+} = 1/(28.4) \cdot 15 = 0.53$ V, lower than the required 1.3 V. For maximum stimulation, this value is easily lower than the 13 V needed as well. For the minimum stimulation, the current source will have to deliver $0.53 + 2 = 2.53$ V. Since only 10 mV will be used by the electrode, a voltage drop of 2.52 V will be present over the drain-source of the PMOS.

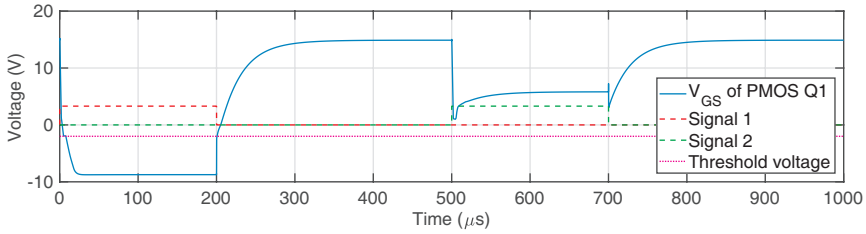
In addition to this, the voltage division of the driver circuit enables the circuit to handle a maximum of 20.5 V, since the PMOS components have a gate-to-source limitation of 20 V. Therefore, a supply of 20 V is safe to use.
Transistor Q7 was chosen to be a N channel MOS 2N7000 [51]. This transistor is similar in speed to the other transistors and the gate threshold voltage is between 0.8 V and 3 V. It is able to handle up to 200 mA through the drain and the maximum drain-source voltage is 60 V.

7.2.3. Simulations

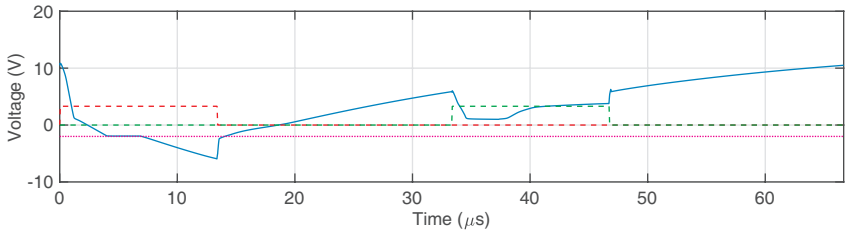
In order to test if the circuit operates the way it is intended to, a simulation of the topology has been made, including the chosen components. After the simulation has been verified, real measurements can be made and compared. The software used for the simulations is LTSpice [52]. The net-list and used libraries can be made available on request. The contact information can be found in appendix A.1.

The circuit has been simulated using signals like in Figure 7.4 at 1 kHz frequency, using the circuit topology of Figure 7.3. The output of this simulation matches the ideal behavior closely when using this frequency. The results are in Figure 7.5a. Here, the 'Maximum current' and 'Minimum current' refer to the amount of current through the load if the current source was connected to the load directly, omitting the H-bridge. As is visible, the current through the load is a biphasic signal that matches the timing of the control signals. Apart from some switching artifacts, the h-bridge influences the signal very little. This is, however at the lowest frequency the system should operate on.

When the stimulation frequency is changed to 15 kHz, which is in the scope of the program of requirements, the performance is significantly worse than the lower frequency. The reason for this is because the switching artifacts do not scale with the frequency of the system. They depend on the turn-on time and turn-off time of the transistors, which in turn depend on he internal capacitances. The results are shown in Figure 7.5b. The main reason for the switching artifacts is that the driver signal does not immediately stabilize after the NMOS in the driver circuit starts conducting.



(a) V_{GS} of PMOS Q1 at 1 kHz



(b) V_{GS} of PMOS Q1 at 15 kHz

Figure 7.6: Comparison of the gate-to-source voltage of PMOS 1 (Q1).

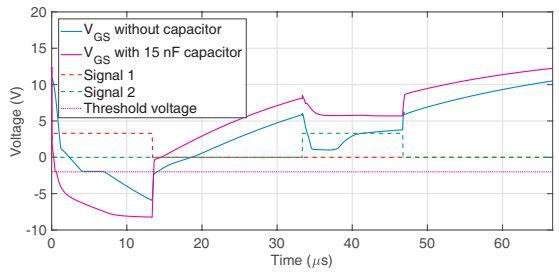
The result of this is particularly clear in the V_{GS} of the PMOS transistors in the H-bridge. Especially when looking at the 15 kHz result, the voltage levels are not as neat as when stimulating 1 kHz. This is visible in Figure 7.6. In this figure, the gate-to-source voltage has to drop below -2 V when Signal 1 is high. The reason for this behavior is due to the resistor that is connected to the ground and the sources of the NMOS driver transistors. Together with the output capacitance of the transistor, it increases the RC time constant, effectively delaying the transistor switch. The output capacitance typically equals 137 pF, and with a resistor of 1 kΩ in series, the RC time constant equals $\tau = RC = 1 \times 10^3 \cdot 137 \times 10^{-12} = 137$ ns [53]. This constant adds an instability to the driver signal of the PMOS, resulting in a long delay and a fluctuating switch, like apparent in Figure 7.5b

Ideally, the resistor should be less prominent at these higher frequencies. In order to achieve this, a capacitor is placed in parallel to this resistor. The capacitor will make sure that high frequency signals will not influence the resistor as much, decreasing the time taken for the driver voltage to stabilize. This can be simplified as a low-pass filter with a cutoff frequency that equals $f_c = \frac{1}{RC \cdot 2\pi}$. It filters out the high-frequency components of the driver signal.

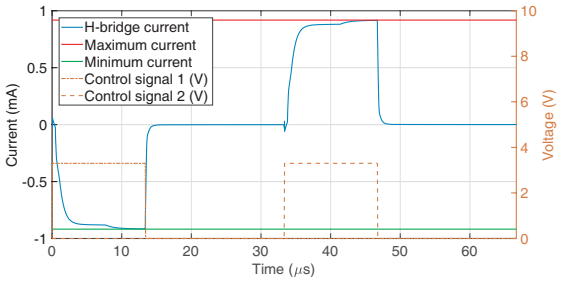
When the capacitor value is too low, it adds no effect, as the cutoff frequency is higher than 15 kHz. If the capacitor value is too high, it will affect low frequencies as well, which is counterproductive since the switching time is faster without the use of a filter on these low frequency signals. The chosen capacitance is 15 nF. Therefore the cutoff frequency of the part equals $f_c = \frac{1}{RC \cdot 2\pi} = \frac{1}{1 \times 10^3 \cdot 15 \times 10^{-9} \cdot 2\pi} = 10.6$ kHz. From simulations, this value had enough effect on higher frequencies and did not alter lower frequencies a lot. The effect for a 15 kHz stimulation on the gate-to-source voltage with and without capacitor can be seen in Figure 7.7a

The result in the output of the H-bridge is that the turn-on time at low frequencies is slightly faster, but at higher frequencies, the waveform is a lot cleaner and quicker, like displayed in Figure 7.7b. When stimulating at an amplitude of 10 mA on a 1 kΩ load, the switching times are summarised in Table 7.1

Like visible, the switching time improves with higher frequencies, but at 15 kHz, still almost 10 % of the pulse is needed to switch the signal. Because this effect is present at both the cathodic and anodic pulse, there will not be extra charge accumulated due to the switch-



(a) Comparison of the gate-to-source voltage of PMOS 1 (Q1) when using a 15 nF capacitor or none.



(b) Simulation of the H-bridge topology of figure 7.3 at 15 kHz frequency with a 1 kΩ load and a 15 nF capacitor.

Figure 7.7: Simulations aat 15 kHz with a pulse width of 20% of the period.

Table 7.1: Time until the signal reaches 63 % of its maximum value with a pulse width of 20% of the stimulation period.

Stimulation parameters		Without capacitor		With capacitor	
Frequency	Pulse width	Time	Percent of total pulse	Time	Percent of total pulse
1 kHz	200 μs	5.34 μs	2.7 %	1.52 μs	0.8 %
3 kHz	66.6 μs	5.31 μs	7.8 %	1.51 μs	2.2 %
6 kHz	33.3 μs	5.11 μs	15.3 %	1.44 μs	4.3 %
9 kHz	22.2 μs	4.88 μs	22.0 %	1.28 μs	5.8 %
12 kHz	16.7 μs	4.73 μs	28.3 %	1.27 μs	7.6 %
15 kHz	13.3 μs	4.63 μs	34.7 %	1.27 μs	9.5 %

ing times.

The final circuit topology, including the capacitor, is shown in Figure 7.8.

7.3. Implementation

The simulation of the H-bridge features all individual transistors. The actual transistors used are in a package of two NMOS and two PMOS transistors. The transistors in this package are already arranged the way the transistors are going to be used. For the driver NMOS transistors, the same package is used, however the PMOS tansistor sources and gates are connected to the 15 V input voltage. Figure 7.9a shows how the transistors are connected in the package [49].

In total, the circuit is connected as is shown in Figure 7.9b.

7.4. Measurements

From simulations, the most important parameters to test for the H-bridge to work correctly are the amplitude of the final signal compared with the current source output and the time 63% of the final amplitude is reached.

A series of measurements have been performed by connecting the 3.3 V and 5 V part of the power management system, the microcontroller, DAC, current source and h-bridge. A 1 kΩ fully resistive load was connected to the electrodes. An ISO-TECH IPS-4303 power supply was used to supply 15 V for the voltage to current converter and H-bridge.

An Extech EX210 multimeter was used to measure current delivered from the current source to the H-bridge. A Tektronix TDS2014C four-channel oscilloscope was used to view and measure the output at the electrodes and the drivers of the H-bridge.

As a first test, H-bridge output was compared to the current that the voltage to current

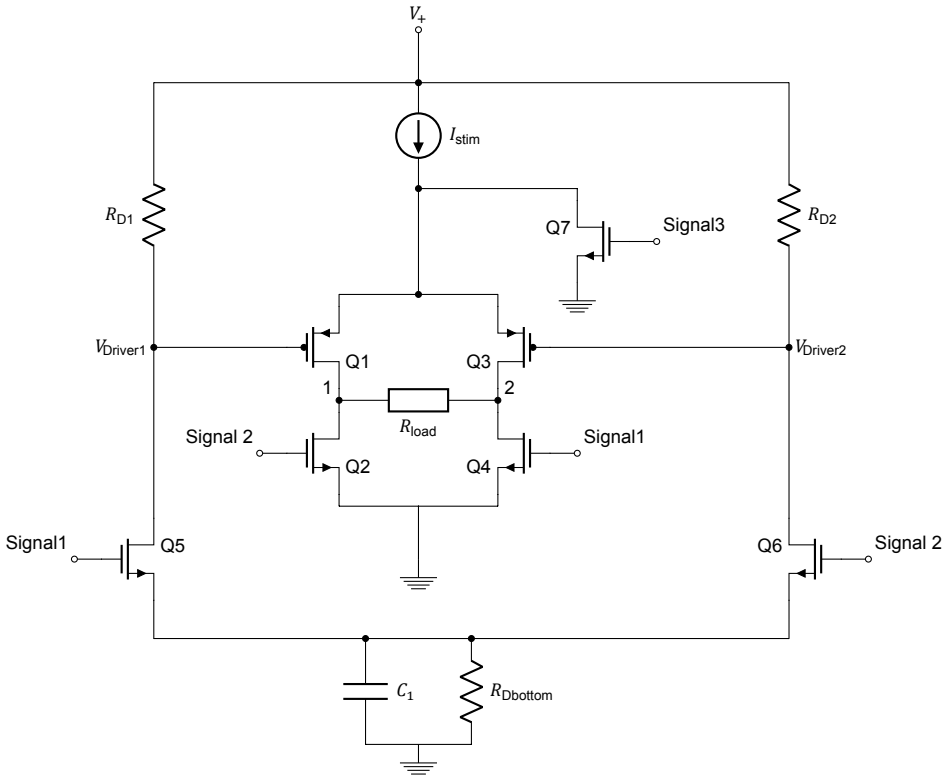


Figure 7.8: The total implementation of the H-bridge.

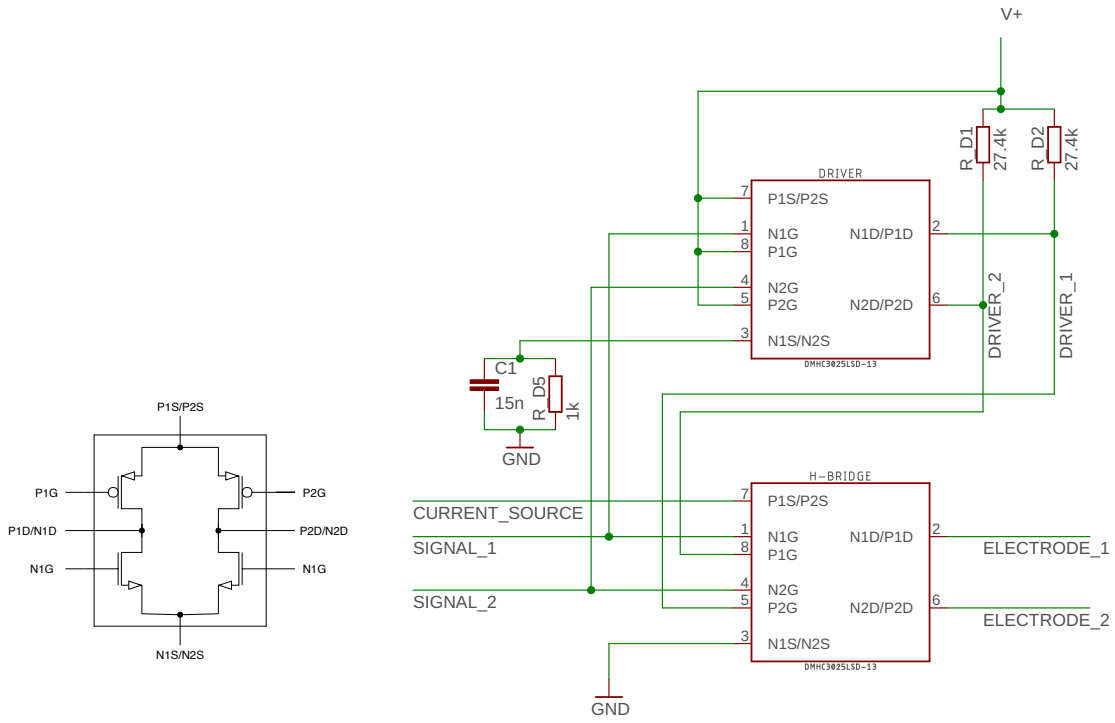
Table 7.2: Measured time until the signal reaches 63 % of its maximum value.

Stimulation parameters		Cathodic pulse		Anodic pulse	
Frequency	Pulse width	Time	Percent of total pulse	Time	Percent of total pulse
1 kHz	127.4 μs	2.42 μs	1.9 %	3.12 μs	2.4 %
3 kHz	42.4 μs	2.30 μs	5.5 %	2.80 μs	6.6 %
6 kHz	21.2 μs	2.24 μs	10.6 %	2.20 μs	10.4 %
9 kHz	14.1 μs	1.98 μs	14.0 %	2.12 μs	15.0 %
12 kHz	10.6 μs	1.80 μs	17.0 %	2.04 μs	19.2 %
15 kHz	8.4 μs	1.80 μs	21.4 %	2.04 μs	24.3 %

source delivered. The source was set to 9.47 mA. The voltage over the 1 kΩ load was measured using the oscilloscope. The measurements from the oscilloscope only have a 0.1 V accuracy, which translates to an accuracy of $I = \frac{V}{R} = \frac{0.1\ \text{V}}{1\ \text{k}\Omega} = 0.1$ mA. The measurements resulted in a constant maximum current, independent of the tested frequency. The minimum current for the cathodic pulse was -9.6 mA and the maximum current for the anodic pulse was 9.4 mA.

Another measurement that has been done is the time the system takes to reach 63 % of the maximum amplitude of a pulse. Judging from the visual measurements in Figure 7.10, the switching time is significant for higher frequencies.

Table 7.2 shows the actual switching times that the H-bridge has for different frequencies and pulse widths. Similar switching times can be lead back to the V_{GS} of the two PMOS transistors, visible in Figure 7.11. There is a difference in time a cathodic pulse takes and an anodic pulse takes to reach 63 % of its value. The result of this is that the waveform is not fully balanced, but can differentiate to 0.6 μs in the worst case.

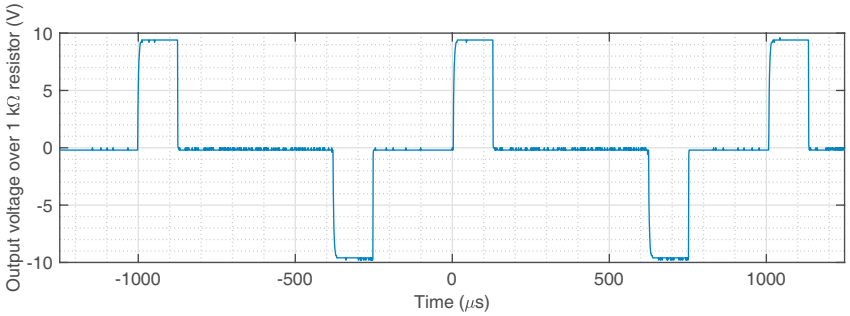


(a) The DMHC3025LSD-13 package.

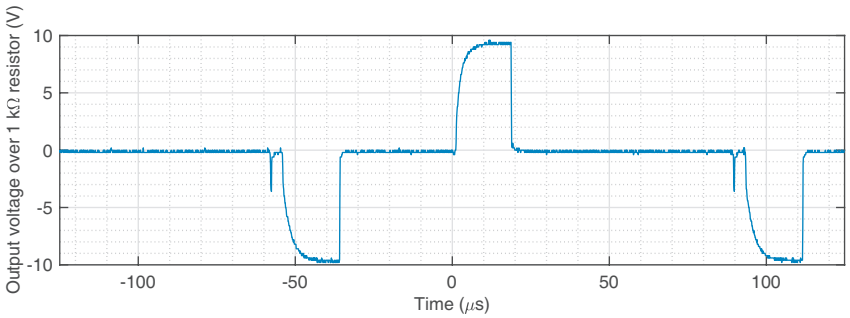
(b) Full implementation of the H-bridge using the DMHC3025LSD-13 package.

Figure 7.9: Implementation of the h-bridge cicruit.

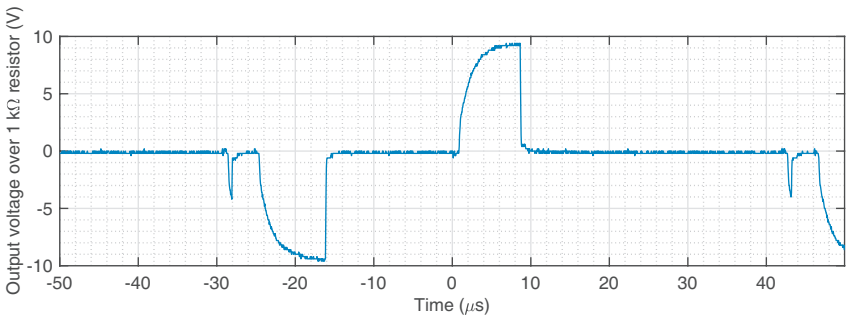
Next to the time to reach the maximum amplitude, the time to return back to 0 is important as well. Since a single transistor is used to connect the current source to the ground, this transition is a lot quicker. The time to return the pulse back to 0 has found to be a constant 0.2 μs.



(a) H-bridge output with a 1 kΩ load at 1 kHz with a pulse width of 127.4 μs

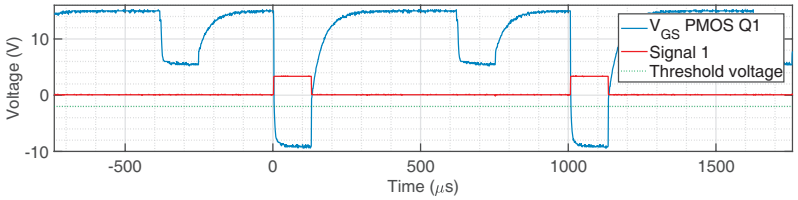


(b) H-bridge output with a 1 kΩ load at 7 kHz with a pulse width of 18.1 μs

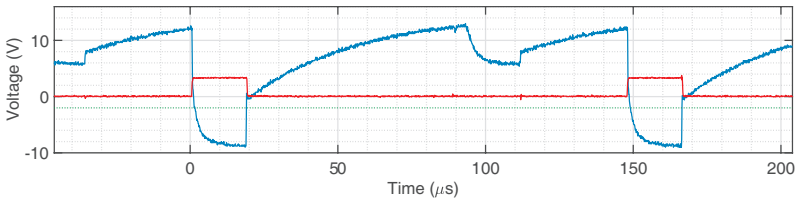


(c) H-bridge output with a 1 kΩ load at 15 kHz with a pulse width of 8.4 μs

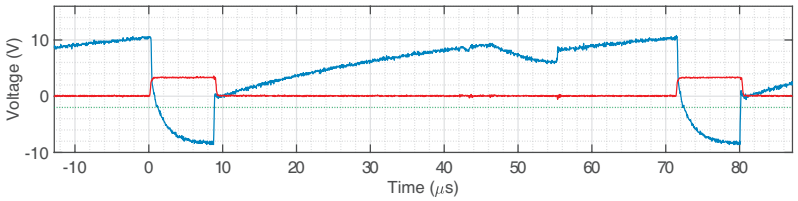
Figure 7.10: Measurements of the H-bridge output with a 1 kΩ load and 9.47 mA stimulation current.



(a) PMOS driver signal at 1 kHz with pulse width of 127.4 μs



(b) PMOS driver signal at 7 kHz with pulse width of 18.1 μs



(c) PMOS driver signal at 15 kHz with pulse width of 8.4 μs

Figure 7.11: Measurements of the V_{GS} of PMOS Q1.

8 Discussion

This chapter provides a discussion about the research described in this report and proposes possible improvements.

8.1. Switching Effects of Voltage Regulators

The voltage regulators are not tested for every possible situation. When the input of the regulator rapidly switches from one voltage to another, the output could behave non nominal. This is however not tested. A situation where the input voltage switches is when the device is turned on. Then the input voltage increases from 0 V to the battery voltage of about 9 V.

8.2. Reference Voltage of the Digital to Analog Converter

The selected 3.3 V LDO regulator gives an average output voltage of 3.336 V. The voltage generated by the DAC will equal this reference voltage for the maximum amplitude setting. So, when a stimulation current of 10 mA is desired, the DAC will give an output voltage of 3.336 V. With this voltage, the voltage to current converter will generate a current which is slightly higher than 10 mA. This happens, because the system is designed to generate a stimulation current of 10 mA when a voltage of 3.3 V is generated by the DAC. The system should have been corrected for this offset by for example subtracting this offset from the binary code that the microcontroller sends to the DAC.

8.3. Error in Output Voltage of the Digital to Analog Converter

Figure 6.3b shows the difference between the measured and expected output voltage of the DAC. This error is measured to be maximum 20 mA. However, this measurement was not very accurate as it was done with the Extech EX210 multimeter which only displays three digits and therefore only shows the voltage in steps of 10 mA. It is recommended to do an improved measurement with more accurate equipment.

8.4. Spike in H-bridge Signal

Like visible in Figure 7.10, there is a small spike in front of the Cathodic pulse. This spike is already visible in the microcontroller signal. The exact reason for the spike is not known yet. It might be related to the code or the transistors of the H-bridge. The effects of the pulse are minimal, since it already adds a negative charge to the tissue. When the real cathodic pulse begins, a small negative charge is already present. In addition to this, the tissue can be simplified as a low-pass filter. Therefore, high frequency spikes, like the one visible are filtered out.

8.5. Speed of H-bridge

Like the simulations and measurements show, the transition time of the transistors in the H-bridge are not quick enough to generate a pure square pulse at higher frequencies. Since both the cathodic and anodic pulse are influenced by this effect, the pulse is still balanced. However, due to measurements for the individual pulses, shown in Table 7.2, the anodic pulse took longer to fully transition. This is probably due to the fact that the transistors used have small deviations in comparison with each other. In general, the Anodic pulse should be shorter than the Cathodic pulse, since a part of the charge injected during the Cathodic pulse is dissipated in the body and does not need to be cancelled.

The time for the pulse to reach 0 again is 0.2 μs. This is quick enough even for 15 kHz, as it only takes 2.4 % of a total pulse of 8.4 μs.

8.6. Current Drop due to the H-bridge

Even though MOSFET transistors are used for the H-bridge, the components are not ideal and some current drop in comparison with the current source is expected. In order to find the order of magnitude of this value, the generated current was measured with a multimeter and the current through the electrodes was measured using an oscilloscope. Due to a limited precision of this measurement (0.1 mA), no conclusive result could be found other than that the current drop could be between 0 and 0.2 mA.

9

Conclusions and Future Research

To conclude, this thesis described the design of an arbitrary waveform generator for a high frequency arbitrary waveform neural stimulator. Each subsystem of the waveform generator is designed, implemented and tested individually, after which the entire system has been tested. It can be concluded that the designed system fulfills all primary requirements. Some secondary requirements can be implemented with only a small change to the system, while others require more effort to implement. The secondary requirements are listed to get an overview of what is achievable without many adjustments.

- **Monophasic waveform** - Implementing a monophasic waveform only requires the current amplitude to be positive or 0 mA. This could be made possible by letting the current through only one side of the H-bridge and can therefore be implemented in the designed system.
- **Other types of waveforms** - As described in the state-of-the-art analysis, in section 1.2, other types of waveforms do not have a significantly higher efficacy or safety. They are mainly investigated to improve energy efficiency. It will also be difficult to implement waveforms other than block shapes, since the amplitude then needs change during a stimulation period. It is therefore seen as a more difficult option to implement other types of waveforms.
- **Low frequency stimulation** - This requires a different timing from the microcontroller. The timers which are currently used are not big enough to implement low frequency stimulation without any changes. A clock divider can be implemented in the microcontroller without much effort, in order to adjust the frequency of the generated waveform.
- **Voltage-based stimulation** - This can be implemented by replacing the voltage to current converter by a voltage to voltage amplifier with a gain of 3. The 3.3 V from the DAC will then be amplified to 10 V.

During this project, many improvements of the arbitrary waveform generator were thought of. However, because of the limited time, these could not be implemented. Therefore, a recommendation of future research is provided here.

- **General circuit topology** - In this research, a DAC, a voltage to current converter and an H-bridge generate the biphasic stimulation current. However, another topology has been thought of, but is not researched in detail. This is a topology where the entire stimulation pulse will be generated as a voltage and then converted into a current by a voltage to current amplifier with appropriate feedback. The feedback could be made adjustable to be able to set the amplitude.
- **Power management - low-pass filter** - The implemented voltage regulators do have noise on their outputs, which might get reduced with a low-pass filter on the output

of the regulators. Some data sheets even provide a suggested low-pass filter. It is recommended to do more research in methods to get even more stable supply voltages for the system.

- **Power management - component selection** - It is recommended to give more attention to the selection of components for the voltage regulators as the precise values determine the behavior of the regulators. More detailed simulations and measurements need to be done in order to determine the best components.
- **Speed of H-bridge** Like visible from the measurements, the H-bridge is not quick enough to switch the current instantaneously. Especially at higher frequencies, the time 63 % of the maximum amlitude is reached, is very high in comparison to the total pulse width. A different topology of a current direction switcher might have been quicker. At the same time, modifications to for example the driver circuit could have made the device faster. These options have not been researched yet.

In addition to this subsection-specific review of requirements, an overview of the general requirements for the whole project is included in the appendix at section A.2 For each requirement stated in section 2.1, the result is clarified in addition to the subgroup(s) responsible.

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List of Descriptions and Abbreviations

ADC Analog to Digital Converter. 20

Anodic The positive part of the pulse. 9, 30, 39

Cathodic The negative part of the pulse. 9, 30, 38, 39

DAC Digital to Analog Converter. 3, 7, 9, 12, 17, 20–22, 24–26, 38, 40

ESR Equivalent Series Resistance. 14–16, 25

I^{2}C Inter-Integrated Circuit. 24

IC Integrated Circuit. 15

LDO low-dropout. 12–18

LPF Low Pass Filter. 13

MOSFET Metal Oxide Semiconductor Field Effect Transistor. 28

MS Multiple Sclerosis. 1

NMOS N-channel MOSFET. 28–30, 32, 33

PCB Printed Circuit Board. 17

PMOS P-channel MOSFET. 28, 30, 32, 33

PMS Power Management System. 11

SCI Spinal-Cord Injury. 1

SMD Surface Mounted Device. 14

SPI Serial Peripheral Interface. 20, 21, 24, 25

UART Universal Asynchronous Receiver-Transmitter. 24

List of Variables

R_{load} The load attached to the H-bridge. 29

V_{GS} Gate-to-source voltage. 28, 30, 32, 34, 37

V_{ref} Reference voltage. 15–17, 22

f_c The cutoff frequency. 32

A

Appendix

A.1. Contact Information for SPICE and LPC Programming Files

Please contact Prof. dr. ir. W.A. Serdijn, Chairman Bioelectronics (BE), Department of Microelectronics, TU Delft.

A.2. Conclusions of General Requirements

After the project completion, most general requirements highlighted in section 2.1, have been realized by all three submodules. Table A.1 clarifies which requirement was carried out by which subgroup and shows if the requirement was met or not.

Table A.1: The General Requirements for the Project and Whether it has been Completed

Requirement	Accomplished	Subgroup(s) involved
The device should have 2 identical connections for 2 extension cables which are connected to a lead. The lead has an array with 4 electrodes (Lead used is Medtronic Model 388928).	No, only 1 lead can be connected	Control & Interface module
The leads must be connected with an extension cable which should fit the connectors of the device.	Yes	Control & Interface module
The device must be able to stimulate on all possible terminals of the lead.	Yes	Control & Interface module
The device must support monopolar and bipolar stimulation.	Yes	Control & Interface module
The device must operate outside the sterile field around the patient	Yes	Control & Interface module
The device must not cost more than €5,000.	Yes	Control & Interface module Arbitrary Waveform Generator Safety module
The device must not be larger than $0.5 \times 0.5 \times 0.3$ meters (length x width x height).	Yes	Control & Interface module Arbitrary Waveform Generator Safety Module
The device must not weigh more than 10 kg.	Yes	Control & Interface module Arbitrary Waveform Generator Safety module
The components of the device must ensure a liftetime of at least 6 months.	Probably, but not tested	Control & Interface module Arbitrary Waveform Generator Safety module
The device must be able to operate between 10° C and 40° C.	Yes	Control & Interface module Arbitrary Waveform Generator Safety Module
The internal temperature of the device must be kept in a range where the device is still fully functioning (so where the device meets all specified requirements).	Probably, but not tested	Control & Interface module Arbitrary Waveform Generator Safety Module
The device must not create sounds which exceed 40 dB [34].	Yes	Control & Interface module Arbitrary Waveform Generator Safety Module
The device must be made from off-the-shelf components.	Yes	Control & Interface module Arbitrary Waveform Generator Safety Module