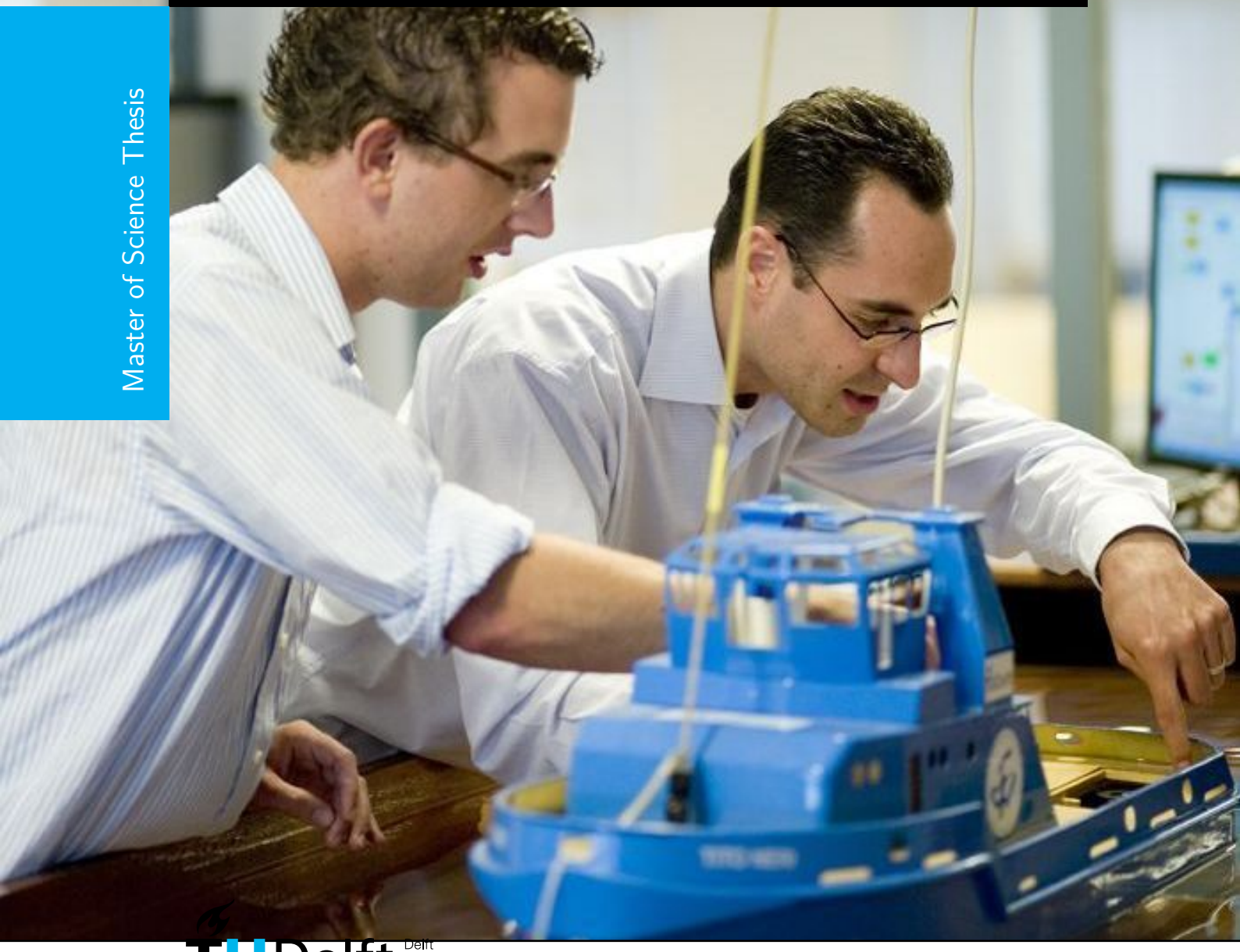
8uW to 1mW Input Power Management IC Design for RF Energy Harvester

Yang Jiang

Master of Science Thesis



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Department of Microelectronics

8uW to 1mW Input Power Management IC Design for RF Energy Harvester

Master of Science Thesis

For the degree of Master of Science in Microelectronics at Delft University of Technology

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August 31, 2016

Faculty of Electrical Engineering, Mathematics and Computer Science (EEMCS) · Delft University of Technology

The work in this thesis was supported by IMEC Holst Center. Their cooperation is hereby gratefully acknowledged.

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Abstract

This master thesis project aims to design a power management block which is suitable for RF energy harvesting application with input power range from 8uW to 1mW. RF energy harvesting applications are low power Wireless Sensor Network or Transceiver with working duty cycle and average power consumption is from tens of uW to hundreds of uW. Based on the transceiver working condition, general power management block system can be designed in a two stages architecture including the Harvest Interface Stage and Load regulation Stage with storage element in between. The purpose of Harvest Interface is to regulated input voltage according to varying input power condition and Load regulation in system is to regulated output voltage for the target application. The Storage Element in between can store energy coming from Harvest Interface and discharge it according to the load. In terms of low input power situation (8uW in this project), the total power management system should be designed to be ultra low power loss.

This project focused on the design of Harvest Interface Stage with the full bridge MOSFET rectifier to be the input of Harvest Interface and output connected to the Storage Element. Power loss estimation was done to evaluate topologies of Harvest Interface Stage. Then, inductive DC/DC boost converter was chosen to be the topology. Next, the switches control principle was analysed and low power switches control design was implemented to regulated input voltage of DC/DC boost converter. In addition, in order to track the varying input power, a power detector has been made which consists of 9bits ADC, DAC, RC integrator and Maximum Power Point Tracking [MPPT] digital design to continuously track the maximum power point by comparing new cycle power value with previous cycle power value. The output of power detector will give a input voltage reference for DC/DC boost converter to regulate its input voltage. The saturated input voltage reference indicates the maximum PCE from rectifier to DC/DC boost converter.

Finally, Schematic and Layout were done in this project and simulations were implemented for both schematic and layout. Maximum Power Point Tracker [MPPT] can track 8uW power source with only 1 percent power loss inaccuracy and for 1mW power source, 7.5 percent inaccuracy power loss will occur. DC/DC converter [Without MPPT] power conversion efficiency post layout simulation(RC Extraction) for 8uW input power is 70 percent and 89 percent for 1mW input power source.

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Acknowledgements

First of all, I would express my great appreciation to Wouter Serdijn who is my supervisor in TU Delft. He is a innovative, kind person and willing to spend his time with his students even when he is busy. We often have a meeting every month and Mr Wouter Serdijn would come from TU Delft to Eindhoven to attend the meeting and help me, encourage me with this project. He also helped me with this report and improved me a lot with the thesis writing. I am very lucky to be one of his student.

Then, I would give my great thanks to Johan Dijkhuis who is one of my daily supervisors in IMEC Holst-center. With his help, I have overcome the design difficulties from system level to schematic level and layout. He is a kind, talkative, creative person and technical professional in Mixed signal and RF IC design field. I have learnt a lot from him not only the methods to solve problems, organize a project but also the way of thinking and talking.

Many thanks for Professor Guido Dolmans who is also one of my daily supervisor in IMEC Holst-center. He gave me a good chance to do this project and arrange technical people to help me when i faced difficulties.

Moreover, I would thank the people in Radio System Group in IMEC Holst-center. Many thanks to Jialue Wang who takes charge of whole RF energy harvester system design and also my senior in TU Delft. He gave me a lot of suggestions and help during the meeting and after the meeting. Thanks to Stefano Traferro who help me with RTL synthesis and $back - end$. Thank my colleagues: Ming Ding, Ao Ba, Stefano Stanzione, Benjamin Busze for helping me with simulation and giving design advice.

Finally, I would like to thank my parents who support and encourage me all the time in my life and i would continuously develop myself and become stronger in the future.

Delft, University of Technology — Yang Jiang
August 31, 2016

Chapter 1

Introduction

1-1 Background

With the development of technologies including MEMS sensors, Data science and Computer Engineering, electronics components are becoming smaller, lighter, more integrated and power efficient. With more sensors to be integrated, the sensor network can sense useful physical information, convert physical signals to electrical analog signals, convert these electrical signals into digital signals and then, feed these digital signals to a microprocessor or micro-controller. There are plenty of devices with sensors such as smart phone, smart watch, smart home furniture and health care applications [7]. They gradually influence people during working, learning and sleeping in a good manner which tends to be more convenient, more power efficient, more comfortable and safer to people in the future.

However, Power Supply Solution is still a problem for mobile devices such as Wireless Sensor Network(WSN) [8]. Short battery lifetime cannot enable the long time working for mobile device and a big battery solution would results in large space and high cost. A better solution to the problem is by applying Wireless Power Transfer technology (WPT) which can enable mobile devices to charge themselves without using a charge cable or while on the move and never switch off. At present, there are four categories of WPTs: Near field magnetic coupling; Near field resonant inductive Coupling; Near field capacitive coupling and Far field EM coupling [8].

Near field magnetic coupling method: Inductive coupling method is widely applied in commercial product such as wireless charging toothbrush, mobile phone and pads. The advantages of high power conversion efficiency, simple structure and high power charging density and the disadvantage is short charging distance which is few centimeters [8].

Near field resonant inductive Coupling: This method can enable to charge a wireless device with few meters range [few times of Coil diameter] to maintain a high power conversion efficiency which means large coil is needed to achieve long distance power transmission. In addition, charging distance is still defined by the alignment settings of two inductive coils

which means alignment settings should be dynamically adjusted when two coils are moved to each other in order to achieve a high power conversion efficiency. At present, for this technology, the applications are mobile phone devices, electrical vehicles and WSNs.

Near field capacitive coupling: In capacitive coupling method, the energy is transferred in the form of electric field between two metal electrode plates including a transmitting electrode plate and a receiving electrode plate. An AC signal would be placed at the transmitting electrode plate and induce an oscillating electric field. The oscillating electric field would induce an AC electric potential at the receiving electrode plate. The amount of power can be transferred is determined by the capacitance, voltage amplitude and input frequency [9]. The disadvantage of near field capacitive coupling is small charging distance.

Far field EM coupling: The principle of EM coupling method is by applying two antennas: one receiving antenna, one transmitting antenna. The transmitting antenna transmits EM wave to the receiving antenna over some distance. Then, the receiving antenna transforms EM wave into an alternating current signal (AC) to realize far field wireless charging. The strength of this method can enable the large charging distance, mobile charging, multiple device charging, battery free, tiny receiving antenna size and longer lifetime for low power sensors network. The weakness of this technology is relative large attenuation resulting in small average power. However, even if the power strength is inversely attenuated by the distance squared, this strength is still possible to power ultra-low power sensors network by a power efficient RF Energy Harvester System. In addition, for electronic devices, such as a low power transceiver (mW) that have low duty cycle, energy harvested can also be temporally accumulated when the transceiver is idle.

1-2 RF Energy Harvester System

As shown in Figure 1-1, RF energy harvester system is composed of an antenna, a rectifier, a matching network between the antenna and the rectifier and a power management block. The power conversion efficiency of this system mainly depends on the received power strength, the sensitivity of the antenna, the size of the antenna, the efficiency of the rectifier, the matching networks and the power management block.

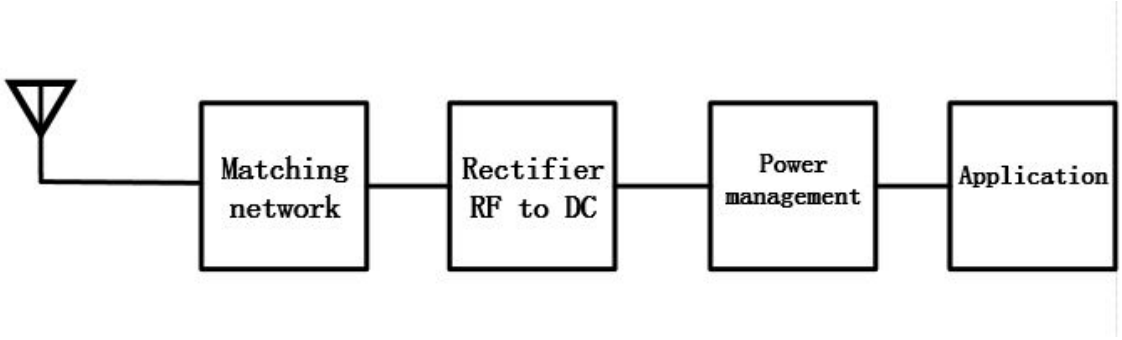

Figure 1-1: RF Energy System

1-2-1 Receiving Antenna

Power strength is influenced by the distance between power transmitter source and harvester. As shown in equation (1-1), Gt and Gr are antenna gains from transmitter and receiver, P_t represents transmitted power, λ stands for wavelength and d is distance between transmitter and receiver. $n = 2$ defines environmental condition which is in free space. In this case, the received power strength P_r would be attenuated by the square of distance d. The maximum distance can be estimated for certain wireless input power device.

$$P_r = P_t G_t G_r (\frac{\lambda}{4\pi})^2 \times (\frac{1}{d})^n \tag{1-1}$$

1-2-2 Rectifier

The functionality of Rectifier is to convert AC signal to DC signal. Figure 1-2 shows full bridge rectifiers structure with diodes connected. The left AC signal input would give right side DC output. Two working phases are shown below. In phase one, diodes D1 and D3 would be on state and D2, D4 off state. During phase two, D2 and D4 are switched on state but D1, D3 off state. For an ideal diodes used in full bridge, no power loss would exist but in reality, the diode is not ideal.

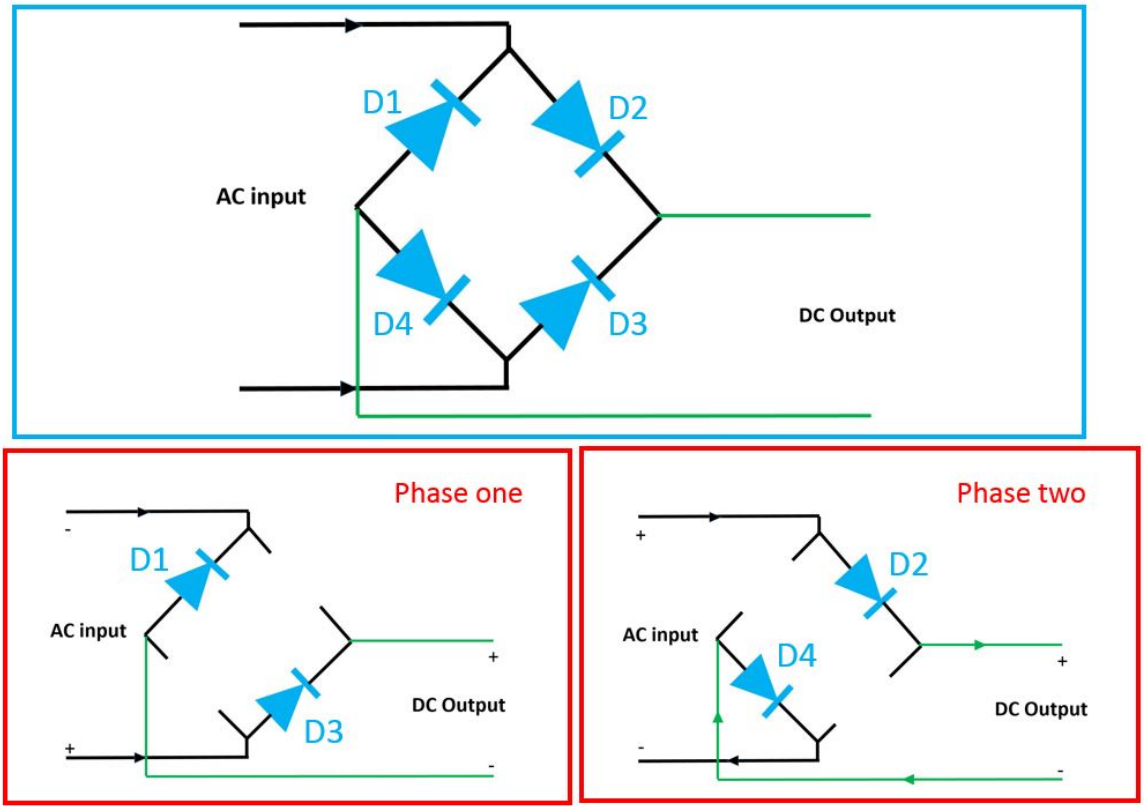

Figure 1-2: Full bridge Rectifier Structure

Figure 1-3 gives the equivalent electrical model of diode. The symbol L_p and C_p represents package parasitic inductance and capacitance. C_j is junction capacitance and R_s, the bulk series resistance. Both Junction capacitance and parasitic capacitance would also cause power loss. However, bulk series resistance is the denominator in total power loss also named conduction loss. For RF energy harvest rectifier, Schottky diode is technical commonly a choice with turn on voltage (Voltage across diode) range from 150mV to 350mV [10]. Conduction power loss of Schottky diode full bridge rectifier can be computed by Equation (1-2).

$$P_{schottky-rectifier} = 2 \times Vdiode \times \frac{1}{T}\int_0^T I_F dt \tag{1-2}$$

V_{diode} in Equation $(1-2)$ is the voltage across Schottky diode during forward biased and I_F stands for forward biased current. The average forward current can be computed by integrating current flow through diode over time T and then, divide the integration by T. Conduction power of diode can be calculated by average current times the voltage difference between two terminals of the diode and for rectifier conduction loss, it is two times of the single diode conduction power loss.

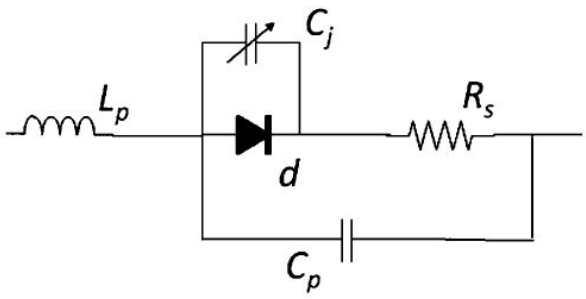

Figure 1-3: Equivalent Electrical Circuit of Packaged Diode [1]

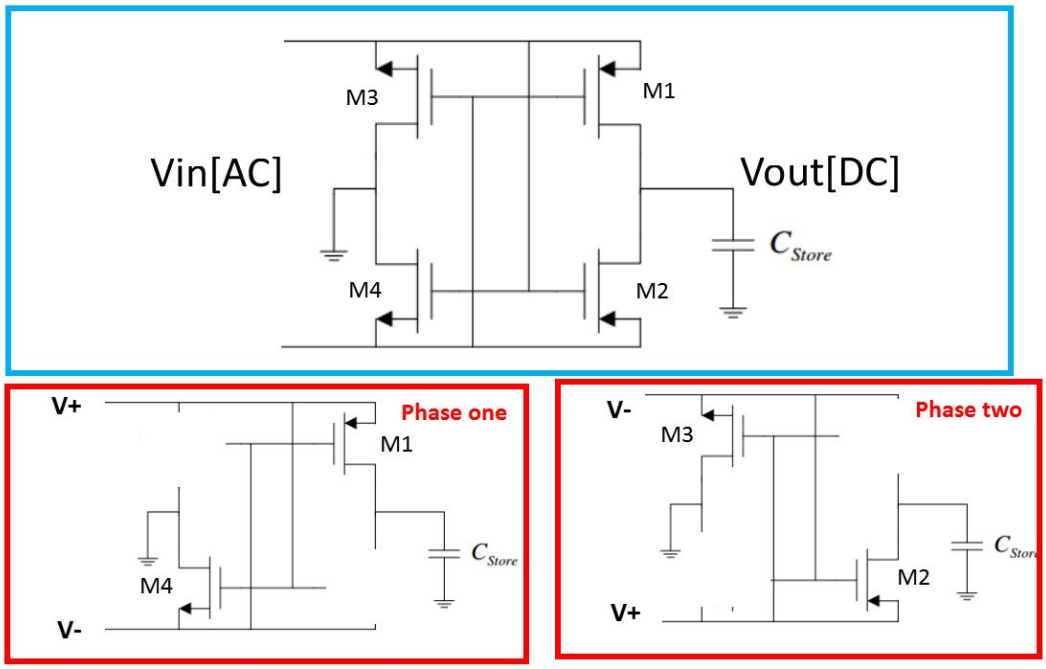

Figure 1-4: Full Bridge MOSFET Rectifier [2]

Except for applying Schottky diode, MOSFET diode can also be applied in rectifier design. Comparing to Schottky diode, the advantage is that MOSFET diode can be integrated on chip but Schottky diode cannot. Therefore, MOSFET diode rectifier is applied in this application. As shown in Figure 1-4, referring to Figure 1-3, the ideal diode can be replaced by four MOSFET transistors including two PMOS transistors M1, M2 and two NMOS transistors M3, M4. During Phase one, transistors M1, M4 work in saturation region and M2, M3 in cut off region. Current would flow from V+ terminal through M1, C_{store} and M4 to V- terminal. In Phase two, current would flow from V+ terminal through M2, C_{store} and M3 to V- terminal. The output voltage V_{out} on C_{store} would be DC. The conduction power loss of MOSFET rectifier occurs due to the voltage difference between source and drain of transistors during conduction phase. In order to reduce conduction power loss, the amplitude of $V_{in[AC]}$ signal can be large enough to enable M1, M4 or M1, M2 to work in saturation region. The other way is by reducing or named 'Cancelling' the threshold voltage V_{th} of transistors.

1-2-3 Matching network between Antenna and Rectifier

For varying input power (Varying Frequency Electrical Magnetic Wave), impedance of the receiving antenna is also varying. A matching network is implemented to match the equivalent input impedance of the antenna with the equivalent load impedance from the rectifier connected to it and maximum power can be transferred from antenna to rectifier. In addition, matching network can simultaneously boost input voltage of rectifier which can enable high Power Conversion Efficiency of rectifier.

1-2-4 Power Management Block

Power Management Block IC in RF harvester system can perform DC/DC conversion, voltage scaling and battery charging. There are four kinds of power conversion methods for Power management block:1. Inductive power conversion method which energy is stored inductor in magneto static field such as inductive DC/DC boost or buck converter. 2. Resistive power conversion method for example, the resistive divider or low dropout voltage regulator[LDO] by converting high voltage to low voltage. 3. Capacitive power conversion method such as charge pump DC/DC boost or buck converter. 4. Transformative power conversion method.

Inductive DC/DC converter topology is widely used in circuit design for its simple design structure. Inductive DC/DC converter has a voltage source, one inductor, two controllable switches and a load. The basic principle of this structure is to extract energy from voltage source and store in inductor during phase one and in phase two, energy would then be transferred from inductor to the load. In the circuit design, capacitors 'C_{in}' and 'C_{out}' are added to replace the voltage source and the load. For the required rated output voltage and input voltage, Cin and Cout is normally designed around tens of nF to few uF and inductor is around tens nH to few uH for maximum current limit consideration. In IC design prospective, both inductor and capacitors should be placed out of chip which is the disadvantage.

LDO voltage regulator also widely applied for its full chip integration characteristic without using external inductors and capacitors, small device size and the absence of switching noise. In Figure 1-5, LDO is normally combined of an amplifier A1, reference voltage Vref and a pass transistor M1. The output of amplifier is connected to pass transistor M1 with R1 and R2 forming a resistive voltage divider negative feedback. Therefore, by controlling the value of resistors R1 and R2, Vout can be generated which is equal to $V_{ref}(\frac{R_2}{R_1})$. The disadvantage is the power dissipation due to the voltage drop on the MOSFET M1 and can only make a lower output voltage.

Charge pump DC/DC converter also named Switched capacitor DC/DC converter utilize the switches and capacitors to generate a input voltage divider or input voltage multiples. The working principle of charge pump DC/DC converter can be divided into two working phases. Phase one is to charge its 'capacitor bank' by Vin. Phase two would then stack capacitors in series or parallel to boost or buck Vin to the load. These capacitors can be integrated on chip and also depend on applications but complex control of switches to capacitors is required.

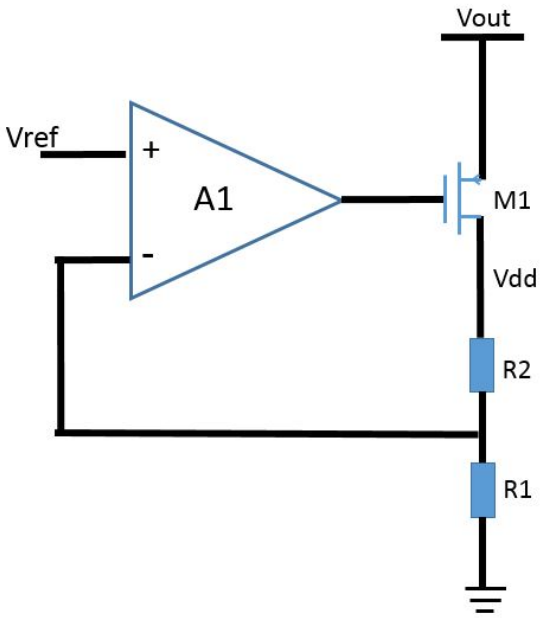

Figure 1-5: LDO block diagram

1-3 Research Objectives and Target Application

The objective of this project is to design High Efficiency Power Management Block IC for front-end 900MHz MOS rectifier in RF energy harvester system. Table 1-1, list the specifications and requirements of Power management IC Block. Table 1-2 displays an example of low power target application which is medical implantable transceiver[Specs provided by Prof Guido Dolmans]. This application only works 2ms in 7s period with 1.1volt supply voltage, 10mA maximum supply current and 250nA leakage current.

Table 1-1: Research Objectives

Specifications	Values
Power Throughput (P_{in})	[8uW, 1mW]
Input Voltage (V_{in})	[400mV, 1V]
Peak PCE	85 %
Min Control Power Loss	3.0uW
Chip Area (A)	500um×500um

Table 1-2: Target Application-Ultra Low Power Implantable Transceiver

Specifications	Values
Working time $t_{working}$	2ms
Working current I_L	[1mA, 10mA]
Period T_{period}	7s
Supply Voltage V_S	1.1V
Max Sleep current I_{sleep}	250nA

1-4 Thesis Outline

In Chapter two, this thesis would determine the basic power management block functionality at the beginning based on working duty cycle and average power consumption of this transceiver application which is in Chapter 2-1. The functionality includes energy storage, input power Detection and DC to DC Conversion control. Then, in order to realize energy storage functionality, storage elements size and type are analysed and determined after considering its DC power loss, AC power loss and capacitor temperature and voltage dependence. The general power management block structure is chosen to be DC/DC boost converter after estimating power dissipation of other structure topologies. Next, the DC/DC boost converter switches control principle, input power tracking and detection principle are verified and determined by applying data analysis from rectifier output. Finally, Switch control and Power Detection principles are implemented with both analog and digital circuit blocks including ADC, DAC, Voltage Comparator, Voltage Level Shifter, Voltage Reference Generator (VRG) and Low Dropout Voltage regulator (LDO).

Chapter three introduces the schematic level design principle of analog circuit blocks. Considering the mismatch issue to comparator, the Monte Carlo simulations were implemented for Voltage comparators. Process, Voltage and Temperature (PVT) simulations were done for VRG and LDO blocks to check the performance. In Chapter four, the simulation would focus on analog Circuit system built and also analog with digital system combined. These simulation would cover the system input, output voltage, inductor current and power dissipation contribution simulations both in schematic level and layout level. Meanwhile, chip layout would also be displayed in Chapter four. Finally, the simulation results would be utilized to do the state of art comparison. Chapter five would give the thesis conclusion, the work contribution and future work for further research.

Chapter 2

Power Management System Level Analysis and Design

2-1 Power Management Block Architecture

The content outline of Chapter two is shown in Figure 2-1. The System analysis would start at the Interface analysis between rectifier and Harvest Interface in section 2-2. In section 2-2, input voltage and current would be analysed. Then, turn to the analysis of Storage Element which is in section 2-3 to determine the element type, size and rated voltage. Next, based on section 2-2 and 2-3, Harvest Interface system structure is proposed to be an inductive DC/DC boost converter as shown in Figure 2-1. Finally, in section 2-5, DC/DC Converter Switches Logic Control topology and Maximum Power Point Tracking topology are determined.

The target application of this project is a wireless transceiver. As shown in Table 1-2, the transceiver only needs to be powered during working period which is 2ms in total period of 7s and maximum load current is equal to 10mA. According to the target application, this power management block should have a function "Energy Storage" which means power management block can charge a storage element during the transceiver sleep period 6.998s and then, storage element can be used to charge transceiver during its working period 2ms.

In addition, from table 1-2, the transceiver average power consumption can be computed as $P_{ave} = \frac{I_L \times V_S \times t_{working}}{T_{period}} + V_S \times I_{sleep}$ =3.42uW. The lowest power value input for the Power management block is equal to 8uW. The power loss between the input and the output terminals of power management block should be less than 4.58uW which is the most critical part in this project. Therefore, this project would focus on the extreme low power consumption of power management block design.

In this case, the design of power management system can be subdivided into two parts as shown in Figure 2-1. The first part is used to do impedance matching between rectifier and power management block and achieve maximum PCE to efficiently charge the 'Storage Capacitor'. The second part have functionality to perform DC to DC conversion from "Storage capacitor" and output voltage regulation for target application.

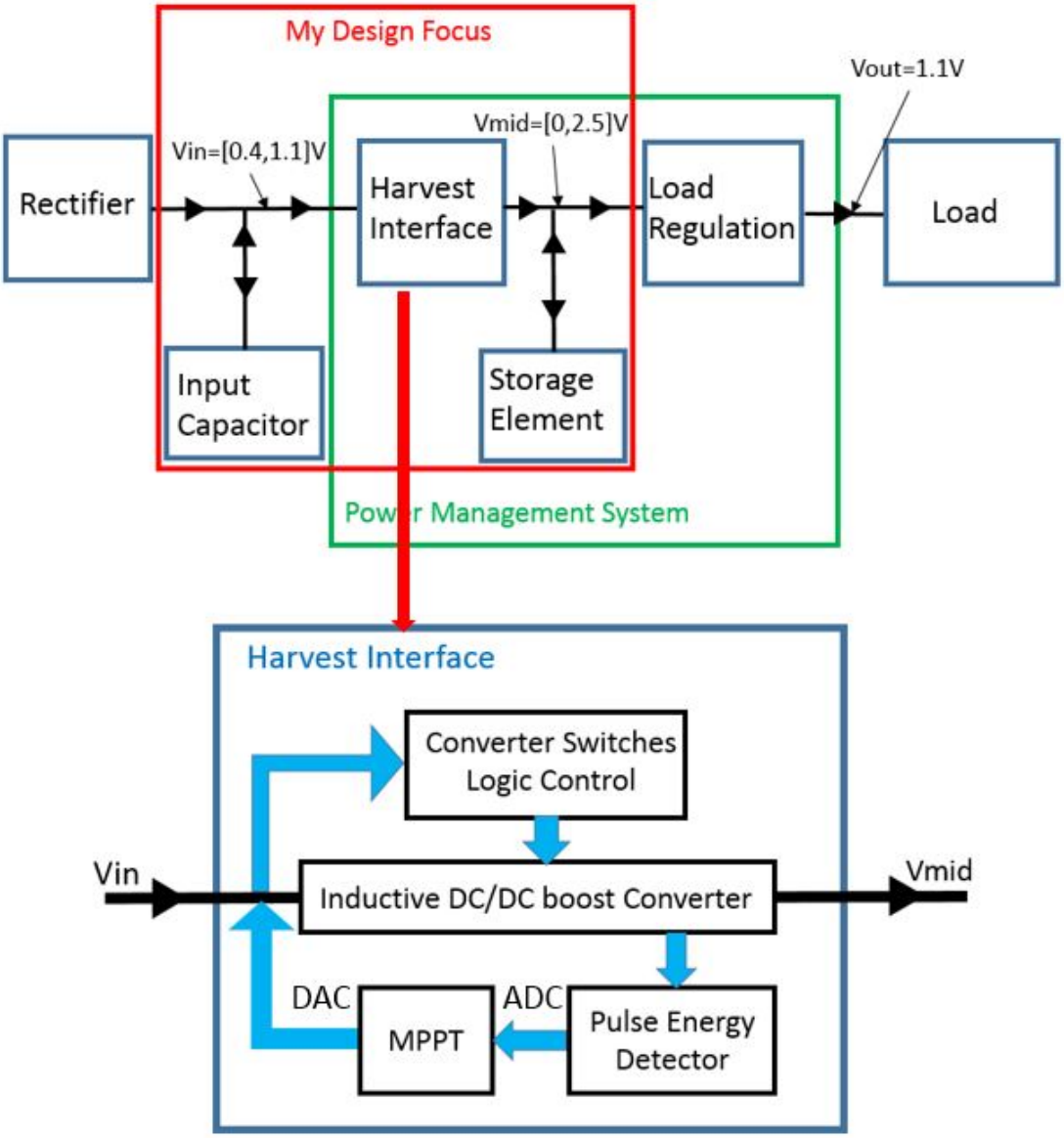

Figure 2-1: Power Management System

In Figure 2-1, the value of the amount of energy stored is determined by the voltage level on storage element and size of storage element. The voltage on Storage Element can be in the range of [0, 3.3]volt because of transistor 40nm TSMC technology. In order to store enough energy, 3.3 volt is chosen to be the maximum voltage for on Storage Element. Then, the structure of Harvest Interface can be a DC/DC boost converter or a DC/DC buck-boost converter or a charge pump boost converter. For Load Regulation part, structure can be DC/DC buck-boost converter or DC/DC buck converter or Charge pump buck converter or a LDO.

Based on 1.1 volt wireless transceiver load condition, considering small power efficiency, the LDO is not suitable in the design due to large voltage difference between input and output terminals in Harvest Interface part or in load regulation part. For the all voltage variation from 0 to 3.3 volt on Storage Element, then, charge pump DC to DC converter are also not suitable for both Harvest Interface and Load Regulation two parts to achieve high PCE. Therefore, a DC/DC buck-boost converter or a DC/DC boost converter structure can be chosen for Harvest Interface Part, a DC/DC buck-boost converter or a DC/DC buck converter structure can be the choice of Load Regulation part.

In section 2-3, Storage Element would be analysed on the voltage level, size and Element type. Section 2-4 would further discuss Harvest Interface Structure and finally determine to be DC/DC boost converter structure comparing to DC/DC buck-boost converter after considering small power dissipation.

2-2 Interface between Rectifier and Power Management Block Analysis

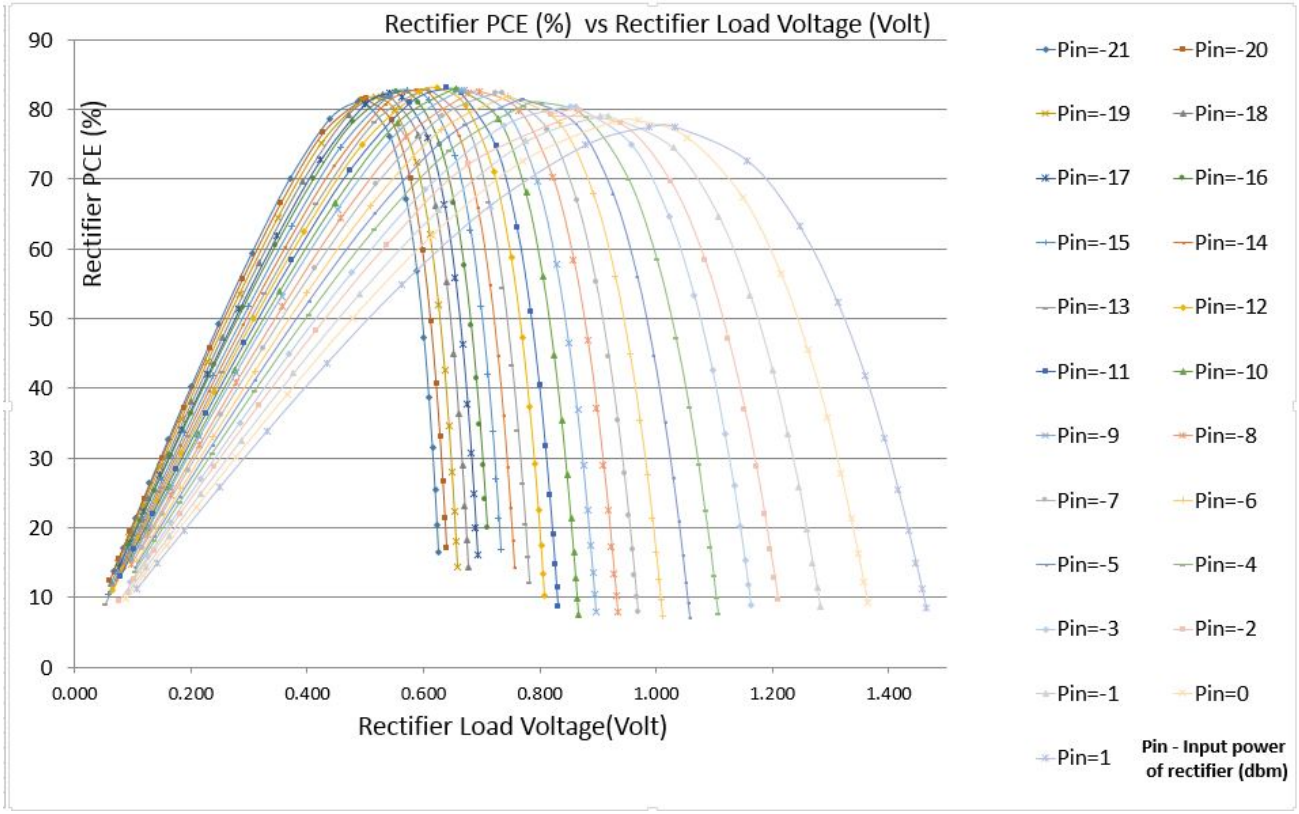

Figure 2-2: Rectifier PCE versus Rectifier Load voltage with Pin=[-21dbm, 1dbm]

Figure 2-2 displays the Power Conversion Efficiency (PCE) of Rectifier versus Rectifier Output Voltage with rectifier input power vary from -21dbm to 1dbm. For the increasing input power of rectifier, the maximum PCE occurs on certain optimum rectifier load voltage. Therefore, the Interface between rectifier and power management block can be explained as dynamically adjusting power management block to achieve varying optimum rectifier load voltage for varying input power into the rectifier.

The right most curve represents Pin = 1dbm. Rectifier PCE increases to 78 % when load voltage increases to 1.04 volt and PCE decreases when voltage increases to 1.40 volt. Comparing to Pin=1dbm, when Pin=-21dbm, PCE curve increases faster and also decreases faster which means that optimum PCE point at low input power condition is more sensitive to rectifier load voltage than PCE point at high input power condition. Therefore, for a good PCE at low input power condition, the variation of rectifier load voltage relative to the optimum load voltage should be smaller than other input power conditions.

As shown in Figure 2-3, in order to achieve 78% PCE of rectifier, rectifier load voltage variation should not exceed ± 40 mv relative to optimum load voltage. In this case, load voltage variation less than ± 40 mv can also enable good PCE in other input power conditions.

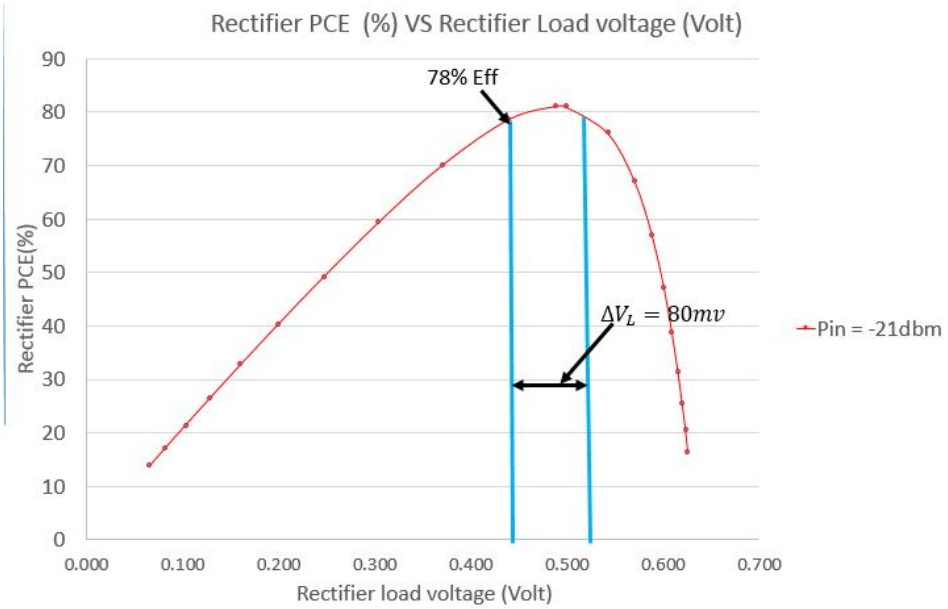

Figure 2-3: Rectifier PCE versus Rectifier Load voltage with Pin=-21dbm

2-3 Storage Element Analysis

Referring to table 1-2, the maximum energy needed to be transferred to transceiver during one period is equal to $E_{single} = V_S \times I_{L-max} \times t_{working} = 26.7$uJ with 2.5 volt maximum voltage level. In this case, at least 14uF size Storage Element capacitor is needed to discharge from 2.5 volt to 1.5 volt to supply 26.7uJ energy to transceiver. 14uF capacitor can hardly be integrated on chip. In this case, Storage Element should be out of chip.

Discrete capacitors are commonly used for low power application. Storage Element as the consideration of size, cost and performance. Discrete Capacitors in the market includes ceramic cap, film cap, Metalized cap, Al electrolytic cap, Tantalum electrolytic cap and double layer super-cap. Figure 2-4 gives a voltage to capacitance reference for six types of capacitors according to their electrical characteristics, performance and cost. Considering 14uF and 1.5 to 2.5 volt rated voltage, only three types of capacitors would be suitable in this application which are ceramic capacitor, tantalum capacitor and Aluminum capacitor. Sections below would compare electrical characteristics among three categories capacitors containing DC power loss, AC power loss, capacitance voltage dependence and capacitance temperature dependence. In last subsection 2-3-4, trade off between capacitance and maximum capacitor voltage would be discussed based on DC power loss.

Figure 2-5 displays the equivalent capacitor model and Figure 2-6 shows corresponding DC and AC power losses. For the same capacitance value, the capacitance losses can be characterized into DC loss which depends on insulation resistance R_{insul} and equivalent series resistance (ESR) of dielectric and AC loss not only depends on ESR but also frequency dependent RMS current flow through. High frequency result in low quality factor, high RMS current and high power loss.

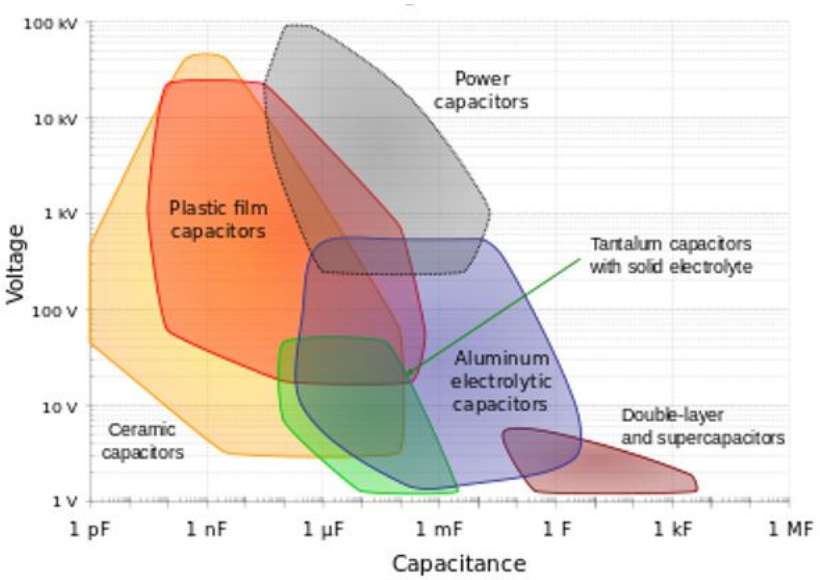

Figure 2-4: Voltage to Capacitance mapping for six categories capacitors [3]

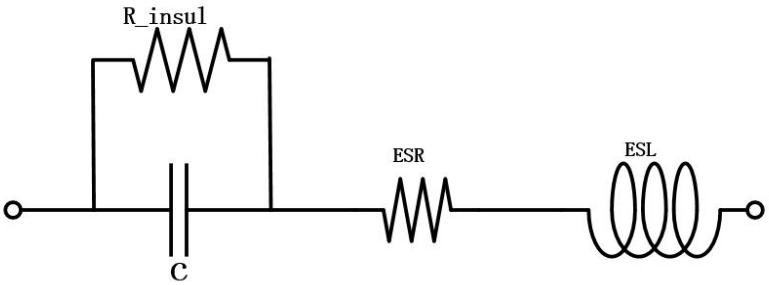

Figure 2-5: Equivalent Circuit Model of real Capacitors

Capacitor Power Loss distribution

AC power loss: $P_{ACloss}=(I_{rms})^2\times ESR$

AC power stored: $P_{ACstored}=(I_{rms})^2\times\sqrt{(X_C)^2+(X_L)^2}$

DC power loss: $P_{DCloss}=(\frac{V_{out}}{R_{insul}+ESR})^2[V_{out}\leq V_{rated}]$

Figure 2-6: Capacitor AC and DC Power Loss

2-3-1 Capacitor DC Power Loss

The DC power loss of the Tantalum or Aluminum capacitors equation is $P_{dc-loss[Ta-Al]} = V_{out} \times DCL = V_{out} \times A \times C \times V_{out}$. DCL stands for capacitor DC leakage current which is equal to factor A times capacitance and voltage value. Factor A value differs from capacitor types and dielectric materials.

In this application, maximum voltage on the storage capacitor is 2.5 volt and capacitance is 14uF. Therefore, maximum DC loss calculated is equal to 875nW and factor A is choosing to be 0.01 for DC loss computation. Maximum 11 % power would be lost due to DCL of Tantalum and Aluminum capacitors for 8uW input power of power management block. For ceramic capacitor, DCL is equal to $DCL = \frac{V_{out}}{R_{insul}}$ and $R_{insul} = \frac{100}{C}$. Maximum DC power loss of ceramic capacitor can be calculated as $P_{dc-loss} = V_{out} \times DCL$=875nW which is equal to power loss of Mno2-Tantalum capacitor and "Wet" aluminum capacitors.

2-3-2 Capacitor AC Power Loss

AC loss of capacitor is composed of losses due to ESR with working frequency range:[3kHz, 100kHz]. Shown in Figure 2-7, for 10uF capacitance, Ceramic capacitor has lowest ESR comparing to other two capacitors. From Figure 2-7, ESR of aluminum cap is around 2ohm, tantalum cap is 0.5ohm and Ceramic cap is 0.015ohm. Total AC power loss for aluminum capacitor is computed in the range of [10nw, 17uW], tantalum capacitor [9nw,15uw] and ceramic capacitor in the range [9.5nw, 15.2uw] corresponding to working frequency [3kHz, 100kHz] referring to Figure 2-6. 9.5nw AC power loss is much smaller than 8uw input power at 3kHz and the same as 15.2uw loss for 1mw input power at 100kHz working frequency.

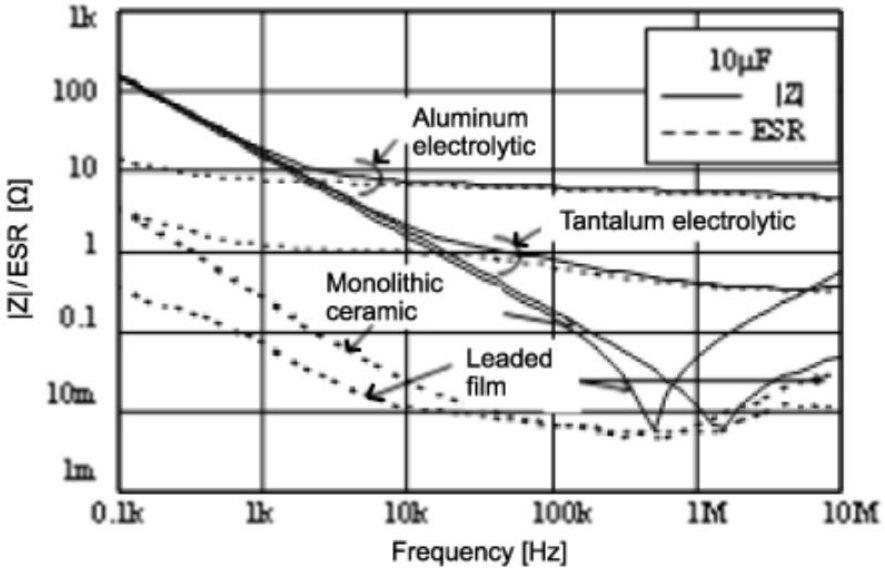

Figure 2-7: ESR frequency characteristics of different types of capacitors [4]

2-3-3 Capacitor Temperature and Voltage Dependence

Capacitor temperature dependence is a factor which give a reference of capacitance variation according to temperature variation. In Figure 2-8, both Aluminum and tantalum capacitors have ±20% temperature coefficient over temperature range -40 to 125 degree. For Multi-Layer Ceramic Capacitor (MLCC), MLCC(C0G) has lowest temperature coefficient than other two classes which are MLCC(X5R) and MLCC(Y5V) dielectric ceramic capacitors. However, MLCC(C0G) is normally in pF level which limits its application area and except for this, MLCC(Y5V) capacitance has strong temperature dependence. Both two types are not suitable in this project.

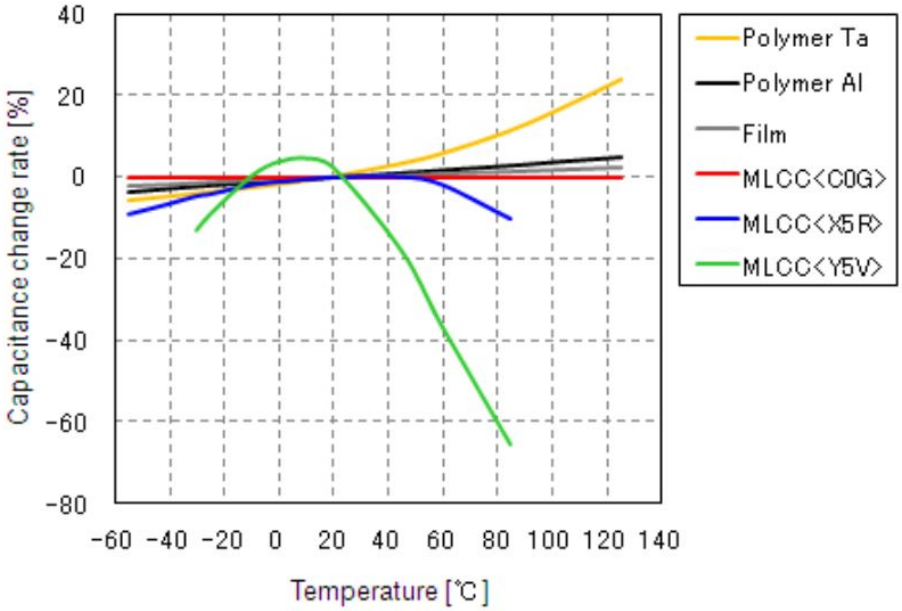

Figure 2-8: Capacitance changing rate versus temperature characteristic [5]

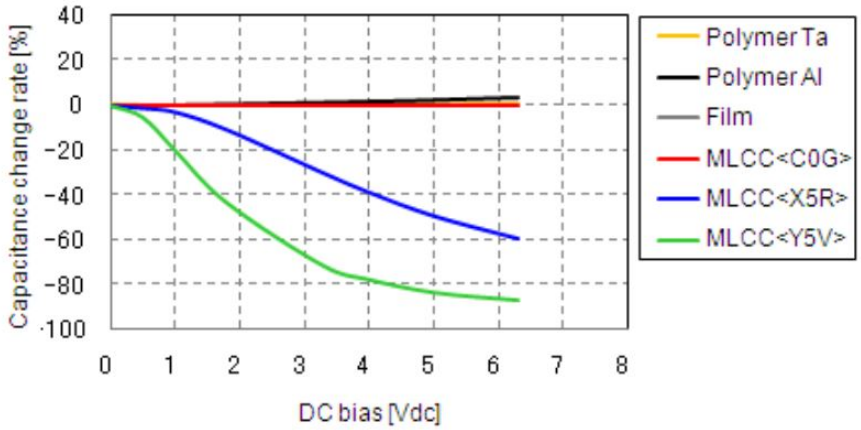

Figure 2-9: Capacitance changing rate versus DC bias voltage in 6.3V rated voltage [6]

Figure 2-9 compares voltage dependence of four types of capacitors. Polymer Titanium,

Aluminium, film capacitors and MLCC(C0G) have small voltage dependence of capacitance. In addition, MLCC(Y5V) has worse bias voltage dependence coefficient than MLCC(X5R) and MLCC(Y5V) is not suitable for this application.

2-3-4 Trade off between capacitance value and maximum capacitor voltage

The maximum capacitor power loss is because of DC power loss. High capacitor voltage and low insulation resistance of capacitor [big capacitance] would cause a big DC power loss. Referring to DC power loss ceramic capacitor equation, $P_{dc-loss} = V_{out} \times DCL = \frac{(V_{out})^2 \times C}{100}$, the value of V_{out} and Capacitance would directly influence DC power loss. Therefore, following subsection would analyze the trade off between capacitor voltage and capacitance.

For a constant energy stored in capacitor, increasing capacitor voltage and decreasing capacitance can result in different power loss values. The optimum capacitance with corresponding capacitor voltage should be found for minimum power loss. In Figure 2-10 left, E_{store} in the equation represents the energy stored in capacitor C with 1.5V minimum DC level. Substitute C into DC power loss equation and get DC power loss equation only depends on capacitor voltage. The graph with DC Power loss versus Capacitor Voltage was plotted in Figure 2-10 right. We can get lower DC power loss with higher capacitor voltage. However, storage capacitor voltage could not be higher than 3.3V in this design. This is because 3.3V is the highest voltage for thick oxide MOSFET transistor in TSMC 40nm and in this design, 3.3V thick oxide transistors are avoided to be used due to the disadvantage of large area and high power losses. In order to minimize DC power loss, 2.5V is chosen to be maximum capacitor voltage instead of 3.3V and 14uF storage capacitor computed from left side equation. Only 180mW extra DCL power comparing to 3.3V capacitor voltage.

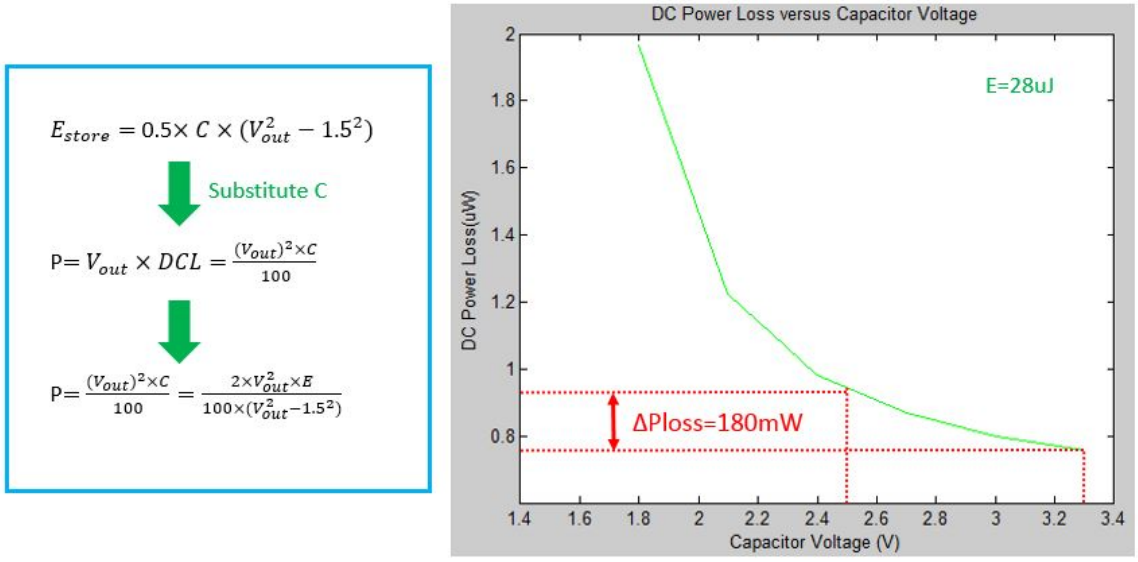

Figure 2-10: DC power loss versus Capacitor voltage for constant E_{store}=28uJ

2-3-5 Conclusion

To conclude, polymer Titanium, polymer aluminium capacitor and MLCC(X5R) are suitable in this design project. However, considering mass production, cost, size and integration specs. 14uF MLCC(X5R/X7R) is chosen to be used in this application after comparing DC, AC loss, temperature and bias voltage dependence. AC power loss can be neglected comparing to DC power loss which will take up 11 % power loss for 8uw input power. Maximum voltage on capacitor is equal to 2.5 volt after considering trade off between capacitor voltage and capacitance for constant 28uJ energy stored in capacitor based on reducing capacitor DC power loss.

2-4 Harvest Interface System Structure Analysis

Referring to Figure 2-1, the Harvest Interface can be inductive buck-boost converter or boost converter in continuous conduction mode(CCM) or discontinuous conduction mode(DCM). In terms of continuous conduction mode, it is not suitable in this design which requires less than 3uW total Harvest Interface power loss. The reasons are :1. Large Varying V_{in} and V_{out} result in high inductor RMS current and lead to large conduction loss occur in both two power switches and inductor parasitic resistance. 2: By increasing frequency to reduce inductor RMS current, high frequency would lead to high power switching loss. 3: By increasing inductance to reduce inductor RMS current, increasing parasitic resistance of inductor would cause extra power conduction loss. 4: Loop stability need to be analysed and circuit implementation increase system complexity. However, DCM DC/DC converter has feasibility by controlling working frequency without loop stability issue and instead of using big inductor to reduce RMS current. In this case, DCM DC/DC converter is applied in this design. Following section 2-4-1 and 2-4-2 would compare performance of DC/DC boost converter with DC/DC buck-boost converter in power dissipation.

2-4-1 Choice 1: DC/DC Boost Converter Structure

Inductive discrete continuous mode (DCM) DC to DC boost converter is shown in Figure 2-11. The working principle of inductive DC to DC converter can be divided into three working phase modes which are "Charge inductor mode", "Inductor discharge mode" and "Sleep mode".

Figure 2-12 displays "Charge Inductor" Mode. Power source is connected to C_{in} and continuously charge C_{in}. By closing NMOS switch and open PMOS switch, the energy is transferred from C_in to inductor L1. There is a significant voltage drop on Vin and current I_L flow through the inductor is increasing to I_{peak} upon opening NMOS switch during ton. The I_{peak} current equation can be written by estimating voltage difference between inductor.

$$I_{peak} = \frac{t_{on} \times V_{in}}{L} \tag{2-1}$$

"Inductor Discharge" Mode is after "Charging Inductor" Mode by opening NMOS switch and closing PMOS switch as shown in Figure 2-13. The energy stored in inductor L1 and Cin are discharged through PMOS switch into storage capacitor Cout and power source is still

continuously charging capacitor Cin. Therefore, current in inductor L1 decreases suddenly into zero during toff upon PMOS switch is opened and voltage in storage capacitor Cout is suddenly increased. Then, inductor current equation can also be derived as:

$$I_{peak} = \frac{t_{off} \times (V_{out} - V_{in})}{L} \tag{2-2}$$

During sleep mode, NMOS and PMOS switches are both opened and inductor is not working. Power source is continuously charging Cin during tdead.

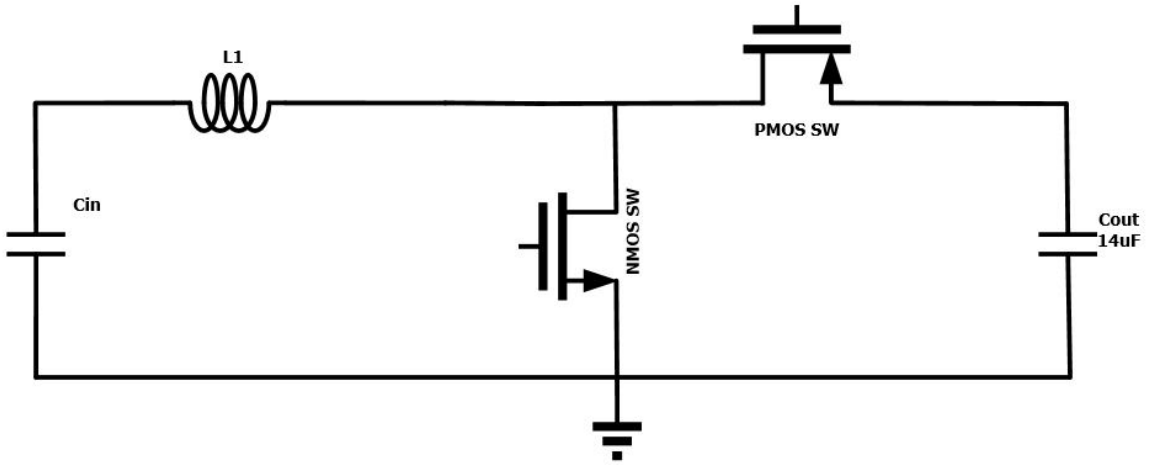

Figure 2-11: DC to DC boost converter ideal model

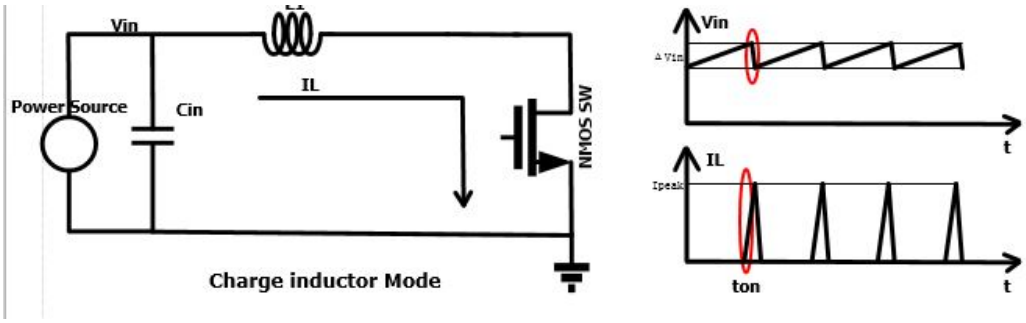

Figure 2-12: Charge Inductor Mode

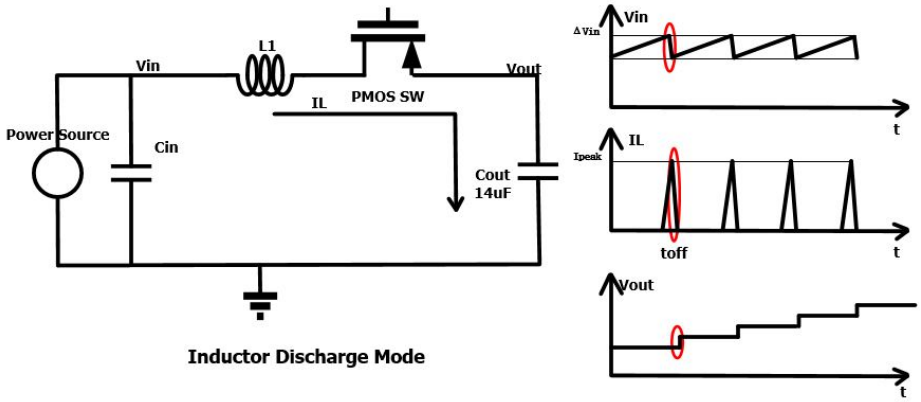

Figure 2-13: Inductor Discharge Mode

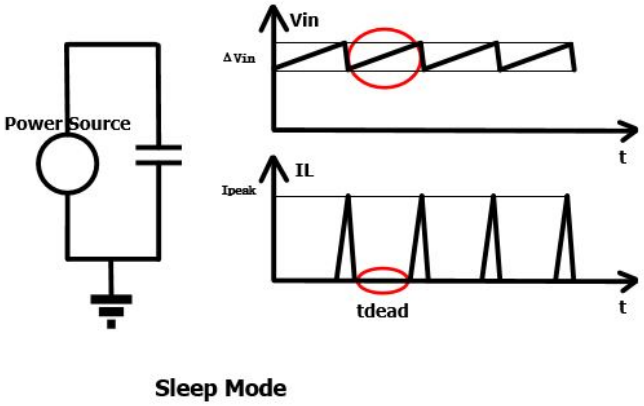

Figure 2-14: Sleep Mode

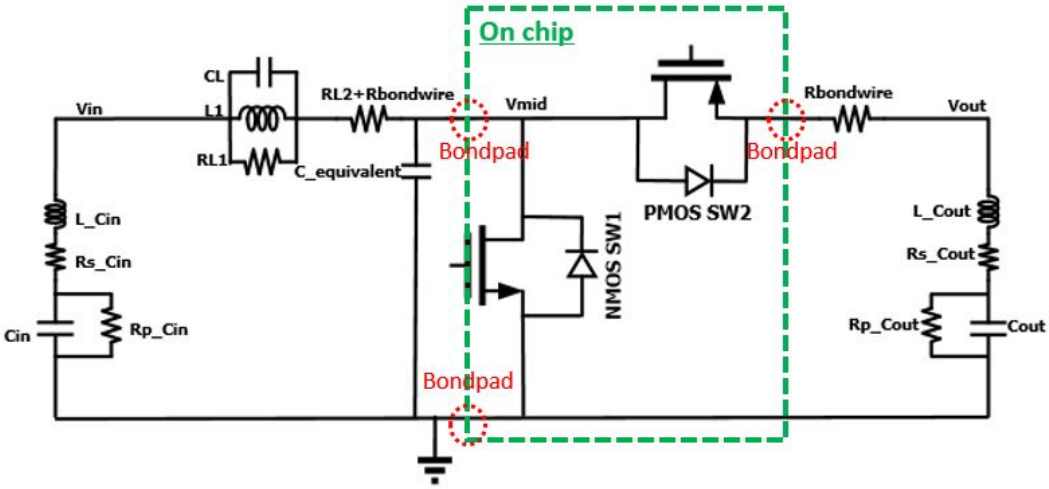

Figure 2-15: DC to DC boost converter non-ideal model

The power loss for the general DC to DC converter would come from input capacitor DC power loss, inductor parasitic resistance loss, inductor parasitic capacitor driving loss, NMOS switching loss & conduction loss, PMOS switching loss & conduction loss, bond wire parasitic resistance & parasitic capacitor loss and storage capacitor DC power loss.

PMOS switching and conduction power loss happens during "Inductor Discharging" Mode during toff period and NMOS switching and conduction loss in "Charge Inductor" Mode during ton period. Inductor parasitic capacitor driving loss, resistance loss and bind wire parasitic capacitor & resistance loss happens during both "Inductor Discharging" Mode and "Charge Inductor" Mode [ton+toff]. Except for these, Cin and Cout DC power loss occurs continuously in whole period [ton+toff+tdead].

In order to figure out power losses distribution in boost converter system, the size of two switches PMOS and NMOS, value of inductor L1, size of Cin would be designed. In this case, DC to DC converter power loss model is built based on equations below:

$$P_{Losstotal} = P_{NMOS} + P_{PMOS} + P_{Inductor} + P_{Bondwire} + P_{Cin} + P_{Cout} \tag{2-3}$$

$$P_{NMOS} = C_{NMOS} \times (V_{Drive})^2 + (\frac{t_{on} I_{peak}}{2 \times T})^2 \times R_{NMOS} \tag{2-4}$$

$$P_{PMOS} = C_{PMOS} \times (V_{Drive})^2 + (\frac{t_{off} I_{peak}}{2 \times T})^2 \times R_{PMOS} \tag{2-5}$$

$$P_{Cin} = V_{in} \times DCL = \frac{(V_{in})^2 \times C_{in}}{100} \tag{2-6}$$

$$P_{Cout} = V_{out} \times DCL = \frac{(V_{out})^2 \times C_{out}}{100} \tag{2-7}$$

$$P_{L1} = C_{Lpara} \times (V_{out})^2 + (\frac{(t_{on} + t_{off}) I_{peak}}{2 \times T})^2 \times R_{L1para} \tag{2-8}$$

$$P_{Bondwire} = C_{Bpara} \times (V_{out})^2 + (\frac{(t_{on} + t_{off}) I_{peak}}{2 \times T})^2 \times R_{Bpara} \tag{2-9}$$

In Equation (2-4) and (2-5), C_{NMOS} or C_{PMOS} and R_{NMOS} or R_{PMOS} depend on 40nm TSMC technology and size of PMOS and NMOS (Width and Length). Both NMOS and PMOS switches are working at linear region. By simplifying Equation (10), conduction resistance of NMOS and PMOS switches can be computed shown in Equation (2-11).

$$I_D = \mu C_{ox} (\frac{W}{L}) \times \{(V_{GS} - V_{th}) V_{DS} - \frac{(V_{DS})^2}{2}\} \tag{2-10}$$

$$R_{NMOS} = \frac{1}{k_n \times \frac{W_{NMOS}}{L_{NMOS}}} \tag{2-11}$$

$$R_{PMOS} = \frac{1}{k_p \times \frac{W_{PMOS}}{L_{PMOS}}} \tag{2-12}$$

$$C_{NMOS} = C_{oxn}(W_{NMOS} \times L_{NMOS}) \tag{2-13}$$

$$C_{PMOS} = C_{oxp}(W_{PMOS} \times L_{PMOS}) \tag{2-14}$$

k_p and k_n in 40nm TSMC and V_{GS}=2.5volt are computed to be the values of $8.1\times(10)^{-5}$ and $2.5\times(10)^{-4}$ correspondingly. In Equation (2-13) and (2-14), NMOS and PMOS switches driving equivalent capacitance values are also related to the size of switches. C_{oxn} and C_{oxp} are capacitance per unit area and in 40nm TSMC, both two parameter are equal to around $5.5\ \times(10)^{-3}$. Equations (2-1) to (2-14) are formulated in Matlab code for the purpose of determining the values of parameters including Cin, L1, ton, toff, tdead, Width and length of NMOS & PMOS switches which contribute minimum power loss.

In order to minimize the power loss, the most significant loss contributors should be reduced first. By applying Matlab Power loss equation model, trade off is found between conduction loss and driving loss for Bondwire, NMOS & PMOS switches and Inductor. NMOS and PMOS switches are optimized at the first place by decreasing I_{peak} [due to $(I_{peak})^2$] which is more effective according to Equation (2-4) and (2-5). Then, choose suitable inductor and optimize the size of NMOS and PMOS switches to balance power loss between switch resistance and capacitance. Minimum Cin is determined by interface between rectifier and DC to DC boost converter. Finally, Cin is designed to be 400nF, L1 inductor 20uH, I_{peak}=15mA, NMOS width to length factor is equal to 3703 and PMOS width to length factor is 14800. The minimum length for 2.5 volt PMOS and NMOS power switch Mosfet is equal to 250nm. bondwire resistance is assumed to be 0.5 ohm with all equivalent capacitance including capacitance from ESD protection bond pad and body diode of SW1 and SW2 at V_{mid} equals to 4pF.

After these parameters are designed, DC/DC converter working frequency range can be determined. DC/DC converter working frequency depends on front end [DC to DC converter] matched rectifier output power or output voltage or equivalent output impedance. Rectifier output impedance can be derived by applying Equation (2-1). For input power varying from 8uW to 1mW, matched rectifier output equivalent resistance differs from 1kOhm to 31kOhm and DC to DC boost converter working frequency vary from 3kHz to 100kHz.

$$R_{Rec-output} = \frac{V_{in}}{I_{ave}} = \frac{V_{in}}{\frac{I_{peak}(t_{on}+t_{off})}{2T}} = \frac{2LT}{t_{on}(t_{on}+t_{off})} \tag{2-15}$$

In Figure 2-16, 'Rloss' represents for resistance loss or conduction loss and 'Dloss' is driving loss or switching loss. Total power loss for inductive DC to DC converter [without NMOS & PMOS switch Control Circuit]is equal to 480nW for 8uW input power [Working frequency 3kHz]. NMOS and PMOS switches losses take up 50 percent of total power loss. The other two 25 percent power loss parts are from bondwire loss and Inductor loss. Inside the bondwire loss, bondwire resistance loss is significant part of power loss. Double the bondwire length would result in double Bond resistance loss. In addition, the leakage power loss of due to

SW1 and SW2 from C_{in} and C_{out} has not been considered yet but it will finally be added into '$SW + Inductor + Bondwire$' power loss contribution by simulation as shown in Figure 4-5. To conclude, for Pin=8uW, $f_{working}$=3kHz, conduction or resistance power loss take a significant part, after balancing, the conduction power loss become slightly bigger than driving loss.

For 1mW input power condition, the total power loss is equal to 27uW. The working frequency of DC to DC boost converter is 200kHz and in this condition, driving loss would be more significant than conduction loss. Then, size of NMOS and PMOS switch transistors are re-optimized to balance switching loss with conduction loss as shown in Figure 2-17.

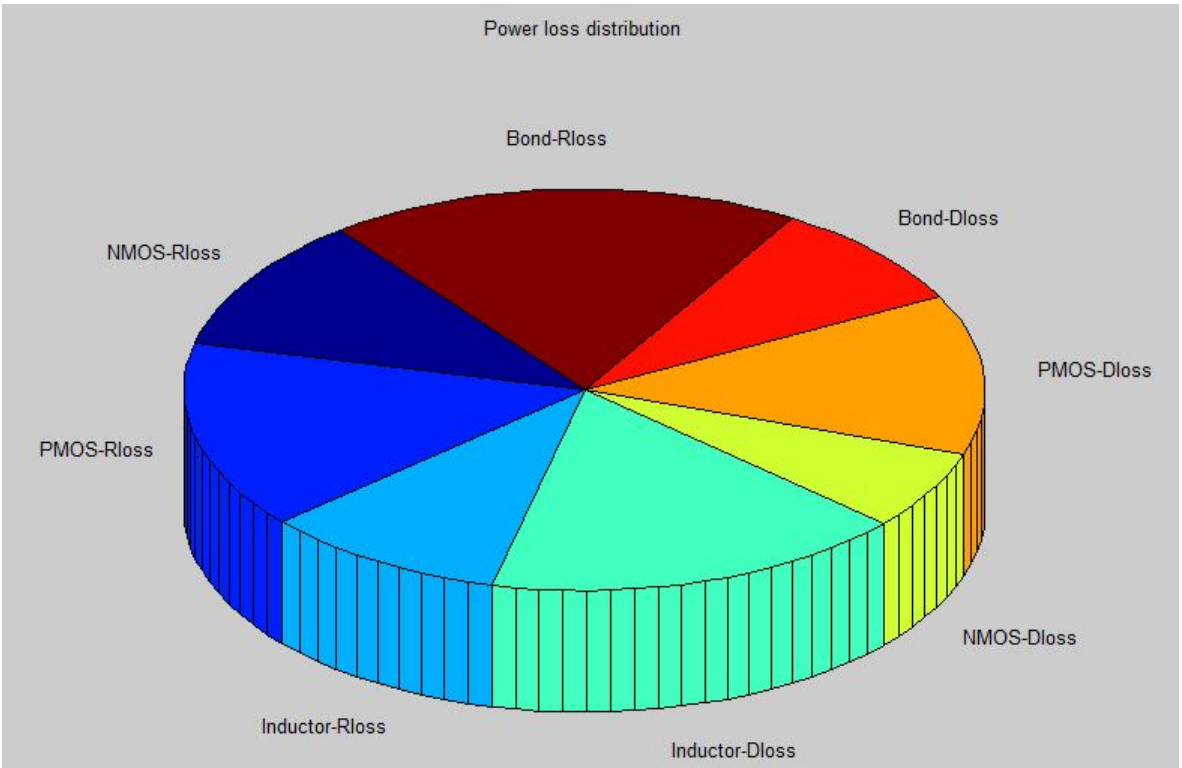

Figure 2-16: Power Loss distribution at Pin=8uW, $f_{working} = 3kHz$

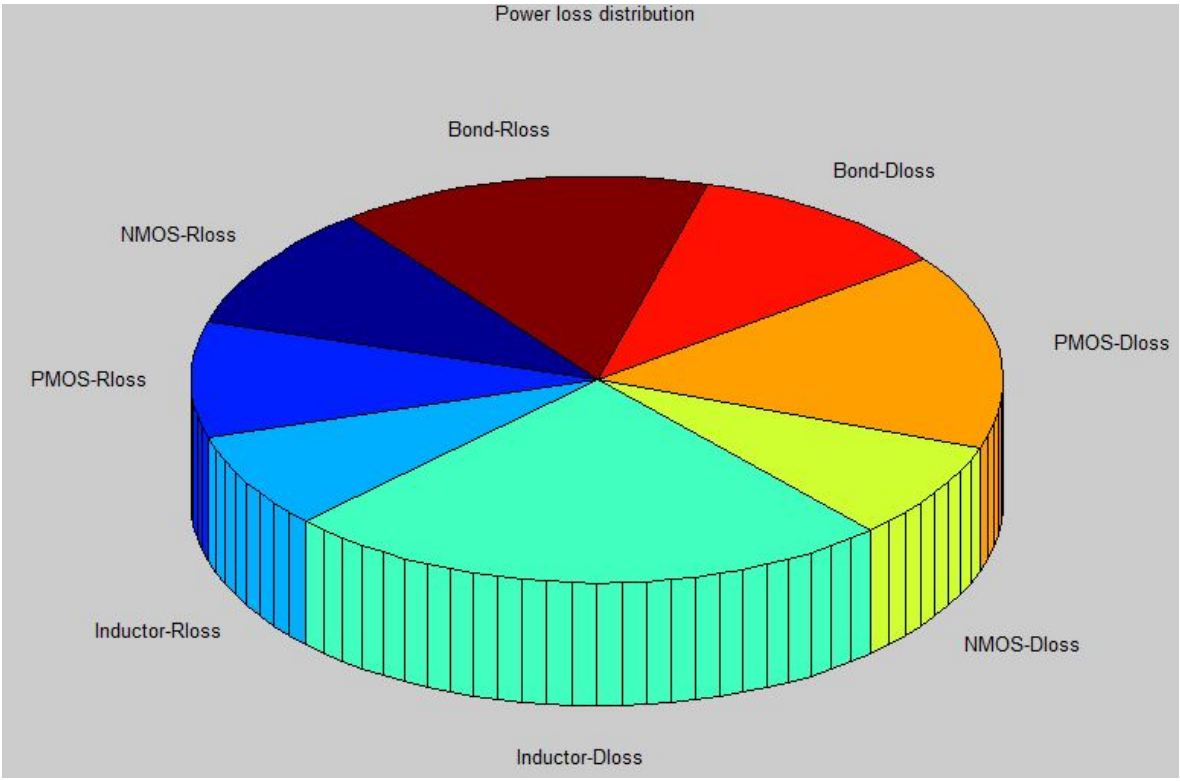

Figure 2-17: Power Loss distribution at Pin=1mW,f$_{working} = 100kHz$

2-4-2 Choice 2: DC/DC Buck-Boost Converter

DC/DC buck-boost converter topology is also a choice which can be implemented for Harvest Interface structure. Input voltage vary from 400mV to 1.1V and output voltage on storage capacitor can continuously increase or decrease freely within [0 , 2.5]V. For the same 26.7uJ energy storage, DC/DC buck-boost converter requires 9uF capacitor with 140nW DC leakage power loss. However, DC/DC boost converter has smaller output varying voltage which is [1.5, 2.5]V and requires 14uF capacitor with 560nW DC leakage power loss. Although, comparing to DC/DC boost converter topology, the DC/DC buck-boost converter topology leakage power can be reduced by 420nW. DC/DC buck-boost converter uses more than two switches than boost converter by as shown in Figure 2-18. Then the loss on switches of DC/DC buck-boost Converter would be doubled ideally including switching loss and conduction loss. In addition, extra two switches need extra control circuitry which adds the system complexity.

In addition, DC/DC buck-boost converter still has an advantage over boost converter during the DC/DC converter start up. An inductive DC/DC converter, start-up phase is needed before functioning. For DC/DC boost converter, it can start to function when voltage on input capacitor is over 0.6 volt and output voltage DC/DC is higher than input voltage. DC/DC boost converter at least needs to charge C_{in}(400nF) to 0.6V and C_{out}(14uF) to 1.1V before total system completely functioning. However, during the start up phase, the PCE of DC/DC converter is low and for 8uW DC/DC input power, during start up, only few uW power can transferred from input of DC/DC converter to slowly charge big storage capacitor C_{out}. This few uW power should be higher than the leakage power consumption of C_{out} or

DC/DC boost converter can never start up by itself.

For DC/DC buck-boost converter, start up can be quicker than DC/DC boost converter without charging C_{out} to 1.1V and directly start up at buck DC/DC mode. However, power consumption of DC/DC buck-boost converter would be higher than Boost DC/DC converter. As shown in Figure 2-18 above, there are extra two more switches comparing to boost converter. In Phase one, NMOS SW1 and SW3 would be turned on and current would flow from C_{in} through SW1, L1, SW2 to ground. During phase two, SW1 and SW3 are turned off but SW2 and SW4 are turned on. Then, current flow though SW2, inductor and SW4 to C_{out}. In this case, switch conduction loss and driving loss would be doubled. Expect for this, switches control circuit power loss would also be doubled. Meanwhile, for phase one, SW1 and SW3 should be controlled to turned on simultaneously and also the turn on for SW and SW2 just after turn off SW1 and SW3. More power would loss during the proper control of four switches. Optimum estimated power loss is around 10% including 3% for extra switches driving and switching loss and 7 % for switches control power loss. In this project, buck&boost converter would cause extra more 10 % power loss which can not be accepted for power constraint power management design.

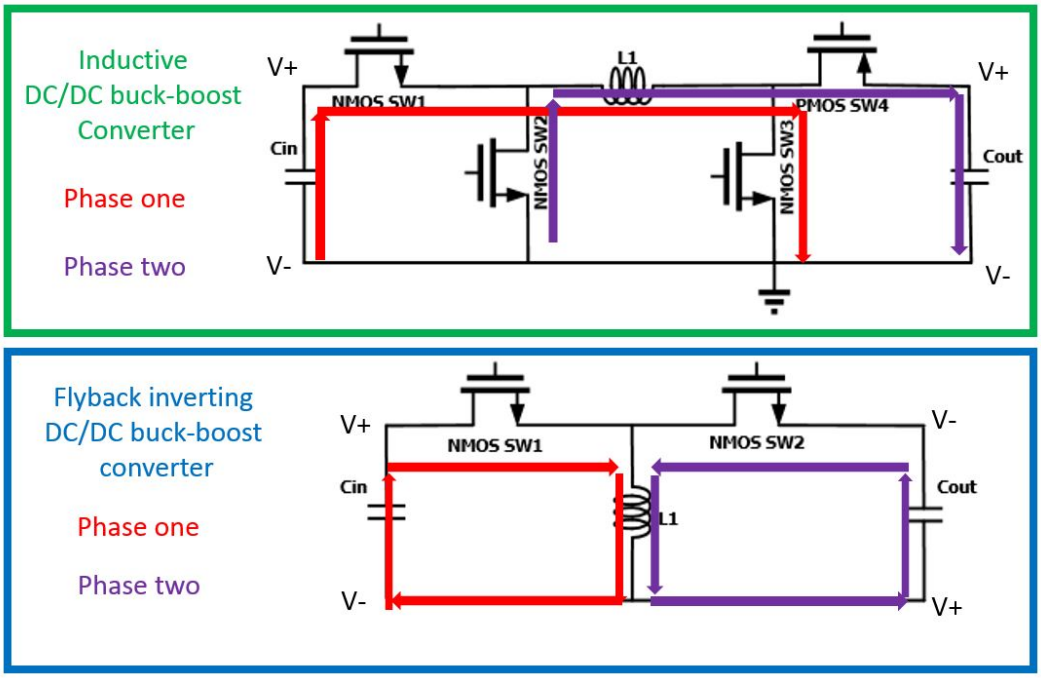

Figure 2-18: Inductive buck-boost DC/DC converter

However, There is an another topology of DC/DC buck-boost converter which utilize two power switches named 'Flyback inverting DC/DC buck-boost converter' with the topology shown in Figure 2-18 below. During phase one, SW1 is turned on and SW2 off, current would flow from C_{in} through SW1 to charge inductor L1. The voltage difference between two terminals of SW2 is equal to $V_{in} + |V_{out}|$. In phase two, after switching off SW1 and on SW2, current from inductor would continue to flow through SW2 without changing direction and immediately, the polarity if inductor L_1 changes. The voltage difference of SW1 is equal to

$2V_{in}$. In addition, output voltage is inverted compared to input voltage polarity which limits its application in this design. The negative output voltage on substrate of chip would result in latch up effect to control block and except for this, the maximum voltage difference of SW1 and SW2 for a TSMC 40nm transistor is 2.5V(V_{ds}). Therefore, the maximum voltage 2.5V should be equal to $V_{in} + |V_{out}|$ which limits the voltage variation range of V_{in} and V_{out}. To concluded, the topology is not suitable for this design.

2-4-3 Conclusion

In Figure 2-3, the topology for the Harvest Interface part is chosen to use DC/DC boost converter topology instead of boost&buck converter. The output voltage variation on storage capacitor is from 1.5 volt to 2.5 volt. Therefore, [1.5, 2.5] volt as for the Load regulation part input and 1.1 volt for the output. An inductive buck DC/DC converter topology is chosen to be applied for the Load regulation part. For Harvest Interface, the minimum power conversion efficiency[PCE] is estimated to be higher than 60 percent and for Load Regulation part, minimum PCE should be higher than 90 %. In this case, for power management block minimum input power P_{in}=8uW condition, 4.32uW power can still be sufficient to power target wireless transceiver application.

2-5 Harvest Interface System Working Principle

The purpose of first part DC/DC boost converter is to charge storage capacitor C_{out} by impedance matching with front end rectifier. For a input power into first part of power management block, there is a corresponding $V_{in(optimal)}$ at C_{in} after perfect matching. With the increasing input power of DC/DC boost converter, $V_{in(optimal)}$ increases continuously. Therefore, one purpose of DC/DC boost converter is to do input power detection and track $V_{in(optimal)}$ values for continuously varying P_{in}. The other purpose is to perform NMOS&PMOS switches control of DC/DC boost conversion for C_{in} and C_{out} in a high efficiency.

2-5-1 Power tracking Principle

Power into DC/DC boost converter can simply be expressed by equation below. The power input into DC/DC converter directly depends input voltage of DC/DC boost converter and the corresponding equivalent rectifier load impedance. Therefore, input voltage can be varied to detect power P_{in}.

$$P_{in} = \frac{(V_{in})^2}{R_{rec-load}} \tag{2-16}$$

Power tracking would be varying input voltage values of DC/DC boost converter and track the maximum power value. Figure 2-1 displays the curve relationship between rectifier load voltage and DC/DC converter input power efficiency. For Pin from -21dbm to 0dbm , the maximum power efficiency happens at rectifier load voltage varying from 0.5 volt to 1.05 volt. Figure 2-19 displays the method to track maximum PCE. For each tracking cycle, an

increment ΔVin is added to Vin to get new power value P2 and P2 is used to compare with the previous power value P1. P2 is larger than P1, Vin would be increased to get P3 and P3 is larger than P2. Vin would still be further increased by ΔVin until new power value is less than previous value. In this case, Vin would stay at V_{ref} and maximum PCE would achieve at V_{ref}. Besides, power tracking can happen from right direction to left with the order of decreasing Vin. In addition, ΔVin should be bigger enough to meet power detection limit which also depends on power detection method. However, ΔVin should not be too big which would influence detection accuracy and cause PCE drop.

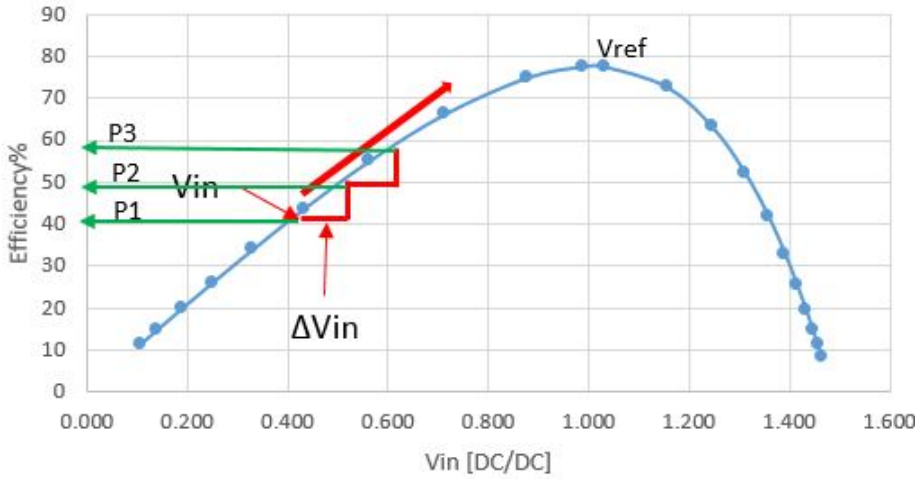

Figure 2-19: Maximum PCE tracked by varying Vin

2-5-2 Power Detection Principle

Considering Power detection, an effective and low power method would be needed. At the beginning, referring to power equations as shown (2-17). The power can be computed by applying voltage times current or energy divided by total time.

$$P = V \times I = \frac{E_{single}}{T_{period}} \tag{2-17}$$

From Figure 2-12, 2-13 and 2-14, DC/DC boost converter has three working phases. During these three phases, energy can transferred from C_{in} to inductor and finally reach C_{out}. Then, power value can be calculated from two directions which are energy coming out of C_{in} or energy received by C_{out}. Energy coming out of C_{in} is equal to total charge out of C_{in} which is equal to $\frac{I_{peak}}{2}(t_{on}+t_{off})$ times V_{in} and energy coming into C_{out} is $(\frac{I_{peak}}{2} \times t_{off})$ times V_{out}. Calculated energy can be divided by one time period to get power value. New power value calculated is compared with previous power value and sign matters which determine ΔV_{in} or -ΔV_{in} to be added to V_{in}. In this case, power value does not need to be accurately known but the sign of comparison which give much more freedom for analog circuit Power Detector design.

$$P_{in} = \frac{E_{Single}}{T_{period}} = \frac{\frac{I_{peak}}{2} \times Vin \times (t_{on}+t_{off})}{T_{period}} = \frac{\frac{I_{peak}}{2} \times V_{out} \times t_{off}}{T_{period}} \tag{2-18}$$

In Equation (2-18), $\frac{\frac{I_{peak}}{2} \times Vin \times (t_{on}+t_{off})}{T_{period}}$, by referring Equation (2-15) (2-16), inductor peak current I_{peak} is designed fixed and then, P_{in} would depend on varying V_{in} and varying $R_{Rec-output}$. Current value I_{in} which is proportional to V_{in} can be generated and integrated on a capacitor over $(t_{on} + t_{off})$ time to compute one energy pulse. In order to realize the division of T_{period}, digital design can utilize fixed long time accumulation of energy pulse E_{single} to get same power relationship and then, do the comparison.

Power Detection Principle One: Based on Equation (2-18), $\frac{\frac{I_{peak}}{2} \times V_{out} \times t_{off}}{T_{period}}$, the simplification can be applied by assuming energy pulse which is at the numerator in the equation as a constant. C_{out} is equal to 14uF which is larger than C_{in} 400nF. Comparing to voltage increasing in C_{in}, voltage increasing on C_{out} is slower. Except for this, according to Equation (2-2), toff can change slowly when I_{peak} is fixed and meanwhile, $(V_{out} - V_{in})$ changes slowly upon V_{out} being larger than V_{in}. In this condition, the energy pulse $\frac{I_{peak}}{2} \times V_{out} \times t_{off}$ can be treat as constant. Then, count numbers of energy pulses within a fixed long time and the number counted would give the information of power value. This simplification would give simple system structure for power detection as shown in Figure 2-20.

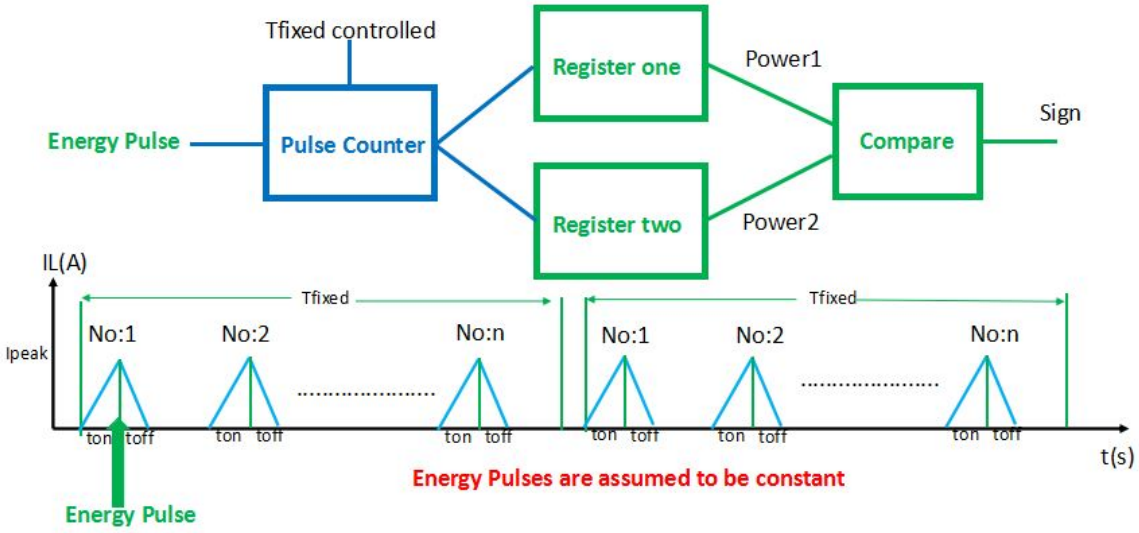

Figure 2-20: Principl One Simplification and Principle

However, this simplification would bring inaccuracy power detection and tracking due to energy pulse value difference between two T_{fixed} time. The energy pulse difference is caused by V_{out} and V_{in} variations. It is more clear to explain by equations below. The energy pulse E_{single} equation is shown in Figure (2-18). By applying Equation (2-1) and Equation (2-2) to substitute t_{on} and t_{off} in E_{single} equation, we can get a new equation shown in Equation (2-19) with energy pulse value only depending on V_{in} and V_{out}. In this Equation (2-19), inductance L is constant and inductor peak current I_{peak} is designed to be fixed. Energy pulse value is only dependent on V_{out} and V_{in}. Assign V_{out} to 1.5V and V_{in} to 1V in Equation (2-19). Based on Equation (2-19), the energy pulse error $E_{single[\%error]}$ Equation (2-20) can be derived. Matlab was used to plot energy pulse error versus variation of V_{in} and versus

variation of V_{out} separately as shown in Figure 2-21. After comparing two graphs, variation of V_{in} when V_{in} is around 1.1V significantly influences the energy pulse energy value with 16 percent of energy pulse error. However, for variation occurring at V_{out}, maximum 3.2% of error occurred on energy pulse when V_{out} equals to 1.5V. Therefore, for worse case condition, when V_{in} is 1.1V and V_{out} is 1.5V, by applying Equation (2-20), the maximum energy pulse error percentage is the sum of 16% and 3.2% which is equal to 19.2%. Therefore, energy pulse cannot be treated as a constant due to maximum 19.2 percentage of energy pulse error.

$$E_{single} = L\frac{(I_{peak})^2}{2}\frac{(V_{out})^2}{V_{in} \times (V_{out} - V_{in})} \tag{2-19}$$

$$E_{single[\%error]} = \frac{\frac{dE_{single}}{dV_{in}} \times \Delta V_{in}}{E_{single}} + \frac{\frac{dE_{single}}{dV_{out}} \times \Delta V_{out}}{E_{single}} \tag{2-20}$$

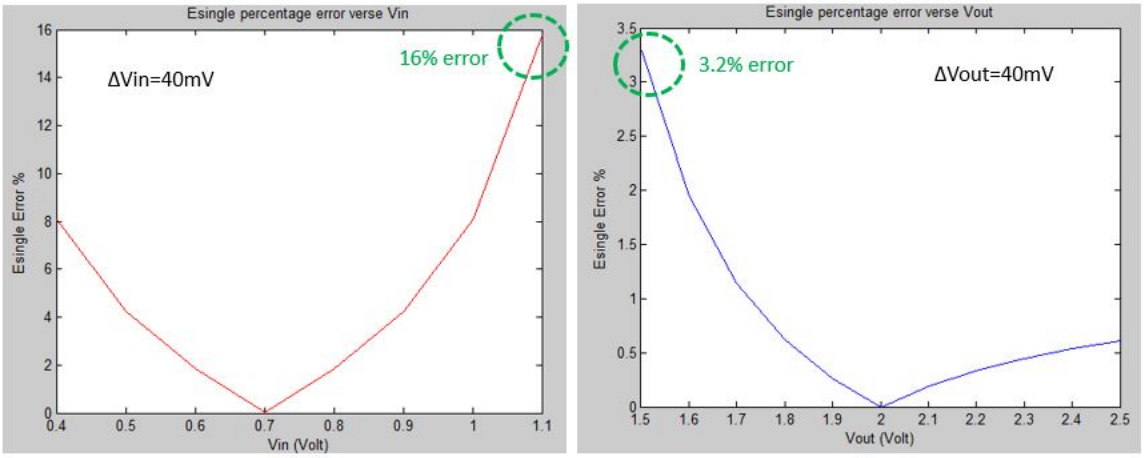

Figure 2-21: Principl One Simplification and Principle

By treating the numerator of Equation (2-18) as a constant and by varying V_{in} for four input power conditions, the power versus V_{in} are plotted in Figure 2-21. In Figure 2-21, for increasing input power P_{in} condition from -20dbm to -10dbm, PCE loss stay at 5% but when P_{in} rising from -10dbm to 0dbm, PCE loss tripled for shifting optimum PCE point. This is because t_{off} cannot stay at a constant for P_{in} increasing from -10dbm to 0dbm. When P_{in} is equal to 0dbm and V_{in} is 1 volt, the value of $(V_{out} - V_{in})$ is smallest among other P_{in} conditions. t_{off} would be sensitive to the increment $\Delta(V_{out} - V_{in})$ for smallest $(V_{out} - V_{in})$. In order to solve this problem, principle two is introduced below.

Power detection Principle two: Instead of treating energy pulse $\frac{I_{peak}}{2} \times V_{in} \times (t_{on} + t_{off})$ as a constant in principle one, ADC is applied in principle two. It can digitalize each energy pulse. Then, digial MPPT part can perform the addition and store into register one within T_{fixed} time to compute power1 and power2 in next T_{fixed}. By applying principle two to detect relative power difference between Power1 and Power2, the advantage over principle one is not only the difference of the number of energy pulse is considered but also the single energy pulse value difference is considered. In this case, the accuracy can be improved as shown in Figure 2-22.

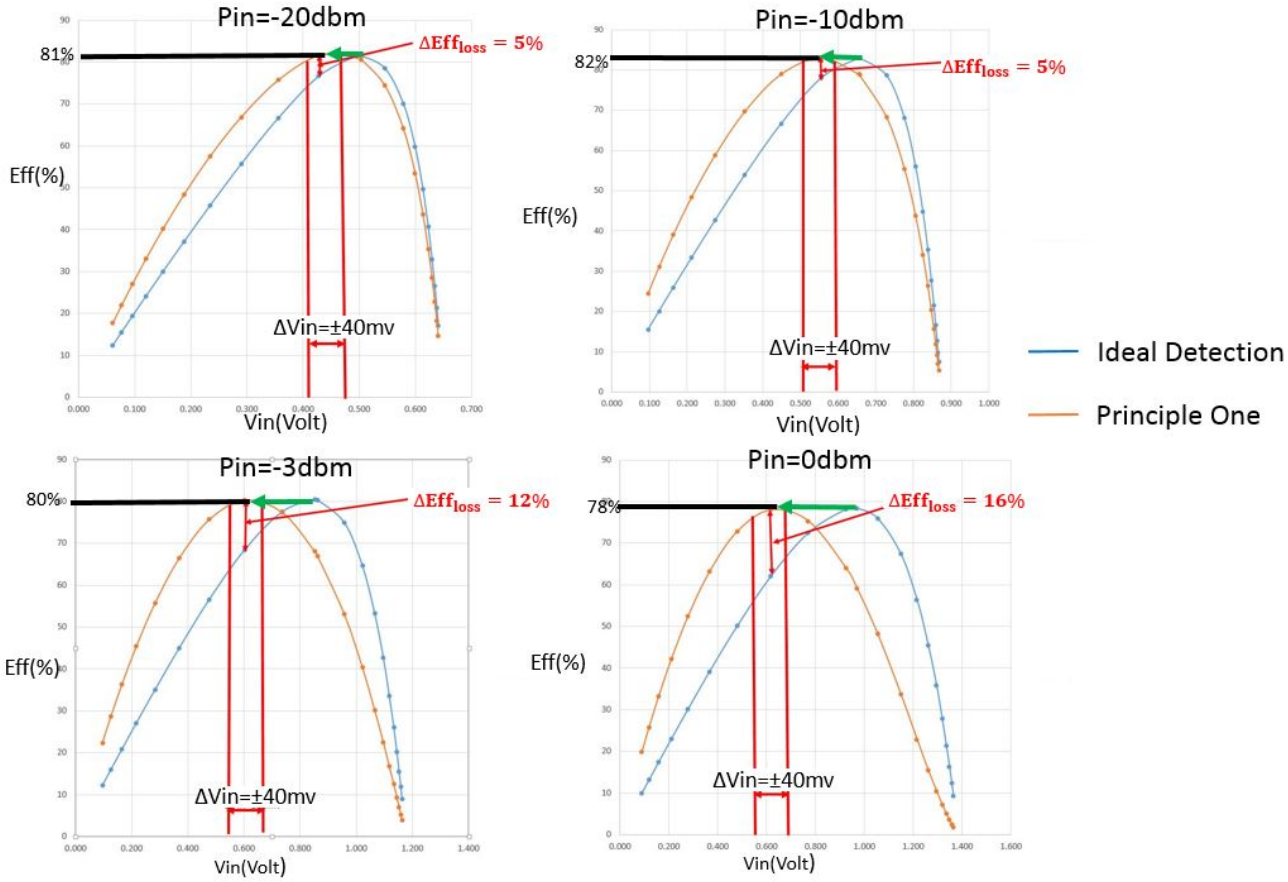

Figure 2-22: PCE versus Vin of DC/DC [Principle One]

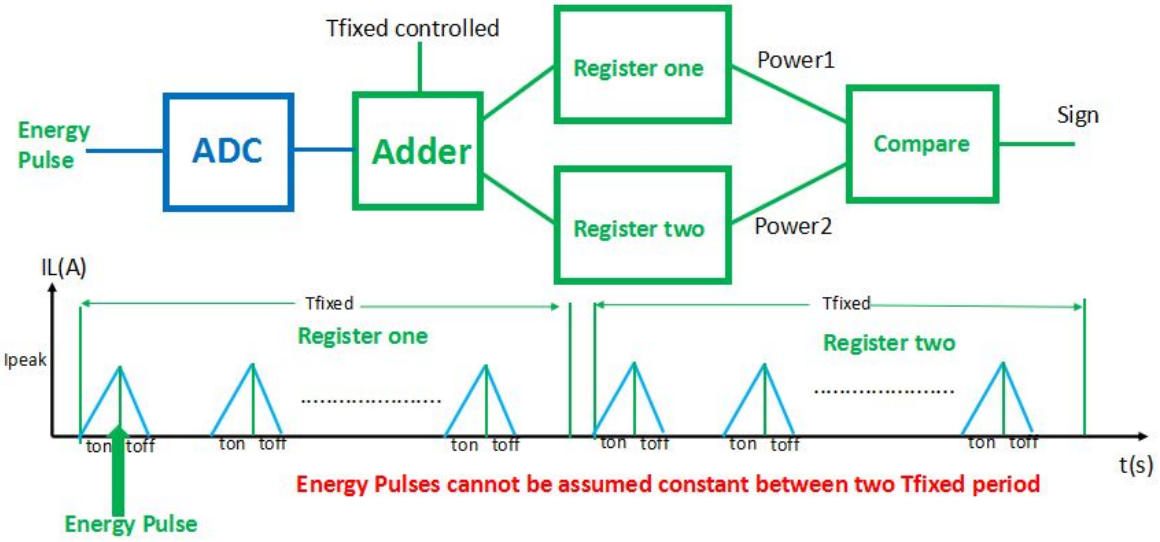

Figure 2-23: Principle Two

To be concluded, Method two is chosen to be the final topology for this design after considering both accurate power tracking and detection for maximum PCE in whole input power range from 8uW to 1mW.

2-5-3 Switches Control Principle

In this project, Harvest Interface is determined to be inductive and discontinuous DC/DC boost converter with I_{peak}=15mA, L1=20uH, C_{in}=400nF, C_{out}=14uF, NMOS switch $\frac{W_{NMOS}}{L_{NMOS}} =$ 3703 and PMOS switch $\frac{W_{PMOS}}{L_{PMOS}} = 14800$.

In this case, I_{peak}=15mA can be used to control NMOS switch during 'Charge Inductor Mode as shown in Figure 2-14. Ton would be triggered at $Vin + \Delta(Vin)$ and generated when linearly increasing IL flow through NMOS switch from power source and Ton finish when IL reach I_{peak}=15mA. After turning off NMOS switch, PMOS switch would be turned on. IL would flow through PMOS switch with its value linearly decreasing during 'Inductor Discharge Mode'. Upon IL crossing 0A, PMOS switch would be turned off to stop IL going negative. Then, NMOS and PMOS switches are both opened and power source would charge Cin from Vin to $Vin + \Delta(Vin)$ during 'Sleep Mode' shown in Figure 2-16. Figure 2-23 displays the state diagram of Switches control method.

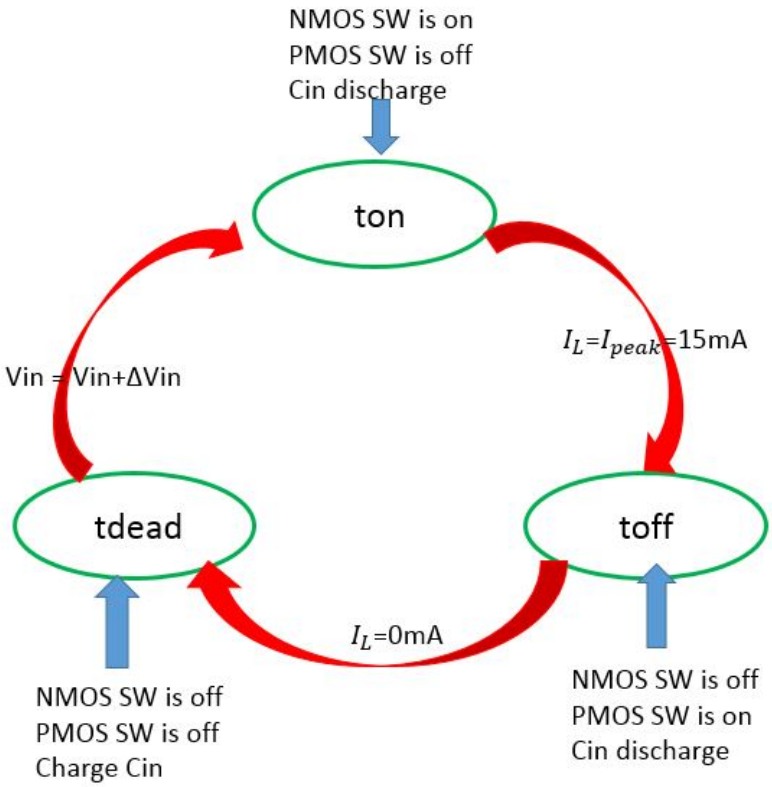

Figure 2-24: State Diagram of Harvest Interface DC/DC converter

2-6 Harvest Interface System Level Design

Figure 2-24 displays Harvest Interface System structure including both analog design part and digital design part. In analog part, not only switch one and two control circuits are designed but also Power Detector, Voltage Reference Generator (VRG) and Low Dropout Voltage Regulator(LDO) are needed. Temperature independent voltage reference 700mV is given to LDO to generate temperature independent 1.1 supply voltage Vdd to DC supply ADC, DAC and Digital Block. 9 bits ADC and DAC can are the interfaces between Analog part and digital part.

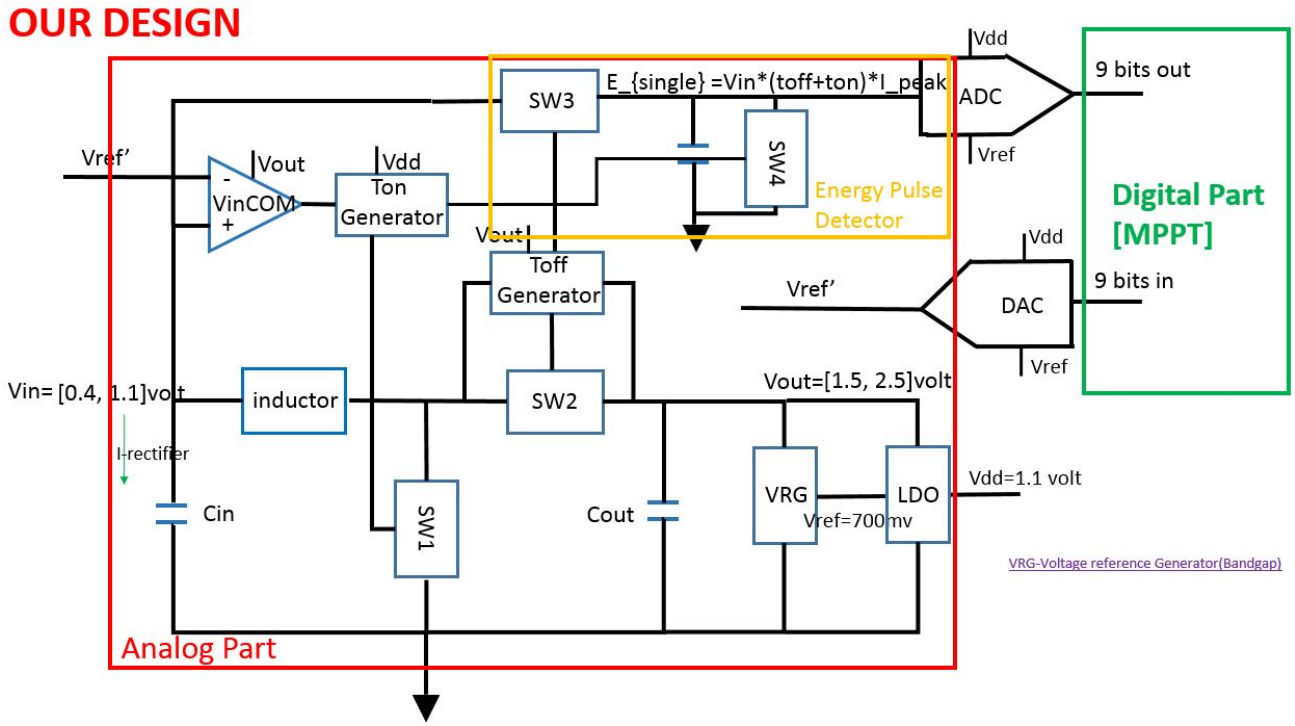

Figure 2-25: Harvest Interface DC/DC converter System Structure

2-6-1 Switch Control System Level Design

System is designed according to State diagram with the initial state of both SW1 and SW2 switched off. Lower power comparator named 'VinCOMP' would detect voltage Vin on Cin referring to V_{ref} generated by DAC and outputs step response to turn on the NMOS switch(SW1), off the PMOS switch(SW2) and meanwhile, trigger 'Tongenerator'. Referring to Figure 2-23, the working state would switch from 'tdead' to 'ton'. Then, 'Tongenerator' would detect I_{peak} of inductor current by detecting the peak voltage Vmid of SW1 to turn on SW2 and off SW1. State changes from 'ton' to 'toff' Next, 'Toffgenerator' can be placed between two terminal of SW2 to detect zero current flow by detecting zero voltage difference of SW2 to turn off SW2. Working state transfer from 'toff' to 'tdead'.

'VinCOM' block should work in a continuous mode but other two circuit blocks: 'Tongenerator' and 'Toffgenerator' can be powered on working duty cycle to save power. Two power save

switches can be added between Vout supply and Vdd of 'Tongenerator' and 'Toffgenerator' blocks. They can be controlled by Ton and Toff correspondingly. Table 2-1 below displays an estimation of power dissipation of three blocks at Pin=8uW and $f_s = 3kHz$ condition. Blocks 'VinCOM', 'Tongenerator' and 'Toffgenerator' all mainly contains a comparator. Based on existing comparators samples designed in IMEC holst-center, low power comparator in TSMC 40nm power consumption is between 250nw to 1uW. In table 2-1 with Pin=8uW condition, 'VinCOM' block working in continuous mode is estimated to be 400nW. 'Tongenerator' block power consumption with duty cycle $\frac{T_{on}}{T_{period}} = \frac{1}{600}$ is less than 1nW and so it is with 'Toffgenerator' block. Considering the leakage current exist in blocks 'Tongenerator' and 'Toffgenerator' with 12.5nA for each branch, power consumption of 'Tongenerator' and 'Toffgenerator' blocks are estimated to 50nW. In Pin=1mW condition, power consumption estimation of 'VinCOM', 'Tongenerator' and 'Toffgenerator' blocks are also estimated in the same way.

Table 2-1: Power dissipation of Blocks 'VinCOM', 'Tongenerator' and 'Toffgenerator' at [Pin=8uW and $f_s = 3kHz$] Or [Pin=1mW and $f_s = 200kHz$]

Block Name	Power Dissipation [Pin=8uW]	Power Dissipation [Pin=1mW]
'VinCOM'	400nW	400nW
'Tongenerator'	50nW	150nW
'Toffgenerator'	50nW	150nW

2-6-2 Energy Pulse Detector Design

Based on equation 2-18, Energy Pulse Detector is applied to detect energy pulse value which is $\frac{I_{peak}}{2} \times Vin \times (t_{on} + t_{off})$ during Ton+Toff and reset to zero after ADC finishing digitalizing energy pulse value. I_{peak} is fixed to be 15mA in this design. In order to achieve the equation $Vin \times (t_{on} + t_{off})$, operational trans-conductance amplifier(OTA) can generate a current proportional to Vin and integrate on a capacitor over Ton+Toff time. However, Vin varies from 400mV to 1V and ΔVin is 40mV. It is difficult and complex to design an OTA with a good linearity, wide input voltage range and extreme low power[less than 400nW].

However, in order to find maximum Power Conversion Efficiency point, $Vin \times (t_{on} + t_{off})$ does not need to be accurate known but relative difference between previous $Vin1 \times (t_{on1} + t_{off1})$ and present $Vin2 \times (t_{on2} + t_{off2})$. Instead of trying to make an ideal Integrator, a simple RC integrator can be applied in this design with same tendency and slope. In Figure 2-25, the equation of RC integrator V_{int} is $V_{in} \times (1 - e^{\frac{-t}{R_{int}C_{int}}})$. The resistance R_{int} is designed 1Mohm and Capacitor C_{int} to be 1pF. SW3 control integration time $t = Ton + Toff$ and SW4 determine reset. Calculation was done to RC integrator output voltage range which is from 0.2V to 0.6V. Comparably, for ideal Integrator, trans-conductance is set to be 0.5u A/V and then, output result is from 0.2V to 0.5V. Next, compare the tendency and slope of ideal Integrator and RC integrator with Vin from 0.4V to 1V as shown in Figure 2-25 below. t_{on} and t_{off} also vary according V_{in} and $V_{out} - V_{in}$ correspondingly referring to Equation (2-1) and (2-2).

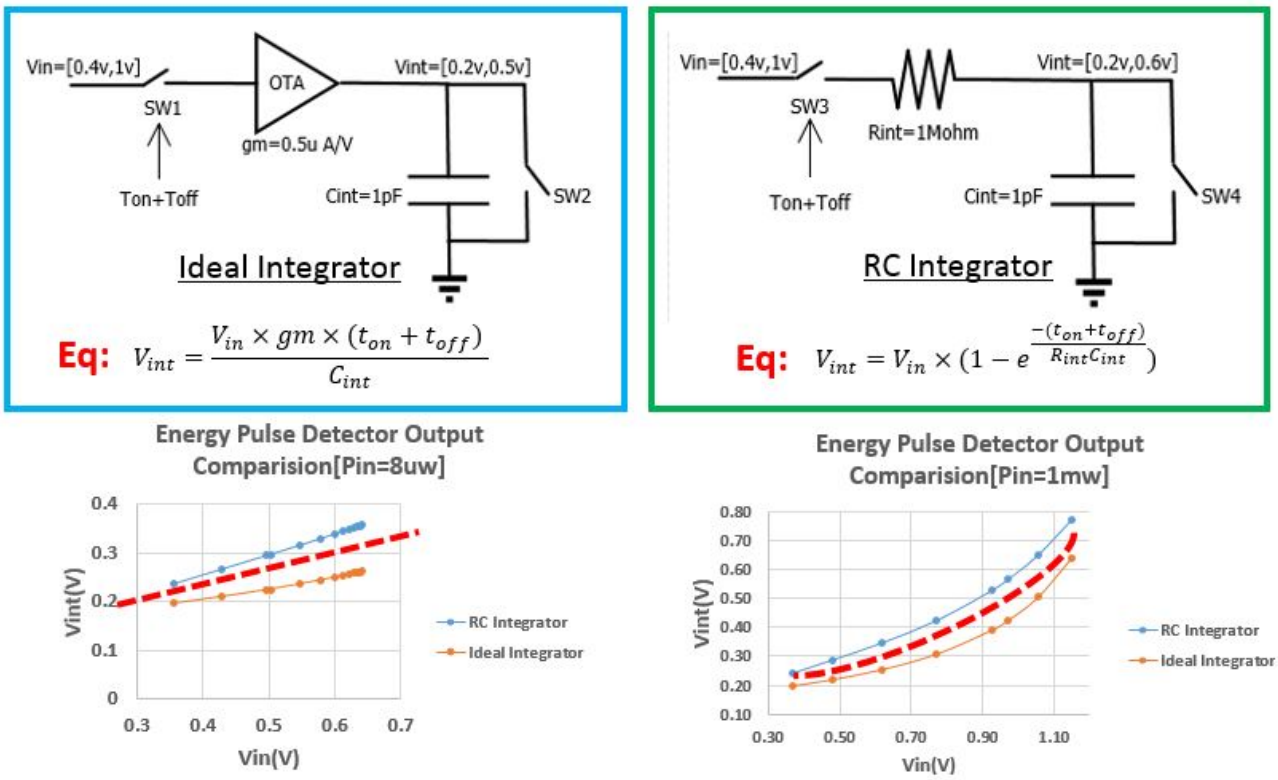

Figure 2-26: RC Energy Pulse Detector/Integrator and Ideal Integrator Output Comparison

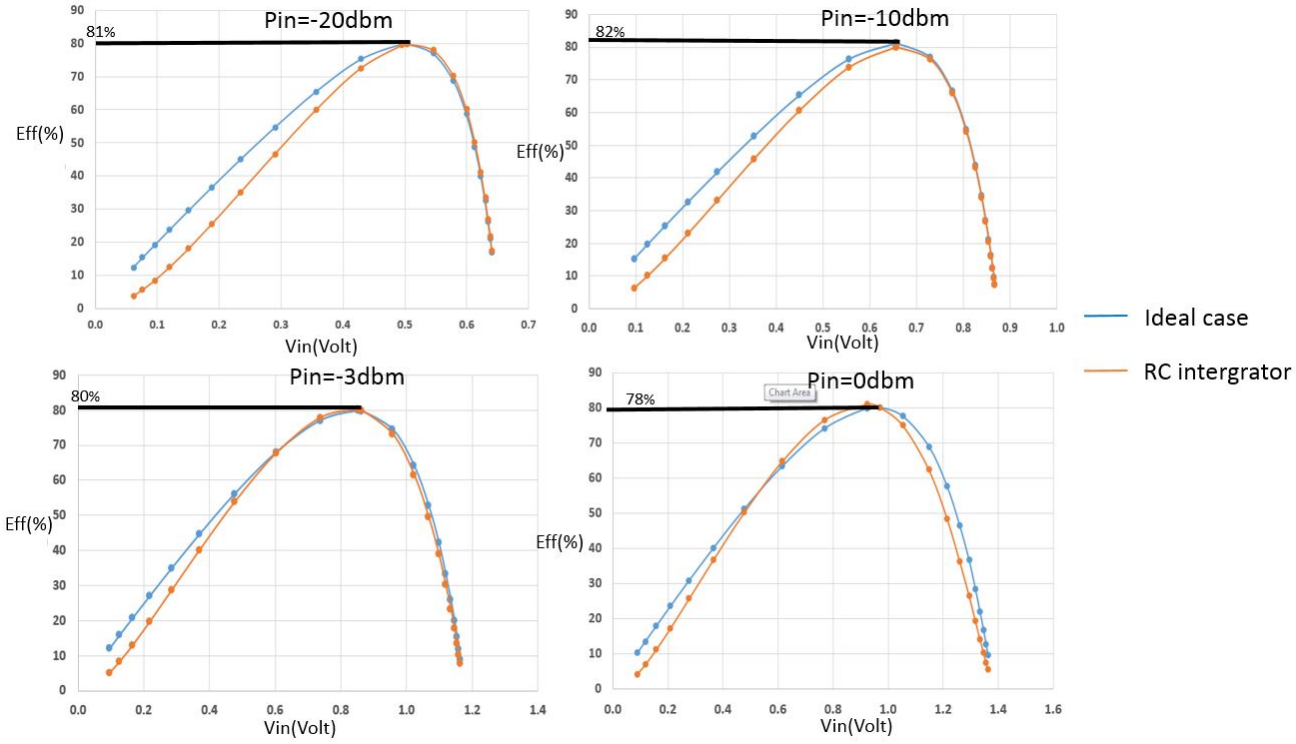

Figure 2-27: PCE versus Vin between Ideal Integrator and RC Integrator

In addition, PCE versus Vin graph was plot to finally verify detection accuracy according to Equation (2-18) by substituting the numerator $\frac{I_{peak}}{2} \times V_{in} \times (t_{on} + t_{off})$ with $\frac{I_{peak}}{2} \times V_{in} \times (1 - e^{\frac{-(t_{on}+t_{off})}{R_{int}C_{int}}})$. For the condition of varying input power of Harvest Interface, PCE points by RC integrator Energy detection method are very close to ideal PCE points which means power tracking would be very accurate. Red asymptote indicate the average tendency and slope.

2-6-3 ADC,DAC,LDO,VGR Blocks Design

The output voltage V_{inte} of Energy Pulse Detector range is from 200mv to 600mv. For V_{in} varies from 400mV to 1V with unit step ΔV_{in} designed to be 40mV. This is because 40mV ΔV_{in} will enable a good PCE at maximum power point for all input power conditions by referring to Figure 2-3. By doing the derivative to RC integrator output Equation $V_{int} = V_{in} \times (1 - e^{\frac{-(t_{on}+t_{off})}{R_{int}C_{int}}})$ with t_{on} and t_{off} referring to Equation (2-1) and (2-2), the graph is plotted between $\frac{d(V_{int})}{d(V_{in})}$ and V_{in} for V_{out} equal to 1.5V, 1.7V, 2.0V and 2.5V. RC Integrator is directly connected to ADC and the minimum resolution of ADC can be determined by the lowest derivative of RC Integrator output times the unit step ΔV_{in}. The unit step ΔV_{in} is equal to 40mV and lowest derivative of RC Integrator output is found to be 0.23 at V_{out} equals to 2.5V when V_{in}=0.7V. In this case, minimum resolution is computed as 9mV. Therefore, at least 6 bits ADC are needed to digitalize V_{inte}. Considering worse ADC working case: one Effective Number Of Bit (ENOB) loss, 7 Bits ADC is required to be applied.

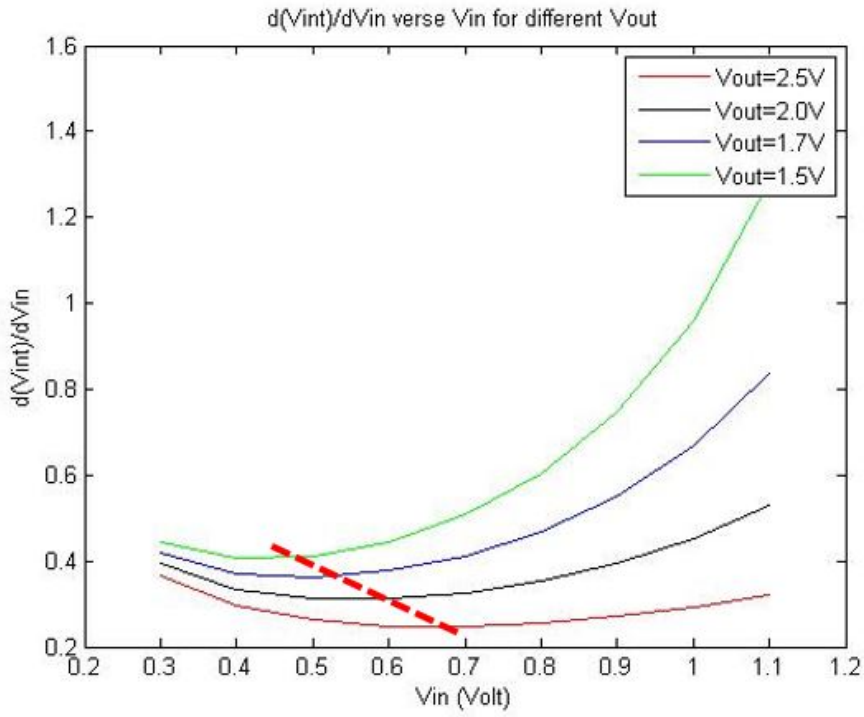

Figure 2-28: PCE versus Vin between Ideal Integrator and RC Integrator

Working frequency of Harvest Interface System varies from 3kHz to 100kHz with low power consumption requirement. Therefore, in this design, ADC topology is chosen to be SAR ADC. Before this design, an existing Ultra Low Power 9 bits SAR ADC which has already been designed by Dr Ming Ding in IMEC Holst-center with 1.0V Vdd supply and 8.5 ENOB is chosen. For 8uW DC/DC input power condition, working frequency of SAR ADC should be 3kHz and power consumption for this ADC is 5.7fJ/Conversion Step for 16MSPs sampling rate based on the Technical Note. Then, SAR ADC 3kHz working frequency power consumption is calculated as $P_{ADC-loss} = P_{leakage} + 2^9 \times f_s \times E_{conversion-step}$= 409nW. The switch capacitors DAC is taken from inside the 9 bits SAR ADC with power consumption 205nW schematic simulation results.

Analog LDO structure is composed of an opamp, feedback and a transistor shown in Figure 1-5. The power loss of a LDO containing the quiescent current power loss, the continuous opamp power loss and the dropout voltage power loss. The minimum quiescent current for Analog LDO achieved in IMEC Holst-center is 35nA, opamp continuous working current is 150nA and average load current needed to be achieved is equal to 200nA for 8uW input power condition. By applying this equation $P_{LDO-loss} = P_{Quiescent-current} + P_{Opamp} + P_{Dropout-Voltage}$. The supply voltage of LDO vary from 1.5V to 2.5V and output voltage is 1V. By taking average 2V for LDO supply and $P_{LDO-loss}$= 70nW+300nW+400nW=570nW. VRG blocks power consumption depends on topology which is roughly assumed to be 400nW before defining the topology and it would be analysed and verified in later Chapter three.

For 1mW input power condition with 200kHz working frequency, the power consumption of ADC can be computed by same equation and the result is 990nW. Power consumption of DAC is 320nW and VRG block is 400nW which is frequency independent. For LDO power loss, the average load current would roughly be $\frac{200kHz}{3kHz}$ times bigger than LDO working at 3kHz. Based on Equation: $P_{LDO-loss} = P_{Quiescent-current} + P_{Opamp} + P_{Dropout-Voltage}$=13uW. In conclusion, the blocks power estimations in Pin=8uW and Pin=1mW two conditions are given on table 2-2.

Table 2-2: Power dissipation estimation of Blocks LDO, DAC, VRG and ADC in TSMC 40nm at Pin=8uW and Pin=1mW

Block Name	Power Dissipation for Pin=8uW	Power Dissipation for Pin=1mW
LDO	570nW	13uW
DAC	205nW	320nW
VRG	400nW	400nW
ADC	409nW	990nW

2-6-4 Digital Part Design

After ADC finishing digitalizing, voltage on C_{int} would be reset and 9 bits SAR ADC output would be the input digital part to perform Maximum Power Point Tracking as shown in Figure 2-21. Besides, fast digital part clock f_{fast} would be given by SAR ADC redundancy bit and slow clock would be given from outside. Digital part would compute new power value, comparing with previous power value and determine Vin varying direction on each cycle.

Figure 2-18 gives the flow chart of digital algorithm. 'FLCK trigger' stands for fast clock trigger which is the conversion ready bit from 9bits SAR ADC. 'SCLK trigger' represents slow clock trigger would be given from out of chip Serial Peripheral Interface Bus (SPI). Total four registers are needed. Register 1 and Register 2 which are controlled by positive and negative edge of slow clock correspondingly are used to accumulate input bits from ADC. Block 'COM' would compare Register 1 with Register 2 and polarity generated by 'COM' together with previous output of 'XOR-NOT' block would be excursive or not treated.

Figure 2-19 shows the partial working timing diagram of digital part. Slow clock is in 50 percent duty cycle and positive edge of slow clock indicate that Register 1 begin to reset and then, accumulate within 50 % slow clock duty cycle. Negative edge of slow clock would mean that register 1 stop to accumulate and keep its state. Besides, register 2 begin to reset and then, accumulate within the next 50 % slow clock duty cycle. 'COM' would compare the Register 1 with Register 2 upon slow clock negative edge and Register 2 with Register 1 on slow clock positive edge. 'Sign Reg3' would record the previous slow clock half cycle information of 'XOR-NOT' block and output of 'XOR-NOT' block would be excursive or not of 'COM' and 'Sig Reg3' blocks' outputs. Finally, value in Register 4 would add or subtract a 24 in decimal according to 'XOR-NOT' output. DAC would converter digits of Register 4 to voltage reference signal supplied to 'VINCOMP' block.

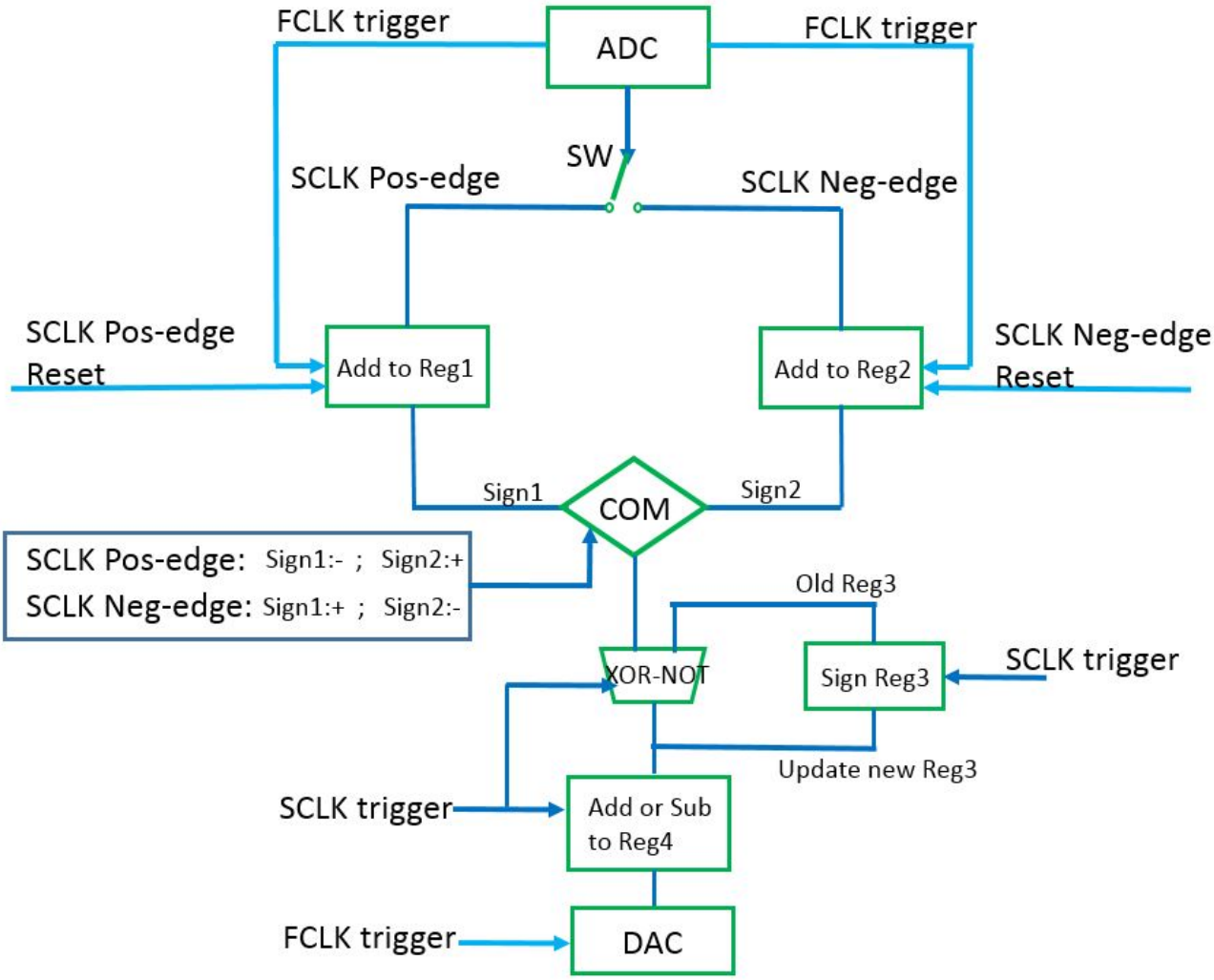

Figure 2-29: Digital Algorithm Flow Chart

The size of sign register 3 is one bit SR-latch. DAC is designed to be 9bits and therefore, Register 4 is 9 bits. In order to avoid the saturation condition happening in high input power condition P_{in}=1mW, register 1 and register 2 size are both 20 bits. The minimum half cycle period of slow clock is determined to be 25ms long to avoid quantization error happened at Register 1 and Register 2 during comparison at low input power condition P_{in}=8uW.

At the output of power detector, the single energy pulse is from 200mV to 600mV which is from 103 to 308 in binary at the output of 9bit SAR ADC. This is because for P_{in}=8uW, maximum Harvest Interface working period is equal to 450us and only 55 energy pulse can be detected within 25ms. As shown in Figure 2-21, considering at maximum PCE point, two relative power difference for 25ms is equal to 165 in binary which is larger than 103, the single energy pulse in binary. In this case, quantization error can be avoided. In addition, for P_{in}=1mW, the minimum Interface working period is equal to 8us and number of 3125 energy pulses are accumulated with single energy pulse 308 in binary. At least, both Register 1 or Register 2 should have 962500 binary space which is 20 bits for both register one and two to avoid saturation.

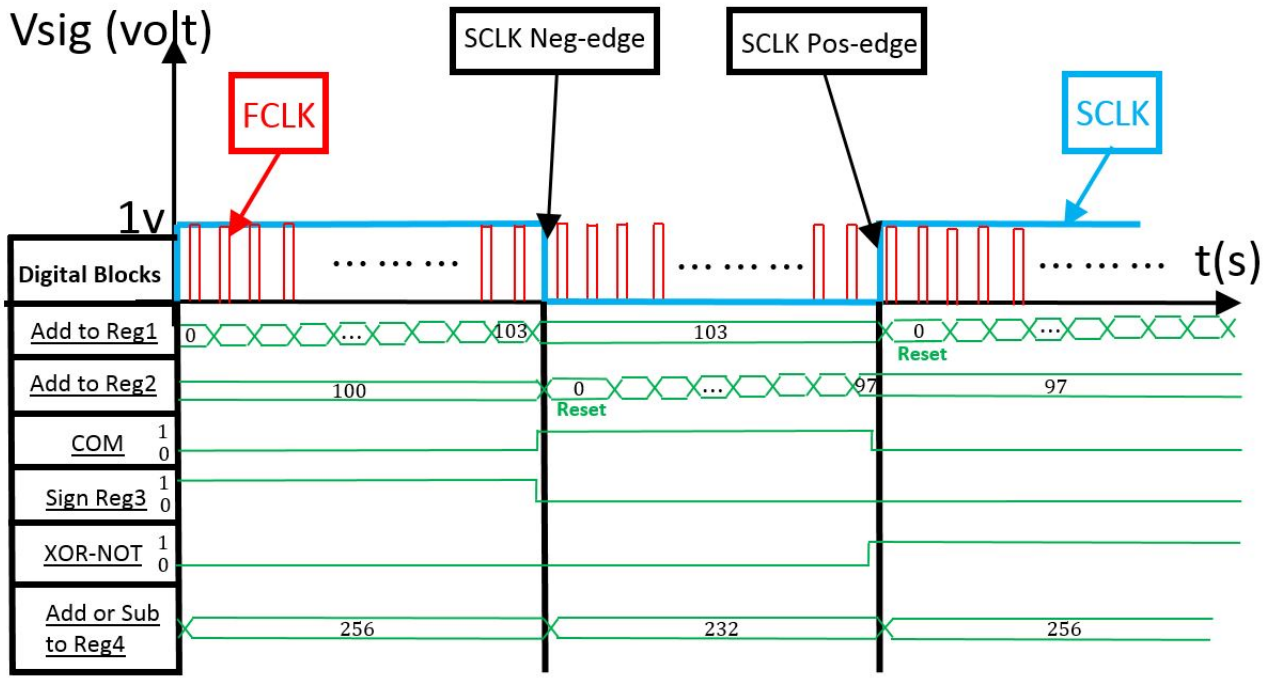

Figure 2-30: Digital Blocks Timing Diagram

After finishing the RTL coding of this digital block and net-list generating, the gate level power consumption simulation has been done for digital MPPT block at two different working frequencies 3kHz and 200kHz. For $f_s = 3kHz$, P_{MPPT}=150nW and with $f_s = 200kHz$, P_{MPPT}=650nW.

2-7 Harvest Interface System Power Budget Estimation

To be concluded, the estimated power consumption for blocks both analog and digital are shown in Figure 2-30 for Pin P_{in}=8uW. The minimum power loss requirement should be less than 4uW and in this design, harvest system power loss is estimated to be 2.58uW which give extra 1.42uW design space for blocks' schematic and layout. In Figure 2-31, in high power 1mW with 200kHz working frequency condition, the switches, the bondwire and the inductor would take up the most significant portion of total power loss and the dropout voltage power loss would also increase significantly due to the significant increasing of loading current.

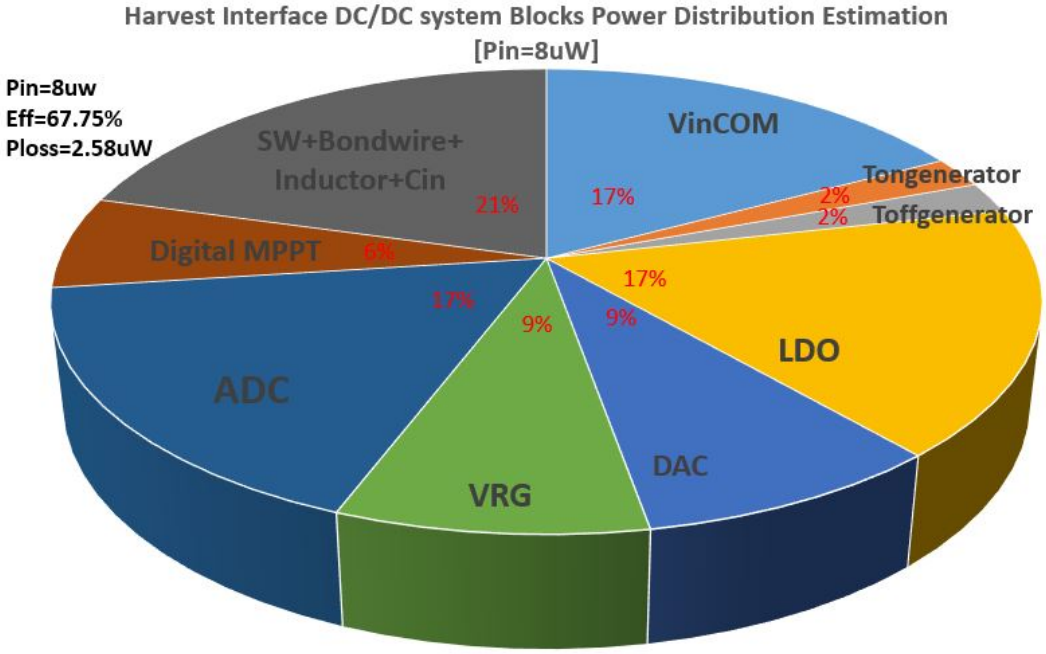

Figure 2-31: Harvest System Blocks Power Distribution Estimation for Pin=8uW

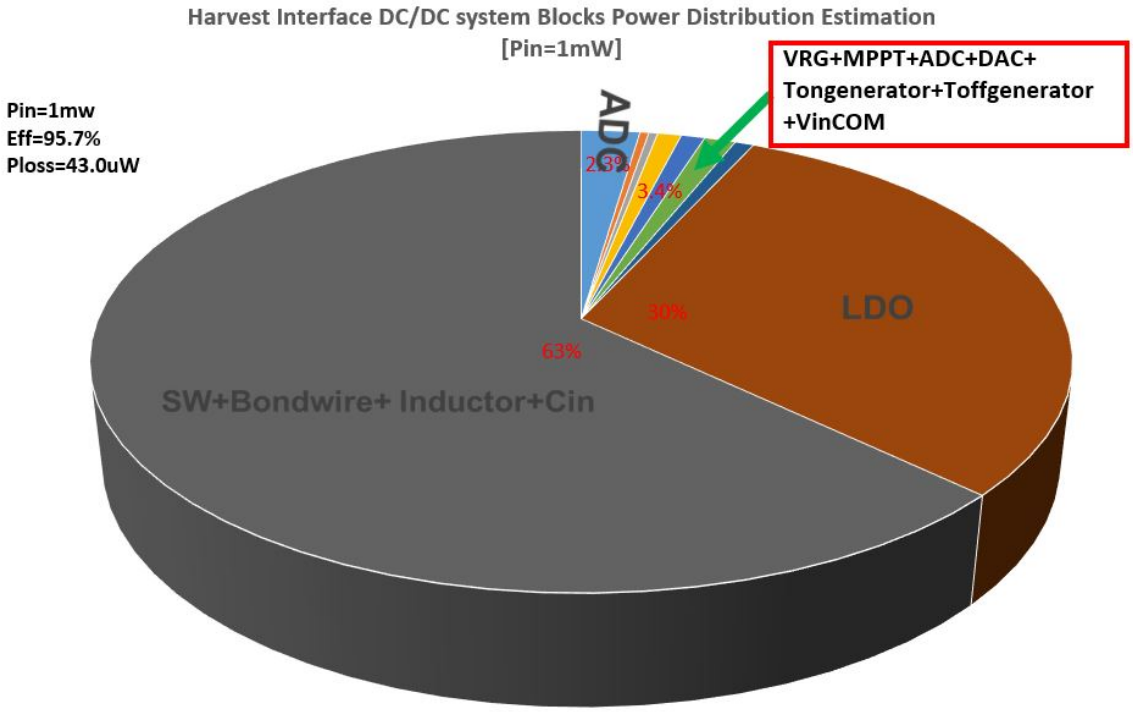

Figure 2-32: Harvest System Blocks Power Distribution Estimation for Pin=1mW

Chapter 3

Harvest Interface Schematic Level Design

3-1 Voltage Reference Generator(VRG)

In this design, Voltage reference generator be needs to generate a voltage reference for LDO and also ADC. Reference voltage should have the characteristics of good power supply rejection ratio (PSRR), good temperature independence and process independence. The output requirement of LDO is from 1 volt to 1.1 volt which require little less voltage variation on reference voltage. LDO would be applied to supply ADC, DAC, Digital and certain analog blocks. In this design, supply voltage V_{out} of voltage reference generator is varied from 1.5 to 2.5 volt, working temperature within -40 to 125 Celsius degree and power consumption should be less than 400nW. Subsections below would introduce Peaking current source to achieve a Lower power design. By applying MOS diode, increasing temperature effect can be compensated. Combined Peaking current source with MOS diode design, high PSRR can be achieved. Finally, the VRG block circuit behaviors including temperature dependence, process dependence and PSRR would be checked by simulation results.

3-1-1 Peaking Current Source

In order to achieve a low power design of voltage reference, Peaking Current Source could be a choice [11]. Figure 3-1 on the left displays schematic view of peaking current source. The input of peaking current source is named as I_{in} and the output is named I_{out}. The input current would flow through resistor R1 and transistor M1. The voltage V1 would drive M1 and V2 drive the gate of M2. Both M1 and M2 are working at weak inversion condition. The Equation (3-1) can be derived by $V_{gsM1} - V_{gsM2} = I_{in} \times R1$. Meanwhile, the plot of Equation (3-1) is displayed in Figure 3-2. With input current vary from 35nA to 105nA, output current increase from 20.5nA, reaching maximum point 23.9nA and then decrease with Power supply rejection ratio 18dB. The maximum point happens at $\frac{d(I_{out})}{d(I_{in})}$=0 for $V_T = I_{in} \times R1$. In this design, R1 is designed to be 400kOhm and I_{in} equals to 65nA at maximum point.

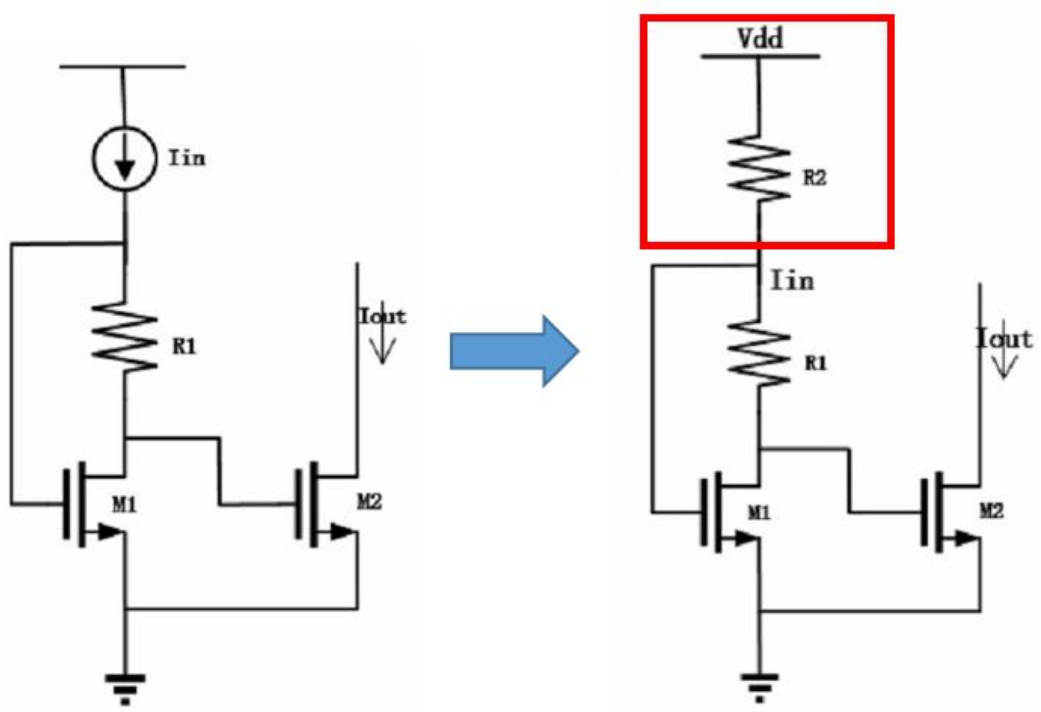

Figure 3-1: Schematic View of Peaking Current Source

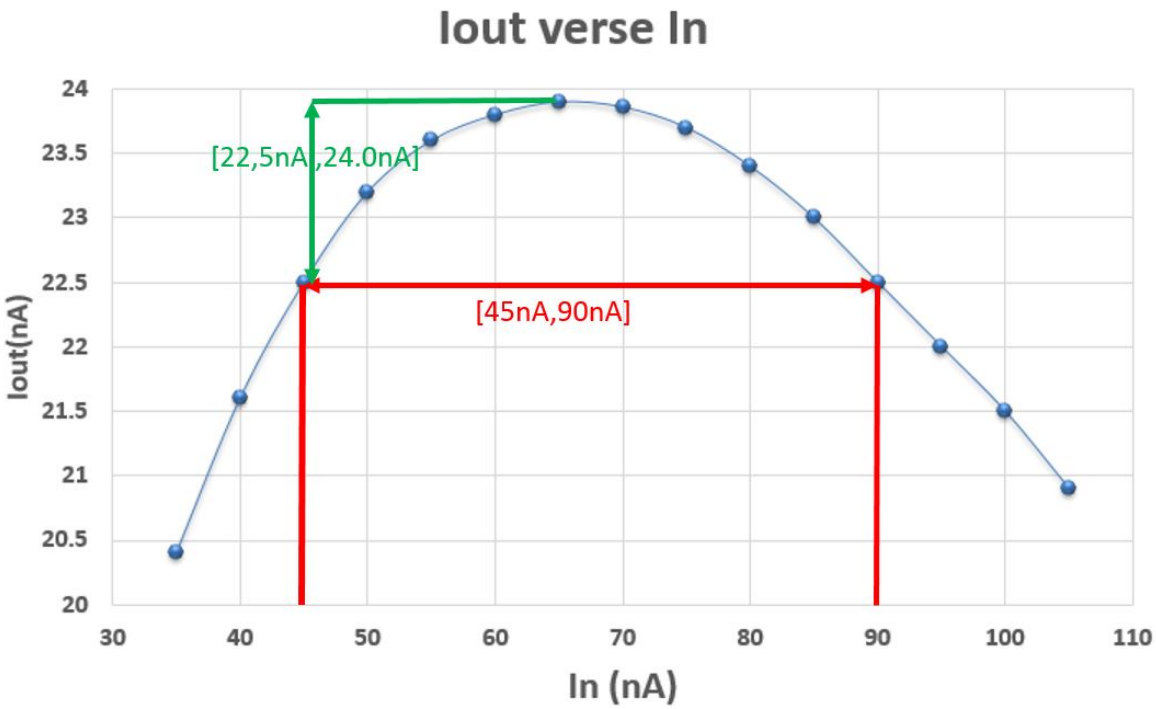

Figure 3-2: I_{out} versus I_{in} for Peaking Current Source

$$\ln\left(\frac{I_{in}}{I_{out}}\right) = \frac{I_{in} \times R1}{V_T} \tag{3-1}$$

Varying input current I_{in} can be transferred into varying input voltage V_{in} by adding a big resistor R2 15MOhm calculated by Equation (3-2) shown in Figure 3-1 on the right. The varying I_{in} does not have to be very accurate but R1 needs to be accurate which would influence the location of I_{in} for I_{out} peaking point. The power consumption can be greatly reduced. The average power consumption of peaking current source shown in Figure 3-3 is 250nW.

$$I_{in} = \frac{V_{in} - V_{gsM1}}{R2} \tag{3-2}$$

3-1-2 Diode Temperature Compensation

In Figure 3-3, I_{out} would then be mirrored by transistors from M3 to M4 both are in saturation region. Current I_{out} through transistors M3 and M4 are positive temperature dependent because of the factor 'V_T' which is equal to $\frac{KT}{q}$. In order to compensate positive temperature effect, the current can flow through a negative temperature diode. The Equation (3-3) gives the relationship of voltage V_{gs} versus current I_D for a MOSFET diode M3 working in saturation condition. MOS M3 with gate terminal connecting to Drain terminal, therefore, V_{gsM3} is also equal to V_{dsM3} and V_{ref}. Current I_D of the diode would be negatively influenced by the temperature due to negative V_{th}. By proper tuning $\frac{W}{L}$ of MOS M3, temperature effect can be cancelled.

$$I_D = \mu C_{ox} \frac{W}{2L} (V_{gs} - V_{th})^2 \tag{3-3}$$

Based on Equation (3-3), graph is plotted with V_{gsM3}[or V_{dsM3}, V_{ref}] versus I_{dsM3} shown in Figure 3-4. With I_{ds} varying from 22.5nA to 24.3nA, V_{gsM3} [or V_{dsM3}, v_{ref}] changes from 0.602V to 0.6052V and PSRR between V_{out} and V_{ref} is calculated to be 42dB by applying Equation (3-4).

$$PSRR = 20 \times \log_{10}\left(\frac{\Delta V_{out}}{\Delta V_{ref}}\right) dB \tag{3-4}$$

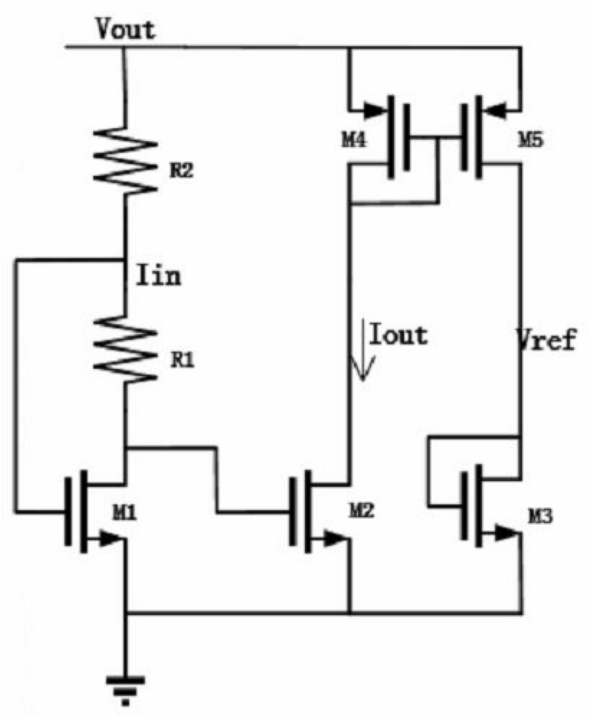

Figure 3-3: Voltage Reference Generator

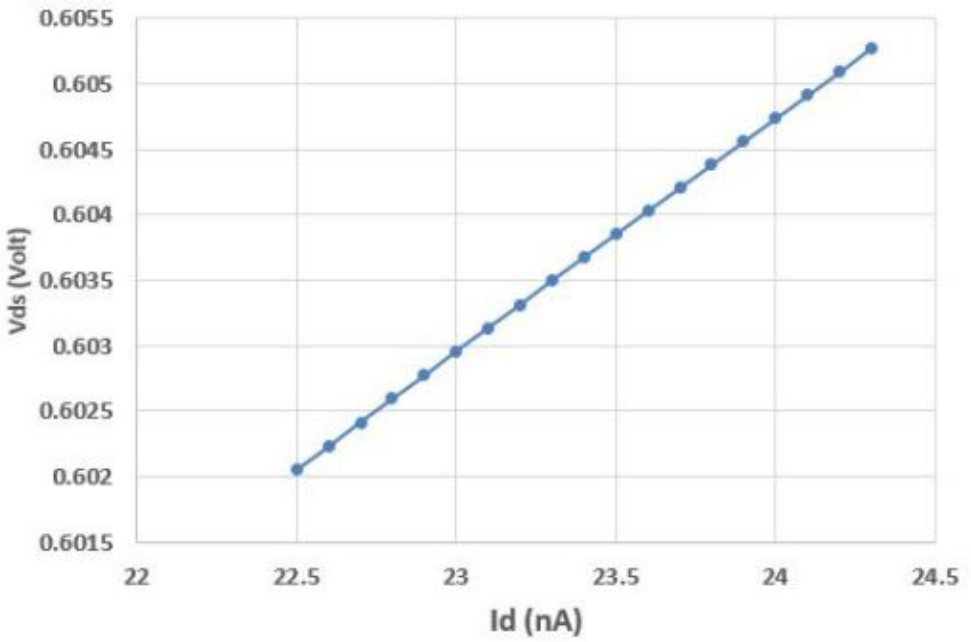

Figure 3-4: V_{ds} versus I_{ds} for MOS diode M3

3-1-3 Process, Voltage and Temperature (PVT) and Power Loss schematic Simulations of VRG block

Figure 3-5 displays the relationship between output reference voltage V_{ref} and temperature variation which is from -50 Celsius degree to 125 Celsius degree. For -50 Celsius degree to 125 Celsius degree temperature variation, the maximum reference voltage variation which is 28mV occurs when V_{out} is equal to 1.5V. In the room temperature, for a 1.5V to 2.5V supply voltage V_{out} variation, the voltage variation occurs at V_{ref} is equal to 17mV. Power Supply Rejection Ratio (PSRR) can be computed to be 35.4dB by Equation (3-4). The average power consumption is simulated to be 430nW at 'TT' Corner in the room temperature. In Figure 3-6, the reference voltage versus temperature variation in 'SS', 'SF', 'FS', 'TT' and 'FF' process corners are plotted with maximum $\Delta Vref$=81mV voltage variation.

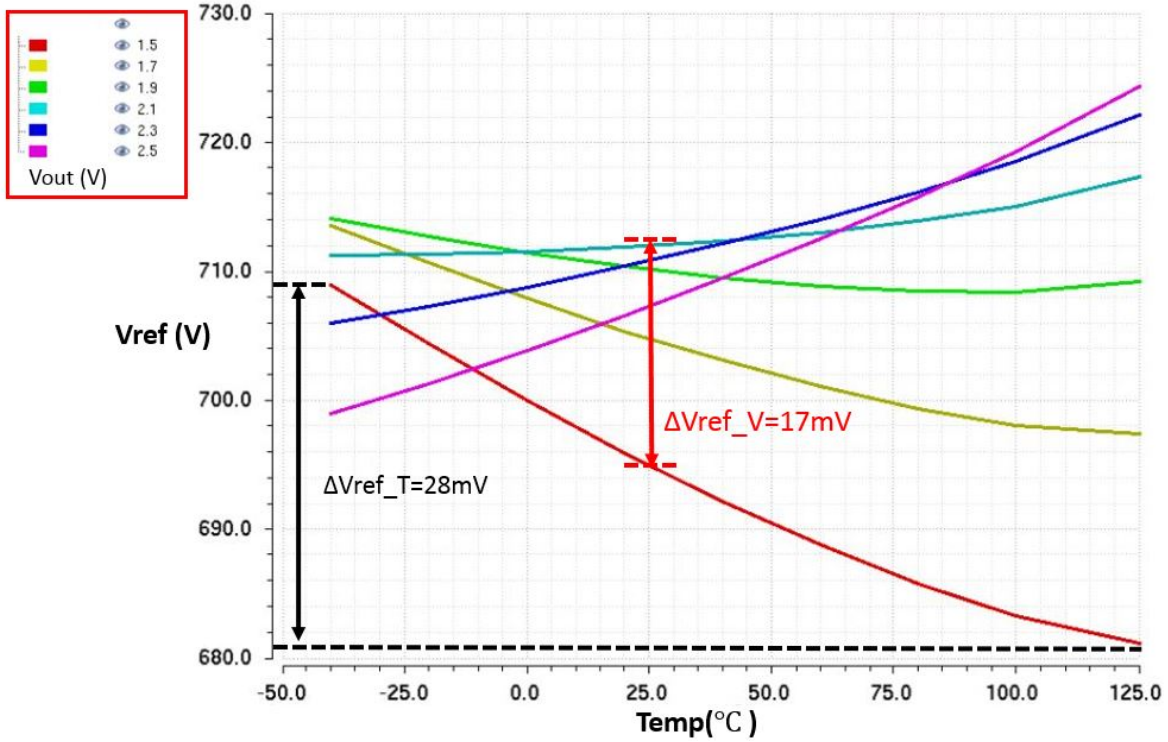

Figure 3-5: V_{ref} versus $Temperature$ of VRG block for V_{out} range [1.5, 2.5]V

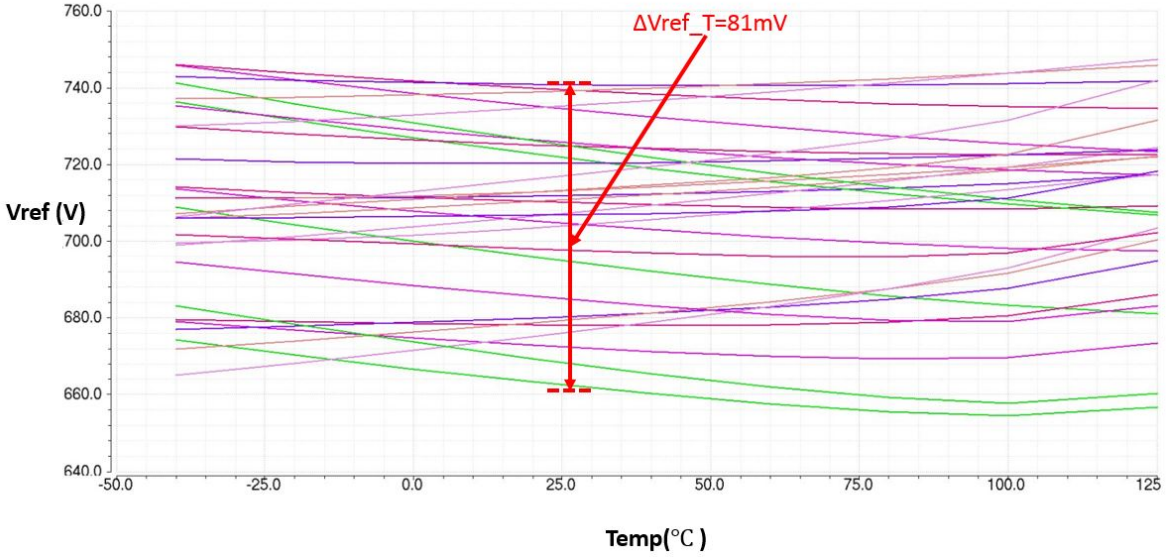

Figure 3-6: V_{ref} versus $Temperature$ of VRG block for V_{out} range [1.5, 2.5]V in SS to FF process corners

3-2 Voltage Comparator-"VinCOMP" Block

Referring to Figure 2-24, "VinCOMP" block need to compare the input voltage of Harvest interface DC/DC converter with output voltage of DAC. The DC voltage level of two inputs terminals are from 300mV to 1.1V. The voltage difference ΔV_{in} between $V+$ and $V-$ is 45mV. In addition, "VinCOMP" works in a time continuous mode and should be low power consumed.

The proposed schematic structure is shown in Figure 3-7. The comparator has two differential pairs comparators including one NMOS differential pair marked in 'Green' rectangle and one PMOS differential pair comparator in 'Red'. PMOS differential pair comparator is responsible for the detection at [300mV, 600mV] input DC voltage level and NMOS differential pair comparator for [600mV, 1.1V] voltage range. 'Purple' parts are two current sources for two comparators.

Transistors M10, M11, M5 and M6 are working in saturation condition. Transistors M5 and M6 can mirror current from M10 and M11 correspondingly. When input DC voltage level varies in [300mV, 600mV] range , PMOS differential pair transistors M1 and M2 are working in saturation condition and also, transistors M10 and M11. However, for NMOS differential pair transistors M3 and M4 work in weak inversion region and also for M10 and M9. In this case, for two voltage difference (V1,V2), PMOS differential pair comparator would have a dominant effect comparing to NMOS differential pair comparator. For [600mV, 1.1V] range, instead, NMOS differential pair comparator would have a dominant effect contribute to V1 and V2 voltage difference.

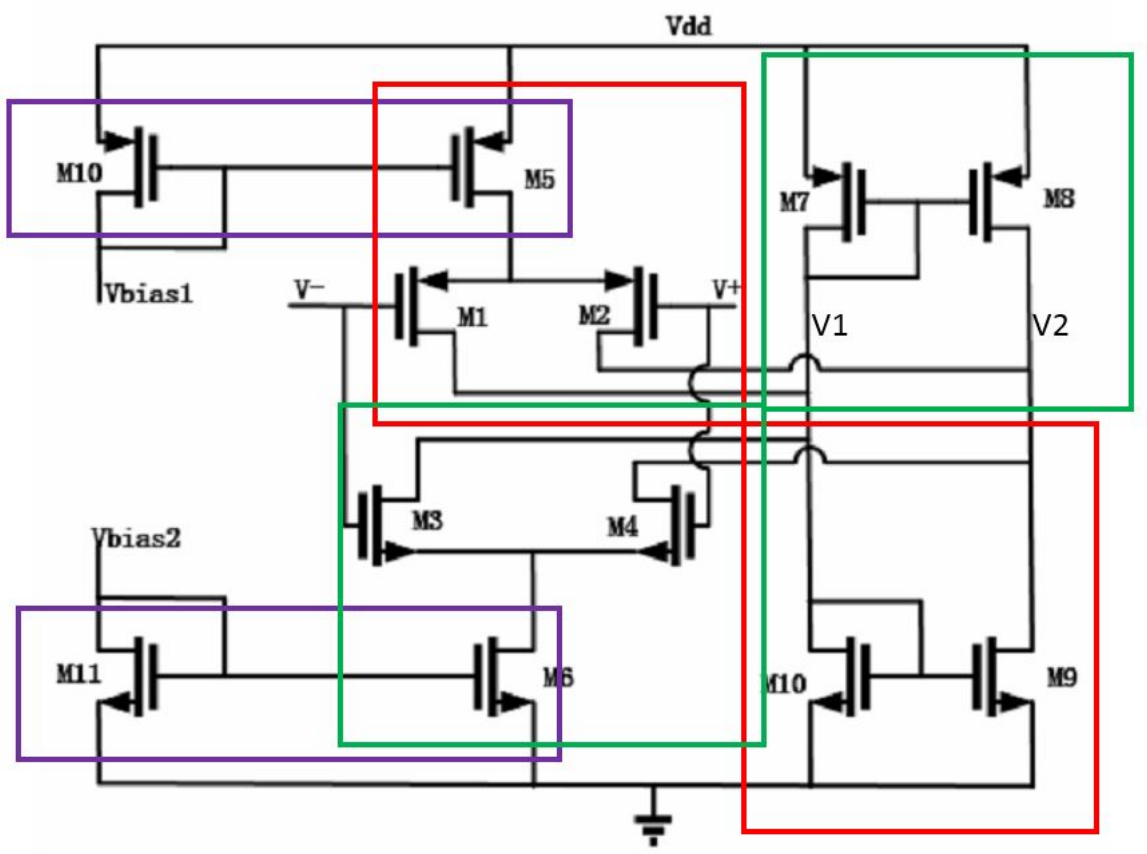

Figure 3-7: Schematic of "VinCOMP"

3-2-1 Comparator Monte Carlo Simulation

The input offset is an important factor which would limit the comparator accuracy. Comparator offset would be process dependent resulting from threshold voltage variation during MOS transistor fabrication. The offset of this comparator should be less than the maximum voltage difference between two input terminals of comparator and the maximum voltage difference is designed to 40mV. Equation (3-5) gives an estimation of offset voltage on PMOS or NMOS transistor. In TSMC 40nm, A_{VT} is equal to 5mV/um for NMOS transistor and 8mV/um for PMOS. In this comparator, one of the input differential terminal $V-$ is connected with both NMOS ($\frac{W}{L} = \frac{340nm}{4um}$) and PMOS transistors ($\frac{W}{L} = \frac{340nm}{3um}$). The maximum offset would be the sum of NMOS and PMOS offset voltages when both NMOS and also PMOS are working together. By applying Equation (3-5), the offset at $V-$ or $V+$ terminal would have a range of [4.28, 12.25]mV. In order to verified the offset calculation result, Monte Carlo simulation with 200 number of simulation points was done to block 'VinCOMP' to test offset spread when comparator output signal is rising up with 0.7V DC level. The mean voltage of total offset points is equal to 544.22uV with maximum 20mV offset spread within 3 standard deviation. Maximum 20mV offset spread is still less than 40mV input voltage difference and meet the offset requirement. The input voltage range of this comparator is from 0.5V to 1V and then, Monte Carlo simulation for 0.5V and 1.0V DC levels are also checked with maximum spread less than 40mW shown in Figure 3-9 and Figure 3-10.

$$V_{os} = \frac{A_{VT}}{\sqrt{W \times L}} \tag{3-5}$$

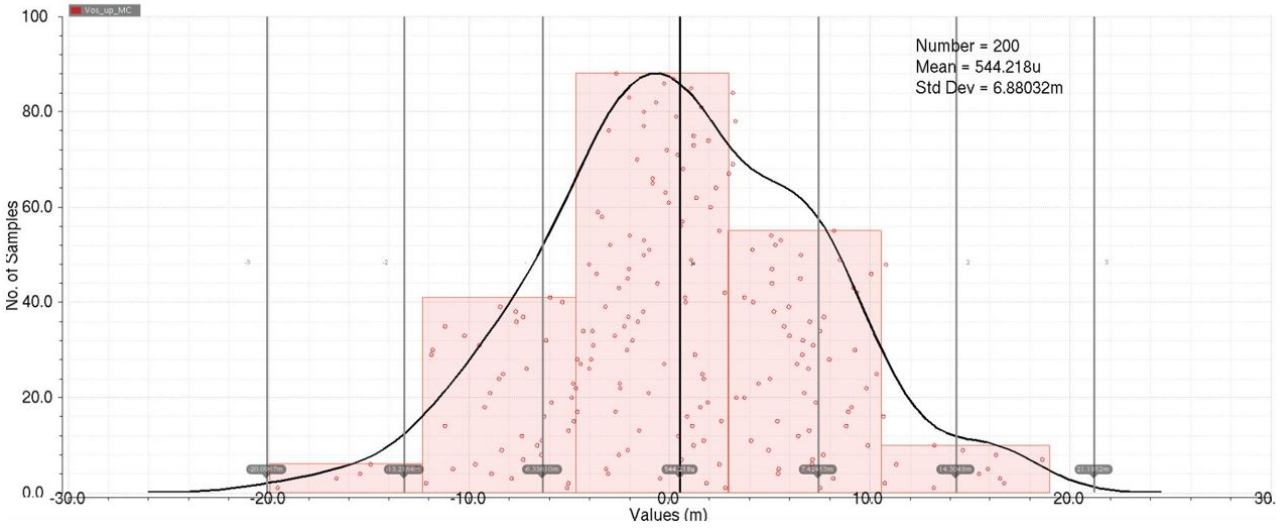

Figure 3-8: Monte Carlo Simulation of 'VinCOMP' with 0.7V DC level

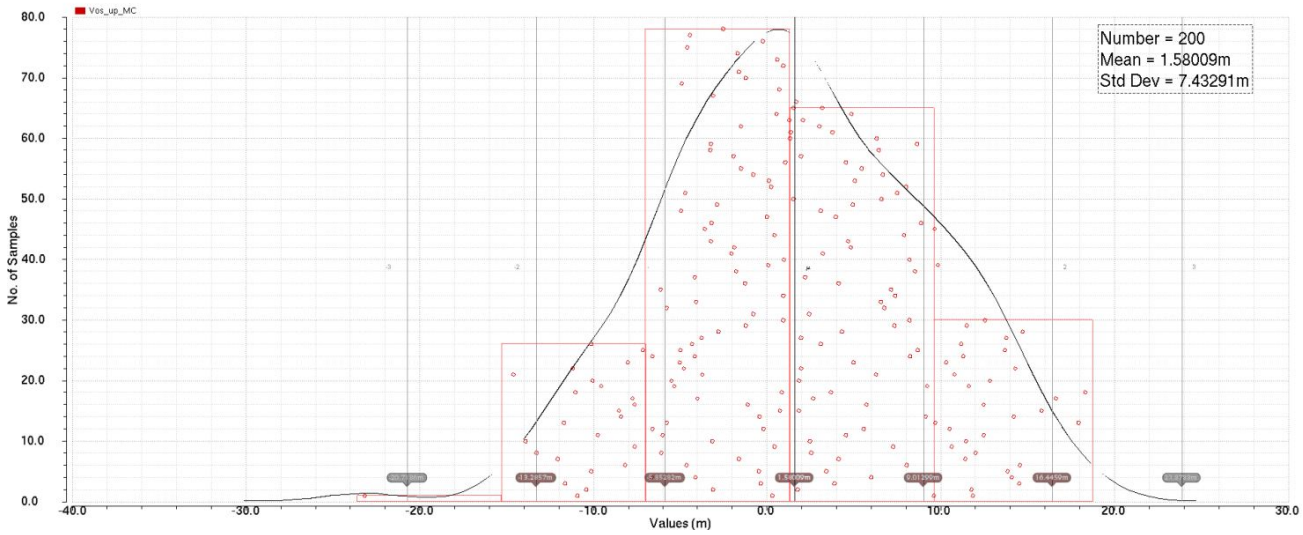

Figure 3-9: Monte Carlo Simulation of 'VinCOMP' with 1.0V DC level

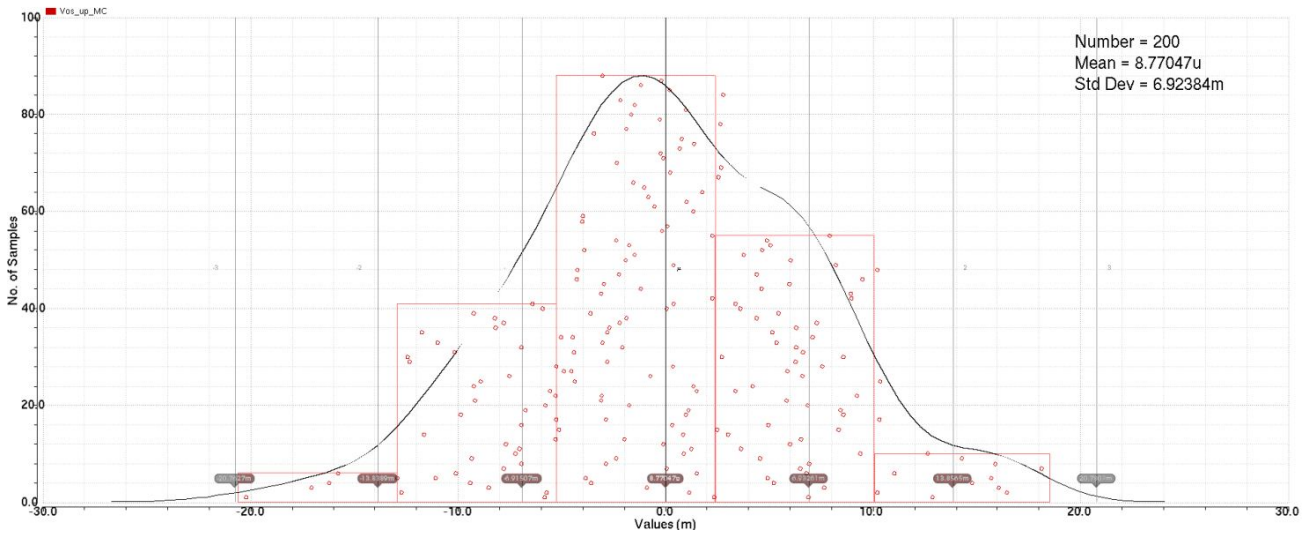

Figure 3-10: Monte Carlo Simulation of 'VinCOMP' with 0.5V DC level

3-3 Ton-generator

Block 'Ton Generator' generate switch one control signal ton. It is firstly positive edge triggered by the output signal from block 'VinCOMP' and ton finish when the maximum current flow through switch one is equal to I_{peak} which is 15mA in this design. Figure 3-11 display the blocks inside 'Ton Generator' which are 'IpCOMP Enable', 'IpCOMP' and 'Schmitt Trigger'.

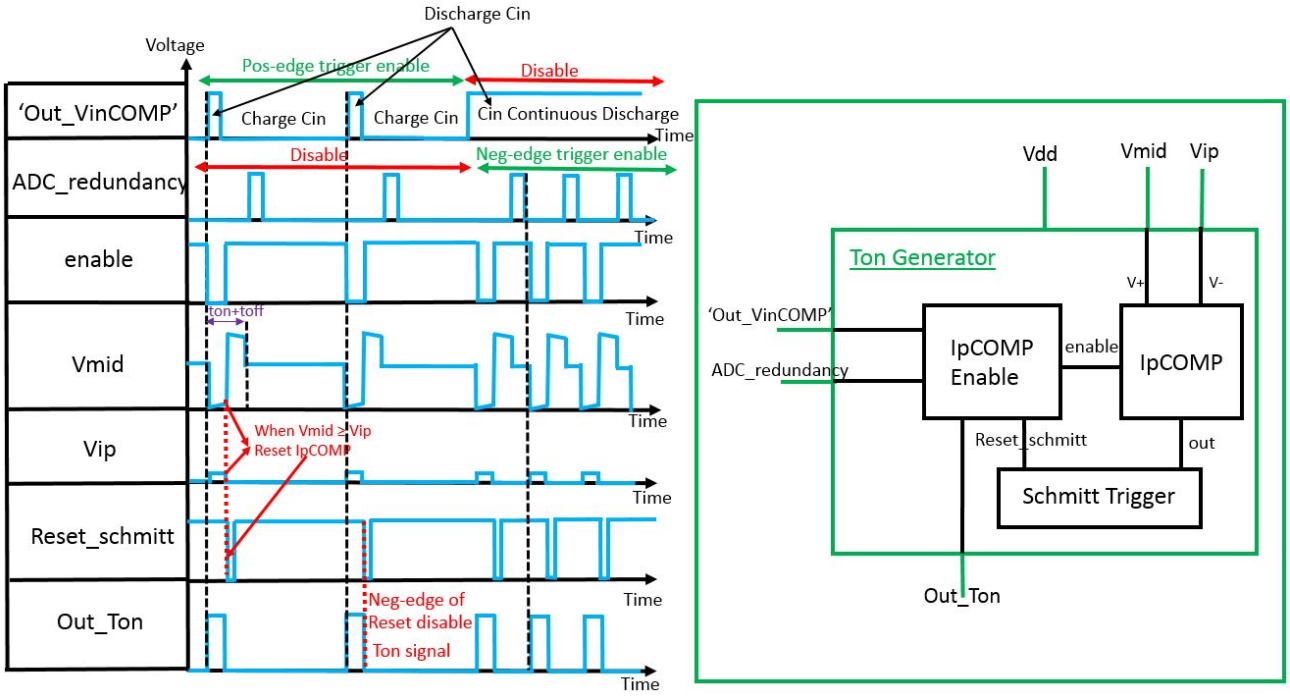

Figure 3-11: Ton-generator Block Composition

3-3-1 'IpCOMP Enable' block

There are three signal input terminals, two output terminals of this block and power terminal Vdd, Vss. The analog signal output from 'VinCOMP' and ADC redundancy bit are used to trigger the generation of Ton signal and also enable 'IpCOMP' comparator by D flip-flop. In addition, buffer is needed to communicate between digital output ($\bar{Q}$) and analog input (Enable). Ton signal will be ended upon '$ResetSmith$' reset the D flip flop.

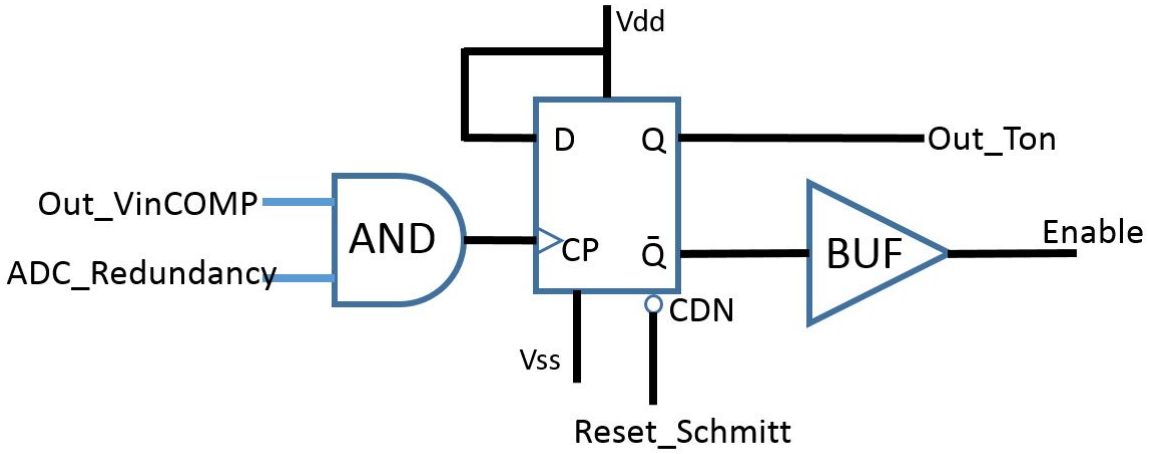

Figure 3-12: 'IpCOMP Enable' block

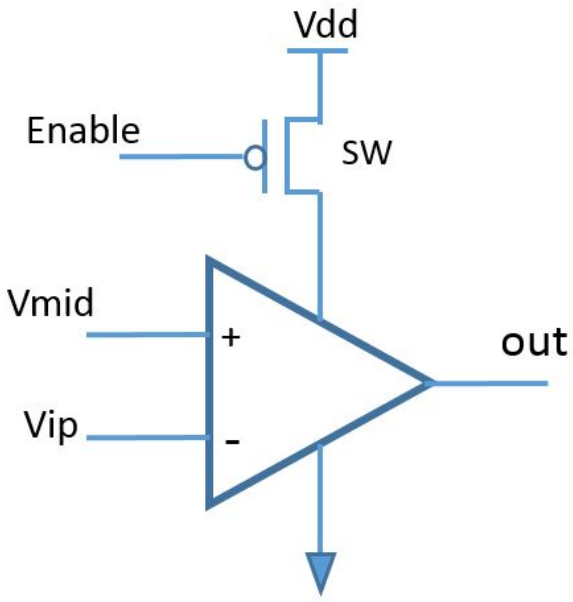

Figure 3-13: 'IpCOMP'block

3-3-2 'IpCOMP'block

Upton Ton signal is triggered, the 'IpCOMP' block is also enabled. The current IL would through inductor to NMOS switch and current would be linearly increasing referring to Figure 2-13. 'Vmid' representing the voltage value between inductor and SW1 would also increasing linearly from 0V. 'Vip' as the reference voltage stands for the maximum voltage limit for 'Vmid'. Representing by equation is $Vip \geq Vmid$ with $Vip = R_{nmosSW} \times IL_{peak}$. The output would change from 0 to 1V upon 'Vmid' is higher than 'Vip' and detected by 'Schmitt Trigger' connected.

3-3-3 'Schmitt Trigger' block

'Schmitt Trigger' block is used to convert analog signal 'out' to digital signal '*Resetschmitt*' by applying positive feedback. As shown in Figure 3-14, for an inverter input A with 1V Vdd supply, 0.5V would be the threshold voltage of this inverter. When A is higher than 0.5V, the output B would be low signal level. Then, the feedback would invert B low signal value and added to A. The loop would finally stable with A equals to 1V and B to 0V. As 'A' is lower than 0.5V, B would be 1V and A to be 0V. The buffers were added to provide diving capability for 'out' and 'B' terminals. '*Resetschmitt*' would be used to reset D flip flop for 'IpCOMP Enable' block.

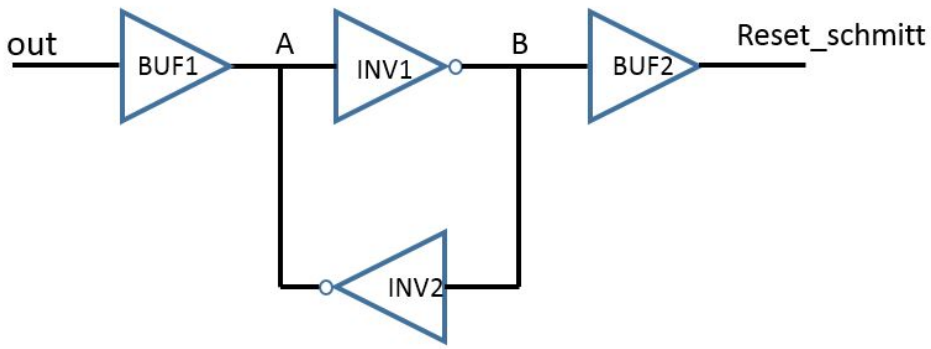

Figure 3-14: 'Schmitt Trigger' block

Buffer 1 should have a strong driving capability than Inverter 2. During 'SF' or 'FS' corner, there is possibility that buffer 1 with NMOS or PMOS is in slow corner and inverter 2 with PMOS or NMOS is in fast corner. If the input state is changing, then, buffer 1 and inverter 2 are pulling against from each other. However, inverter 2 fast PMOS driving capability is larger than buffer 1 slow NMOS driving capability. This would cause signal 'A' and signal 'B' cannot changing state according to signal 'out'. Therefore, buffer 1 should be designed big enough. Simulations among different corners especially 'SF' and 'FS' with temperature variation were done to guarantee buffer 1 has enough driving capability.

3-4 Toff-generator

The toff generator is triggered by the falling edge of Ton signal and then, Zero Current Detector Block would be enabled to compare 'Vmid' signal node with 'Vout' referring to Figure 2-15. The current I_L would flow from inductor through PMOS switch and voltage difference would exist between voltage node 'Vmid' and 'Vout'. Current I_L would decrease linearly with the time and also, 'Vmid'. Until 'Vmid' is lower than 'Vout', the output of ZCD block would reset 'ZCD Enable' block, disable ZCD block and Toff signal would switch off PMOS switch. In addition, DC voltage level for 'Vmid' and 'Vout' is from 1.5V and 2.5V. Therefore, for 'ZCD' and 'Schmitt Trigger' blocks the voltage supply is Vout.

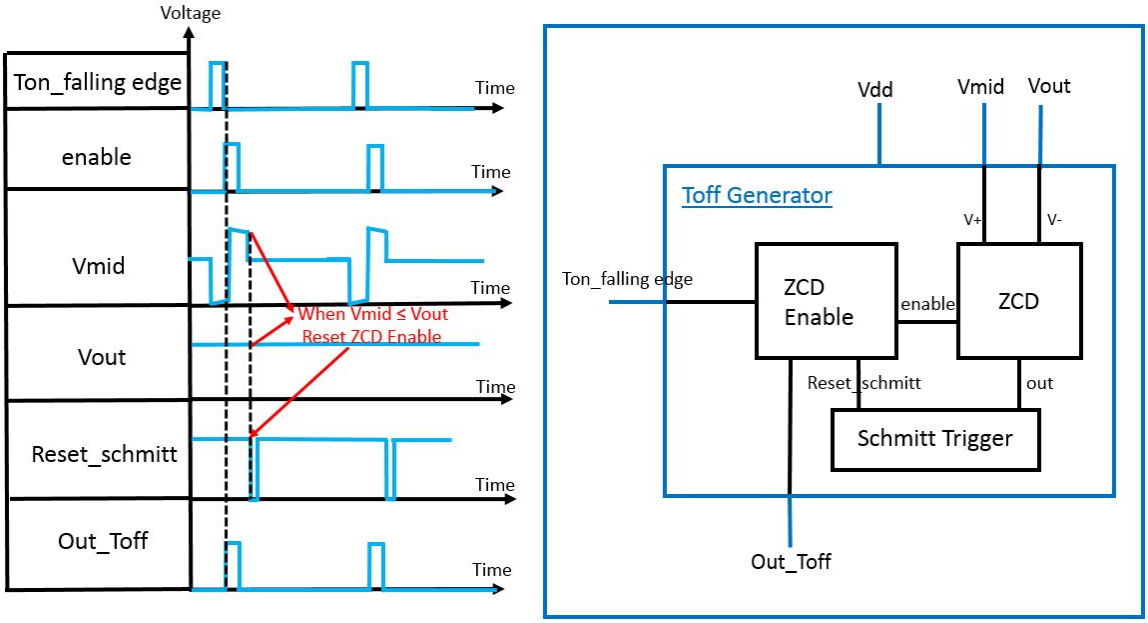

Figure 3-15: Toff-generator

3-4-1 'ZCD Enable' block

Ton signal would be inverted to clock the D flip flop and trigger Toff signal. Output signal from the $\bar{Q}$ would be level shifted to enable or disable 'ZCD' block. Conventional level shifter was implemented with stack technique to reduce leakage power consumption and tt can shift input voltage signal 'SigIn' from 1V to Vout.

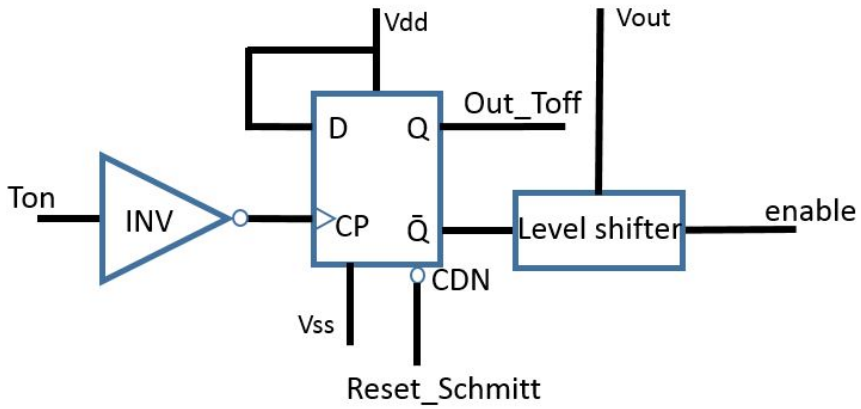

Figure 3-16: 'ZCD Enable' block

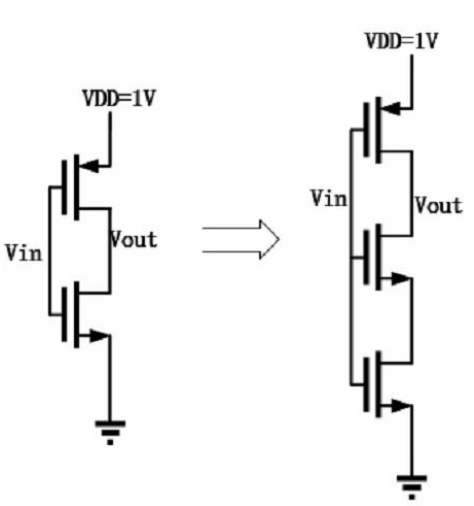

Figure 3-17: Inverter by applying Stacking technique

Figure 3-17 displays the inverter by using stacking technique. By Stacking two NMOS transistor in series, the equivalent turn off resistance of two NMOS transistors can be almost 4 times larger than single turn off resistance NMOS transistor. This is because of Drain-induced barrier lowering (DIBL) effect causing short channel between drain and source at single NMOS transistor due to high drain voltage. This effect would reduce the threshold voltage of NMOS transistor and NMOS transistor would work in weak inversion triode region. However, by series stacking, let upper NMOS transistor work in weak inversion triode region with low Vth and the below work in weak inversion saturation region with high Vth. DC leakage current of inverter can be reduced.

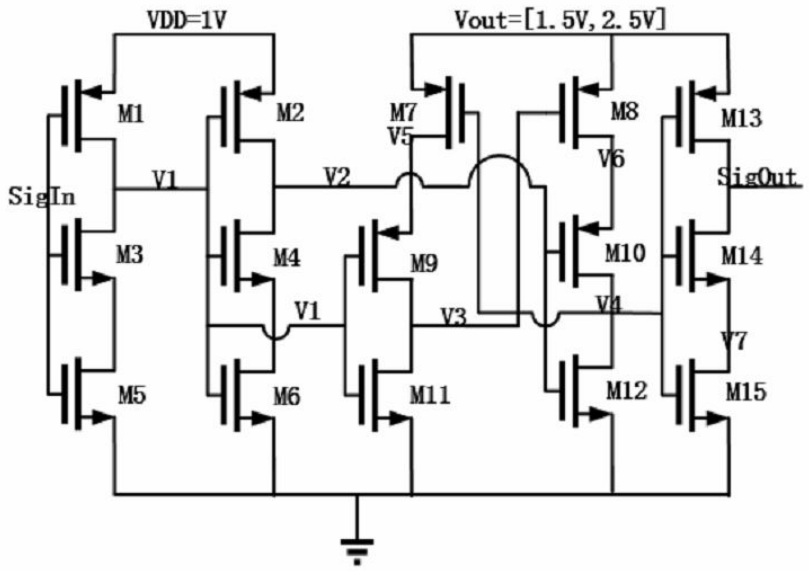

Figure 3-18: Level shifter with stacking technique

By applying stacking technique, level shifter schematic is shown in Figure 3-18. When input voltage 'SigIn' is equal to 1V, for V1 and V2, the voltage values are 0V and 1V correspondingly. $V2 = 1V$ would turn on transistor M12 causing V4 connecting to ground and further turn on PMOS transistor M7. $V5 = 1.5V$ and V1 would turn on transistor M9 causing $V3 = V5$. High voltage V3 would turn off M8 and V4 would stay at 0V. Finally, 'Sigout' would turn to be 1.5V. In this case, 1V is shifter to 1.5V. When 'SigIn' is equal to 0V, 'SigOut' would stay at 0V.

The performance is checked by doing the schematic simulation. The power consumption for Voltage Level shifter is equal to 700pW at 3kHz DC/DC working frequency and 53nW at 200kHz DC/DC working frequency. In addition, the simulation was done to check the delay between input signal 'SigIn' and 'SigOut' both in positive rising edge and negative falling edge. Besides, the temperature variation and 'SS' to 'FF' corners conditions are taken into consideration in the simulation. Toff Generator block utilise voltage level shifter to generate Toff signal and the delay of voltage level shifter would cause the delay of Toff signal which would influence the DC/DC circuit performance.

The big delay of Toff would result in a high voltage overshoot at node V_{mid}. As shown in Figure 2-14, when inductor is charged and MOSFET switches including SW1, SW2 are switched off, the inductor would discharge to the body diodes from SW1, SW2 and result in a large increased voltage in node of V_{mid}. This voltage would continuous with time and finally, shorten the switches lifetime or causes even worse the electrical breakdown result. Therefore, voltage level shifter input and output rising edge delay should be checked and minimised. Except for this, the falling edge delay of input and output should also be simulated. The large falling edge delay would lead to high power loss. During second phase when the inductor charges output capacitor through SW2, the decreasing voltage V_{mid} finally equals to V_{out} and SW2 is going to switch off. However, the big delay can not enable SW2 to immediately switch off. Then, the voltage V_{mid} would fall down below V_{out} resulting in the discharge of C_{out} to

inductor. The power loss caused by falling edge delay time $\Delta toff$ is analysed shown in Figure 3-19.

In Figure 3-19, the amount of charge ΔQ from C_{out} discharged to inductor is equal to the average discharge current times the delay time Δt_{off}. Then, the energy loss can be computed as the output voltage V_{out} times the loss charge from C_{out}. Divided the energy loss each pulse by pulse energy, the energy loss percentage or power loss percentage can be calculated. 10 percent t_{off} delay would result in 1 percent of power loss. According to system design in Chapter Two, t_{off} varies from 350ns to 600ns for full range DC/DC input power range. Then, 35ns falling edge delay would lead to 1 percent power loss.

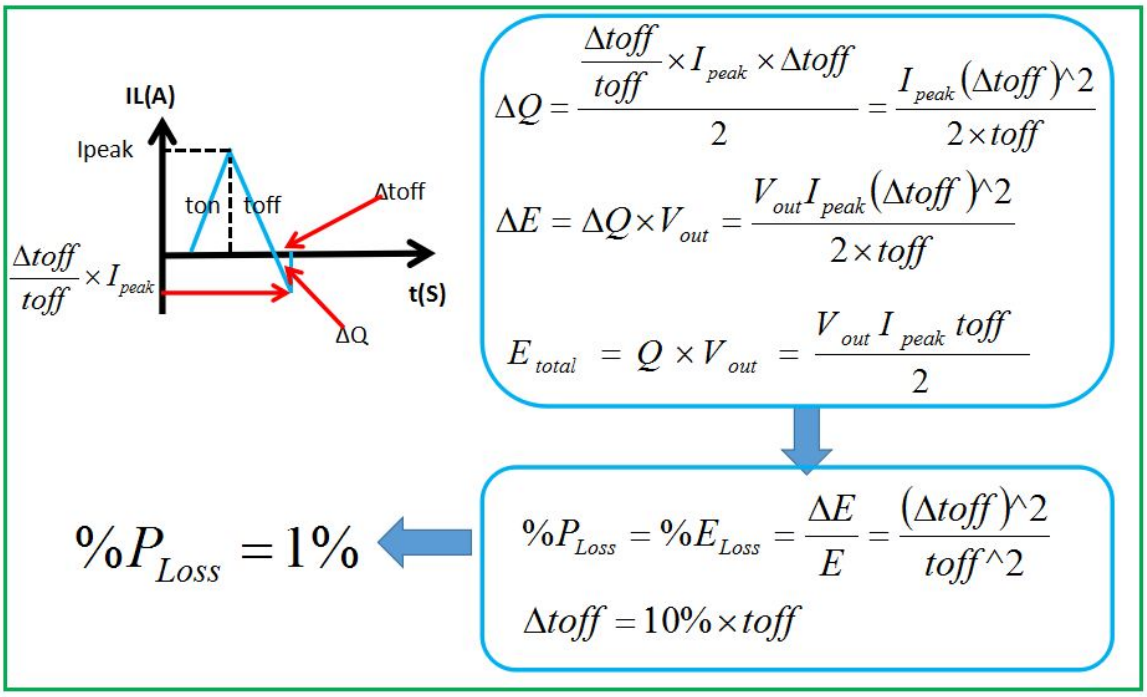

Figure 3-19: Power Loss Computation for delay of T_{off}

The simulation was done in Figure 3-20 to estimate the maximum input and output delay of voltage level shifter. Input voltage is shifted from 1V to 2V output voltage with delay. By simulating from 'SS' to 'FF' corners over [-40, 125] Celsius degree temperature variation, the minimum rising edge delay was 670ps and maximum rising delay 1.22ns occurs at 'SF' corner with 125 Celsius degree. The maximum falling edge delay 1.05ns was at 'SS' corner and minimum was 620ps.

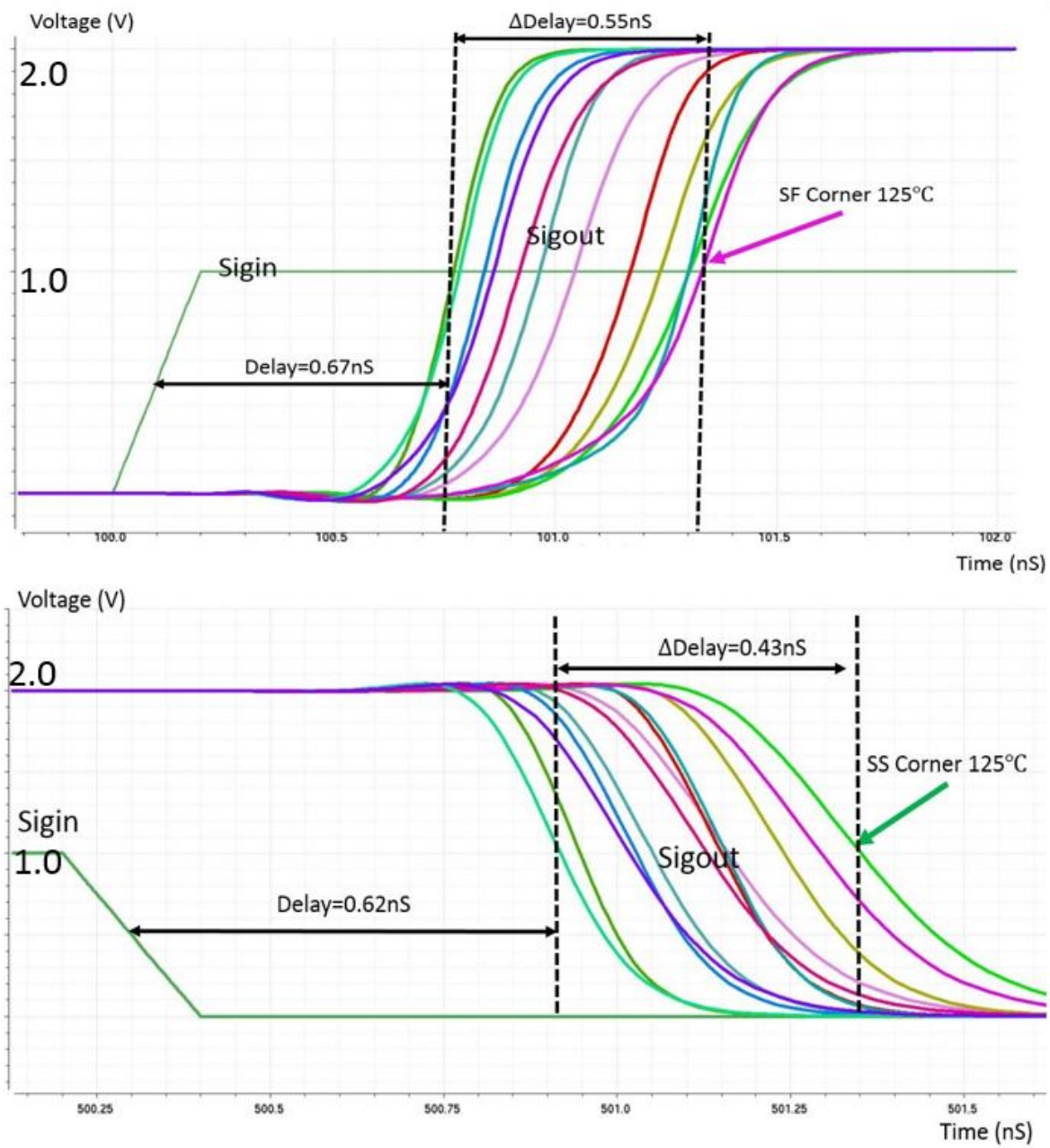

Figure 3-20: Voltage Level Shifter Input and Output Delay Check for 'SS' to 'FF' corners over [-40, 125] Celsius Degree

3-5 Capacitor Bank 9 bits DAC

DAC structure is shown in Figure 3-21. 9 capacitors are lined up in parallel with capacitance values from 0.6fF to $256 \times 0.6fF$. $C_{VinCOMP}$ is capacitor from differential pair transistor of block 'VinCOMP' These capacitors are charged by D flip flops with buffers connected in between. D flip flops are clocked by 'CLK' signal simultaneously with 9 bits digital inputs Q0 to Q8 from Digital part referring to Figure 2-24. After each digital to analog conversion, the charge on 9 capacitors and capacitor $C_{VinCOMP}$ are discharged through NMOS switch. In order to avoid latch up, a small resistor is added in series with switch. In this design, the 9 bits DAC was selected from 9 bits SAR ADC which is already pass the Monte Carlo simulation and capacitors spread evaluation.

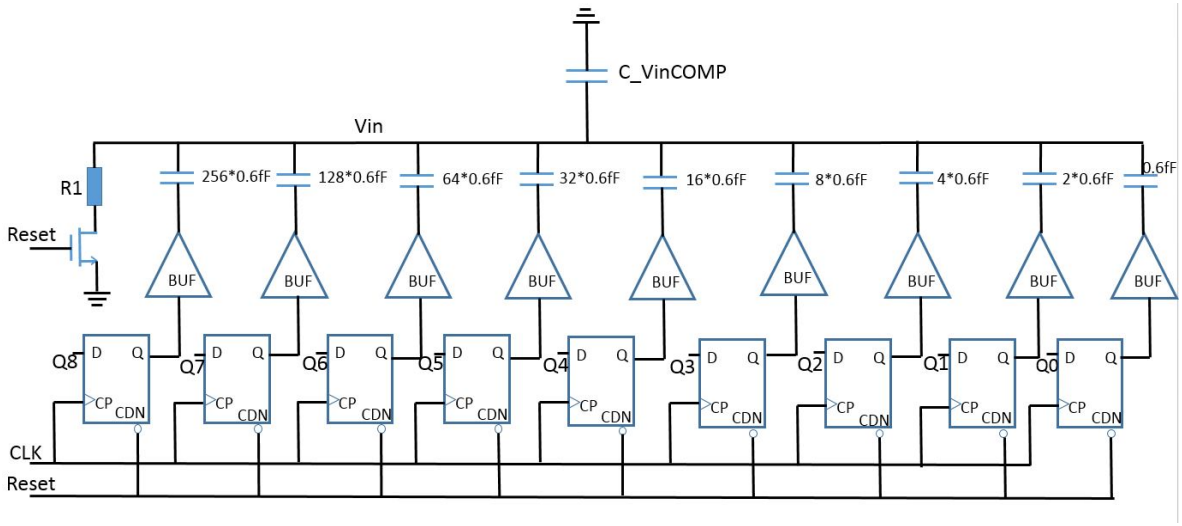

Figure 3-21: DAC circuit Implementation

The supply voltage of buffers and D flip flops is equal to 1V and DAC output range can vary from 0V to 1V. By applying charge conservation law, 0C charge exist at Vin after reset. When inputs Q0 to Q8 are applied to D flip flops, after D flip flops being clocked, Vin becomes $\frac{SUMC_{Q=1}}{C_{Total}} \times Vdd$. C_{Total} represents the sum of total capacitors including 9 DAC capacitors and $C_{VinCOMP}$. $SUMC_{Q=1}$ stands for sum of capacitors with input Q equals to 1V.

3-6 Switch Buffers and LDO

Multistage buffer technique is used to drive both NMOS and PMOS switches. In order to reduce the power consumption of multistage buffer, a control switch is added to constantly switch on or off to reduce power loss. The block diagram is shown in Figure 3-22. In order to drive a big NMOS switch (big capacitance) with ($\frac{W}{L} = \frac{320u}{40n}$), multistage buffers are applied with buffer 1 ($\frac{W}{L} = \frac{1u}{40n}$), buffer 2 ($\frac{W}{L} = \frac{10u}{40n}$), buffer 3 ($\frac{W}{L} = \frac{20u}{40n}$) and buffer 4 ($\frac{W}{L} = \frac{30u}{40n}$). In this condition, 'signin' can have enough driving capability to drive NMOS switch.

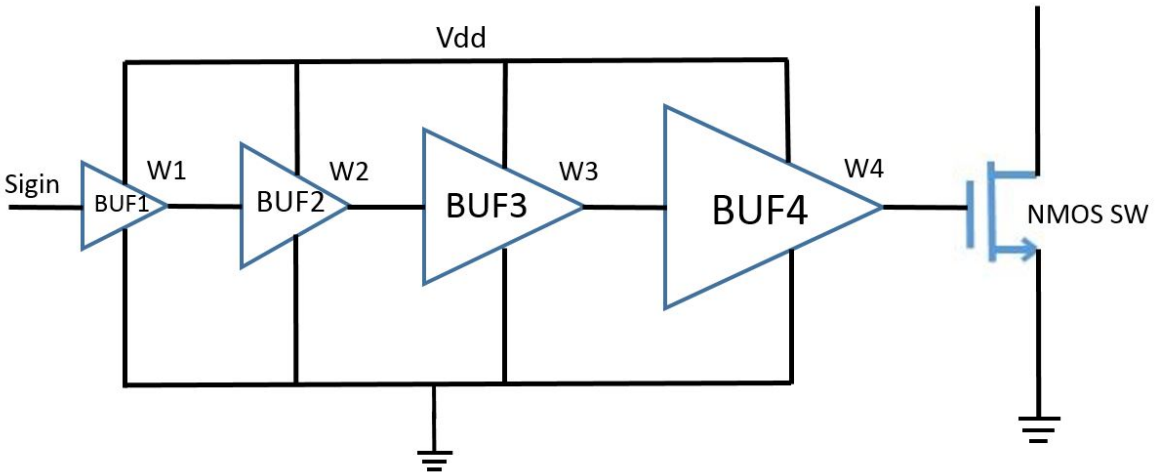

Figure 3-22: Switch Buffer block diagram

In terms of LDO block, the structure of LDO is shown in Figure 3-23. The reference voltage V_{ref} of LDO is given by Voltage Reference Generator which is equal to 700mV. The supply voltage Vout range is from 1.5V to 2.5V and Vdd is required to be 1.1V. Two big resistors R1 and R2 in series connected after switch M1 forms a negative feedback network together with opamp A1 which control switch resistance. The ratio of (R1+R2) to R2 is design to be 1.54 and Vdd is equal to 1.08V. Finally, R1 is designed to be 7Mohm and R2, 3.8Mohm to reduce the leakage current loss. In addition, to avoid voltage variation at Vdd, 1nF decoupling capacitor is connected to the output Vdd.

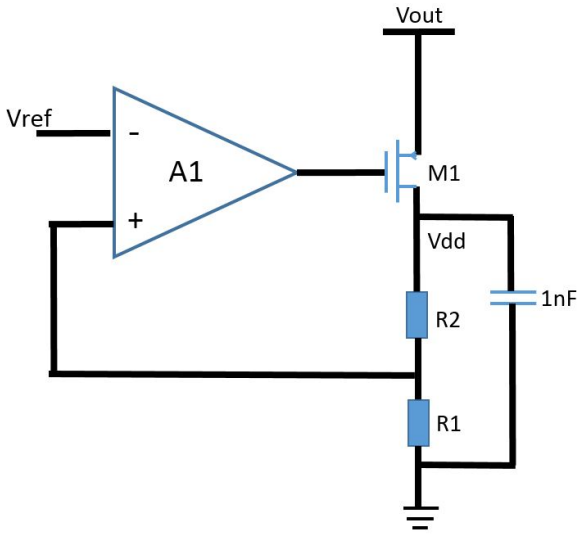

Figure 3-23: LDO block diagram

3-6-1 LDO Process, Voltage and Temperature (PVT) Simulations

LDO is simulated through all corners, supply voltage varying from 1.5V to 2.5V and temperature range [-40, 125] Celsius Degree. Figure 3-24 displays the LDO output voltage variation due to the variation of supply voltage from 1.5V to 2.5V, temperature at 25 Celsius Degree and Process in 'TT' corner. The maximum output voltage variation is simulated to be 9mV. By applying Equation (3-4), PSRR is computed to be 40.92dB which is suitable to be the supply of SAR ADC and digital part supply. In addition, all the corners with varied voltage and temperature are simulated for LDO shown in Figure 3-25. 'SS', 'SF', 'FF' and 'FS' corners at 125 Celsius Degree would result in a large output voltage variation up to 120mV. In other PVT conditions, the variation of output decreases to 23mV.

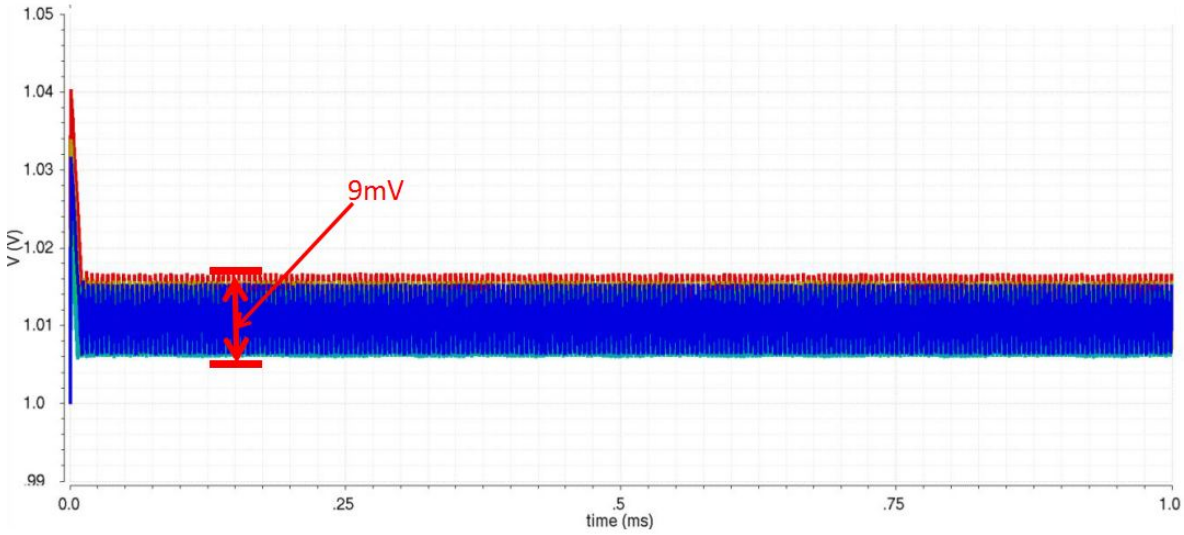

Figure 3-24: LDO Process[TT corner], Voltage Supply[1.5, 2.5]V, Temperature[25]Celsius Degree Simulation

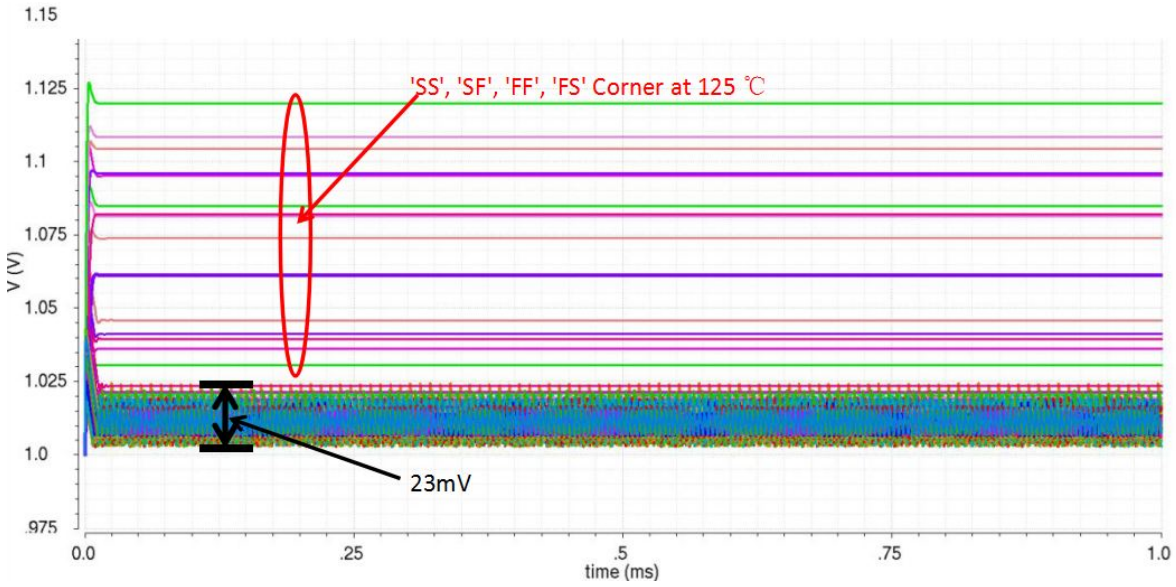

Figure 3-25: LDO Process[TT, SS, SF, FS, FF corners], Voltage Supply[1.5, 2.5]V, Temperature[-40, 125]Celsius Degree Simulation

Chapter 4

Harvest Interface System Layout and Simulation results

Figure 4-1 gives the test bench schematic of DC/DC boost converter. The input of DC/DC boost converter is an ideal power source to model MOS non-linear rectifier. This is because the simulation of rectifier is in high frequency domain and DC/DC boost converter is in low frequency. Combining them together to do the simulation would cause extreme slow simulation speed. 1mW and 8uW ideal power source with P_{out} versus V_{in} are shown in Figure 4-3 and Figure 4-4.

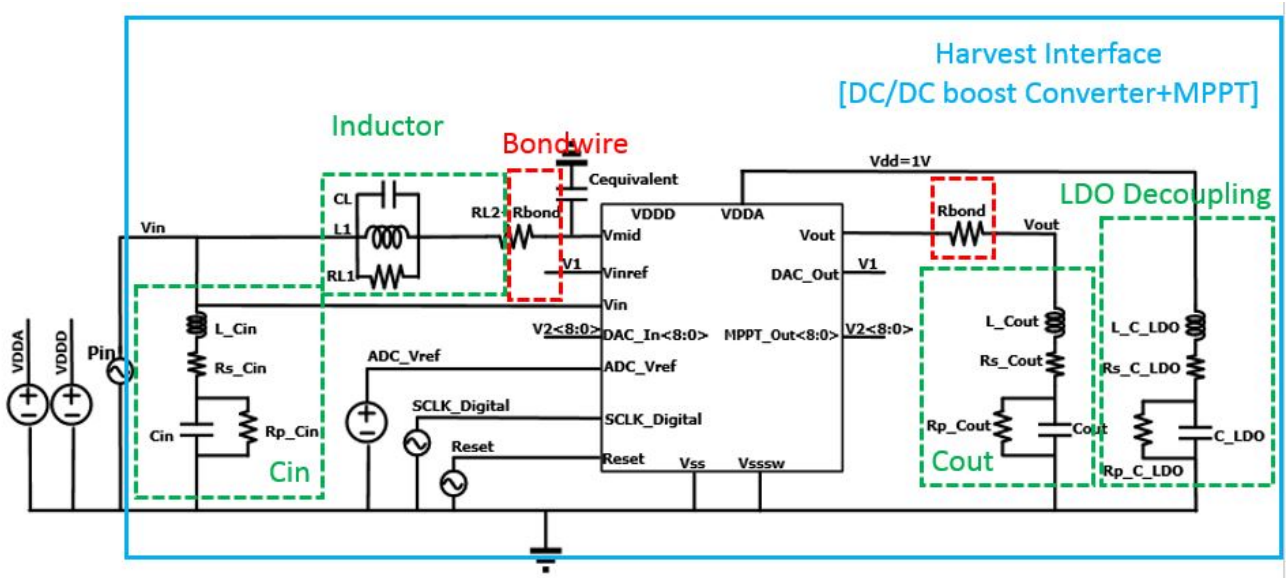

Figure 4-1: The schematic of Test Bench

Ideal power source is connected to the input capacitor C_{in} with series number "GRM32MB11H434JA01" from Murata Company and Inductor with series number "VLCF4028T-220MR72-2". In addi-

tion, power source also connect to V_{in} terminal of chip to detect V_{in}. The inductor is connect V_{mid} through the bondwire which has equivalent series resistance. At V_{mid}, there is an equivalent capacitance connected to ground. This equivalent capacitance includes the capacitance of bond pad, ESD protection and body diode of switches. A stable reference voltage needs to connect to ADC negative terminal, Digital MPPT needs a slow clock (SCLK) referring to Figure 2-29 and reset is needed to ADC and MPPT Digital part. At the output terminal, storage element C_{out} is connected to store energy coming from V_{out} with series number 'C1608X5R0G156M080AA' from TDK Company. According to Figure 2-24, DAC output (DAC_Out) is connected to V_{inref} and output of MPPT ($MPPT\_Out < 8:0 >$) should be connected to DAC input ($DAC\_In < 8:0 >$). Two terminals 'VDDD' and 'VDDA' means the voltage supplies to digital part and analog part. Stable DC voltage sources can be connected to 'VDDD' and 'VDDA' terminals to check simulation of Analog Part only or Digital Part only. In addition, LDO inside the chip is connected to 'VDDA' and 1nF LDO decoupling capacitor is added with series number 'CGJ2B2X7R1C102K050BA' from TDK Company.

4-1 System Simulation

4-1-1 [DC/DC(Schematic)+Digital MPPT (RTL)+ADC+DAC] Simulation

Total system simulation was done to check the power track and detection accuracy. This simulation is combined of DC/DC Boost converter schematic, RTL code for digital part and schematic of ADC and DAC in order for a fast simulation speed. For Figure 4-2, the simulation takes up almost one week and it is will be a very long time by applying layout to do total system simulation.

Figure 4-2 displays the DC/DC boost converter maximum power tracking accuracy capability by connecting two ideal input power sources: 1mW and 8uW input power sources. Increasing V_{in} by ΔVin, power difference can be detected due to ΔVin. These two power sources are shown in Figure 4-3 and Figure 4-4 with output power P_{out} versus input voltage of Load(DC/DC converter) relationship plotted. In Figure 4-2, for 1mW input power source, DC/DC boost converter would track the input power starting at V_{in} equals 430mV and gradually climb the V_{in}. At last, V_{in} would converge at 0.72V with voltage variation from 0.68V to 0.77V. Referring to Figure 4-3, the tracking accuracy can be checked. With the average of V_{in}=0.72V, for 1mV input power source, only 7.5 percent of power would lost due to the inaccurate power tracking.

The inaccuracy tracking is mainly due to the upper voltage limit of 9bits SAR ADC. For 1mW input power, the voltage on RC integrator (Refer to Figure 2-26) reaches the upper limit of 9bits SAR ADC. Meanwhile, ADC clips against its upper limit and pulse detection would not be accurate enough. For input power source equals to 8uW, DC/DC boost converter can track V_{in} at 0.52V with voltage variation from 0.48V to 0.55V. Referring to Figure 4-4, for V_{in} equals to 0.52V, the tracking accuracy is equal to 99 percent with only 1 percent tracking inaccuracy power loss.

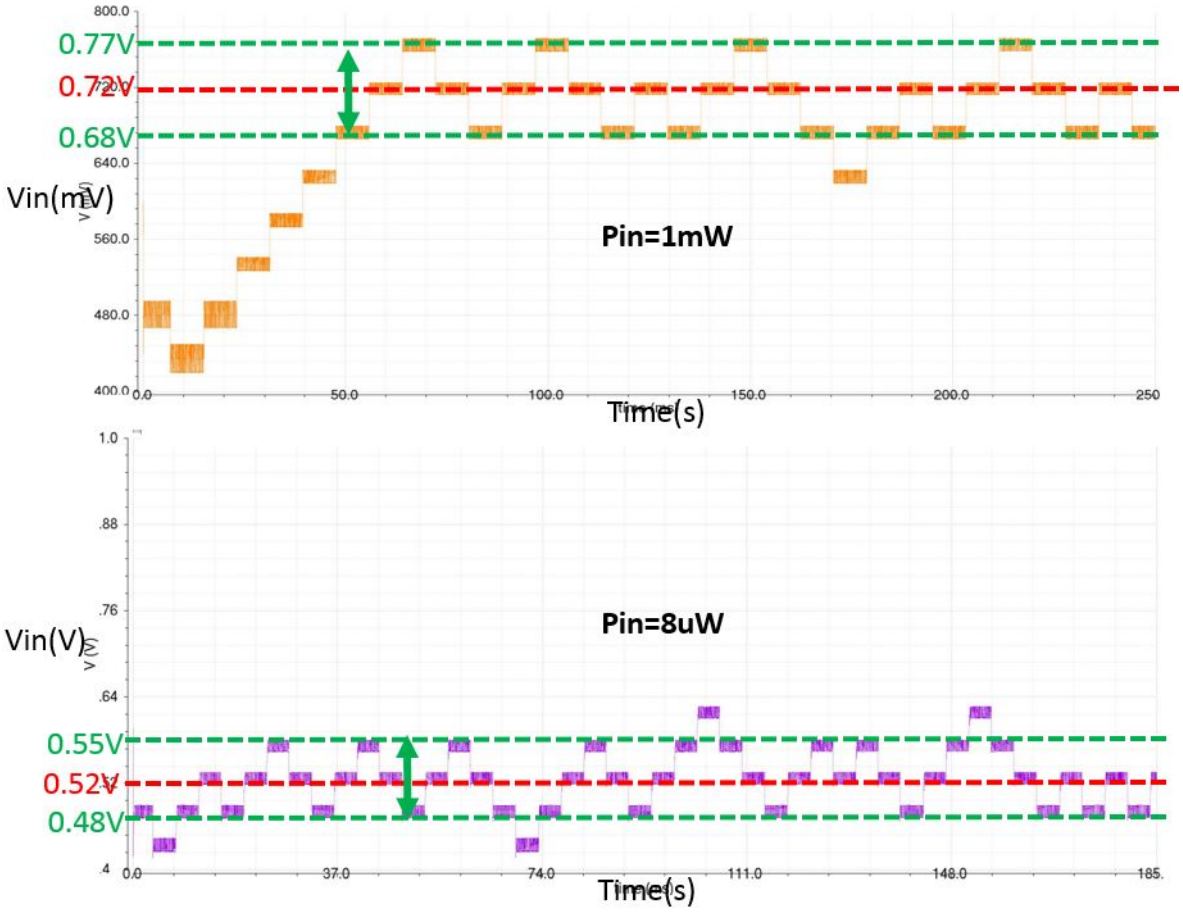

Figure 4-2: Maximum Power Point Tracking of DC/DC boost converter for Pin=1mW and Pin=8uW

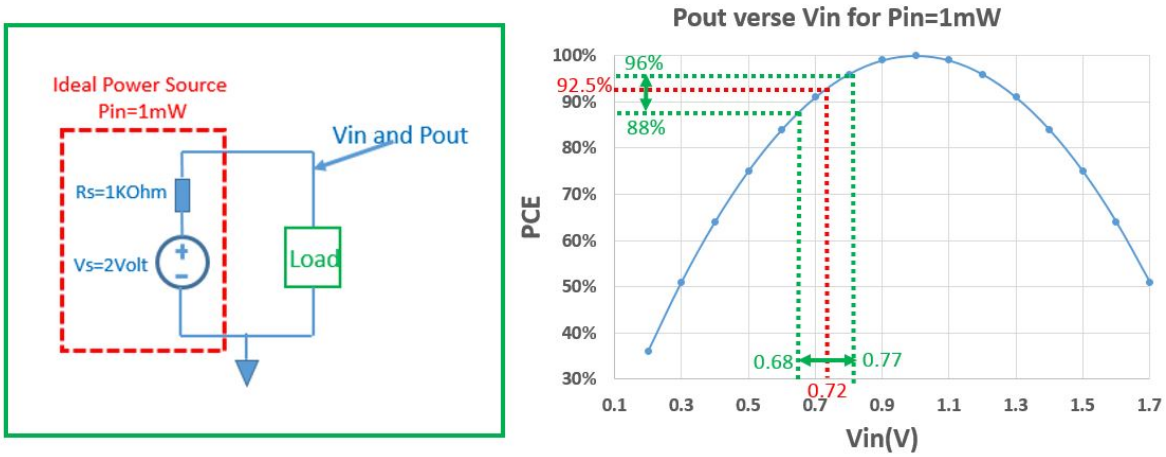

Figure 4-3: 1mW Ideal power source Output Power versus Voltage

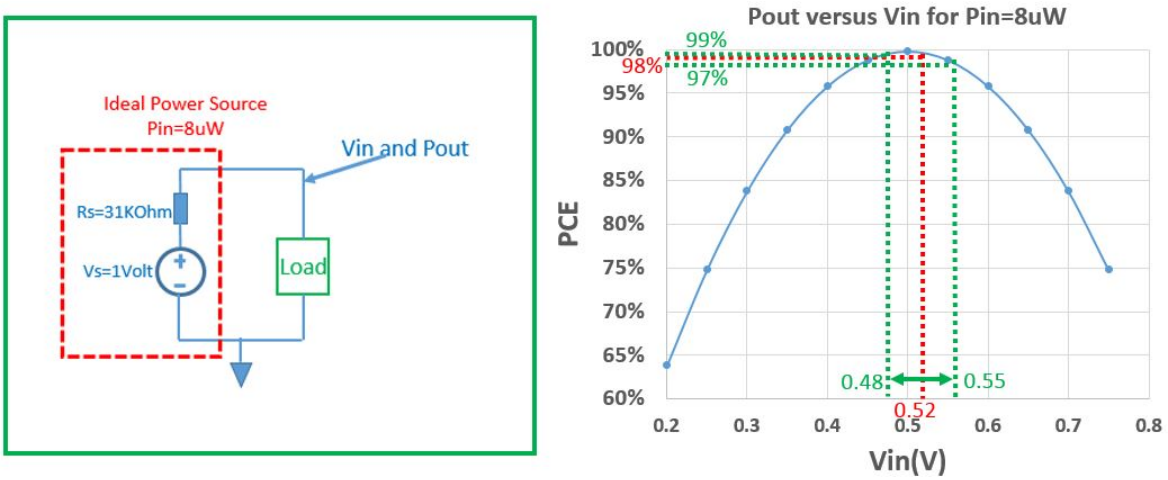

Figure 4-4: 8uW Ideal power source Output Power versus Voltage

Figure 4-5 and Figure 4-6 give simulated power loss distribution for P_{in} equals to 8uW and 1mW. For 8uW power input, the significant power loss (19 percent) come from the DC/DC converter switches, inductor and Bond wire. LDO power loss takes up 18 percent of total power loss. Other blocks power losses are almost evenly distributed. However, for 1mW input, power loss resulting from switches, inductor and Bond wire occupy the most significant part which is 82 percent of total power loss. Based on Equation (2-18), the energy dissipation for transmitting one pulse energy which is on the numerator of Equation (2-18) is almost the same for both Pin=8uW and Pin=1mW. However, the T_{period} for Pin=8uW condition is 60 times larger than T_{period} of Pin=1mW condition which causes the power loss 60 times higher at Pin=1mW condition than Pin=8uW.

The total power loss could be divided into two types which are dynamic power loss and static power loss. As shown in Figure 4-5, LDO, Bias, VRG and VinComp blocks' power loss belong to static power loss due to working continuously. Other blocks' loss is dynamic power loss with different duty cycles in one working period. Decreasing or increasing working period by times would increase or decrease blocks' power loss by time. For 8uW input power condition, the working period is 60 times of the working period of 1mW input power condition resulting in no changed static power loss but 60 times larger dynamic power loss. Due to Switches, inductor and Bond wire power loss is the most significant dynamic power loss at 8uW condition. Therefore, for 1mW input power condition, this loss would be 60 times larger and will be significantly among all types of power loss. In addition, the leakage power loss of dynamic working blocks will not be influenced by the changing working period.

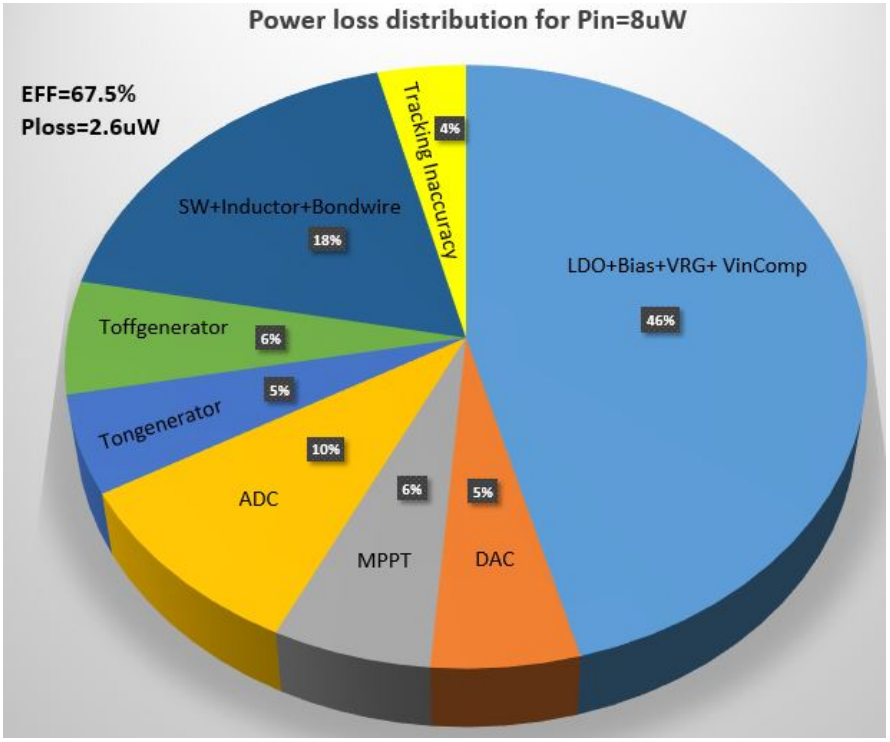

Figure 4-5: The Whole System schematic simulation for Pin=8uW

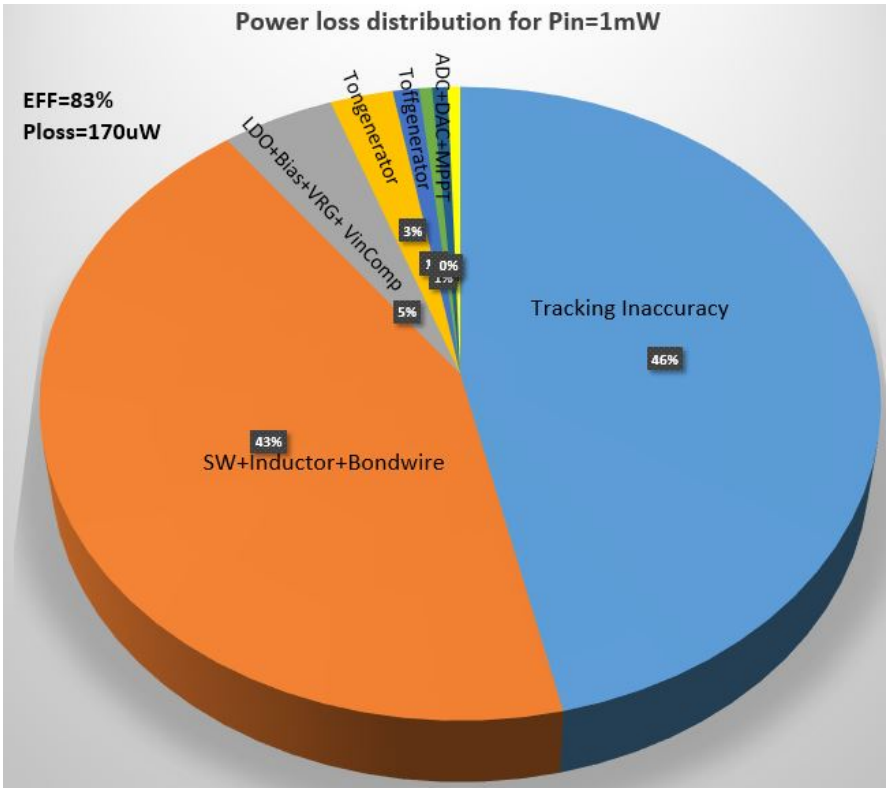

Figure 4-6: The Whole System schematic simulation for Pin=1mW

Figure 4-3 and Figure 4-4, the Harvest Interface can detect ideal power source with 92.5 percent power detection accuracy for Pin=1mW and 98 percent power detection accuracy for Pin=8uW which is could also applied to rectifier to be the input power source. When an ideal power source is replaced with the rectifier, the detection accuracy in two input power conditions are plotted in Figure 4-7. In order to avoid the long time system simulation [rectifier + Harvest Interface], a single rectifier simulation with PCE versus Vin [output of rectifier or input of DC/DC] at Pin=8uW and Pin=1mW are simulated and plotted in Figure 4-7 by my group partner i.r. Jialue Wang. Then, referring to ideal power source simulation results with optimum V_{in} at 0.72V for 92.5 percent detection accuracy and at 0.52V for 98 percent accuracy, we can get 0.77V for 92.5 percent detection accuracy and 0.52V for 98 percent accuracy for the rectifier.

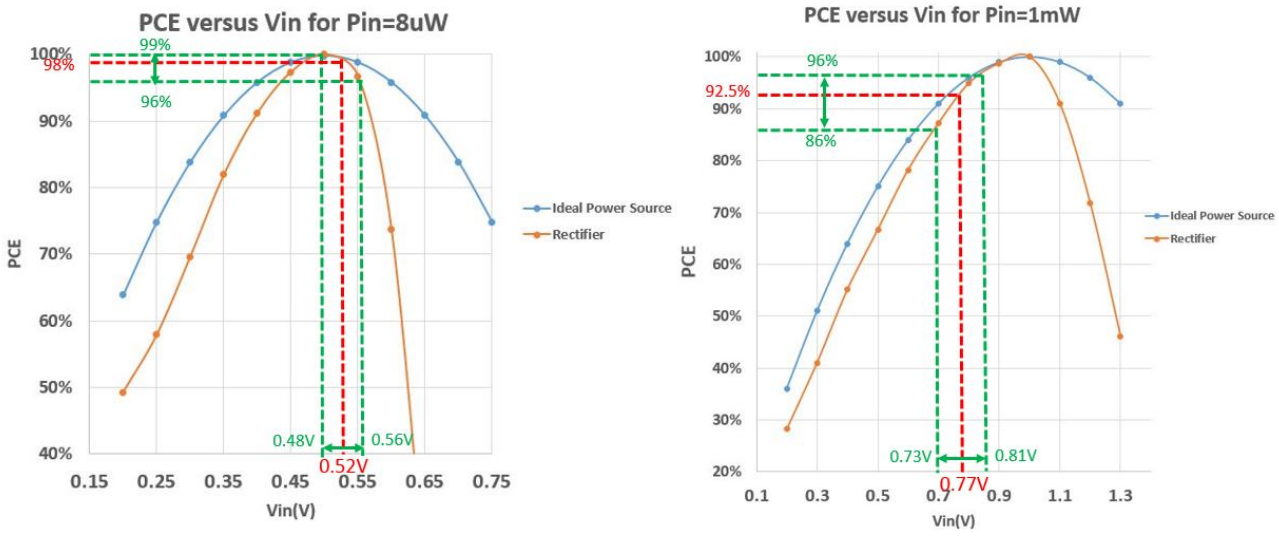

Figure 4-7: PCE versus Vin: Ideal power source and Rectifier Comparasion

4-1-2 DC/DC post Layout [Without MPPT+ADC+DAC] Simulation

Referring to Figure 2-24, the total system is combined of Analog system and digital system. In this subsection, the simulation was done to verify the performance of analog system layout. The simulation includes the DC/DC boost converter input voltage, output voltage, inductor current and power dissipation of analog system.

Figure 4-7 gives the input, output voltage simulation curve of DC/DC boost converter layout RC extraction with input power equals to 1mW. During ton, C_{in} would charge inductor with V_{in} decrease and inductor current increases to I_{peak} and decreases during toff with C_{in} continuously discharge. After t_{off}, there is a small current ringing at the inductor. This is because energy in this inductor is not fully discharge to C_{out} after t_{off} is finished. The inductor would charge and discharge through the equivalent capacitance on V_{mid} node cause ringing. The equivalent capacitance is composed of capacitance from bond pad, ESD protection and body diode of two MOS switches. In addition, the overshoot voltage is equal to 2.4V. As shown in Figure 2-11, when SW1 is switching off and SW2 is not switching on immediately, fully charged inductor would charge the equivalent capacitance on V_{mid} when both MOS SW1 and SW2 are turned off. This would cause a sharp increasing voltage overshoot. During t_{dead}, rectifier would charge V_{in} until V_{in} reaches V_{ref}. Figure 4-8 displays the complete charging graph of V_{in} charge V_{out}. The input voltage is regulated at 1V for P_{in} equals 1mW. The maximum inductor current is equal to 19mA and inductor will charge itself from V_{in} and discharge to V_{out}. V_{out} would store the energy from inductor and voltage level increases from 1.5V to 1.51V.

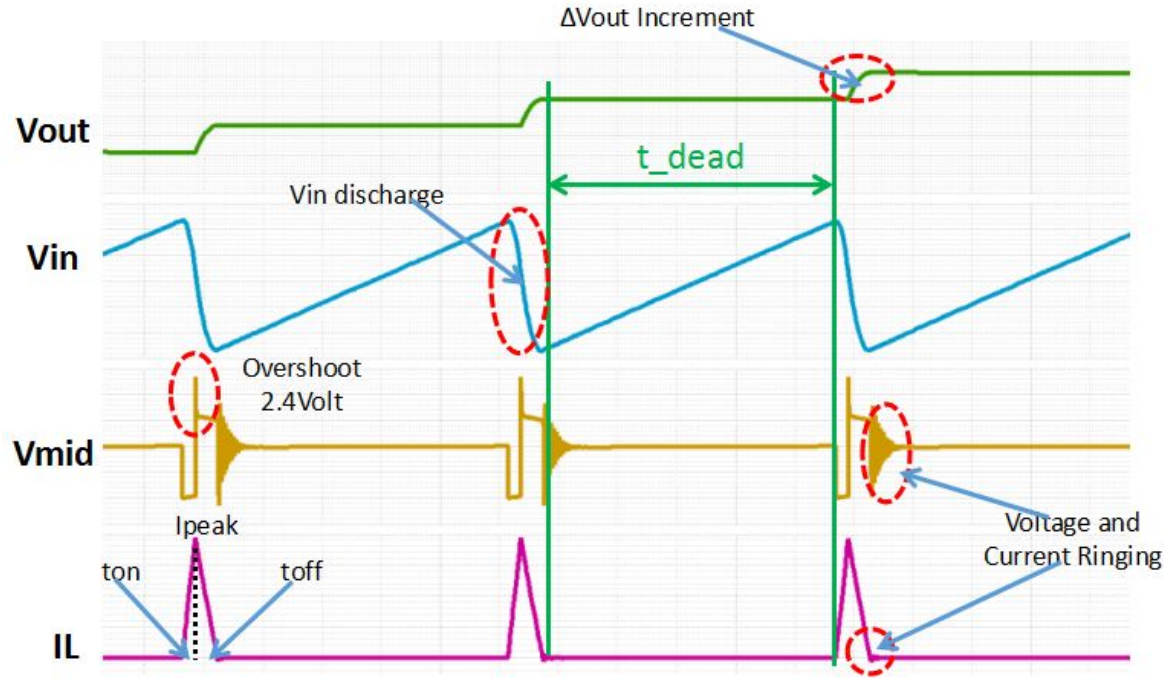

Figure 4-8: DC/DC Post Layout: Vin, Vout, IL simulation results for Pin=1mW (1)

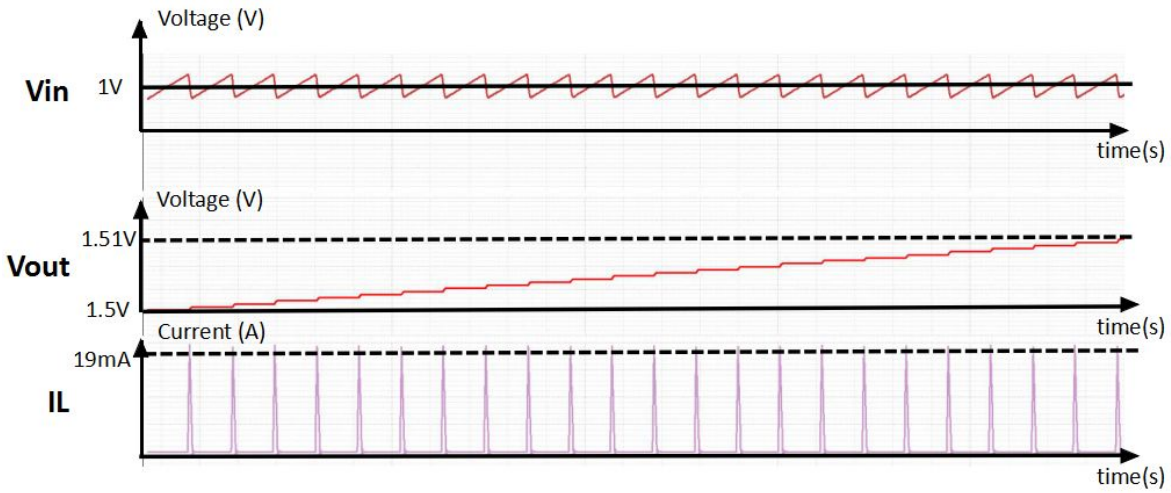

Figure 4-9: DC/DC Post Layout: Vin, Vout, IL simulation results for Pin=1mW (2)

The post layout simulations of DC/DC converter [without MPPT, ADC and DAC] were displayed in Figure 4-9 and Figure 4-10 above.Comparing with simulation results shown in Figure 4-5 and Figure 4-6, Deduct the ADC, DAC Tracking and MPPT power loss in Figure 4-5 from total power loss and we can get power loss of DC/DC converter schematic equalling to 2uW which is closed to layout simulation result 2.42uW. By deducting the ADC, DAC tracking and MPPT power loss in Figure 4-6, DC/DC converter power loss schematic is computed to be 86.7uW which is smaller than Layout simulation 110uW. This is due to equivalent parasitic capacitance at node V_{mid} and also layout wire series resistance which connect SW1, SW2, inductor and C_{out}.

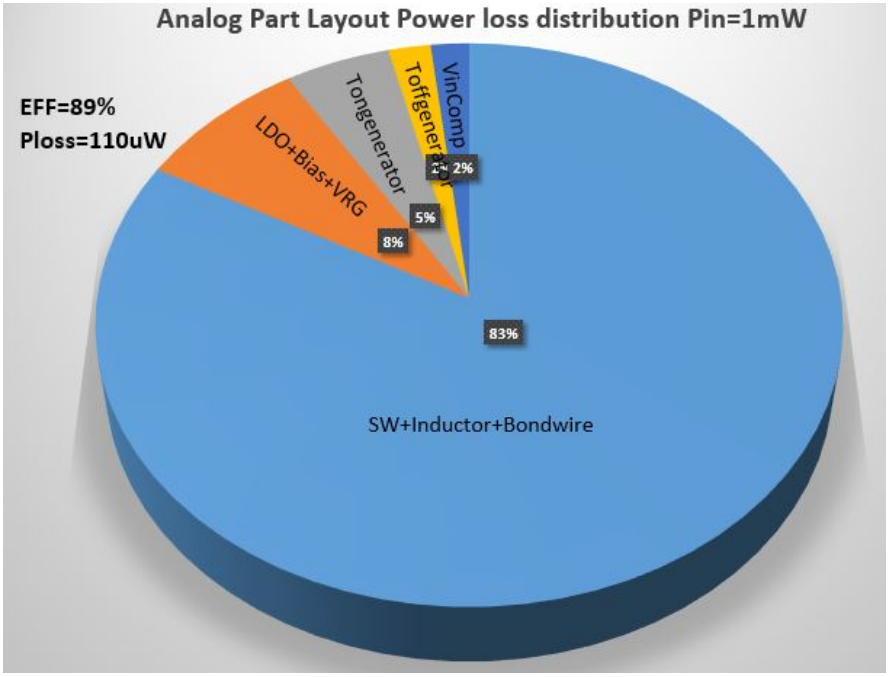

Figure 4-10: The power loss distribution for DC/DC Layout and Pin=1mW

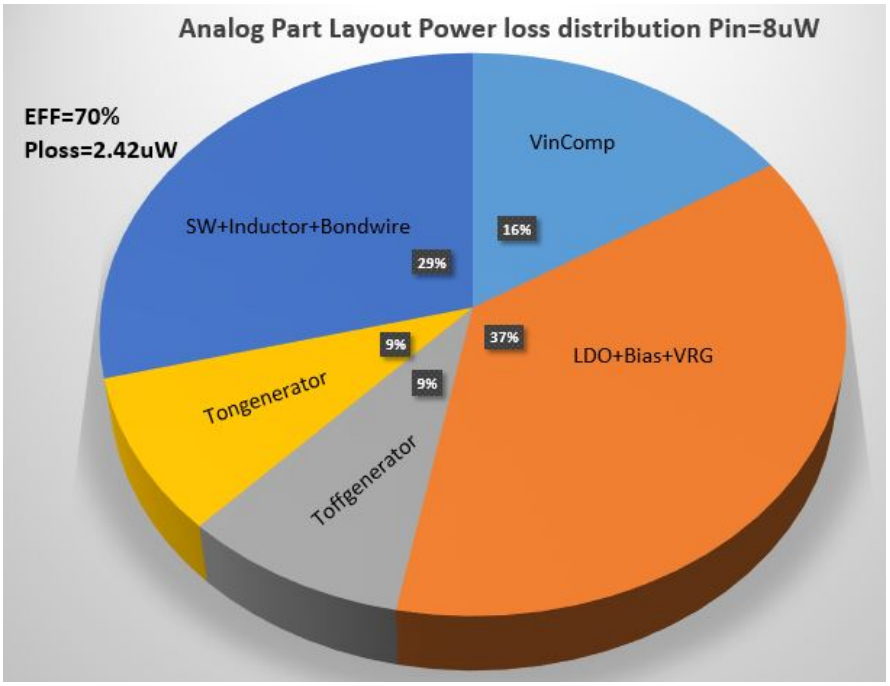

Figure 4-11: The power loss distribution for DC/DC Layout and Pin=8uW

4-2 Harvest Interface Layout

The design area of Harvest Interface DC/DC boost converter without bond pads on this chip is equal to 450um times 400um with silicon area in TSMC 40nm equalling to 0.15 mm^2. With bond pads, the silicon area increases to 0.55 mm^2. The 9 bits ADC take up almost 50 percent of the design area in total DC/DC boost converter layout. The big resistors in LDO and VRG block design also take up a large amount of area. This layout can still be optimised for the space.

There is one comparator missing on this chip which should be connected to capacitor C_{out}. This is because C_{out} cannot be charged for infinite voltage level and 2.5V is the maximum voltage for C_{out}. Therefore, this comparator is used to detect maximum 2.5V at C_{out}. Due to the time constraints of this design, I did not put this comparator on chip. Instead, for PCB design, an discrete comparator could be added on PCB to realize C_{out} discharge function. The future work can put this comparator designed on chip and an estimated 10um$\times$ 10um area comparator layout could be added directly to DC/DC converter layout shown in Figure 4-11 without affecting DC/DC converter total area.

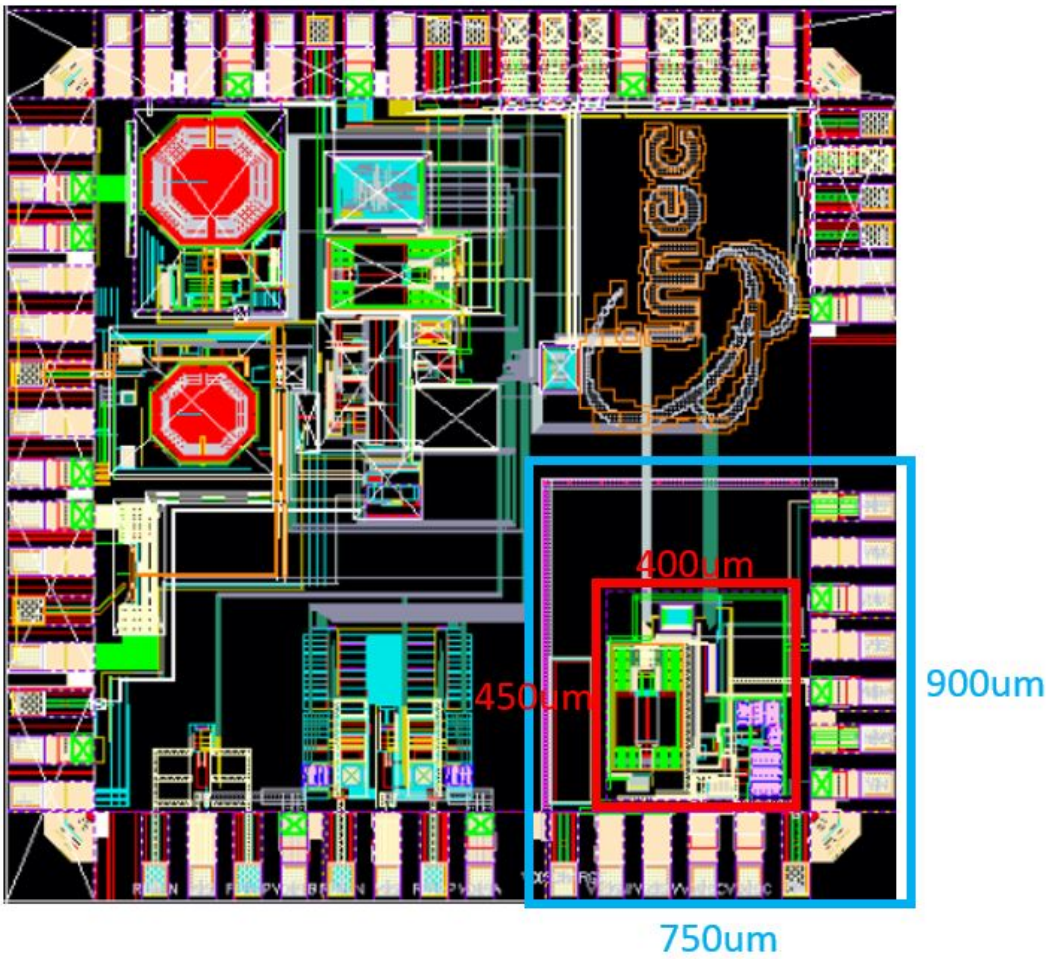

Figure 4-12: Layout of Harvest Interface

Chapter 5

Conclusion

5-1 Summary

This thesis gives the design of the Power Management Block which is suitable for Wireless Energy Harvesting system application. The final power management block would be composed of 'Harvest Interface' block and 'Load Regulation' block as shown in Figure 2-1. My Design is focus on Harvest Interface design. For 8uW minimum input power of power management system, a power dissipation estimation was done among Harvest Interface topologies and after comparing the power dissipation, DC/DC boost converter was chosen to be the topology in this design. In order to match with the rectifier output power conditions, DC/DC boost converter should aim to regulate the input voltage of DC/DC boost converter and leave the output to charge the storage element to a high voltage from a low voltage level to store enough energy. Then, low power switches control circuit was designed to regulate input voltage. Next, RC integrator together with ADC and digital Maximum Power Point Tracking [MPPT] Algorithm design becomes a power detector which detect output power from rectifier, digitalize by ADC and compare it with previous cycle output power by digital MPPT. DAC would then translate output from digital MPPT to analog input voltage reference for DC/DC boost converter in Harvest Interface. DC/DC boost converter would then regulate input voltage based on input voltage reference from DAC. In order to reduce power dissipation in this system, based on working duty cycle of different blocks, power saving switches are added between supply voltage and blocks to save power. Big resistor was added into resistive feedback of an analog LDO to reduce leakage power loss and also, the stacking inverter technique was applied to Voltage Level Shifter.

The schematic design has been implemented to DC/DC boost converter analog part and RTL coding for MPPT digital part in TSMC 40nm. The simulation was done to verified power detection performance for varying input power. Finally, the analog layout and RTL coding back-end have been done with post-layout RC extraction to check power dissipation of the system.

5-2 Thesis Contributions

* A complete design flow of DC/DC Power Management from schematic to layout.

This project begins from the research of the energy harvester system. As shown on Figure 5-1, the energy harvester system is combined of high frequency front end and low frequency power management part. In the power management block system, the system topology has been determined to be two stages including Harvest interface stage and load regulation stage based on front-end input voltage, current conditions and the load output condition. This design would focus on Harvest Interface Block design and by estimating power dissipation of Harvest interface system topologies, the final system topology has been determined. Then, comes to schematic level implementation and the final layout design. Simulations were done to check with schematic and layout design.

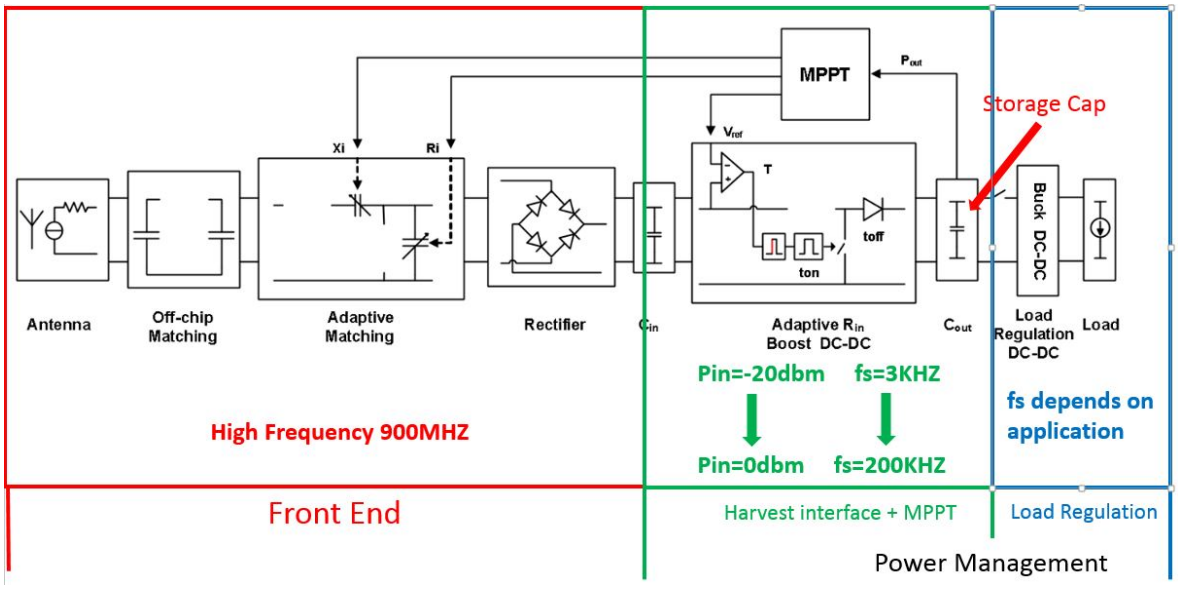

Figure 5-1: RF Energy Harvester System Architecture

*Power Management System level research and Design

The power management system level research begin with the input both voltage and current and load output power and voltage. Then, power management system should be designed two stages. Then, focus on Harvest Interface block system level design. (1). In order to determined the Harvest Interface block structure, power dissipation has been done to evaluate DC/DC converter structures and inductive DC/DC boost converter was applied. (2). DC/DC boost converter switches control circuitry was designed to regulate input voltage by comparing with input voltage reference V_{ref}. (3). Switches Control circuitry blocks are designed to be low power and duty cycle control to reduce the power dissipation. A rough power estimation of switches control blocks was made to help with schematic and layout design.

*Power Detection and Tracking Design

Based on power formulas and input voltage, current data sheet from MOS rectifier, the model has been built on both matlab and Excel to evaluate power detection and tracking methods. After comparing power detection accuracy and circuit implementation, RC integrator together with Digital MPPT were proposed to be the final topology. Meanwhile, the existing low power 9 bits SAR ADC and 9 bits DAC in TSMC 40nm were applied before and after Digital MPPT block. Power dissipation has been estimated before the schmatic design. In addition, as shown in Figure 5-1, the digital MPPT block would also help with the tuning of adaptive matching between antenna and rectifier in front end part to improve PCE of energy harvester system.

*Storage Elements Research

Storage element is also an important part in Harvest Interface block considering power dissipation. The final storage element is determined to be 14uF size Multilayer Ceramic Capacitor with X5R/X7R dielectric type after considering minimum DC power loss, size and cost. In Chapter two, numbers of Storage Elements in the market have been researched including ceramic cap, film cap, Metalized cap, Al electrolytic cap, Tantalum electrolytic cap and double layer super-cap. Then, capacitor characteristics containing DC power loss, AC power loss, capacitance voltage and temperature dependence have been researched. DC power loss was found to be the dominant power dissipation with its value increases with capacitance. Finally, the maximum voltage on storage element was determined to be 2.5V with 850nW DC power loss.

*Analog Blocks and the Digital Block Schematic, Layout Design and Simulation.

The low power analog blocks designed in both schematic and layout of this project includes LDO, Voltage Reference Generator (VRG), Zero Current Detector (ZCD), Voltage Level Shifter, Comparators, Energy Pulse Detector, Signal Generator, Schmitt Trigger and Buffers for DC/DC converter switches. Simulations have been done for these analog blocks' schematic and RC extraction Layout. For the system schematic simulation of DC/DC converter [without MPPT, ADC, DAC blocks], the DC/DC converter can function in 'FF', 'SS', 'FS', 'SF', 'TT' corners with temperature variation from -40 to 125 Celsius Degree.

*High Power Conversion Efficiency of DC/DC converter RC extraction Layout and high accuracy MPPT tracking

DC/DC converter [Without MPPT] power conversion efficiency post layout simulation(RC Extraction) can achieve 70 percent for 8uW input power and 89 percent for 1mW input. Maximum Power Point Tracker [MPPT] can track 8uW power source for 1 percent power loss inaccuracy and 1mW power source for 7.5 percent inaccuracy power loss.

5-3 Comparison with state-of-the-art publications

The comparison with state-of-the-art publications is shown in Figure 5-2. This work [layout simulation] achieved a smallest design area which is 0.18 mm^2 among other works: Qiu(2011) [12], Shim(2014) [13] and Stanzione(2015) [14]. The end to end Efficiency is only checked for Pin=1mW (83%) and Pin=8uW(67.5%) conditions and has not been checked in the whole input power range from 8uW to 1mW. The simulation to find the maximum end to end efficiency is still on going which will take one or two weeks to finish the simulation.

Parameter	Qiu	Shim	Stanzione	This Work (Layout)
Process	0.25um BCD	0.25um BCD	0.25um BCD	40nm
Max input voltage	2V	7V	60V	1.1V
Output Voltage	0 – 5V	1 – 8V	0 – 5V	1.5-2.5V
Input Power	10uW-300mW	33uW-10mW	1uW-1mW	8uW – 1mW
Function	Harvester Interface +MPPT	Harvester Interface +MPPT	Harvester Interface +MPPT	Harvester Interface +MPPT+LDO
Harvester type	Photovoltaic	Piezoelectric	Electret-based EEH	RF
Architecture	Boost	Buck-Boost	Buck	Boost
Control Power (nW)	2400	N.A.	500	2400 (Without LDO)
Max MPPT Efficiency (%)	N.A.	99	99	98
Maximum end to end Efficiency(%)	70	80	85	>83
Area(mm^2)	13	5.5	3	0.18

Figure 5-2: Comparison with state-of-the-art publications

5-4 Future Work

Figure 5-1 displays the final concept of energy harvester system. In this system, high frequency RF front end has been Schematic and Layout designed and also, Harvest Interface block has been designed in this master thesis project. Future work can be focus on:

*The design of Load Regulation part

The proposed structure of load regulation block is DC/DC buck converter to regulation output voltage with output voltage level requirement 1.1V and power conversion efficiency of Load Regulation part DC/DC buck converter should be over 90 percent. The output ripple voltage should be designed based on the application PSRR requirement.

*The design of the interface between Harvest interface block and load regulation block

As shown in Figure 5-1, the interface between Harvest interface block and load regulation block is composed of C_{out}[Energy Storage Element], a comparator[Continuously Monitor voltage on C_{out}] and control switches which is controlled by the comparator to charge and discharge C_{out}. This is because the voltage on C_{out} cannot be higher than 2.5V which is upper limit for 2.5V thick oxide power transistor in TSMC 40nm. When C_{out} is charged to 2.5V, harvest interface is switches off. Until C_{out} discharge to the load with V_{out} less than 2.5V, Harvest Interface is switched on to charge C_{out}.

*The improvement of MPPT detection accuracy

Shown in Figure 4-3, for Pin=1mW, the power detection accuracy is 92.5 percent which could be improved in the future work. This inaccuracy is mainly due to output voltage of RC integrator results in ADC input upper voltage clipping in Pin=1mW condition. The improvement could be to replace existing ADC with a higher input voltage range ADC.

*The establishing of rectifier model for Harvest Interface Simulation

The reason for not using rectifier for DC/DC boost converter simulation is due to the high working frequency of rectifier and low frequency DC/DC boost converter. In this project, the system simulation combined of DC/DC(Schematic), Digital MPPT (RTL), ADC+DAC with an ideal input power source will take one week to get results shown in Figure 4-2. Combining MOS Rectifier with DC/DC converter will be even worse! However, rectifier is an nonlinear Model in power, voltage or current and an ideal power source cannot fully model MOSFET rectifier. For future work, an effective way is need to establish an accurate MOSFET model for the Harvest Interface system simulation.

Appendix A

Appendix

A-1 Discrete Components

As shown in Figure 4-1, the discrete components contains input capacitor C_{in}, Output Capacitor C_{out}, Inductor $L1$ and LDO decoupling capacitor C_{LDO}. Below give the company series number and website of discrete components:

C_{in} Company Name: Murata Series Number: GRM32MB11H434JA01 Website: http://search.murata.co.jp/Ceramy/image/img/A01X/G101/ENG/GRM32MB11H434JA01-01.pdf

C_{out} Company Name: TDK Series Number: C1608X5R0G156M080AA Website: http://www.mouser.com/ds/2/400/lcc_commercial_general_en-837201.pdf

L_1 Company Name: TDK Series Number: VLCF4028T-220MR72-2 Website: https://product.tdk.com/info/en/catalog/datasheets/inductor_commercial_power_vlcf4028-2_en.pdf

C_{LDO} Company Name: TDK Series Number: CGJ2B2X7R1C102K050BA Website: http://www.mouser.com/ds/2/400/lcc_highreliability_general_en-520187.pdf

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Glossary

LDO Low Dropout Voltage Regulator

VRG Voltage Reference Generator

PCE Power Conversion Efficiency

ADC Analog to Digital Converter

DAC Digital to Analog Converter

ZCD Zero Current Detector

MPPT Maximum Power Point Tracking

PVT Process, Voltage and Temperature

WPT Wireless Power Transfer

WSN Wireless Sensor Network

MLCC Multi Layer Ceramic Capacitor

CCM Continuous Conduction Mode

DCM Discontinuous Conduction Mode

OTA Operational Trans-conductance Amplifier

ENOB Effective Number Of Bits

SCLK Slow Clock

FCLK Fast Clock

Reg Register

Pos-edge Positive Edge

Neg-edge Negative Edge

COM Comparator

XOR Exclusive Or

SPI Serial Peripheral Interface

RTL Register Transfer Level