# Combined ZVS–ZCS topology for high-current direct current hybrid switches: design aspects and first measurements

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**Abstract:** Power electronic switches have been considered for load switching ever since their invention. This is because semiconductor switches enable fast, arc-less, reliable and maintenance-free switching. The main disadvantages in relation to conventional switches (i.e. circuit breakers), however, are their sensitivity to transients, high on-state losses and the presence of leakage current. The advantages of both types of switches can be exploited by combining the semiconductor and the mechanical switch and thereby their disadvantages, arc formation and regular maintenance, can also be eliminated. For hybrid switches (HSs), both zero voltage switching (ZVS) and zero current switching (ZCS) are frequently used. A new hybrid switching topology has been developed where both ZVS and ZCS techniques are applied to the mechanical switch. The 'symbiosis' between these solid-state switching techniques and a mechanical switch eliminates several of the disadvantages, resulting in a more reliable direct current (DC) HS that requires less maintenance. The first turn-off measurement (up to 5 kA) from a prototype that has been developed for a 3-kV DC grid is presented.

## 1 Introduction

The implementation of direct current (DC) transmission systems in new applications such as ship supplies, renewable energy supplies and battery storage systems has grown rapidly during the past few decades [1, 2]. The joint Anglo-French ship program, Electric Ship Technology Demonstrator (ESTD) is a remarkable example thereof. The experience gained there still fuels the ongoing debate whether to adopt an AC or, alternatively, a DC transmission system [3]. Furthermore, that programme foresees the adoption (i.e. widespread implementation) of DC transmission systems in the long term – the next 5–10 years. The reason behind this prediction is that most power electronic systems, today, already implement an intermediate DC stage, which provides an easy access point for similar systems to be coupled to. This enables electrical energy to be exchanged among the respective systems. Such a direct DC coupling reduces the number of power conversion stages and results in a more reliable system with high efficiency. However, fast, reliable and maintenance-free DC switchgear needs to be developed before such a system can be realised. A large refit market for mechanical DC switchgear already exists for present DC applications such as traction for public transport and material handling systems. This also provides an interesting market for new DC switchgear in the future. The interest in using conventional DC switches for the ever-increasing power demands (short circuit power and currents) have subsided dramatically because of their high maintenance. The maintenance is required to counteract the contact erosion and subsequent damage to the insulated parts, brought about by the extended period of arcing when the switch is forced to open [4]. This has led to an increased interest in hybrid switching techniques and has already resulted in several direct current -hybrid switch (DC-HS) patents for ABB, Elpro, GEC-Alstom, Schneider, Siemens and Westinghouse. Even so, present techniques for constructing hybrid switches (HS) still have many disadvantages although they are being implemented in industry.

This contribution first describes the problems encountered when implementing the common techniques of Zero Voltage Switching (ZVS) as well as Zero Current Switching (ZCS) and thereafter defines a new hybrid switch topology which combines both these switching techniques and thereby eliminates several of the disadvantages mentioned above. Preliminary tests on a prototype of this hybrid switch technology, with a rated current of 7 kA and a line voltage of 3 kV DC, will be discussed. The prototype itself is shown in Fig. 1.

## 2 Hybrid switching

Hybrid switching was already described by Heumann and Koppelmann [5] in 1965. A HS combines a mechanical switch with a solid-state semiconductor to profit from the low on-state resistance (mechanical switch) and reduced arcing (semiconductor), respectively. The advantages and disadvantages regarding mechanical and solid-state switching are given by Atmadji and Sloot [6]. The HS is able to turn-off significantly faster than its conventional mechanical counterpart. Hereby, the conducted current is interrupted long before it can reach its prospective fault level, and therefore also at a far lower current value than would be the case for a mechanical switch. This implies that a low current-breaking capacity HS would



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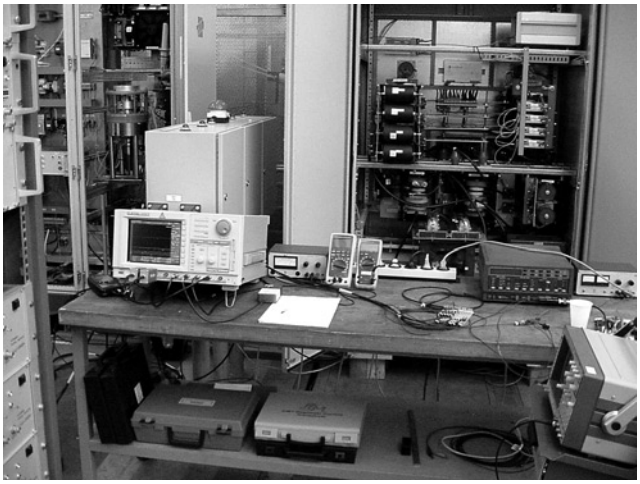

**Fig. 1** *Prototype of the switch under test:(left) the mechanical switch implementing ZVS, (right) the power electronics to realise ZCS*

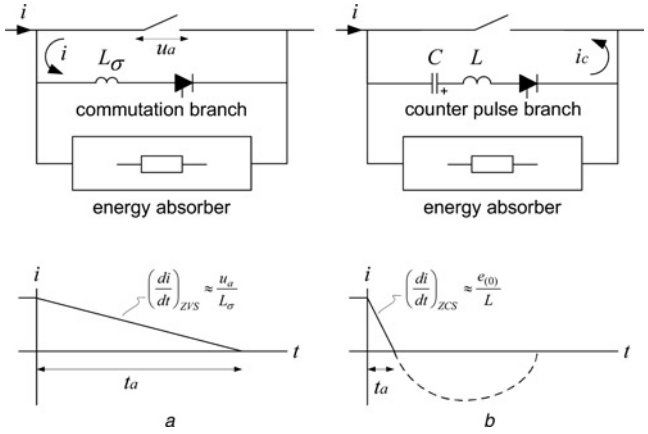


**Fig. 2** *Turn-off technique in a hybrid switch topology*

*For ZVS switching the $di/dt$ is determined mainly by parasitic components. The energy absorber reduces the voltage caused by the line current and the stored grid energy

*a* for ZVS

*b* for ZCS

be able to replace a mechanical switch with far higher current-breaking capacity.

Extensive research is being done on new HS topologies, like the one recently presented by Francis *et al.* [7], which removes some of the disadvantages mentioned above but only for a specific topology or application. Their results indicate that the contact wear for a HS (defined as material losses because of arc formation) is two to three orders of magnitude lower than that for conventional breakers [8]. Another important conclusion from them is that the material wear rapidly increases at arc durations >50–100 μs

Unfortunately, a HS still has a moving contact, making the occurrence of a short arc unavoidable for a successful commutation. The maximum arcing time together with the commutation speed (i.e. $di/dt$) can be translated to a maximum turn-off current [8], and is used as a design criterion. In general, two main techniques such as zero voltage switching (ZVS) and zero current switching are used in hybrid switching. These techniques, which are discussed in the next paragraphs, must reduce the arcing time and thereby increase the lifetime of the mechanical switch. The energy provided to an arc during the turn-off transition depends on the voltage across the mechanical switch, the current through the mechanical switch, and the duration of the arc. In general, arc reduction and thereby radiated electro-magnetic interference (EMI) reduction can be realised by introducing a parallel branch to the mechanical switch, as shown in Fig. 2.

### 2.1 Zero voltage switching

During ZVS, the main current is commutated to the parallel branch, which keeps the voltage across the switch close to zero when opening. The commutation process is dominated mainly by the arc voltage and the stray inductance between the mechanical switch and the power electronics. These parasitic components determine the typical ZVS turn-off technique, which is shown in Fig. 2*a*. The rate of current rise in the commutation branch can be determined by

$$\left(\frac{\mathrm{d}i}{\mathrm{d}t}\right)_{\mathrm{ZVS\_avg}} = \frac{u_\mathrm{a} - u_\mathrm{Tavg} - (i \cdot r_\mathrm{T})}{L_\sigma} \tag{1}$$

where $u_\mathrm{a}$ is the material dependent arc voltage, $u_\mathrm{Tavg}$ the average on-state semiconductor voltage and $L_\sigma$ the stray inductance between the mechanical switch and the commutation branch. The $i \cdot r_\mathrm{T}$ component can be neglected if it is small in relation to the $(u_\mathrm{a} - u_\mathrm{Tavg})$ component. If the contact current and voltage are greater than the minimum required values for arc formation, an arc will form [4]. Shortly after releasing the contacts, when the opening slit is close to 50 μm, the arc voltage steps to the so-called minimum required value that is typically between 11 and 14 V. The non-inductive voltage drop must remain smaller than the arc voltage in order for the current transfer to complete. It is possible to determine the maximum arcing time during the ZVS technique when the turn-off current, the typical rate of current rise, the stray inductance and the semiconductor parameters are known.

$$\begin{aligned} t_\mathrm{a}(i) &\simeq i \cdot \left(\frac{L_\sigma}{u_\mathrm{a} - u_\mathrm{T0} - (1/2) \cdot r_\mathrm{T} \cdot i}\right) + t_\mathrm{d} \\ &= i \cdot \left(\frac{\mathrm{d}i}{\mathrm{d}t}\right)^{-1}_{\mathrm{ZVS\_avg}} + t_\mathrm{d} \end{aligned} \tag{2}$$

where $i$ is the turn-off current, $u_\mathrm{T0}$ the semiconductor threshold voltage, $r_\mathrm{T}$ is the slope resistance and $t_\mathrm{d}$ the semiconductor turn-on delay time. This turn-on delay is often larger than that mentioned in most datasheets because of the low forward voltage and the often-reduced gate current at turn-on. Thus, the largest currents can be switched off when a small delay time, a large arc voltage, a small on-state voltage and a small stray inductance is realised. The complete ZVS commutation is illustrated in Fig. 3.

Fig. 4 shows the arcing time against turn-off current for typical $di/dt$ values [8] and a delay time $t_\mathrm{d}$ of 10 μs. This, together with the parameters mentioned in (2) is an important design criterion for hybrid ZVS techniques. For example, the parameters $u_\mathrm{a} - u_\mathrm{Tavg} = 4$ V and $L_\sigma = 100$ nH, resulting in an average $di/dt$ of 40 A μs$^{-1}$, will enable currents up to ~3.7 kA to be interrupted without violating the maximum critical arcing time of 100 μs.

### 2.2 Zero current switching

In the ZCS turn-off technique, an additional resonant current is realised, which flows in the opposite direction to the mechanical switch to reduce the main current (Fig. 2*b*). At the moment, the switch opens the current through the mechanical switch is already close to zero,

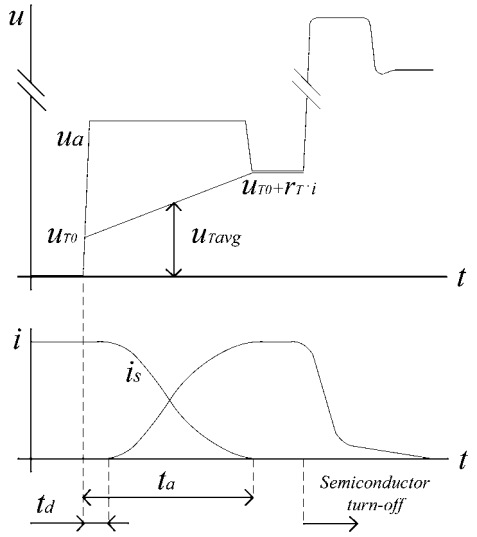


**Fig. 3** *Typical commutation when using the ZVS technique, where $u_a$ is the arcing voltage, $u_T$ the thyristor threshold voltage, $i_s$ the mechanical switch current, $t_d$ the delay time thyristor $t_a$ and the arcing time mechanical switch*

which reduces the arcing time and thereby the radiated EMI drastically. The counter current is realised with a pre-charged capacitor, and the peak value ($i_c$) must be at least equal to the maximum short circuit current. This results in the first constraint for the determination of $L$ and $C$ in the counter pulse branch, shown in Fig. 2*b*

$$e_{(0)} - \hat{i}_c \cdot \sqrt{\frac{L}{C}} = 0 \tag{3}$$

where $e_{(0)}$ is the capacitor pre-charge value, $L$ the total loop inductance and $C$ the capacitance. Selecting the oscillation frequency is the next step. Its half period should be equal to the time required to open the mechanical switch just far enough that it is able to withstand the full network voltage. This results in the second constraint.

$$t_{\mathrm{MSfv}} - \pi \cdot \sqrt{LC} = 0 \tag{4}$$

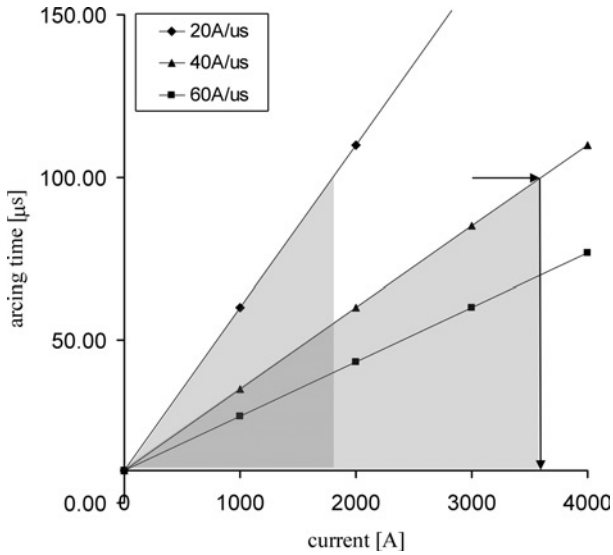


**Fig. 4** *Typical arcing time against turn-off current for three $di/dt$ values*

filled diamond, 20 A $\mu s^{-1}$, filled triangle, 40 A $\mu s^{-1}$, filled square, 60 A $\mu s^{-1}$ at $t_d = 10$ $\mu s$

where $t_{\mathrm{MSfv}}$ is the time between when the mechanical switch opening command is issued and the time it is capable of withstanding the full network voltage. Determining the values for $L$ and $C$ is not only restricted by these two constraints, but also by the grid inductance – the resonant inductor should be small in relation to the grid inductance (five times lower for example). Another important difference between ZVS and ZCS is that the $di/dt$ during a ZCS turn-off transition depends on the values of $L$, $C$ and $e_{(0)}$, which can be determined, within certain limits, during the design of the power electronics, and is thereby less dependent on the stray inductance. This will also results in more design freedom for the complete system. A larger $di/dt$ results in the arc extinguishing faster and also creates the possibility to turn-off larger currents without violating the maximum arcing time of $\sim$100 $\mu$s. The $di/dt$, which can be typically a few times higher than for ZVS, can be determined by

$$\left(\frac{di}{dt}\right)_t = \frac{e_{(0)}}{L} \cdot \cos\left(\frac{t}{\sqrt{LC}}\right) \tag{5}$$

For $t = 0$, the initial $di/dt$ can be found, which is the well-known $e_{(0)}/L$ value. The average $di/dt$, calculated by the integrating (5) over a period of $T/4$, will be

$$\left(\frac{di}{dt}\right)_{\mathrm{ZCS\_avg}} = \frac{2}{\pi}\frac{e_{(0)}}{L} \tag{6}$$

In reality, the $di/dt$ will be between the two limits given by (5) and (6), respectively. By turning off a relatively small current in relation to the counter pulse current, the $di/dt$ will approximate the initial $di/dt$. If both currents are approximately equal, the $di/dt$ will be the average value. Together with the turn-off current specification for a certain ZCS HS, the arcing time can be determined by

$$t_a(i) \simeq i \cdot \frac{\pi}{2} \cdot \frac{L}{e_{(0)}} = i \cdot \left(\frac{di}{dt}\right)^{-1}_{\mathrm{ZCS\_avg}} \tag{7}$$

With both switching principles applied the arcing time is reduced drastically in relation to the conventional breakers. This increases the lifetime and decreases the maintenance of the mechanical switch. Both techniques have their own distinct advantages and disadvantages. These are
Advantages of ZVS:

- no arcing at turn-on when the parallel semiconductors are used,
- no large resonant components.

Disadvantages of ZVS:

- smaller $di/dt$, lower current rating for the same arcing time,
- more difficult to realise large currents and short arcing times (i.e. parallel branches are needed to keep the stray inductance low, which can bring switch synchronisation problems),
- semiconductor needed for turn-on and turn-off capability.

Advantages of ZCS:

- larger $di/dt$, higher current rating possible,
- no need for tightly coupled power electronics (it offers more design freedom),
- semiconductor needed for only turn-on capability,
- less semiconductors needed for the same rating.

Disadvantages of ZCS:

- arcing during turn-on,
- large resonant components are required,
- continuous pre-charged capacitor present,
- every turn-off is associated with a large counter current, even with low currents.

## 3 Combined hybrid switching

One can perform some initial calculations based on the DC-HS specification, for the switch that has been built in this Research and Technology Project (RTP 16.16), and the information provided above. All the main considerations, which form the basis of the new topology choice, are briefly discussed and summarised next.

### 3.1 HS specification

A complete list of specifications has been compiled after deliberation with all project participants. Owing to the unavoidable influence from the electrical surroundings around the HS, the specification shown in Table 1 also includes grid-related demands.

The operation sequence mentioned in Table 1 attempts to clear the occurring fault and resembles that for purely mechanical switches. Thirty seconds after the first opening, the switch is closed again to re-energise the rest of the network behind the switch. If the fault persists, the switch will re-open and stay open for a longer time (180 s) before trying once again.

### 3.2 Topology choice considerations

For the ZVS technique, the stray inductance, $L_\sigma$, should be a few tens of nanoHenries, according to (2) and a maximum turn-off current requirement of 22 kA. This, however, is very difficult to realise. Fortunately, these large turn-off currents force more components to be placed in parallel to the HS, which keeps the stray inductance relatively low. Another difficult specification to meet is the turn-off capability of the semiconductor. It needs to be able to switch-off 22 kA, and it is here where the system reliability might falter. One solution proposed by Genji *et al.* [9] suggests placing semiconductors with relatively high turn-off capability in parallel to achieve the very high turn-off capability required. Press-pack turn-on semiconductor devices in the conduction state are far more suited to handle such large currents and should be implemented instead of turn-on/off semiconductors equipped with wire bondings. The limiting load integral, or the so-called $I^2t$ parameter, of the press-pack devices is sufficiently large to cope with these large currents without switching off, making them more suited for ZCS. The major disadvantage of ZCS is that a large counter pulse current (at least equal to the maximum turn-off current which in this case amounts to 22 kA) is required to switch-off the device at all current levels, even as low as 1000–2000 A. Despite this limitation, a requirement of bulky resonant capacitors and a current limitation due to contact wear (maximum turn-off current in case of ZVS is typically 2–4 kA), the ZCS is still considered favourable. The two HS techniques have been combined here to alleviate the problems encountered in the ZCS and ZVS techniques, respectively. The ZCS technique is capable of reducing fault currents up to 22 kA, while a small ZVS commutation branch is added to clear the currents up to a few kiloAmperes. This extra ZVS module, with reduced current specifications, eliminates the following disadvantages of the ZCS and ZVS technique:

- ZCS: no mechanical stress at low current turn-off,
- ZCS: no arcing at turn-on (i.e. ZVS turn-on is possible),
- ZVS: power electronics can be tightly coupled due to reduced current demand (small value of $L_\sigma$),
- ZVS and ZCS: arcing time can be kept below the critical value of $\sim$100 μs (implies less contact wear).

Probably, an even larger problem arises when considering the fault clearing operation sequence shown in Table 1. The problem occurs when the switch turns on during a downstream fault. In this situation, the parallel ZVS semiconductor used at turn-on experiences the huge $di/dt$ associated with a large over-current situation. This current usually exceeds the turn-off capability of the ZVS part and to resolve this, the combined topology uses the counter pulse branch to clear the fault current. A detailed explanation is given in the next chapter.

**Table 1: Summary of main switch specifications**

| Parameters | Value |
|---|---|
| Switch type | DC unidirectional |
| Cooling | Natural convection |
| Rated voltage | 3, kV DC |
| Maximum voltage | 3.4, kV DC |
| Rated current | 7, kA |
| Maximum turn-off current | 22, kA |
| Prospective fault current | 80, kA |
| Grid inductance | 100–300, μH |
| Short circuit time constant (i.e. $L/R$) | 2.7–8, ms |
| Operation sequence[a] (IEC 947-2) | O (30 s) CO (180 s) CO |

[a]A downstream fault.

## 4 System set-up and working principle

Fig. 5 shows the main components of the combined HS as well as the DC grid representation that was used. The complete HS assembly is divided into two main cabinets, the ZVS and ZCS cabinet, respectively. The cabinet in the middle contains the ZVS power electronics (hereafter called main stack), the mechanical switch and its electromagnetic (EM) drive [10]. The main stack has been mounted parallel to the mechanical switch that has two anti-parallel branches: a Gate Turn Off thyristor (GTO) branch and diode branch, T6 and D6, respectively. Current reduction during ZCS is performed by a LC counter pulse circuit, realised in a separate cabinet, and is located around T7, L7 and C7. This ZCS cabinet also contains the energy absorber (C7), the chopper (R8 and T8) and the charge reversal electronics (L9 and T9). All commutation steps have been subdivided into equivalent circuits, which contain only linear components (such as sources R, L and C). To determine the component specifications for both switching techniques, the equivalent circuits have been used to derive analytical (current) waveforms. Table 2 shows the components used for this first prototype. These will be discussed in detail in the next paragraphs.

### 4.1 Mechanical switch and drive

The mechanical switch is the limiting factor in a HS combination because of its inferior switching time when compared with semiconductor switches. The mechanical switch must

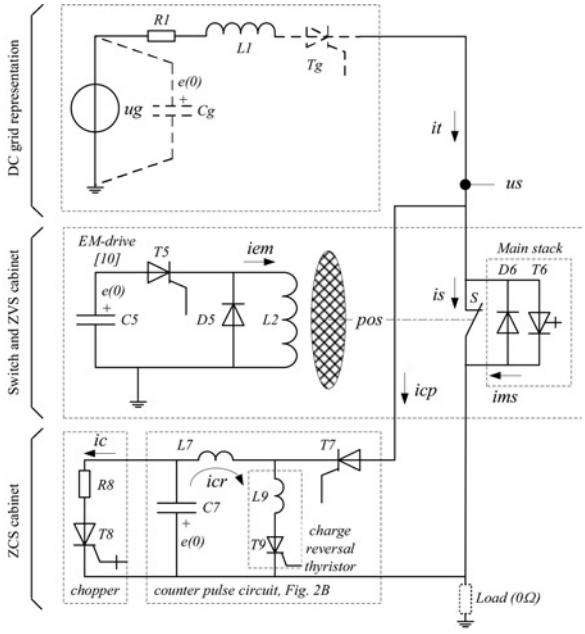


**Fig. 5** *HS topology including cabinet division and DC grid representation*

Grid parts are R1 and L1; Mechanical switch drive parts are T5, L5 and C5; ZVS parts are L$\sigma$ and T6; ZCS parts are T7,L7 and C7; Chopper parts are T8 and R8; Charge reversal parts are L9 and T9

be able to maintain the insulation and withstand the circuit voltage fastly. By using a high-speed EM drive, which can accelerate the movable contact up to 45 000 m $s^{-2}$, it is possible to maintain full network voltage (3 kV DC) over the switch after ~400 μs. The time to maintain full voltage across the mechanical switch determines the values for the LC counter pulse circuit when using ZCS. The development of this fast air-insulated mechanical switch is described in Roodenburg *et al.* [10] and falls beyond the scope of this contribution.

### 4.2 ZVS turn-off operated by the main stack

Fig. 7 shows the main stack used for ZVS. There are three main parameters that influence the commutation process:

**Table 2: Components used for the ZVS and ZCS topologies**

| Component | Type/value | Remark |
|---|---|---|
| C7 | 1170 μF (total) | Two in series |
| D6 | 4500 V 1300 A fast diode | Two in series |
| L7 | 25 μH | At 1 kHz |
| L9 | 40 μH | At 1 kHz |
| R1 | 37 mΩ | |
| R8 | 445 mΩ (total) | Two in series, four parallel |
| T6 | 4500 V/4000 A GTO | Two in series |
| T7 | 8500 V/1200 A thyristor | Two in series |
| T8 | 4500 V/3500 A IGCT | Two in series, four parallel |
| T9 | 8500 V/1200 A thyristor | |
| C5/T5/D5/L2 | 1250 μF | [10] |
| | 2000 A/5200 V thyristor | |
| | 2500 A/5500 V diode | |
| | 8–23 μH/L2 = *f*(pos) | |

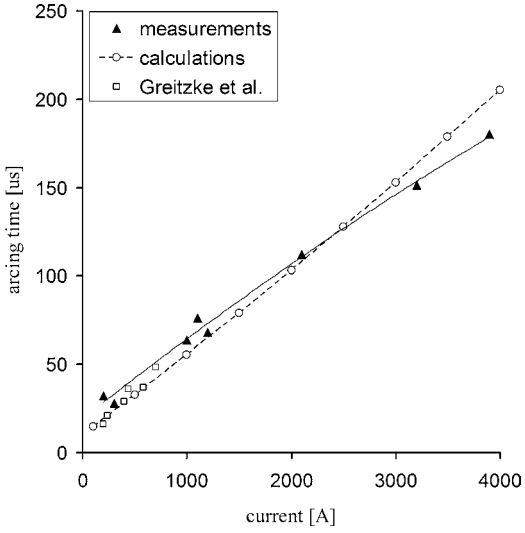


**Fig. 6** *Calculated and measured arcing time against turn-off current*

filled triangle, measurements of this contribution; open circle, calculations (i.e. $u_a = 12$ V, $u_{T0} = 4$ V, $r_T = 0.36$ mΩ, $L_\sigma = 350$ nH); open square, measurements from Greitzke and Lindmayer [8]

the loop inductance $L_\sigma$, the arc voltage and the turn-on delay of the semiconductor switch. The inductance depends on the loop area. During normal conductive operation, the mechanical switch is closed, which is shown in Fig. 7, state β. After the opening command, thyristor T6 is fired and the EM drive opens the mechanical contact. The arc voltage initiates the commutation, and when the commutation is completed, T6 is turned-off, both is shown in Fig. 7, states $\gamma$ and $\delta$, respectively. For all states mentioned equivalent circuits have been determined, which contains linear components (such as sources R, L and C). Analytical current waveforms for a ZVS turn-off sequence, with the same sequence indication as used in Fig. 7, are shown in Fig. 8*a*.

The main stack has been developed to turn-off currents up to 2 kA with a maximum arcing time of 100 μs. Using (2), this results in a $di/dt$ of at least 20 A $\mu s^{-1}$ or equivalently a stray inductance smaller than ~0.4 μH. Stray inductance calculations have been done with the method described in Evenblij *et al.* [11]. Fig. 6 shows the calculated arcing times as a function of the turn-off current (dotted line). Besides our own measurements, which will be discussed later, there is also arcing data added in Fig. 6 from Greitzke *et al.* [8], where a similar ZVS topology is described. Our own calculations are based on the parameters of the main stack, which are $L_\sigma = 0.35$ μH, $u_a = 12$ V, $u_{T0} = 4$ V, $R_T = 0.36$ mΩ and $t_d = 10$ μs.

### 4.3 ZCS turn-off

Larger currents (2 kA) and fault currents should be turned-off via ZCS or via the combination of ZVS and ZCS, which is described in the next paragraph. During normal conductive operation, the switch is closed and capacitor C7 is pre-charged, as shown in Fig. 7 state B. A certain delay after the opening command, which is the dead time of the EM drive, the counter pulse thyristor T7 is fired. The arc, which was already formed, is extinguished and the excess in current (i.e. pulse current minus line current) flows through the diode D6, which is shown in Fig. 7 state C. The extinguishing of the arc is much faster because of a much higher $di/dt$. Thus with the ZCS technique, the nominal turn-off current can be increased

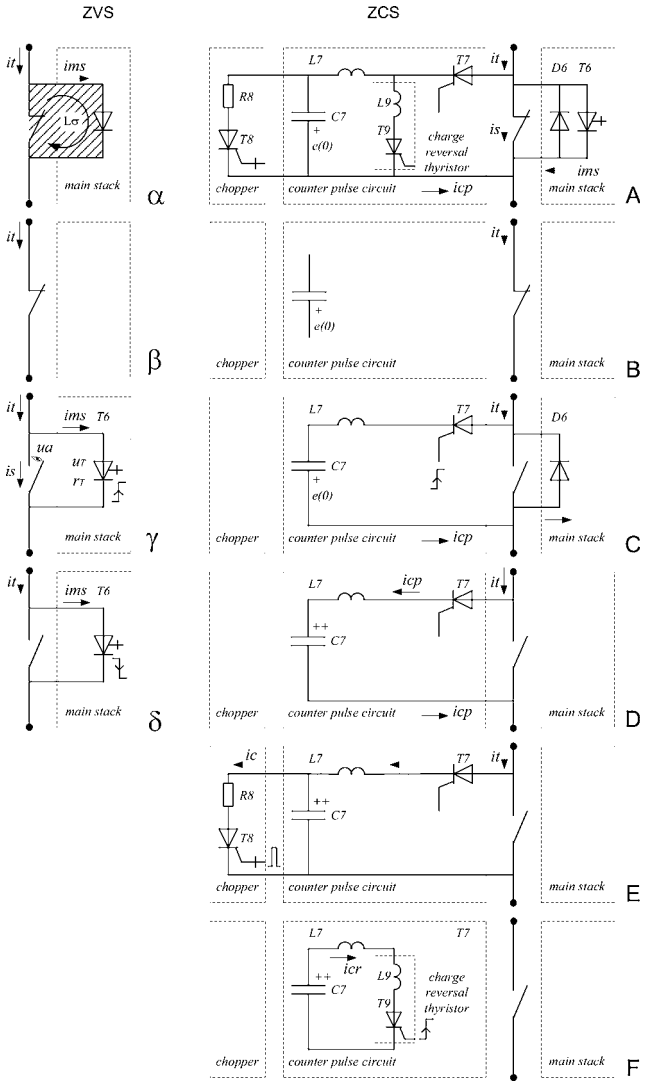


**Fig. 7** *Commutation steps during both switching techniques*

ZVS ($\alpha$): normal conduction ($\beta$), commutation to main stack ($\gamma$), turn-off ($\delta$); ZCS (A): normal conduction (B), counter pulse (C), energy absorbance without chopper (D), energy absorbance with chopper (E) and charge reversal (F)

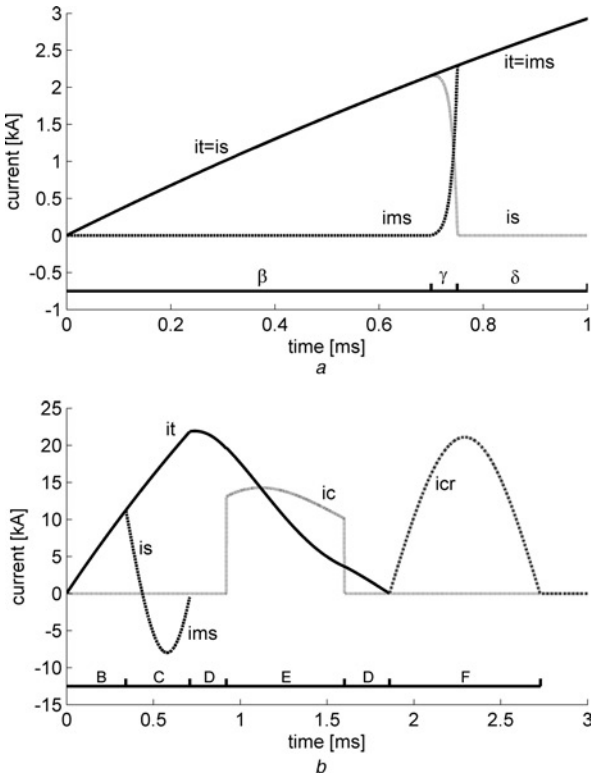


**Fig. 8** *Typical main currents (analytically determined via linear equivalent circuits) and the following component parameters: Grid: $R1 = 37\ m\Omega$, $L1 = 100\ \mu H$; ZVS: $L\sigma = 0.35\ \mu H$, $r_T = 0.36\ m\Omega$, $u_T = 4\ V$; ZCS: $C7 = 1170\ \mu F$, $L7 = 25\ \mu H$, $L9 = 40\ \mu H$, $R8 = 445\ m\Omega$, Chopper hysteresis settings = 5.9–4.5 kV*

*a* for ZVS commutation
*b* ZCS turn-off

further, while the arcing time can be kept below the critical value of 100 μs. The timing during such a ZCS turn-off can be critical. If the counter pulse reduces the current while the mechanical contact is still closed, a fast rising current transfer occurs in the diode, instead of low decreasing current in the mechanical contact.

After the counter pulse, a new low-frequency oscillation, involving line inductance L1, starts. Initial conditions are determined from the continuity in the line current (Figs. 5 and 7 state D). The capacitor voltage is reversed and the line current starts decreasing only when the voltage of C7 exceeds the grid voltage. The stored network energy in $L1$ and the driving voltage will increase the voltage across C7 further. If this voltage becomes very high, the energy is dissipated with the chopper, which is shown in Fig. 7 state E. Typical current waveforms during such a turn-off sequence, with the same sequence indication as used Fig. 7, is drawn as shown in Fig. 8*b*. During this turn-off, a single chopper intervention can be obtained, which is arbitrarily and depends on the chopper settings and the grid inductance.

With the demands specified in Table 1, (3) and (4), one is able to define components for the resonant counter pulse circuit. The value of $L7$ should be small in relation to the minimum value for $L1$, which is 100 μH. With the maximum turn-off current, the time to withstand full voltage, and an assumption for the pre-charge value, which are 22 kA, 400 μs and 3.5 kV, respectively, the resonant components L and C can be determined. The use of (3) and (4) results in two equations with two unknown variables, which must be ~20 μH and 800 μF. In practice, the choice is determined by commercial models. In the first prototype, 25 μH and 1170 μF is used, which results in slightly different, but still usable, values. Using (5) and (6), one can determine the $di/dt$ during the ZCS commutation, which initially is 140 and 90 A $\mu s^{-1}$. For a nominal line current of 7 kA, the arcing time can be determined using (7) and results in 80 μs.

### 4.4 Combined ZVS and ZCS turn-off

The GTO T6 is not strictly necessary in ZCS turn-off, it could be left open (un-triggered). Nevertheless, the GTO can co-operate in the turn-off process and it will be used as follows: the GTO is turned-on as soon as the switch turn-off command is given. After the switch delay time, the arc is initiated and commutates the current completely (or partly), which depends on the $di/dt$ of the fault current and the $di/dt$ during commutation, to the GTO (ZVS). After a certain delay, which is a combination of the dead time of the mechanical switch–drive and the main current, the counter pulse capacitor T7 is fired. The arc, if still there, is extinguished and the excess of current (pulse current minus line current) flows through the diode D6. In this phase, the GTO T6 is turned-off softly (i.e. its voltage

and current are close to zero). Hereafter, the switch sequence will be equal to the normal ZCS turn-off transition, which can be seen in Fig. 7 states D, E and F.

### 4.5 Chopper intervention

The line current after turn-off and grid energy in $L1$ will increase the voltage across the counter pulse capacitor (C7), which is shown in Fig. 7 state D. If the counter pulse capacitor must act alone as a clamping device, the voltage will increase (in this case up to ~11 kV), which is very high. The increase in energy, which amounts to 70 kJ, is caused by two phenomena: the energy delivered by the grid and the stored energy in the grid inductance. For this reason, HSs have an extra parallel branch to absorb this energy, as shown in Fig. 2. For this prototype, an Insulated Gate Commutated Thyristor (IGCT) chopper has been realised, which is symmetrically build around the counter pulse capacitor that consists of two capacitors in series. The chopper is controlled by the capacitor voltage and has its hysteresis-band between 5.9 and 4.5 kV. The turn-off threshold, which is set at 4.5 kV, must be larger than the maximum line voltage (of 3.9 kV), so that the current decreases continuously. The equivalent resistance of the chopper, *R8* in Fig. 7, equals ~445 mΩ. In this case, the maximum chopper current equals ~13 kA and the total IGCT turn-off current ~10 kA. Together with the voltage specification this results in four parallel branches with two IGCTs in series (at turn-off 2250 V and 2.5 kA per IGCT). The excess energy can therefore be dissipated in 1 ms with this chopper.

### 4.6 Charge reversal

During the ZCS counter pulse, the voltage across C7 is reversed and further charged because of the line current. When the capacitor voltage reaches its maximum value of 5.9 kV, the chopper activates. The chopper intervention stops at 4.5 kV. Thus, after turn-off, there is always enough charge stored for the next turn-off event, but its polarisation is reversed. However, the chopper intervention stops at 4.5 kV and the required pre-charge voltage is limited to 3.5 kV. To match these conflicting values, a small resistance is added in the resonant reversal circuit. Via the charge reversal thyristor, the polarisation is reversed, which is shown in Fig. 7 state F and Fig. 8, respectively. If the voltage caused by leakage in active and passive components falls below 3.5 kV, the remaining charge will be added by an external capacitor charger. This charger is also needed to charge the capacitor during the initial start-up of the system. To reduce the peak current and thereby the mechanical stress, an extra inductor L9 is added, which has a value of 40 μH. The relationship between capacitor voltage and peak current is equal to (3), but now with a total inductance of L7 + L9, it equals 65 μH.

### 4.7 Zero voltage turn-on

When the command to close reaches the HS, the GTO parallel to the mechanical contact is turned-on first. If a short circuit is present and a trip occurs, the fault current, which flows through GTO, is cleared with the ZCS counter pulse without involving the mechanical switch. If the initial $di/dt$ of the line current and its final level are within the rated limits, the mechanical switch is ordered to close (depends on grid specifications). After closing the mechanical switch, the GTO remains closed for 10 ms to prevent arcing during the bouncing of the mechanical contacts. By using the ZVS technique during turn-on, one is able to meet the demanding sequence 'open; closed-open; closed-open' prescribed in IEC947-2.

## 5 First measurements

The first measurements have been carried out with reduced contact speed. This has led to small changes in the switch timing. The dotted components, which are depicted in Fig. 5, are now used as DC grid representation (a pre-charged capacitor Cg of 3320 μF, an inductor L1 of 266 μH and an extra thyristor Tg). Via this artificial grid, the HS is connected to the load, which in this case is a short circuit. All described experiments start with an initially closed mechanical switch and the opening command is triggered at a preset trip level. Owing to this change in grid representation, there is less energy to be dissipated and thereby lower turn-on and turn-off settings for the chopper are needed. The turn-on and turn-off values have been set to 2.6 and 2.3 kV, respectively. With the described topology, two types of measurements have been carried out: a hard turn-off in the ZVS mode by using only the main stack and a combined ZVS and ZCS turn-off. During the ZCS experiments, the pre-charge voltage of the counter pulse capacitor (C7) is lowered to the maximum required value of 2.5 kV.

### 5.1 ZVS turn-off

Fig. 9 shows a hard turn-off with a line current $di/dt$ close to zero. Fig. 10 is a magnification of Fig. 9 and shows in more detail the commutation and the switch voltage during arcing. At 1 ms, the capacitor Cg is discharged by firing the thyristor Tg. At 2.8 ms, the trip command is given and, after a short delay time of the EM drive a small

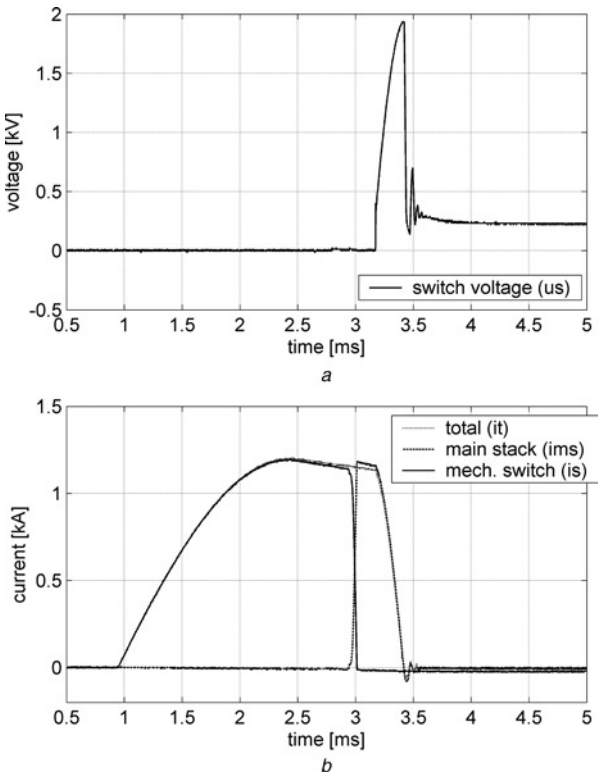


**Fig. 9** *Typical ZVS hard turn-off transition at ~1.2 kA*

*a* Voltage across the switch
*b* ZVS commutation and snubbered GTO turn-off at 3 and 3.2 ms, respectively

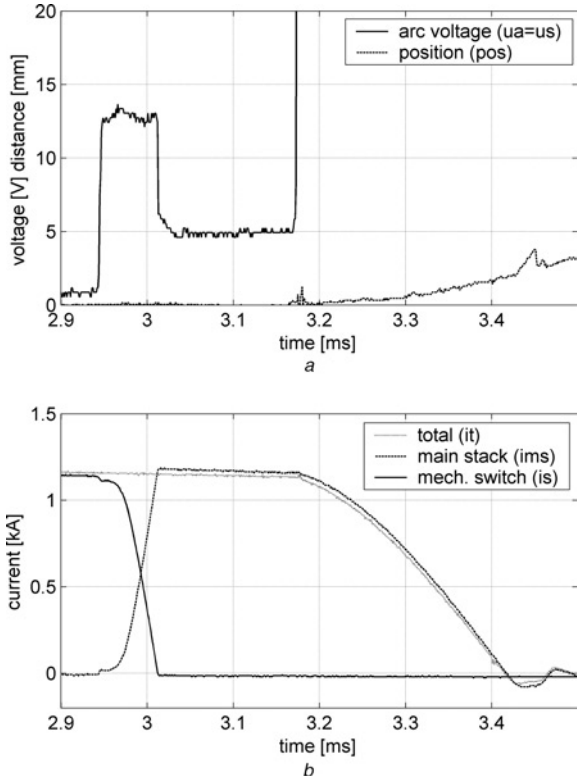


**Fig. 10** *Magnification of Fig. 9*

*a* Detailed arc voltage and contact position
*b* Detailed current commutation

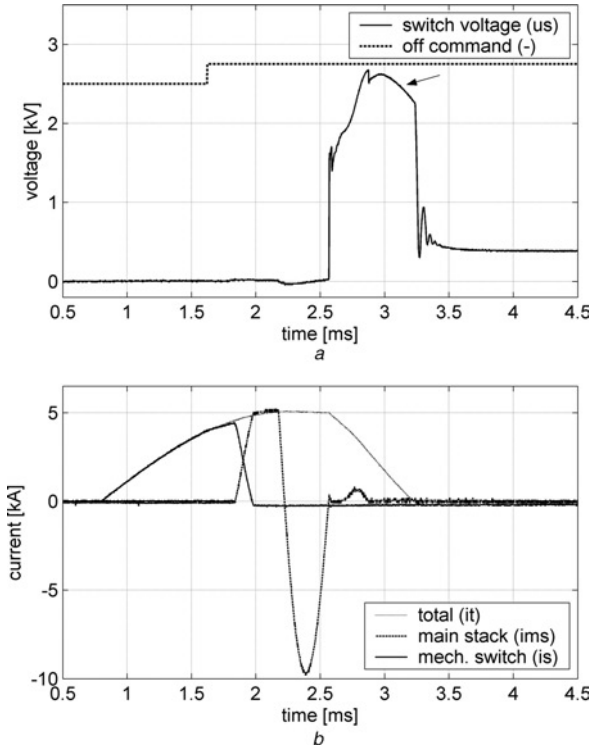


**Fig. 11** *Typical turn-off for the combined ZVS and ZCS at ∼5 kA*

*a* Voltage across the switch and the turn-off command
*b* Current commutation from mechanical switch to main stack followed by ZCS turn-off

contact slit in the order of 50 μm appears, which results in the typical material-dependent arc voltage of ∼13 V. This voltage is nearly constant during the commutation and lasts ∼68 μs. This measured arcing time value is depicted together with its calculated equivalent in Fig. 6. The calculations have been performed using (2) and are in good agreement with the measured values. From ∼3 ms, the load current flows completely in the parallel GTO branch and is turned-off after 180 μs. Commutation from the mechanical switch to the GTO takes place with an average $di/dt$ of ∼22 A $\mu s^{-1}$. With the measured $di/dt$ and the GTO anode–cathode voltage, the real stray inductance can be determined to be ∼0.4 μH. This value is in good agreement with the calculated value.

The first movement determined by the position transducer can be observed from ∼3.2 ms, which is 400 μs after the trip that takes place at 2.8 ms. In the normal situation, this means that the contact will be able to maintain full voltage at 3.2 ms, without reduced speed. In this particular case, the GTO turn-off is, from a safety point of view, too early. But on the other hand, the full voltage (1.9 kV) caused by the snubber, which must absorb the line current, is reached at 3.4 ms. The contact separation is already ∼2 mm after 3.4 ms, which is sufficient to avoid re-striking at this voltage level. The total turn-off time of the 1200 A then amounts to ∼600 μs.

### 5.2 Combined turn-off

Figs. 11 and 12 show two different combined ZVS–ZCS turn-off experiments. For the first one, the trip level was set at 4 kA and the opening command to the mechanical switch is given almost immediately. Shortly after this command, the voltage across the switch rises to the arc voltage of ∼16 V, which is slightly higher than that for the ZVS experiment at 1200 A. This is mainly caused by the increased gap distance during current commutation. Owing to a line current $di/dt$ of 3 A $\mu s^{-1}$, the ZVS commutation starts at 4.4 kA. The arc voltage commutates the current to the main stack in ∼180 μs and afterwards the

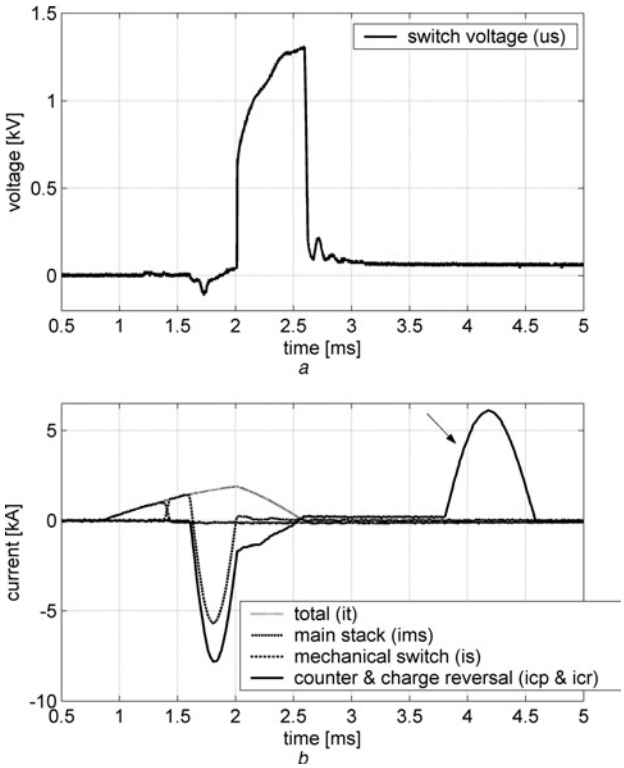


**Fig. 12** *Typical turn-off for the combined ZVS and ZCS*

*a* Voltage across the switch
*b* ZVS and ZCS commutation followed by charge reversal, respectively

voltage steps to the anode–cathode voltage of the two GTOs in series. At the end of this interval the counter pulse circuit is fired, which reduces the GTO current, at that moment 5 kA, with an average $di/dt$ of $\sim$100 A $\mu s^{-1}$ to zero. This value depends on $e_{(0)}$, which was lowered for this experiment to 2.3 kV. This value is in good agreement with the calculated value using (5), which equals 92 A $\mu s^{-1}$. If the last mentioned $di/dt$ had been directly used in a single ZCS turn-off (i.e. not the combined ZVS–ZCS) the arcing time would have been $\sim$54 $\mu$s.

Owing to the voltage reversal, the anti-parallel diode conducts the excess counter pulse current. After the negative part of the counter pulse, the voltages rise rapidly because of the energy in the grid inductance. At $\sim$2.5 kV, the upper chopper level has been reached and the chopper is activated. From 3 ms onwards, the voltage decreases while the total current remains positive. Equal voltage and current shapes (determined analytically) are shown in Fig. 8.

The arc voltage in Fig. 10*a* is directly measured across the mechanical contacts, which means that for commutations in the ZVS branch (between D6 and T6 in Fig. 7) the stray inductance $L\sigma$ is always involved. From 2.5 ms, the voltage rises rapidly and the contact distance is large enough (at least 5 mm) to sustain the reapplied voltage. Total turn-off time of the 5 kA takes $\sim$1.6 ms.

The second experiment (Fig. 12) also shows a typical combined ZVS–ZCS turn-off at $\sim$1 kA, but now the current in L7 has been measured. This current contains the counter pulse current from 1.6 to 2 ms, the grid current from 2 to 2.5 ms and the charge reversal current from 3.8 to 4.6 ms.

## 6 Discussion

Besides these three described measurements, measurements have been taken in the range from 200 A to 4 kA. All measured arcing times have been added in Fig. 6. The calculated values are in good agreement with the measured data in this contribution and with the measurements from Greitzke and Lindmayer [8]. However, for larger currents, a lower measured value has been obtained. This lower arcing time at higher current values is mainly caused by a slightly higher average arc voltage, $\sim$16 V instead of $\sim$13 V. This is caused by the increased distance between the two contacts, which resulted in a larger arcing voltage [4].

Currents, that are smaller than 1.5 kA are switched off with the main stack, while all currents above 1.5 kA have been turned off with the 22-kA counter pulse current. For currents in the range of 1.5–15 kA, this is greatly over dimensioned. One method to decrease this gap is to increase the current capability of the ZVS part (main stack) without violating the maximum arcing time demands. This can be realised by decreasing stray inductance, decreasing the semiconductor threshold voltage or increasing the material-dependent arc voltage (1). A decrease in threshold voltage, up to $\sim$50%, can be reached by using so-called TGTOs, which have, due to the transparent emitter, a much lower threshold voltage. A decrease in stray inductance can also be realised by placing switching branches in parallel (e.g. two main stack branches in parallel results in half the stray inductance and thereby double the turn-off current for the same arcing time).

At first, the HS topology described here was especially designed for a DC application, but, with some extensions it can also be used for AC applications. For instance, the well-known bi-directional topology for a ZCS [12], it can be expanded with a bi-directional version of the main stack. The GTO and diode in this main stack, which fulfil the ZVS, should be replaced with two anti-parallel, fully controllable devices and switch them according to the current direction during the trip condition and all subsequent phases of the turn-off. The control of this bi-directional system gets more complicated, but it is feasible.

Future measurements with this system will verify the arcing times with currents up to 7 kA, in only the ZCS mode. The intermediate ZVS step, which was carried out in advance, will be skipped. Also in this case the expected arcing time, which can be calculated with (7), will be below the critical value. For the maximum turn-off current, in this case 22 kA, the arcing time will be two times the critical value; how this relates to contact wear will be investigated in the near future.

## 7 Conclusions

This contribution describes the design and the successful first tests of a DC-HS, which uses a fast mechanical switch and the combination of two solid-state techniques: ZVS, and ZCS. This 'symbiosis' eliminates several disadvantages of the individual techniques, which brings these DC switchgear techniques closer to the commercial market. The developed prototype has been designed initially for a 3 kV DC ship distribution grid and has a nominal current of 7 kA. With this new combined topology

- The arcing times in the mechanical switch can be kept below the critical value for turn-off currents up to 7 kA. This to minimise contact wear.
- Low currents are no longer turned-off with a large counter pulse current, like in a single ZCS HS, but rather a simple hard ZVS turn-off is used.
- One has more design freedom in choosing the current distribution between ZVS and ZCS turn-off. Low current turn-off with the ZVS part, results in smaller power electronics, which must be tightly coupled with the mechanical switch. On the contrary, a large ZCS cabinet can placed further away from the mechanical switch.
- There is no arcing at turn-on because of the implementation of parallel ZVS semiconductors. The operation sequence mentioned in IEC947-2 can hereby be fulfilled.

To minimise the contact wear, simple formulae have been derived to estimate the arcing times for both switching techniques. From literature it is known that arcing times below the critical value, typical 100 $\mu$s, result in less contact wear. For small arcing times ($<$200 $\mu$s), the simple linear behaviour described in this contribution can be used, which uses the fixed material dependent arcing voltage. With this knowledge, one is able to choose the correct current distribution between ZVS and ZCS. For the first prototype, ZVS turn-off is used for currents between 0 and 2 kA and ZCS turn-off between 2 and 22 kA. By optimisation of the design, the ZVS current range can be increased a few times by using parallel branches and semiconductors with a low on-state voltage, this decreases the stray inductance and increases the commutation voltages, respectively.

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