

DELFT UNIVERSITY OF TECHNOLOGY  
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# Performance of a KID

*On the influence of the resonator geometry on the noise and  
Q-factor of a kinetic inductance detector*

in partial fulfillment of the requirements for the degree of

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## Abstract

Space-based astronomy is in need of a photon-noise limited detector with multiplexing opportunities. The kinetic inductance detector (KID) is capable of both properties. An incoming photon breaks Cooper pairs in the superconducting layer of the KID, which leads to a change in inductance, which can be detected with phase- and amplitude read-out. Photon noise, generation-recombination noise are inevitable noise sources, but two-level system noise can be minimized by adjusting the resonator and its geometry.

To gain insight in the noise and loss sources this thesis investigates the difference between microstrip and co-planar waveguide resonators; and the difference between a silicon substrate and a silicon-on-insulator substrate.

Numerical analysis shows that: noise in all types of resonators are dielectric bulk dominated; an Al superconducting layer shows has different losses in terms of Q-factor, compared to a NbTiN superconducting layer, but quantitatively the same internal Q-factor in the order of  $10^5$  is achieved; an Al superconducting layer in a microstrip has 5dBc/Hz and 2dBc/Hz higher noise in the metal-air and metal-edge interfaces, respectively, compared to a NbTiN superconducting layer; an Al on Si CPW and microstrip have the same Q-factor performance; an Al on Si CPW has a 2-8dBc/Hz more noise at all interfaces compared to an Al on Si microstrip; a buried oxide layer has no influence on the loss in terms of the Q-factor for 100nm Al on Si substrate CPWs; and that the noise of an Al on SOI CPW is bulk dominated, and the dielectric bulk contributes 10dBc/Hz more to the noise, compared to an Al on Si CPW.

Experimental analysis shows that a gapwidth of  $w_{gap} \geq 10\mu\text{m}$  for Al on SOI CPWs shows no response, due to high two-level system noise. Low Q-factors in the order of  $10^4$  have been measured for Al on SOI CPWs, which is low compared to literature. A high set-up noise of -85dBc/Hz and divergent relationships with the internal power indicate that TLS-noise does not dominate the measurements, and set-up negatively influences the measurements.

In conclusion, the resonator geometry is an important factor for the performance of a KID in terms of noise and Q-factors. A buried oxide layer has no consequence for the Q-factor, and negatively affects the noise of a CPW.





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# Preface

This document is my Bachelor of Science graduation thesis, and in it I reported the research on kinetic inductance detectors that I have carried out from January up till July 2015.

When I started my research, I had to familiarize myself with jargon and new concepts. *Chapter 1* contains an explanation of the concepts and a motivation for the research on kinetic inductance detectors and the specific geometries and materials in this thesis.

*Chapter 2* contains an explanation and the results of the numerical analysis in modeling software COMSOL. The numerical analysis has proven useful to gain insight and expectations of the differences in performance of various geometries and materials.

*Chapter 3* gives an overview of the experimental set-up which was used to measure the kinetic inductance detectors at SRON in Utrecht.

*Chapter 4* presents the results of these measurements and comments on data and figures.

The experimental results of *Chapter 4* are discussed and compared to the numerical analysis of *Chapter 2* and to other literature in the discussion in *Chapter 5*.

*Chapter 6* contains conclusions which are drawn from the numerical analysis in *Chapter 2* and the experimental results in *Chapter 4*, and its discussion in *Chapter 5*.

## Acknowledgements

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# Chapter 1

## Introduction

### 1.1 Terahertz astronomy

Terahertz astronomy is a subdivision of observational astronomy, which has been divided in bands in terms of wavelength and frequency. The terahertz range is loosely defined, but generally concerns frequencies of 0.1-10THz. The terahertz range includes the infrared and submillimetre range. Half of the luminosity of the universe and 98% of the photons emitted since the Big Bang are observable in the far-infrared range [1] and the early universe is redshifted in this range [2]. In the terahertz range astronomers can examine molecular clouds, dark cloud cores and gain insight in the formation and evolution of stars and galaxies.

The Herschel Space Observatory was a submillimetre and far-infrared telescope, and was launched on the 14th May 2009. Planetary systems and processes like the birth of galaxies in the early Universe have been researched during its lifetime of four years. An infrared image by Herschel of the star-forming region Cygnus-X is presented in figure 1.1, where sites of massive dust and star formation can be seen.

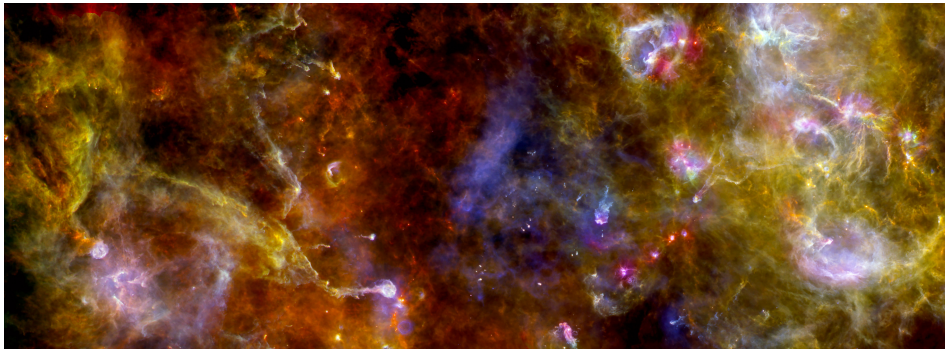


Figure 1.1: ESA Herschel image of star-forming region Cygnus-X using PACS and SPIRE instruments to observe at infrared wavelengths:  $70\mu\text{m}$  (blue),  $160\mu\text{m}$  (green) and  $250\mu\text{m}$  (red). Photo: ESA/PACS/SPIRE/Martin Hennemann & Frédérique Motte.

The Earth's atmosphere, and especially the water in it, absorbs THz radiation. This makes ground-based infrared observations difficult and limited. However, some ground-based observations are carried out in the terahertz range and are located at places with dry, cool and stable weather, such as the South Pole and the Atacama Desert in Chile. Even observations from an airplane in the stratosphere above have been carried out with the Stratospheric Observatory for Infrared Astronomy (SOFIA) by NASA and DLR to overcome the obstacles of ground-based observations [3]. Space-based astronomy remains the ideal option for observations in the terahertz range in terms of visibility.

On top of the Earth's atmosphere THz astronomy also suffers from the lack of suitable detectors. Detectors are much harder to make than detectors in the optical range. There is a need for large imaging arrays for submillimetre wavelengths [4]. Only detectors operating at very low temperatures reach the required sensitivity.

### 1.1.1 Low temperature detectors

Low temperature detectors work at cryogenic temperatures around 100mK and are sensitive to incoming photons. There are two methods to measure photons in the terahertz range: bolometric detection which detects a small change in temperature due to the incoming photons and pair-breaking detection which detects an increase in the quasiparticle density due to the incoming photons. Multiplexing multiple detectors into large arrays causes problems, because there are limitations to the number of single detectors that can be linked to one main multiplexed line. The MUX-ratio (MUX is short for Multiplexer) is a measure for the quantity of multiplexing, and is defined as the number of wires per main multiplexed line.

The most common low temperature detectors are bolometers and pair-breaking detectors:

- **Bolometers** are thermal detectors which measure the change in temperature due to incoming photons using a resistive thermometer. The technology has been around for long and is mature, but detectors and electronics are relatively large. A bolometer is a variable resistance, and has to be read out with a parallel Volt meter, which leads to a low MUX-ratio around 30-100. This makes bolometers hard to multiplex.
- **Transition edge sensors** (TES) are bolometric detectors that use the temperature-dependent resistivity around the critical temperature of a superconductor. An incoming photon can change the phase transition of the superconductor, and this changes the resistivity which can be measured. Large arrays and multiplexing is possible, but difficult with a TES, because the response is not very fast and each sensor needs a superconducting quantum interference detector (SQUID) as an amplifier for readout [5]. TES's have a low MUX-ratio of 30-100.
- **Superconducting tunnel junctions** (STJ) are pair-breaking detectors that detect quasiparticles, which are excited by photons, crossing a barrier between two superconductors [6]. However, Cooper pairs also cross the barrier creating a Josephson current [7], which have to be leveled out using a magnetic field. Each detector needs to suppress its Josephson



current, which is slightly different for each detector. This makes multiplexing into a large array inconvenient.

- **Kinetic inductance detectors (KID)** are pair-breaking detectors that detect the breaking of a Cooper pair due to an incoming photon. KIDs have the main advantage that frequency domain multiplexing is possible, so they can be placed in large arrays [8] with MUX-ratios around 1000-10000.

In conclusion: The possibility for easy frequency domain multiplexing, the high Q-factor and the possibility to measure small changes in the Cooper pair density makes the KID a promising new detector.

## 1.2 Working principle of a KID

The microwave kinetic inductance detectors (MKID or KID) is a type of a superconducting photon detector first developed at California Institute of Technology in 2003 [9]. The working principle of the KID is explained in this section.

### 1.2.1 Superconductor

Metals, such as Aluminium, behave like superconductor below a critical temperature  $T_c$  (for Aluminium  $T_c \approx 1.1\text{K}$ ). A superconductor has zero electrical resistance and expulsion of the magnetic field of the superconductor, known as the Meissner effect [10]. A MKID is a type of superconducting detector. The detector is cooled down to  $T \approx 100\text{mK}$ , so the Aluminium in the detector behaves like a superconductor very close to its ground state, because  $T < T_c$ .

Aluminium has long been used in MKIDs, because of its low gap energy ( $\Delta = 168\mu\text{eV}$ ), a long electron-phonon time constant  $\tau_0$  of 458ns which leads to long quasiparticle lifetimes at intermediate temperature and a high enough quality factor [11]. The detector works at photon energies  $\hbar f > 2\Delta$ . This means photons with a frequency of roughly  $f > 80\text{GHz}$  can be detected, which means the whole THz range (which starts  $\sim 100\text{GHz}$ ) can be detected with superconducting Aluminium.

### 1.2.2 Cooper pair and quasiparticles

A Cooper pair is a pair of electrons bound together at low temperature, and was first discovered by Leon Cooper in 1956 [12]. The Cooper pair state is responsible for superconductivity according to the BCS theory [13].

A Cooper pair is bonded with an energy of  $2\Delta$ , where  $\Delta$  is the superconducting gap energy. A Cooper pair can break, due to an incident photon with an energy of  $\hbar\omega > 2\Delta$ , and two quasiparticles emerge (see figure 1.2 left).

This breaking of Cooper pairs changes the inductance of the MKID, because the inductance is dependent on the amount of quasiparticles in the superconductor. A MKID can be seen as

an electronic circuit as showed on the right in figure 1.2, where an incoming photon changes the inductance of the circuit.

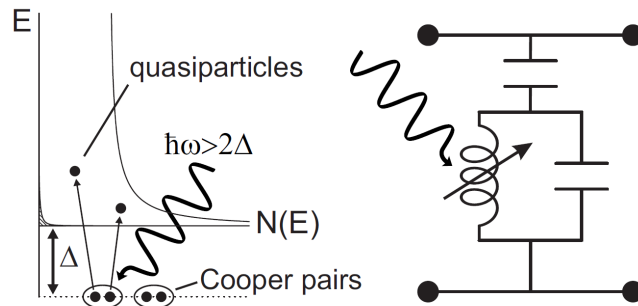


Figure 1.2: Left: Energy diagram of a breaking Cooper pair by a photon with energy  $\hbar\omega > 2\Delta$  into quasiparticles. Right: Electronic representation of a MKID, where an incoming photon leads to a change in the kinetic inductance of the resonator. Figure from [5].

The microwave transmission of a MKID changes when a photon breaks a Cooper pair. The change in inductance shifts the resonant frequency and the change in resistance decreases the depth of the resonant dip. This effect can be measured, and is shown in the left figure of figure 1.3. In the complex plane, a change in the radius  $\delta A$  and in phase  $\delta\theta$  can be seen, which can be seen in the right figure of figure 1.3. The measurement of  $\delta A$  is called amplitude read-out and of  $\delta\theta$  is called phase read-out.

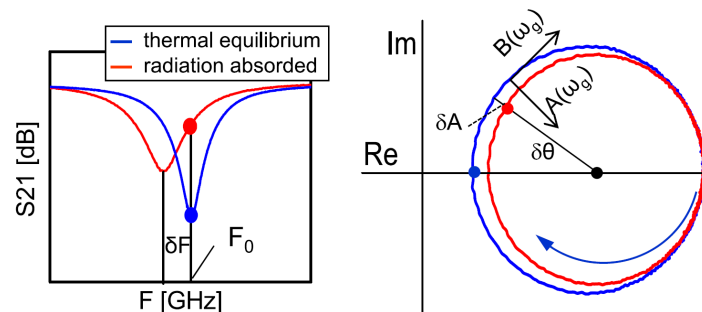


Figure 1.3: Microwave transmission and the effect of the absorption of radiation. An incoming photon breaks Cooper pairs, shifting the resonant frequency by  $\delta F$  and decreasing the depth of the resonant dip (left figure). The right figure show the same results, but in the complex plane. Here, a change in amplitude  $\delta A$  and a change in phase  $\delta\theta$  can be seen. The blue lines indicate the situation in equilibrium and the red lines the change due to incoming radiation. Figure from [14].

### 1.2.3 Multiplexing

Readout multiplexing is the technique to read out multiple detectors using a single read-out circuit, thereby minimizing electronics and read-out wiring. MKIDs are read out using frequency domain multiplexing (FDM), where each MKID resonance frequency is different by design, with the result that each detector can be read out at a different (microwave) frequency. Every KID antenna is connected with a coupler to the feedline (the coupling to the main feed line can be seen in the bottom right corner of figure 1.5). A single line can be used to read out up to 10,000 detectors. Every KID will create a dip in the transmission at their unique resonant frequency, creating an overall transmission shown in figure 1.4. The frequency of the FDM is often around 6-8GHz, with subbands at every MHz. Due to FDM, KIDs do not require complex cryogenic multiplexing electronics [15].

High-speed read-out of sub- $\mu$ s has been shown for KIDs with a per-resonator bandwidth of 1.2MHz [16]. Observations with the 30-meter telescope at Pico Veleta, Spain, have been made with a multiplexed KID array [17]. For 2015 a dual-band 5000 pixel NIKA2 camera at 1.25mm and 2.14mm is announced [18]. Furthermore, the DESHIMA is an array of 5000-10000 KIDs with an on-chip filterbank to instantaneously observe the entire submillimeter band of 320-950GHz [19].

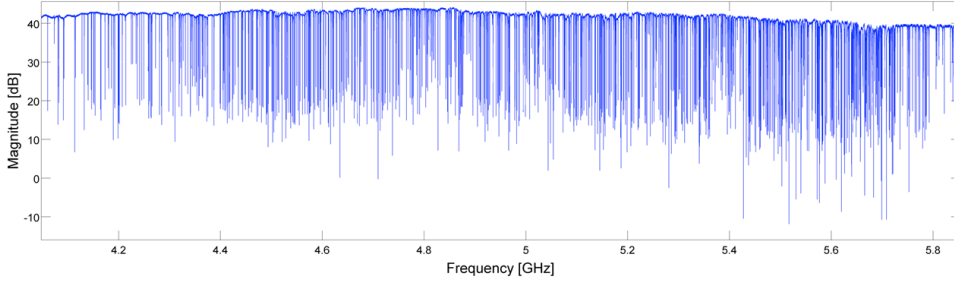


Figure 1.4: Microwave transmission of a multiplexer feed line, with all the dips (or rather spikes) representing one MKID at its resonant frequency.

### 1.2.4 Hybrid

A hybrid MKID is a combination of NbTiN and Al superconductors for the KIDs. NbTiN for the low noise and Al for its high sensitivity. The hybrid design presented in [20] is photon noise limited in phase and amplitude readout for loading levels of 100fW. An image of the design can be seen in figure 1.5. This design is capable of a simultaneous readout of 1800 pixels in perfect conditions, which opens the door for hybrid NbTiN-Al KIDs for astronomical imaging and spectroscopy [20].

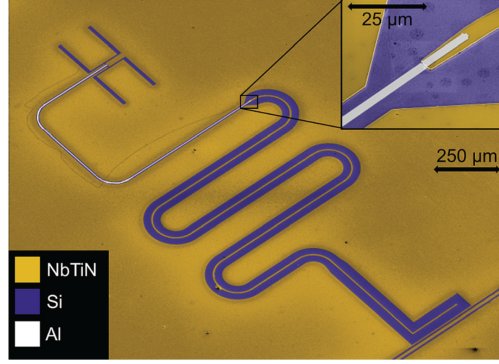


Figure 1.5: Scanning electron micrograph of antenna-coupled hybrid design from Janssen et al. (2013), where a wide NbTiN CPW is used to minimize TLS-noise and a central line to the antenna made from thin Al for its high sensitivity. Figure from [20].

## 1.3 Performance of a KID

The performance of a MKID is limited in terms of the Q-factor and noise. To reach background limited photon detection, the noise performance must be limited by intrinsic noise sources, which means the output signal of the detector is a direct amplification of the input signal (photons). This means all excess noise sources must be reduced if possible. This section covers all the most prevalent limitations on the performance of a KID.

### 1.3.1 Q-factor

The Q-factor determines the width of the dip of the microwave transmission. When the Q-factor is higher, the width of the dip, expressed as the full width half maximum (FWHM), is lower. This effect is illustrated in figure 1.6. Due to multiplexing every KID has a certain bandwidth, and by increasing the Q-factor (in the design) the bandwidth can be reduced and more KIDs can be placed per frequency band. The coupler Q-factor  $Q_c$  is the Q-factor due to the coupling from the antenna to the main line. The internal Q-factor  $Q_i$  is the Q-factor due to the performance of the KID, and  $Q_i$  is therefore sensitive to temperature and internal power  $P_{int}$ .

The relationship between the minimum of the dip  $S_{21,min}$  and the Q-factor is expressed in equation 1.1:

$$S_{21,min} = \frac{Q_c}{Q_i + Q_c} \quad (1.1)$$

wherein  $S_{21,min}$  is the minimum of the microwave transmission,  $Q_c$  is the coupling Q-factor and  $Q_i$  is the internal Q-factor.

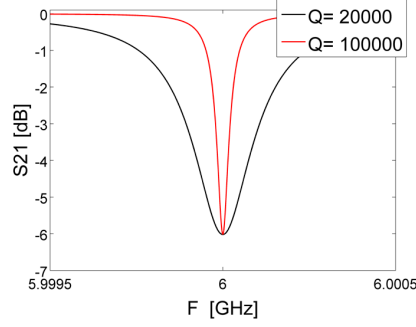


Figure 1.6: Microwave transmission  $S_{21}$  for Q-factor 20000 and 100000 at resonant frequency. When the Q-factor becomes higher, the width of the dip becomes smaller.

### 1.3.2 Photon noise

A fundamental noise any photon-detector will have is photon noise. A light source, such as an astronomical object, emits photons. These photons are emitted at random times, and therefore the photon flux can change with time. These fluctuations cause a noise called photon noise. Photon noise is always observed, at high and low photon fluxes. However, when the photon arrival rate is faster than the detector time constant you cannot see individual photons. The limit of the NEP caused by the photon noise can be seen in figure 1.7 (blue dashed line).

### 1.3.3 Generation-recombination noise

Generation-recombination noise (GR-noise) is the noise due to the fluctuation in the recombination and generation of the Cooper pairs and quasiparticles in the superconducting detector. GR-noise is a thermal noise source, driven by the amount of quasiparticles excitations in the system. The inductance of the detector is dependent on the amount of quasiparticles, and because the quasiparticles don't instantaneously generate and recombine into a Cooper pair a GR-noise is always present. The noise is thermal, and increases as the temperature increases. The GR-noise and the photon noise are the fundamental limits in terms of sensitivity [21,22]. Both the photon noise limit (blue dashed line), and the GR-noise limit (red dashed line) for the sensitivity are shown in figure 1.7.

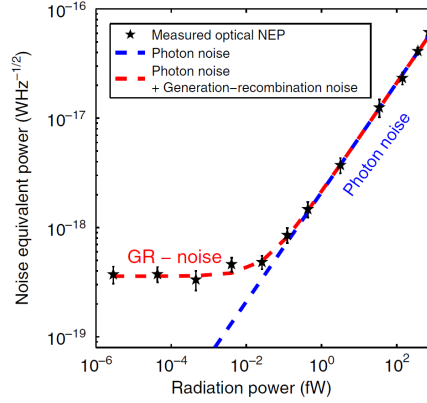


Figure 1.7: Optical sensitivity (NEP) as a function of radiation power. Above 0.1fW the NEP is photon noise limited, and below 0.1fW the NEP is GR-noise limited. Figure from [22].

### 1.3.4 Two-level system noise

A two-level system (TLS), also known as a two-state quantum system, is a system which is in a superposition of two quantum states. A well known example is the superposition of an electron in orbit of the ground state and the first excited state, or the superposition of the spin ( $\uparrow$  ( $S_z = \hbar/2$ ) and  $\downarrow$  ( $S_z = -\hbar/2$ )) of an electron.

These TLSs cause noise, because they can absorb and release energy. The hypothesis that TLS noise is present in KIDs is supported by experiments that show a dependence on the internal power  $P_{int}$  [23].

TLS reduces the performance of a KID, as it can be larger than the photon or GR noise. If this is the case the detector is limited by excess noise, and not anymore by intrinsic noise sources (photon noise, GR noise).

Some research has been conducted on the influence of TLS on noise and loss. Some conclusions of this research are:

- TLS noise is a fluctuation in the dielectric constant  $\epsilon$ . KID TLS phase noise  $\propto (4Q)^2$ , just as the photon noise.
- The TLS noise [24] and losses [25] decrease for higher temperatures. However, other noise sources (GR-noise) increase with higher temperatures, so still a low temperature is preferred.
- TLS exist mostly in surface layers at the metal-air interface or at the metal-substrate interface [25, 26].
- The internal power dependency of the frequency noise can be characterized as  $S_{\delta f}/f_r^2 \propto P_{int}^{1/2}$ , as described in [27].

- The TLS losses and noise decrease for wider CPW's and microstrips. The frequency noise  $S_{\delta f}/f_r^2$  has a dependency on the total width  $s_r$  of the CPW, expressed as  $S_{\delta f}/f_r^2 \propto s_r^{-1.58}$  [27], which can be seen in figure 1.8.
- A  $S_{\delta f}/f_r^2 \propto s_r^{-0.69 \pm 0.03}$  dependency has been observed for Al on SiN membrane microstrips in [28].

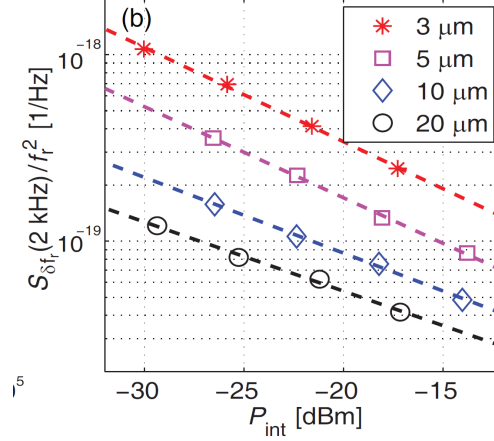


Figure 1.8: Frequency noise plotted for different internal powers  $P_{int}$ , for different total widths of the CPW. Figure from [27].

### 1.3.5 System noise

When reading out the signal of a MKID the readout chain will not be perfect. The noise from this readout system is called system noise. This noise is normally expressed with an effective noise temperature  $T_N$ . The system noise can be reduced to a minimum by using state of the art cryogenic amplifiers and “outboard” amplifiers.

The total phase noise is expressed as:

$$S_\theta = \frac{k_B T_N}{P_{read}} \left( \frac{1}{\left( \frac{1 - S_{21,min}}{2} \right)} \right)^2 \quad (1.2)$$

wherein  $S_\theta$  is the phase noise,  $k_B$  the Boltzmann constant,  $T_N$  the noise temperature (with a typical value of  $T_N \approx 4$  K),  $P_{read}$  the read-out power and  $S_{21,min}$  the depth of the transmission dip (as can be seen on the left in figure 1.3). The noise temperature  $T_N$  is a measure of the system noise.

To give an impression on the effect of TLS-noise, GR-noise and the amplifier noise on amplitude and phase measurements, an overview of all the influences is presented in figure 1.9. Ideally, a detector only sees photon noise, but from the figure it is clear that the phase noise is dominated

by excess TLS-noise. The noise has a  $1/f$  frequency dependency and is rolled off by the detector time constant of  $\sim 100\text{kHz}$ .

Phase read-out gives the largest response, but also suffer from excess noise, which limits the sensitivity [29].

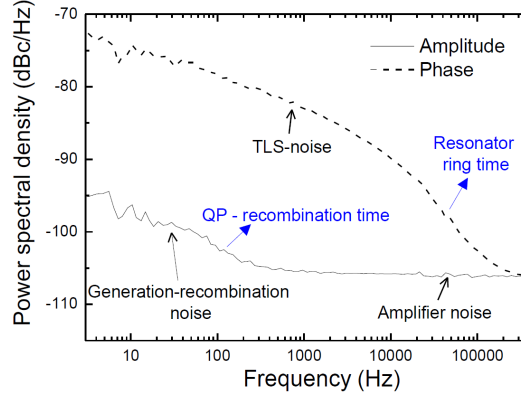


Figure 1.9: Amplitude and phase power spectral density as a function of frequency of an Aluminium CPW at 120mK. All noise sources are indicated in black and the causes of that noise in blue. Figure from [11].

## 1.4 KID Design

The most common resonator designs are the microstrip and the co-planar waveguide. All designs have their pro's and cons, and therefore even hybrid design which utilize multiple geometries are considered.

### 1.4.1 Co-planar waveguide (CPW)

There are two types of geometries which we are interested in: The Co-planar waveguide (CPW) and the microstrip. The CPW is a type of electrical transmission line which is used to convey microwave-frequency signals. The left schematic in figure 1.10 shows the basic geometry of a CPW. The area marked as “ground” is in all our experiments Aluminium.

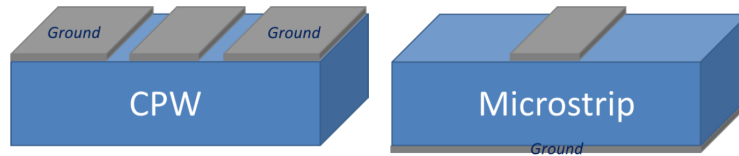


Figure 1.10: Left: Cross section of a CPW. Right: Cross section of a microstrip. Figure from [28].



### 1.4.2 Microstrip

The microstrip is also a electrical transmission line for microwave-frequency signals. The geometry is different from a CPW and can be seen on the right in figure 1.10. A microstrip is a non-planar geometry.

### 1.4.3 Silicon on insulator (SOI)

Silicon on insulator (SOI) is a type of layered silicon-insulator-silicon substrate, which is an alternative to regular Silicon substrates. SOI substrates have a lot of advantages to regular Si substrates such as separating the source and drain in  $p$ - $n$  junctions, reducing power consumption while maintaining performance and many more [30]. In this research the insulator is silicon dioxide ( $\text{SiO}_2$ ), but sapphire is also used in semiconductor devices. SOI is often implemented to minimize parasitic capacitance, which exists when two electric components are near to each other. By changing the depth of the insulating layer the parasitic inductance can be tuned. A CPW on SOI at 32GHz has been shown to have similar characteristics as the same structure on a high resistivity silicon substrate [31].

## 1.5 Outline of thesis

The main thesis is: What are the differences in noise and Q-factor for different resonator geometries; such as a Al microstrip on Si, Al CPW on Si and Al CPW on SOI. A SOI-wafer has been used, which allows crystalline dielectric Si ([1 0 0]-plane) with good noise properties. This question has been examined numerically and experimentally.

In the numerical analysis three geometries are analyzed: the Al on  $5\mu\text{m}$  Si microstrip, Al on  $5\mu\text{m}$  Si CPW and Al on SOI CPW. The Al on  $5\mu\text{m}$  Si microstrip model has no direct relationship to the thesis, but can serve as a reference for future measurements of an Al on SOI microstrip. The Al on  $5\mu\text{m}$  Si CPW served as a reference for the Al on SOI CPW. The differences between the models give insight in the influence of the buried oxide layer on the performance.

In the experimental analysis two geometries are analyzed: the Al on  $5\mu\text{m}$  Si microstrip and Al on SOI CPW. The measurements will give insight in the performance of a microstrip. The Al on SOI CPW can be compared with a NbTiN on Si CPW in [28] and the aluminium parallel plate capacitor on SOI in [32].

The results from the numerical analysis and experimental analysis can be compared. The numerical analysis gives insight in the source of the loss and noise, and the experimental analysis gives quantitative results which can be compared to other literature.

## Chapter 2

# Numerical analysis

In order to get an impression of the performance of the measured KIDs (as described in chapter 3 and 4) a theoretical study on the performance of the KIDs in terms of noise, losses and the Q-factor is performed. Three resonator geometries are analyzed: a 100nm Al on 5 $\mu$ m Si microstrip, a 100nm Al on 5 $\mu$ m Si CPW and a 100nm Al on SOI CPW.

The theoretical study has been carried out in the numerical simulation software COMSOL MULTIPHYSICS [33]. The software calculates in finite elements the electromagnetic fields, given the geometry and material features of the KIDs. From the electromagnetic fields, a theoretical prediction can be made of the noise, loss and Q-factor of the specific KID.

As a starting point I used the COMSOL model made by Werner Daalman, which he used for his numerical analysis for his research on the performance of KIDs in [28], which treats the metal regions as superconductors using a theory of superconductivity.

### 2.1 Theoretical framework

The model is based on a few theories, and some assumptions have been made. Instead of assuming the metal regions to be perfect metals, the Mattis-Bardeen theory of superconductivity [34] is used for the Aluminium superconducting regions to calculate the complex conductivity. This conductivity was calculated in MATLAB [35], and then used as a variable input for COMSOL. In COMSOL the so-called *Electromagnetic Waves, Frequency Domain* toolbox was used. In the model COMSOL calculated equations 2.1 and 2.2.

$$\nabla \times \frac{1}{\mu_r} (\nabla \times E) - k_0^2 e_r E = 0 \quad (2.1)$$

This is the Helmholtz equation, wherein  $\mu_r$  is the relative permeability,  $\vec{E}$  the electric field vector,  $k_0$  the free-space wavenumber and  $e_r$  the electric displacement field defined as  $e_r = e'(1 - j \tan \delta)$ . Here,  $e'$  is the relative permittivity and  $\delta$  the loss tangent.

The second equation is:

$$\vec{E}(x, y, z) = \tilde{E}(x, y)e^{-ik_z z} \quad (2.2)$$

This is the electromagnetic wave equation, wherein  $\vec{E}$  is the electric field vector,  $k_z$  the wave number and  $z$  the spatial coordinate.

Both differential equations are solved by COMSOL for every mesh-area, using the constraints of the boundaries, material properties and geometry. These will be described in the next section.

## 2.2 Assumptions and parameters

The assumptions are represented in the model as parameters or boundary conditions for the differential equations 2.1 and 2.2. The frequency at which the model works is 600GHz, because COMSOL causes meshing problems at the frequencies around 6GHz, due to the small system size versus wavelength ratio. The results do not change significantly between 6GHz and 600GHz [28]. The metal is modeled as a superconductor, instead of using a Perfect Electric Conductor (PEC) model.

### 2.2.1 Boundaries

A few boundaries can be discerned in the geometry. Only one half of the geometry is modelled, because the electric fields are assumed to be symmetric on both sides of the CPW or microstrip. The symmetry axis corresponds to the left boundary of the system box. Therefore, no current can flow through this boundary, and the boundary is then a Perfect Magnetic Conductor (PMC) [36], which satisfies the condition:

$$\vec{B} \times \hat{n} = \vec{0} \quad (2.3)$$

wherein  $\vec{B}$  is the magnetic field vector, and  $\hat{n}$  the normal perpendicular to the interface.

The metal boundaries (metal-air and metal-substrate) will behave like a perfect metal. So no current will flow away from the surface to the interior, and the electric field will be perpendicular to the boundary. The boundary is then a Perfect Electric Conductor (PEC) [36], and satisfies the condition:

$$\vec{E} \times \hat{n} = \vec{0} \quad (2.4)$$

wherein  $\vec{E}$  is the electric field vector, and  $\hat{n}$  the normal perpendicular to the interface.

At last, a box is placed around the system which also must satisfy boundary conditions. Ideally, the distances of the system boundaries are very large (and in theory at infinity). To be sure no current will flow out of the system box, the system box is also modelled as a PMC. The outer system boundaries thus also satisfy equation 2.3.

## 2.2.2 Material properties

Four different materials are present in the models: Air (or vacuum), superconducting Aluminium, Silicon and Silicon Oxide. Their used properties in the model are summed up in table 2.1, and references are placed at corresponding columns or cells (after value). The values for the superconducting Aluminium were suggested in COMSOL example “Superconducting wire”.

Table 2.1: Material properties of Air, superconducting Al, Si and SiO<sub>2</sub>: Relative permittivity  $\epsilon_r$ , relative permeability  $\mu_r$  and loss tangent  $\delta$ .

| Material<br>Property | Air  | Al   | Si          | SiO <sub>2</sub> [37] |
|----------------------|------|------|-------------|-----------------------|
| $\epsilon_r$         | 1    | 1    | 11.7 [28]   | 3.9                   |
| $\mu_r$              | 1    | 1    | 1 [28]      | 1                     |
| $\delta$             | n.a. | n.a. | 5.6e-6 [38] | 0.001                 |

## 2.3 Geometry

### 2.3.1 Microstrip: Al on 5 $\mu$ m Si

For the microstrip, a parametric sweep of different linewidths was done. The modeled widths are: 3.0 $\mu$ m, 4.0 $\mu$ m, 6.0 $\mu$ m, 8.0 $\mu$ m, 11 $\mu$ m, 16 $\mu$ m, 22 $\mu$ m and 30 $\mu$ m. The geometry consisted of five layers enclosed in a system box with a width of 250 $\mu$ m and height of 56.25 $\mu$ m. The COMSOL system geometry can be seen in figure 2.1(a).

The layers from top to bottom are: air, superconductor, substrate, superconductor and air. The first superconductor is the microstrip: a small line of 100nm superconducting Aluminium on top of the substrate. The substrate is 5 $\mu$ m thick Silicon. The second superconductor layer is the ground, and is a 100nm superconducting Aluminium layer. The last layer is another air layer. A schematic of the geometry can be seen in figure 2.1(a).

### 2.3.2 CPW: Al on 5 $\mu$ m Si

The Al on 5 $\mu$ m Si CPW had is the same geometry as the Al on 5 $\mu$ m Si microstrip, except for the CPW pattern on top of the substrate instead of the microstrip pattern. Only one gapwidth was modelled:  $g = 3\mu$ m. The geometry consisted of four layers, from top to bottom: air, 100nm superconducting Al CPW structure, the 5 $\mu$ m Si substrate and another air layer. A schematic of the COMSOL system geometry can be seen in figure 2.1(b).

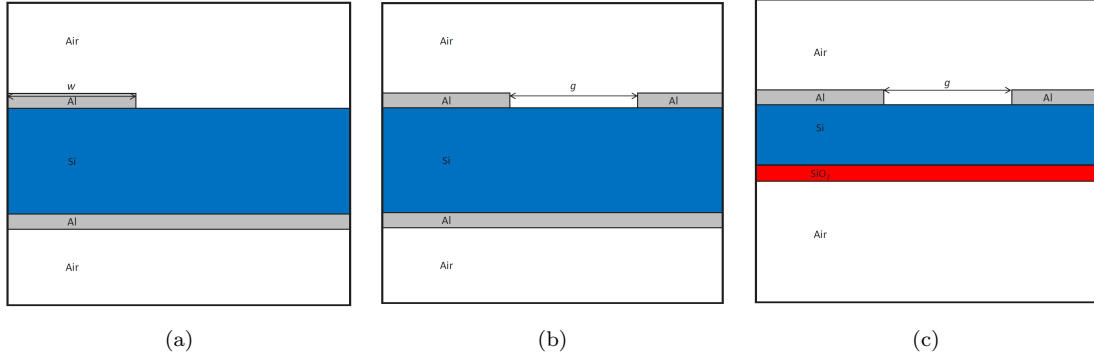


Figure 2.1: System geometries as implemented in COMSOL. Only the right half of the structure is shown (as opposed to figure 1.10): (a) Schematics of the Al on  $5\mu\text{m}$  Si microstrip geometry:  $w$  is the linewidth of the microstrip and the different layers are labeled. (b) Schematics of the Al on  $5\mu\text{m}$  Si CPW geometry:  $g$  is the gapwidth of the CPW and the different layers are labeled. (c) Schematics of the Al on SOI CPW geometry:  $g$  is the gapwidth of the CPW and the different layers are labeled. Not to scale.

### 2.3.3 CPW: Al on SOI

For the CPW, two parametric sweeps were performed. One to sweep through the different widths, and one to sweep through different system box sizes (for reasons explained in the next section).

The geometry consisted of five layers enclosed in a system box with varying widths and heights. The layers from top to bottom are: air, superconductor, substrate, insulator and air. The first superconductor layer is the CPW structure, two lines of 100nm superconducting aluminium on top of the substrate. The substrate is  $4\mu\text{m}$  thick Silicon. Because the modelled substrate is SOI, the next insulator layer consists of  $1\mu\text{m}$  thick  $\text{SiO}_2$ . A schematic of the COMSOL system geometry can be seen in figure 2.1(c).

## 2.4 Mesh

The size system box of the microstrip model is straightforward, and sufficiently large to dissolve all the electric fields to 0 at the edges. To add detail to the calculations a denser mesh is added at the edges of the metal and all the boundaries (metal-air, metal-substrate and substrate-ground). A detailed image of the mesh for the microstrip can be seen in figure 2.2.

For the CPW, such a straightforward method can unfortunately not be used. The size of the system box influences the nodes which COMSOL finds for CPW's, and even finds non-physical nodes at some system box sizes. To resolve this issue, the electric fields are calculated with different system sizes. The width and height of the model were varied as a factor of the total minimum width, defined as  $2g + w$ , wherein  $g$  is the gapwidth and  $w$  the linewidth. The factors for the system width were 1.2, 1.5, 2, 5, 10, 20, 50, 100; and the factors for the system height were

1.5, 3, 5, 10, 20. All possible combinations were calculated, and the most probable system size was used for further calculations (for a complete description of this determination of the “best” size, see Appendix of [28]).

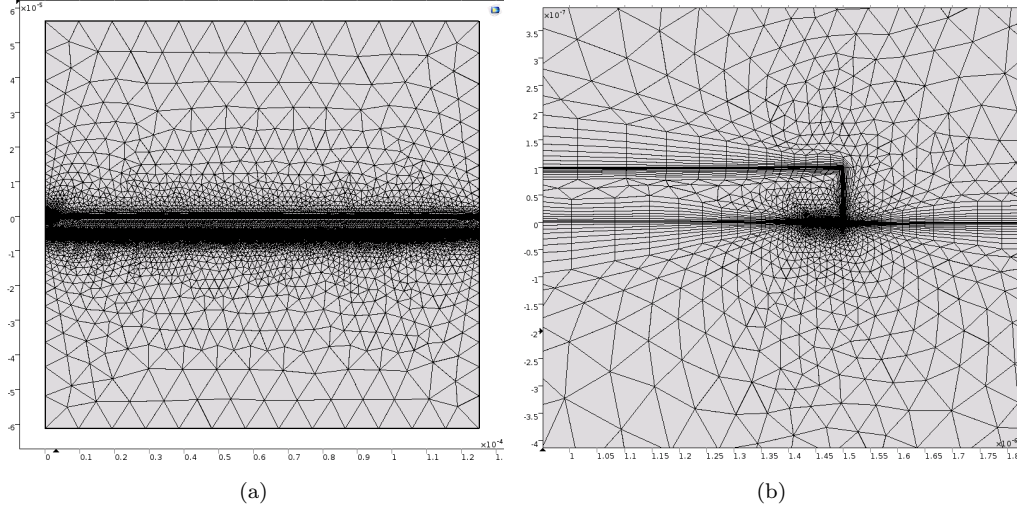


Figure 2.2: (a) The whole system box, with mesh refinement around the interfaces. (b) Close-up of the superconductor-substrate interface, with mesh refinement around the corners and interfaces. All distances in meters.

## 2.5 Post-processing

The post-processing was carried out in MATLAB [35] and entailed the calculation of the participation ratios, noise and Q-factor. The electric field and some geometry parameters are exported from COMSOL into MATLAB.

The Q-factor was calculated using an expression from [25]:

$$\frac{1}{Q} = 0.002 \frac{\epsilon_{sdi} t_{sdi} \int \frac{|E|^2}{\sqrt{1+|E|^2/E_s^2}} ds_{sdi}}{W'} \quad (2.5)$$

wherein  $\epsilon_{sdi}$  is the dielectric constant,  $t_{sdi}$  the surface layer thickness (3nm),  $|E|^2$  the norm of the electric field,  $E_s$  the saturated electric field (values of 5 and 0.05kV/m for surface dielectrics on Si and NbTiN [25], no value for Al found) and  $s_{sdi}$  the width of the system over which the integral is taken. Power  $W'$  is defined as [38]:

$$W' = \frac{\int \epsilon |E|^2 dA_{system}}{2} \quad (2.6)$$

wherein  $Q$  is the Q-factor of the specific domain,  $\epsilon$  is the dielectric constant,  $|E|^2$  the norm of the electric field and  $A_{system}$  the surface of the whole system over which the integral is taken.

The fraction in equation 2.5 is the participation ratio of that interface, in this case the surface dielectric layer. It is expressed as a fraction of the total power  $W'$  as defined in 2.6. The frequency noise was calculated using an expression from [39]:

$$\frac{S}{f_r^2} = \frac{\kappa(\nu, f, T)}{4E_s l} \frac{t \int \frac{|E|^4}{\sqrt{1+|E|^2/E_s^2}} ds}{W'^2} \quad (2.7)$$

wherein  $\frac{S}{f_r^2}$  is the normalised frequency noise,  $\kappa$  the noise spectral density coefficient,  $t$  the thickness of the layer,  $|E|^2$  the norm of the electric field,  $s$  the width,  $E_s$  the energy,  $l$  the resonator length and  $W'$  the total power (as defined in 2.6).

The noise spectral density coefficient  $\kappa$  in equation 2.7 is dependent on variables  $\nu$ ,  $f$  and  $T$ , therefore we can write:  $\kappa = \kappa(\nu, f, T)$  [24]. For the numerical analysis  $\kappa(\nu, f, T) = \kappa(500\text{Hz}, 5\text{GHz}, 120\text{mK}) = 5 \cdot 10^{-26} [\text{Vm}^2/\text{Hz}] \epsilon_0^2$ , for all dielectric surfaces ( $\text{SiO}_2$  and  $\text{Si}$ ).

All interfaces (metal-air, metal-substrate and substrate-ground) are exported on a grid with spacing between points  $\Delta x$  and  $\Delta y$  constant. The fields are evaluated  $3 \cdot 10^{-3}$  nm above the interface boundary, because COMSOL averages the fields *on* the boundary from both sides.

The expressions for the Q-factor and the normalised frequency noise are calculated in MATLAB at five different interfaces: the metal-air, metal-edge, metal-substrate, substrate-air and dielectric bulk interfaces. An overview of the different interfaces can be seen in figure 2.3.

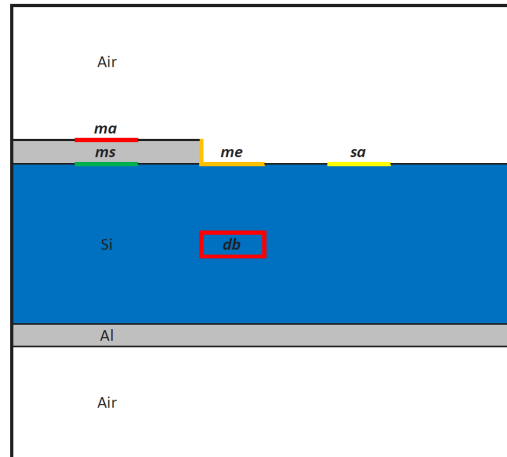


Figure 2.3: Overview of the different interfaces where the expressions are calculated. The names of the interfaces are above the indicated interfaces. Metal-air (ma) is red, metal-substrate (ms) is green, metal-edge (me) is orange, substrate-air (sa) is yellow and the dielectric bulk (db) is indicated with a red box.

## 2.6 Results

### 2.6.1 Al on 5 $\mu$ m Si microstrip

The results of the 100nm Al microstrip on 5 $\mu$ m Si are presented in four figures.

The Q-factor as a function of the internal power  $P_{int}$  per interface is presented in figure 2.4. The different interfaces are metal-air (ma), metal-edge (me), metal-substrate (ms), substrate-air (sa) and dielectric bulk (db). The dashed lines show the 300nm NbTiN microstrip on 4 $\mu$ m Si ( $w = 3\mu$ m) model results from [28]. The results are very similar as the 300nm NbTiN microstrip on 4 $\mu$ m Si ( $w = 3\mu$ m) model results, as expected.

The total Q-factor of the resonator is limited by the lowest Q-factor contribution, in this case the ms interface at  $Q \approx 10^5$ . The 300nm NbTiN and 100nm Al microstrip will have a comparable Q-factor performance, due to the limiting low Q-factors ( $\sim 10^5$ ) of the ms, sa and db interfaces. The ma-interface yields a lower Q-factor compared to [28], and the me-interface yields a higher Q-factor compared to [28]. The higher Q-factor at the me-interface can be attributed to the fact that the metal layer is thinner, thus the losses in the edges are lower.

The noise as a function of the internal power  $P_{int}$  per interface is presented in figure 2.5. The dashed lines show the 300nm NbTiN microstrip on 4 $\mu$ m Si ( $w = 3\mu$ m) model results from [28]. Clearly, the dielectric bulk dominates the noise and the 1 $\mu$ m difference in substrate thickness has little effect on the noise. The metal-air and metal-edge noise of the 100nm Al microstrip has higher noise levels compared to the 300nm NbTiN microstrip (5dBc/Hz higher for the metal-air interface and 2dBc/Hz higher for the metal-edge interface).

The Q-factor and the central linewidth are presented in figure 2.6. The Q-factor of the metal-edge and substrate-air interfaces show a weak dependency on the central linewidth.

The noise and the central linewidth are presented in figure 2.7. The metal-air interface shows some strange jumpy behaviour, which is likely a meshing problem in COMSOL. All the other interfaces show a clear dependency on the central linewidth: The noise decreases at all interfaces when the central linewidth of the microstrip increases. The dielectric bulk dominates the noise.



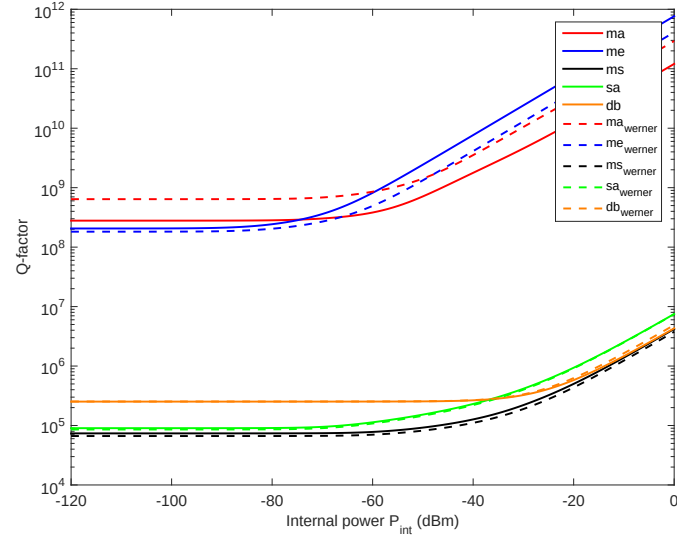


Figure 2.4: Internal power  $P_{int}$  against Q-factor for central linewidth  $3\mu\text{m}$  compared to results from [28] (dashed lines), for different interfaces (ma is metal-air, me is metal-edge, ms is metal-substrate, sa is substrate-air and db is the dielectric bulk).

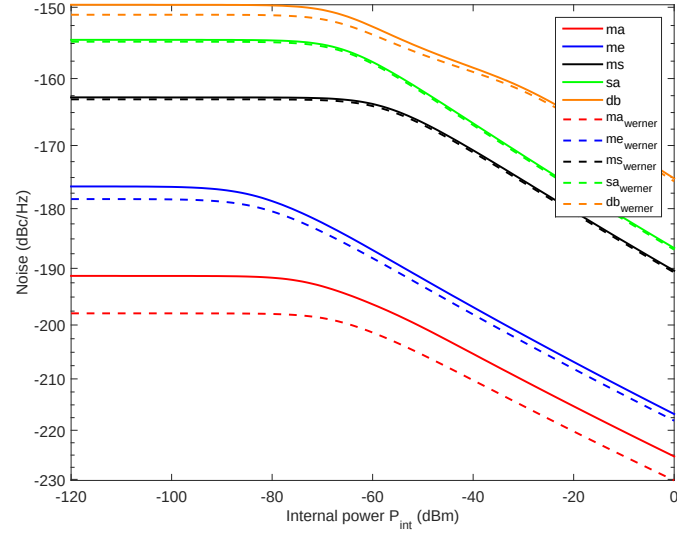


Figure 2.5: Internal power  $P_{int}$  against noise for central linewidth  $3\mu\text{m}$  compared to results from [28] (dashed lines), for different interfaces (ma is metal-air, me is metal-edge, ms is metal-substrate, sa is substrate-air and db is the dielectric bulk).

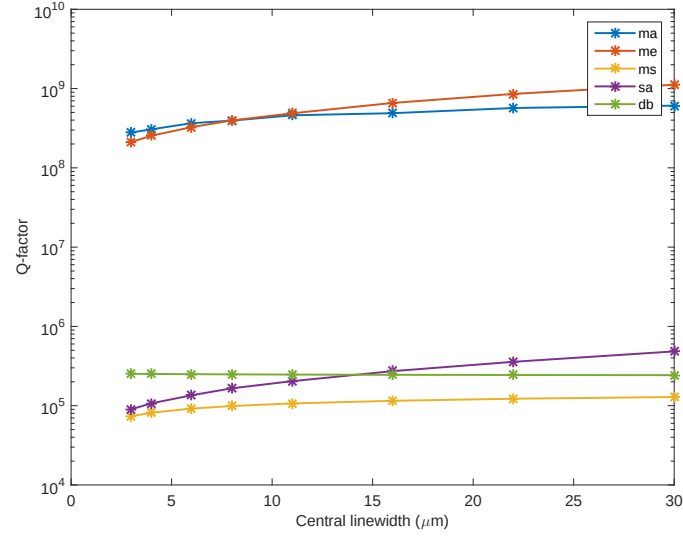


Figure 2.6: Central linewidth  $w$  against Q-factor, for different interfaces (ma is metal-air, me is metal-edge, ms is metal-substrate, sa is substrate-air and db is the dielectric bulk).

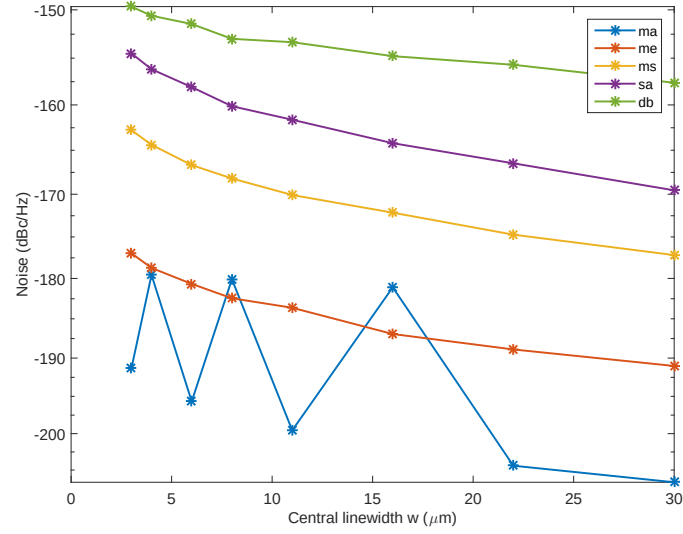


Figure 2.7: Central linewidth  $w$  against noise, for different interfaces (ma is metal-air, me is metal-edge, ms is metal-substrate, sa is substrate-air and db is the dielectric bulk).

## 2.6.2 Al on 5 $\mu$ m Si CPW

The results of the the 100nm Al on 5 $\mu$ m Si CPW are presented in two figures.

The Q-factor as a function of the internal power  $P_{int}$  per interface is presented in figure 2.8. The dashed lines show the results from the Al on 5 $\mu$ m Si microstrip from subsection 2.6.3. Both the microstrip and the CPW have a linewidth of 3 $\mu$ m.

The noise as a function of the internal power  $P_{int}$  per interface is presented in figure 2.9. The dashed lines show the results from the Al on 5 $\mu$ m Si microstrip from subsection 2.6.3. Both the microstrip and the CPW have a linewidth of 3 $\mu$ m.

As can be seen, the performance in terms of Q-factor are almost identical for the CPW and microstrip. The microstrip has a slightly higher Q-factor at the metal-edge and metal-air interfaces. The limiting Q-factors in the order of  $10^5$  of the ms, sa and db-interfaces are almost exactly the same for the CPW and microstrip, which will result in a similar Q-factor performance.

The noise is comparable but slightly higher for the CPW for all the interfaces, except the substrate air layer. The metal-edge gives a 8dBc/Hz extra contribution to the noise, compared to the microstrip. Overall, the CPW will have a few dBc/Hz more noise compared to the microstrip.

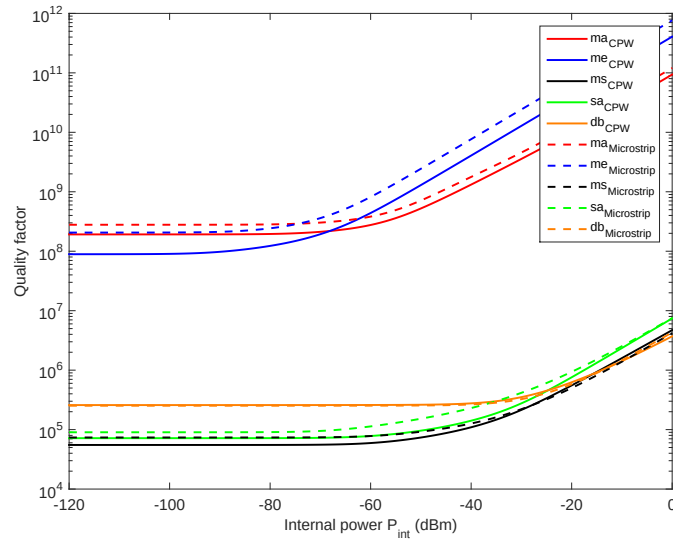


Figure 2.8: Internal power  $P_{int}$  against Q-factor for a linewidth of 3 $\mu$ m compared with results from the Al on 5 $\mu$ m Si CPW with a 3 $\mu$ m linewidth (dashed lines), for different interfaces (ma is metal-air, me is metal-edge, ms is metal-substrate, sa is substrate-air and db is the dielectric bulk).

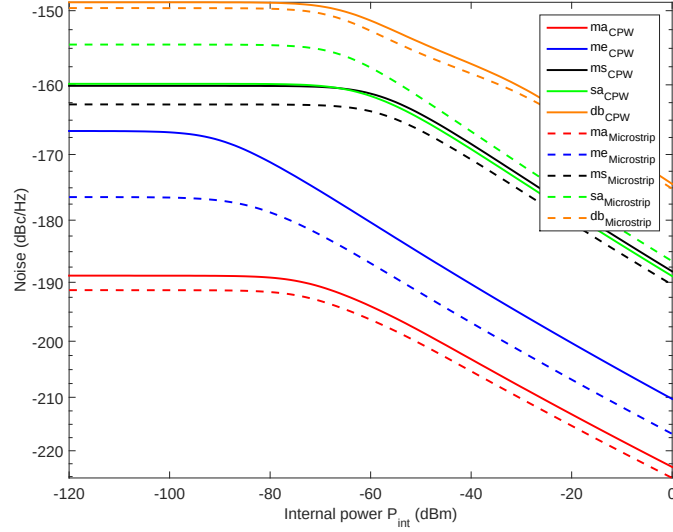


Figure 2.9: Internal power  $P_{int}$  against noise for a linewidth of  $3\mu\text{m}$  compared with results from the Al on  $5\mu\text{m}$  Si CPW with a  $3\mu\text{m}$  linewidth (dashed lines), for different interfaces (ma is metal-air, me is metal-edge, ms is metal-substrate, sa is substrate-air and db is the dielectric bulk).

### 2.6.3 Al on SOI CPW

The Q-factor as a function of the internal power  $P_{int}$  per interface is presented in figure 2.10. The dashed lines show the Al on  $5\mu\text{m}$  Si CPW results. As can be seen, the ms, sa and db-interfaces are the most limiting factors for the total Q-factor with a  $Q \sim 10^5$ . Compared to the Al on  $5\mu\text{m}$  Si CPW there are no great differences in the Q-factor, although a very slight improvement can be seen at the metal-air and metal-edge interfaces. Overall, the Q-factor of the resonator will be limited around  $Q \approx 10^5$ .

The noise as a function of the internal power  $P_{int}$  per interface is presented in figure 2.11. The dashed lines show the Al on  $5\mu\text{m}$  Si CPW results. As with the Al on  $5\mu\text{m}$  Si CPW the dielectric bulk dominates the noise. In contrast the Al on SOI CPW has a 9dBc/Hz higher noise, compared to the Al on  $5\mu\text{m}$  Si CPW. Because for both Si and  $\text{SiO}_2$  the same  $\kappa$  value was used in equation 2.7, the higher noise must be attributed to a change in the participation ratio of the dielectric bulk. In comparison, the metal-air, metal-edge, metal-substrate and substrate-air interfaces show no big ( $< 2\text{dBc/Hz}$ ) difference in noise.

The Q-factor and the central linewidth are presented in figure 2.12. The trend shows very jumpy behaviour, which can be attributed to the meshing error and problems in COMSOL (see section 2.4). The Q-factor of all interfaces show a weak dependency on the central linewidth.

The noise and the central linewidth are presented in figure 2.13. This data is jumpy, and therefore hard to interpret. The dielectric bulk noise does decrease, when the gapwidth increases.

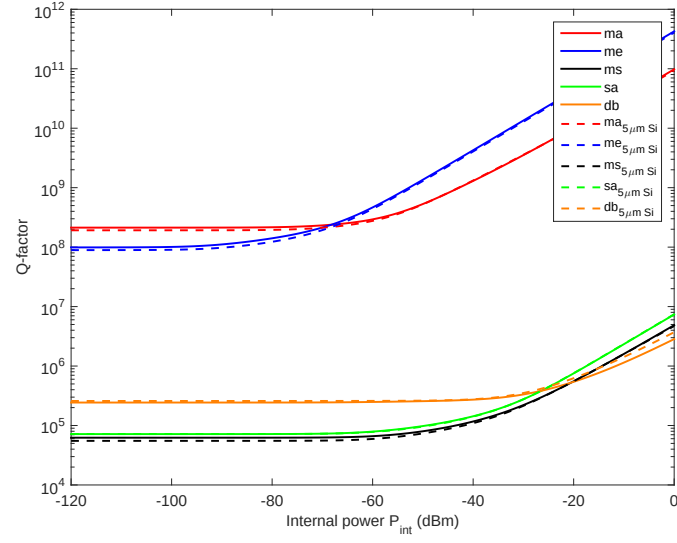


Figure 2.10: Internal power  $P_{int}$  against Q-factor for a gapwidth of  $3\mu\text{m}$  compared with results from the Al on  $5\mu\text{m}$  Si CPW (dashed lines), for different interfaces (ma is metal-air, me is metal-edge, ms is metal-substrate, sa is substrate-air and db is the dielectric bulk).

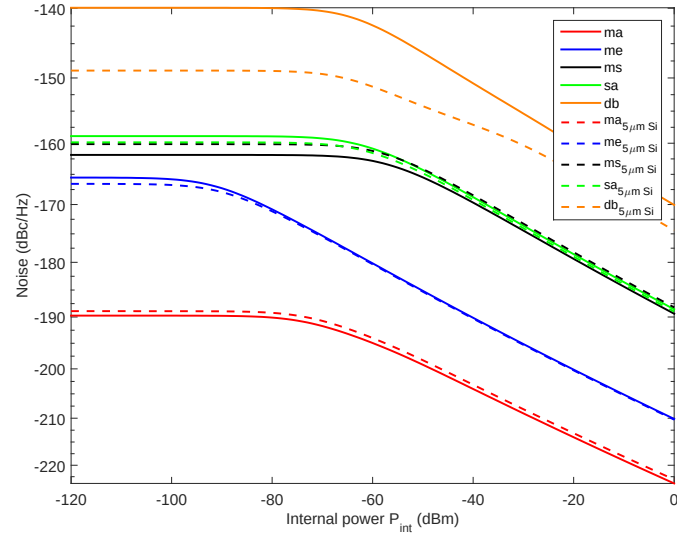


Figure 2.11: Internal power  $P_{int}$  against noise for a gapwidth of  $3\mu\text{m}$  compared with results from the Al on  $5\mu\text{m}$  Si CPW (dashed lines), for different interfaces (ma is metal-air, me is metal-edge, ms is metal-substrate, sa is substrate-air and db is the dielectric bulk).

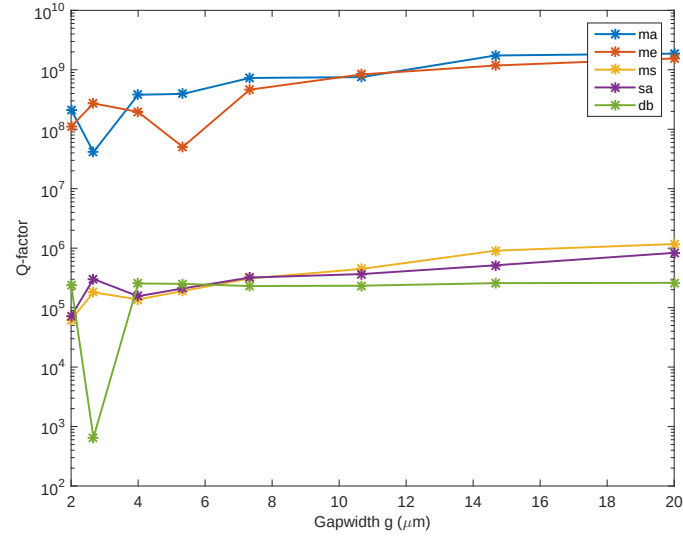


Figure 2.12: CPW gapwidth  $g$  against Q-factor, for different interfaces (ma is metal-air, me is metal-edge, ms is metal-substrate, sa is substrate-air and db is the dielectric bulk).

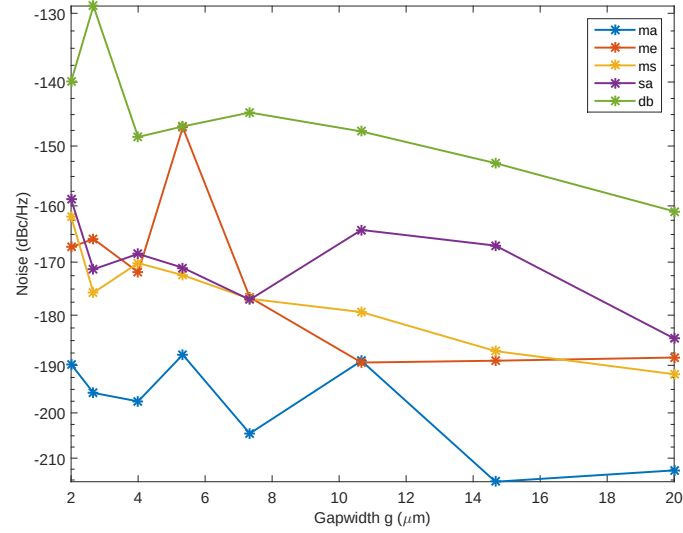


Figure 2.13: CPW gapwidth  $g$  against noise, for different interfaces (ma is metal-air, me is metal-edge, ms is metal-substrate, sa is substrate-air and db is the dielectric bulk).

# Chapter 3

## Experimental setup

The experimental setup was situated at SRON in Utrecht<sup>‡</sup>. This chapter will explain the basics of the experimental setup. For a more detailed and technical description of the experimental setup consult chapter 3 of [11].

### 3.1 Design

#### 3.1.1 Al on 5 $\mu$ m Si microstrip

The Al on 5 $\mu$ m Si microstrip consisted of three layers and its fabrication is based upon a SOI wafer. The top layer is a 100nm aluminium microstrip pattern. The second layer is 5 $\mu$ m crystalline silicon. On the bottom of the silicon layer is a 100nm thick aluminium ground layer. The different widths and their corresponding resonant frequencies are shown in table 4.1. The design is the same as in figure 2.1(a)

#### 3.1.2 Al on SOI CPW

The Al on SOI CPW consisted of four layers. The top layer is a 100nm aluminium CPW pattern. The second layer is a SOI substrate which consists of three layers from top to bottom: 4 $\mu$ m silicon, 1  $\mu$ m silicon dioxide and 300 $\mu$ m silicon. The geometry differs from the simulated geometries in chapter 2.

The CPW's were designed at two frequencies: 4GHz and 6GHz. The 4GHz KIDs have a constant total width, and the design parameters with the corresponding resonant frequencies are presented in table 4.2. The 6GHz KIDs have a varying total width, but a constant ratio between the gapwidth, linewidth and total width. The design parameters and the corresponding resonant frequencies are presented in table 4.3. The 4GHz KIDs will be referred to as the “constant width KIDs”, and the 6GHz KIDs will be referred to as the “varying width KIDs”.

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<sup>‡</sup>SRON Netherlands Institute for Space Research, Sorbonnelaan 2, 3584 CA Utrecht, Netherlands.

## 3.2 Fabrication

The fabrication of the KID is a very delicate process, and was completed in a cleanroom at SRON in Utrecht. Especially due to the thin layer of Si the chip is very fragile.

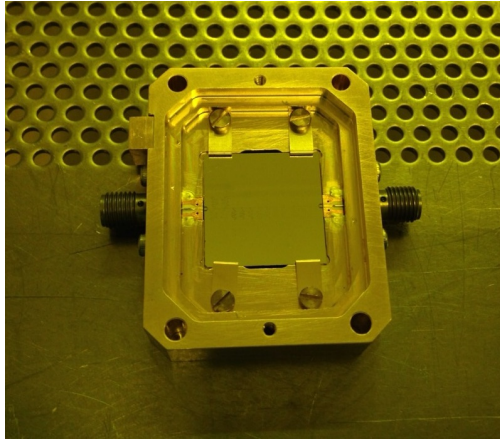


Figure 3.1: The chip in the sample holder: at the left and right of the sample holder are the coax inputs; the chip is mounted to the holder with four clips and bonded at the coax inputs. The antenna-structure of the KIDs can be seen on the chip when studied closely.

The first step of the fabrication process is the production of the wafer, which will serve as a blueprint of the chip. The patterns which are instilled on the wafer are printed, or actually “photographed”, upon the chip. Then, with the process called etching, the material which is redundant is removed, leaving the inverse of the pattern on the wafer on the chip. Then the chip is carefully cleaned, and placed in a holder. An overview of the wafer fabrication is given in Appendix A: Process flow wafer fabrication.

Electrical contact to the chip is made using a wire bonding machine, which works like a soldering iron, but much more accurate. To reduce the inductance multiple wire bonds are made between the holder and the chip. Furthermore, long and short bonds are made to prevent them from breaking when the chip moves with respect to the holder. The chip was examined one last time under a microscope, to check for any anomalies. A picture of the chip in the sample holder can be seen in figure 3.1.

## 3.3 Cryostat and mounting

The cryogenic system is an adiabatic demagnetization refrigerator (ADR) combined with a pulse tube refrigerator by VeriCold Technologies GmbH, as patented in [40]. The cryogenic system contains of four thermal stages: a 70K stage, a 4K stage, a 1K stage and a 100mK stage. The 70K and 4K stages are cooled with a pulse tube refrigerator. The 1K and 100mK stage are cooled with an ADR. With a vacuum pump the pressure in the whole system is brought near



absolute vacuum during the cool down. A picture of the cryostat is shown in figure 3.2(a).

The chip is placed in the 100mK stage and the box in the 1K stage, which hangs suspended on Kevlar wires in the cryostat to minimize thermal exchange. The stages are connected with a thermal bridge, so heat can be transferred from the 100mK stage to the 4K stage during cooling.

The chip is placed inside a sample box, which is placed in a light-tight box. This set-up is called a box-in-box configuration [41]. A representation of the set-up can be seen in figure 3.2(b). The multi-stage shielding is used to minimize stray infrared light which leads to significant losses [41, 42].

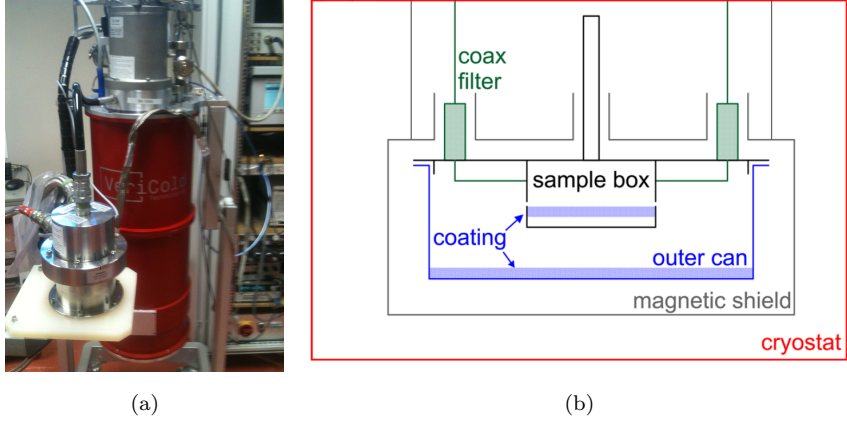


Figure 3.2: (a) The VeriCold 100mK cryogenic system with four thermal stages. (b) Light-tight sample box schematics: the sample box is mounted in an outer can. The inner side of the sample box lid and outer can are coated with a blackbody absorber (blue). The readout lines are filtered (green). The entire 100mK stage is magnetically shielded (grey). Figure from [42] (with minor adjustments).

### 3.4 Measurement

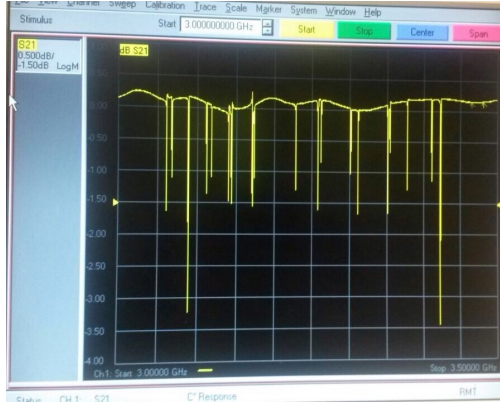
To measure the KIDs they were mounted in the sample box and the cryostat was cooled down to 100mK, by changing the current in the ADR.

A signal generator (Agilent E8257D) generates a microwave signal at the start of the readout circuit, which is immediately split into two. One part serves as a reference for the IQ-mixer (Miteq IRM0218LC1Q), and the other part goes to the KID in the cryostat and back to the IQ-mixer. A Vector Network Analyzer (VNA) is used to measure amplitude and phase to calibrate the system. The VNA has a lower resolution, but a faster sweeping time compared to the synthesizer. When using the VNA you always ground yourself using a wrist band. A complete overview of the electronic circuit of the readout system can be seen in Appendix D: Readout system.

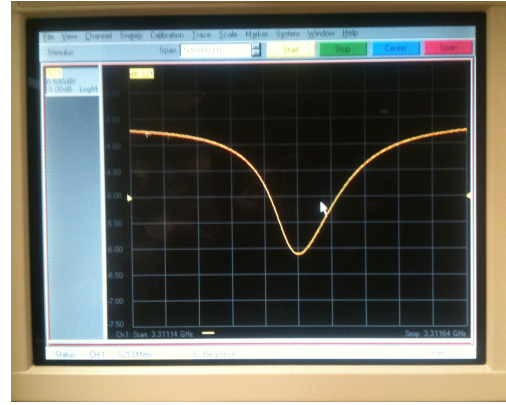
The system is first calibrated at  $T \approx T_c/2$ , because the dips of the KIDs are not visible yet at this temperature. The minimum of the dip is defined in equation 3.1.

$$S_{21,min} = \frac{Q_c}{Q_i + Q_c} \quad (3.1)$$

The KIDs can be detected, because a dip in the transmission will be present at the resonant frequency of the KID, as explained in section 1.2.2. When the sample is cooled down to 100mK the KIDs start to appear as sharp dips at their resonant frequency, as can be seen in figure 3.3(a). When you zoom in at the resonant frequency of a KID, you see a more rounded dip, as can be seen in figure 3.3(b).



(a)



(b)

Figure 3.3: On both figures the x-axis show the frequency (in Hz) around the resonant frequency and y-axis the microwave transmission  $S_{21}$ . (a) Overview of the dips at the resonant frequencies of the KIDs (b) Zoomed in at the resonant frequency of a KID showing a more rounded dip.

## Chapter 4

# Experimental results

### 4.1 Al on 5 $\mu$ m Si microstrip

The measurements were conducted on february 16 2015 at SRON in Utrecht. No KIDs could be found, and therefore no data was yielded. For the sake of completeness the design is presented.

The design of the microstrip was a single 100nm aluminium microstrip on top of a 5 $\mu$ m silicon substrate, with an etch under the microstrip. An aluminium ground layer was on the bottom of the chip. The designed linewidths  $w$  with their corresponding designed resonant frequency  $f_{res}$  can be seen in table 4.1.

Table 4.1: The design parameters of the Al on Si microstrip, measured on 16/2/2015. Width  $w$  is the total width of the microstrip.

|                 |     |     |     |     |     |     |     |     |
|-----------------|-----|-----|-----|-----|-----|-----|-----|-----|
| $f_{res}$ (GHz) | 6.0 | 6.1 | 6.2 | 6.3 | 6.4 | 6.5 | 6.6 | 6.7 |
| $w$ ( $\mu$ m)  | 3.0 | 4.0 | 6.0 | 8.0 | 11  | 16  | 22  | 30  |

### 4.2 Al on SOI CPW

The measurements were conducted on april 23 2015 at SRON in Utrecht. The design parameters and the actual resonant frequency  $f_{res}$  of the Al on SOI CPW of the constant width 4GHz and varying width 6GHz KIDs are presented in table 4.2 and table 4.3, respectively. All KIDs were designed to have a coupler Q-factor  $Q_c = 200000$ .

Table 4.2: The design parameters of the constant width Al on SOI CPW KIDs at 4GHz, measured on 23/4/2015. A '-' means no KID could be found at that frequency.

|                               |      |      |      |      |      |     |     |
|-------------------------------|------|------|------|------|------|-----|-----|
| $Designf_{res}$ (GHz)         | 4.1  | 4.2  | 4.3  | 4.4  | 4.5  | 4.6 | 4.7 |
| $Actualf_{res}$ (GHz)         | 4.16 | 4.28 | 4.41 | 4.52 | 4.59 | -   | -   |
| $w_{line}$ ( $\mu\text{m}$ )  | 21   | 19   | 16   | 12   | 6    | 4   | 2   |
| $w_{gap}$ ( $\mu\text{m}$ )   | 1.5  | 2.5  | 4    | 6    | 9    | 10  | 11  |
| $w_{total}$ ( $\mu\text{m}$ ) | 24   | 24   | 24   | 24   | 24   | 24  | 24  |

Table 4.3: The design parameters of the varying width Al on SOI CPW KIDs at 6GHz, measured on 23/4/2015. A '-' means no KID could be found at that frequency.

|                               |      |       |      |        |        |        |        |     |
|-------------------------------|------|-------|------|--------|--------|--------|--------|-----|
| $Designf_{res}$ (GHz)         | 6.1  | 6.2   | 6.3  | 6.4    | 6.5    | 6.6    | 6.7    | 6.8 |
| $Actualf_{res}$ (GHz)         | 5.87 | 6.07  | 6.34 | 6.52   | 6.69   | -      | -      | -   |
| $w_{line}$ ( $\mu\text{m}$ )  | 3    | 4     | 6    | 8      | 11     | 16     | 22     | 30  |
| $w_{gap}$ ( $\mu\text{m}$ )   | 2    | 2.667 | 4    | 5.333  | 7.333  | 10.667 | 14.667 | 20  |
| $w_{total}$ ( $\mu\text{m}$ ) | 7    | 9.333 | 14   | 18.667 | 25.667 | 37.333 | 51.333 | 70  |

The constant width KIDs underperformed, compared to the varying width KIDs. The dip depth was very shallow, which according to equation 1.1 is due to a low internal Q-factor  $Q_i$ , which is plotted in figure 4.3. The constant width KIDs (shown in blue) have an internal Q-factor in the order of  $10^3$ .

Figure 4.1 shows the difference between a low frequency 4GHz KID (KID 4) with a gapwidth  $w_{gap} = 6\mu\text{m}$  and linewidth  $w_{line} = 12\mu\text{m}$  and a high frequency 6GHz KID (KID 11) with a gapwidth  $w_{gap} = 2.667\mu\text{m}$  and a linewidth  $w_{line} = 4\mu\text{m}$  to illustrate the difference in noise. Also, a plot of the noise on-resonance and off-resonance can be seen in figure 4.2.

The system noise levels are high (with a system noise of -80dBc/Hz). From the expression of the phase noise  $S_\theta$  in equation 1.2, it is clear that when  $S_{21,min}$  increases (and the dip becomes more shallow) this leads to a high  $S_\theta$ , because the expression between brackets goes very fast to high values. For example, a  $Q_i = 5 \cdot 10^3$  leads to a  $S_{21,min} = 0.8$  (using equation 3.1). With a typical noise temperature of  $T_N = 4\text{K}$  and a  $P_{read} = -60\text{dBm}$  this would lead to a very high phase noise  $S_\theta \approx -83\text{dBc/Hz}$  (using equation 1.2).

The result from this effect is that the difference between on resonance noise and off resonance noise is very small (maximum of 5dBc/Hz for phase noise), while you expect a bigger difference due to the TLS noise. KID 11 shows a bigger difference of 10dBc/Hz. A plot of the on resonance noise and off resonance noise of KID 11 is included in Appendix B: Al on SOI CPW additional figures for completeness.

All constant width KIDs showed similar noise performance as KID 4 and all varying width KIDs showed similar noise performance as KID 11. Because the performance of the constant

width KIDs is so poor, the data analysis will focus on the varying width KIDs as presented in table 4.3.

A plot of the internal Q-factor  $Q_i$  against internal power  $P_{int}$  for the different total widths  $t$  is presented in figure 4.4. A plot of the internal Q-factor  $Q_i$  against total width of the CPW is presented in figure B2. A plot of the internal Q-factor  $Q_i$  against the gapwidth is included in Appendix B: A1 on SOI CPW additional figures.

A plot of the frequency noise against frequency for the varying width KIDs is presented in figure 4.5.

The frequency noise is calculated by subtracting  $S_{TLS} = S_\theta - S_A$  from figure 4.5, and correcting it for the set-up noise.  $S_{TLS}$  is the remaining noise due to TLS, and this noise is taken at  $F = 1\text{kHz}$ . The results are plotted against the internal power in figure 4.6. A  $t = 3\mu\text{m}$  CPW model from [27] serves as a reference.

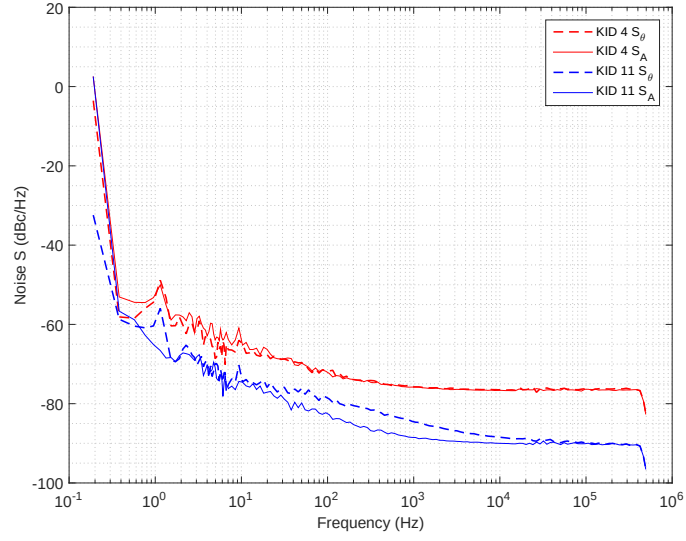


Figure 4.1: Amplitude noise and phase noise of KID 4 (constant width KID with  $w_{gap} = 6\mu\text{m}$  and  $w_{line} = 12\mu\text{m}$  at 4GHz) and KID 11 (varying width KID with  $w_{gap} = 2.667\mu\text{m}$  and  $w_{line} = 4\mu\text{m}$  at 6GHz).

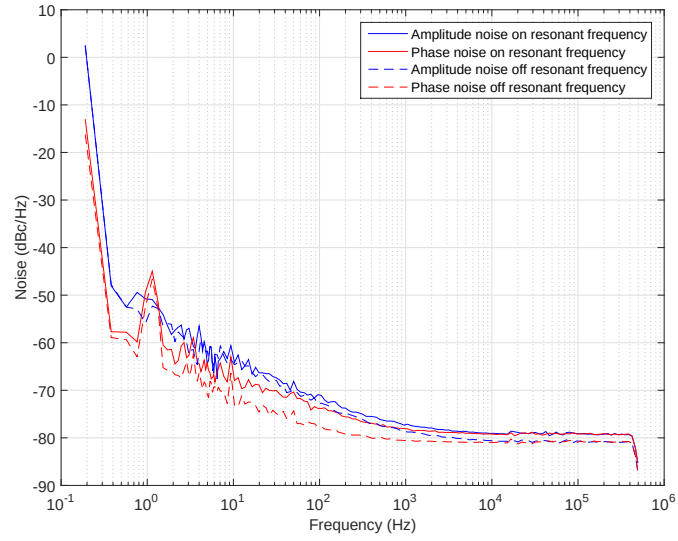


Figure 4.2: Amplitude noise (blue) and phase noise (red) on resonance (solid line) and off resonance (dashed line) for KID 4 (constant width KID with  $w_{gap} = 6\mu\text{m}$  and  $w_{line} = 12\mu\text{m}$  at 4GHz).

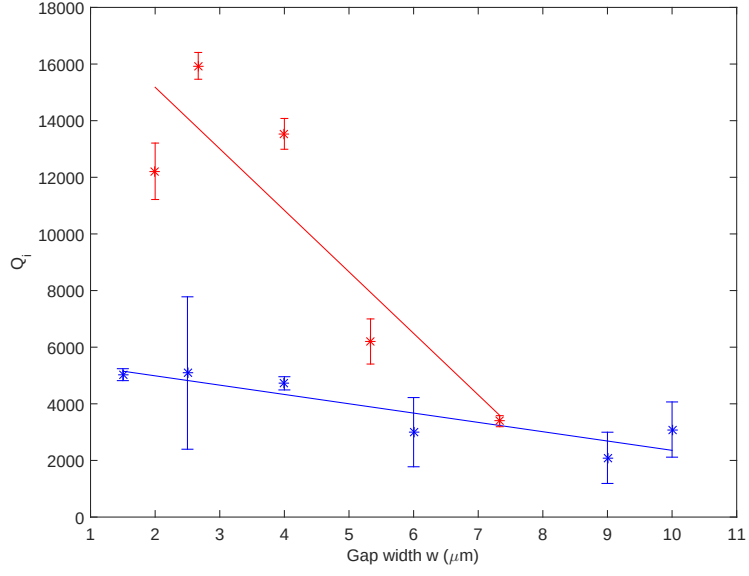


Figure 4.3: Internal Q-factor  $Q_i$  and gap width  $w$  for the constant width KIDs at 4GHz (blue) and varying width KIDs at 6GHz (red).

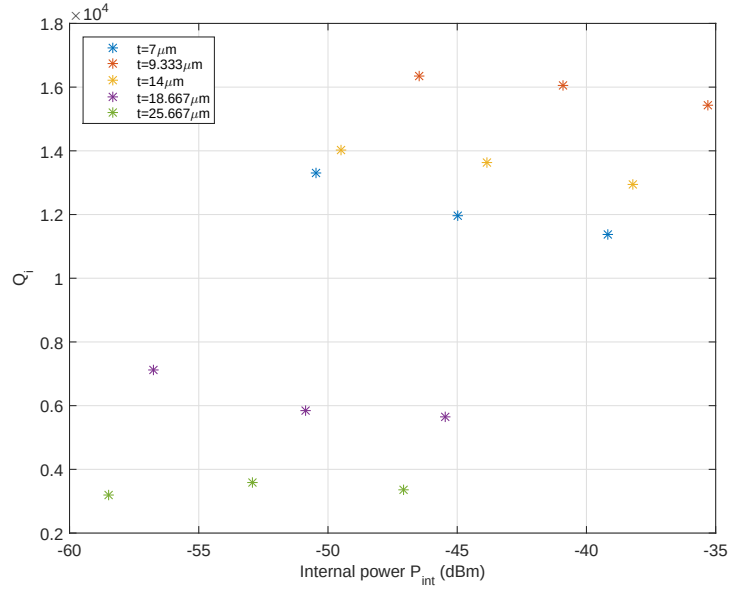


Figure 4.4: Internal Q-factor  $Q_i$  against internal power  $P_{int}$ , with different total widths  $t$  of the CPW.

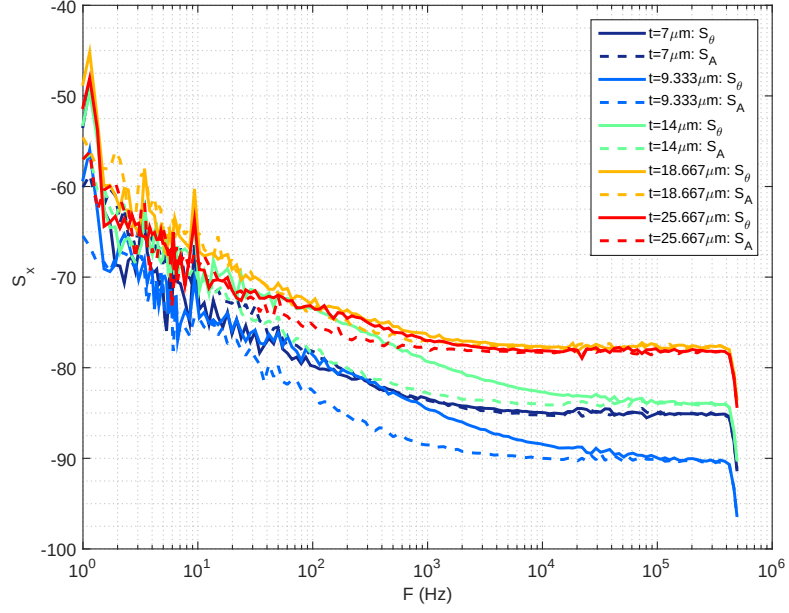


Figure 4.5: Noise and frequency at optimal power  $P_{opt}$  for the varying width KIDs.

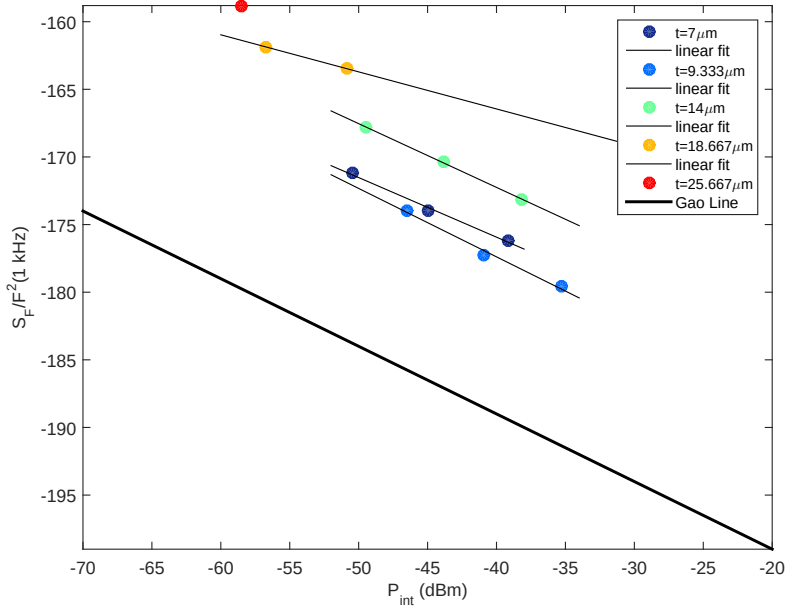


Figure 4.6: Noise  $S_{TLS} = S_\theta - S_A$ , normalized for the set-up noise at 1kHz and internal power for varying width KIDs. The Gao Line from [27] is a  $t = 3\mu\text{m}$  CPW model which serves as a reference.



# Chapter 5

## Discussion

In this chapter the results from the numerical analysis in chapter 2 and the experimental results from chapter 4 will be discussed.

### 5.1 Al on 5 $\mu$ m Si microstrip

The measurement of the Al on 5 $\mu$ m Si microstrip yielded no results, because no dips could be found using the VNA and therefore no KIDs could be detected. This is probably due to a design error or an element in the design that has broken down during the cooling (e.g. bonds that break) to 100mK. Also, a mistake could have been made in the cleanroom, so consequently parts got broken.

Due to the lack of experimental results only the results from the numerical analysis will be discussed. The results from the numerical analysis in subsection 2.6.1 can be summarized as follows:

- **Q-factor:** The Al on 5 $\mu$ m Si microstrip shows a very similar Q-factor as the 300nm NbTiN on 4 $\mu$ m Si microstrip in [28]. The Q-factor is limited by the metal-substrate, substrate-air and dielectric bulk interfaces by a  $Q \sim 10^5$ . The metal-edge and metal-air interfaces have a higher Q-factor of  $Q \sim 10^8$ . The metal-edge and substrate-air interface both show an increase of the Q-factor of 500% between the linewidth of 3 $\mu$ m and 30 $\mu$ m. The rest of the interfaces show no notable dependency on the linewidth. Effectively, a 100nm Al on 5 $\mu$ m on Si microstrip will yield the same Q-factor performance as the 300nm NbTiN on 4 $\mu$ m Si microstrip.
- **Noise:** The noise is bulk dominated, just as the 300nm NbTiN on 4 $\mu$ m Si microstrip in [28]. All interfaces show a higher or identical noise performance as the 300nm NbTiN on 4 $\mu$ m Si on microstrip. The metal-air and metal-edge show a higher noise of 5dBc/Hz and 2dBc/Hz, respectively, compared to the 300nm NbTiN on 4 $\mu$ m on Si microstrip. This is due to the aluminium superconducting layer, which means that 100nm aluminium layer

leads to a few dBc/Hz higher noise. The dielectric bulk of the 5 $\mu$ m Si has a higher noise of approximately 1dBc/Hz, which is due to the extra 1  $\mu$ m Si compared to the 4 $\mu$ m Si. The substrate-air and metal-substrate interfaces show identical noise performance.

- **Width dependency noise:** The noise is dependent on the linewidth by the power law  $S = a \cdot s^b$ , where  $b = 0.0339 \pm 0.0140$ ; wherein  $a$  and  $b$  are fit parameters,  $S$  the noise in dBc/Hz and  $s$  the linewidth of the microstrip. For all the MATLAB fit parameters for the different interfaces, see Appendix C: MATLAB fit parameters.

## 5.2 Al on 5 $\mu$ m Si CPW

Only a numerical analysis was carried out, and the numerical results in subsection 2.6.2 can be summarized as follows:

- **Q-factor:** The Q-factor of the CPW is almost identical to the Al on 5 $\mu$ m microstrip. The Q-factor performance is limited by the metal-substrate, substrate-air and dielectric bulk interfaces with Q-factors in the order of  $10^5$ . The metal-edge and metal-air interfaces have the highest Q-factors in the order of  $10^8$ . The metal-substrate, substrate-air and dielectric bulk show almost identical Q-factors ( $< 10^4$  difference) for both the microstrip and the CPW. The metal-edge and metal-air interfaces have a slightly higher Q-factor (an increase of  $\approx 10^7$ ) for the microstrip compared to the CPW. Effectively, a similar Q-factor performance is achieved for the CPW and microstrip, due to the small difference in the limiting dielectric bulk, substrate-air and metal-substrate interfaces.
- **Noise:** The noise of the CPW is higher for all interfaces compared to the Al on  $\mu$ m microstrip. The noise is dominated by the dielectric bulk at -150dBc/Hz for both the CPW and microstrip (difference  $< 1$ dBc/Hz). The noise of the CPW for the substrate-air, metal-substrate, metal-edge and metal-air is higher for the CPW than the microstrip with 4dBc/Hz, 2dBc/Hz, 8dBc/Hz and 2dBc/Hz, respectively.

## 5.3 Al on SOI CPW

For Al on SOI CPW numerical results and experimental results have been obtained. The results from the numerical analysis in subsection 2.6.3 are summarized as follows:

- **Q-factor:** The Q-factor is limited by the metal-substrate, substrate-air and dielectric bulk interfaces at  $Q \sim 10^5$ . The Q-factor is high for the metal-air and metal-edge interfaces with Q-factors of  $Q \sim 10^8$ . The Q-factors of the 100nm Al on SOI CPW are almost completely the same compared to the 100nm Al on 5 $\mu$ m Si CPW, with just minor differences ( $< 10^4$ ). Overall, the 100nm Al on SOI CPW will show similar Q-factor performance as the 100nm Al on 5 $\mu$ m Si CPW. This means that the buried oxide layer has very little influence on the Q-factor.

- **Noise:** The noise of the Al on SOI CPW is bulk dominated. The Al on SOI CPW has a 9dBc/Hz higher noise due to the different dielectric bulk with the SiO<sub>2</sub>, compared to the Al on 5μm Si. This increase can be attributed to the buried oxide layer in the SOI. The metal-air, metal-edge, metal-substrate and substrate-air interfaces show no notable (< 2dBc/Hz) difference in noise levels.
- **Width dependency noise:** The noise is dependent on the linewidth by the power law  $S = a \cdot s^b$ , where  $b = 0.05500 \pm 0.04810$ ; wherein  $a$  and  $b$  are fit parameters,  $S$  the noise in dBc/Hz and  $s$  the linewidth of the CPW. For all the MATLAB fit parameters for the different interfaces, see Appendix C: MATLAB fit parameters. The jumpy behaviour of the data due to the errors in COMSOL leads to a big error in  $b$  of  $\pm 87.45\%$ .

The experimental results in section 4.2 are summarized and compared as follows:

- **Q-factor:** The shallow dips and a high  $S_{21,min}$  lead to low internal Q-factors  $Q_i$ . The internal Q-factors are  $Q \sim 10^4$ , and shows a trend to decrease as the total width of the CPW increases. A study by Weber et al. of an aluminium parallel plate capacitor on SOI showed internal Q-factors of  $Q_i \sim 10^5$ , when surface oxide was removed; and internal Q-factors of  $Q_i \sim 10^4$ , with native surface oxide [32]. However, experimental results from W. Daalman indicate internal Q-factors of  $Q_i \sim 10^6$  for a “normal” Al on Si CPW and internal Q-factors of  $Q_i \sim 10^5$  for an Al on SiN CPW [28]. The measured Q-factors appear lower than comparable measurements in literature.
- **Noise:** The shallow dips and the high  $S_{21,min}$  yielded low internal Q-factors. This leads to a high set-up noise of -80dBc/Hz. A difference between on resonance and off resonance noise of 10dBc/Hz is minimal, and is the result of the high set-up noise. The subtracted frequency noise is the lowest for  $t = 9.333\mu m$  with a of approximately -177dBc/Hz at an internal power of  $P_{int} = -40dBm$ . The frequency noise curves (in figure 4.6) are not all parallel to the Gao Line, which indicates that the dependency on the internal power is not solely governed by TLS noise [27], which is also a consequence of the high set-up noise. Other literature present frequency noise levels of approximately -185dBc/Hz at  $P_{int} = -40dBm$  at 1kHz for a CPW with a linewidth and gapwidth of 2μm and 1μm, respectively [5]. Similar results are presented in [23]. Frequency noise normally decreases when the linewidth increases [27], and this means that a frequency noise level of -177dBc/Hz at  $P_{int} = -40dBm$  is lower than a regular Al on Si CPW.

A comparison between the numerical results and the experimental results leads to the following observations:

- **Q-factor:** The measured internal Q-factors are approximately one order of magnitude smaller than the slightly different numerical model predicted. This can lead to two conclusions: The numerical analysis is too different and does not take effects into consideration that greatly reduce the Q-factor or the measured KIDs underperformed due to an unforeseen design or measurement error. This is further discussed below.

- **Noise:** The measured noise is higher than the expected noise from the numerical analysis. The numerical analysis predicted that the dielectric bulk has an increased noise of approximately 10dBc/Hz. This would lead to a higher noise, but the system noise levels around -85dBc/Hz are very high and disturb the measurements. Furthermore, the curves of the frequency noise are mostly parallel to the Gao Line but not all, which indicates that other noise sources disturb the measurements, other than TLS-noise.

The difference in Q-factor and noise between the numerical analysis and the measurements make both the numerical model and the measurements dubious. However, because the model (or rather the same approach to modeling a KID in COMSOL) yielded trustworthy results in [28] and [38] there is reason to believe that the model also holds when a (relatively simple) buried oxide layer is added to the geometry. However, the geometry which has been modeled differs from the measured Al on SOI CPW. The difference is that the numerical model has a vacuum beneath the buried oxide layer, and the measured CPW has 300 $\mu$ m Si beneath the buried oxide layer. Yet, this difference would probably not lead to notable differences in the Q-factor, because the losses in terms of the Q-factor are most prevalent in the substrate-air and metal-substrate interfaces, which are not different.

Furthermore, there is reason to doubt the manufacturing process of the wafer, and the deposition of some layers in particular. Characteristic defects at the Si-SiO<sub>2</sub> interface are strongly influenced by low-temperature treatments [43]. Also, atomic hydrogen is found to simultaneously passivate and depassivate silicon dangling bonds at the Si-SiO<sub>2</sub> interface at room temperature, meaning that it changes the way it reacts with the environment (such as water and air) [44]. In the complex procedure of fabricating the wafer (as shown in detail in Appendix A: Process flow wafer fabrication) it cannot be excluded that the SOI-interface or the SOI-substrate has been damaged in such a way that it affected the properties of the CPW notably. Therefore, the numerical analysis seems more trustworthy than the measurements.

## Chapter 6

# Conclusion

With regard to the question if and how the resonator geometry has influence on the noise and Q-factor performance of a kinetic inductance detector, and bearing in mind the discussion in the previous chapter, a couple of conclusions can be drawn:

- For a 100nm Al on Si microstrip the metal-edge interface contributes  $\sim 10^7$  more to the internal Q-factor and the metal-air interface contributes  $\sim 10^7$  less to the internal Q-factor, compared to a 300nm NbTiN on Si microstrip. This is due to the difference in the superconducting layer. Yet, the overall Q-factor performance is limited by the metal-substrate, substrate-air and dielectric bulk interfaces at  $Q \sim 10^5$ . Therefore, a similar performance is achieved in terms of the Q-factor.
- The noise performance of a 100nm Al on Si microstrip is somewhat worse than a 300nm NbTiN on Si microstrip with 1-5 dBc/Hz, especially at the metal-air and metal-edge interfaces. This is due to the difference in the superconducting layer.
- A 100nm Al on  $5\mu\text{m}$  Si CPW and microstrip have an almost identical Q-factor performance, except for a higher Q-factor for the microstrip (difference in the order of  $10^7$ ) for the metal-edge and metal-air interfaces compared to the CPW. However, the Q-factor performance is limited by the metal-substrate, substrate-air and dielectric bulk interfaces at  $Q \sim 10^5$ . Therefore, a similar Q-factor performance is achieved.
- The noise performance of a 100nm Al on  $\mu\text{m}$  Si CPW and microstrip are both dielectric bulk dominated at -150dBc/Hz. However, the noise of the CPW for the substrate-air, metal-substrate, metal-edge and metal-air is higher compared to the microstrip with 4dBc/Hz, 2dBc/Hz, 8dBc/Hz and 2dBc/Hz, respectively. These interfaces are not dominant, so the noise performance will not differ.
- A buried oxide layer has no influence on the loss in terms of the Q-factor for an Al on SOI CPW (compared to an Al on Si CPW).

- The noise of an Al on SOI CPW is dielectric bulk dominated, and the dielectric bulk contributes 10dBc/Hz more to the noise compared to an Al on Si CPW.
- The measured dips (high  $S_{21,min}$ ) from the Al on SOI CPWs were very shallow, which leads to internal Q-factor  $Q_i \sim 10^3$  for the constant width KIDs and  $Q_i \sim 10^4$  for the varying width KIDs and a high set-up noise of -85dBc/Hz.
- All measured Al on SOI CPWs, both the constant width and varying width KIDs, with a gapwidth  $w_{gap} \geq 10\mu\text{m}$  show no response, because high set-up noise make the KIDs undetectable.
- The measured internal Q-factors  $Q_i$  of the varying width Al on SOI CPWs are in the order of  $\sim 10^4$ , which is low compared to measurements and models in [28], [11], [32] and the numerical results in chapter 2 where typically  $Q_i \sim 10^5 - 10^6$ .
- The measured Al on SOI CPWs have a poor noise performance, which is not dominated by TLS-noise but by set-up noise.

The conclusions from the research carried out in this thesis lead to the following design considerations:

- A 300nm NbTiN on Si microstrip is favoured over a 100nm Al on Si microstrip, due to the similar performance of the Q-factor and the better noise performance.
- An Al on Si microstrip is preferred over an Al on Si CPW, because the Q-factor performance is similar and the noise performance is better.
- A buried oxide layer is not advisable for a CPW, because the Q-factor is the same and the noise worsens with 10dBc/Hz.

## Suggestions

A couple of questions are still not completely answered in this thesis and are interesting for further research. The following issues and questions are still worth investigating:

- Look at the exact performance of the Al on SOI CPW, with a  $300\mu$  silicon substrate. A model could be made in COMSOL and compared to the experimental results presented in this thesis.
- A question that remains not clearly answered is if the CPWs that were measured were actually the designed CPWs that were *meant* to be measured. The experimental results do not seem to be trustworthy (and the Al on Si microstrip did not yield any results at all), and further research could settle this uncertainty. One could change the wafer production in such a way, that deposition at high temperature is avoided, so the chance of changing

the composition of Si and SiO<sub>2</sub> is minimized. Also, a design with a lower coupling Q-factor  $Q_c$  to confirm the low internal Q-factors  $Q_i$  at a lower noise, and this would also yield more trustworthy experimental results about the noise performance. Furthermore, a closer look at the design could be useful, because a low  $Q_i$  indicates a lot of the microwave transmission is reflected and absorbed by the resonator.

- The influence of a buried oxide layer can also be examined for microstrips by altering the developed COMSOL model. Also, the numerical results from the Al on 5 $\mu$ m on Si microstrip can be used as a reference. Also, it is worthwhile to conduct measurements on an Al on SOI microstrip and compare this to the numerical prediction.
- The measurement of the Al on 5 $\mu$ m Si could be repeated. However, avoiding a SOI-based wafer and using regular Si wafer would be advisable, because the SOI-based wafer could be the cause of the unmeasurable KIDs in this thesis.

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# Appendix

## Appendix A: Process flow wafer fabrication

All the steps for the Al on SOI wafer are explained in two figures: the first part in figure A1 and second part in figure A2. To follow the whole process read the figures from top to bottom, then left to right. The first column of figure A1 shows the fabrication of the layers on the bare SOI wafer. The second column of figure A2 shows the etching of the Si substrate and the SiO<sub>2</sub> layer.

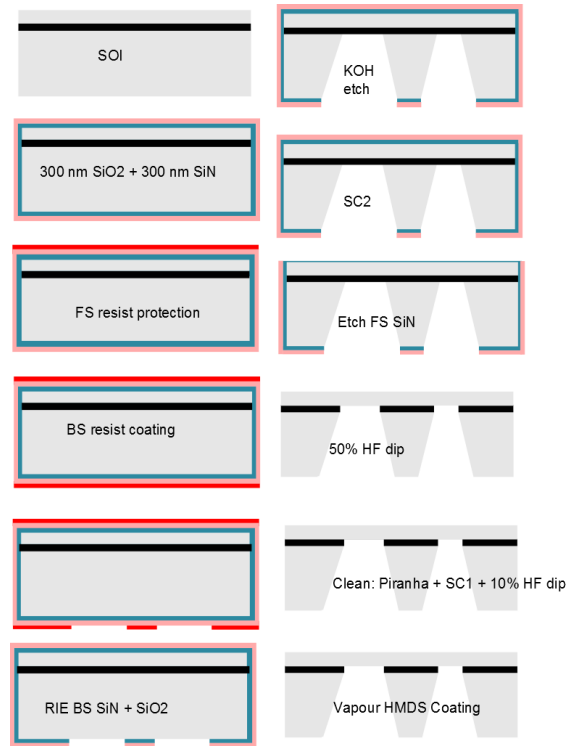


Figure A1: Process flow wafer fabrication, part I. The Silicon substrate is gray; the buried SiO<sub>2</sub> layer is black; the outer SiO<sub>2</sub> and SiN layers are cyan and pink, respectively; the coating is red; and air (created by etching) is white.

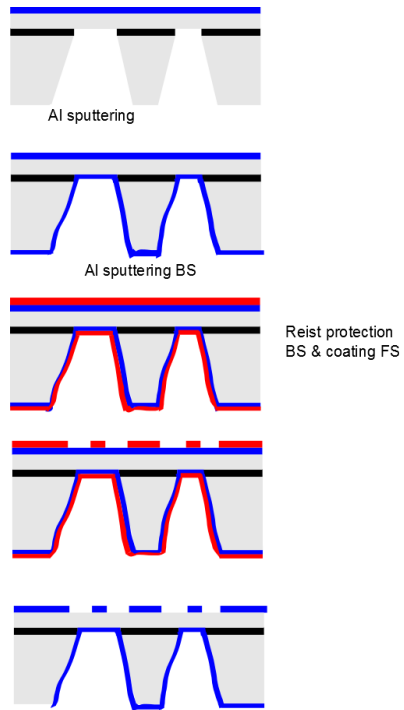


Figure A2: Process flow wafer fabrication, part I. A double CPW-pattern can be seen in the bottom frame. The Silicon substrate is gray; the buried SiO<sub>2</sub> layer is black; the sputtered Aluminium is blue; the coating is red; and air (created by etching) is white.

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## Appendix B: Al on SOI CPW additional figures

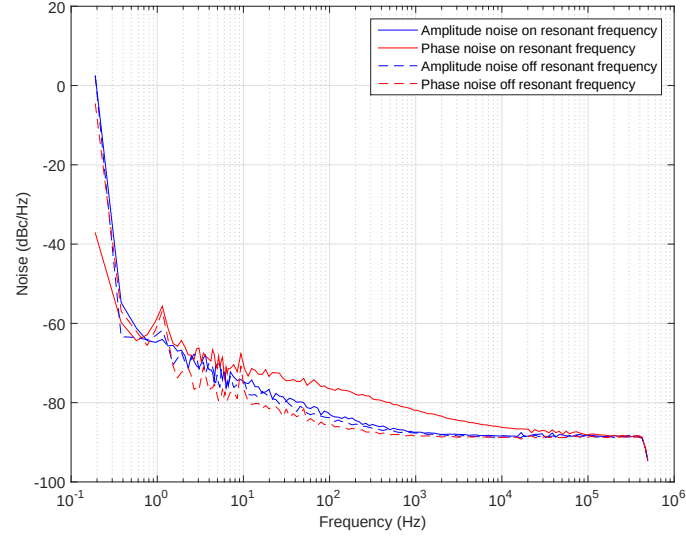


Figure B1: Amplitude noise (blue) and phase noise (red) on resonance (solid line) and off resonance (dashed line) for KID 4.

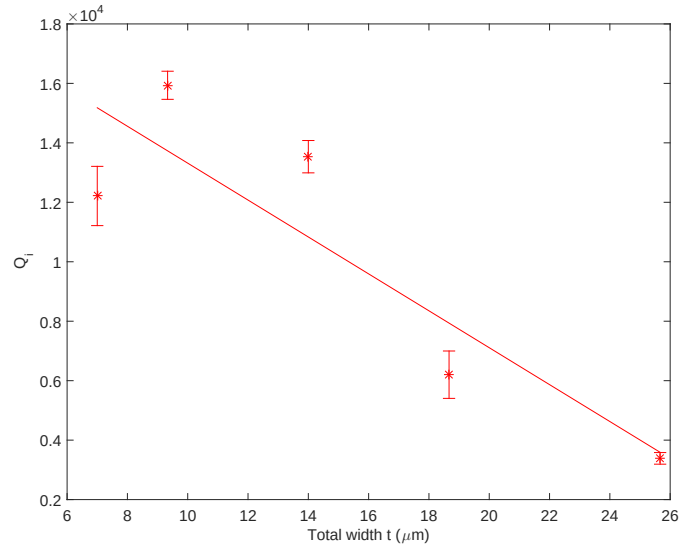


Figure B2: Internal Q-factor  $Q_i$  plotted against total width  $t$ . The error bars show the mean square deviation due to the different readout powers.

## Appendix C: Matlab fit parameters

Table C1: Noise and width MATLAB fit parameters for the Al on  $5\mu\text{m}$  Si microstrip model with 95% confidence bounds.

| Parameter<br>Interface | $a$              | $b$                   |
|------------------------|------------------|-----------------------|
| ma                     | $-175.9 \pm 5.0$ | $0.03945 \pm 0.05879$ |
| me                     | $-170.4 \pm 1.1$ | $0.03308 \pm 0.00040$ |
| ms                     | $-156.2 \pm 0.9$ | $0.03616 \pm 0.00238$ |
| sa                     | $-147.6 \pm 1.3$ | $0.03931 \pm 0.00357$ |
| db                     | $-146.0 \pm 1.0$ | $0.02138 \pm 0.00274$ |
| mean                   | n.a.             | $0.03390 \pm 0.01400$ |

Table C2: Noise and width MATLAB fit parameters for the Al on SOI CPW model with 95% confidence bounds.

| Parameter<br>Interface | $a$               | $b$                   |
|------------------------|-------------------|-----------------------|
| ma                     | $-179.7 \pm 21.2$ | $0.04531 \pm 0.04877$ |
| me                     | $-147.7 \pm 27.0$ | $0.07321 \pm 0.07449$ |
| ms                     | $-154.2 \pm 9.9$  | $0.06046 \pm 0.02621$ |
| sa                     | $-158.8 \pm 18.2$ | $0.03096 \pm 0.04749$ |
| db                     | $-126.2 \pm 13.5$ | $0.06510 \pm 0.04360$ |
| mean                   | n.a.              | $0.05500 \pm 0.04810$ |

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## Appendix D: Readout system

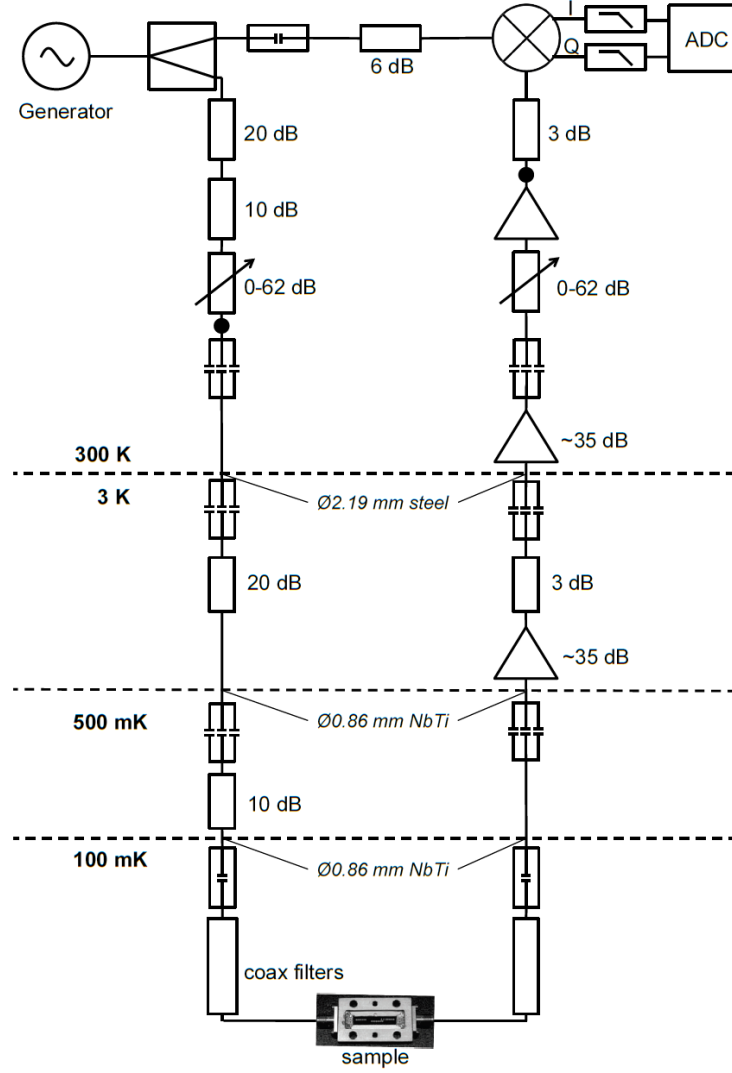


Figure D1: The microwave readout system in the experimental setup. Figure from [11].