

A Double-mode Linear Imaging System for IC-compatible Microspectrometers in Visible Light

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Submission to

The Faculty of Electrical Engineering,

Mathematics and Computer Science

In Partial Fulfillment of the Requirements

For the Degree of

MASTER OF SCIENCE

In Electrical Engineering

Delft University of Technology

January 2010

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Abstract

This thesis is a final report of a Master project which lasted from September 2008 to January 2010. The work has been done in the Electronic Instrumentation Laboratory, Department of Microelectronics, Delft University of Technology.

In the thesis a double-mode linear imaging system is designed for the application of microspectrometers. The imaging system is optimized to work with a Planar Double Grating System and a Linear Variable Optical Filter, which are suitable candidates of high-resolution low-cost microspectrometers. This linear imaging system comprises one linear photodiode array and two readout modes: the integration mode and the coherent detection mode. The integration mode is applied for the low-leakage-current case, which increases the measured SNR by long integration time and improves the dynamic range by variable integration time control. The coherent detection mode is applied for the high-leakage-current case, which aims at reducing the error caused by leakage current. The imaging system is implemented in AMIS 0.35um CMOS process.

Key words: Microspectrometer, CMOS Image Sensor, Correlated Double Sampling, Capacitive Transimpedance Amplifier, Coherent Detection, Optical Chopper

Acknowledgement

The works presented in this thesis can never have been done without the help of many individuals.

First of all, I would like to express my gratitude to my supervisor Dr. Ir. Reinoud F. Wolffenbuttel for his continuous guidance and support.

Additionally, I would like to express my profound appreciation to my daily supervisors, Huaiwen Wu and Arvin Emadi. Thank you for sharing your valuable experience with me and guiding me patiently.

I would also like to thank our technicians, Ger de Graaf and Zu-yao. Without their constant support, the implementations will never come true.

Further I would like to thank all my friends who have ever shared the room HB 13.140 with me, Jun Ye, Xiaodong Guo, Guang Ge, Chao Yue, Jianfeng Wu, Karfee Tang. I would like to thank my girlfriend Yang Xu and Tianyi Zhang. I would like to thank all my friends in space box, Deheng Liu, Xiao Zhang, Lu Nie, Xiaolei Cui, Jing Jin, Yajing Huang, Xin Xu and Daoxin Li. All the time and the discussions shared with you are a treasure for me.

Finally I want to thank my parents Chunying Peng and Yinlin Liu, and my boyfriend, Ruimin Yang. Thank you for surrounding me and supporting me with love.

Chi, Liu

January 24, 2010

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Chapter 1 Introduction to Microspectrometers

The project of this thesis is to design a linear imaging system used with a Linear Variable Optical Filter (LVOF) or a Planar-double-grating-system (PDGS) to achieve a high-resolution microspectrometer. The design equipped with one photodiode array and two readout systems is finally integrated on-chip. Before going to the electrical and optical details, this chapter gives an introduction to microspectrometers. The content includes the applications, the components and the IC-compatible implementations

1.1 From Spectrometer to Microspectrometer

1.1.1 Spectrometers

Spectrometers are the systems that separate the incoming light into a frequency spectrum, so as to measure the light properties versus the electromagnetic wavelength. A typical example is shown in Figure 1. 1 [1].

Spectrometer finds its applications in abundant fields, including drug analysis, food analysis, agriculture analysis, cosmetics analysis and etc. The mid-infrared spectrometers are utilized in the measurement of gases during some chemical or biological processes. As the global warming becomes a more and more serious problem, the mid-infrared spectrometers play an active role of monitoring the greenhouse emissions or the combustion processes, not only in the daily life but also in the industrial activities. The mid-infrared spectrometers are also helping improve the quality of life by simplifying and fastening the food inspection without reducing the testing reliability. For example, they are commonly used for detecting oil and fat.

The UV-visible spectrophotometers involved with more energetic photons compared with the mid-infrared spectrometers. They have been used in many biological experiments, for quantifying the protein or the DNA concentrations [2].

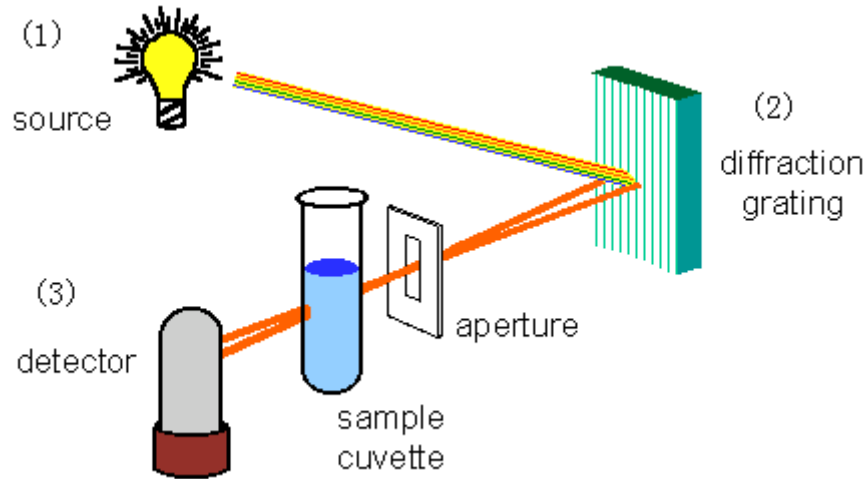


Figure 1. 1 a typical example of spectrometers

Generally speaking, a spectrometer comprises three parts, as is shown in Figure 1. 1: (1) the light source, (2) the optical dispersion system, and (3) the imaging system.

(1) The light source: the reference light is generated inside the spectrometer or coupled from a laser. The reference light is projected onto the objective sample, where interactions like absorption or scattering happen between the radiation and the matter. These interactions result in a new light beam with different properties, like different light intensities, different polarizations or a new direction of light beam [3]. A comparison between the original beam and the new beam carries information about the chemical structure of the illuminated sample.

(2) The optical dispersion system: the light beam can be dispersed based on several different principles, like refraction, diffraction and interference. The dispersive performance varies much among these optical principles. Some collimating elements can be also integrated for collecting as much light as possible.

(3) The imaging system: illuminated by the dispersed light, this part of the system transforms the radiation energy to the processible electrical signals. The imaging system is composed of two basic sub-modules: (i) one detector array; (ii) readout circuits. The A/D converter and additional signal processing circuits can be implemented in this part too.

The typical specifications concerned in spectrometers are the resolving power and the Full Width Half Maximum (FWHM) achieved in the dispersion system [4]. The imaging system should be designed without setting any limit for the spectrometers. The specifications concerned in the imaging system are the spatial resolution, the sensitivity, the SNR, the dynamic range as well as the readout speed.

In order to achieve a high-performance spectrometer, large optical components and long optical paths are necessary. Most spectrometers are bulky, heavy and expensive. And trained personnel are needed to operate these systems.

1.1.2 Microspectrometer

Nowadays there have been more opportunities and requirements for the spectrometers to be miniaturized. Microspectrometers have plenty of benefits: (1) They are portable due to the reduced size and weight; (2) The sample volume can shrink as the spectrometers are scaled down; (3) The integration of the systematic functions becomes possible as the IC-compatible microspectrometer becomes available, which means that the control circuit and the signal processing can be integrated into one chip. Thus, the microspectrometer becomes suitable for mass production and easy for operation.

The miniaturization of spectrometers involves scaling down both the optical systems

and the imaging systems. Thanks to the development of the IC technology, the imaging system is ready to be scaled down with high performance. And the miniaturization of the optical system is also achieved due to the development of the Micro-Optical Micro-Electro Mechanical Systems (MOMEMS).

The microspectrometers are mainly used in the small-sample detection. Some examples are listed here: (1) the forensic analysis, e.g. the analysis for small samples of textile fibers, hair, drugs, toxic materials, explosives, paint, toners, inks etc; (2) the analysis of the pharmaceutical products and the biomedical materials, e.g. the tumor detection in tissue samples or the acetone detection by breath analysis. The microspectrometer is also a suitable candidate for the measurement aboard satellites, where the small-size and lightweight systems are preferred.

1.1.3 Different Implementations: macro- and micro- spectrometers

As to the optical systems, the macro-spectrometers usually use the optical devices with a curved structure, like lenses, convex mirrors, prisms and gratings. In microspectrometers, planar optical structures are utilized for easy fabrication.

As to the imaging system, the mainstream techniques are similar for both the macro- and the micro- spectrometers. However, the microspectrometer has a higher requirement on the spatial resolution and the IC-compatibility. The CCD sensors with cooling techniques are usually used in the macro-spectrometers for low-noise and low-leakage-current detection. In the design of microspectrometers, CMOS image sensors are always preferred in the microspectrometers for the on-chip integration and the lower power consumption.

1.2 The Classification of Microspectrometers

The classification of microspectrometers is introduced in this section, to find out what kinds of structures are suitable for the IC-compatible implementation.

1.2.1 The classification based on the dispersion system

The dispersion system determines the overall systematic performance in two aspects: (1) it determines the optical resolution that can be achieved and the difficulty for the fabrication; (2) it determines the spatial resolution and the illumination range for the imaging system.

The microspectrometers are divided into three types based on the optical principles used in the dispersion system [5]:

(1) The refraction type: the light is dispersed in this type based on the fact that the refractive index varies with the light wavelength. Each wavelength is projected to a different direction. In this type the size of the dispersive device determines the spectral resolving power. The scaling down will result in a sharply reduced resolution. Thus this type is not a suitable candidate for the high-resolution microspectrometer.

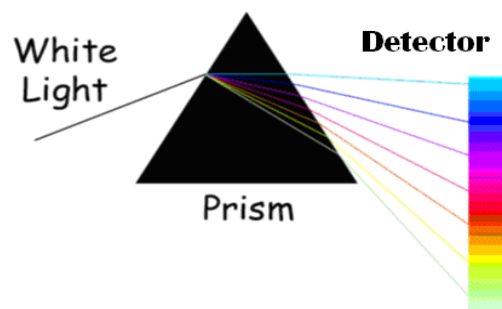


Figure 1. 2 the refraction type of microspectrometer

(2) The diffraction grating type: the light is dispersed in this type based on the diffraction and the interference caused by the grating. The grating can be implemented in the planar structure conveniently. And the reflective or transparent pattern on the grating, which decides the final dispersive performance, can be controlled accurately in the modern MOMEMS technology.

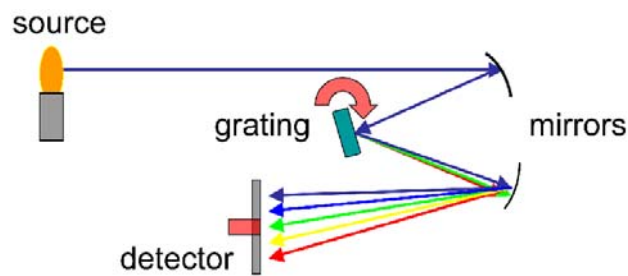


Figure 1. 3 the diffraction grating type of microspectrometer [6]

(3) The Fabry-Perot types: the light is dispersed in this type based on the interference phenomenon. A Fabry-Perot device is used in this type as an optical filter, which can be formed simply by placing a thin transparent spacer between two highly reflective parallel coatings. With the modern MEMS technology, the distance between the coatings can be tuned or achieved with a high resolution. And a high-reflectivity material can be fabricated as the coating. Both facts make this type suitable for achieving high-resolution microspectrometers.

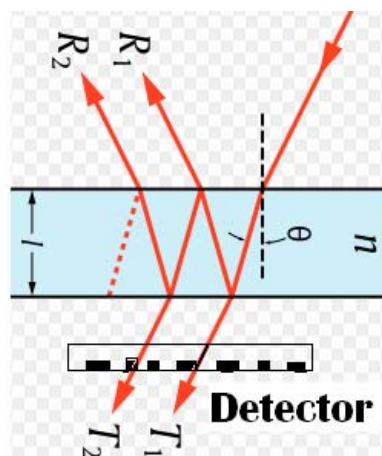


Figure 1. 4 the Fabry-Perot type of microspectrometer

1.2.2 The classification based on the imaging system

The imaging system is designed based on two considerations: (1) the requirements from the dispersion system; (2) the wavelength of the detected light. Different detectors are chosen for different spectral ranges to achieve an optimum responsivity. For instance, the PN-junction photodiodes and the phototransistors are usually applied for the visible-light detection. But for infrared detection, the thermal detectors such as the thermopiles and the bolometers are commonly utilized.

The microspectrometer is divided into several types based on the light wavelength concerned in the imaging system: (1) the mid-infrared microspectrometers; (2) the UV microspectrometers; (3) the microspectrophotometer which works within the visible region.

1.3 Objective of this Project

Single-chip optical microspectrometers have huge potential thanks to their properties of low cost and low-volume sample. Fueled by the urgent demand in the applications like identification of bio-molecules and chemistry analysis, the background of this project is to design high-resolution microspectrometers.

Our group has done a great deal of research under this background. Two delicate dispersion systems have been published which are compatible with the modern MOMEMS technologies, i.e. LVOF (linear variable optical filter) and PDGS (planar double grating system). Once integrated with a high-sensitivity linear imaging system, either of them can be a suitable candidate for a high-resolution microspectrometer.

The objective of this project described in this thesis is thus to design a visible-light imaging system that can work with high photodetection performance and can work adaptively with both the published LVOF [7] and the PDGS [8]. Each dispersion system has low light throughputs and put high requirements on the spatial resolution. The imaging system design is thus challenging in terms of low-illumination detection and small-pitch pixel design. The detailed discussions are left to Chapter 2.

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Chapter 2 Design of Photodetectors and the Principles of their Readout

As concluded in Chapter 1, the challenge of this project is to design a photodetection system used in high-resolution microspectrometers. It is required to operate in the visible light range and work with both newly developed optical dispersive systems, i.e. the Planar-double-grating System (PDGS) and the Linear Variable Optical Filter (LVOF). In this chapter, optical sensor structures and proper principles for their readout are considered together, in order to obtain the optimum solution in the system level.

Section 2.1 introduces the general information and the conclusive parameters related to PDGS and LVOF. Their optical features have given the design limitation of the photodetection modules. Having considered the possible trade-offs, the design of a linear photodiode array is used and will be presented in section 2.2. Two different readout principles will be reviewed in section 2.3, with one leading to a high SNR and the other eliminating the leakage-caused error.

2.1 From optical domain to electrical domain

2.1.1 Introduction to the PDGS and the LVOF

The Planar-double-grating System (PDGS)

The PDGS [1] applies two reflective diffraction gratings to achieve both dispersion and focusing functionalities. The second grating provides additional compensation of the aberrations introduced by the first grating. As depicted in Figure 2. 1(a), the light

from a source is first reflected by a stripe mirror which acts as a slit. The incident light is diffracted on the grating 1, and then redirected by the second mirror to the grating 2 and finally goes to the photodetectors through the glass plate.

Linear Variable Optical Filter

The LVOF [2] is basically a linear array of Fabry-Perot etalons. Instead of being consisted by a huge number of discrete devices, the LVOF has only one resonator cavity in the shape of a wedge. As shown in Figure 2. 1 (b), as the thickness of the cavity varies linearly along its length, the transmitted wavelength shifted linearly along the spectrum. The light coming from the entrance slit is collimated and projected through the device onto the detectors. The optical resolution of the LVOF filter is mainly decided by the reflectance of the two highly reflective coatings.

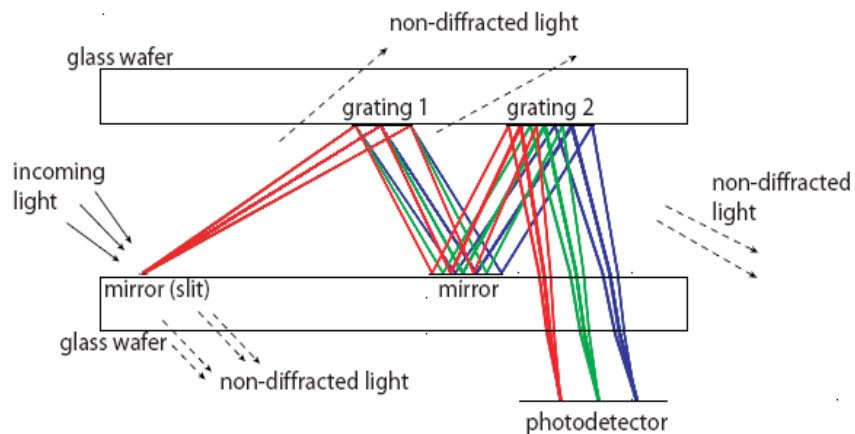


Figure 2. 1 (a) the Planar Double Grating System [1]

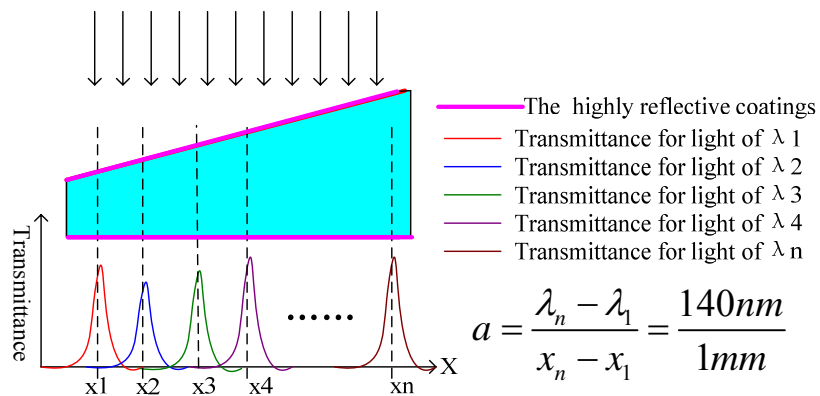


Figure 2. 1 (b) the Linear Variable Optical Filter (LVOF)

2.1.2 Summary of optical specifications

The optical dispersion systems PDGS and LVOF are described in Figure 2. 1(a) and 2.1(b) respectively. Although they are different mechanisms, their functions are basically the same. They both function to build a linear relationship between the light wavelength λ and the location on the imaging system (x, y) . It should be noticed that the variation on the Y direction is often cancelled by optics. Therefore these dispersion systems have a transfer function of $\lambda(x, y) = ax + b$, where a and b are constants defined by the optical design. It is depicted more clearly in Figure 2. 2. In the PDGS microspectrometers, the constant “ a ” represents the reciprocal of the aberration D . “ $1/a$ ” usually ranges from 10 to 11 $\mu\text{m}/\text{nm}$ [1]. In the LVOF microspectrometers, the constant “ a ” is usually obtained by measurement. In our design it is measured that a change of 1mm in x leads to a change of 140nm in λ as shown in Figure 2. 1(b). Therefore $1/a = 7.14\mu\text{m}/\text{nm}$.

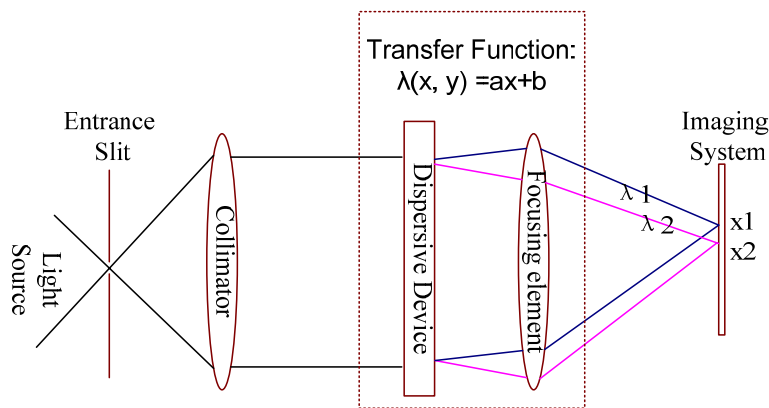


Figure 2. 2 the transfer function of the general dispersion system

The optical resolution ($\Delta\lambda$) sets a critical value for the pixel pitch (P) in order to capture the required spectrum features in a spectrometer. Since $\Delta\lambda = a\Delta x + b$, two conclusions can be made:

- (1) The dispersed pattern has a spatial bandwidth of $1/\Delta x$;
- (2) The imaging system has a spatially sampling frequency of $1/P$.

According to the Nyquist sampling theorem, the sampling frequency should be at least twice as large as the system spatial bandwidth, i.e. $1/P \geq 2/\Delta x$ or $P \leq \Delta x/2$.

Based on the analysis, the acceptable pitches are calculated for the PDGS and the LVOF. The related parameters are listed in Table 2. 1.

	$\Delta\lambda$ (nm)	Δx (um)	1/a (um/nm)	Pitch (um) \leq	Wavelength range
PDGS [3]	1.5	15	10	7.5	150nm
LVOF [2]	2	14.4	7.2	7.2	140nm

Table 2. 1 Pixel pitch for PDGS and LVOF

2.1.3 Constraints and trade-offs in photodetection

The imaging system in microspectrometer is different from what are used for photography or video. The latter ones need high spatial resolution, two-dimensional photodiode arrays and high line rate. Compared with the imaging systems in cameras, the imaging in microspectrometers has three advantages but one drawback which are listed in Table 2. 2.

The common problem of photodetection in microspectrometers is low luminosity. Luminosity describes the available radiation energy for the imaging system. It is defined to describe the amount of light that passes from the source onto the detectors through the instrument. In the process of light dispersion, most of the light leaves the system without being projected onto the detectors. In the PDGS, the luminosity is only 9% due to the low diffraction efficiency and small aperture in optical design. In the LVOF, the luminosity is only 7% because most of light is distributed over the

whole area of LVOF. And since each channel allows only one specific wavelength to pass and blocks the other light by destructive interference, the output light intensity is further attenuated.

The decrease in luminosity is the price paid for the down scaling the optical components. Therefore there is a big demand for an imaging system which is capable of low-illumination detection, high sensitivity and high SNR.

The good news is that the requirements on spatial resolutions and measurement time are not as high as those for photodetection in photography. It is the datum collected that is important in the measurement, instead of the visual effects. In such case, larger pixel sizes and longer integration time can be applied to achieve a higher SNR. According to the function $\lambda(x, y) = ax + b$, the dispersive pattern shows no variance in the dimension of Y. Therefore a linear array of strip-photodetectors placed along the X direction would be enough to obtain the spectral graph. Chip space in the Y direction can be used to implement readout circuits that have lower noise and higher gain.

Features	√ Or X?	Remark
Low luminosity	X	It means small photocurrents to be measured, requiring readout circuits to be implemented with high sensitivity and low noise.
Intermediate spatial resolution	√	It means intermediate pixel pitch, enabling a larger pixel size which is good for improving SNR.
Low readout speed	√	Long integration time can be used, which is good for achieving a high SNR.
One-dimensional photodiode array	√	<ol style="list-style-type: none"> 1. Strip pixels can be used instead of square pixels, with larger pixel size that is good for SNR. 2. Complete amplifiers can be placed in the other dimension, in order to achieve better electrical performances.

Table 2. 2 Merits and demerits of the photodetection in microspectrometers
(With “X” standing for demerits and “√” standing for merits)

In section 2.2, the electrical considerations will be derived from these optical features. The constraints and trade-offs in photodetection are discussed. Based on these discussions, the photodetector array is designed and introduced in the following section.

2.2 Design of photodetectors

2.2.1 Why not commercially available image sensors?

Commercially available CCD and CMOS image sensors can also be used in microspectrometers for photodetection. In the experimental setup used in [1], the Videology 21K137 CCD board camera was used as photodetectors. Reasonable performances were achieved at the cost of big sizes and high power consumption. Complex signal processing was also used to reduce noise and increase linearity.

These commercially available image sensors are not optimized for on-chip photodetection of microspectrometers. Instead these image sensors are mainly designed for visualization. They have a spatial resolution that is much higher than what is needed in microspectrometers. The pixel size which is determined by the image quality can not be designed flexibly. The cooling techniques are usually applied to achieve low leakage current and low noise, which result in extra volume and power consumption [4].

There are also commercially available CMOS and CCD linear photodiode arrays. They apply strip pixels instead of square pixels and are suitable for spectrograph. Examples are the P-series and L-series from PerkinElmer [5]. The problem for these sensors is that the pitches specified are far from enough in this application. According to the analysis in section 2.1.2, the pixel pitch needed for the developed PDGS and

LVOF is 7.2 μ m. Small pitches from the commercial products also exist but their prices are really high. Since the goal is to develop a low price microspectrometer, a commercial image sensor is not suitable in this case.

A photodetection system is designed and optimized for the specific applications. The design of the imaging system includes designing a linear photodiode array and two sensitivity-enhanced readout systems.

2.2.2 Pixel size: spatial resolution V.S. SNR

The pixel size is determined by two factors: the optical pattern and the electrical readout.

On one hand, the pixel pitch must be small enough to achieve a high spatial sampling frequency, so as to satisfy the Nyquist sampling theorem and capture the concerned details in the spectrogram. Following the analysis in section 2.1.2, the pixel pitch is chosen as 7.2 μ m to meet the requirements of both the PDGS and the LVOF.

On the other hand, the pixel size can be enlarged by increasing the pixel length in the Y direction. This will improve the SNR while not affecting the spatial resolution in the X direction. Take the commonly used CMOS image sensor 3T-APS as an example. The temporal noise sources in photodetection can be divided into three parts: pixel photon shot noise, pixel leakage current shot noise and readout circuit noise. Both shot noise sources are proportional to the square root of pixel size while the photocurrent is proportional to the pixel size. Table 2.3 shows that increasing the pixel size helps improving the SNR [6]. Hence the length of pixel is chosen as the maximal value set by the optical feature, i.e. 300 μ m.

2.2.3 Choice of photodetectors

There are several types of standard CMOS compatible photodetectors, for instance photodiodes, phototransistors and photo gates. They are respectively shown in Figure 2. 3. They all have a responsivity that varies much as the light wavelength. An example is shown in Figure 2. 4.

	Expression	Remark
Pixel photon shot noise	$N_{photon} = \sqrt{\frac{I_{photo} t}{q}} = \sqrt{\frac{A \cdot R \cdot P \cdot t}{q}}$	$N_{photon} \propto \sqrt{A}$
Pixel leakage current shot noise	$N_{leakage} = \sqrt{\frac{I_{leakage} t}{q}} \propto \sqrt{\frac{A \cdot t}{q}}$	$N_{leakage} \propto \sqrt{A}$
Readout circuit noise	σ_r^2	It's determined by the readout circuits.
Example SNR of 3T-APS	$SNR = 20 \log \frac{I_{photo} t_{int}}{\sqrt{\sigma_r^2 + (I_{photo} + I_{leakage}) t_{int}}}$	$I_{photo} \propto A$ $A \uparrow, SNR \uparrow$

A: pixel size; R: responsivity; P: incident optical power

Table 2. 3 Temporal noise sources in 3T-APS

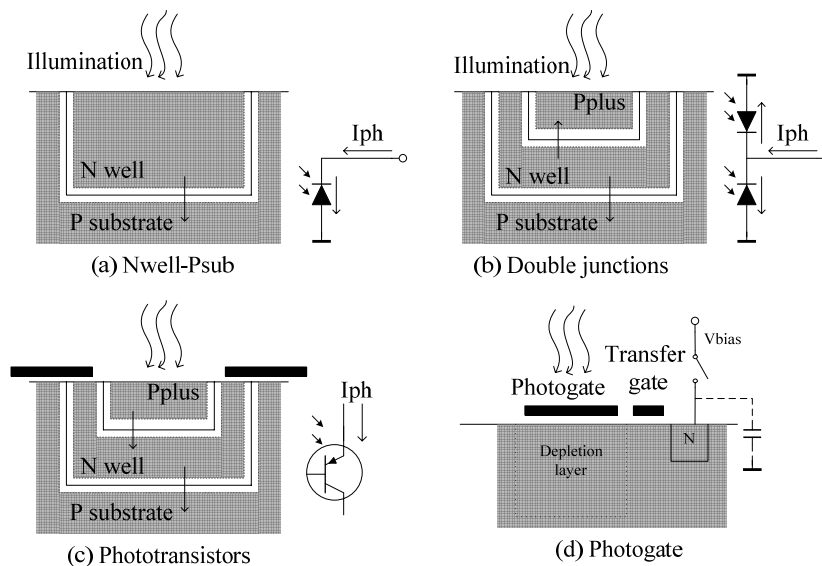


Figure 2. 3 four types of photodetectors [7] [8]

A phototransistor consists of a photodiode and a built-in current amplifier. Although it has a higher responsivity, a phototransistor is not better than a photodiode in detecting low-level light. Phototransistors are not preferred in many applications due to their drawbacks in response time, linearity, sensitivity variation and available light wavelengths. Photo gates are not used in this design due to their low quantum efficiency and large pixel sizes.

As seen in Figure 2. 4, the double junctions show an improved photo response within a wider spectral range. But they also introduce a much large leakage current. If the influence of the leakage current can be suppressed in the readout, the double junctions would be a suitable candidate for improving the responsivity.

Thus a linear array of N-well-P-substrate photodiodes is designed for photodetection. And the double junctions are fabricated as a test structure. The geometric sizes are listed in Table 2. 4. Based on these pixel designs, two active readout circuits are then designed, towards two different sets of target specifications.

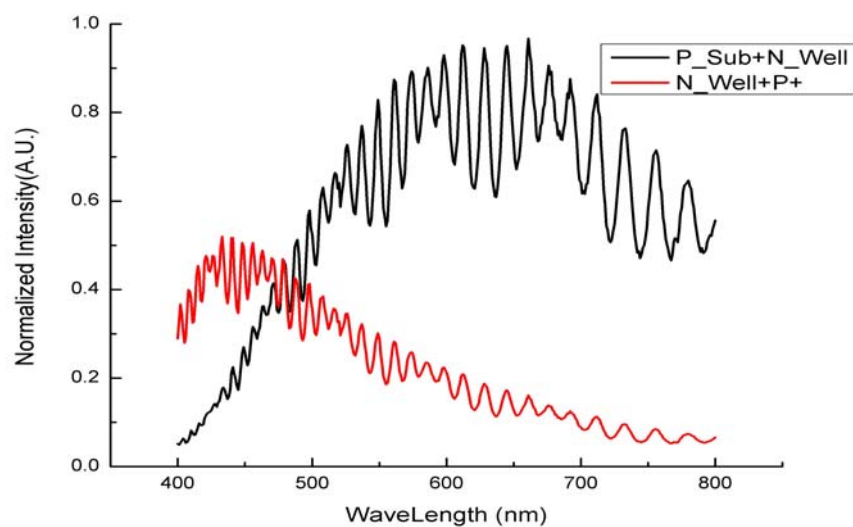


Figure 2. 4 an example of the photo response

Type	Pixel Length	Pixel Pitch	Effective absorption area	Number of Channels	Fill Factor
Nwell-Psub	300 um	7.2 um	4.5um* 300um	128	60%

Table 2. 4 Geometric sizes of the linear photodiode array

2.3 Targets and Solutions: Readout Principles

Two design targets are summarized for the photodetection in microspectrometers: (1) Target I: when leakage current is small, the design target is to improve SNR and sensitivity. (2) Target II: when leakage current is relatively large, the design target is to suppress the influence of leakage current while maintaining a reasonable sensitivity.

Referring to photodetection, there are two traditional principles: (1) charge integration which detects the accumulated photon-generated charge. An example is the commonly used CMOS image sensor 3T-APS. Photocurrent is integrated onto the parasitic junction capacitor and transformed into a voltage [9]. (2) Transimpedance amplifier, which converts the photocurrent into a readable voltage. Examples are those circuits used in optical communication systems for accurate optical power measurements. Photocurrent passes through an accurate resistor and is transformed into a voltage for further signal processing [10]. As will be discussed, both methods have their strongpoints but also drawbacks for the low-illumination photodetection.

As a conclusion, this imaging system is designed with two modes: (1) Mode I, in which the principle of charge integration is applied for a high-sensitivity high-SNR detection in the case of low leakage current; (2) Mode II, in which the principle of coherent detection is applied for a low-offset high-sensitivity detection in the case of high leakage current; in Mode II, a novel transimpedance amplifier is implemented

for achieving the low-noise current-to-voltage conversion.

The implementation details will be left to Chapter 3 and Chapter 4. Here comes the general introduction of the principles and their advantages.

2.3.1 Principle I: towards high SNR using charge integration

In this principle, the electrons generated by the absorption of photons are accumulated onto a capacitor, which continuously changes the voltage across the capacitor. This voltage change versus time can be used as a good measure for the photocurrent. This principle works in the charge domain. Almost all the APS in CMOS image sensors are working with this principle.

The noise analysis in the charge integration mode is in Table 2. 3. Two key parameters are described in Equation 2- 1 and Equation 2- 2, where q_{\max} is the well capacity. The two equations are drawn for the fixed integration time [6]. A conclusion is made from the two equations: as the integration time is increased, the SNR is improved but the dynamic range (DR) is degraded. In order to improve the SNR and the DR at the same time, a good option would be using variable integration time, which means that the integration time is tuned according to the illumination, assuring a big enough accumulated charge ($I_{\text{photo}}*t$). Figure 2. 5(a) and (b) are two Matlab simulation results listed for verification. Note that the influence of leakage current is also included in these figures.

It can be seen that the principle of charge integration is not the best option in applications where large leakage current presents. The key reason is that the leakage current is indistinguishable from the photocurrent with this kind of readout principle. So both currents contribute to the accumulated charge and the shot noise, but only the

photocurrent contributes to the signal power. This will harm both the SNR and the DR.

As a result, the principle of charge integration is chosen as the solution for Target I. Besides the traditional techniques (like Variable Integration Time Control and Correlated Double Sampling), there are novel techniques applied for enhancing sensitivity and linearity.

$$SNR = 20 \log_{10} \frac{I_{photo} t}{\sqrt{\sigma_r^2 + q(I_{photo} + I_{leakage})t}} \quad \text{Equation 2- 1}$$

$$DR = 20 \log_{10} \frac{q_{max} - I_{leakage} t}{\sqrt{\sigma_r^2 + q(I_{photo} + I_{leakage})t}} \quad \text{Equation 2- 2}$$

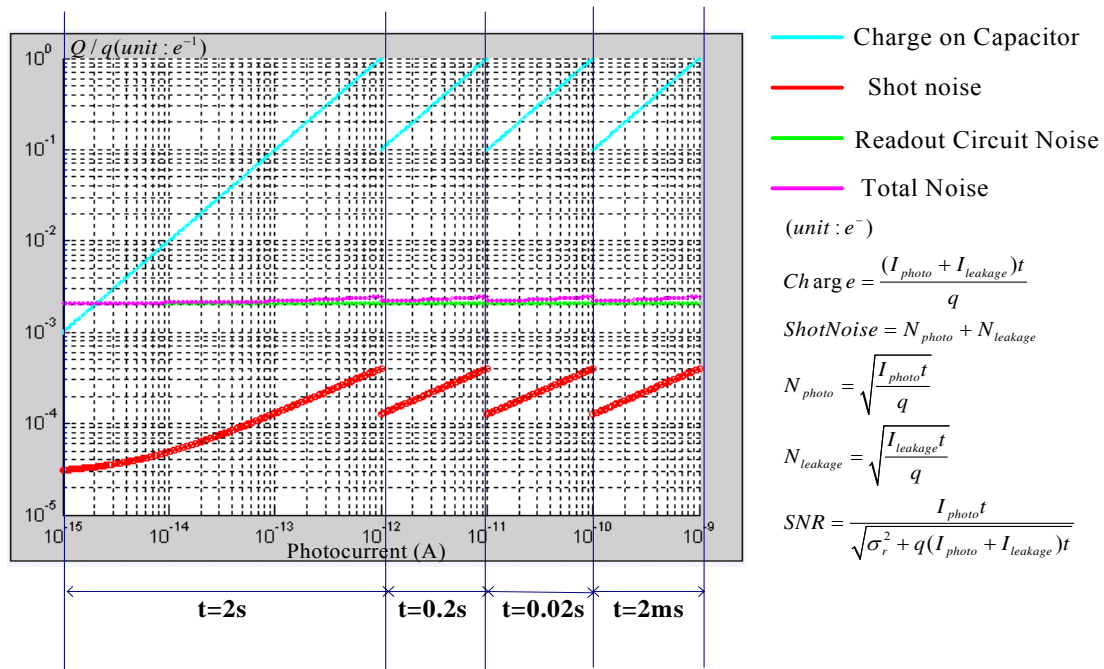


Figure 2. 5 (a) Noise Analysis V.S. Integration Time, with a small leakage current

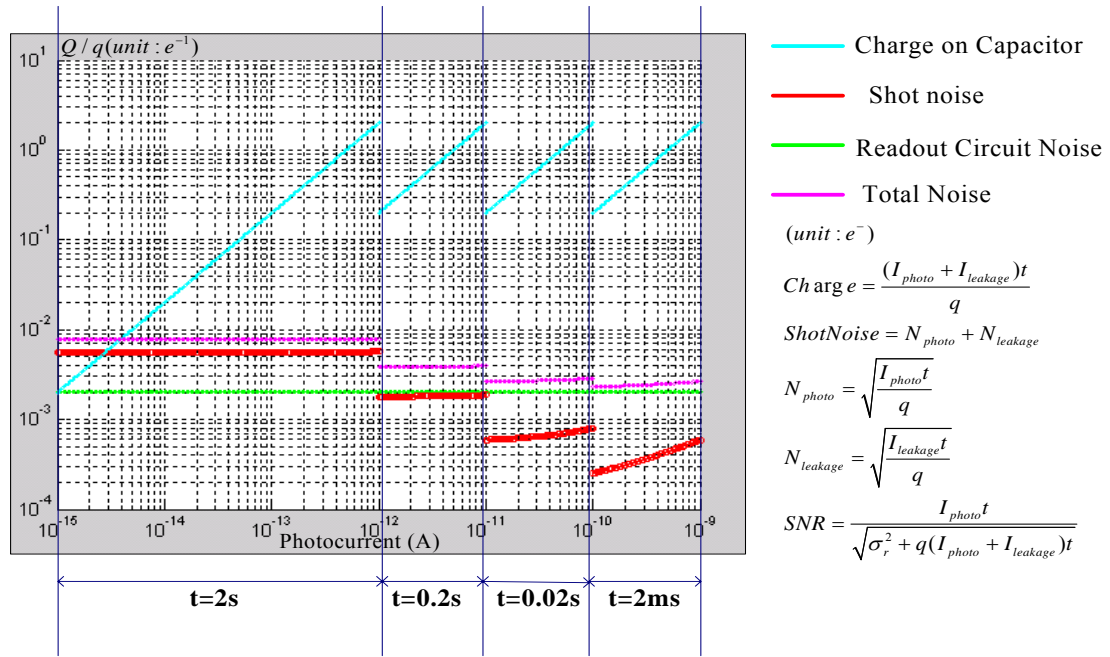


Figure 2. 5 (b) Noise Analysis V.S. Integration Time, with a large leakage current

Furthermore, charge integration is a simple principle which is not area-consuming for implementation. That allows the design of Active Pixel Sensors. This brings two benefits. First, the readout speed can be increased greatly. Second, it avoids a large capacitive load at the readout input which may be introduced by sharing active circuits between pixels. That would also influence the distribution of the accumulated charge and lead to a reduced accuracy.

2.3.2 Principle II: reducing the leakage-oriented error by coherent detection

Leakage current influences the accuracy of measurement in two aspects: (1) it contributes to the offset, which degrades the DR and causes an error in the measurement results, as shown in Equation 2- 2; (2) it contributes to the shot noise, which decreases the SNR.

The influence of the leakage current is resulted from the fact that the leakage current is indistinguishable from the photocurrent to a readout circuit. They are produced within photodiodes similarly with different mechanisms, i.e. the leakage current by thermal generation and the photocurrent by optical generation.

To circumvent this problem, the coherent detection can be applied with the assistance of an optical chopper, which interrupts the impinging light periodically before it's illuminated onto the photodiodes. In this way the input optical signal is modulated into a square wave, while the leakage current is still at DC. In other words, the signal spectrum is partly shifted from low frequency to high frequency, suffering less from noise and offset. A more sensitive measurement can thus be performed. A general structure is taken as an example in Figure 2. 6. The feedback resistor is used, for biasing the circuits and for providing the transimpedance gain. The lock-in amplifier at the end of the analog chain acts as a demodulator. It recovers the optical signal while attenuates the offset caused by leakage current.

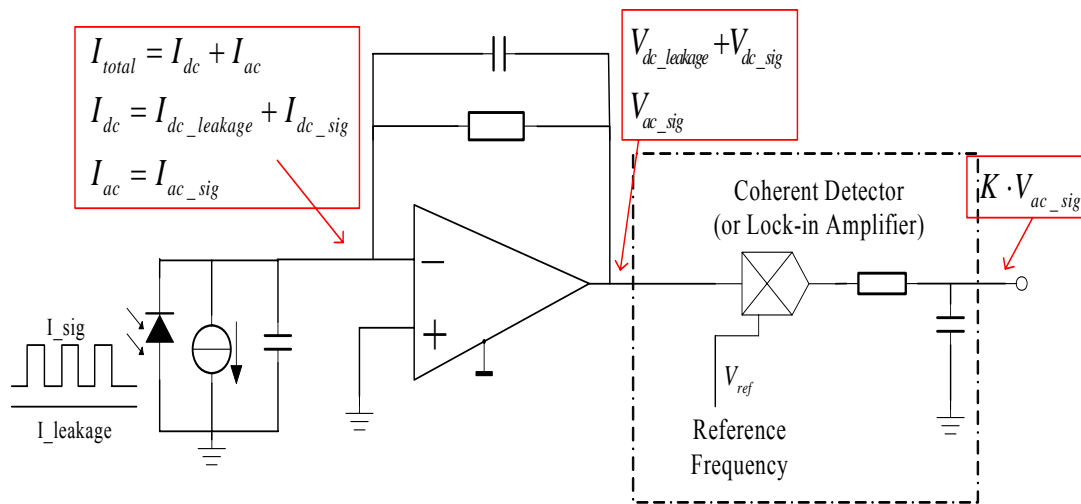


Figure 2. 6 Traditional Example of using Optical Chopper and Coherent Detection

In this way, the offset and the low frequency noise can be reduced greatly. But there are three more issues that should be taken in to account:

(1) The leakage current is still setting the detection limit indirectly since it determines

the shot noise even in high frequencies;

(2) The chopping frequency is limited by the mechanical properties of the optical chopper, which can not be set as high as that in the electrical domain. It will be discussed in Chapter 4 that how the chopping frequency influences the design.

(3) The photocurrent becomes distinguishable from the leakage current. But the price to pay is that part of the signal energy is lost. Only the AC components of the signal are identified by the lock-in amplifier as the information carrier. Further amplification is needed.

For small current detection, the transimpedance amplifier in Figure 2. 6 shows some drawbacks related to on-chip implementation:

(1) Implementation of large resistor: On one hand, the resistor R_f decides the DC gain; and on the other hand, it contributes to the input referred noise level. In other words, this resistor needs to be accurate enough to ensure the precision; and it also needs to be large enough to contribute low noise. In discrete component solutions, a resistor as large as hundreds of $M\Omega$ is usually applied for small current detections, which is difficult for an on-chip solution. A high-value, stable and linear resistor is lacked in the integrated IC technologies. The resistance for an on-chip solution is usually limited around hundreds of $k\Omega$.

(2) Limited dynamic Range: The biasing point of V_o depends on the photocurrent. As the photocurrent increases or if a larger feedback resistor is applied, the DC output shifts a lot. That leads to a great reduce of output swing.

(3) Limited bandwidth: Large feedback resistors are used for low input referred noise. There is unavoidable stray capacitance in parallel with the feedback resistor. That results in a reduced bandwidth, slowing the operation and reducing the AC gain.

Based on the above considerations, novel techniques are proposed to realize this

principle. The main task is to design a low-noise high-gain transimpedance amplifier with enough dynamic range and a reasonable bandwidth. An integrator-differentiator scheme [11] is explored and optimized for this case. The key techniques include:

- (i) How a DC-servo loop is implemented to replace the large feedback resistor for biasing;
- (ii) How an accurate current-to-voltage factor is achieved within a large bandwidth;
- (iii) How large resistors are implemented to achieve large time constants using the available IC technologies;
- (iv) How the frequency compensation is done at extremely low frequencies.

The target of applying this principle is to reduce the error caused by the leakage current and thus enable a more sensitive measurement. Because this implementation is area consuming, this readout circuit is designed to be shared by 16 photodiodes. These photodiodes are connected together to the readout input through a multiplexer.

2.4 Address Decoder

According to the discussions in the above sections, the proposed block diagram of the system can be shown as below.

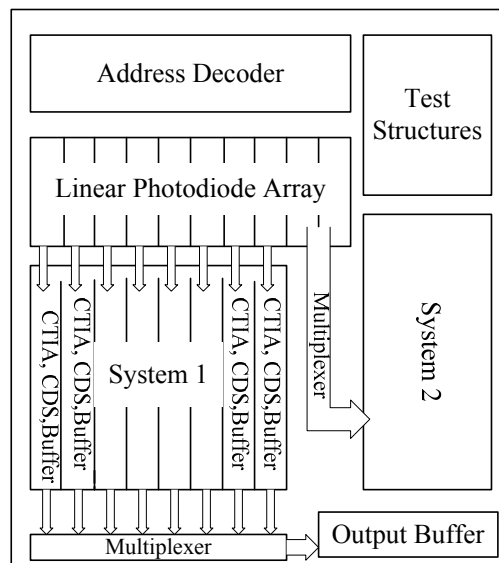
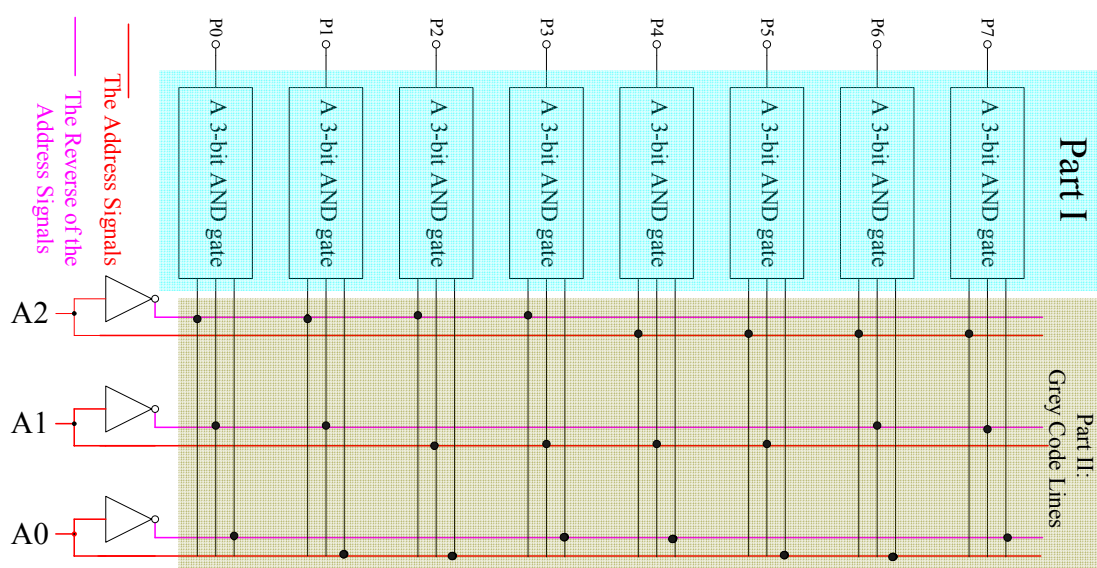


Figure 2. 7 The distribution of the chip

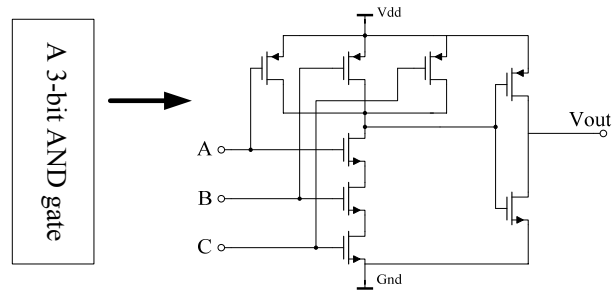
The 128 photodiodes are divided into two parts and connected to two different readout systems. But the 128 photodiodes are still sharing one set of address lines. Each photodiode is selected independently through the address decoder, which sets one of its 128 outputs to “1” based on those unsigned binary values on the 7 address lines. Here the decoder is implemented based on the grey code.

The associated circuitry is divided into two parts as shown in Figure 2. 8: (1) an array of 7-bit AND gates; (2) 7 grey decoder lines, which carry the address signals and their reverse signals. The layouts of the two parts manually, which are optimized to fit into the pitch as narrow as 7.2um.

The main drawback of this structure is that it consumes a large number of transistors, which is area-consuming and power-consuming. It results in a high capacitive load at the address inputs, which is contributed by the long runs of wires and the gate capacitance of the transistors. Therefore the address inputs will have to be buffered to provide enough driving capability. Furthermore the associated large capacitance also adds to long delays which may result in a shift in the achieved timing chart.



(a)



(b)

Figure 2. 8 A 3-bit example of the normal Grey-Code Decoder

In order to circumvent this problem, there is a structure called “dynamic NOR decoder” proposed in Figure 2. 9 [12]. The decoder works in two steps, as explained below:

(1) Pre-charge cycle: the terminal V_c is set as “Logic 0” and the address lines are kept in the high-impedance state. In such a case the PMOS transistors are all turned on. Charges are integrated onto those parasitic capacitors, keeping the voltages across them as around V_{dd} .

(2) Readout cycle: the terminal V_c is set as “Logic 1” and the address signals are conveyed onto the address lines. In such a case the PMOS transistors are turned off. Only the selected column has all its NMOS inputs as “Logic 0”. Since no discharging path is available for the corresponding parasitic capacitor, the voltage across it is read out as V_{dd} . In other words, this column output is set as “Logic 1” while the others are discharged to “Logic 0”.

The advantage of this structure is that the number of the used transistors is reduced by more than half. That thus reduces the power consumption and the chip area. The total gate capacitance is also reduced. But this structure also has two disadvantages: (1) the decoder speed is limited by the operation of pre-charge. (2) The PMOS transistor size must be designed carefully because it determines the dynamic performance and the

consumed area. The larger the PMOS transistor is, the faster the pre-charging is. (3) the timing becomes important in this case. There will be errors if the strobe signals are read in the wrong cycles. Thus extra control circuits may be needed to take care of the timing constraints.

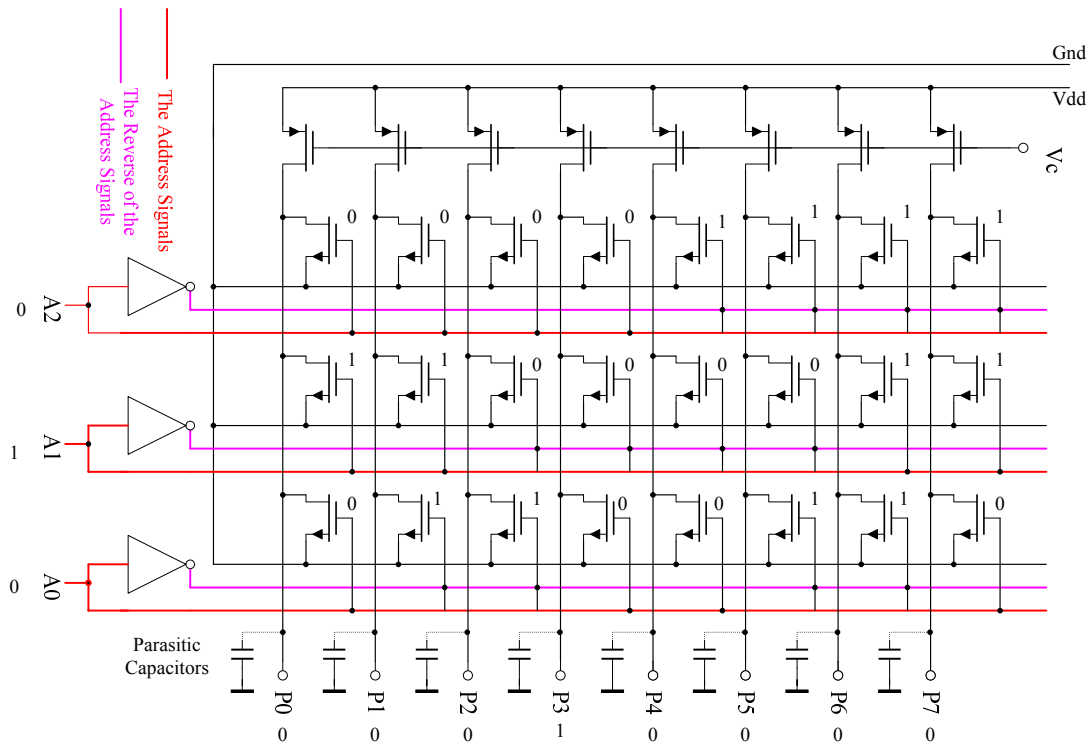


Figure 2. 9 A 3-bit example of the dynamic-NOR Grey-Code Decoder

The structure of the normal Grey-Code decoder is selected here, because it is simple for layout and requires no extra timing control. But the dynamic NOR decoder can be considered as an alternative.

2.5 Conclusion of this Chapter

In this chapter, the mapping from optical performances to the electrical considerations is done. The specific features in this photodetection and imaging are analyzed. Based on such analysis, a photodiode linear array is designed and two readout targets are

summarized for different applications. Solutions are also proposed. In applications with low leakage current, the principle of charge integration is applied to achieve high SNR at the cost of time. In this mode, the photo energy is accumulated together with the negligible leakage charge. On the other hand, in applications where the leakage current is non-ignorable, optical chopper and coherent detection are chosen to suppress the leakage-oriented error. Methods for minimizing noise and improving dynamic range are included in the design of a novel transimpedance amplifier for this application.

After the merits and demerits of the two principles are discussed theoretically, it will come to the detailed circuit implementations. System I will be introduced in Chapter 3 as a realization of Mode I using the charge integration principle; and System II will be introduced in Chapter 4 as a realization of Mode II using the coherent detection principle. All the techniques and simulation results will be presented there. Finally a comparison between the two principles is listed as the conclusion.

Principle	Principle I
Name	Charge Integration
Measurand	Accumulated photo-generated charge
Number of Shared Pixels	One pixel for One readout circuit (an linear array of APS)
Target	1. Improving the SNR at cost of time; 2. Improving the sensitivity at cost of area; 3. Improving the DR by using dynamic integration time control.
Applications	Where the leakage current is low
Disadvantage	1. Accuracy may be bad due to the leakage current; 2. Power consumption may be large so that extra powering-down techniques are required.

Principle	Principle II
Name	Coherent Detection
Measurand	Photocurrent
Number of Shared Pixels	16 Pixels sharing One readout circuit
Target	1. Reducing the leakage-caused error with the assistance of an optical chopper; 2. Achieving a high sensitivity.
Applications	Where the leakage current is high
Disadvantage	1. The readout speed may be low; 2. The optical chopper can not be integrated on chip; 3. The integration of the demodulation function is left to future work.

Table 2. 5 A comparison between the two principles

2.6 References

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Chapter 3 Implementation of Mode I: Charge Integration

As an extension of section 2.4.1, in which the working principle of charge integration is introduced, this chapter is focused on the corresponding circuit implementation. It starts with the introduction of traditional circuit structures and the proposal of an improved schematic for sensitivity enhancement. The encountered challenges and possible solutions for implementing this schematic are analyzed in section 3.2. After summarizing the key specifications in section 3.3, the architectures for each sub-block are built and simulated in section 3.4. Finally the analysis and the conclusions are given out.

3.1 Introduction to Charge integration and CTIA-APS

3.1.1 Traditional Structures and Drawbacks

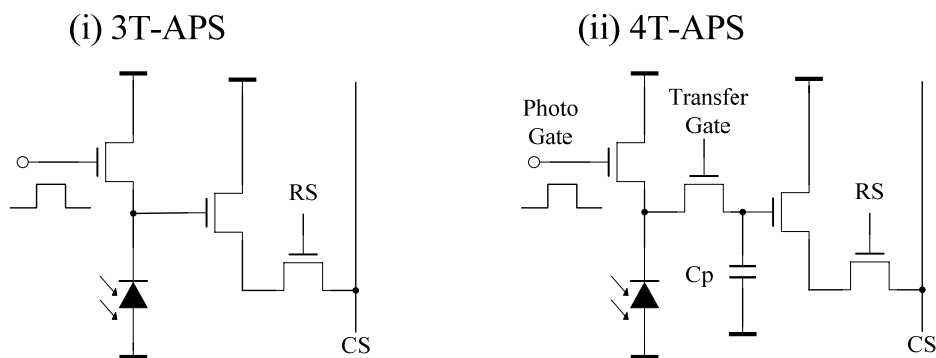


Figure 3. 1 the modern structures for detecting photocurrent [1]

A few modern structures for detecting photocurrent are shown in Figure 3. 1. For implementing the principle of charge integration, there are three indispensable elements: (1) a photoelectric device which is used for capturing light as small charge

carriers; (2) an integration capacitor which is used for storing the photo-generated charge before the charge is reset or transferred; (3) additional circuitry, which is used for output voltage reading and further signal processing, indispensably includes a sampling capacitor for charge-to-voltage conversion. In Figure 3. 1(i) the junction capacitor of the photodiode is also utilized for charge accumulation and charge-to-voltage conversion; In Figure 3. 1(ii) the photodiode functions as the photoelectric device while the capacitor C_p works as the integration and the sampling capacitor.

The 3T-APS is the most commonly used structure in CMOS image sensors, because it solved a lot of the noise problems. But it has three drawbacks as will be analyzed: (1) the sensitivity is hard to be improved; (2) the linearity is limited; (3) it suffers from a large reset noise component.

Sensitivity

The general expression of sensitivity is derived in Equation 3- 3 [2], where A is the active area for the photoelectric device; C_s is the sampling capacitor; $I(\lambda)$ is the illumination intensity with units lx; $V_o(\lambda)$ is the photopic luminous efficiency function; K_m is the constant scaling factor, which equals 683lm/W; $R(\lambda)$ is the responsivity with units A/W; $P(\lambda)$ is the optical power with units W/m²; S is the sensitivity with units V/ (lx*s). Here t_{int} is defined as the integration time.

$$P(\lambda) = \frac{I(\lambda)}{V_o(\lambda)K_m} \text{ (unit : W / m}^2\text{)} \quad \text{Equation 3- 1}$$

$$V = \frac{P(\lambda)R(\lambda)At_{int}}{C_s} \quad \text{Equation 3- 2}$$

$$S = \frac{V}{I(\lambda)t_{int}} = \frac{R(\lambda)A}{V_o(\lambda)K_mC_s} \text{ (unit : V / lx} \cdot \text{s)} \quad \text{Equation 3- 3}$$

In CMOS 3T-APS, the photodiode functions as the integration capacitor and the

sampling capacitor at the same time. Since the junction capacitor of the photodiode is proportional to the photodiode active area, Equation 3- 3 can be written as:

$$C_s = A \cdot C_0 \quad \text{Equation 3- 4}$$

$$S = \frac{R(\lambda)A}{V_0(\lambda)K_m \cdot AC_0} = \frac{R(\lambda)}{V_0(\lambda)K_m \cdot C_0} \quad \text{Equation 3- 5}$$

Where C_0 is the junction capacitance per unit area and is determined by the process. As shown in Equation 3- 5, none of the parameters that determine sensitivity is designable, which restricts the improvement of sensitivity.

Linearity

In the discussions above, C_0 is assumed to be a fixed value. But in real world C_0 varies as the charge integration goes on, because the voltage across the photodiode is changed. The relationship between C_0 and V is shown in Equation 3- 6 where ϵ_{si} is the silicon permittivity, N_A is the doping concentration and q is the elementary charge [3].

$$C_0(V) = \frac{1}{2} \sqrt{\frac{2q\epsilon_{si}N_A}{V}} \quad \text{Equation 3- 6}$$

The nonlinearity can be observed by rewriting Equation 3- 2 as below:

$$V = \frac{P(\lambda)R(\lambda)At_{\text{int}}}{C_s} = \frac{I(\lambda)R(\lambda)}{V_0(\lambda)K_m} \cdot \frac{t_{\text{int}}\sqrt{2V}}{\sqrt{q\epsilon_{si}N_A}} \quad \text{Equation 3- 7}$$

Where V is no longer proportional to the illumination $I(\lambda)$. This nonlinearity is due to the floating biasing of the photodetector during the readout.

3.1.2 An Improved Structure: CTIA

Taking into account the chip area in Y direction which is free for readout circuit design, the structure in Figure 3. 2 is proposed to implement a linear array of

CTIA-APS in order to circumvent the drawbacks mentioned above [2, 4]. CTIA is short for Capacitive Transimpedance Amplifier.

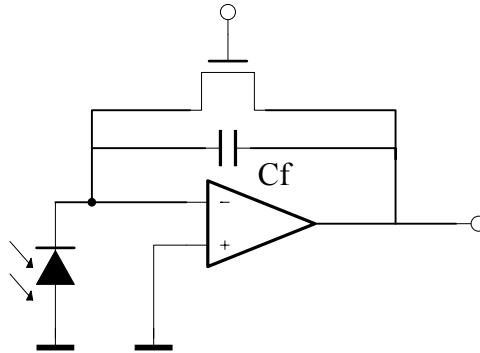


Figure 3. 2 the improved structure: CTIA-APS

Advantages

In this structure, the feedback capacitor C_f is used as the integration and sampling capacitor, while the photodiode functions as a photoelectric device. This CTIA-APS has three advantages:

- (1) The charge modulation is suppressed, since the junction capacitance is maintained as a constant value by biasing the photodiode with the virtual ground.
- (2) The sensitivity of the pixel can be designed flexibly. The sensitivity can be enhanced by increasing the light sensitive area of the photodiode or decreasing the feedback capacitor.
- (3) A better linearity is achieved, since the feedback capacitor can be implemented as poly-to-poly which is much less voltage-dependent and has higher accuracy.

Noise Considerations

Though having its sensitivity and linearity improved greatly, the CTIA-APS suffers from a few noise components just like the 3T-APS, as will be analyzed:

- (1) The reset noise

The reset noise is determined by the feedback capacitor, as is shown in Equation 3- 7 where R_{reset} is the off-resistance of the MOS switch. The smaller the feedback

capacitor is, the higher the reset noise is.

$$V_{n,reset} = \sqrt{4kTB R_{reset}} = \sqrt{4kTR_{reset} \cdot \frac{1}{4R_{reset}C_{int}}} = \sqrt{\frac{kT}{C_{int}}} \quad \text{Equation 3- 8}$$

(2) The flicker noise

The CTIA-APS is designed to work at low frequencies since long integration time is required for low-illumination detection. As will be discussed, an integration time as long as 500msec may be used. Hence the flicker noise is a big concern in such design.

(3) The spatial noise

The mismatch of the feedback capacitors between pixels contributes to the gain variations between the pixels, which leads to the spatial noise and can not be cancelled by CDS (Correlated Double Sampling). Calibration may be needed for each pixel.

3.1.3. Correlated Double Sampling

Reset Noise or Flicker Noise?

Correlated Double Sampling is commonly performed in image sensors to reduce reset noise and flicker noise. In structures like photogate or pinned photodiode, both noise components can be removed effectively. But in the CTIA-APS, CDS only removes one of them, depending on the timing chart used.

The effect of CDS is analyzed referring to Figure 3. 3. The expressions for Sample 1, 2 and 3 are listed in Table 3. 1, where $V_{reset,in}$, $V_{1/f,in}$ and $V_{thermal,in}$ stands for the reset noise, the flicker noise and the thermal noise in Sample i respectively. V_{reset} stands for the output voltage during the reset. The relationships between the samples are listed as below:

(1) Since Sample 1 and Sample 2 are taken within the same frame, they are fully correlated, i.e. $V_{reset,1n} = V_{reset,2n}$;

(2) Since Sample 2 and Sample 3 are taken within a short time interval ΔT , the two samples have their flicker noises correlated at frequencies lower than $1/\Delta T$, i.e.

$$V_{1/f,1n} = V_{1/f,2n}$$

Sample	Expression
Sample 1	$V_{reset} + V_{reset,1n} + V_{thermal,1n} + V_{1/f,1n}$
Sample 2	$V_{reset} + V_{reset,2n} + V_{thermal,2n} + V_{1/f,2n} + V_{sig}$
Sample 3	$V_{reset} + V_{reset,3n} + V_{thermal,3n} + V_{1/f,3n}$

Table 3. 1 Expressions of samples including noises: CDS

Hence two equations can be derived as below:

Sample2 – Sample1

$$= \sqrt{V_{thermal,1n}^2 + V_{thermal,2n}^2} + \sqrt{V_{1/f,1n}^2 + V_{1/f,2n}^2} + V_{sig} \quad \text{Equation 3- 9}$$

Sample2 – Sample3

$$= \sqrt{V_{thermal,2n}^2 + V_{thermal,3n}^2} + \sqrt{V_{reset,2n}^2 + V_{reset,3n}^2} + V_{sig} \quad \text{Equation 3- 10}$$

Therefore, by subtracting Sample 2 and Sample 1 the reset noise is reduced; by subtracting Sample 2 and Sample 3 the flicker noise is reduced.

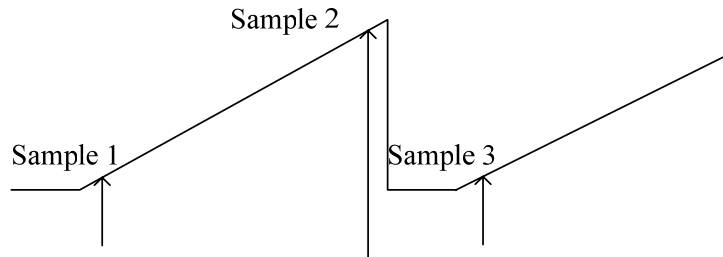


Figure 3. 3 the timing chart used for the noise analysis in CDS

Quadra Sample Method

A method called “Quadra Sample Method” [5] is explored to reduce noise further for the CTIA-APS. The timing chart is shown below in Figure 3. 4. There are four samples taken within each frame. The expressions of samples are listed in Table 3. 2. The relationships between samples are explained as below:

- (1) Since Sample 2 and Sample 3 are taken within the same frame, their reset noises are considered correlated, i.e. $V_{reset,2n} = V_{reset,3n}$;
- (2) Since Sample 1 and Sample 2 are taken with a short interval, their flicker noises are considered correlated, i.e. $V_{1/f,1n} = V_{1/f,2n}$;
- (3) Since Sample 3 and Sample 4 are taken with a short interval, their flicker noises are considered correlated, i.e. $V_{1/f,3n} = V_{1/f,4n}$;

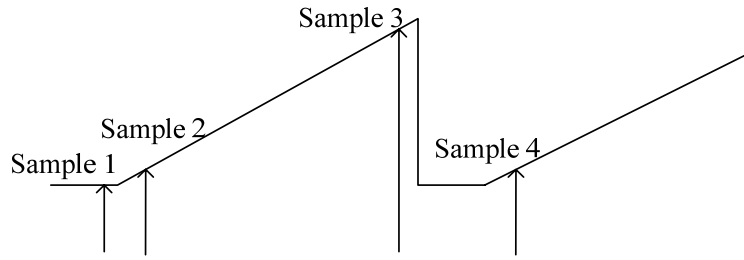


Figure 3. 4 the timing chart used for the noise analysis in CDS

Sample	Expression
Sample 1	$V_{reset} + V_{thermal,1n} + V_{1/f,1n}$
Sample 2	$V_{reset} + V_{reset,2n} + V_{thermal,2n} + V_{1/f,2n}$
Sample 3	$V_{reset} + V_{reset,3n} + V_{thermal,3n} + V_{1/f,3n} + V_{sig}$
Sample 4	$V_{reset} + V_{thermal,4n} + V_{1/f,4n}$
Sample 2-Sample 1	$\sqrt{V_{thermal,1n}^2 + V_{thermal,2n}^2} + V_{reset,2n}$
Sample 3-Sample 4	$\sqrt{V_{thermal,3n}^2 + V_{thermal,4n}^2} + V_{reset,3n} + V_{sig}$

Table 3. 2 Expressions of samples including noises: Quadra Sample Method

$$(Sample3 - Sample4) - (Sample2 - Sample1)$$

$$= \sqrt{V_{thermal,1n}^2 + V_{thermal,2n}^2} + \sqrt{V_{thermal,3n}^2 + V_{thermal,4n}^2} + V_{sig} \quad \text{Equation 3- 11}$$

Since Sample 1 is taken during the reset, there is no reset noise in this sample. As is shown in Equation 3- 11, by proper signal processing, both the flicker noise and the reset noise are reduced effectively. But the price to pay is that the thermal noise is increased.

Schematics for CDS

In our design, the in-pixel subtraction is implemented for CDS. In this case, no additional subtraction circuit is required. Figure 3. 5 shows the schematics [2] . The operation is shown in Figure 3. 6. Figure 3. 5 (a) can realize $V_{in1} - V_{in2}$ or $V_{in2} - V_{in1}$, depending on the timing chart. Figure 3. 5 (b) is the simplified schematic and only utilized for $V_{in2} - V_{in1}$.

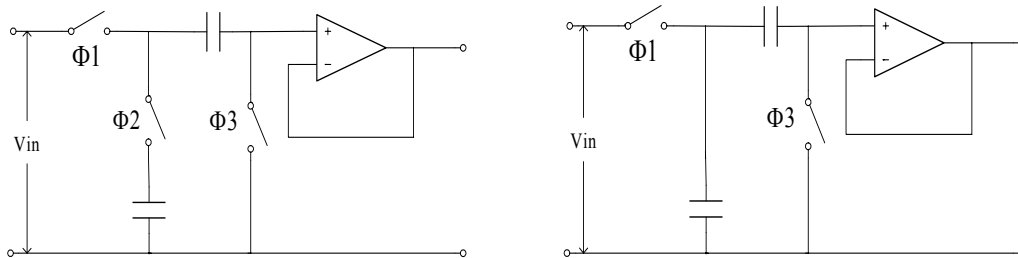


Figure 3. 5 (a) Schematic for CDS

(b) Simplified Schematic for CDS

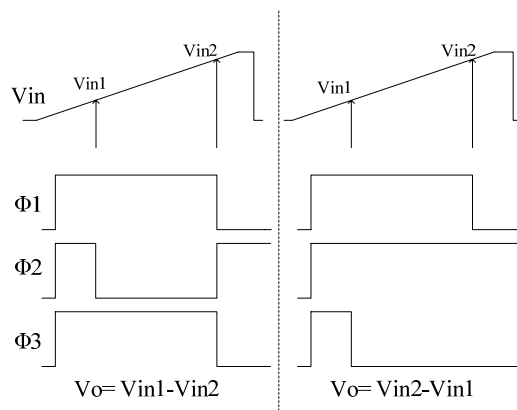


Figure 3. 6 Two Operations of the CDS in Figure 3.5 (a)

3.1.4 Variable Integration Duration Control

Equation 3- 12 is the transfer function for the i_{th} pixel, where N_i is a constant related to light wavelength λ_i , and t_{int_i} is defined as the integration time for the i_{th} pixel. S_i is defined as the sensitivity of the i_{th} pixel. Equation 3- 13 shows that it is the rate of output voltage increase that shows how large the light intensity is.

$$V_i = \frac{I(\lambda_i)R(\lambda_i)}{V_0(\lambda_i)K_m} \cdot \frac{At_{int_i}}{C_f} = N_i \cdot I(\lambda_i)t_{int_i} \quad \text{Equation 3- 12}$$

$$I(\lambda_i) = \frac{1}{N_i} \cdot \frac{V_i}{t_{int_i}} \Rightarrow S_i = \frac{V_i}{t_{int_i}} \quad \text{Equation 3- 13}$$

In order to perform a reliable measurement, the readout has three options of control: (1) fixing the integration time; (2) fixing the voltage difference; (3) varying the integration time based on fixed rules. The last two options allow the integration time adapted to the illumination by further signal processing and proper control circuits, which can improve the dynamic range of measurement.

Fixed Integration Time

The integration interval is fixed as t_{int_0} for all the pixels. The samples are taken when $t = T_a$ and T_b respectively. Hence,

$$S_i = \frac{V_i}{t_{int_0}} = \frac{V_{ia} - V_{ib}}{t_{int_0}} \quad \text{Equation 3- 14}$$

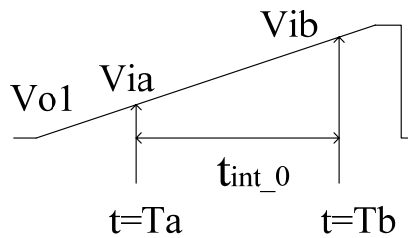


Figure 3. 7 the Sampling Timing for the Fixed Integration Time

In this case, the dynamic range is limited. But under such control, the signal can be processed flexibly. Techniques like the CDS and the Quadra Sample Method can be applied simply.

Fixed Voltage Difference

The voltage difference is fixed as V_{i0} for all the pixels. The integration time consumed by the CTIA-APS to achieve this voltage difference is recorded by the control circuit as t_i . Hence,

$$S_i = \frac{V_{i0}}{t_i} = \frac{V_{i0}}{t_a - t_b} \quad \text{Equation 3- 15}$$

The working principle for Fixed Voltage Difference Control is shown in Figure 3. 8 [6]. A clock signal is necessary in such control circuit.

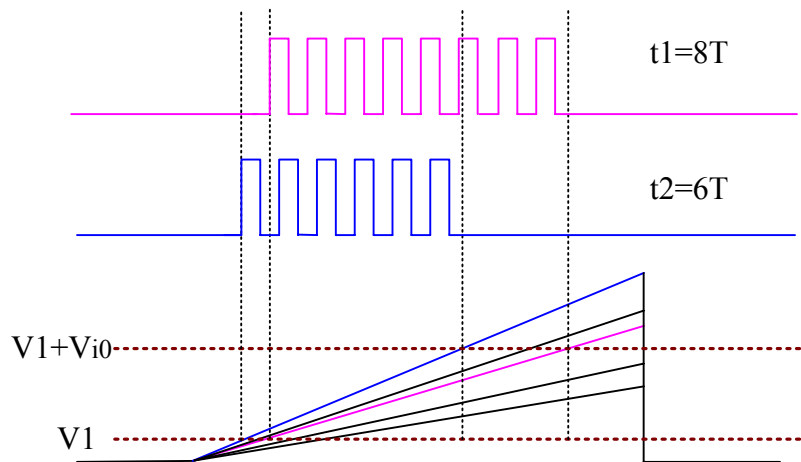


Figure 3. 8 the working principle for the Fixed Voltage Difference Control

There are three advantages about this control:

- (1) The improvement of SNR can be performed by increasing V_{i0} within the acceptable range;
- (2) The dynamic range is no longer limited by the saturation voltage. In such case it depends on the clock frequency, which determines the maximum detectable

photocurrent, and the temporal noise, which determines the minimum detectable photocurrent, as is shown in Equation 3- 16. In Equation 3- 16, σ_r^2 is the temporal noise contributed the readout circuit and B is the noise bandwidth determined by the reset network.

$$DR = 20 \log_{10} \frac{I_{max\,sig}}{I_{min\,sig}} = 20 \log_{10} \frac{f_{clk} V_{i0} C_f - I_{leakage}}{\sqrt{\sigma_r^2 B^2 + 2qI_{leakage} B}} \quad \text{Equation 3- 16}$$

If a large time constant can't be implemented for the reset network or the CDS circuit, the maximum integration time is limited to t_{max} , which changes the minimum detectable photocurrent. Hence the dynamic range is reduced to:

$$DR = 20 \log_{10} \frac{(f_{clk} V_{i0} C_f - I_{leakage}) \cdot t_{max}}{V_{i0} C_f - I_{leakage} t_{max}} \quad \text{Equation 3- 17}$$

(3) Under this control rule, the CTIA-APS can be made more integrated, with the control circuits and the A/D conversion integrated in pixel. An example is shown in Figure 3. 9. By counting the clock cycles that are consumed to achieve V_{i0} , the A-to-D conversion is performed. Hence a digital counter can be simply integrated as an A/D converter.

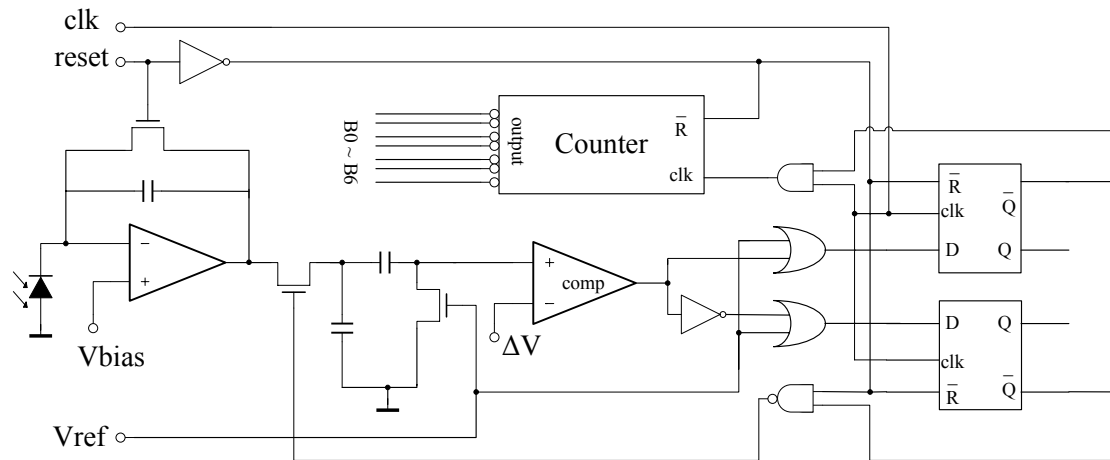


Figure 3. 9 a proposed schematic for the Fixed Voltage Difference Readout

Variable Integration Time based on Fixed Rules

The integration time and the voltage difference can be made tunable. The latter is tuned in order to optimize the SNR while the former is tuned to maximum the dynamic range. But this option involves more complicated control and processing.

3.1.5 Summary of Approaches

In this section, the approaches utilized for performance optimization are summarized. Section 3.2 will focus on the circuit implementation of these approaches. The challenges encountered in the circuit implementation would be pointed out. A block diagram for the CTIA-APS is summarized as is shown in Figure 3. 10. It's noticed that the digital control circuit is implemented outside the chip so as to verify the ideas discussed above flexibly.

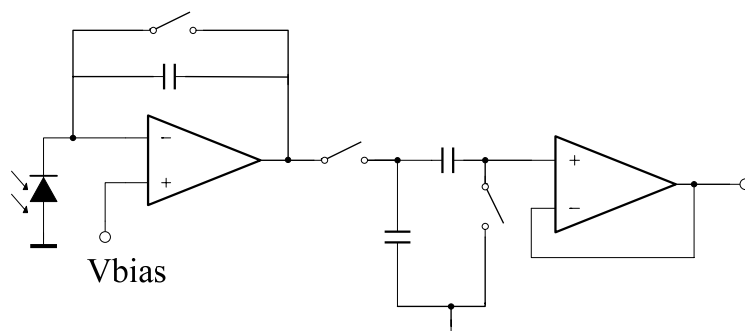


Figure 3. 10 the schematic for this design of charge integration

Approach	Target
CTIA	Enhancing sensitivity and linearity
CDS	Reducing fixed pattern noise, flicker noise and reset noise
Variable Integration Time (Fixed Voltage Difference Control)	Improving Dynamic Range; Assuring a high SNR

Table 3. 3 Approaches used in readout design

3.2 Specifications and Implementations

3.2.1 Specifications: the range of the detectable photocurrent

In order to obtain the specifications of the photocurrent to be detected, a research on illumination is done first. In Table 3. 4 list the light intensities of several typical LEDs, which may be used in microspectrometers as the light source.

Type	Color	Luminous intensity	Viewing Angle	Wavelength
Standard	Red	5mcd @ 10mA	60°	660nm
Standard	Bright Red	80mcd @10mA	60°	625nm
Standard	Yellow	32mcd @ 10mA	60°	590nm
Standard	Green	32mcd @ 10mA	60°	565nm
High Intensity	Blue	60mcd @ 20mA	50°	430nm
Super Bright	Red	500mcd @ 20mA	60°	660nm
Low current	Red	5mcd @ 20mA	60°	625nm

Table 3. 4 Typical LEDs with light intensity [7]

The luminous intensity is the brightness of the LED at give current and “mcd” means milli candela. Based on the datum in Table 3. 4, the following calculations are done to provide a reference for deciding the photocurrent range in our design.

A LED that emits 32mcd with a radiation angle of 30° has its light intensity as F (units: lumens):

$$F = \frac{I_v}{M_{sr@30^\circ}} = \frac{32 \times 10^{-3}}{4.671} = 6.85 \times 10^{-3} \quad \text{Equation 3- 18}$$

The illuminance for the total light sensitive area A_{tot} , i.e. for the 128 pixels, is

calculated as (units: lx):

$$I(\lambda) = \frac{F}{A_{tot}} = \frac{6.85 \times 10^{-3}}{128 \times 7.2 \times 300 \times 10^{-12}} = 24.78 \times 10^3 \quad \text{Equation 3- 19}$$

Then the photocurrent generated within each pixel under this illumination is calculated as (units: A):

$$\begin{aligned} I_{photo} &= \frac{I(\lambda)AR(\lambda)}{V_0(\lambda)K_m} \\ &= \frac{(24.78 \times 10^3) \times (4.2 \times 300 \times 10^{-12}) \times (300 \times 10^{-3})}{1 \times 683} = 13.7n \end{aligned} \quad \text{Equation 3- 20}$$

Table 3. 4 and the calculations above show that it is typical of a LED to produce a photocurrent of tens of nano-ampere, based on the photodiode size designed in Chapter 2. After the low luminosity of the dispersion system is considered, which is lower than 10%, the photocurrent range to be detected is set as 1pA~ 10nA, with a dynamic range of 80dB.

3.2.2 Specifications: Sensitivity and the Feedback Capacitor

The junction capacitance of each photodiode can be estimated as below:

$$\begin{aligned} C_s &= C_j A + C_{jsw} l \\ &= 2.31 \times 10^{-4} \times 7.2 \times 300 \times 10^{-12} + 2.55 \times 10^{-10} \times 614.4 \times 10^{-6} \\ &\approx 660 fF \end{aligned} \quad \text{Equation 3- 21}$$

The feedback capacitor is accordingly chosen as $C_f = 500fF$. The conversion gain is calculated as $320nV/e^-$. The reset noise is calculated at the room temperature as:

$$\langle n_{reset} \rangle = \frac{\sqrt{kTC_f}}{q} \approx 300e^- \quad \text{Equation 3- 22}$$

The sensitivity is then estimated at the wavelength of 555nm as:

$$S = \frac{R(\lambda)A}{V_0(\lambda)K_m C_f} = \frac{300 \times 10^{-3} \times (4.2 \times 300 \times 10^{-12})}{1 \times 683 \times 500 \times 10^{-15}} \approx 1.5V/lx \cdot s \quad \text{Equation 3- 23}$$

3.2.3 Specifications: Variable Integration Time

Fixed Voltage Difference Control

A proper choice of V_{i0} is based on three considerations: (1) the input biasing and the output swing of the main amplifier; (2) the temporal noise of the main amplifier and the required SNR; (3) the dynamic range and the maximum integration time that can be achieved.

(1) The input biasing voltage is set tunable between 0.9V~1.6V based on the consideration of minimizing leakage current. The output is designed to swing from 0.3V to 2.9V. Hence V_{i0} can be set somewhere between 1V and 2V.

(2) The larger V_{i0} is, the better the SNR is. Ignoring the influence of leakage current, the SNR is expressed as below, where σ_r^2 is in the units of e^- :

$$SNR = 20 \log_{10} \frac{V_{i0} C_f}{\sqrt{\sigma_r^2 + 2qV_{i0} C_f}} \quad \text{Equation 3- 24}$$

The temporal noise of the main amplifier is estimated as $300e^-$. Then the SNR can be calculated for $V_{i0}=1V$ and $V_{i0}=2V$ respectively:

$$\begin{aligned} SNR|_{V_{i0}=2V} &= \\ 20 \log_{10} \frac{2 \times 500 \times 10^{-15}}{\sqrt{(300 \times 1.6 \times 10^{-19})^2 + 2 \times 1.6 \times 10^{-19} \times 2 \times 500 \times 10^{-15}}} & \quad \text{Equation 3- 25} \\ \approx 68dB & \end{aligned}$$

$$SNR|_{V_{i0}=1V} = 20 \log_{10} \frac{1 \times 500 \times 10^{-15}}{\sqrt{(300 \times 1.6 \times 10^{-19})^2 + 1.6 \times 10^{-19} \times 2 \times 500 \times 10^{-15}}} \approx 65dB$$

Equation 3- 26

Therefore on one hand, a SNR larger than 60dB can be achieved with V_{i0} set as 1V; on the other hand, the increase of V_{i0} from 1V to 2V doesn't improve the SNR effectively.

(3) A larger V_{i0} requires a longer integration time, which may degrade the linearity especially for the low illuminations. As analyzed in Table 3. 5, for $V_{i0}=2V$ an integration time as long as 1sec is required, which is difficult for the on-chip implementation.

$V_{i0} \backslash I_{ph}$	1pA	10pA	100pA	1nA	10nA
1V	500ms	50ms	5ms	500us	50us
2V	1s	100ms	10ms	1ms	100us

Table 3. 5 Required Integration Time for different V_{i0} and different photocurrents

Hence, V_{i0} is chosen as 1V. After considering the range of the detected photocurrent, the clock frequency in the Fixed Voltage Difference Control is determined for $V_{i0}= 1V$ according to Table 3. 5, i.e.:

$$f_{clk} \geq \frac{1}{50\mu sec} = 20kHz$$

Equation 3- 27

Variable Voltage Difference and Variable Integration Interval

A table is made to assign a proper integration time for a photocurrent. As is shown in Table 3. 6, the detected photocurrent is divided into 12 levels. Each level is assigned a specific t_{int} . In such way, the amount of the accumulated charge is assured and the

high SNR is achieved. It will be verified in the measurement.

I _{ph}	T _{int}	I _{ph}	T _{int}	I _{ph}	T _{int}
1p~2p	450ms	2p~5p	180ms	5p~10p	90ms
10p~20p	45ms	20p~50p	18ms	50p~100p	9m
100p~200p	4.5ms	200p~500p	1.8ms	500p~1n	900u
1n~2n	450us	2n~5n	180us	5n~10n	90u

Table 3. 6 Varied Integration Time for Varied Voltage Difference

3.2.4 Summary of the Systematic Specifications

Based on the discussions above, some parameters and target specifications are summarized.

Specifications	Value
Current range	1pA~10nA
Parasitic capacitor	Around 660fF
Integration time	9usec ~ 500msec
Feedback capacitor	500fF
Biasing for photodiode	Tunable, 0.9V~1.6V
Leakage current	Around 20 fA
Output Swing	0.3V~ 2.9V

Table 3. 7 Systematic Specifications and Considerations

3.3 Circuit Implementation of Each Block

3.3.1 Input Capacitive Transimpedance Amplifier: input CTIA

Amplifier

The amplifier in the input CTIA is the main front-end amplifier. Its performance is critical for the whole readout. There are four requirements for this amplifier:

- (1) The amplifier should be designed with low noise. An input referred noise of 2mV_{rms} contributes to a temporal noise of $6250e^-$.
- (2) The amplifier should be designed with high open-loop gain to stabilize the input biasing point.
- (3) The amplifier should be designed with a large output swing to maximize the well capacity.
- (4) The amplifier should be designed with low power consumption, since there are 128 APS in total.

Figure 3. 11 show the schematic of the amplifier used in CTIA. It is configured by a two-stage differential-input single-ended amplifier. The two-stage structure is chosen to obtain a large input common mode range as well as a large output swing. The first stage is a folded-cascode amplifier. P-MOSFET is used as the input transistors pair, which brings two benefits: (1) it is good for reducing the flicker noise; (2) the input biasing voltage can be set lower to 0.3V , which is good for suppressing the photodiode leakage current. The miller compensation is also used for stabilization, resulting in a capacitive load driving capability of 3pF . The achieved specifications are listed in Table 3. 8.

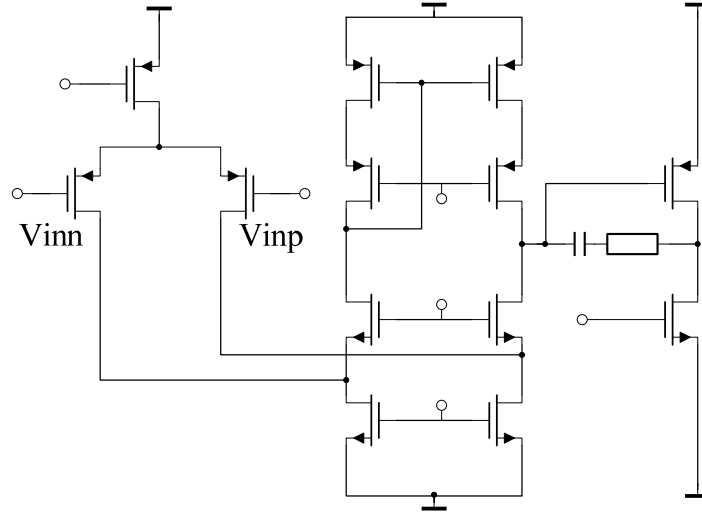


Figure 3. 11 Schematic of the OTA of the CTIA

Specifications	Value
Input CMR	0.22V~2.2V
Clload	0~3pF
GBW	>5M
Slew Rate	2V/usec
Output swing	0.22V~3.0V
Phase Margin	>60degrees
Input Referred Noise (white)	80nV/sqrt(Hz) @ 10kHz
Input Referred Noise (flicker)	7.5uV/sqrt(HZ) @ 1Hz
Settling time (0.1%)	<550ns
Power Consumption	25uA
Open Loop Gain	123dB

Table 3. 8 Specifications for the Input Charge Amplifier

Reset Switch

A T-type switch is utilized as the reset switch [8]. The T-type structure is chosen to provide a large time constant when the reset switch is off, which allows a good linearity within a long integration time. The transistor sizes are chosen properly to

minimize the charge injection. The schematic is shown in Figure 3. 12.

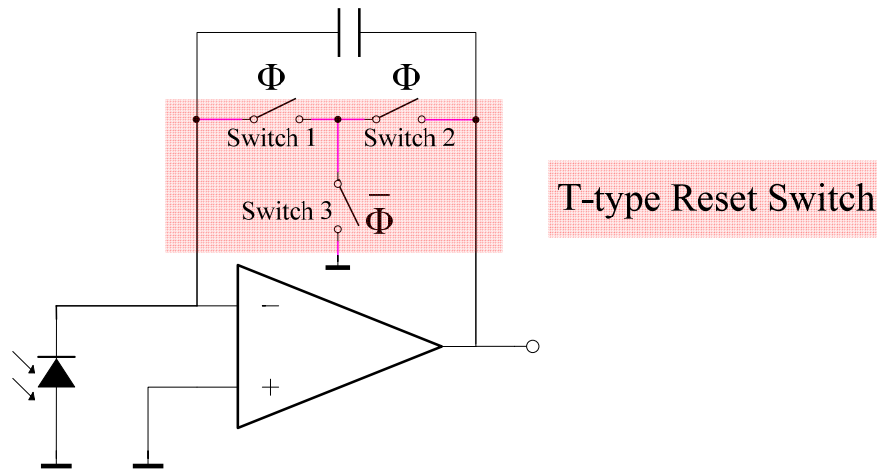


Figure 3. 12 a T-type switch used as the reset switch

The equivalent off-resistance of the T-type switch is calculated as blow:

$$R_{offeq} = \frac{R_{off1} \cdot R_{off2}}{R_{on3}} \gg R_{off1} \quad \text{Equation 3- 28}$$

Where R_{offeq} is the equivalent off-resistance of the T-type reset switch; R_{off1} , R_{off2} are the off-resistance of the switch 1 and the switch 2 respectively; R_{on3} is the on-resistance of the switch 3.

3.3.2 CDS Circuit

The working principle of CDS has been introduced in section 3.1.3. The simplified schematic is chosen for the on-chip implementation. The schematic and the timing chart are shown in Figure 3. 13 further.

Switches

The requirements on the switch $\Phi 1$ and the switch $\Phi 2$ are different: (1) for $\Phi 1$ a large input voltage range is required. The switch $\Phi 1$ has its input voltage probably ranging from 0.3V to 2.9V, depending on the photodiode biasing and the charge accumulation. (2) For $\Phi 2$ a large off-resistance is required and the charge injection should be minimized. The switch $\Phi 2$ is kept off for a long integration time, especially when the

illumination is low. It should be able to prevent C_r from being discharged after the reference voltage (V_r) is sampled onto C_r .

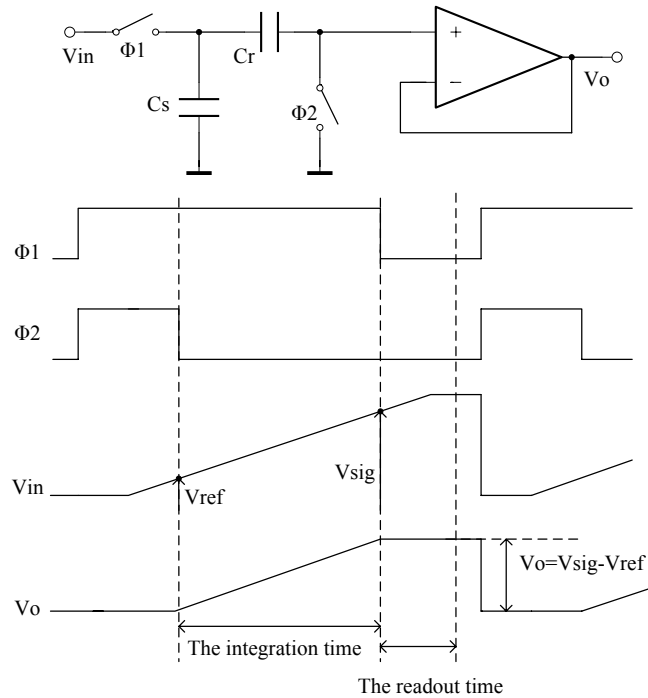


Figure 3. 13 the schematic for the on-chip implementation of CDS

The switch Φ_1 is implemented as the complementary switch to obtain the full input and output swing, as is shown in Figure 3. 14 (a) and (b). The switch Φ_2 is implemented with the dummy switch to minimize the charge injection effect, as is shown in Figure 3. 14 (c).

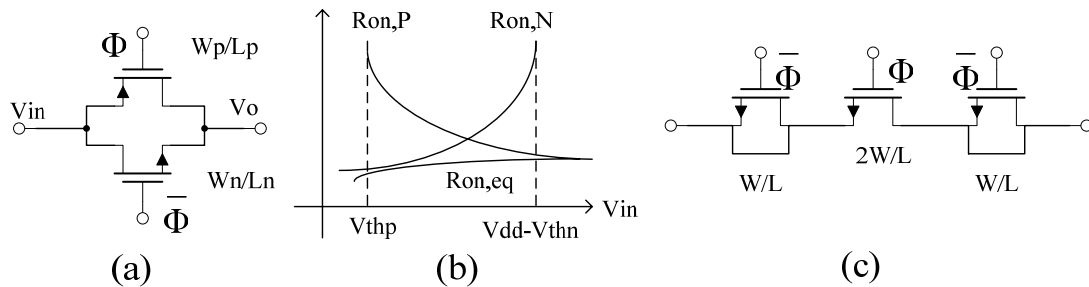


Figure 3. 14 (a) complementary MOS switch; (b) on-resistance V.S. input voltage in the complementary switch; (c) the dummy switch [9]

Components' values for CDS

The sampling capacitors are both chosen as 1pF, after considering the kTC noise introduced by the CDS circuits. The sizes for the transistors and the capacitors are summarized in Table 3. 9, referring to Figure 3. 14.

Cr	Cs	Wp	Lp	Wn	Ln	W	L
1pF	1pF	2um	0.6um	1um	0.6um	1um	0.6um

Table 3. 9 the transistors and the capacitors used for CDS

3.3.3. Column Output Buffer

The outputs of all pixels are connected together so as to be read out. A multiplexer will be used for pixel selection. Thus a Column Output Buffer is designed for each pixel to avoid the parasitic effects of wiring capacitances. It should be noticed that the input voltage range of the buffer could be 0.9V~2.9V. The schematic and the achieved specifications are listed in Figure 3. 15 and Table 3. 10 respectively.

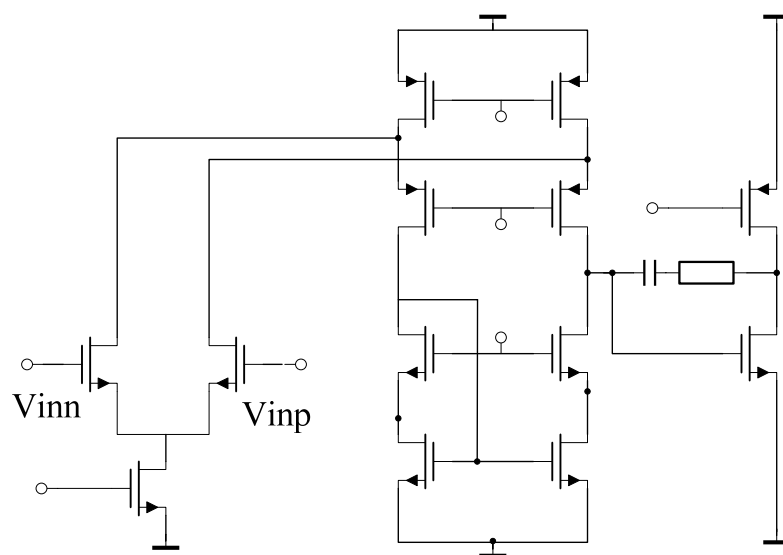


Figure 3. 15 Schematic of the Column Output Buffer

Specifications	Value
Input CMR	0.9V~2.9V
Clload	0~2pF
GBW	>7M
Slew Rate	2V/usec
Output swing	0.3V~2.9V
Phase Margin	>60degrees
Input Referred Noise (white)	90nV/sqrt(Hz) @ 10kHz
Input Referred Noise (flicker)	7.8uV/sqrt(HZ) @ 1Hz
Settling time (0.1%)	600ns
Power consumption	25uA
Open Loop Gain	123dB

Table 3. 10 Specifications for the Column Output Buffer

3.3.4 Digital Control Circuit

In CMOS image sensors the pixels are always selected and operated in sequence since they are using a fixed integration time. In order to maximize the time efficiency, the pixels in this linear imaging system are designed so that they can be selected specifically by proper programming. The purpose is to enable different integration time for different pixels.

The digital control circuit is used in each pixel. It functions to translate the global control signals into the local control signals based on address strobe. As is shown in Figure 3. 16, there are four control signals in total, for the operations of reset, S&H and readout. The address strobe consisted of a 7-bit AND gate and a Grey-code decoder, is as introduced in Chapter 2.

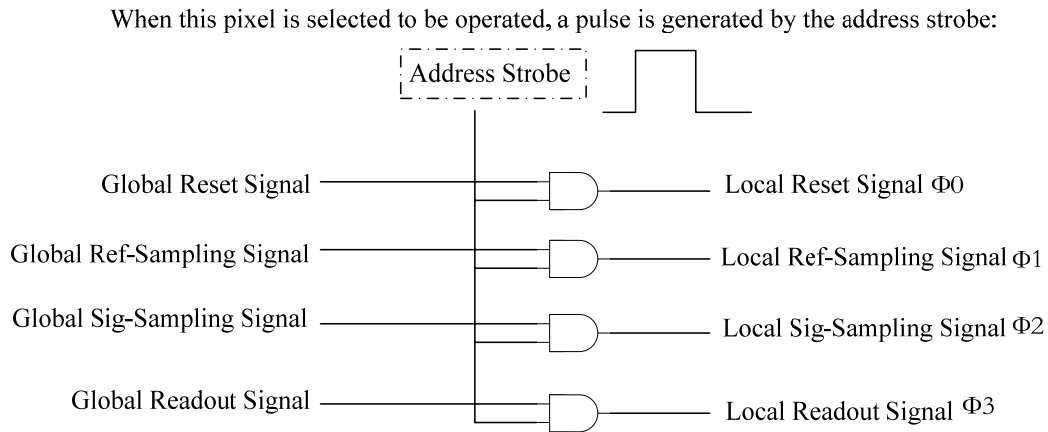


Figure 3. 16 Digital Control Circuit: from global control to local control signals

3.3.5 Systematic Output Buffer

This systematic output buffer is placed between the systematic output node and the bonding pad, providing enough capacitive and resistive driving capability. As will be discussed, we reuse the amplifier designed in Chapter 4 to reduce the design cycle, with its schematics and performance listed in Figure 4. 21 and Table 4. 13.

3.3.6 Summary of the Column Readout Circuits

Figure 3. 17 shows the block diagrams and the distributions of the column readouts. Four pixels of CTIA-APS are taken as an example. The switches before the Systematic Output Buffer are designed as the complementary switches to obtain a full input swing.

3.4 Timing Chart and Analog Signal Processing

The discussions above mainly focus on the inner structure of each pixel. It is explain now how the blocks inside a pixel are working with the global bus. Figure 3. 18

shows the timing chart of one pixel during the CDS operation. The photocurrent is integrated through the CTIA in Phase II and Phase III. The effective integration time is the duration of Phase III, because $V_o = V_s - V_r$ is sampled as the effective output. The transient simulation results accords with this signal chronogram well.

3.5 Layout of Mode I

The layout overview for each column of CTIA-APS is shown below, which is consisted of five parts: (1) the input CTIA; (2) the in-pixel CDS circuit; (3) the output buffer; (4) the digital control circuit generating local control signals; (5) the grey code line. The overviews of the layout are shown below for each block.

3.6 Conclusion of this Chapter

In this Chapter, a CMOS CTIA-APS linear array is implemented. A CTIA-APS is actually a photodiode with its readout working in the charge integration mode. The sensitivity and linearity are enhanced by applying the Capacitive Transimpedance Amplifier. The SNR is improved by Correlated Double Sampling, long integration time and large light sensitive area; the DR is improved by variable integration time. A control rule using Fixed Voltage Difference is introduced, which improves the dynamic range and is suitable for system integration. After the systematic analysis, the readout circuits are specified and implemented. Their transient simulations accord well with the theoretical analysis. The performance improvements are obtained in this design at the cost of power consumption, chip area and detection rate. These costs are acceptable and useful in microspectrometers for low-illumination detection, though unacceptable in CMOS image sensors.

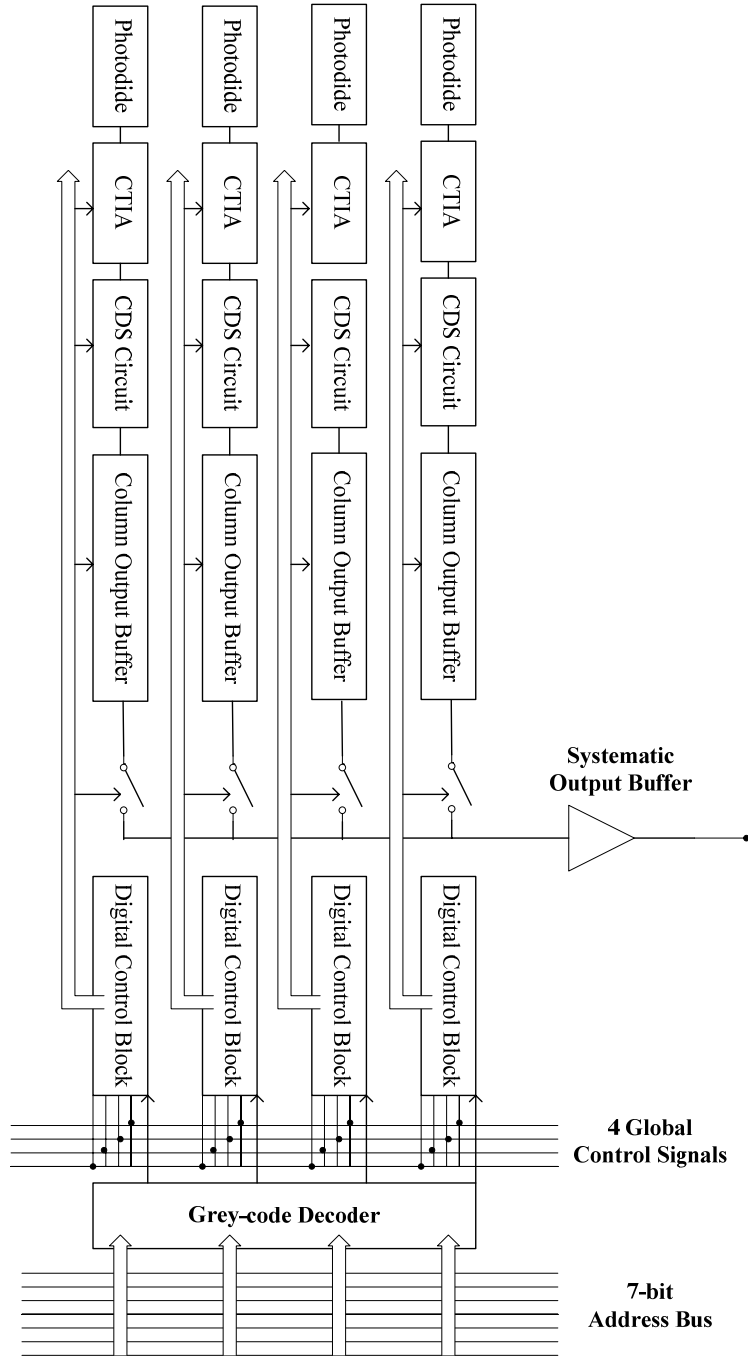


Figure 3. 17 Diagram of the Column Readout Circuits taking 4 APS as an example

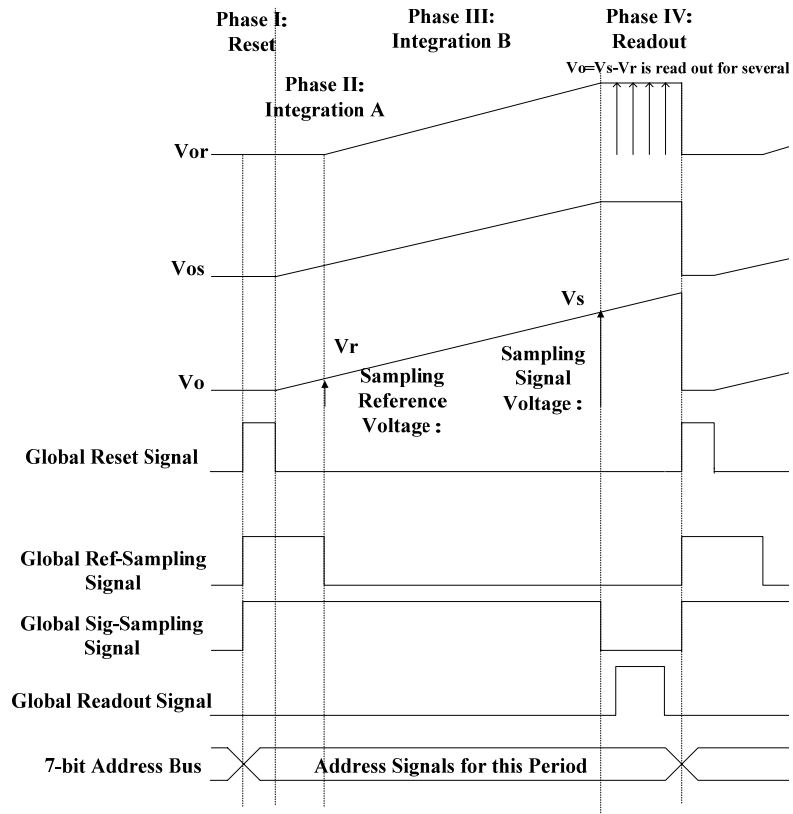


Figure 3. 18 the timing chart for the pixel operation in one period

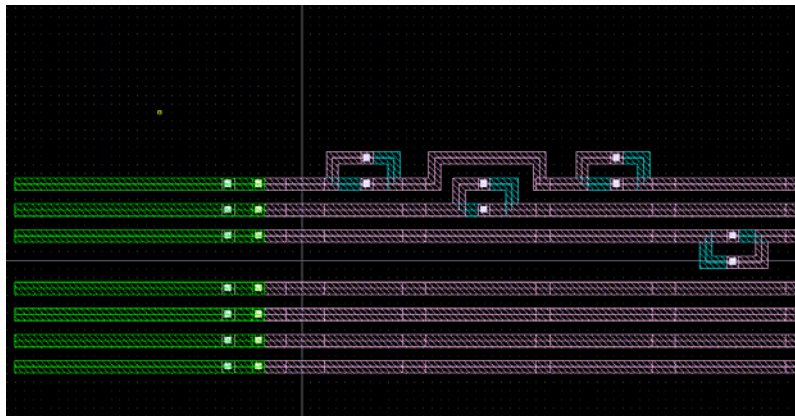


Figure 3. 19 (a)

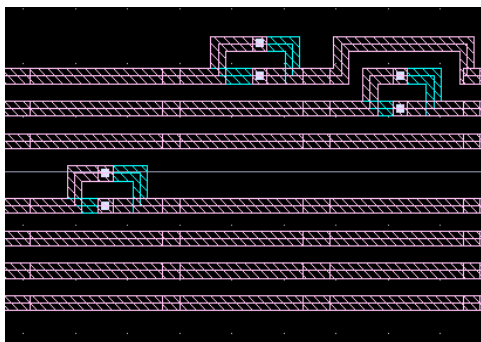


Figure 3. 19 (b)

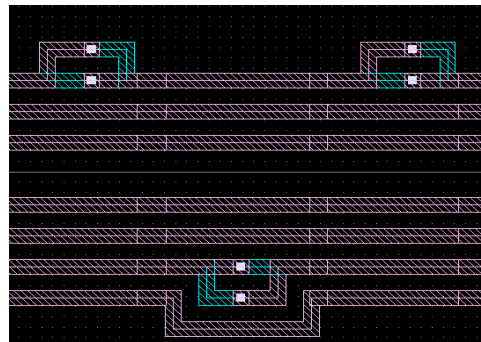
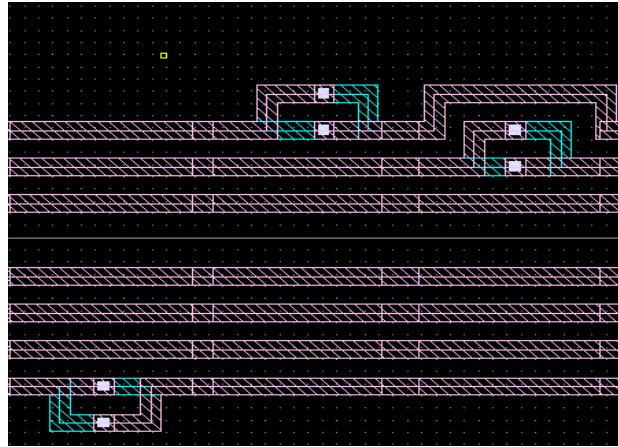
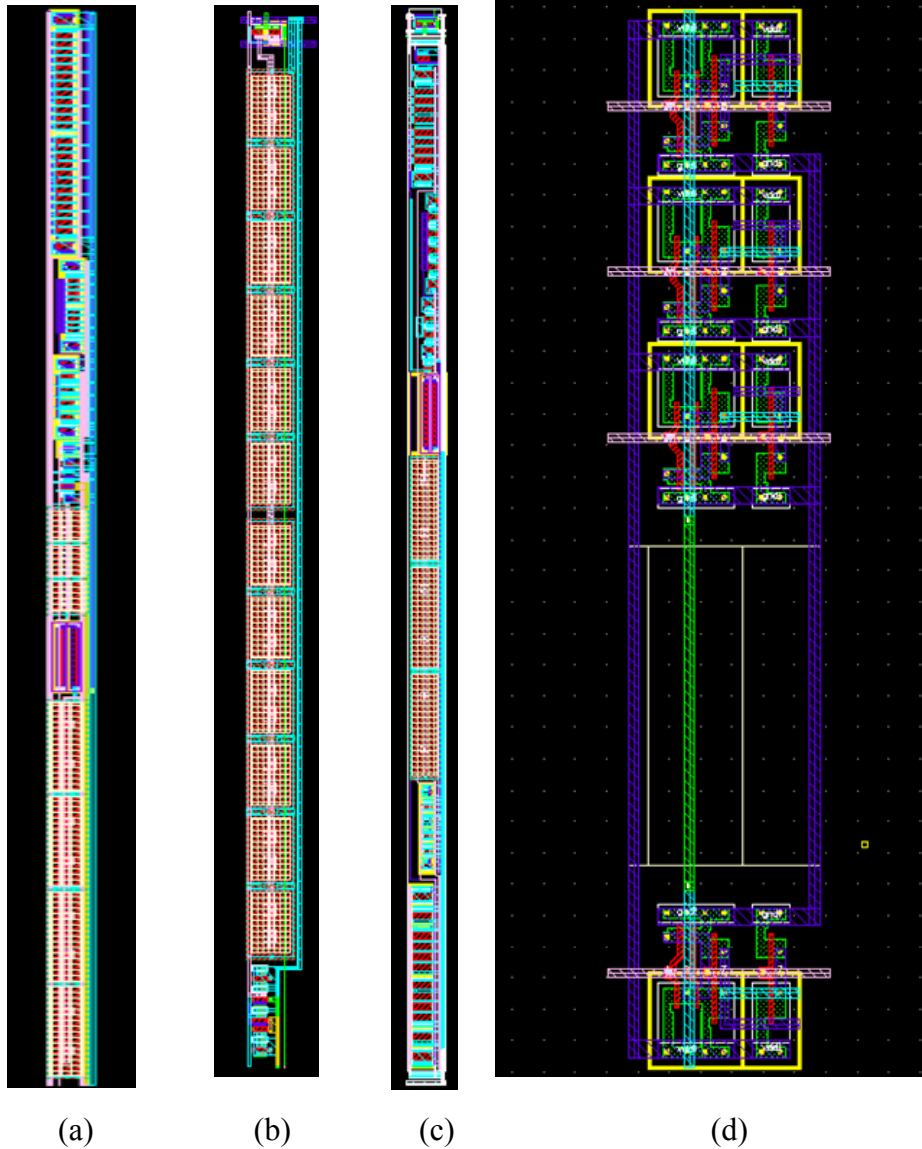


Figure 3. 19 (c)



(d)

Figure 3.19 Several layout sections of the Grey Code Line



(a)

(b)

(c)

(d)

Figure 3.20 the layout overviews of (a) the CTIA; (b) the CDS circuit; (c) the column buffer; (d) the digital control circuit

3.7 References

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Chapter 4 Implementation of Mode II: Coherent Detection

The working principle introduced in section 2.3.2 is implemented in this chapter. Here a transimpedance amplifier with a DC-servo loop is designed [1]. It's originally used for impedance measurements of nano-devices. After several modifications, it can be used with the optical chopper and the lock-in amplifier for coherent detection. It has the function to suppress the measurement error caused by the leakage current. Compared with traditional transimpedance amplifier, the adding of the DC-servo loop brings two benefits: (1) It increases the dynamic range by separating the DC path from the AC path; (2) It eliminates the requirement for a large and accurate feedback resistor. The combination of an integration stage and a differentiator stage maintains enough bandwidth and meanwhile a high gain. The total Bode diagram looks like a band-pass filter with its lower cut-off frequency extending to as low as milli hertz, and its higher cut-off frequency as high as 1MHz.

In section 4.1, the signal processing will be analyzed along the analog signal chain. In other words it will be analyzed how the signal is modulated by the optical chopper, then amplified by the transimpedance amplifier and finally demodulated by the lock-in amplifier. After this analysis, the basic structure of this novel transimpedance amplifier will be introduced in detail. The system-level analysis will be presented for the transimpedance amplifier and the target specifications will be deduced for each sub-system in section 4.2. The challenges encountered in the circuit implementation will be introduced and followed by the proposed solutions in section 4.3. Finally the schematics and the simulation results will be given out in section 4.4.

4.1 Introduction to the Coherent Detection Mode

4.1.1. Analog Signal Chain

The whole signal chain is analyzed theoretically. Figure 4. 1 shows how the light intensity, which carries the information about the absorption spectrum of the micro-fluidic channels, is transformed into the photocurrent and then into the voltage that can be read out with high SNR. The novel transimpedance amplifier is used instead of the traditional one. Table 4. 1 shows the signal and noise components at each node are explained. Table 4. 2 shows the relationship between them.

Loss of the Energy

There are two blocks causing the loss of energy in Figure 4. 1: the optical chopper and the lock-in amplification. Due to the optical chopper, some part of light is scattered and has no access to the photodiode. In the lock-in amplification, only the fundamental and the harmonic frequent components can be identified by the Phase Sensitive Detector. The DC component is attenuated and lead to the loss of energy.

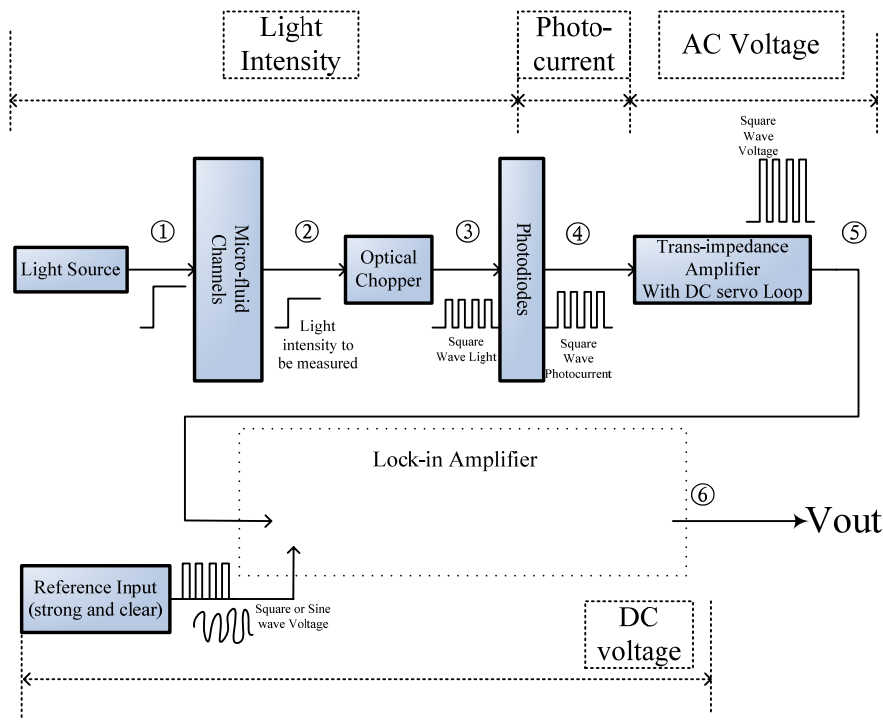


Figure 4. 1 Analog Signal Chain in the Coherent Detection Mode

Node	Symbol	Type	Physical Quantity	Frequency Component
②	$I_0(\lambda)$	Sig	Light Illuminance	Only DC
③	$I_1(\lambda)$	Sig	Light Illuminance (chopped)	$I_{1@dc}; I_{1@f_0}; I_{1@2f_0}; \dots$
④	I_{ph}	Sig	Photocurrent (square wave)	$I_{ph@dc}; I_{ph@f_0}; I_{ph@2f_0}; \dots$
	$I_{leakage}$	Noise	Leakage current	Only DC
⑤	V_{ph}	Sig	Voltage	$V_{ph@f_0}; V_{ph@2f_0}; V_{ph@3f_0}; \dots$
⑥	V_o	Sig	Voltage	Only DC

Table 4. 1 Signal components at each node

Node	Input	Expression
③	$I_0(\lambda)$	$I_1(\lambda) = I_0(\lambda) \cdot U(t)$ Where U (t) is the unit square wave function decided by the optical chopper.
④	$I_1(\lambda)$	$I_{ph} = \frac{I_1(\lambda)}{V_0(\lambda)K_m} R(\lambda)A$ Where $V_0(\lambda)$ is the photopic luminous efficiency function.
⑤	$I_{tot} = I_{ph} + I_{leakage}$	$V_{ph} = (I_{ph} + I_{leakage}) \cdot Z = (I_{ph} + I_{leakage}) \cdot Z = (I_{ph@f_0} + I_{ph@2f_0} + \dots)Z$ Where Z is the gain decided by the transimpedance amplifier and has the feature of band-pass.
⑥	V_{ph}	$V_o = V_{ph@f_0} \cdot K$ Where K is the constant decided by the demodulation of the lock-in amplifier.

Table 4. 2 Transfer functions of each block

Gain of the Coherent Detection

The square wave photocurrent at Node 4 can be written as [2]:

$$I_{ph}(t) = \frac{I_{ph0}}{2} + \frac{2I_{ph0}}{\pi} \left(\sin \omega_0 t + \frac{1}{3} \sin 3\omega_0 t + \frac{1}{5} \sin 5\omega_0 t + \dots \right) \quad \text{Equation 4- 1}$$

Where $\omega_0 = \frac{2\pi}{T}$ and $\frac{I_{ph0}}{2}$ is the dc component of the square wave photocurrent. The expressions in the time domain and in the frequency domain are plotted in Figure 4. 2.

The transimpedance block has a band-pass transfer function and is required to have a large bandwidth. The purpose is to reserve the signal energy as much as possible. If the transimpedance gain within the pass band is written as Z_0 , the square wave voltage at Node 5 can be written as:

$$V_{ph}(t) = Z_0 \cdot \frac{2I_{ph0}}{\pi} \left(\sin \omega_0 t + \frac{1}{3} \sin 3\omega_0 t + \frac{1}{5} \sin 5\omega_0 t + \dots \right) \quad \text{Equation 4- 2}$$

In the lock-in amplification block, both a sine-wave and a square-wave voltage can be used as reference. For the former case, it's written as:

$$\begin{aligned} V_o &= \int_{t=0}^{t=N \cdot T} V_{\sin}(t) V_{ph}(t) \cdot dt = \\ &= \int_{t=0}^{t=N \cdot T} Z_0 \cdot \frac{2I_{ph0}}{\pi} \left(\sin \omega_0 t + \frac{1}{3} \sin 3\omega_0 t + \frac{1}{5} \sin 5\omega_0 t + \dots \right) \cdot K_1 \sin \omega_0 t \cdot dt \quad \text{Equation 4- 3} \\ &= \frac{Z_0 K_1 N T}{\pi} I_{ph0} \end{aligned}$$

For the latter case, it's written as:

$$\begin{aligned} V_o &= \int_{t=0}^{t=N \cdot T} V_{\sin}(t) V_{ph}(t) \cdot dt = \\ &= \int_{t=0}^{t=N \cdot T} K_2 Z_0 \cdot \frac{2I_{ph0}}{\pi} \left(\sin \omega_0 t + \frac{1}{3} \sin 3\omega_0 t + \frac{1}{5} \sin 5\omega_0 t + \dots \right)^2 \cdot dt \quad \text{Equation 4- 4} \\ &= \int_{t=0}^{t=N \cdot T} K_2 Z_0 \cdot \frac{2I_{ph0}}{\pi} \left(\sin^2 \omega_0 t + \frac{1}{9} \sin^2 3\omega_0 t + \frac{1}{25} \sin^2 5\omega_0 t + \dots \right) \cdot dt \\ &= \frac{K_2 Z_0 N T}{\pi} \left(1 + \frac{1}{9} + \frac{1}{25} + \dots \right) \cdot I_{ph0} \end{aligned}$$

K_1 and K_2 are the amplification factor within the lock-in amplifier. From Equation 4- 3 and Equation 4- 4, it's also seen that the SNR and the gain of the coherent detection can be improved by increasing the integration time inside the lock-in amplification, i.e.

$T_{int} = NT$. It can be considered as a compensation for the energy loss in the optical chopping and the dc-component filtering.

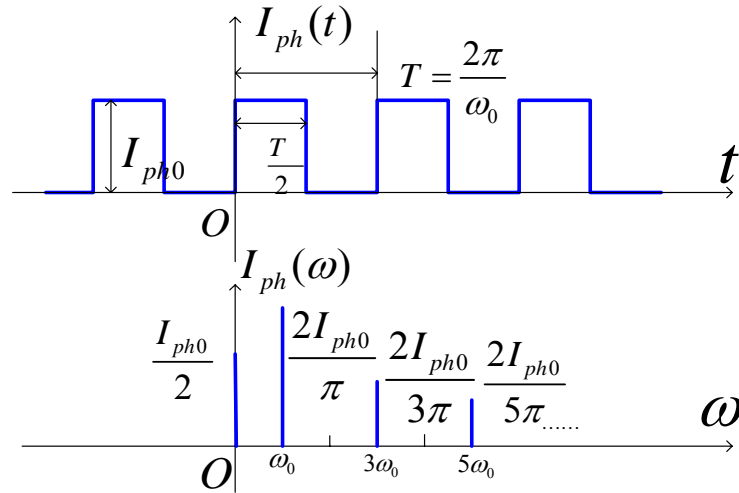


Figure 4. 2 Photocurrent generated by the chopped light in time and frequency domain

4.1.2 A Novel Transimpedance Amplifier

Figure 4. 3 shows the basic structure of the novel transimpedance amplifier [3]. It has two features:

- (1) It comprises a series connection of an integrator stage and a differentiator stage, which ensures a large bandwidth;
- (2) It has a DC-servo Loop as the continuously reset block, which biases the Amplifier without using a large resistor;

The two features are introduced in detail in the following paragraphs.

An Integrator-Differentiator Scheme

The first stage is the integrator stage and the second stage is the differentiator stage. The two stages work together to provide a flat overall frequency response.

(1) Bandwidth

The bandwidth in such case is extended to MHz. The linear decrease of the gain in the

integrator stage is compensated by the differentiator stage. The -3dB bandwidth is decided by three components: the photodiode junction capacitance (C_p), the integration capacitor (C_i) and the GBW of the Integrator Amplifier (GBP). The expression is shown below in Equation 4-5.

$$BW = GBP \cdot \frac{C_i}{C_i + C_p} \quad \text{Equation 4- 5}$$

(2) Gain

The gain in such case is determined by the ratio of two capacitors. Equation 4- 6 shows that a high and accurate gain can be achieved without requiring a large and stable resistor.

$$Z = \frac{C_d}{C_i} R_{fd} \quad \text{Equation 4- 6}$$

(3) Noise: without considering the Reset block

The noise contributed by the reset block would be discussed later, which varies according to the circuit implementations. It is the noise from the feedback resistor R_d that is mainly considered here. The input referred noise contributed by R_{fd} is as:

$$i_{n,R_{fd}}^2 = \frac{4kTR_{fd}}{Z^2} = 4kTR_{fd} \left(\frac{C_i}{C_d R_{fd}} \right)^2 = \frac{4kT}{R_{fd}} \left(\frac{C_i}{C_d} \right)^2 = \frac{4kT}{R_{eq}} \quad \text{Equation 4- 7}$$

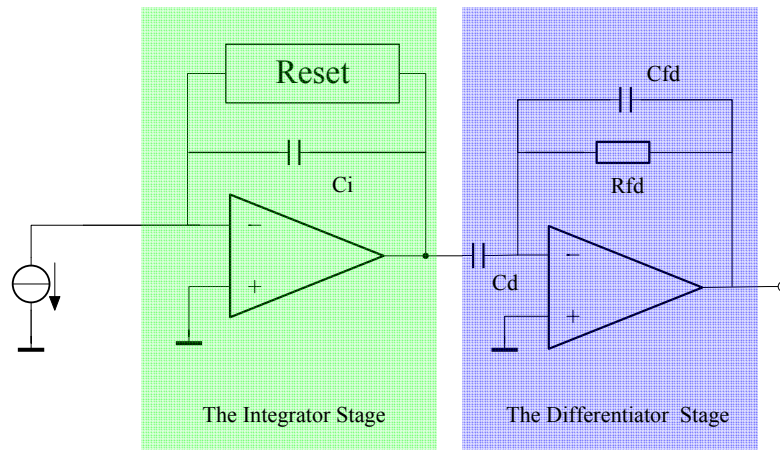


Figure 4. 3 the Integrator-Differentiator Scheme

Table 4. 3 shows the trade-off between the three parameters. Some practical values of resistors and capacitors are taken as an example for the quantitative analysis.

R _{fd} (Ω)	C _d (pF)	C _i (fF)	C _p (pF)	Input Referred Current Noise (by R _{fd})	GBP of the Integrator Amplifier (Hz)	Z (dB)	BW of the Transimpedance Amplifier (Hz)
100k	10	100	1	$4fA/\sqrt{Hz}$	100M	140	10M

Table 4. 3 an example showing the relationship between Bandwidth, Gain and Noise

Biasing the amplifier: a DC-servo Loop

The reset block functions to bias the amplifier. In other words, the reset block functions to prevent the integrator stage from being saturated by the leakage current and the dc component of the photocurrent. There are several ways to implement this reset block [4, 5]: (1) a large resistor R_{fi}; (2) a switched capacitor; (3) a simple reset switch which is turned on when the output voltage of the integrator stage reaches a defined threshold; (4) a DC-servo Loop.

(1) In the case of using a large resistor R_{fi}, on one hand the dynamic range is limited; on the other hand a precise control over the value of R_{fi} is required since R_{fi} determines the frequency response of the integrator stage.

(2) In the case of using a switched capacitor, the charge injection becomes a critical problem. A switching frequency of 10MHz and a charge injection as low as 1fC give a spurious current of 10nA while the photocurrent to be measured only ranges from 1pA~10nA.

(3) In the case of using a reset switch, the maximum time interval available for one measurement is limited by the leakage current.

Since the three options are not suitable in such case, a DC-servo Loop is implemented as the reset block. The structure is shown in Figure 4. 4. The block $H(s)$ is a low-pass filter, which senses the dc component at the integrator output and negatively feedback a current to the input node through R_f . Consequently the AC signal and the DC signal are flowing through two different paths, to Node A and Node B respectively. The output DC point at Node A is fixed by realizing a high $H(0)$. Ideally the frequency response of such an integrator stage is shown in Figure 4. 5.

This DC-servo loop is a continuously active system, which reset the DC continuously while leaving the AC untouched. It is a perfect reset block in terms of the frequency response. But the price to pay is power consumption, chip area and design complexity. The noise contributed by this active feedback needs to be analyzed for optimization.

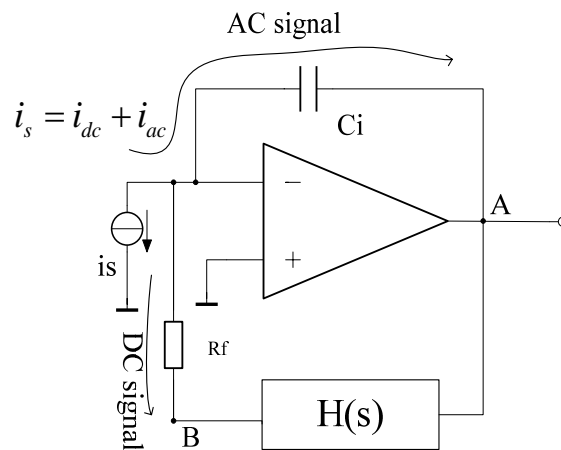


Figure 4. 4 the Integrator Stage with a DC-servo Loop

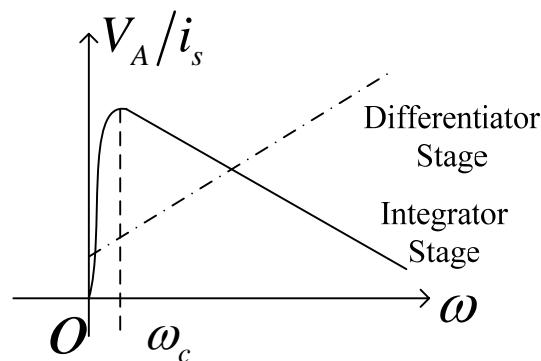


Figure 4. 5 Frequency Response of the Integrator Stage

Figure 4. 4 can be translated into an equivalent structure as is shown in Figure 4. 6. The equivalent structure comprises (1) the Transimpedance Feedforward path and (2) the Transconductance Feedback path. The expressions for the two paths can be written as below.

$$V_A = \frac{1}{sC_i} \cdot i_{ac} \quad \text{Equation 4- 8}$$

$$V_B = R_f \cdot i_{dc} \quad \text{Equation 4- 9}$$

$$Z_{\text{int, feedforward}} = \frac{A_{\text{int}}}{\frac{1}{R_f} + s(1 + A_{\text{int}})C_i} \quad \text{Equation 4- 10}$$

$$G_{\text{int, feedback}} = \frac{H(s)}{R_f} \quad \text{Equation 4- 11}$$

The loop gain of this DC-servo loop can be thus written as:

$$G_{\text{loop}} = \frac{A_{\text{int}}}{\frac{1}{R_f} + s(1 + A_{\text{int}})C_i} \cdot \frac{H(s)}{R_f} = \frac{A_{\text{int}}H(s)}{1 + s(1 + A_{\text{int}})C_iR_f} \quad \text{Equation 4- 12}$$

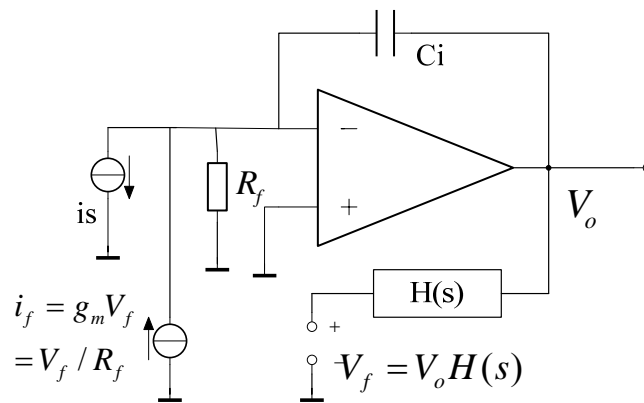


Figure 4. 6 the Integrator Stage with the Feedforward path and the Feedback path

4.1.3 Optical Chopping and the DC-servo Loop

In Figure 4. 5 the lower cut-off frequency of the band-pass feature is marked as ω_c . It

defines the frequency boundary between DC and AC. Any signal with the frequency lower than ω_c is defined as DC and flows to Node B, where it is recognized as a monitoring reference. Otherwise the signal is defined as AC and flows to Node A, where it is read out or amplified.

The chopping frequency ω_0 put a requirement on ω_c and $\omega_c=2\pi f_c$. To minimize the energy loss, the chopped photocurrent must have its fundamental frequent component lying within the pass band. It means that $\omega_c < \omega_0$. It's worth a notice that the optical chopping frequency is much lower than the electrical chopping frequency. The optical chopping frequency usually ranges from 0.01Hz to tens of kHz [6], which challenges the design of the DC-servo Loop in two aspects: (1) the flicker noise at ω_0 is still high since ω_0 is not high enough; (2) A pole must be placed at a really low frequency so that $\omega_c < \omega_0$ can be achieved.

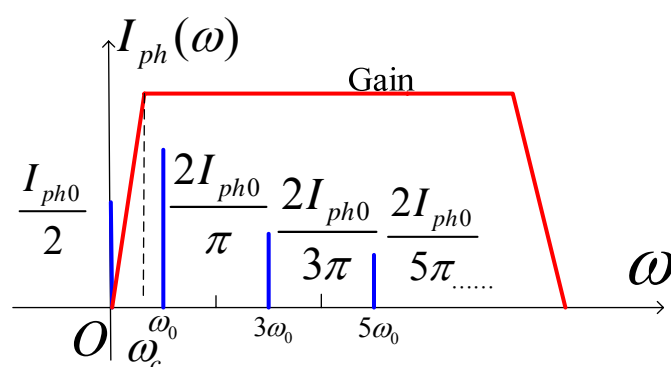


Figure 4. 7 the Chopping frequency and the DC-servo Loop

4.2 System-level Analysis of the Novel Transimpedance Amplifier

The last section introduces the working principle of the novel transimpedance amplifier. It is seen that the main challenge lies in the design of the integrator stage, which suffers from the active feedback in three aspects: (1) stability; (2) dynamic

range; (3) extra noise.

The systematic analysis is done and the target specifications for each block are derived, in order to obtain a good implementation of H(s) and Rf.

Target Specifications of the Transimpedance Amplifier

The target specifications are summarized in Table 4. 4, after considering the optical chopper and the lock-in amplifier that will be utilized in the measurement.

Specifications	Value
Gain	140dB
Bandwidth	990Hz~1MHz (f ₀ =1kHz)
Dynamic Range	80dB
Input Referred Current Noise	100 fA/√Hz
DC output variation	0.1% of Output Swing
Input Current range	1pA~10nA
Capacitive Load	30pF
Resistive Load	100kΩ

Table 4. 4 Target Specifications of the transimpedance amplifier

4.2.1 Design of H(s)

Bandwidth

As is shown in section 4.2.3, the parameter ω_c is defined as the lower cut-off frequency of transimpedance amplifier. Actually ω_c is also the unity gain frequency of the DC-servo loop gain in the integrator stage.

$$\left|G_{loop}(f_c)\right| = \left|G_{loop}\left(\frac{\omega_c}{2\pi}\right)\right| \approx \frac{|H(f_c)|}{2\pi f_c C_i R_f} = 1 \quad \text{Equation 4- 13}$$

It can thus be obtained that:

$$f_c = \frac{|H(f_c)|}{2\pi C_i R_f} \quad \text{Equation 4- 14}$$

According to the target specifications, the f_c must be designed as $f_c < f_0$, hence:

$$|H(f_c)| < 2\pi C_i R_f \cdot f_0 \quad \text{Equation 4- 15}$$

Dynamic Range

The DC gain $H(0)$ is related to the dynamic range. It determines the DC variation at the AC output node in the integrator stage. Based on Table 4. 4, it is obtained that

$$\frac{V_{\Delta}}{V_{A,\max}} = \frac{V_{B,\max}}{H(0)V_{A,\max}} < 0.1\% \Rightarrow H(0) > 60dB \quad \text{Equation 4- 16}$$

Stability

From Equation 4- 14, it's noticed that f_c is determined by $H(s)$. According to Equation 4- 12, there are two poles within the Unity Gain Bandwidth of the DC-servo loop gain, with f_{p1} contributed by C_i and f_{p2} by $H(s)$. Hence $H(s)$ introduces a zero at f_z for frequency compensation. The relationship in Equation 4- 19 must be achieved to assure a phase shift of less than 60 degrees.

$$f_{p1} = \frac{1}{2\pi(1 + A_{\text{int}})C_i R_f} \quad \text{Equation 4- 17}$$

$$H(s) = \frac{H_0}{(1 - \frac{s}{\omega_z})(1 - \frac{s}{\omega_{p2}})} \quad \text{Equation 4- 18}$$

$$f_z \leq 2f_{p1} \quad \text{Equation 4- 19}$$

The Schematic and the Transfer Function

Based on the discussion above, the desired frequent response of the $H(s)$ is concluded as is shown in Figure 4. 8. A schematic is proposed to realize the desired frequency response as is shown in Figure 4. 9. The transfer function is derived as below:

$$H(s) = \frac{A_h(1 + sC_2R_a)}{1 + sR_a[C_2 + C_1(1 + A_h)]} \quad \text{Equation 4- 20}$$

Where A_h is the DC gain of the H Amplifier. The pole and the zero of $H(s)$ are at the frequencies:

$$f_{p2} = \frac{1}{2\pi R_a [C_2 + C_1(1 + A_h)]} \quad \text{Equation 4- 21}$$

$$f_z = \frac{1}{2\pi R_a C_2} \quad \text{Equation 4- 22}$$

Since $f_c > f_z > f_{p2}$, it can be obtained that:

$$|H(0)| = A_h \quad \text{Equation 4- 23}$$

$$\begin{aligned} |H(f_c)| &\approx \frac{j2\pi f_c A_h C_2 R_a}{j2\pi f_c R_a [C_2 + C_1(1 + A_h)]} \\ &\approx \frac{j2\pi f_c A_h C_2 R_a}{j2\pi f_c R_a C_1(1 + A_h)} \approx \frac{C_2}{C_1} \end{aligned} \quad \text{Equation 4- 24}$$

The capacitors and the resistors must be chosen properly so that Equation 4- 15 to Equation 4- 24 are satisfied.

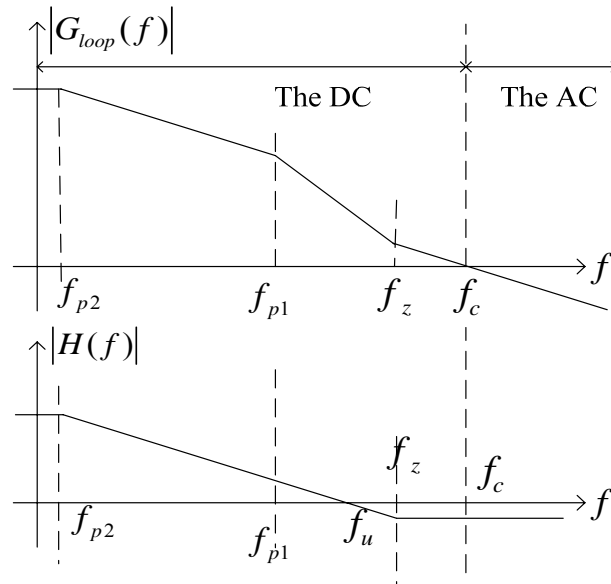


Figure 4. 8 the Loop Gain of the integration stage

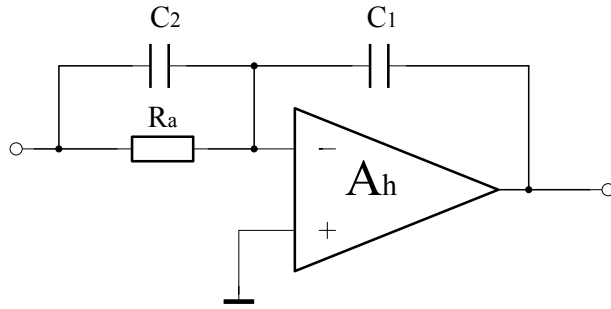


Figure 4. 9 the Schematic of the block $H(s)$

4.2.2. Design of the Integrator Stage

The full schematic of the Integrator stage is shown in Figure 4. 10. The design in this section is based on this figure.

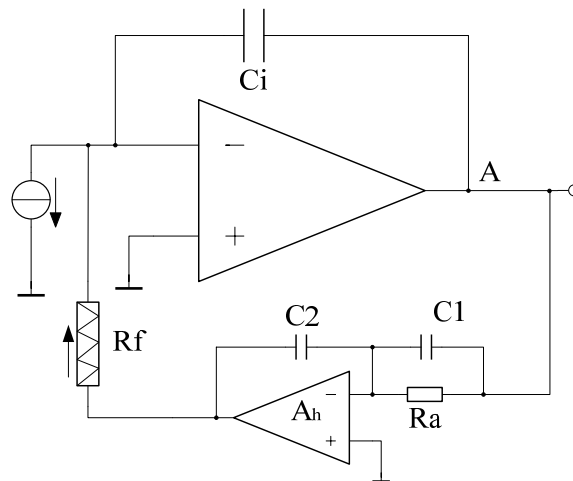


Figure 4. 10 the full schematic of the integrator stage

Transimpedance gain

In order to achieve a transimpedance gain as high as 140dB, the practical values of the capacitors and the resistors have been chosen as below in Table 4.5. These choices are also based on noise considerations as will be discussed later.

C_i	C_d	R_{fd}
200fF	20pF	100k Ω

Table 4. 5 Values of the capacitors and the resistors

Bandwidth

As analyzed before, the bandwidth is related to the parasitic capacitance at the input node C_p . It is noticed that the transimpedance amplifier are shared by an array of photodiodes through a multiplexer. For each photodiode, its parasitic capacitance is $C_{p0}=650\text{fF}$. Taking into account the capacitance of the multiplexer and the interconnector capacitance, C_p is estimated as around 800fF . In order to achieve a bandwidth of 1MHz for this transimpedance amplifier, the GBW for the Integrator Amplifier should reach at least:

$$GBW = BW \frac{C_i + C_p}{C_i} \approx 5\text{MHz} \quad \text{Equation 4- 25}$$

Dynamic Range

There are two output nodes for the integrator stage, Node A and Node B. Both of them are limiting the maximum detectable input current. Depending on the signal frequency, one of them is dominant. In the equations below, V_{\max} means the maximum output voltage allowed.

(1) For the frequency $f < f_u$, since $|G_{loop}(f)| > 1$, the input current flows to Node B; since $|H(f)| > 1$, the output swing at Node B is the most limiting factor. Hence the relationship below should be satisfied:

$$V_B = I_{in} R_f < V_{\max} \Rightarrow I_{in} < V_{\max} / R_f \quad \text{Equation 4- 26}$$

(2) For the frequency $f_u < f < f_c$, since $|G_{loop}(f)| > 1$, the input current flows to Node B; but since $|H(f)| < 1$, the output swing at Node A is the most limiting factor.

Hence the relationship below should be satisfied:

$$|V_A| = \frac{V_B}{|H(f)|} = \frac{I_{in} R_f}{|H(f)|} < V_{\max} \Rightarrow I_{in} < \frac{V_{\max} |H(f)|}{R_f} \quad \text{Equation 4- 27}$$

(3) For the frequency $f_c < f < \frac{1}{2\pi C_d R_d}$, since $|G_{loop}(f)| < 1$, the input current flows to Node A; since $|H(f)| < 1$, the output swing at Node A is the most limiting factor. Hence the relationship below should be satisfied:

$$|V_A| = \frac{I_{in}}{2\pi f C_i} < V_{max} \Rightarrow I_{in} < 2\pi f C_i V_{max} \quad \text{Equation 4- 28}$$

(4) For the frequency $f > \frac{1}{2\pi C_d R_d}$, since the differentiator gain is larger than 1, the output node of the differentiator stage V_{out} becomes the limiting factor. Hence the relationship below should be satisfied:

$$V_{out} = \frac{C_d R_d}{C_i} I_{in} < V_{max} \Rightarrow I_{in} < V_{max} \frac{C_i}{C_d R_d} \quad \text{Equation 4- 29}$$

Based on the discussion above, the relationship between the maximum acceptable input current and the frequency is plotted as is shown in Figure 4. 11 [4].

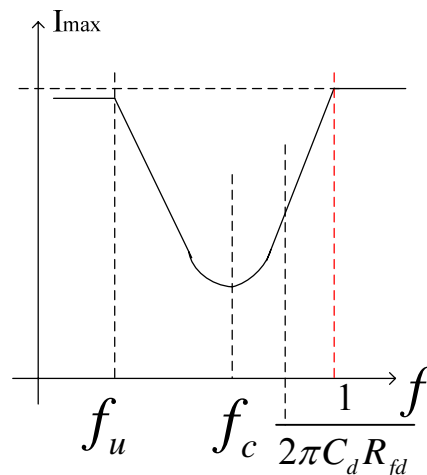


Figure 4. 11 the maximum detectable input current versus the signal frequency

Feedback Resistor

R_f influences the photodetection in the frequencies lower than f_u . The maximum

detectable chopped photocurrent is calculated based on Equation 4- 26 as below:

$$\frac{I_{ph0,max}}{2} + I_{leakage} = \frac{V_{max}}{R_f} \Rightarrow I_{ph0,max} = 2\left(\frac{V_{max}}{R_f} - I_{leakage}\right) \quad \text{Equation 4- 30}$$

Hence the larger the Rf is, the smaller the acceptable $I_{ph0,max}$ becomes, which degrades the dynamic range.

On the other hand, the feedback resistor Rf determines the input referred noise. The larger the Rf is, the smaller the input referred current noise is. In Equation 4- 31 is the thermal noise contributed by Rf:

$$i_{n,R_f}^2 = 4kT/R_f \quad \text{Equation 4- 31}$$

After considering the dynamic range and the noise, Rf is chosen as below:

$I_{ph0,max}$	V_{max}	R_f	$I_{leakage}$
62nA	1.6V	49.5M Ω	1nA

Table 4. 6 Choice of the Rf and the maximum detectable chopped photocurrent

The feedback resistor is designed to be 49.5M Ω , which is too high to be implemented with good accuracy and good linearity in standard CMOS technology. Fortunately the feedback resistor only functions for biasing. Hence the requirements on its accuracy and its linearity are low.

The H(s) Block

Based on the chosen capacitors and resistors, the H(s) is designed as below. After considering Equation 4- 15 and Equation 4- 16, Equation 4- 24 and Equation 4- 25, the capacitors and the specifications are set as is shown in Table 4. 7.

C1	C2	Ah	f_c
200fF	20pF	120dB	$f_0/8 = 125\text{Hz}$

Table 4. 7 Choice of the capacitors in the block H(s)

4.3 Challenges and Solutions in the Circuit Implementation

The Integrator-Differentiator scheme is shown in Figure 4. 12. The discussion in this section is based on this figure.

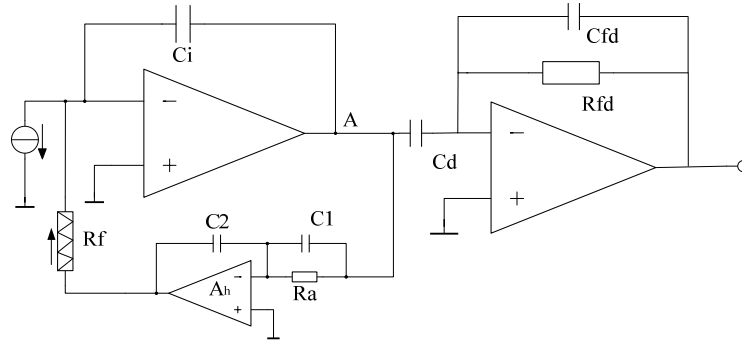


Figure 4. 12 the full schematic of the Integrator-Differentiator

4.3.1 Challenges in the implementation

According to Table 4. 5, Table 4. 6 and Table 4. 7, setting $A_{int}=120dB$, several parameters can be calculated as below, which show the challenges in the design:

$$|H(f_c)| = \frac{C_2}{C_1} = 2\pi C_i R_f \frac{f_0}{8} \approx -40dB \quad \text{Equation 4- 32}$$

$$f_{p1} = \frac{1}{2\pi(1 + A_{int})C_i R_f} = 0.016Hz \quad \text{Equation 4- 33}$$

Hence f_z should be designed as below:

$$f_z = 2f_{p1} = 0.032Hz \quad \text{Equation 4- 34}$$

Since $|H(f_z)| = |H(f_c)| = -40dB$ and $|H(f_{p2})| = |H(0)| = 120dB$,

according to Figure 4. 8, f_{p2} should be designed as below:

$$f_{p2} < \frac{f_z}{10^8} = 0.32nHz \quad \text{Equation 4- 35}$$

Based on these calculations, it can be concluded that there are three challenges in the design:

(1) it's seen from Equation 4- 34 and Equation 4- 35 that both the pole and the zero contributed by $H(s)$ are located at really low frequencies. This is the requirement from the low chopping frequency that is limited by the mechanical properties. In order to realize this pole-zero pair at milli and nano frequencies, the resistor R_a has to be as large as $T\Omega$ according to Equation 4- 21 and Equation 4- 22. This is very difficult for an IC implementation.

(2) It's seen from Equation 4- 17 that f_{p1} is directly determined by A_{int} . Since the DC gain of an amplifier is too high to be designed accurately, f_{p1} can not be designed with high accuracy. That makes the frequency compensation so difficult that the stability becomes the major concern for this DC-servo loop.

(3) The feedback resistor is designed as $49.5M\Omega$, which is too high to be implemented as passive components in standard CMOS technology. Hence, pseudo-resistors consisted of active circuits are used as an alternative. But the active circuits usually introduce extra noise and have to be designed properly.

Solutions are found in the next section to solve these problems.

4.3.2 Solutions in the implementation

(1) Approach towards the low-frequent pole f_{p2} in $H(s)$

Two transistors are used in series to generate an equivalent resistance as large as $100G\Omega$ [7]. The schematic and the equivalent models for both cases are shown in Figure 4. 13.

(1) For positive V_{GS} , i.e. $V_m < V_n$, when I_{dc} is small, each transistor acts as a reversely biased diode; when I_{dc} is large, each transistor acts as a diode-connected PMOS

transistors with an equivalent resistance of $1/g_m$.

(2) For negative V_{GS} , i.e. $V_m > V_n$, each device acts as a diode-connected BJT instead of MOSFET. The transistors are cut-off and the parasitic source-well-drain p-n-p bipolar junctions are activated.

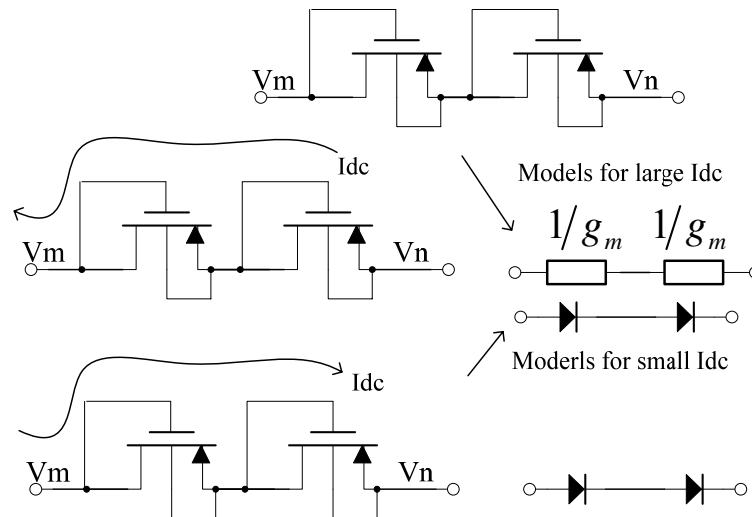


Figure 4. 13 A pseudo-resistor device consisted of MOS transistors

This device needs no extra biasing circuitry. But there are two drawbacks: (1) the equivalent resistance is voltage/current dependent. This device functions as a large resistance within only a small voltage range. The simulated I-V relationship is shown in Figure 4. 14. For larger voltage or larger current, the p-n-p junction could break down or g_m could decrease greatly, reducing the incremental resistance. Two MOS-bipolar devices are thus connected in series to enlarge the maximum acceptable voltage difference. (2) The equivalent resistance is process-dependent. Thus it is not designable. The order of magnitude of the equivalent resistance can be simulated and estimated.

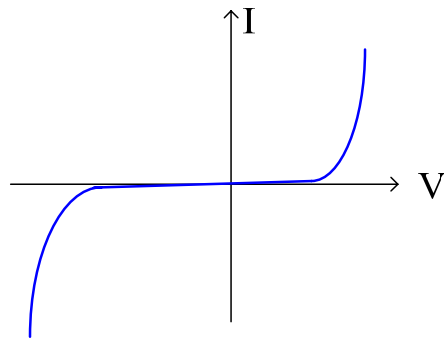


Figure 4. 14 Simulated I-V relationship of a MOS-bipolar pseudo-resistor

This device is utilized as R_a in the block $H(s)$, to produce the nano-Hz pole, as is shown in Figure 4. 15.

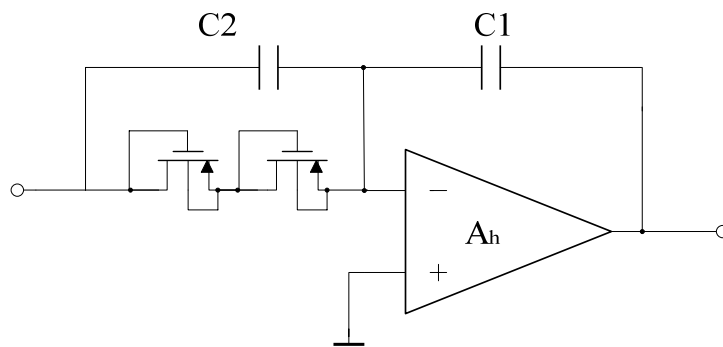


Figure 4. 15 the schematic of $H(s)$ with a MOS-bipolar Pseudo-resistor

The reasons are listed as below:

- (1) The accuracy of R_a is not required to be high. A solution is found to circumvent the inaccuracy caused on f_z .
- (2) The voltage across R_a is not high, since the current through the Feedforward path is small.

The geometric sizes of the transistors are chosen as below:

W	L	MOSFET
4um	4um	PMOS

Table 4. 8 the MOS geometric sizes for implementing R_a

(2) Approach towards frequency compensation

The milli-Hz zero f_z is introduced in $H(s)$ to compensate the pole f_{p1} contributed by the integration capacitor. However neither f_{p1} nor f_z can be designed accurately. f_{p1} is not accurate since the DC gain of the integrator amplifier can not be controlled accurately. f_z is not accurate since R_a as a pseudo-resistor is not implemented with high accuracy.

It leads to the question: how can we match the pole and the zero accurately and reliably?

This problem is solved by three operations: (1) introducing a pseudo-resistor R_i in parallel with C_i ; (2) matching the resistors R_i and R_a ; (3) matching the capacitors C_i and C_2 . The modified schematic is shown in Figure 4. 16. The new loop gain is derived accordingly as $G_{i\text{loop}}$.

$$G_{i\text{loop}}(s) = \frac{A_{\text{int}}H(s)}{1 + (1 + A_{\text{int}})(sC_i + \frac{1}{R_i})R_f} \quad \text{Equation 4- 36}$$

It's obtained then:

$$f_{p1} = \frac{1}{2\pi R_i C_i} \quad \text{Equation 4- 37}$$

Since the voltage differences across R_i and R_a are the same due to the virtual ground, R_i and R_a can be matched by matching $M1$ and $M3$, $M2$ and $M4$ respectively. It is by matching R_i and R_a , C_i and C_2 respectively that f_{p1} and f_z can be matched.

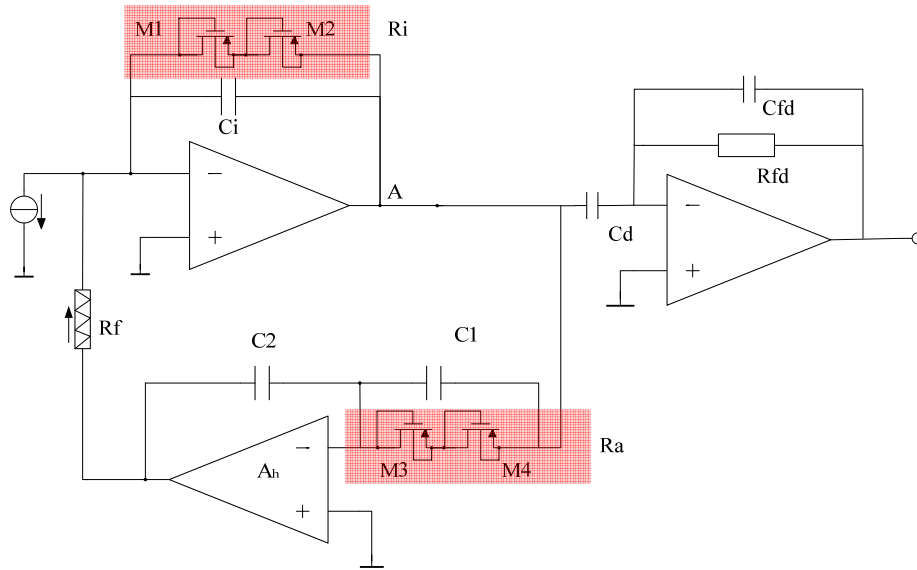


Figure 4. 16 Modified Schematic for the Integrator-Differentiator Scheme

(3) Approach towards the high feedback resistor R_f

As is shown in Figure 4. 16, the feedback resistor has three features: (1) R_f should be designed as around $49.5M\Omega$; (2) R_f should be designed as a current-inverter since $H(s)$ utilizes an inverter amplifier; (3) The current flowing through R_f is at low frequencies. Based on the discussion above, a schematic is proposed as is shown in Figure 4. 17.

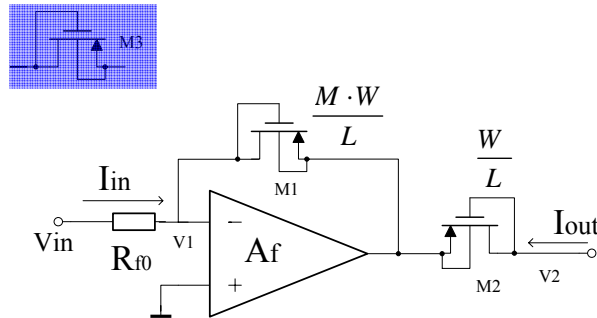


Figure 4. 17 Schematic for the feedback resistor block

The schematic in Figure 4. 17 implements a large pseudo-resistor through the current division with an active control [8]. The current division is based on the fact that the current flowing through a transistor is proportional to the transistor width W , as is shown in Table 4. 9. A diode-connected MOSFET like M_3 may work in three conditions: saturation, weak inversion and cut off. The I-V relations of these

conditions are demonstrated in Table 4. 9, where E and T are the width and the depth of the P-plus region respectively.



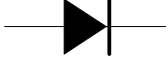
Condition	I-V relationship	AC Model
Saturation	$I_d = \frac{K}{2} \frac{W}{L} (V_{gs} - V_{th})^2 \Rightarrow I_d \propto W$	$1/g_{ms} \propto W$ 
Weak inversion	$I_d = I_{d0} \frac{W}{L} e^{-V_{gs}/\alpha V_T} (1 - e^{-V_{gs}/V_T}) \Rightarrow I_d \propto W$	$1/g_{mw} \propto W$ 
Cut-off	$I_d = J_{s0} [2TE + W(2T + E)] (e^{V_{gs}/V_T} - 1)$ $\approx 2J_{s0} WT (e^{V_{gs}/V_T} - 1) \Rightarrow I_d \propto W$	

Table 4. 9 the equivalent models of the diode-connected MOSFET [8]

Suppose M1 and M2 have the same length and they are biased with the same $V_{gt} = V_{gs} - V_{th}$. Then for small dc current, M1 and M2 can be implemented as two resistors that have an accurate ratio between them, i.e.

$$\frac{R_1}{R_2} = \frac{g_{m2}}{g_{m1}} = \frac{W_2}{W_1} = \frac{1}{M} \quad \text{Equation 4- 38}$$

Then the current division is realized as:

$$\frac{I_{out}}{I_{in}} = \frac{V_{gs2}/R_2}{V_{gs1}/R_1} = \frac{R_1}{R_2} = \frac{1}{M} \quad \text{Equation 4- 39}$$

The active control has two functions here: (1) it keeps M1 and M2 under the same biasing condition; (2) it provides enough current for M1 and M2 so that this pseudo-resistor can work as a current inverter.

The equivalent resistance in Figure 4. 17 is derived below:

$$I_{out} = \frac{I_{in}}{M} = \frac{V_{in}}{R_{f0}M} \Rightarrow R_{eq} = \frac{V_{in}}{I_{out}} = MR_{f0} \quad \text{Equation 4- 40}$$

The final schematic of this transimpedance amplifier is shown in Figure 4. 18. The geometric sizes of the involved transistors are chosen as below:

W	L	M	R _{f0}	R _f = R _{eq}	MOSFET
1um	14.5um	150	330kΩ	49.5MΩ	PMOS

Table 4. 10 the MOS geometric sizes and the poly resistor for implementing R_f

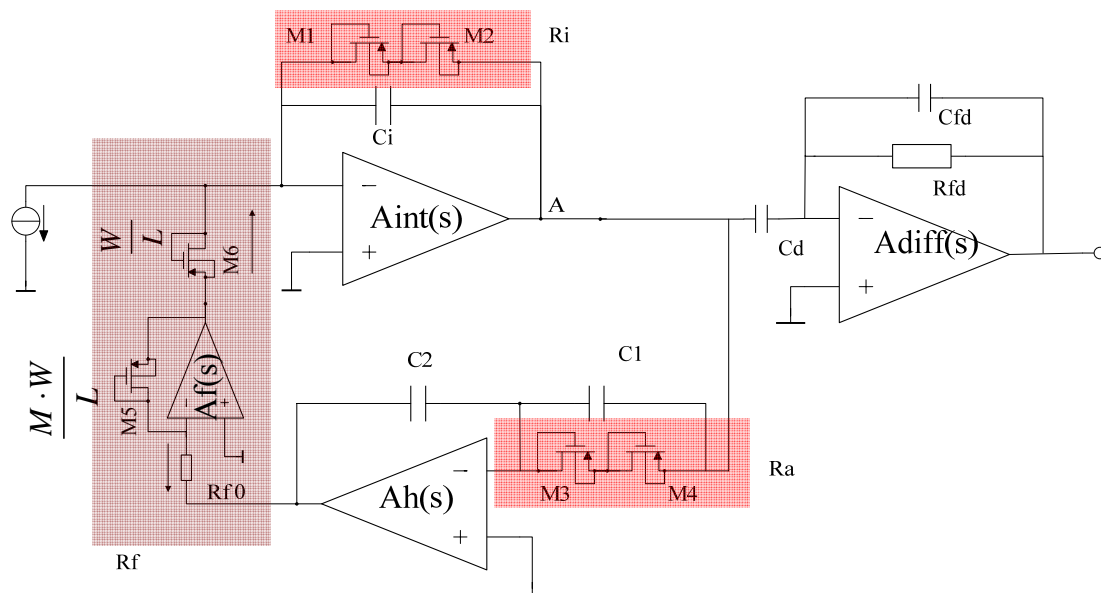


Figure 4. 18 the full schematic of the Transimpedance amplifier

4.3.3. Conclusion of the Designed Capacitors and Resistors

Up to now all, the theoretic analysis of the novel transimpedance amplifier has been introduced. The final schematic is as shown in Figure 4. 18. The designed capacitors and the resistors are summarized as below:

Ci	Cfd	Cd	C1	C2
200fF	15pF	20pF	200fF	20pF

(a) The capacitors

Rf d	Rf 0
100k Ω	330k Ω

(b) The resistors

	M1	M2	M3	M4	M5	M6
L	4 μ m	4 μ m	4 μ m	4 μ m	14.5 μ m	14.5 μ m
W	4 μ m	4 μ m	4 μ m	4 μ m	150 μ m	1 μ m

(c) The transistors

Table 4. 11 Summary of the designed capacitors and resistors

4.4 Circuit Implementation: Amplifier Design

In this section, the utilized amplifiers are designed. The circuit architectures and the achieved specifications are given out. There are totally four amplifiers used in this novel transimpedance amplifier, i.e. $A_{int}(s)$, $A_h(s)$, $A_f(s)$ and $A_{diff}(s)$.

$A_{int}(s)$ is designed specially to obtain a low noise and high detection sensitivity. And the design of $A_h(s)$ is reused as $A_f(s)$ and $A_{diff}(s)$ to shorten the design cycle.

4.4.1 The Integrator amplifier: $A_{int}(s)$

The schematic of the integrator amplifier is shown in Figure 4. 19 The schematic of the Integrator amplifier. This amplifier plays an important role in four aspects:

- (1) it sets the noise level of the system and thus determines the detection limit;
- (2) it sets the higher cut-off frequency of the full transimpedance and thus determines the system bandwidth;

- (3) its output swing sets the system dynamic range for the main frequency band; (
- 4) it decides the input DC voltage which influences the implementation of the feedback resistor R_f .

The specification requirements are summarized in Table 4. 12, with the achieved parameters listed as a counterpart. The schematic, as is shown in Figure 4. 19, is consisted of three stages: (1) the first stage is designed for the noise optimization; (2) the second stage is designed to provide enough gain; (3) the third stage is designed to provide a rail-to-rail output swing.

Specification	Required Value	Achieved Value
Input DC Voltage	1.6V	1.6V
GBW	>5MHz	8MHz
Specification	Required Value	Achieved Value
Output Swing	1.6V	3.2V
DC Gain	120dB	132dB
Input Referred Noise	$990nV/\sqrt{Hz}$	$3uV/\sqrt{Hz} @1Hz$ $90nV/\sqrt{Hz} @10kHz$
Capacitive Load	21pF	30pF
Slew Rate	—	3V/usec
Phase Margin	60 degree	63 degree
Power Consumption	—	520uA

Table 4. 12 Specifications of the Integrator amplifier

The First Stage: the noise consideration

The input stage is designed to be resistively loaded. The active load with a current mirror would have fully added its noise, whose white component would be higher than the one of a simple resistor and whose 1/f component would be very high considering that NMOS transistors should be used. The input referred noise

contributed by the load resistor R_L is expressed as below, which could be reduced by increasing the g_{m1} .

$$v_{R_L,n}^2 = \frac{4kT}{R_L g_{m1}^2} \quad \text{Equation 4- 41}$$

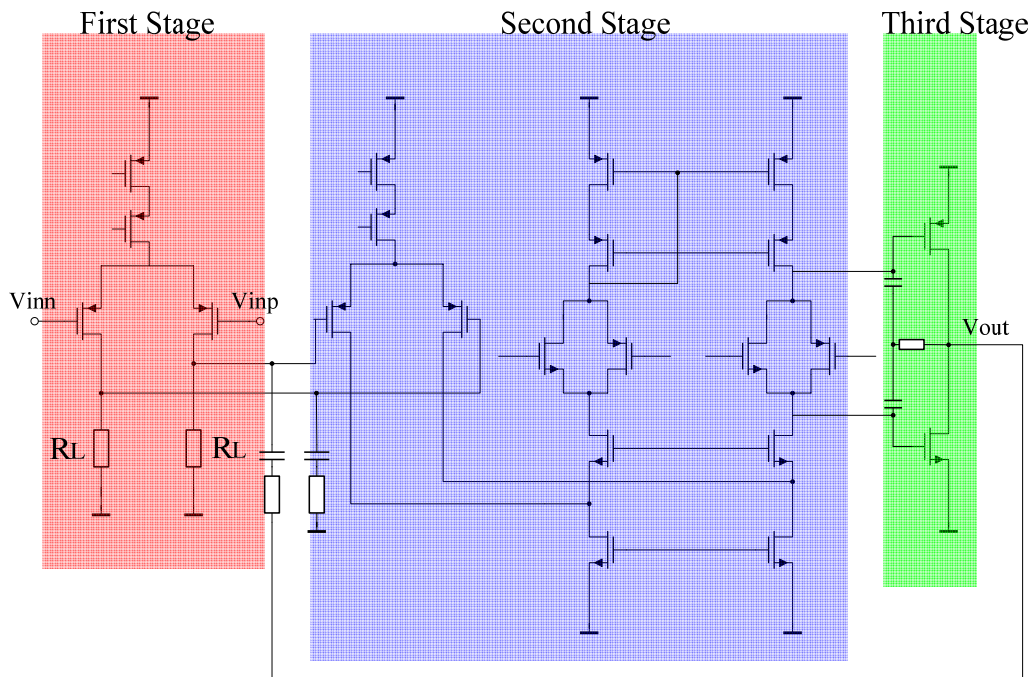


Figure 4. 19 The schematic of the Integrator amplifier

The input pair is chosen as PMOS transistors to minimize the flicker noise. The thermal noise generated by the input pair is:

$$\begin{aligned} v_{th,n}^2 &= 2 \cdot \frac{8kT}{3g_m} = 2 \cdot \frac{8kT}{3} \cdot \frac{L}{\mu_p C_{ox} W (V_{gs} - V_{th})} \\ &= 2 \cdot \frac{8kT}{3} \cdot \frac{L^2}{\mu_p C_{gate} (V_{gs} - V_{th})} \end{aligned} \quad \text{Equation 4- 42}$$

In the integrator stage, this noise generates an equivalent current noise at the input as:

$$\begin{aligned}
i_n^2 &= v_{th,n}^2 \left[2\pi f (C_i + C_p + C_{gate}) \right]^2 && \text{Equation 4- 43} \\
&= 2 \cdot \frac{8kT}{3} \cdot \frac{L^2 (2\pi f)^2}{\mu_p (V_{gs} - V_{th})} \left[\frac{(C_i + C_p)^2}{C_{gate}} + C_{gate} + 2(C_i + C_p) \right] \\
&\geq 2 \cdot \frac{8kT}{3} \cdot \frac{L^2 (2\pi f)^2}{\mu_p (V_{gs} - V_{th})} \cdot 4(C_i + C_p)
\end{aligned}$$

It can be concluded that when $C_i + C_p = C_{gate} = C_{ox}WL$, the thermal noise of the input transistors is optimal. Here C_i equals to 200fF and C_p is estimated as 800fF, leading to the choice of $W=250\mu\text{m}$ and $L=1\mu\text{m}$.

The Second Stage: the GBW consideration

The second stage is chosen as the folded-cascode structure for a high DC gain. Though it consumes more power, it allows a more flexible input and output voltage range, so that the class-AB control circuit for the next stage can be embedded here.

The Third Stage: the output swing consideration

In this stage, the driving capability is not the major concern. The key is to enlarge the output voltage swing so as to improve the system dynamic range. Thus the CMOS inverter schematic is used to accomplish the rail-to-rail output voltage range.

The frequency compensation: Nested Miller Compensation

There are three stages in this amplifier design in total to satisfy the requirements on the low noise, the large output swing and the high GBW. In order to ensure an enough phase margin for the three-stage design, nested miller compensation is used as shown in Figure 4. 20. The nullor resistors are added for strong loop stability.

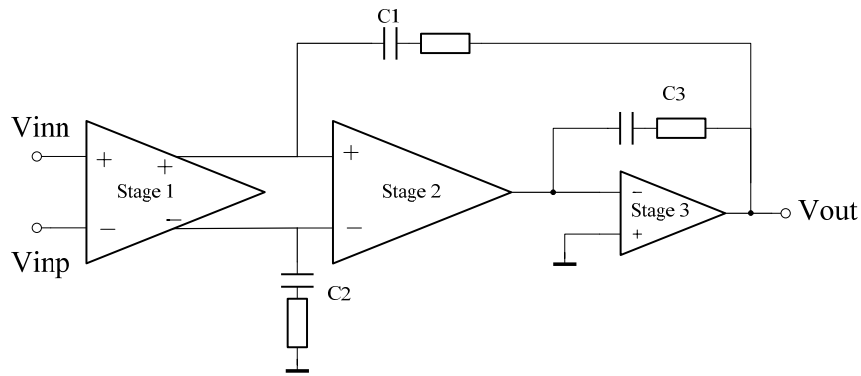


Figure 4. 20 Nested Miller Compensation for the Integrator amplifier

4.4.2 The H amplifier

This amplifier is reused as the differentiator amplifier and the feedback-resistor amplifier. Its performance requirements are summarized in Table 4. 13. The schematic is shown in Figure 4. 21. The two-stage structure is chosen for the H amplifier, with the first stage as the folded cascode and the second stage as the class-AB output.

From Table 4. 13 it's seen that (1) this amplifier is designed to drive a large capacitive load. So it can be used as the differentiator amplifier with its output connected to bonding pad directly. It is also designed with a high GBW so that the system bandwidth is not limited here. (2) This amplifier is designed with a large driving capability. It can provide an output current as large as 50uA and allows a voltage swing of 3.2V. So it can be used as the active control for the current division when implementing the feedback resistor. Its DC gain is also high enough to keep the two transistors under the same biasing condition.

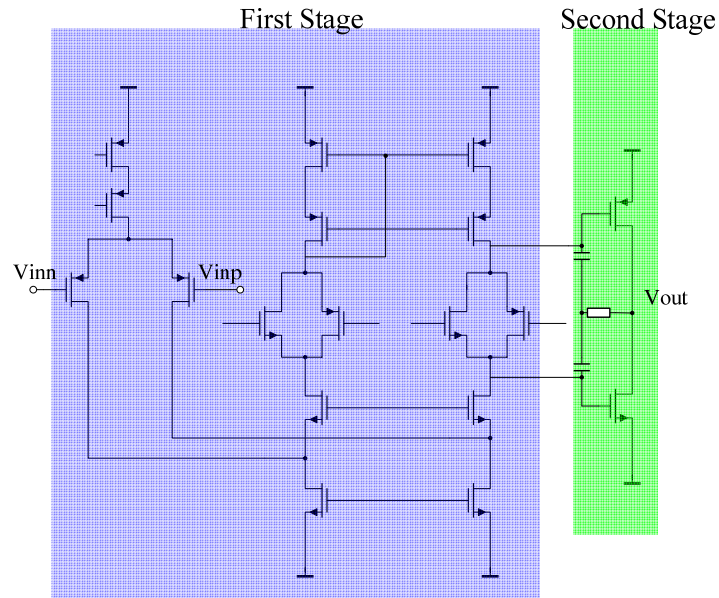


Figure 4. 21 the Schematic of the H amplifier

Specification	Required Value	Achieved Value
Input DC Voltage	1.6V	1.6V
GBW	>5MHz	8MHz
Output Swing	3.2V	3.2V
DC Gain	120dB	123dB
Input Referred Noise	—	$20\mu V/\sqrt{Hz}$ @1Hz $103nV/\sqrt{Hz}$ @10kHz
Capacitive Load	21pF	25pF
Slew Rate	—	3V/usec
Phase Margin	60 degree	65 degree
Power Consumption	—	520uA

Table 4. 13 Specifications for the H amplifier

Noise Analysis: the Feedback Path

It's worth a notice that the H amplifier $A_h(s)$ and the feedback-resistor amplifier $A_f(s)$ are both located in the feedback path. This active feedback influences the noise performance of the integrator stage directly.

The noise contributed by the feedback path is shown in Equation 4- 44. The first item is the input referred current noise contributed by $A_h(s)$; the second item is the input referred current noise contributed by $A_f(s)$; the third item is the input referred current noise contributed by the resistor R_{f0} ; the last item is the shot noise contributed by the diode-transistor M6 referring to Figure 4. 18.

$$i_{feedback,n}^2 = \frac{v_{H,n}^2 |A_h(s)|^2}{(MR_{f0})^2} + \frac{v_{f,n}^2}{(MR_{f0})^2} + \frac{4kTR_{f0}}{(MR_{f0})^2} + 2qI_{dc} \quad \text{Equation 4- 44}$$

$$= \frac{v_{H,n}^2 (|A_h(s)|^2 + 1)}{(MR_{f0})^2} + \frac{4kTR_{f0}}{(MR_{f0})^2} + 2qI_{dc}$$

For the concerned signal bandwidth, $|A_h(s)| \ll 1$ so that:

$$i_{feedback,n}^2 = \underbrace{\frac{v_{H,n}^2}{(MR_{f0})^2}}_{i_{f1,n}^2} + \underbrace{\frac{4kTR_{f0}}{(MR_{f0})^2}}_{i_{f2,n}^2} + \underbrace{2qI_{dc}}_{i_{f3,n}^2} \quad \text{Equation 4- 45}$$

Some data is used here to obtain a general idea about how much the noise level is:

$v_{H,n}$	M	R_{f0}	I_{dc}	$i_{f1,n}$	$i_{f2,n}$	$i_{f3,n}$
$100nV/\sqrt{Hz}$	150	330k Ω	10nA	$2fA/\sqrt{Hz}$	$1.5fA/\sqrt{Hz}$	$57fA/\sqrt{Hz}$

Table 4. 14 An example of the noise contribution

4.4.3 Simulations and Layout

In this section the simulation results are introduced in three aspects: (1) the AC simulations; (2) the DC simulations of pseudo-resistors; (3) the transient simulations.

The AC Simulations

(1) The Integrator Stage

The AC simulation results of the integrator stage are introduced first. In Figure 4. 22 the circuits used for simulation are shown. In reality, the three amplifiers A_{int} , A_h and A_f are biased through the DC-servo loop. But huge resistors are used here for biasing so that the Feedforward network and the feedback network can be simulated separately.

It's seen in Figure 4. 23 that the stability is assured for the DC-servo loop, which used to be the big concern of such design. The pole contributed by the Feedforward network is matched well with the zero introduced by the H block. Such matching results in a phase margin of 80 degree. And the unity gain bandwidth of the Loop Gain can be read out as $f_c=812\text{Hz}$. But this simulation result is reliable only in case that the feedback resistor is implemented well, which will be verified in the following paragraphs.

(2) The Differentiator stage

The stability is first verified for this stage by the circuit shown in Figure 4. 25. Figure 4. 26 shows the influence of C_{fd} on the stability. C_{fd} is then selected as 15pF to avoid oscillation.

The Pseudo-resistors

(1) The Feedback Resistor: I-V

As shown in Figure 4. 27 is the I-V curve of the implemented feedback resistor. There is a small asymmetry for the positive and the negative biasing. That is caused by the different offsets of those related amplifiers, which leads to the mismatch in the polarizations of the diode-connected transistors.

Though with the slight asymmetry, a good linearity is achieved in the positive and in

the negative branch respectively. As is shown in Figure 4. 27, the equivalent resistor is $|R_f| \approx 40\text{M}\Omega$ for $V_{in}>0$ and $|R_f| \approx 50\text{M}\Omega$ for $V_{in}<0$.

The direction of the leakage current and the photocurrent determines that V_{in} is negative during the measurement. Compared with the target value i.e. $|R_f| \approx 49.5\text{M}\Omega$, the feedback pseudo-resistor is implemented with an error of 1%, which is acceptable. According to Figure 4. 27, the voltage difference across the feedback pseudo-resistor can range from 0V to 3.2V, thanks to the finely-designed active control.

(2) The Diode-connected Pseudo-resistor: I-V

Figure 4. 28 shows the I-V curve of the pseudo-resistor R_a that comprises of two diode-connected transistors. For an AC operation, the equivalent resistance is the incremental resistance i.e. $R_{eq} = dV/dI$. The resistance is achieved as larger than $10\text{G}\Omega$ for $|V|<0.5\text{V}$. As the DC voltage increases, the resistance is reduced greatly but can be still kept around hundreds of $\text{M}\Omega$. For a DC operation, the pseudo-resistor i.e. $R_{eq} = V/I$ is realized as $\text{G}\Omega$ for $|V|<1\text{V}$.

The Transient Simulations

(1) Sine-wave Input: THD and IMD

This readout system targets at detecting the chopped photocurrent. The distortion caused by the current-to-voltage conversion would influence the demodulation. Therefore the related performance is analyzed for the novel transimpedance amplifier. A two-tone simulation is done with $f_1 = 2.4\text{KHz}$ and $f_2 = 2.5\text{KHz}$. The IMD3 is read out as 68dB. For a simulation at 2.5 KHz, the THD is obtained as 64dB. The simulation results are shown in Figure 4. 29 and Figure 4. 30 respectively.

(2) Square-wave Input: Single pixel

A square-wave current is used to mimic the chopped photocurrent. The corresponding output voltage is shown in Figure 4. 32. As seen there are some distortions since parts

of the high frequency components have been attenuated and filtered. But the information is mainly carried by the low-frequency components that are well amplified and can be fully recovered through the lock-in demodulation. It's verified by the DFT in Figure 4. 29.

(3) Square-wave Input: Switching between several pixels

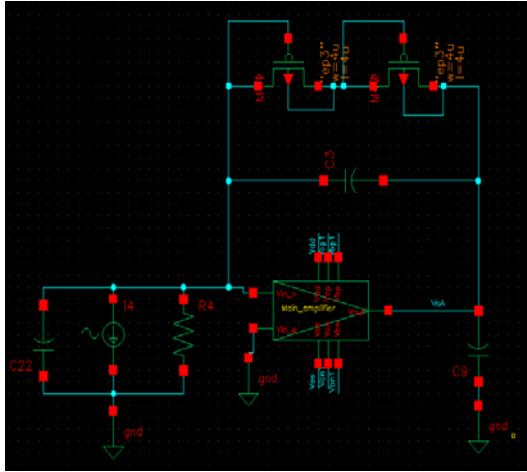
This transimpedance amplifier is shared by 16 pixels through a multiplexer. The circuit used for simulation is shown in Figure 4. 31. Since the measurand is the photocurrent, a path to ground should be found for the pixels when they are not switched onto the readout. The switches are designed to minimize the charge integration on the parasitic junction capacitors.

The readout is simulated taking into account the multiplexer behavior. Three photodiodes illuminated differently are connected to the transimpedance amplifier one by one. The output result is shown in Figure 4. 33.

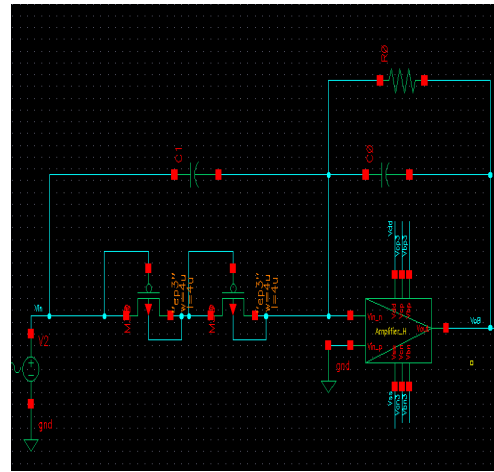
Summary

-3dB Bandwidth	300Hz ~ 1.2MHz
Transimpedance Gain	140dB
Input Referred Current Noise	$105 \text{ fA}/\sqrt{\text{Hz}} @ 1\text{kHz}$

Table 4. 15 the achieved specifications for the fully transimpedance amplifier



(a)



(b)

Figure 4. 22 Circuits for simulations (a) the Feedforward Network (b) the H(s) block

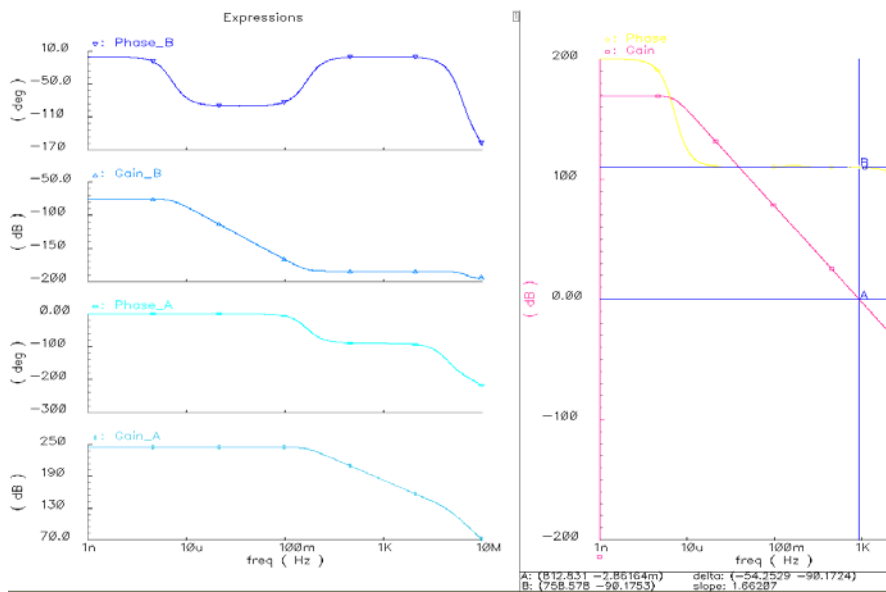


Figure 4. 23 the AC simulations results: A stands for the transfer function of the Feedforward network; B stands for H(s). Supposing Rf is implemented as a 49.5MΩ resistor ideally, then $\text{Gain} = \text{AB}/R_f$ stands for the Loop Gain of the Integrator stage with its Bode diagram shown in right part of the figure.

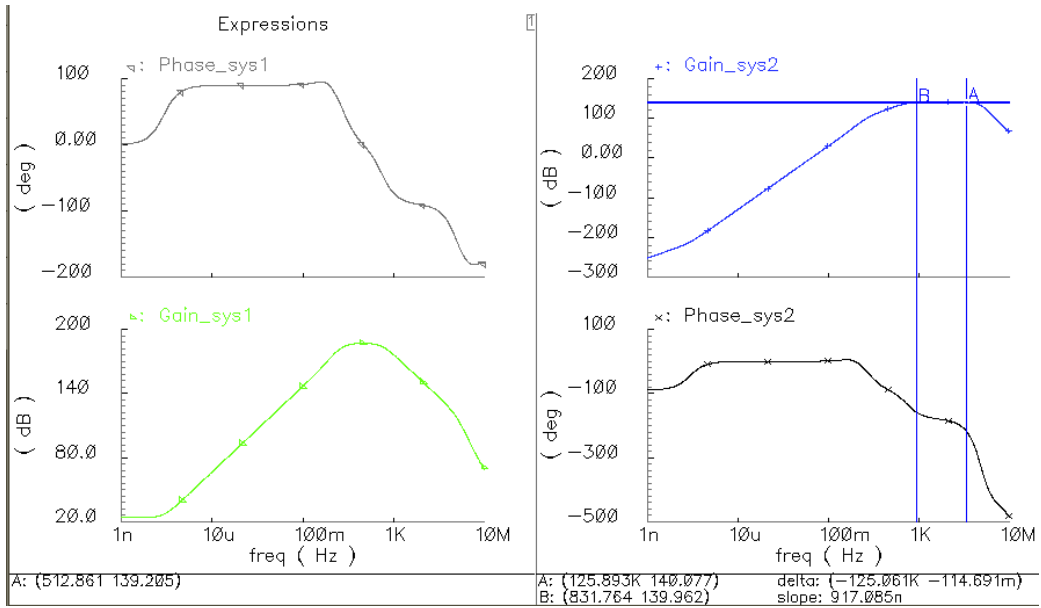


Figure 4. 24 The transfer function of the full Transimpedance Amplifier: the left half part shows the bode diagram of the integrator stage; the right half part shows the bode diagram of the full integrator-differentiator scheme.

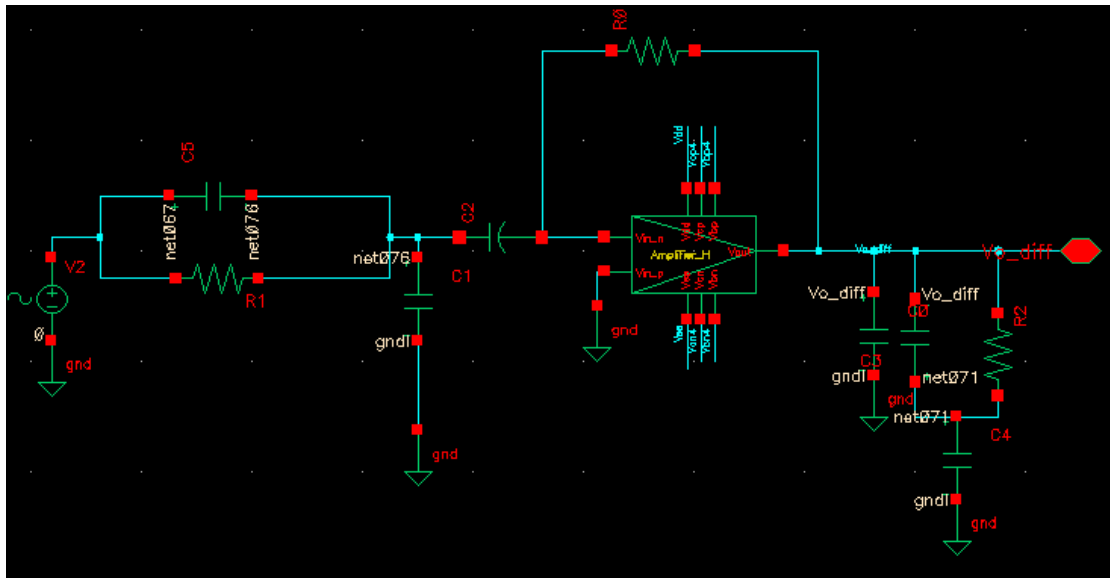
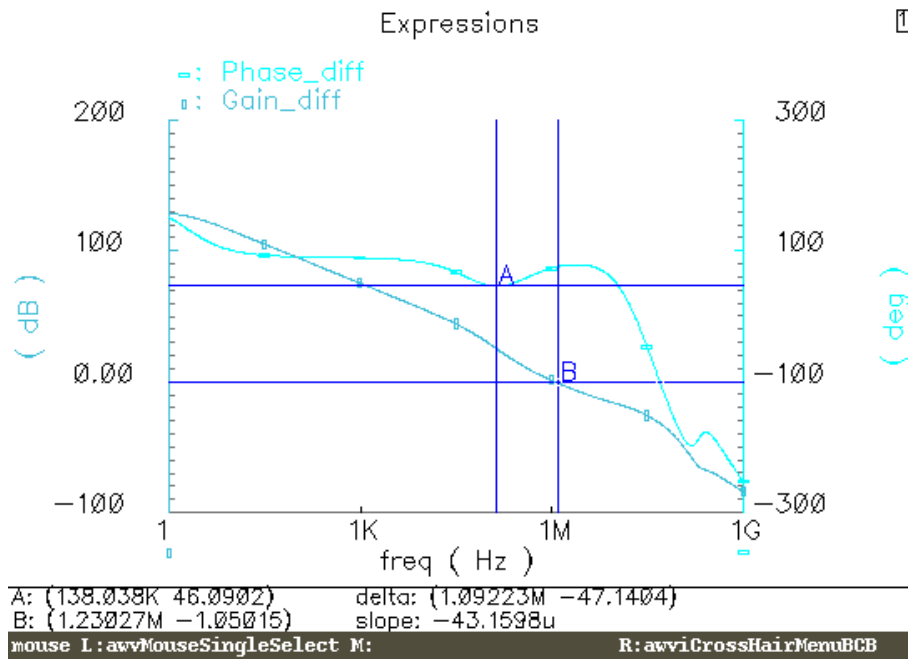
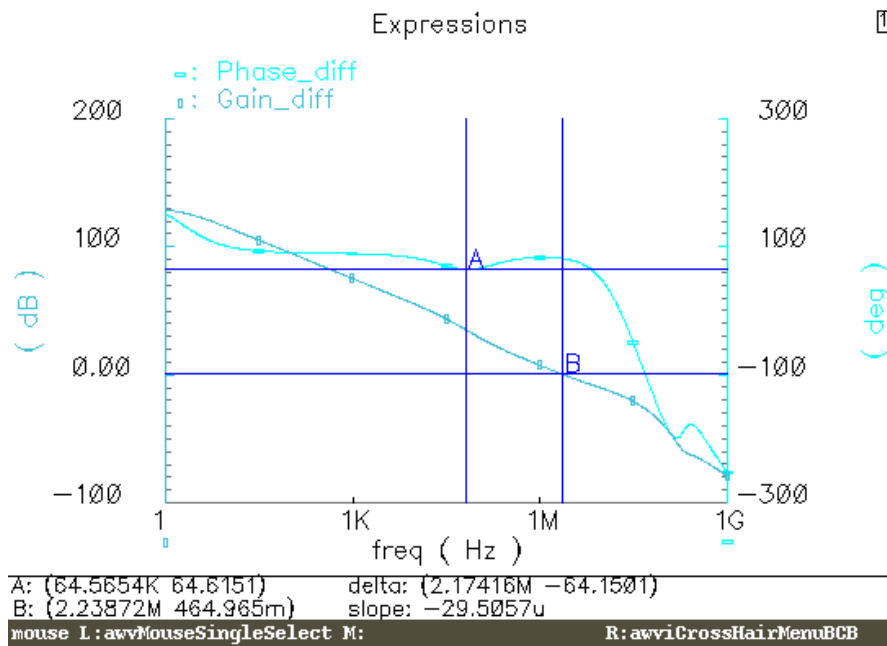


Figure 4. 25 the circuit for the phase-margin simulation of the Differentiator Stage



(1) Cfd = 5pF



(b) Cfd = 15pF

Figure 4. 26 the result of the phase-margin simulation for the Differentiator Stage

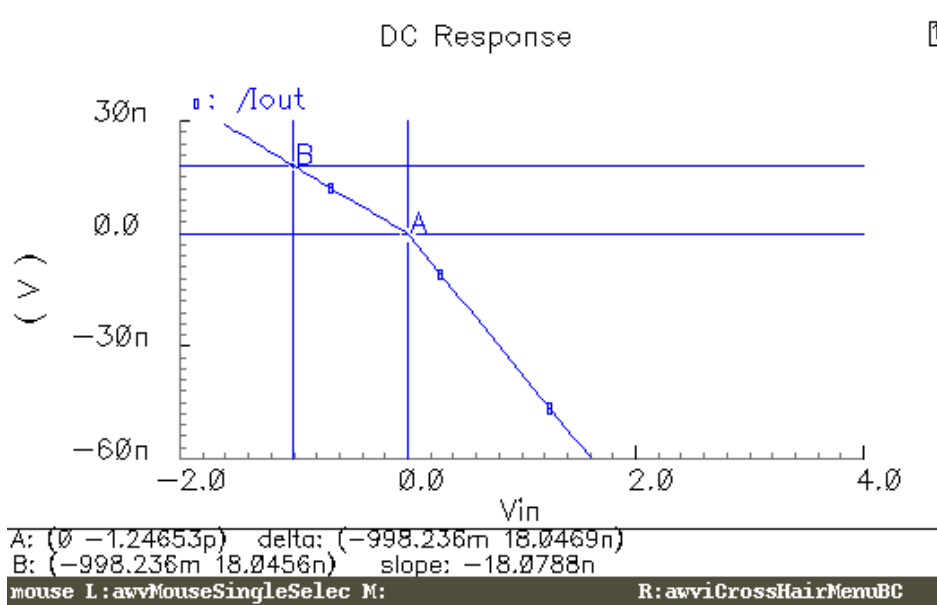


Figure 4. 27 I-V characteristics of the feedback resistor

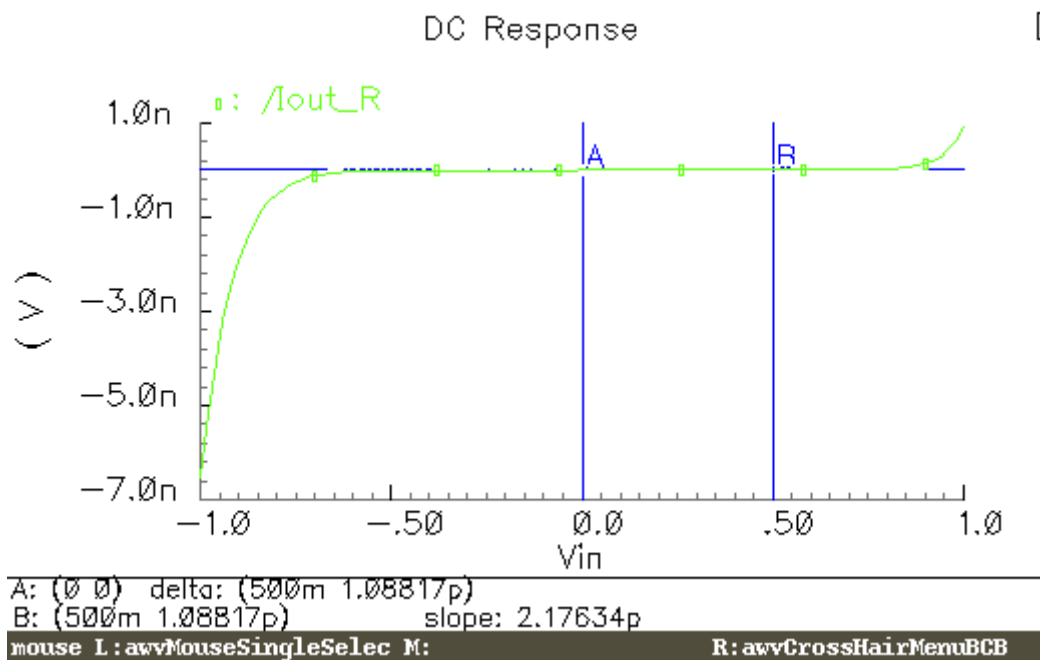


Figure 4. 28 I-V characteristics of the two diode-connected transistors

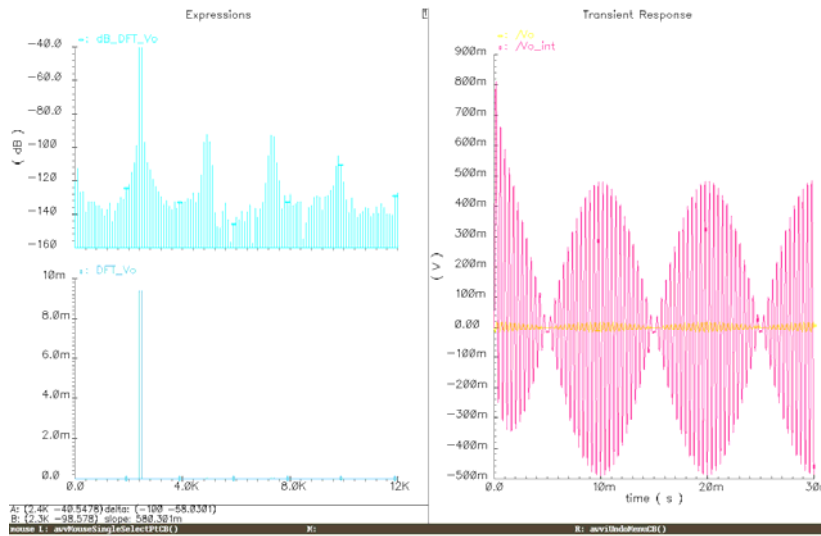


Figure 4. 29 the Two-tone Simulation with the transient and the DFT results

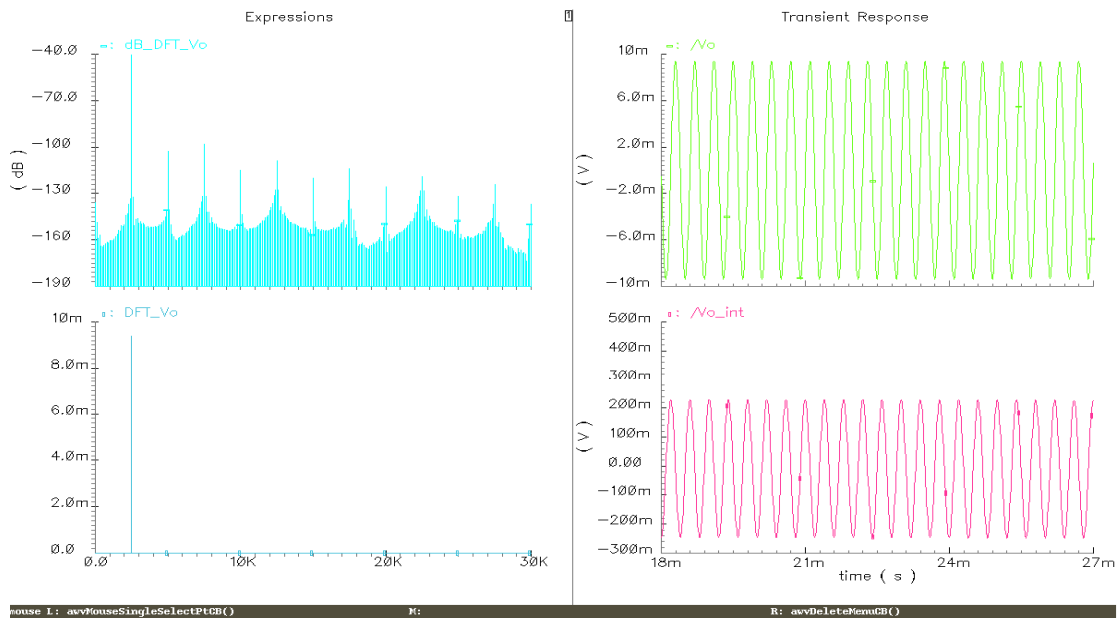


Figure 4. 30 the THD simulation @ 2.5 KHz

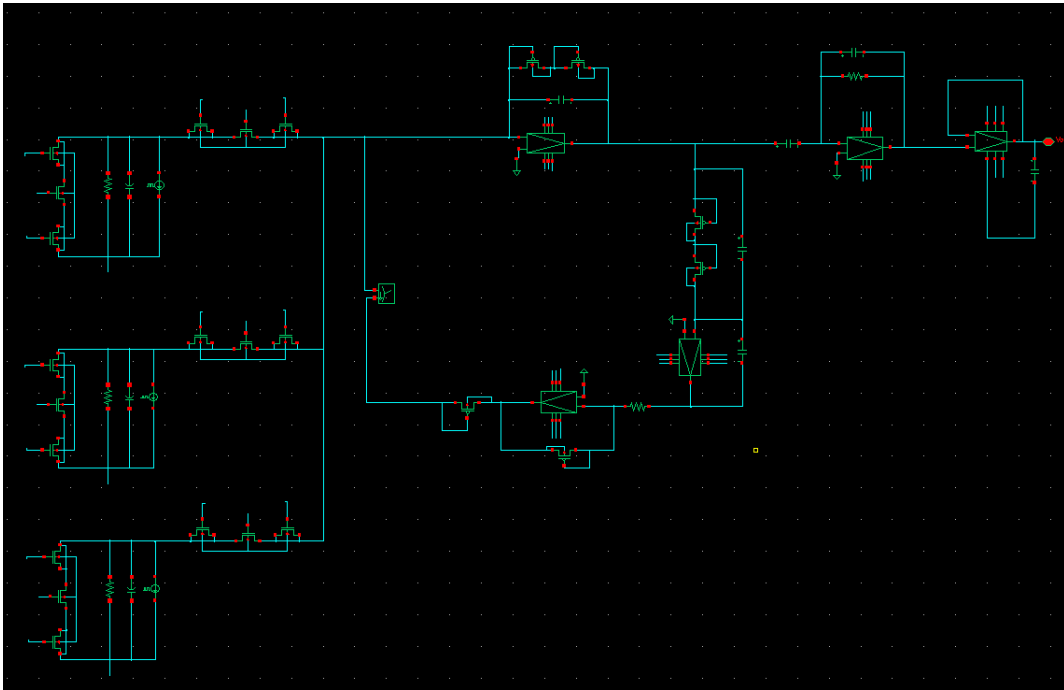


Figure 4. 31 the schematic for the transient simulation with multi-pixels

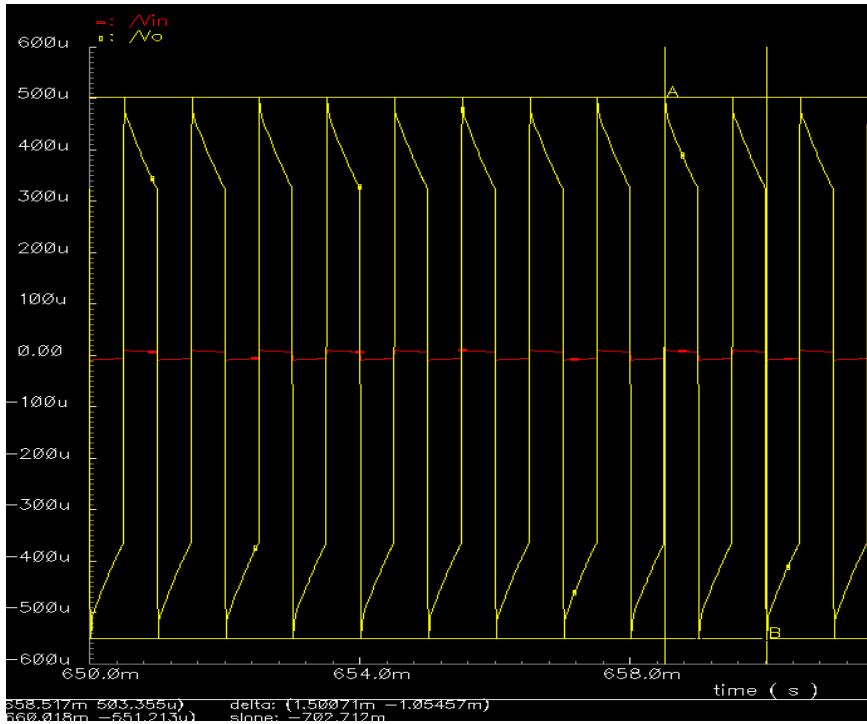


Figure 4. 32 the simulation result for the single pixel with a square wave input current

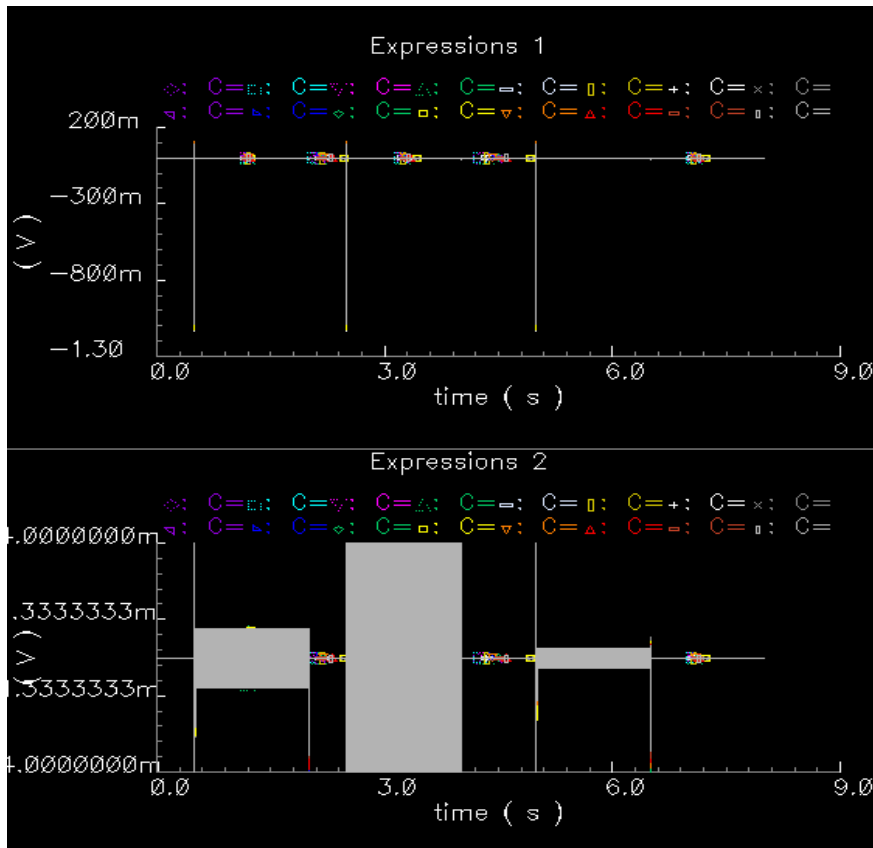


Figure 4. 33 the transient simulation result for multi-pixels

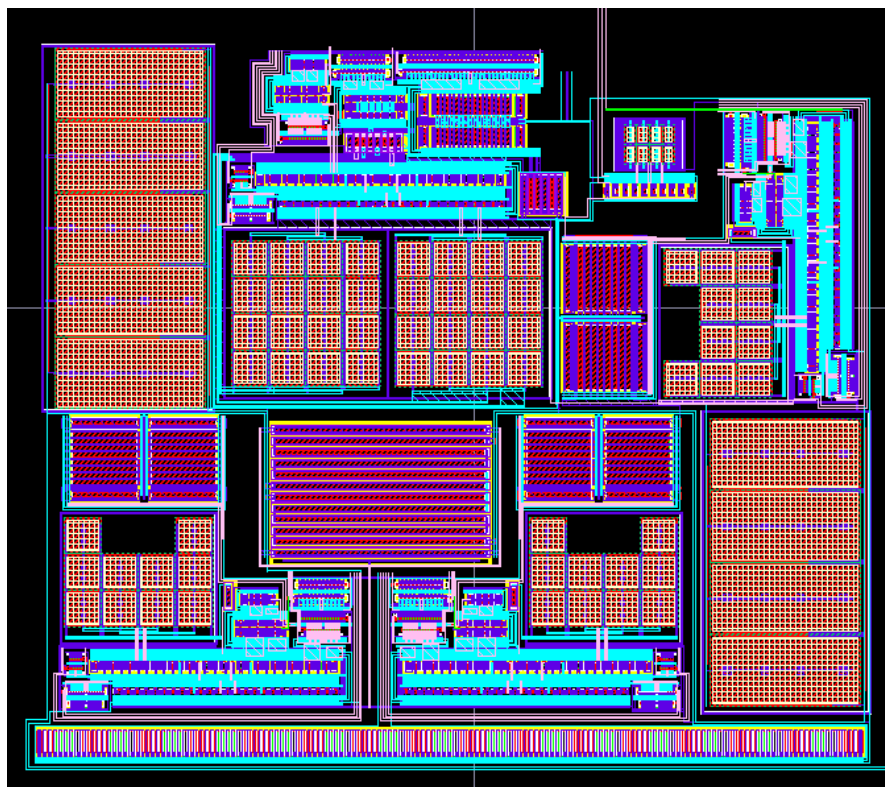


Figure 4. 34 the layout overview of the transimpedance amplifier

4.5 Conclusion

In this chapter, the transimpedance amplifier is realized with two functions: (1) perform the current-to-voltage conversion with a high GBW; (2) perform the separation between the input DC components and AC components. Thanks to the two features, the coherent detection can be done with a high dynamic range and a good sensitivity. The noise analysis shows that a photocurrent as low as 200fA can be detected with the assistance of an optical chopper and a lock-in amplifier. Though the leakage current still sets the detection limit by shot noise, the leakage-related offset is minimized for this design. The achieved specifications would be verified by the measurement results in Chapter 5. The layout overview of the transimpedance amplifier is shown in Figure 4. 34.

4.6 Reference

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Chapter 5 Measurement Results

This chapter focuses on the measurement of the designed linear imaging system. The setup architecture is introduced first, followed by a simple analysis of measurement strategy. The measurement results are finally presented. The photodiode array and a few test structures are tested independently to figure out more potential detector suitable for the microspectrometer. The performances of the two readout systems are summarized and compared with the theoretical analysis. Finally the conclusions are drawn and it's pointed out how this imaging system performs in different applications. First of all, the die photo of the chip is shown here.

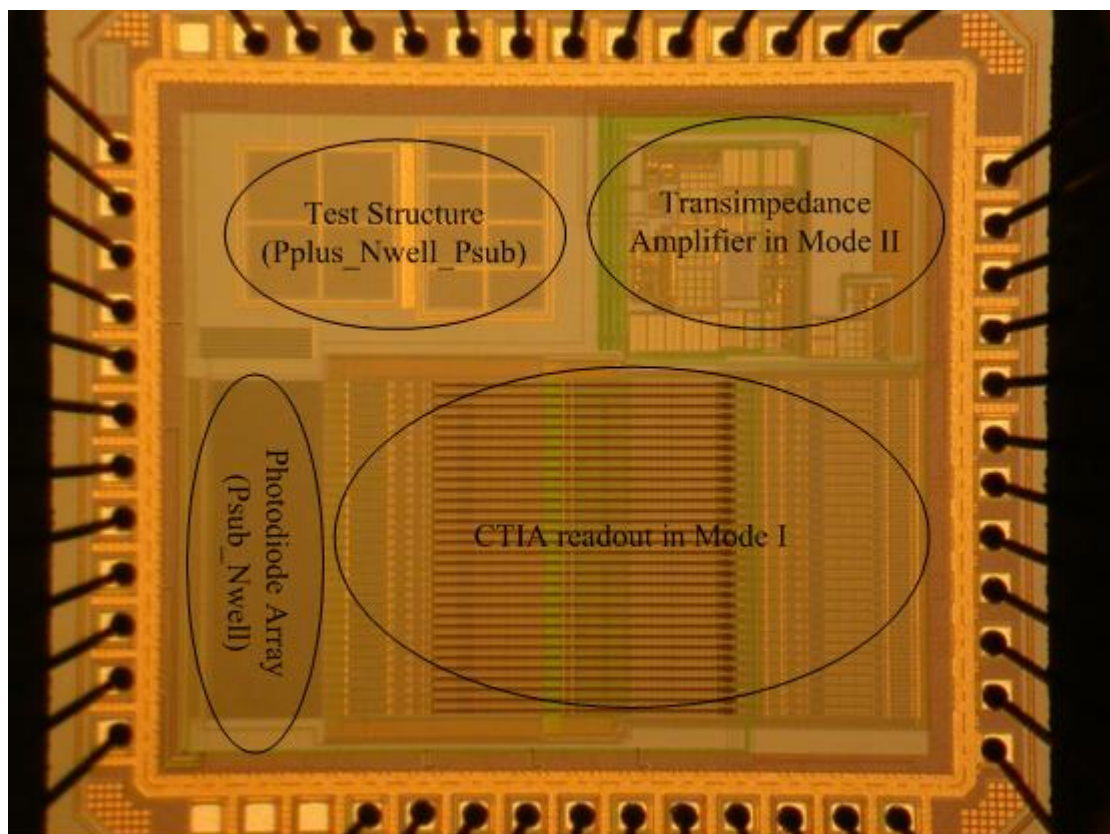


Figure 5. 1 the die photo for the chip

5.1 Measurement Setup

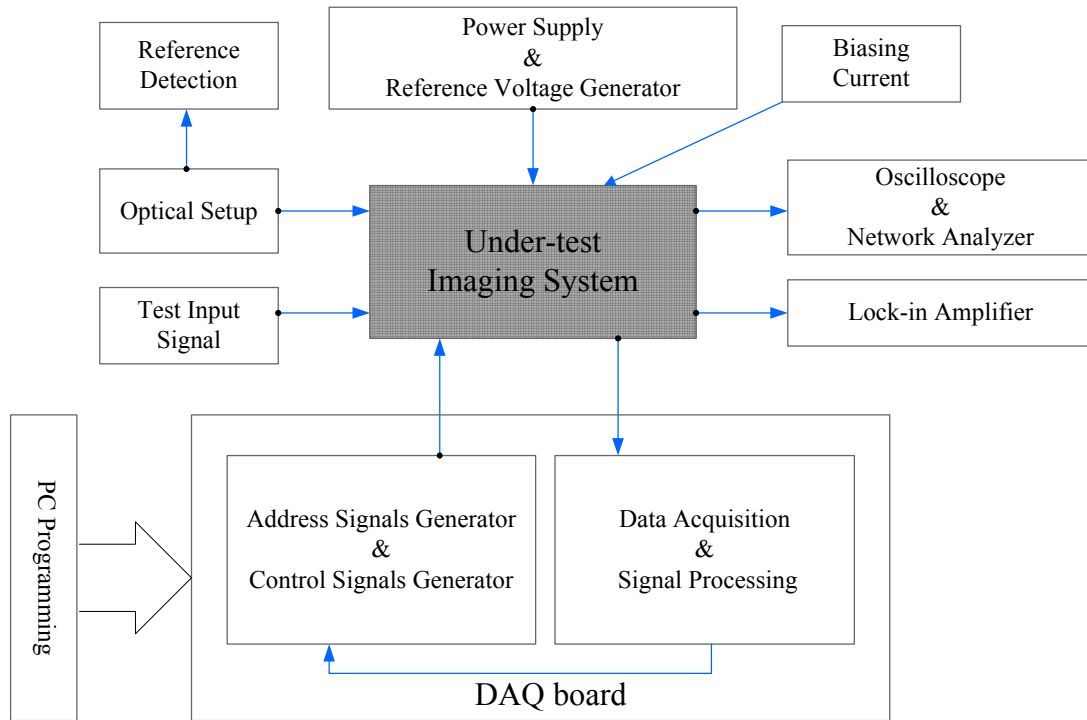


Figure 5. 2 the measurement setup for the imaging system

The measurement setup is presented in Figure 5. 2. In this stage of measurement, the dispersion system is not included. The function of imaging sensing is initially tested. A simple description is listed below for each block.

Optical Setup & Reference Detection

The illumination should be collimated and projected onto the detectors uniformly. A laser light source can be used, followed by a pinhole and an attenuator which adjusts the incident light intensity for the image sensor. A commercial photodetector from Oriol Instrument (Model 71638) is utilized as a reference, with which the optical power density can be calibrated. The measurement results of the linear imaging system can be compared with the reference for a detailed analysis. An optical chopper is applied for the measurement of System II.

Power Supply & Reference Voltage Generator

Voltage regulators are utilized to generate the power supply voltage ($V_{dd}=3.3V$) and two reference voltage ($V_{in1}= 1.6V$ and $V_{in2}=0.9V\sim 1.6V$). The regulators are applied to provide stable and accurate voltages. A good driving capability is provided, especially for the power supply terminal.

Biasing Current

As designed and simulated, a biasing current of $1\mu A$ should be supplied for the chip. The programmable DC source YOKOGAWA 7651 is utilized. It is monitored continuously to ensure the accuracy.

Test Input Signal & Oscilloscope

The test signal would be applied at the inputs of the two readout systems respectively. The purpose is to test the readout performance independent of the photodiodes. The network analyzer can be used to obtain the Bode plot. The transient response can also be monitored at several test pins by the oscilloscope.

Lock-in Amplifier: for System II

The lock-in amplifier is only used for the measurement of System II. It's used as the demodulator in the coherent detection. The output of the transimpedance amplifier would be connected directly to the input of the Stanford SR531. The demodulated result would be read from the screen directly.

DAQ Board: for System I

The DAQ board is mainly used for the measurement of System I. It has three functions: (1) the pixel selection; (2) the CDS control; (3) the sampling and the A-to-D conversion. The encoding from the natural binary code to the grey code is finished within the Lab View. The resulted address signals are then transported onto the chip. With a proper programming, the dynamic integration duration can be achieved accurately outside the chip.

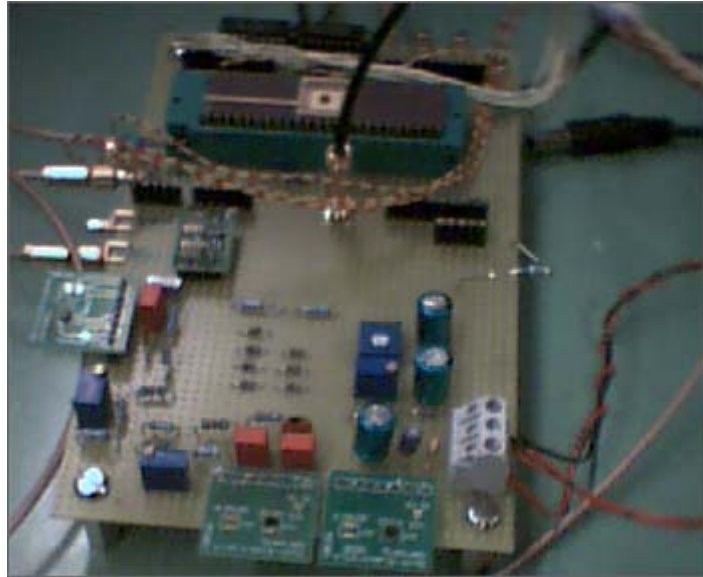


Figure 5. 3 the electrical measurement setup (including the power supply& reference voltage generator, the input of biasing current and the test outputs)

5.2 Measurement Strategy and Initial Measurement Results

This imaging system is designed to have two readout modes which can work independently. A proper measurement procedure is arranged to obtain valid measurement results.

Step Number	Content
Step 1	Calibration of the Optical Power
Step 2	Testing of the photodiode array and the test structure (including the I-V curve of the leakage current, the spectral response and the responsivity)
Step 3	Testing of System I (including sensitivity, effects of CDS, fixed voltage difference control, temporal noise and Fixed Pattern Noise)
Step 4	Testing of System II (including tests of different blocks, the frequency response, the step response, the noise performance and the coherent detection)

Table 5. 1 the measurement procedure

Since the time is limited, a full measurement procedure has not yet been finished. Only a few initial measurement results are obtained, which shows the basic function of the imaging system.

5.2.1 Photodiode Characterization

I-V curve of the leakage current

The leakage current of one pixel is tested for the linear photodiode array, which is shown Figure 5. 4. It is observed that the leakage current goes to 4pA for a biasing voltage of 1.6V.

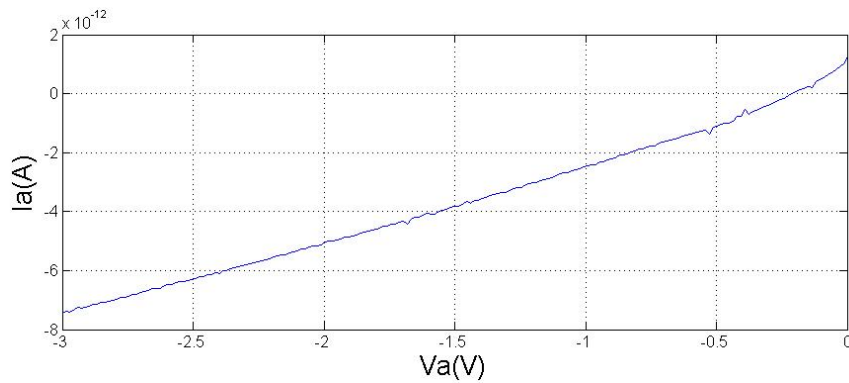


Figure 5. 4 leakage current V.S. reverse bias voltage for the psub-nwell junction

The leakage current of the test structure is also listed, i.e. the double junction shown in Figure 2. 3(b). As is shown in Figure 5. 5, the leakage current goes to 10pA as the reverse bias voltage increases to 1.6V.

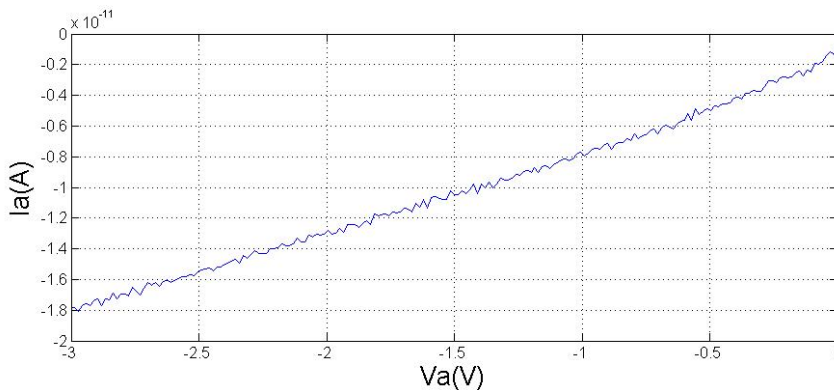


Figure 5. 5 the leakage current V.S. reverse bias voltage for the double junction

Spectral response of Photodiodes

The spectral response of the psub-nwell junction is tested and shown in Figure 5. 6.

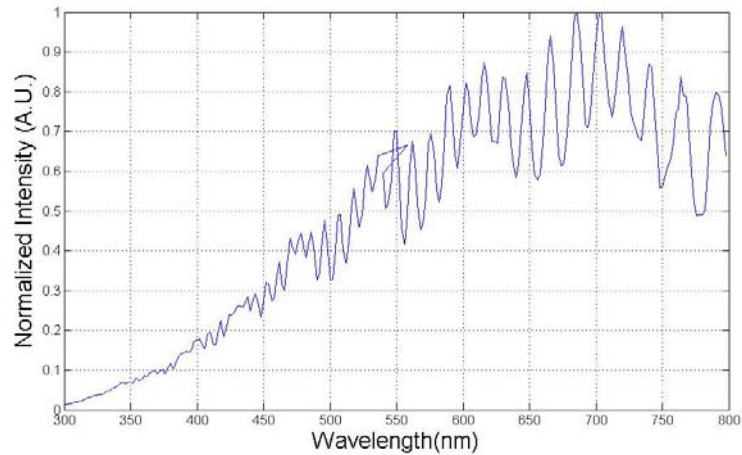


Figure 5. 6 the spectral response of the psub-nwell junction

5.2.2 Readout Characterization

Test of Mode I

The Pixel No.127 is selected to observe the continuous voltage change during the integration. The CTIA has its output monitored by the oscilloscope. The illumination changes from strong to weak. A fixed integration is applied with $T_{int} = 0.5\text{msec}$. The reset pulse is applied at the end of each period.

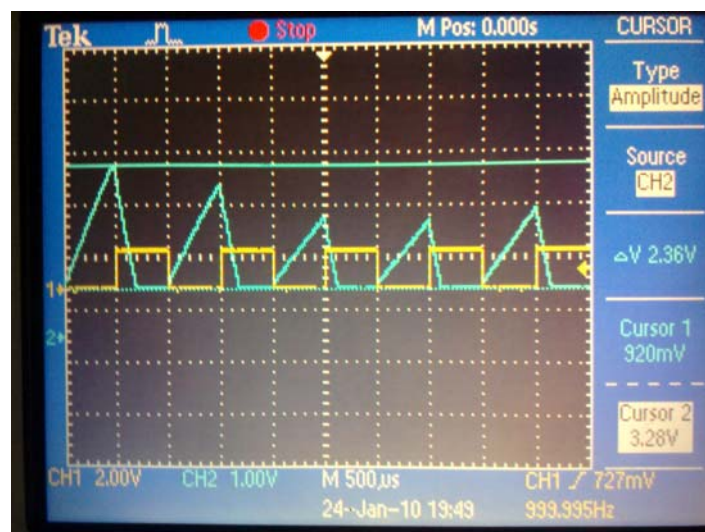


Figure 5. 7 the CTIA readout for different illumination ($T_{int} = 0.5\text{msec}$)

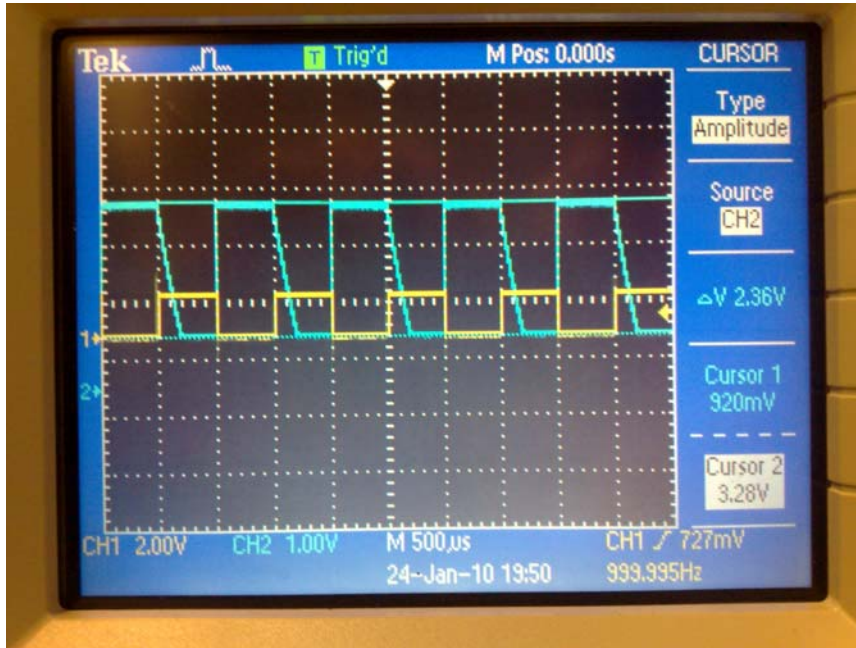


Figure 5. 8 the CTIA readout for high illumination ($T_{int} = 0.5\text{msec}$)

As shown in Figure 5. 7, the illumination decreases from high to low for the first three periods during which the detected peak voltages changes from 3.3V, to 2.9V and then to 2.3V. As shown in Figure 5. 8, the output voltage is saturated in a short time due to the really high light intensity. Figure 5. 9 shows that an integration time as long as 4sec can be applied for low illumination detection.

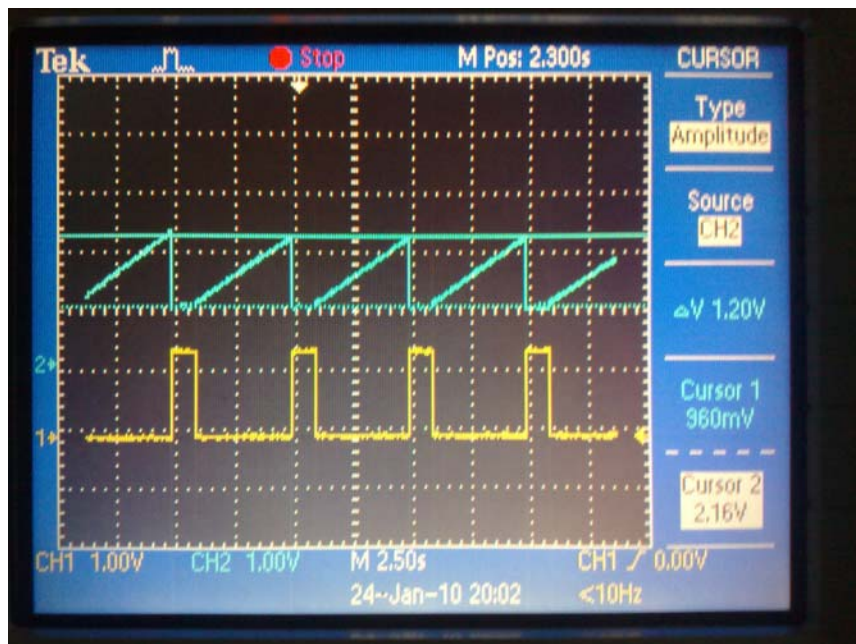


Figure 5. 9 the CTIA readout for low light intensity ($T_{int}=4\text{sec}$)

Test of CDS

The operation of CDS is observed for the Pixel No.127 as is shown in Figure 5. 10. Figure 5. 9 shows the voltage on the sampling capacitor decreases dramatically, which could be due to the parasitic shunt resistance.

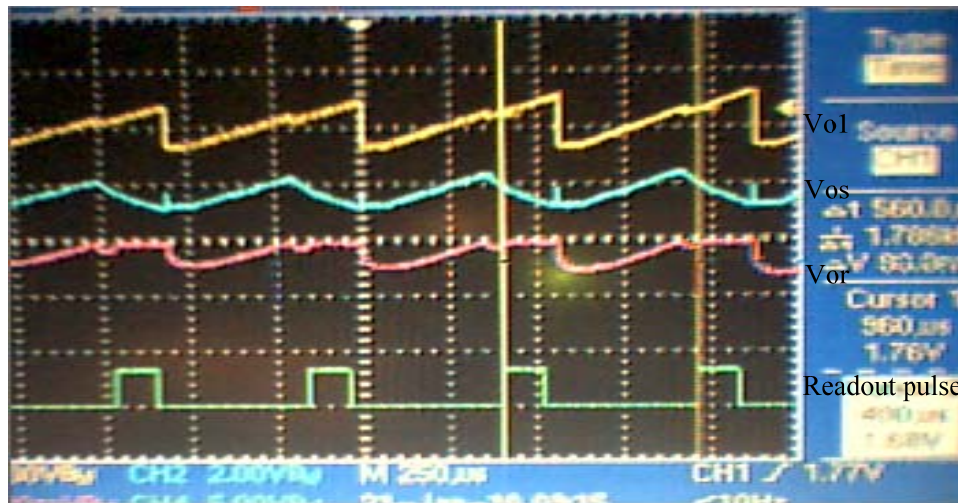


Figure 5. 10 the CDS with short integration time (Vo1, Vos, Vor and timing chart)

Fixed Voltage Difference Control

The operation of Fixed Voltage Difference Control is observed for the Pixel No.127. Vo1 is sampled at a time interval of Tclk by the DAQ board. The sampled value is compared periodically with the reference voltages in order to generate the control signals based on the rules below:

- (i) when $V_{o1} < V_1$, the counter is kept reset;
- (ii) when $V_{o1} \geq V_1$, the counter is started up;
- (iii) when $V_1 < V_{o1} < V_2$, the counter keeps counting;
- (iv) When $V_{o1} \geq V_2$, the counter stops counting and generates a reset pulse with the width of Tclk.

According to the program, the values of V1 and V2 can be changed flexibly.

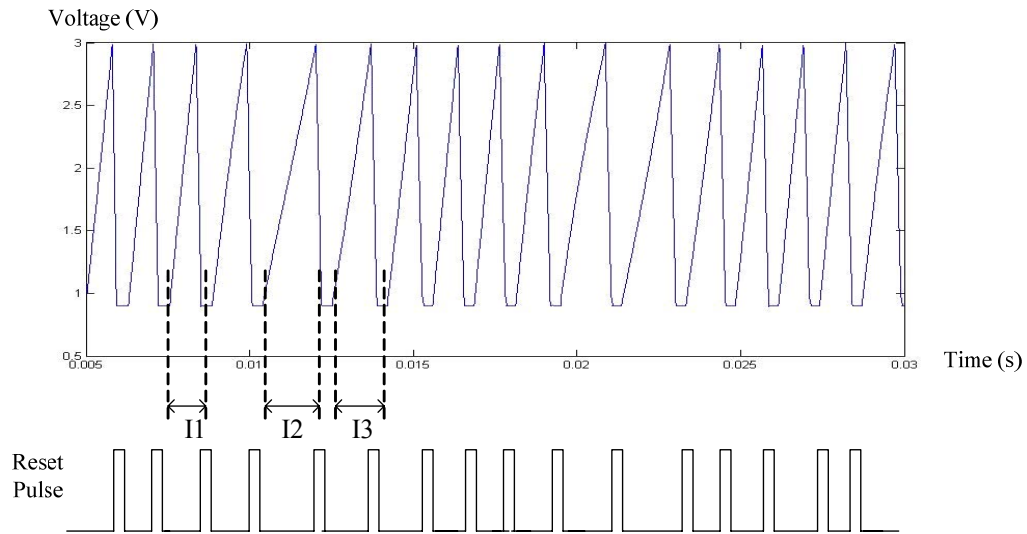


Figure 5. 11 the Fixed Voltage Difference Control ($V_1=0.9V$; $V_2=3V$; $T_{clk}=10\mu s$)

Figure 5. 11 shows a measurement result for variable light intensities, where I_1 , I_2 and I_3 stand for the illuminations in the correspondent periods. Since $T_{int1} < T_{int3} < T_{int2}$, it can be concluded that $I_1 > I_3 > I_2$.

5.3 Conclusion

With the initial measurement results, it has been shown that the Mode I designed in Chapter 3 can work properly together with Correlated Double Sampling to reduce noise and with Fixed Voltage Difference Control to increase the dynamic range. An integration time as long as 4sec can be applied for the low illumination detection. The transimpedance amplifier in Mode II is also tested initially. Furthermore the DC biasing point of circuitry has been proved correctly operated. And the DC-servo loop is able to work making the DC photocurrent flowing through the R_f . An extensive measurement is still required, so as to prove the full function of the double-mode linear imaging system.

Chapter 6 Conclusion and Future Work

A double-mode linear imaging system is designed, fabricated and preliminary tested. Double-mode indicates two different readouts implemented separately to measure photo current for spectroscopy application. This imaging system is anticipated to work with two optical dispersion systems (i.e. the LVOF and the PDGS) to realize high-resolution microspectrometers. The prototype of linear image sensor is fabricated with standard 0.35um CMOS process.

6.1 Conclusion and Highlight of the work

The goal of this thesis is to find solutions for single-chip microspectrometers which have found applications in many fields due to their low cost and low sample volume. A Planar-double-grating System and a Linear Variable Optical Filter have been developed for optical dispersion in microspectrometers. Their developments generate a demand for linear imaging systems that have optimized performance in high-sensitivity low-illumination detection. The highlights of this thesis are concluded as below:

- (1) The imaging features are elaborately explored for the developed PDGS and LVOF, leading to an optimum design of photoelectric devices.
- (2) Leakage current as the main challenge in low-illumination detection is analyzed. Two modes of readout are proposed separately for the low-leakage-current case and the high-leakage-current case, to achieve best performances in different application.
- (3) For low-leakage-current case, the integration mode is applied and implemented, so as to lower the detection limit and increase the measured SNR by extending the integration time. The Capacitive Transimpedance Amplifier is applied to achieve a high sensitivity and a better linearity with reduced reset noise. The traditional technique in CMOS image sensors, i.e. Correlated Double Sampling, is also

implemented in this mode for decreasing noise and improving accuracy. Furthermore, the Fixed Voltage Difference Control is proposed to increase the measured dynamic range by using variable integration time.

- (4) For high-leakage-current case, the integration mode is considered less useful since the leakage current causes a huge offset and contributes a large shot noise. Therefore the coherent detection is proposed to reduce the influence of leakage current. The whole detection system then comprises an optical chopper, a linear photodiode array, a transimpedance amplifier and a lock-in demodulator. A novel transimpedance amplifier is designed specially for this application, with a DC-servo loop to increase the dynamic range and with an integrator-differentiator scheme to enlarge the bandwidth.

6.2 Future work

The basic functions have been realized for the two modes of readout. The readout principles are proved to be promising in microspectrometers. Several practical efforts will result in a more integrated imaging system.

For Mode I, those efforts include: (1) Integrating the digital circuits for the Fixed Voltage Difference Control in each pixel. This effort can not only improve the readout speed, but also integrate the A-to-D conversion on-chip. (2) Integrating the powering-down function. When the readout speed is not the limiting factor, the pixels can be accessed one by one randomly. The columns that are not being accessed can be powered down for saving power consumption. (3) Simplifying the input amplifier and the buffer.

For Mode II, the main drawback is that the whole detection system is complex. It is necessary to add chopping function externally. The efforts will be focused on integrating the function of lock-in demodulation on-chip.