# CMOS Drivers for RF-DACs

Ossama El Boustani

Technische Universiteit Delft

TU Delft

# CMOS Drivers for RF-DACs

by

Ossama El Boustani

to obtain the degree of Master of Science
at the Delft University of Technology,
to be defended publicly on Monday, June 5, 2023 at 12:30.

| | | |
|---|---|---|
| Student number: | 4542274 | |
| Project duration: | September 1, 2021 – August 31, 2022 | |
| Thesis committee: | Prof. dr. ir. L. C. N. de Vreede, | TU Delft, Chair ELCA, supervisor |
| | Dr. ir. F. Sebastiano, | TU Delft, EI |
| | Dr. ir. S. M. Alavi, | TU Delft, ELCA |
| | Ir. R. J. Bootsman, | TU Delft, ELCA, supervisor |
| | J. R. Gajadharsing, | Ampleon |

*This thesis is confidential and cannot be made public until June 1, 2025.*



TU Delft AMPLEON

# Summary

This work describes a fully digital transmitter (DTX) for 5G mMIMO base stations that combines the strengths of high-speed digital CMOS with the high-power capabilities of a Monolithic Microwave Integrated Circuit (MMIC) high-voltage technology. This technology platform offers high integration and scalability for implementing Radio Frequency Digital-to-Analog Converters (RF-DACs). To facilitate the digital operation of the gate-segmented output power stage, a custom $V_T$-shifted LDMOS technology has been utilized. The relatively high output capacitance of the LDMOS devices makes digital class-C operation the preferred class of operation to achieve high efficiency with good linearity metrics for the digital power amplifier (DPA). In this work, we analyze this operation, assuming a trapezoidal-shaped current profile, which allows investigation of the impact of the non-zero rise and fall times on the theoretical (normalized) output power and drain efficiency.

To drive the gate segments in this custom $V_T$ LDMOS technology with a gate-to-source voltage ($V_{GS}$) swing of 2.2 V, a driver is proposed comprising: inverter chains, a level shifter, and a high-voltage output buffer. This driver is fully digital and can be implemented using thin-oxide bulk CMOS devices whose $V_{DD}$ is limited to 1.1 V. A model of the DTX comprising only the drivers and DPA at the circuit level is created in ADS to evaluate the output power, drain efficiency, and system efficiency. The DTX is simulated at 3.5 GHz full power and achieves an output power of 19.79 W/23.43 W, a drain efficiency of 67.28%/59.22%, and a system efficiency of 60.34%/54.48% with a non-empirical and empirical model of LDMOS, respectively. Rise and fall times of around 20% of the RF cycle ($t_r = t_f = 0.2/f_c$) are found to be the most suitable in terms of power consumption and system efficiency.

# Acknowledgments

The starting moment of this thesis traces back to before COVID lockdowns. As part of an orientation event for bachelor students in their final year, the TU Delft organized tours to the different research departments at EEMCS. Professors gave a small demonstration of current research projects at their department. A particular professor was very enthusiastic while showing off a magical box. This professor is Prof. Dr. L. C. N. de Vreede (Leo), holding what I later discovered to be a power amplifier for base stations. As luck would have it, my dear friend Mohammed Abo Alainein was also interested in pursuing a master's degree in microelectronics after graduation.

While picking up interesting courses, he happened to pick up RF-related courses. My interest in wireless communications only grew more after taking these courses. Especially after hearing Leo say: "You might think that everything is already invented, but there is still work for you to do!" I might be paraphrasing here, but this stuck with me. While working on my thesis project, my knowledge and skills have expanded. I sincerely thank Leo de Vreede and Rob Bootsman, who taught and guided me during this journey. They were enormously resourceful mentors. They were very patient with me and granted me to have complete freedom to be creative. My gratitude also goes to Ampleon for their financial support. Not to forget my fellow ELCA members, including master students and PhD. candidates, thank you all for both the lovely social and insightful technical discussions. Last but not least, my gratitude goes to my loving family for supporting me in every sense of the word.

*Ossama El Boustani*
*Delft, April 2023*

# Contents

# List of Figures

# List of Tables

# 1 Introduction

People have always found ways to communicate with one another, such as smoke signals and church bells. In the 19th century, James Clerk Maxwell theorized electromagnetic waves in 1864, and Heinrich Hertz validated the theory in 1887, paving the way for Guglielmo Marconi's transatlantic transmitters. The potential of wireless communication and the tactical advantage it can bring to warfare was quickly recognized by the British, Italian, and American navies. Furthermore, forget about winning wars; try entertaining a child without the internet, and you will quickly discover that it is (virtually) impossible. Put differently, with all of the benefits that wireless communication provides, it has become indispensable.

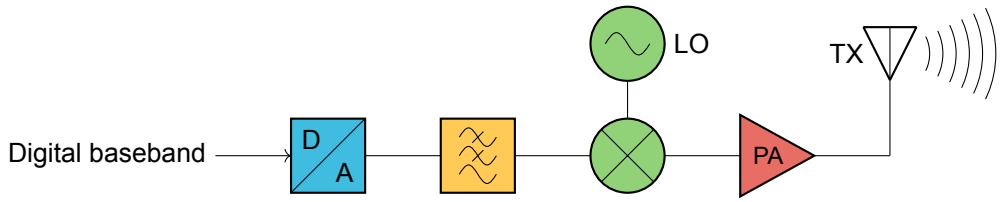
So, how do we communicate wirelessly? One possible answer can be found by exploring the "apparatus" we use to communicate and refer to as a radio frequency (RF) transceiver. For wireless communication, the highway is free space and the vehicle is electromagnetic (EM) waves. True communication necessitates the ability to both listen and talk. A conventional RF transceiver as depicted in Fig. 1.1 achieves these tasks. In modern (wireless) communication, information is represented by bits. For these bits of information to travel wirelessly from one device to another, they must go through an RF transceiver. It is important to note that Fig. 1.1 oversimplifies wireless communication hardware and merely highlights (some) functional building blocks. Transceiver topologies and modulation techniques are covered in detail in [1].

A transmitter (TX) serves to convert bits into modulated electrical signals first, then into EM waves. A conceptual transmitter is illustrated in Fig. 1.1a. A digital-to-analog converter (DAC) generates electrical signals from bits. A low-pass filter (LPF) removes the aliases at the output of the DAC. A mixer multiplies the signal with a local oscillator (LO) resulting in a signal at RF. In other words, the signals are up-converted. A power amplifier (PA) increases the power level of the up-converted signal. An antenna converts the amplified signal into EM waves and radiates them into free space.

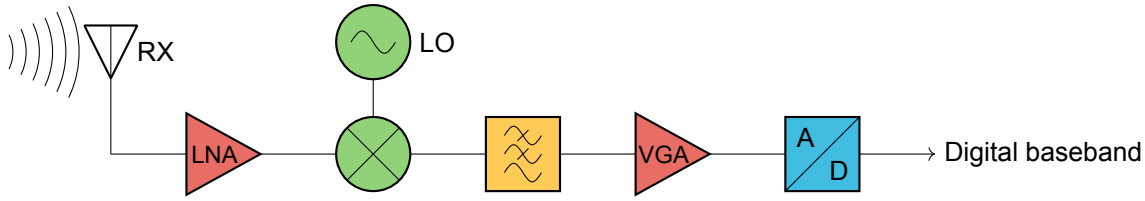
A receiver (RX) converts EM waves to electrical signals, which are then demodulated and converted into bits. A conceptual receiver is illustrated in Fig. 1.1b. The conversion starts at the antenna where EM waves are converted to electrical signals. A low noise amplifier (LNA) amplifies these signals. A mixer multiplies the amplified signals with a local oscillator (LO) and a low-pass filter (LPF) removes the high-frequency signal components. An analog-to-digital converter (ADC) quantizes the down-converted signals. The digital version of the received signals is said to be in the digital baseband.

Radio transceivers are everywhere, ranging from RFID tags on pets and wireless modules in smartphones to commercial base stations. As the demand for more connectivity and higher data rates grows, both spectrum-efficient and energy-efficient wireless networks are highly desired. The number of connected devices is expected to grow to 100 billion by 2030 [2]. As a result, the electricity bill and the environmental impact of wireless communication will grow. The contribution of information and communication technology (ICT) to worldwide greenhouse gas emissions (GHGE) is expected to reach 14% by 2040 [3]. Although studies state a range of contrasting estimates of energy consumption and carbon footprint attributed to global ICT [4], a strong incentive for innovation remains.

The insatiable appetite for higher data rates demands higher levels of integration. Already in 1999, there was a desire to use advanced complementary metal-oxide-semiconductor (CMOS) technology for




(a) Transmitter.




(b) Receiver.

Figure 1.1: An oversimplified block diagram description of a radio frequency transmitter and receiver.

single-chip radio integration [5]. But in contrast to VLSI design, analog/RF circuit design become more difficult in advanced CMOS process nodes. As a result, there is a compelling argument for developing digital architectural solutions for RF functions [6]. A revolutionary development that followed quickly set the stage for a new branch of electronics: Digital RF [7]. It was the first demonstration of a fully-digital frequency synthesizer and transmitter for RF wireless applications. The foundation of Digital RF stems from the following paradigm:

"*In a deep-submicron CMOS process, time-domain resolution of a digital signal edge transition is superior to voltage resolution of analog signals.*" Staszewski in [8]

This new paradigm was leveraged to integrate RF functions and subsequently gave rise to fully-digital transmitter (DTX) architectures [7, 9]. Common DTX architectures, illustrated in Fig. 1.2, exploit digital power amplifiers (DPAs) suitable for handheld devices and capable of driving an external PA for base station applications. A DPA combines the functionality of a DAC and a PA into the same circuit [10]. Additionally, terms such as digital-to-RF amplitude converter (DRAC), bit-in RF-out, or RF-DAC (or RFDAC) are used to refer to similar circuits. With the massive multiple-input and multiple-output (mMIMO) [11], the number of transceivers per base station has increased. The true potential of mMIMO base stations stems from the low-cost and low-power units [12]. Therefore, DTX line-ups (e.g., [13, 14]) are serious competitors for their expansive and power-hungry analog counterparts [15].

## 1.1. Thesis Goal

The aim is to design compact and low-power CMOS drivers in 40 nm bulk CMOS (by TSMC) capable of activating segmented power banks (LDMOS/GaN).

## 1.2. Thesis Objectives

System efficiency is perhaps the most critical metric in transmitter design, at least from the financial perspective of telecommunications operators. Especially when considering mMIMO base stations. For the external PA to achieve high drain efficiency, the CMOS driver must produce pulses with steep edges. Ideally, a rectangular wave yields the best drain efficiency. However, maximizing drain efficiency does not automatically guarantee maximum system efficiency. More specifically, aiming to produce pulses with steeper edges results in an oversized driver, will lead to increased power consumption. Besides, the form factor of a fully digital transmitter must be minimized. Hence, the drivers in a DTX should claim as little chip area as possible.

The design of a CMOS driver suited for a high-efficiency DTX targeting the mMIMO band of 3.5 GHz requires a careful consideration of the trade-offs concerning the CMOS process as well as the entire system. Consequently, the main objectives of this work are as follows:

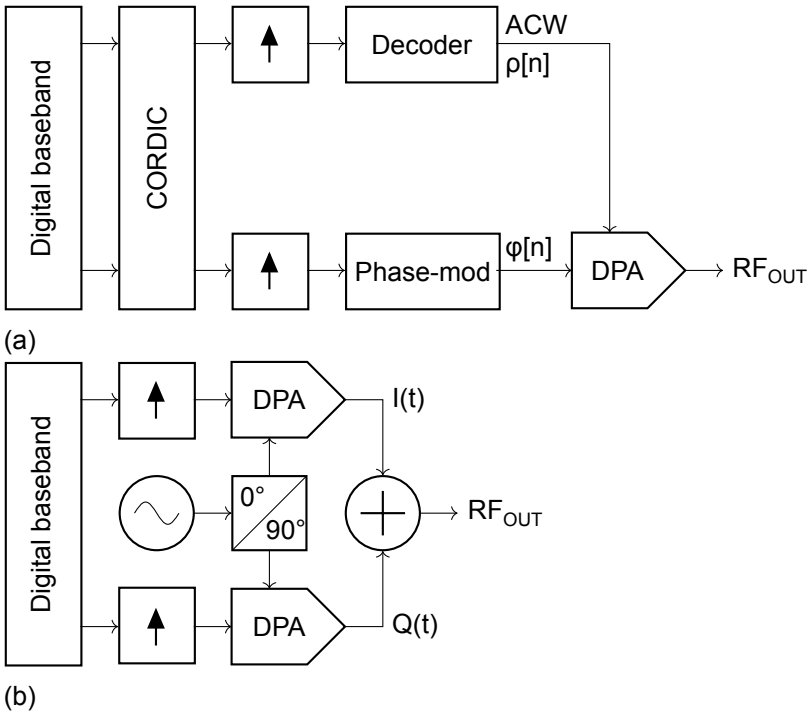



Figure 1.2: (a) Polar and (b) Cartesian digital transmitter architectures.

- The driver operates at a frequency of 3.5 GHz.
- The driver claims no more than 40 µm × 40 µm of chip area.
- The driver can activate capacitive loads up to 150 fF.
- The driver comprises (preferably) only thin-oxide CMOS.
- The driver generates a swing (of at least) 2.2 V.
- The driver consumes low power.

## 1.3. Thesis Outline

This thesis is structured as follows:

In Chapter 2, the fundamentals of power amplifiers are briefly discussed. Pertinent definitions and metrics are introduced. The operating classes of (analog) transconductance PA are briefly described. In addition, digital operating classes are introduced and discussed, with a particular emphasis on digital class-C. Finally, the theoretical output power and drain efficiency of analog and digital operating classes are compared to highlight the potential of digital class-C for DTX applications.

In Chapter 3, the groundwork for the design of a CMOS driver for LDMOS-based RF-DACs is laid out. This chapter presents a concise discussion of key design considerations and covers the custom $V_T$ LDMOS technology used in the DTX. Additionally, the chapter outlines the design specifications and justifies them. A design for a CMOS driver is proposed and its implementation in thin-oxide bulk CMOS is described. The chapter concludes by detailing the performance results of the proposed design.

In Chapter 4, a short background for GaN technology for RF applications is provided. The chapter describes some key design considerations and states the necessary modifications applied to the proposed driver for LDMOS-based RF-DACs in anticipation of GaN-based RF-DACs.

Lastly, Chapter 5 draws relevant conclusions of work put forward in this thesis and states recommendations for future works.

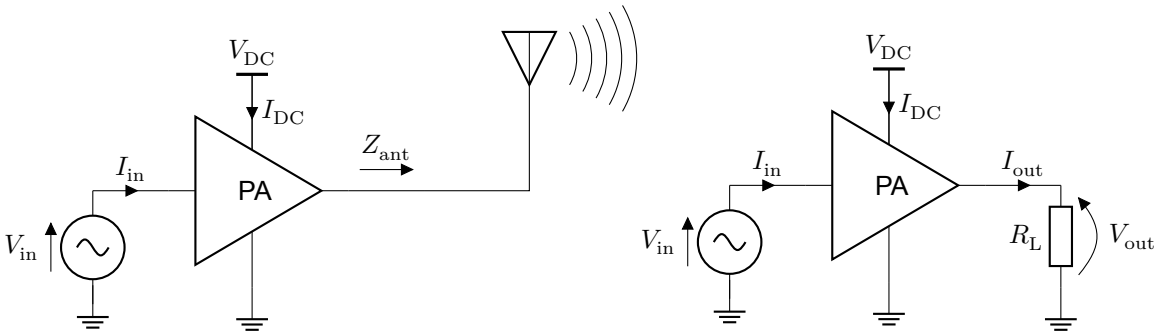
# 2

# Theory

Wireless communication is an essential part of daily life. In response to the continuously increasing demand for more connectivity, more massive multiple-input multiple-output (mMIMO) technologies are deployed. Subsequently, the global energy consumption and carbon emissions contributed by wireless communication technology are expected to increase substantially [2]. Therefore, the need for efficient transmitters is higher than ever before. This raises the question: how do radio frequency transmitters become energy-efficient?

## 2.1. Power Amplifier Basics

The most power-hungry building block in a radio frequency transceiver is the power amplifier (PA). The fundamentals of a PA are extensively explained in [16–19]. Nonetheless, it is worthwhile to recapitulate some fundamental concepts. More specifically, output power, power gain, efficiency, and linearity of a conceptual power amplifier as depicted in Fig. 2.1.




(a) (b)

Figure 2.1: A conceptual power amplifier.

### 2.1.1. Output Power

The output power of a power amplifier is defined as the power emanating from its output port and finally flowing toward the load (antenna). In general, the signals dealt with by a power amplifier are periodic. Therefore, the link between instantaneous output power Eq. (2.1) and average out power Eq. (2.2) is straightforward.

$$p_{\text{out}}(t) \triangleq v_{\text{out}}(t) \cdot i_{\text{out}}(t) \tag{2.1}$$

$$P_{\text{out}} = \frac{1}{T} \int_{-T/2}^{T/2} p_{\text{out}}(t) \mathrm{d}t \tag{2.2}$$

At radio frequency, however, the power of the fundamental component is of most interest. That is to say, only the power of a modulated bandpass signal around a certain carrier frequency ($f_c$) is desired. The fundamental average output power $P_1$ is defined in Eq. (2.3), where $V_1$ and $I_1$ are the first Fourier component of the voltage and current waveforms, respectively. If the signals are purely sinusoidal, the RMS values can be used to compute the fundamental average output power in Eq. (2.4).

$$P_1 = \frac{V_{\text{out},1}^2}{2R_\text{L}} = \frac{1}{2} I_{\text{out},1}^2 \cdot R_\text{L} \tag{2.3}$$

$$P_1 = \frac{V_{\text{out,RMS}}^2}{R_\text{L}} = I_{\text{out,RMS}}^2 \cdot R_\text{L} \tag{2.4}$$

### 2.1.2. Power Gain

Gain is essentially a dimensionless metric expressing a ratio of one quantity to another. In general, RF and microwave engineers refer to *a power gain*. This term can be ambiguous since at least four different power gain metrics can be measured [20]. All those gains are valuable but convey different information about what the power amplifier is doing [21]. Nonetheless, the most common power gain is the ratiometric power gain [22] expressed in Eq. (2.5).

$$G_P \triangleq 10 \log_{10} \left( \frac{P_\text{out}}{P_\text{in}} \right) \tag{2.5}$$

### 2.1.3. Linearity

A power amplifier's main job is to increase the power of its input signal before it is transmitted through a medium. The term linearity refers to how faithfully the input signal is reproduced by the PA. Multiple metrics are used to quantify linearity based on the actual application, i.e., the applied modulation and relevant regulatory specification [16].

The error vector magnitude (EVM) and the adjacent channel leakage ratio are commonly reported linearity metrics. EVM indicates the quality of a modulated signal and measures the deviation of a transmitted or received constellation point from its ideal location [23]. The adjacent channel leakage ratio (ACLR) or adjacent channel power ratio (ACPR) measures spectral purity. ACLR or ACPR is the ratio of the total power in the adjacent channel to the main channel's power.

Although EVM and ACLR are valuable linearity measures, they are cryptic by nature. That is, neither metric conveys information about the shortcomings of circuit implementation. The amplitude-to-amplitude (AM-to-AM) conversion and amplitude-to-phase (AM-to-PM) are more appropriate metrics in that respect. AM-to-AM conversion, or rather an AM-to-AM distortion, is explained by gain compression. More specifically, the change in the output signal amplitude is not linearly related to the change in the input signal amplitude. AM-to-PM conversion, or rather an AM-to-PM distortion, describes the fact that a change in input signal amplitude causes a change in the output signal phase. Just like AM-to-AM conversion, AM-to-PM is caused by a physical phenomenon. The occurrence of AM-to-PM conversion is related to signal clipping or nonlinear reactance [16], e.g., due to nonlinear output capacitance of an active device like an LDMOS transistor [24].

### 2.1.4. Efficiency

Energy efficiency is another performance metric for a power amplifier. Energy efficiency expresses the ratio of the useful power in the fundamental frequency band provided to the load/antenna and the power provided to the (amplifying) system. Amplifiers are evaluated for efficiency using a conservation of power calculation Eq. (2.6) [25]. Multiple efficiency definitions are found in literature and datasheets. These efficiencies include drain efficiency, total efficiency, and power-added efficiency, and are expressed in Eqs. (2.7) to (2.9), respectively.

$$P_\text{in} + P_\text{DC} + P_\text{out} + P_\text{dis} = 0 \tag{2.6}$$

$$\eta_\text{D} = \frac{P_\text{out}}{P_\text{DC}} \tag{2.7}$$

$$\eta_{\mathrm{T}} = \frac{P_{\mathrm{out}}}{P_{\mathrm{DC}} + P_{\mathrm{in}}} \tag{2.8}$$

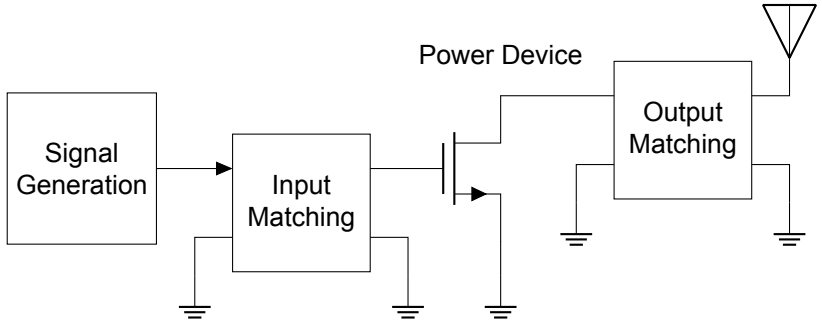
$$PAE = \frac{P_{\mathrm{out}} - P_{\mathrm{in}}}{P_{\mathrm{DC}}} \tag{2.9}$$

Which of these efficiency definitions is the most appropriate depends on the nature of the design (analog/digital) and the designer's interest. From an application point of view, it is perhaps most propitiate to focus on the total system efficiency Eq. (2.10). Unlike the other efficiency definitions; total system efficiency entails a full picture of a transmitter chain.

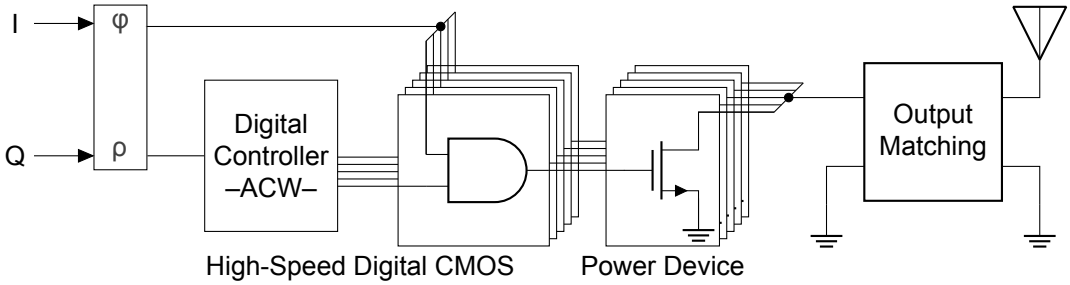
$$\eta_{\mathrm{T,system}} = \frac{P_{\mathrm{out}}}{P_{\mathrm{DC}} + \sum_{n=0}^{N} P_{\mathrm{DC},n} + P_{\mathrm{in}}} \tag{2.10}$$

## 2.2. Amplifier Classes Based on Analog and Digital Operation

Conventional radio frequency (RF) transmitter chains are analog-intensive and impose difficult linearity-efficiency trade-offs. An answer to the desired low-cost, highly-integrated, and energy-efficient mMIMO base stations lies in the fully-digital transmitter (DTX), i.e., bits-in and RF-out [14, 26, 27]. It is worthwhile to analyze the analog-intensive and the fully-digital architectures conceptually to understand their strengths and weaknesses. Although it is possible to implement both, a digital polar and a digital I/Q transmitter just like their analog counterparts [14], only the polar architecture is considered in this thesis.




(a) A conceptual analog-intensive transmitter.




(b) A conceptual polar fully digital transmitter.

Figure 2.2: A comparison between a conceptual polar analog-intensive and a fully digital transmitter.

To compare power amplifiers in terms of their output power and efficiency, it is insightful to analyze the Fourier decomposition of their drain voltage and current waveforms [16]. Provided these waveforms are periodic, they can be expressed in terms of Fourier series Eqs. (2.11) and (2.12). Moreover, only the transconductance classes and their digital equivalent are discussed.

$$f(t) = a_0 + \sum_{n=1}^{\infty} a_n \cos(n\omega t) + b_n \sin(n\omega t) \tag{2.11}$$

$$\begin{cases} a_0 = \frac{1}{T}\int_{-T/2}^{T/2} f(t)\mathrm{d}t \\ a_n = \frac{2}{T}\int_{-T/2}^{T/2} f(t)\cos(n\omega t)\mathrm{d}t \\ b_n = \frac{2}{T}\int_{-T/2}^{T/2} f(t)\sin(n\omega t)\mathrm{d}t \end{cases} \tag{2.12}$$

### 2.2.1. Analog Amplifier Operation

Analog transmitter architectures are extensively explained in [1, 18, 19]. An analog transmitter essentially utilizes a PA to increase the power level of an RF signal. An abstraction of a conceptual analog transmitter is shown in Fig. 2.2a where the power amplifier is represented by a single common source (CS) transistor. The rest of the transmitter chain is represented by a functional block labeled as *Signal Generation*. Moreover, all implementation details, e.g., biasing and DC-feed are ignored.

Traditionally, the concept of the conduction angle ($\alpha$) is introduced to compare different analog power amplifier classes [16, 17]. This concept is illustrated in Fig. 2.3. The different amplifier classes are defined in Table 2.1. The conduction angle describes the portion of one RF cycle during which the PA is conducting current. Thinking of an RF cycle in terms of a unit circle helps express the conduction angle in radians or degrees.

Expressions for the output power and drain efficiency are derived using Eqs. (2.13) and (2.14), where the maximum normalized drain voltage is 2 and the maximum normalized drain current is 1, just like in [16]. It is worth noting that the conduction angle links the amplitude of the drain current ($I_{\mathrm{DS}}$), the quiescent current ($I_{\mathrm{Q}}$), and the maximum drain current ($I_{\mathrm{max}}$). Eqs. (2.16) and (2.19) express the RF output power and drain efficiency as derived in [16].

$$v_{\mathrm{DS}}(t) = 1 + \cos(\omega t) \tag{2.13}$$

$$i_{\mathrm{DS}}(t) = \begin{cases} \dfrac{(\cos(\omega t) - \cos(\alpha/2))}{1 - \cos(\alpha/2)}, & \text{if } -\alpha/2 \leq (\omega t \triangleq \theta) \leq \alpha/2. \\ 0, & \text{otherwise.} \end{cases} \tag{2.14}$$

$$I_{\mathrm{DC}} = I_0 = \frac{1}{2\pi}\int_{-\alpha/2}^{\alpha/2} i_{\mathrm{DS}}(\theta)\mathrm{d}\theta = \frac{1}{2\pi}\frac{2\sin(\alpha/2) - \alpha\cos(\alpha/2)}{1 - \cos(\alpha/2)} \tag{2.15}$$

$$I_{\mathrm{fund.}} = I_1 = \frac{2}{2\pi}\int_{-\alpha/2}^{\alpha/2} i_{\mathrm{DS}}(\theta)\cos(\theta)\mathrm{d}\theta = \frac{1}{2\pi}\frac{\alpha - \sin(\alpha)}{1 - \cos(\alpha/2)} \tag{2.16}$$

$$P_{\mathrm{DC}} = P_0 = V_0 \cdot I_0^* = \frac{1}{2\pi}\frac{2\sin(\alpha/2) - \alpha\cos(\alpha/2)}{1 - \cos(\alpha/2)} \tag{2.17}$$

$$P_{\mathrm{fund.}} = P_1 = \frac{1}{2}V_1 \cdot I_1^* = \frac{1}{2\pi}\frac{\alpha - \sin(\alpha)}{1 - \cos(\alpha/2)} \tag{2.18}$$

$$\eta_D = \frac{P_{\mathrm{fund.}}}{P_{\mathrm{DC}}} = \frac{1}{2}\frac{\alpha - \sin(\alpha)}{2\sin(\alpha/2) - \alpha\cos(\alpha/2)} \tag{2.19}$$

Table 2.1: Conventional PA class definitions vs. conduction angle.

| Class | Conduction angle | Normalized quiescent current |
|---|---|---|
| A | 2π | 0.5 |
| AB | π < $\alpha$ < 2π | 0 < $I_{\mathrm{Q}}$ < 0.5 |
| B | π | 0 |
| C | 0 < $\alpha$ < π | 0 |

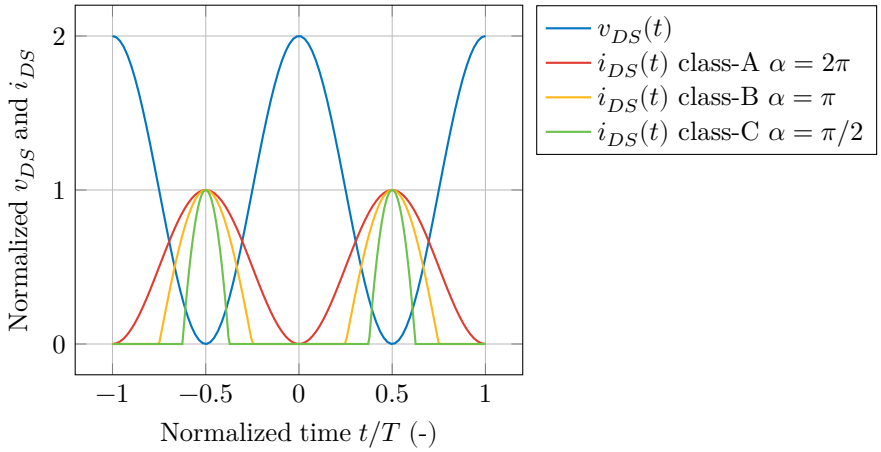



Figure 2.3: Normalized drain voltage and current (time scale is shifted to simplify calculations).

### 2.2.2. Digital Amplifier Operation

Digital transmitter architectures are described in more detail in [9, 13, 14]. In a digital polar transmitter as proposed in [26], two parts can be distinguished: (1) a high-speed digital CMOS controller die, and (2) a segmented power die (e.g. LDMOS or GaN). The baseband in-phase and quadrature-phase (I/Q) data is converted into an amplitude code word (ACW) and a digital representation of its phase, which are used to modulate an RF carrier [28].

The gate-segments of the LDMOS/GaN are individually controlled by the ACW and are either “fully off” or “fully on” [15]. This implies a class-E operation which is seemingly the most natural option [28]. Although class-E can be very efficient, it has also serious drawbacks. Its operating frequency and output power are very constrained. In addition, it enforces stringent requirements on the driver(s) and the digital pre-distortion techniques (DPD). Instead of switching the LDMOS/GaN segments either “fully off” or “fully on”, the segments can be also kept in their saturation region or current limited regime. When assuming ideal current-mode DTX operation, the LDMOS/GaN segments produce square-wave currents. The sum of these unit currents is proportional to the ACW. The PA’s drain voltage and current waveform can be used to gain an understanding of their operation mode. To compare the various digital amplifier classes with their analog counterparts, the duty cycle can be used as a substitute for the conduction angle [28]. Table 2.2 provides the definition of the digital classes A to C in terms of the duty cycle. The conduction angle and duty cycle are related according to Eq. (2.20) as can be deduced from Table 2.2.

Table 2.2: Digital PA operation class defined in terms of duty cycle.

| Class | Duty cycle | Corresponding analog conduction angle |
|---|---|---|
| A | 100% | 2π |
| AB | 50% < $d$ < 100% | π < $\alpha$ < 2π |
| B | 50% | π |
| C | 0% < $d$ < 50% | 0 < $\alpha$ < π |

$$d = \alpha/2\pi \tag{2.20}$$

A mathematical expression of the drain voltage and current is provided in Eqs. (2.21) and (2.22). These equations not only help to express the instantaneous voltage and current, but are also useful to derive expressions for RF output power and drain efficiency. Fig. 2.4 is used to visualize the normalized drain voltage and current waveforms of the digital class-C amplifier. The Fourier components of the current waveform are derived in Eqs. (2.23) and (2.24). Subsequently, the RF output power and the drain efficiency are derived in Eqs. (2.26) and (2.27).

$$v_{\mathrm{DS}}(t) = 1 + \cos(\omega t) \tag{2.21}$$

$$i_{\mathrm{DS}}(t) = \begin{cases} 1, & \text{if } (n-d)\,T/2 \leq t \leq (n+d)\,T/2 \quad \{n \in \mathbb{Z} | n \neq 0\}. \\ 0, & \text{otherwise.} \end{cases} \tag{2.22}$$

$$I_{\mathrm{DC}} = I_0 = \frac{1}{T}\int_{-T/2}^{T/2} i_{\mathrm{DS}}(t)\mathrm{d}t = \frac{1}{T}\int_{-dT/2}^{dT/2} 1 \cdot \mathrm{d}t = d \tag{2.23}$$

$$I_{\mathrm{fund.}} = I_1 = \frac{2}{T}\int_{-T/2}^{T/2} i_{\mathrm{DS}}(t)\cos(\omega t)\mathrm{d}t = \frac{2}{T}\int_{-dT/2}^{dT/2} \cos(\omega t) \cdot \mathrm{d}t = \frac{2}{\pi}\sin(\pi d) \tag{2.24}$$

$$P_{\mathrm{DC}} = P_0 = V_0 \cdot I_0^* = 1 \cdot d = d \tag{2.25}$$

$$P_{\mathrm{fund.}} = P_1 = \frac{1}{2}V_1 \cdot I_1^* = \frac{1}{2} \cdot 1 \cdot \frac{2}{\pi}\sin(\pi d) = \frac{1}{\pi}\sin(\pi d) \tag{2.26}$$

$$\eta_{\mathrm{D}} = \frac{P_{\mathrm{fund.}}}{P_{\mathrm{DC}}} = \frac{\sin(\pi d)}{\pi d} \tag{2.27}$$

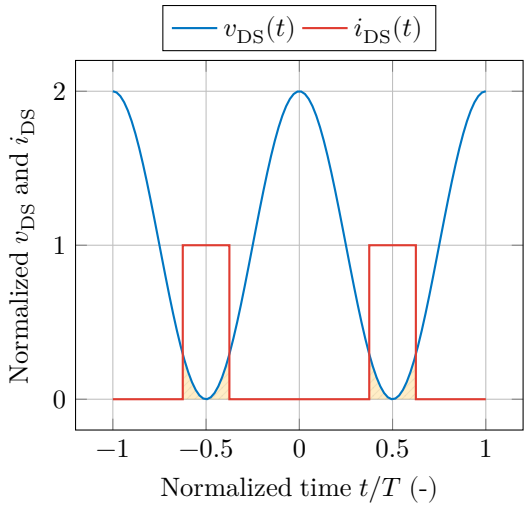


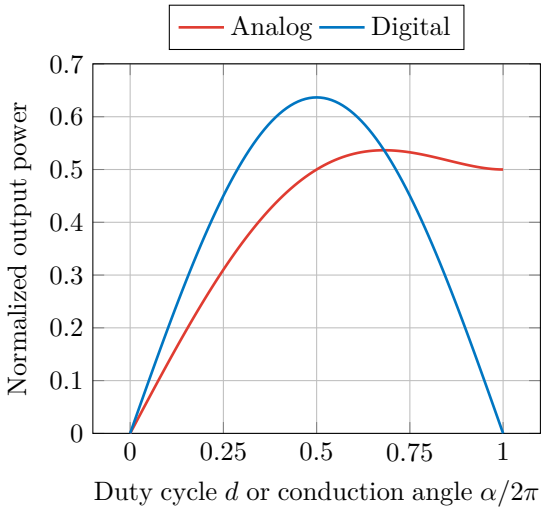

Figure 2.4: Normalized drain voltage and current waveforms (rectangular).

### 2.2.3. Comparison between the Analog and Digital Operation

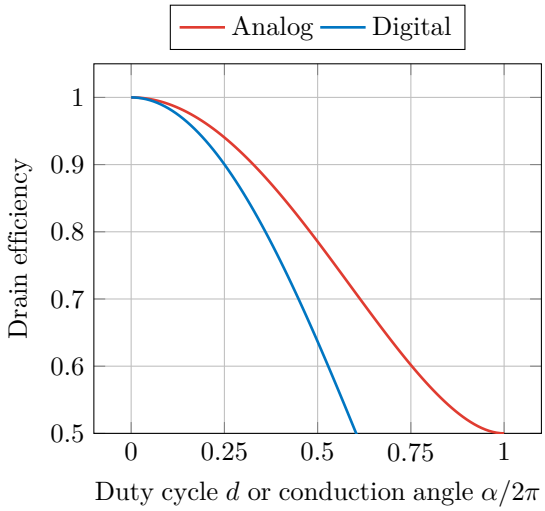
The analog transconductance amplifier classes are analyzed in terms of their theoretical output power and drain efficiency using Fourier decomposition in Section 2.2.1. The same is done for their digital counterparts in Section 2.2.2. In order to compare the amplifier classes, it is worth looking at three different plots in Fig. 2.5. The first two figures (Figs. 2.5a and 2.5b) show that the digital class-C has significant potential. That is to say, for the same output power higher, efficiency is achieved as shown in Fig. 2.5c.

Although the analog and digital amplifier classes show some similarities, they are fundamentally distinct. Notably, taking a closer look at Figs. 2.5a and 2.5b along with Table 2.2 and Eq. (2.20) reveals the differences. To be more specific, given a certain duty cycle, the digital class does not have the same output power nor the drain efficiency as the corresponding analog conduction angle. Furthermore, the benefits of digital amplifier classes seize to exist at a duty cycle of nearly 60%.

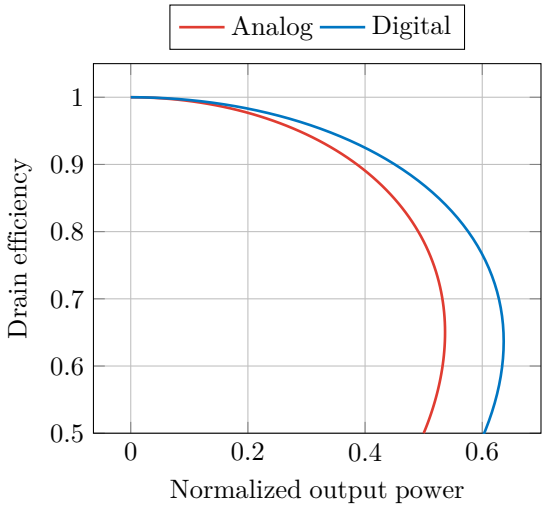
Digital class-C is an excellent substitute for switch-mode amplifier classes exploited in fully-digital transmitters, such as class-E. Fully-digital transmitters, like conventional transmitter line-ups, can benefit from efficiency enhancement techniques, such as Doherty [29]. Their digital nature allows for more accurate control of the Doherty branches, resulting in improved efficiencies.




(a) Normalized output power vs. duty cycle.




(b) Drain efficiency vs. duty cycle.




(c) Drain efficiency vs. normalized output power.

Figure 2.5: Normalized output power and drain vs. duty cycle/normalized conduction angle.

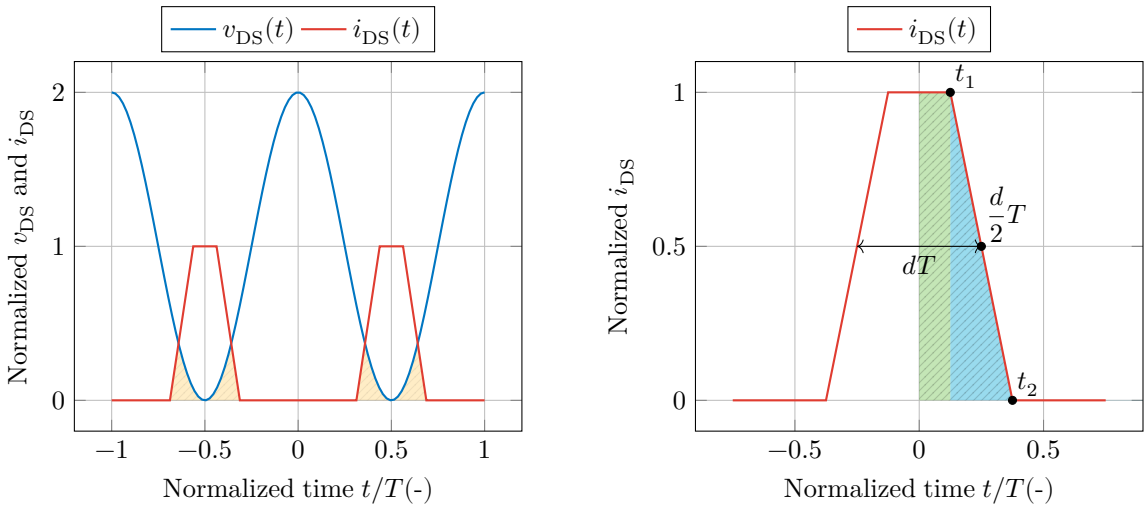
### 2.2.4. Practical Digital Amplifier Operation

The analysis of digital amplifier classes in Section 2.2.2 assumes perfect rectangular currents. This assumption simplifies analysis and serves to gain insight. However, the rise and fall times are never equal to zero. To make the analysis more realistic, the waveforms are assumed to have a trapezoidal shape instead of a rectangular one. It is worth noting that trapezoidal waveforms are still ideal waveforms. This assumption allows for the impact of the rise and fall times on output power and drain efficiency to be accounted for. An example of a trapezoidal current waveform is illustrated in Fig. 2.6a.

The rise and fall times of a trapezoidal waveform are not necessarily equal. However, for the purpose of analysis, the rise and fall times are assumed to be equal. For the sake of simplicity, a trapezoidal pulse as illustrated in Fig. 2.6b is considered. The pulse is expressed in Eqs. (2.28) and (2.29). The symmetry of the pulse comes with one more advantage. Particularly, it can split into two parts, each consisting of a rectangular and a triangular part. The fundamental component of this pulse is calculated using the integration limits identified in Fig. 2.6b. The results are expressed in Eqs. (2.31) to (2.32).

$$i_{\mathrm{DS}}(t) = \begin{cases} 1, & \text{if } -(dT - t_{\mathrm{r}})/2 \leq t \leq (dT - t_{\mathrm{r}})/2. \\ a + bt, & \text{if } -(dT + t_{\mathrm{r}})/2 < t < -(dT - t_{\mathrm{r}})/2 \text{ and } (dT - t_{\mathrm{r}})/2 < t < (dT + t_{\mathrm{r}})/2. \\ 0, & \text{otherwise.} \end{cases} \tag{2.28}$$

$$\begin{cases} t_1 = (dT - t_\mathrm{r})/2 \\ t_2 = (dT + t_\mathrm{r})/2 \\ a = (1 + dT/t_\mathrm{r})/2 \\ b = 1/t_\mathrm{r}, & \text{if } -(dT - t_\mathrm{r})/2 < t < -(dT + t_\mathrm{r})/2. \\ b = -1/t_\mathrm{r}, & \text{if } (dT - t_\mathrm{r})/2 < t < (dT + t_\mathrm{r})/2. \end{cases} \tag{2.29}$$




(a) Normalized drain voltage and current.

(b) Normalized current pulse annotated.

Figure 2.6: Normalized drain voltage and current waveforms (trapezoidal).

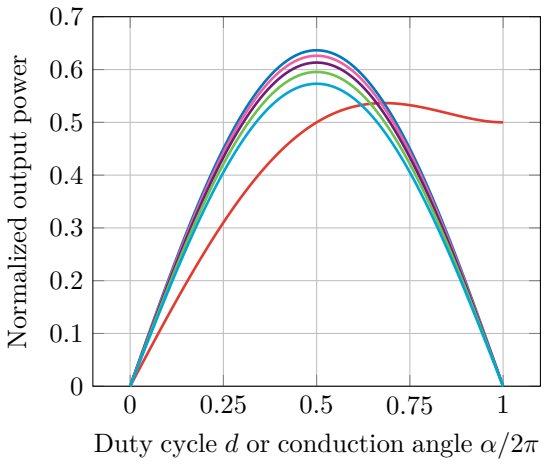
$$I_\mathrm{tri.} = 2 \cdot \frac{2}{T} \int_{t_1}^{t_2} i_\mathrm{DS}(t) \cos(\omega t) \mathrm{d}t = \frac{2}{\pi} \left[ a \sin(\omega t) + bt \sin(\omega t) + \frac{b}{\omega} \cos(\omega t) \right]_{t=t_1}^{t=t_2} \tag{2.30}$$

$$I_\mathrm{rect.} = 2 \cdot \frac{2}{T} \int_{0}^{t_1} i_\mathrm{DS}(t) \cos(\omega t) \mathrm{d}t = \frac{2}{\pi} \sin\left( \pi \left( dT - \frac{t_\mathrm{r}}{T} \right) \right) \tag{2.31}$$

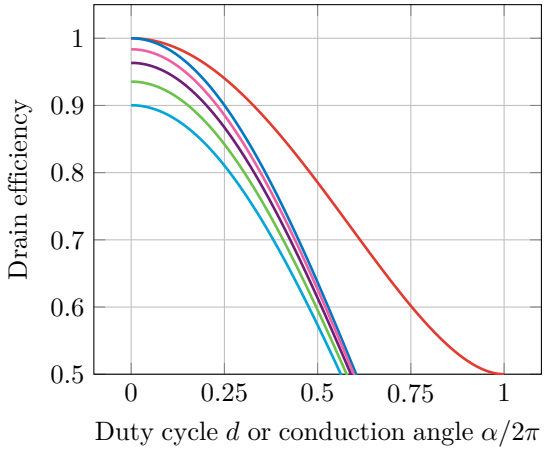
$$I_\mathrm{fund.} = I_\mathrm{rect.} + I_\mathrm{tri.} \tag{2.32}$$

The duty cycle is defined at the 50% marks as depicted in Fig. 2.6b. From a certain point of view, the point $dT/2$ remains fixed, the slope of the pulse reduces and the points $t_1$ and $t_2$ get pushed further apart. Hence, resulting in a longer rise/fall time. The overlap between the drain voltage and the drain current increases as shown Fig. 2.6a (cf. Fig. 2.4). This is indicative of a drop in drain efficiency. The DC component remains constant as the rise/fall time increases, whereas the fundamental component decreases. As a result, both the output power and the drain efficiency decrease as the rise and fall times increase. This is confirmed by Fig. 2.7a. This figure also compares the analog classes with their digital counterparts corresponding to a selected set of rise/fall times ($0.10T$, $0.15T$, $0.20T$, and $0.25T$).

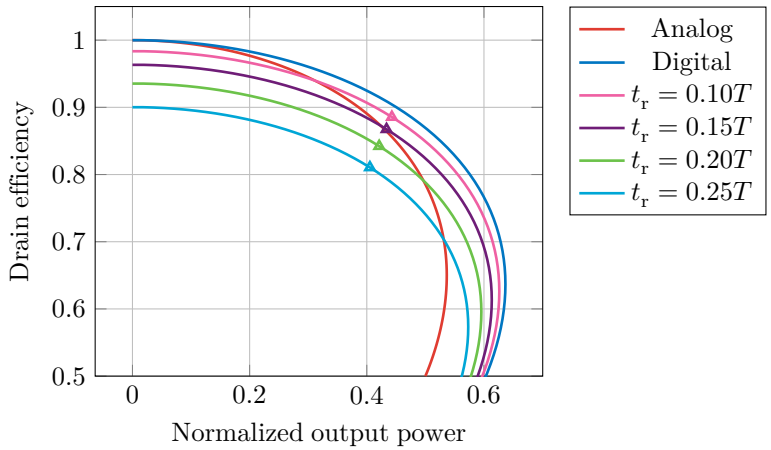
This analysis is shortsighted. It only concerns the output power and drain efficiency. These two aspects do not entail the full picture. Demanding (extremely) short rise and fall times puts strain on the preceding stage of the PDA. Especially as the operating frequency increases. The power consumption of the DPA's driver increases, and as result, the system efficiency deteriorates. The implications of short rise/fall time for system efficiency are addressed in more detail in Chapter 3.




(a) Normalized output power vs. duty cycle.




(b) Drain efficiency vs. duty cycle.




(c) Drain efficiency vs. normalized output power (markers indicate $d$ = 25%).

Figure 2.7: Normalized output power and drain efficiency vs. duty cycle/normalized conduction angle.

# 3

# Driver for LDMOS-Based RF-DACs

A fully-digital transmitter (DTX) offers high system integration and energy efficiency. The DTX line-up comprises a CMOS controller and a custom $V_T$-shifted LDMOS/GaN output stage [27]. This particular implementation of DTX is also known as a power digital-to-analog converter or RF-DAC. The main advantage of a DTX is that it utilizes both the high speed and high scalability of digital CMOS and the high power of LDMOS/GaN. The realization of such a DTX does not come without challenges though. Besides the development of custom $V_T$-shifted LDMOS/GaN, the design of a CMOS controller can also be challenging. Driving large capacitive loads at radio frequency (RF) with high voltage swings, short rise/fall time and low power consumption involves conflicting requirements. A CMOS driver for such a DTX line-up targeted at sub-6 GHz application is proposed here. Moreover, some design aspects affecting the system performance of such a driver are highlighted.

## 3.1. Design Considerations

Digital power amplifiers have great potential in fully-digital amplifiers, especially when operating in digital class-C. A DPA operating digital class-C is capable of producing 21% higher output power compared to the analog class-B operation [29]. Design trade-offs concerning RF output power and drain efficiency of theoretical digital power amplifier (DPA) are identified and highlighted in Fig. 2.7c. To account for non-zero rise/fall times or transition time, the DPA's rectangular current waveform is substituted by a trapezoidal one. The Fourier decomposition of the latter proves that the non-zero rise/fall time reduces the fundamental component and negatively affects the output power and drain efficiency. A somewhat realistic waveform illustrated in Fig. 3.1, unlike a trapezoidal one, assumes smooth transitions, resulting in a more severe drop in output power and drain efficiency.

In reality, pulses are not necessarily symmetrical. Besides, they (can) exhibit overshooting, undershooting, and ringing/ripple effects. All these imperfections generally deteriorate the performance of a DPA. To verify the curves from Section 2.2.4, the ideal DPA is substituted by a realistic model of $V_T$-shifted LDMOS in a simulation setup. The output power and drain efficiency curves are normalized and plotted alongside those resulting from the ideal DPA in Fig. 3.2. It should be noted that the LDMOS device is operated at a frequency of 3.5 GHz. The equations for an ideal DPA operating in digital class-C are derived in Section 2.2.2 and repeated here for convenience. The output power from the simulation is normalized similarly to [28] to allow for comparison against the ideal rectangular and trapezoid case. The purpose of these simulations is to find a reasonable trade-off between the output power and the drain efficiency. Additionally, the impact of the rise/fall time is accentuated at a duty cycle of 25% or lower as shown in Fig. 3.2b.

$$P_{\text{fund.}} = P_1 = \frac{\sin(\pi d)}{\pi} \tag{3.1}$$

$$\eta_{\text{D}} = \frac{\sin(\pi d)}{\pi d} \tag{3.2}$$

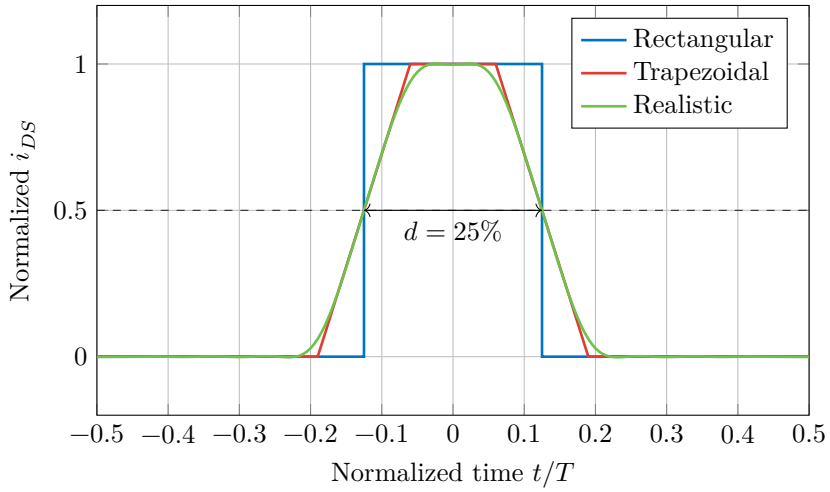
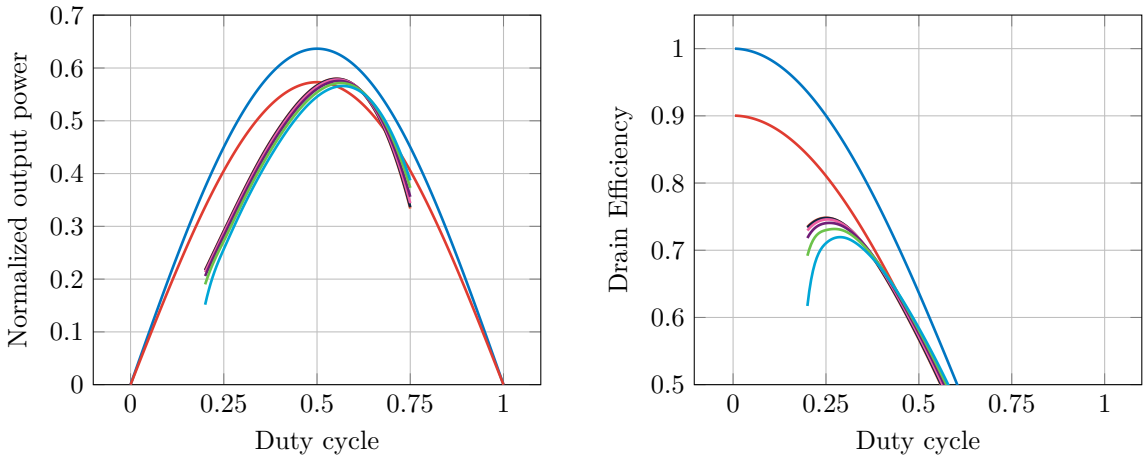
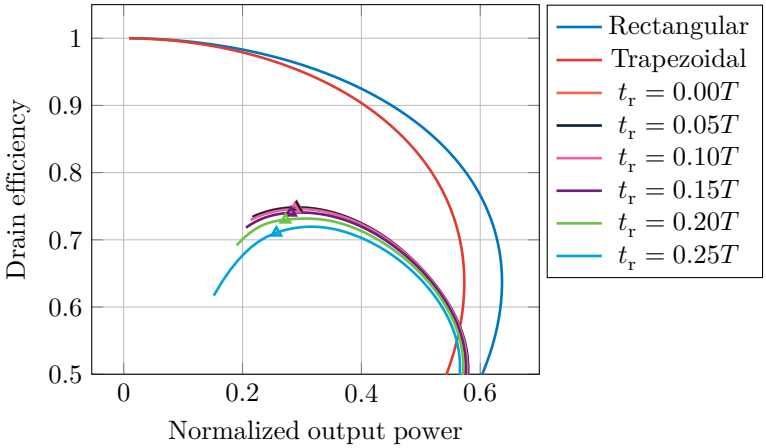



Figure 3.1: Normalized current pulses of an ideal DPA.




(a) Normalized output power vs. duty cycle.

(b) Drain efficiency vs. duty cycle.




(c) Drain efficiency vs. normalized output power.

Figure 3.2: Normalized output power and drain vs. duty cycle (markers indicate $d$ = 25%).

While short transitions benefit output power and drain efficiency, they require drivers to dissipate more power [26, 30]. The drain and system efficiency are computed using Eqs. (3.3) and (3.4).[1] Demanding rise and fall time in the range of 0.10 to 0.20 of the RF cycle takes a huge toll on system efficiency as the operating frequency increases due to switching losses $\propto fCV^2$ [31]. Besides, the expected "square-wave" operation would not be possible [31].

$$\eta_{\mathrm{D}} = \frac{P_1}{P_{\mathrm{DC}}} \tag{3.3}$$

$$\eta_{\mathrm{S}} = \frac{P_1}{P_{\mathrm{DC}} + P_{\mathrm{driver}}} \tag{3.4}$$

To understand the fundamental limit to the "square-wave" operation, an inverter is used as a proxy for a generic class-D driver. Its speed is inherently limited by the CMOS technology used to implement it. The oscillation frequency ($f_{\mathrm{osc}}$) of the inverter-based ring oscillator is generally a good indication of the achievable speed. The operating frequency is usually 50 to 100 times smaller than $f_{\mathrm{osc}}$ in Eq. (3.5) [32]. Another metric of the maximum achievable speed of a certain device in a certain technology is the transit frequency ($\omega_{\mathrm{T}}$). Since the output maximum slew rate is determined by the drain current and the load capacitance [33], Eq. (3.6) can be used to link $\tau_{\mathrm{p}} = 1/(2Nf_{\mathrm{osc}})$ and $\omega_{\mathrm{T}} = g_{\mathrm{m}}/C_{\mathrm{gg}}$.

$$f_{\mathrm{osc}} = \frac{1}{2N\tau_{\mathrm{p}}} \tag{3.5}$$

$$I_{\mathrm{D}} = C_{\mathrm{L}} \left| \frac{\mathrm{d}v_{\mathrm{out}}}{\mathrm{d}t} \right|_{\mathrm{max}} \tag{3.6}$$

The derivation of Eq. (3.8) makes the following assumptions:

1. $\mathrm{d}v_{\mathrm{out}}/\mathrm{d}t \rightarrow (V_{\mathrm{DD}}/2)/\tau_{\mathrm{p}}$.
2. $V_{\mathrm{th,n}} = V_{\mathrm{th,p}}$.
3. $\beta = \mu_{\mathrm{p}}/\mu_{\mathrm{n}}$ (typically set to 2).
4. $C_{\mathrm{out}} = \gamma C_{\mathrm{in}}$ where $C_{\mathrm{in}} = C_{\mathrm{gg,n}} + C_{\mathrm{gg,p}}$.
5. $C_{\mathrm{L}}$ is the sum of $C_{\mathrm{out}}$ of current stage and $C_{\mathrm{in}}$ of subsequent stage.
6. The high-to-low and low-to-high transitions are identical.
7. Both the NMOS and PMOS are in saturation at $V_{\mathrm{in}} = V_{\mathrm{out}} = V_{\mathrm{DD}}/2$.

$$\tau_{\mathrm{p}} \approx \frac{(1+\gamma)(1+\beta)C_{\mathrm{gg,n}} \cdot \frac{1}{2}V_{\mathrm{DD}}}{\frac{1}{2}g_{\mathrm{m}}(V_{\mathrm{DD}}/2 - V_{\mathrm{th}})} \tag{3.7}$$

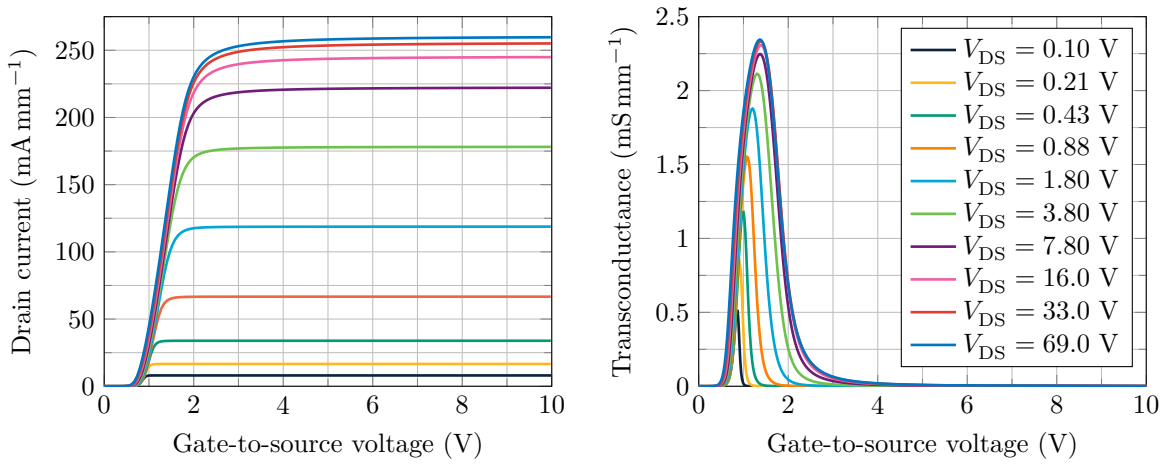
$$\tau_{\mathrm{p}} \approx \frac{(1+\gamma)(1+\beta)V_{\mathrm{DD}}}{\omega_{\mathrm{T}}(V_{\mathrm{DD}}/2 - V_{\mathrm{th}})} \tag{3.8}$$

It should be noted that Eq. (3.8) is by no means an accurate estimation of the propagation delay of an inverter-based ring oscillator. The equation provides insight into the achievable speed depending on the technology node and the device type. For certain supply and load, a fast driver is accomplished by maximizing its $\mathrm{d}v_{\mathrm{out}}/\mathrm{d}t$. This boils down to the fact that short rise and fall times are achieved by increasing the current flowing through the pull-up and pull-down networks of the driver. In other words, the driver is oversized at the expense of increased power dissipation. Typically low $V_{\mathrm{th}}$ (LVT) bulk-CMOS or SOI is chosen for high speed.

## 3.2. Custom $V_T$ LDMOS Technology

The LDMOS technology used to implement the DTX is developed by Ampleon and optimized for RF-DAC applications. Its threshold voltage is shifted down towards 0.7 V to relax its $V_{\mathrm{GS}}$ swing requirements. The gate-segmented LDMOS can be driven by 2.2 V swing and has $C_{\mathrm{GS}}$ of 1.9 pF mm$^{-1}$ at 2.2 V. The DC characteristics of this technology are shown in Fig. 3.3.

[1] Eqs. (3.3) and (3.4) are adopted from [26] and $P_{\mathrm{RFout}} = P_1$, $P_{\mathrm{LD}} = P_{\mathrm{DC}}$, and , and $P_{\mathrm{Ch}} = P_{\mathrm{driver}}$.




(a) (b)

Figure 3.3: DC $I_{DS}$-$V_{GS}$ and $g_m$-$V_{GS}$ curves of the custom $V_T$ LDMOS.

## 3.3. Driver Topology

In a polar DTX, the DPA comprises an array of sub-power amplifier cells [34]. The IQ baseband data is converted to an Amplitude Code Word (ACW) and its digital phase representation [28], which are bit-wise mixed through logic gates [26]. For base station applications, the DPA is a segmented high-power output stage driven by a CMOS chip. A CMOS driver provides a high-speed interface between a digital CMOS IC and an LDMOS die.

The maximum achievable current density of LDMOS is somewhat limited by the lower voltage swing from the CMOS driver [15]. A $V_T$-shift can be applied to the LDMOS to achieve the desired current density with lower swings. Provided that $V_T$-shift lowers $V_T$ to 0.7 V, it is possible to implement a CMOS driver in 40 nm bulk CMOS. The driver produces an output voltage that swings between the ground rail and $2V_{DD} = 2.2$ V with reasonably short transitions. It comprises a level shifter, two tapered inverter chains, and a high-voltage output buffer as illustrated in Fig. 3.4. The driver is explained by discussing each block, starting with the high-voltage output buffer in Section 3.5. The level shifter and the tapered inverter chains are discussed in Sections 3.6 and 3.7.

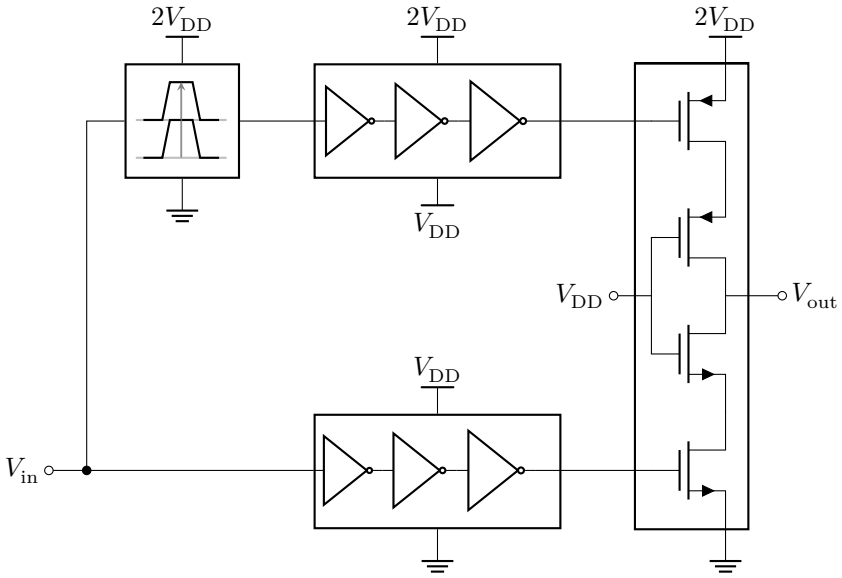



Figure 3.4: Topology of the proposed CMOS driver.

## 3.4. Design Specifications

An LDMOS-based RF-DAC has three to four LDMOS banks, each with 512 elements. A CMOS driver activates each of these elements individually. When an element is activated/deactivated, the driver charges/discharges its gate-to-source capacitance ($C_{GS}$) at 3.5 GHz. The target value for $C_{GS}$ is 150 fF. The driver's 25% duty cycle pulses should have sharp edges. According to Fig. 3.2 the rise and fall times ($t_r$ and $t_f$) should be around 20% of the RF period to achieve a drain efficiency of 74%. The LDMOS segment is on and off for 25% and 75% of an RF cycle, respectively. As a result, $t_f > t_r$ is allowed. Simply put, there is more time for the LDMOS segment to turn off before the next RF cycle begins. The fall time can be 30% of the RF cycle. At 3.5 GHz these percentages of the RF cycle yield: $t_r \leq 57$ ps and $t_f \leq 86$ ps. The 10%-90% definition common to VLSI design is used to define $t_r$ and $t_f$.

In VLSI design, the percentage of the clock period where clock signals cross 50% is defined as the duty cycle. The effective duty cycle ($d^*$) at the LDMOS drain is reduced if the output signal of the driver is assumed to have the same definition. When its gate-to-source voltage is lower than $V_T$ (and ignoring leakage currents), the LDMOS is effectively turned off. Therefore to achieve the needed duty cycle at the level midway between 0.7 V and 2.2 V (i.e., halfway between $V_T$ and $2V_{DD}$) the driver must adjust the duty cycle as illustrated in Fig. 3.5.

The drain efficiency following from Fig. 3.2c lies around 73%, provided the LDMOS is activated by realistic waveforms with $t_r = 0.2T$. Assuming that one bank has an RF output power of 20 W and a system efficiency ≥65%, it is reasonable to allocate 3.37 W for the CMOS drivers based on [26]. Therefore, a single driver switching a load of 150 fF at 3.5 GHz can dissipate up to 6.59 mW. Finally, the flip-chip bonding of the CMOS controller IC on top of the LDMOS die requires the driver to fit inside a square of ≤40 µm × 40 µm. The design specifications are summarized in Table 3.1.

Table 3.1: Design specifications of a CMOS driver for an LDMOS-based RF-DAC.

| Frequency | Power | Area | Rise/fall time | Voltage swing | Load capacitance |
|---|---|---|---|---|---|
| 3.5 GHz | ≤6.59 mW | ≤40 µm × 40 µm | ≤57 ps/≤86 ps | 2.2 V | 150 fF |

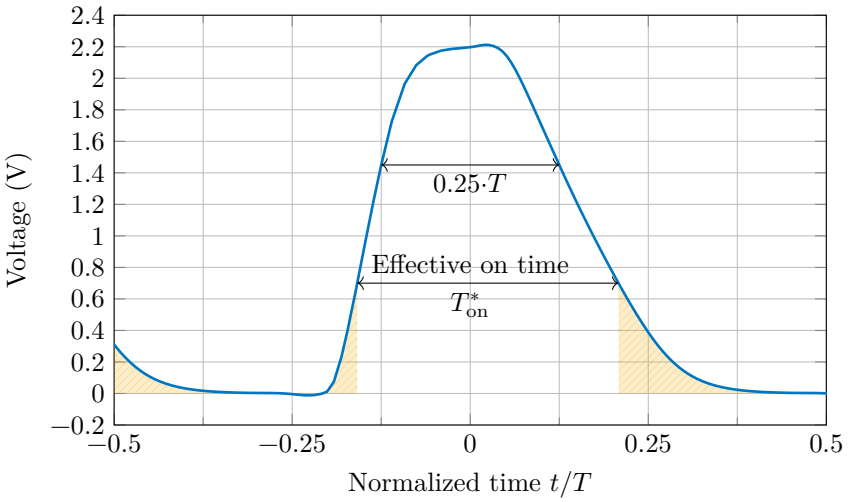


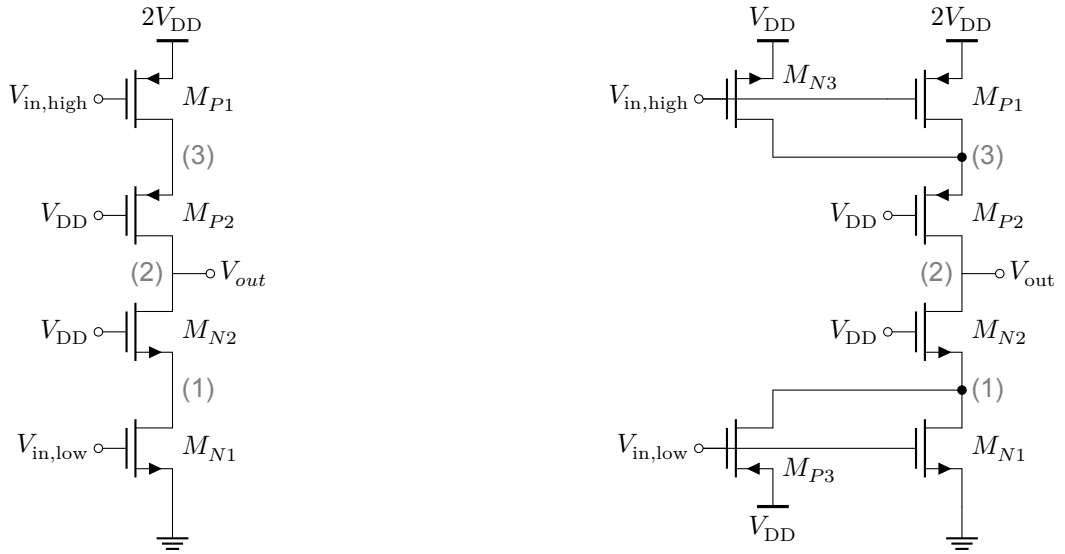

Figure 3.5: Driver's output voltage annotated with relevant definitions.

## 3.5. High-Voltage Output Buffer

The high-voltage output buffer is essentially a large inverter that produces signal swings of $2V_{DD} = 2.2$ V. A simple high-voltage output buffer is shown in Fig. 3.6a [35–37]. The cascodes $M_{N2}$ and $M_{P2}$ are added to alleviate voltage stress across $M_{N1}$ and $M_{P1}$, ensuring that their gate-to-drain ($V_{GD}$) and gate-to-source ($V_{GS}$) voltages do not exceed $1 \times |V_{DD}|$. The gate bias of both $M_{N2}$ and $M_{P2}$ is set at $V_{DD}$.

The devices $M_{N1}$ and $M_{P1}$, in turn, are driven by the signal $V_{in,low}$ and $V_{in,high}$ whose swing is $V_{DD}$. The signal $V_{in,high}$ drives the top side of the high-voltage output buffer and is a level-shifted version of $V_{in,low}$. Put differently, $V_{in,high}$ is a copy of $V_{in,low}$ whose DC-offset is increased by $V_{DD}$.

The high-voltage output buffer in Fig. 3.6a, however, suffers from large transient drain-to-source voltages $V_{DS}$ across the cascode devices, because nodes (1) and (3) are slow to switch. In fact, the source voltages of $M_{N2}$ and $M_{P2}$ settle to $V_{DD} - V_{th,n}$ and $V_{DD} + V_{th,p}$, respectively. This issue has been tackled previously by using thick-oxide devices for $M_{N2}$ and $M_{P2}$ [38]. To help the nodes (1) and (3) settle to $V_{DD}$ instead, devices $M_{P3}$ and $M_{N3}$ are added to the high-voltage output buffer, resulting in the modified structure shown in Fig. 3.6b. This structure comprises solely thin-oxide devices and is referred to as a *House-of-Cards* or HoC in [39]. Since the load capacitance of the driver is either charged by the $M_{P1}$–$M_{P2}$ stack or discharged by the $M_{N1}$–$M_{N2}$ stack, $M_{P3}$ and $M_{N3}$ can be minimum size [39]. Consequently, the increase in capacitance at the inputs of the output buffer is minimized.




(a) A simple high-voltage output buffer.

(b) A modified high-voltage output buffer.

Figure 3.6: A high speed high-voltage output buffer with a swing of $2V_{DD}$.

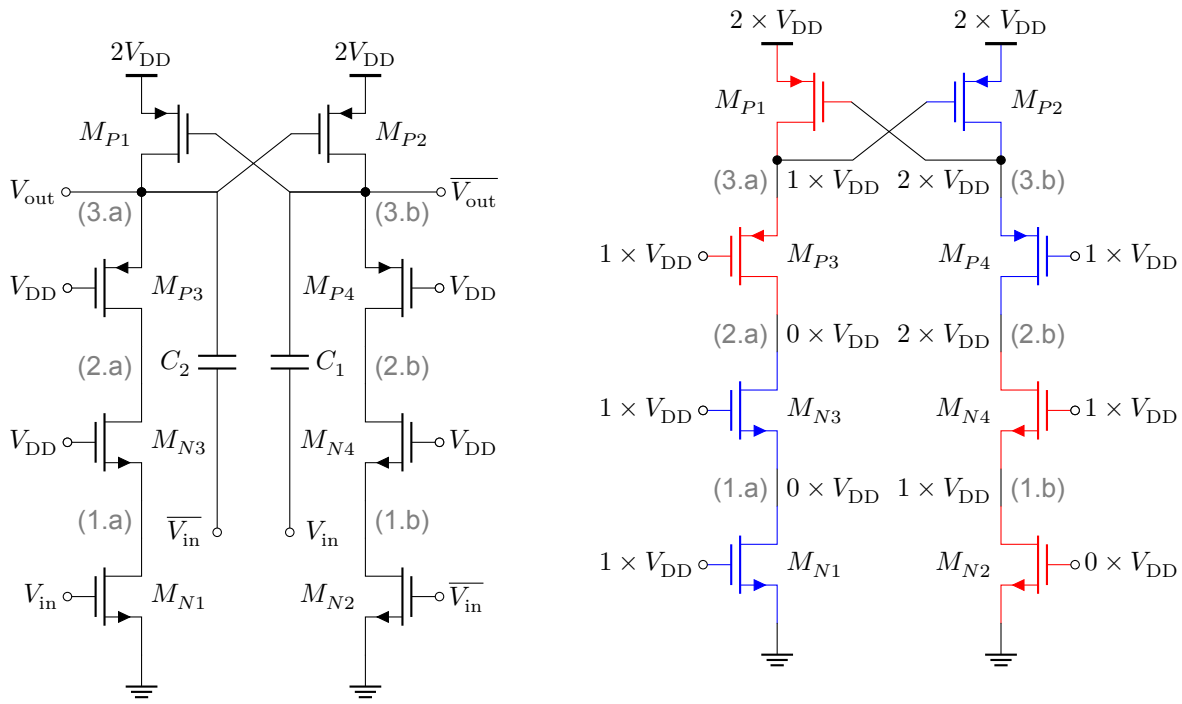
## 3.6. Level Shifter

To drive the PMOS side of the output buffer, i.e., $M_{P1}$, a level shifter is needed. A level shifter capable of operating at frequencies near 6 GHz is shown in Fig. 3.7a. The level shifter requires two complementary input signals, $V_{in}$ and $\overline{V_{in}}$, whose swing is $V_{DD}$. Complementary output signals switching between $V_{DD}$ and $2V_{DD}$ are generated at node (3.a) and (3.b) by taking advantage of the cross-coupling of $M_{P1}$ and $M_{P2}$ as illustrated in Fig. 3.7b. To improve the speed of the level shifter, the input is capacitively coupled to the gate of $M_{P1}$ and $M_{P2}$ using $C_1$ and $C_2$ [35, 36]. The operation of this level shifter is illustrated in Fig. 3.7b where these capacitors are left out for the sake of simplicity.

The nodes (1.a), (1.b), (3.a), and (3.b) in the level shifter Fig. 3.7 suffer from the same limitation as nodes (1) and (3) in the high-voltage output buffer Fig. 3.6a. Namely, not settling to $V_{DD}$. The nodal voltages in Fig. 3.7b are steady-state values, but the level shifter does not achieve this steady state during operation. To help the nodes (1.a) and (1.b) settle quickly, the devices $M_{P7}$ and $M_{P8}$ are added as shown in Fig. 3.8. To help the nodes (3.a) and (3.b) also settle quickly, the devices $M_{N5}$, $M_{N6}$, $M_{P5}$ and $M_{P6}$ are added as shown in Fig. 3.8. Since the pairs $M_{N5}$–$M_{P5}$ and $M_{N6}$–$M_{P6}$ form an inverter, they also help improve quality of the output signal due to the regenerative property of CMOS inverters [32].

## 3.7. Tapered Inverter Chain

The remaining part of the CMOS driver is the two tapered inverter chains. These inverter chains are designed according to conventional VLSI design [32, 40]. Their primary purpose is buffering the signals




(a) A conventional low to high level shifter. (b) A simplified description of operation.

Figure 3.7: A conventional low to high level shifter and an illustration of its operation.

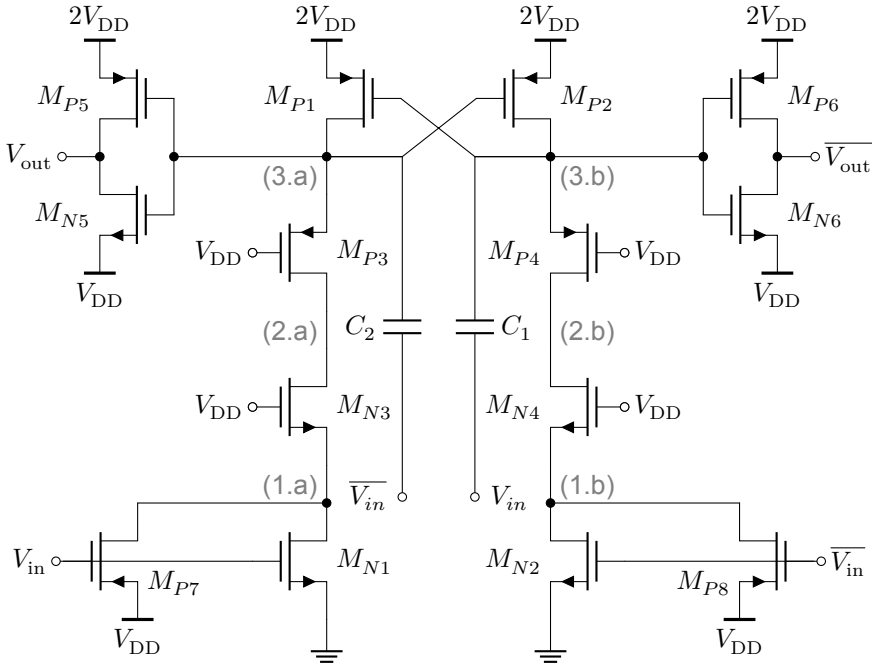



Figure 3.8: A modified low to high level shifter.

driving the large transistors $M_{N1}$ and $M_{P1}$ in the high-voltage output buffer (Figs. 3.6a and 3.6b), in addition to synchronization of the signals $V_{in,low}$ and $V_{in,high}$. However, unlike in conventional VLSI design, these inverter chains have no strict requirement regarding stage fan-out, i.e., tapering factor. The point is to reduce sensitivity to supply variations while maintaining sharp transitions as elaborated in Section 3.8. Ideally, both the number of stages and transition time are minimized. Furthermore, short

inverter chains are preferred to minimize undesired phase changes at the output of the DTX [15].

## 3.8. Sensitivity of Propagation Delay to Supply Variation

Supply variation affects propagation delay and causes jitter [32]. In time-to-digital converters (TDC), this fact can be exploited to tune the delay corresponding to delay cells, since typically a change of +1% in supply voltage corresponds to a change of −1% in propagation delay and vice versa [41, 42]. However, it is worth mentioning that is one-to-one relation is valid for only an extremely narrow range around the nominal supply voltage $V_{\mathrm{DD,norm}}$. Besides the supply voltage, propagation delay also depends on the drive capability of the inverter. The factor $C_{\mathrm{L}}/I_{\mathrm{DSAT}}$ in Eqs. (3.9) to (3.11) implicitly expresses the impact of stage fan-out on propagation delay.

$$t_{\mathrm{pHL}} = \ln(2)\frac{3}{4}\frac{C_{\mathrm{L}}V_{\mathrm{DD}}}{I_{\mathrm{DSAT,n}}} = \ln(2)\frac{3}{4}\frac{C_{\mathrm{L}}V_{\mathrm{DD}}}{(W/L)_{\mathrm{n}}\mu_{\mathrm{n}}C_{\mathrm{ox}}V_{\mathrm{DSAT,n}}\left(V_{\mathrm{DD}} - V_{\mathrm{th,n}} - V_{\mathrm{DSAT,n}}/2\right)} \tag{3.9}$$

$$t_{\mathrm{pLH}} = \ln(2)\frac{3}{4}\frac{C_{\mathrm{L}}V_{\mathrm{DD}}}{I_{\mathrm{DSAT,p}}} = \ln(2)\frac{3}{4}\frac{C_{\mathrm{L}}V_{\mathrm{DD}}}{(W/L)_{\mathrm{p}}\mu_{\mathrm{p}}C_{\mathrm{ox}}V_{\mathrm{DSAT,p}}\left(V_{\mathrm{DD}} - |V_{\mathrm{th,p}}| - |V_{\mathrm{DSAT,p}}|/2\right)} \tag{3.10}$$

$$t_{\mathrm{p}} = \left(t_{\mathrm{pHL}} + t_{\mathrm{pLH}}\right)/2 \tag{3.11}$$

To investigate the impact of supply variation on a tapered inverter chain of N stages long, it is insightful to assume that supply variations impact both the high-to-low propagation time and the low-to-high propagation time equally. In addition, assuming a fixed tapering factor throughout the chain allows the total propagation delay to be approximated by Eq. (3.15). To simplify derivation and highlight the stage fan-out $f_k$ and $V_{\mathrm{DD}}$, Eqs. (3.9) to (3.11) are rewritten as Eq. (3.12). The constants a, b, and c are defined in Eq. (3.13). The sensitivity of the total propagation delay is expressed in Eq. (3.16), that is, the partial derivative with respect to $V_{\mathrm{DD}}$. Assuming that $a_{\mathrm{n}} \approx a_{\mathrm{p}}$ and $c_{\mathrm{n,p}}$ is much less than $V_{\mathrm{DD}}$ Eq. (3.16) and yields the relationship in Eq. (3.17).

$$\frac{\partial}{\partial x}\left(\frac{ax}{bx+c}\right) = \frac{ac}{(bx+c)^2} \tag{3.12}$$

$$a = \ln(2)\frac{3}{4}\frac{1}{(W/L)\mu C_{\mathrm{ox}}V_{\mathrm{DSAT}}}, \quad b = 1, \quad \text{and} \quad c = V_{\mathrm{th}} + V_{\mathrm{DSAT}}/2 \tag{3.13}$$

$$t_{\mathrm{p}} = \sum_{k=1}^{k=N}\frac{f_k C_{\mathrm{in}}V_{\mathrm{DD}}}{2}\left(\frac{a_{\mathrm{n}}}{V_{\mathrm{DD}}+c_{\mathrm{n}}} + \frac{a_{\mathrm{p}}}{V_{\mathrm{DD}}+c_{\mathrm{p}}}\right), \quad f_k = f\forall k \tag{3.14}$$

$$t_{\mathrm{p}} \approx \frac{N f_k C_{\mathrm{in}}}{2}V_{\mathrm{DD}}\left(\frac{a_{\mathrm{n}}}{V_{\mathrm{DD}}+c_{\mathrm{n}}} + \frac{a_{\mathrm{p}}}{V_{\mathrm{DD}}+c_{\mathrm{p}}}\right) \tag{3.15}$$

$$\frac{\partial t_{\mathrm{p}}}{\partial V_{\mathrm{DD}}} = \frac{N f_k C_{\mathrm{in}}}{2}\left(\frac{a_{\mathrm{n}}c_{\mathrm{n}}}{(V_{\mathrm{DD}}+c_{\mathrm{n}})^2} + \frac{a_{\mathrm{p}}c_{\mathrm{p}}}{(V_{\mathrm{DD}}+c_{\mathrm{p}})^2}\right) \tag{3.16}$$

$$\frac{t_{\mathrm{p}} \mp |\Delta t_{\mathrm{p}}|}{t_{\mathrm{p}}} \propto \left(\frac{V_{\mathrm{DD}}}{V_{\mathrm{DD}} \pm |\Delta V_{\mathrm{DD}}|}\right)^2 \tag{3.17}$$

To verify that Eq. (3.17) indeed holds for supply variation within ±10% $V_{\mathrm{DD}}$, the simulated propagation delay different inverter chains driving the same load is analyzed. The load capacitance $C_{\mathrm{L}}$ is 100×$C_{\mathrm{in}}$, here $C_{\mathrm{in}}$ is the input capacitance of the first inverter in the chain. Based on Eq. (3.17), a 10% drop in supply voltages results in a 23.5% rise in the total delay. Therefore, even a linear approximation based on Eq. (3.18) yields good results in this range. This trend is confirmed by Eq. (3.16). That is, the relative change in supply voltage causes a relative change in propagation delay according to Eq. (3.18) and Fig. 3.10.

$$t_{\mathrm{p}}(V_{\mathrm{DD}}) = t_{\mathrm{p}}(V_{\mathrm{DD}} = V_{\mathrm{DD,norm}}) \cdot \left[1 - 2\frac{V_{\mathrm{DD}} - V_{\mathrm{DD,norm}}}{V_{\mathrm{DD,norm}}}\right] \tag{3.18}$$

It is an undeniable fact that the total delay is proportional to supply variation within the ±10% $V_{\mathrm{DD}}$ range. It is therefore important to minimize the total delay to mitigate delay variations. On the one hand, minimizing the chain length requires large stage fan-outs, hence degrading the drive capability

of inverter stages. On the other hand, minimizing the stage fan-out requires longer chains, hence adding more delay. Minimum delay variations are achieved by striking a balance between the drive capability and the number of stages in the inverter chain. A good trade-off not only benefits resilience against supply variations but also benefits area and power consumption. In addition, mitigating delay variations avoids unwanted phase change in the DTX output [15].

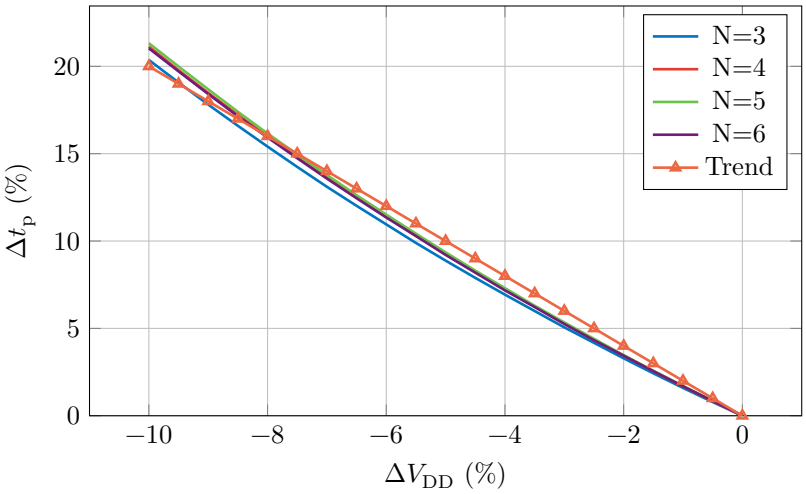



Figure 3.9: Relative variations in $t_p$ vs. relative variations in $V_{DD}$ for different chain lengths.

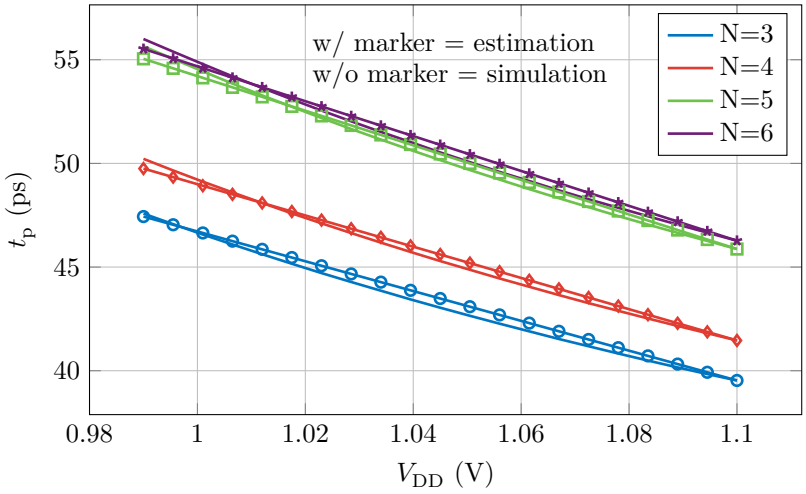



Figure 3.10: Propagation delay vs. supply voltage for different chain lengths.

## 3.9. Design Procedure

The CMOS driver can be thought of as an interface between the core CMOS domain and the LDMOS domain. The design of such a driver starts at the LDMOS end. A high-voltage output buffer is designed based on the gate-to-source capacitance $C_{GS}$ of the LDMOS segment, which can be modeled as a lumped capacitor. After the high-voltage output buffer (HoC), tapered inverter chains are designed such that input capacitances of the high-voltage output buffer $C_{in,low}$ and $C_{in,high}$ are translated to a fan-out of ≤4. Subsequently, a level shifter is designed such that the complementary input signals are DC-shifted upwards with $V_{DD}$. Finally, depending on the delay of each inverter chain, a delay cell is designed to ensure that $V_{in,low}$ (0–$V_{DD}$) and $V_{in,high}$ ($V_{DD}$–2$V_{DD}$) are synchronized. Perfect synchronization is, however, neither necessary nor easy to achieve. Besides, a 5 ps delay of $V_{in,high}$ with respect to $V_{in,low}$ proves to be beneficial for a quick low-to-high transition of the HoC structure at 3.5 GHz.

To simplify the design of the high-voltage output buffer, the devices in Fig. 3.11 are parameterized according to Table 3.2. The final sizing is achieved iteratively. The first step to find an optimal unit width is to set α and β at 1 and sweep the device width. This parameter sweep takes place in a transient simulation where ideal and synchronized clock signals $V_{\text{in,low}}$ (0–$V_{\text{DD}}$) and $V_{\text{in,high}}$ ($V_{\text{DD}}$–2$V_{\text{DD}}$) at $f_{\text{c}}$ = 3.5 GHz with a duty cycle of 25% are driving the high-voltage output buffer, which in turn is driving the load capacitor representing a single LDMOS segment. Once an appropriate fall time $t_{\text{f}}$ is achieved, the unit width is fixed. The second step is to find β = $W_{P1}/W_{N1}$ that satisfies the desired rise time $t_{\text{r}}$ by increasing its value. The third step is to find α = $W_{P1}/W_{N3}$ that minimizes the input capacitances $C_{\text{in,low}}$ and $C_{\text{in,high}}$. When α is too large, $M_{P3}$ and $M_{N3}$ are not capable of charging and discharging the nodes (1) and (3). The fourth and final step is balancing the currents through the high-voltage output buffer. This step is, however, optional and is discussed in Section 4.4.

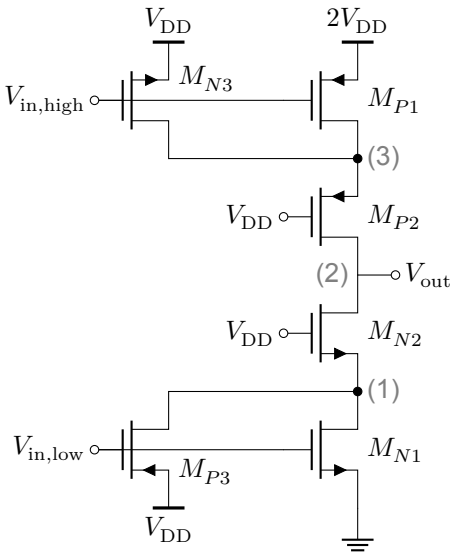



Figure 3.11: High-voltage output buffer.

| Device | Width |
|---|---|
| $M_{N1}$ | W |
| $M_{N2}$ | W |
| $M_{N3}$ | βW/α |
| $M_{P1}$ | βW |
| $M_{P2}$ | βW |
| $M_{P3}$ | W/α |

Table 3.2: Relative sizing of the devices.

To design a tapered inverter chain, the fan-out-based procedure put forward by Rabaey in [32] proves to be effective. In general, an inverter chain comprising $K$ number stages receives an input signal $V_{\text{in}}$ with certain characteristics, and a similar signal at the output of the final stage drives a load capacitance $C_{\text{L}}$. When $K$ is an odd, the signal $V_{\text{in}}$ appears to be inverted. These characteristics of $V_{\text{in}}$ include duty cycle, rise time $t_{\text{r}}$ and fall time $t_{\text{f}}$.

First, the effective input capacitance to be switched at both inputs of the high-voltage output buffer is estimated using Eq. (3.19). The effective output capacitance is estimated using Eq. (3.20) and is not utilized in any calculation. It is rather provided for completeness. The first integration interval $t_1$–$t_2$ stands for a rising output edge, where the charge is pulled out of $C^*_{\text{in}}$. The second integration interval $t_3$–$t_3$ stands for a falling output edge, where the charge is pushed into $C^*_{\text{in}}$. For each input of the high-voltage output buffer, a separate inverter chain is designed based on the estimated $C^*_{\text{in}}$. The integration interval in Eq. (3.20) is one clock cycle long $T_{\text{c}}$ and can start at any arbitrary time $t_0$. Furthermore, $i_{\text{g}}$(t) is the instantaneous gate current, $i_{V_{\text{DD}}}$(t) is the instantaneous current supplied by the power rail, and $i_{V_{\text{SS}}}$(t) is the instantaneous current returning to the ground rail.

$$C^*_{\text{in}} = -\frac{1}{V_{\text{DD}}}\int_{t_1}^{t_2} i_{\text{g}}(t)\text{d}t = \frac{1}{V_{\text{DD}}}\int_{t_3}^{t_4} i_{\text{g}}(t)\text{d}t \tag{3.19}$$

$$C^*_{\text{out}} = -\frac{1}{V_{\text{DD}}}\int_{t_0}^{t_0+T_{\text{c}}} i_{V_{\text{DD}}}(t)\text{d}t = \frac{1}{V_{\text{DD}}}\int_{t_0}^{t_0+T_{\text{c}}} i_{V_{\text{SS}}}(t)\text{d}t \tag{3.20}$$

Once $C_{\text{in,low}}$ and $C_{\text{in,high}}$ are determined, the first inverter stage is sized depending on the desired stage fan-out. This inverter has an aspect ratio β = $W_{\text{P}}/W_{\text{N}}$. $W_{\text{N}}$ = W is the unit width in the design of

the tapered inverter chains. The effective input capacitance of the first inverter stage is estimated using Eq. (3.19). Furthermore, the overall fan-out $F$ is computed using Eq. (3.22), where $C_L$ is either $C_{in,low}$ (bottom chain) or $C_{in,high}$ (top chain), and $C_{in}$ corresponds to the first inverter in the chain. Finally, the number inverter stages $K$ is computed according to Eq. (3.23). The stage fan-out Eq. (3.21) follows from a trade-off between signal integrity on the one hand, and power consumption and occupied silicon area on the other hand. The resulting inverter chain has $K$ stage and is illustrated in Fig. 3.12. The sizing is summarized in Table 3.3.

$$f_k = C_{\mathrm{in},k}/C_{\mathrm{in},(k-1)}, \quad f_k = f \forall k \tag{3.21}$$

$$F = C_{\mathrm{L}}/C_{\mathrm{in},1} \tag{3.22}$$

$$K = \log_{f_k}(F) \tag{3.23}$$

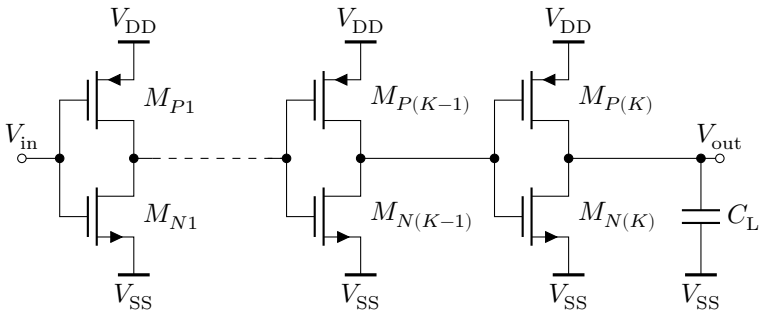



Figure 3.12: Tapered inverter chain.

| Device | Width |
|---|---|
| $M_{N1}$ | W |
| $M_{P1}$ | βW |
| $M_{N2}$ | $f_k \cdot W$ |
| $M_{P2}$ | $\beta f_k \cdot W$ |
| $M_{N(k)}$ | $f_k^{(k-1)} \cdot W$ |
| $M_{P(k)}$ | $\beta f_k^{(k-1)} \cdot W$ |
| $f_k \approx f \forall k$ | |

Table 3.3: Relative sizing of the devices.

The compact low power level shifter in Fig. 3.13 distinguishes several standard cells. The pairs $M_{N1}$–$M_{P7}$, $M_{N2}$–$M_{P8}$, $M_{N5}$–$M_{P5}$, and $M_{N6}$–$M_{P6}$ constitute inverters. These inverters can be sized as a unit inverter, i.e., the same size as the first inverter stage in the tapered inverter chain. The cross-coupled pair $M_{P1}$–$M_{P2}$ can have similar sizing as $M_{P3}$–$M_{P4}$. The capacitors $C_1$ and $C_2$ provide capacitive coupling from (1.a) to (3.a), and from (1.b) to (3.b). Provided that the inputs of the level shifter are square waves with the magnitude of $V_{DD}$, the capacitive coupling ensures that the input voltages are visible at nodes (3.a) and (3.b) with an offset $\Delta V$. This offset depends on the capacitance at the nodes (3.a) and (3.b), and the capacitors $C_1$ and $C_2$ as shown in Eq. (3.24) [35]. It is tempting to make $C_1$ and $C_2$ (nmoscaps) as large as possible, however, their role is to help the cross-coupled pair switch more easily. Therefore, the size of these capacitors follows from a performance-area trade-off.

$$\Delta V = \frac{1}{1 + C_{\mathrm{par}}/C_{\{1,2\}}} V_{\mathrm{DD}} \tag{3.24}$$

The design procedure put forward in this section gives clear and structured instructions on how to size the proposed driver. Nevertheless, this procedure does not lead to an optimum design, not necessarily. The final sizing provided in Section 3.10 is achieved iteratively.

## 3.10. Implementation

The high-voltage output buffer generates an output voltage swing of $2V_{DD}$. To achieve the desired drive capability at 3.5 GHz, the house-of-cards structure (HoC) is sized according to the design procedure laid out in Section 3.9. Based on the desired switching behavior explained in Section 3.4, the HoC structure is sized for $t_r < t_f$. The assisting devices $M_{N3}$ and $M_{P3}$ are kept at a relatively small size. As a result, $M_{N3}$ and $M_{P3}$ have a small contribution to the input capacitance. Therefore, the drive capability expected from the tapered inverter chains is relaxed. The final device sizing is summarized in Table 3.5.

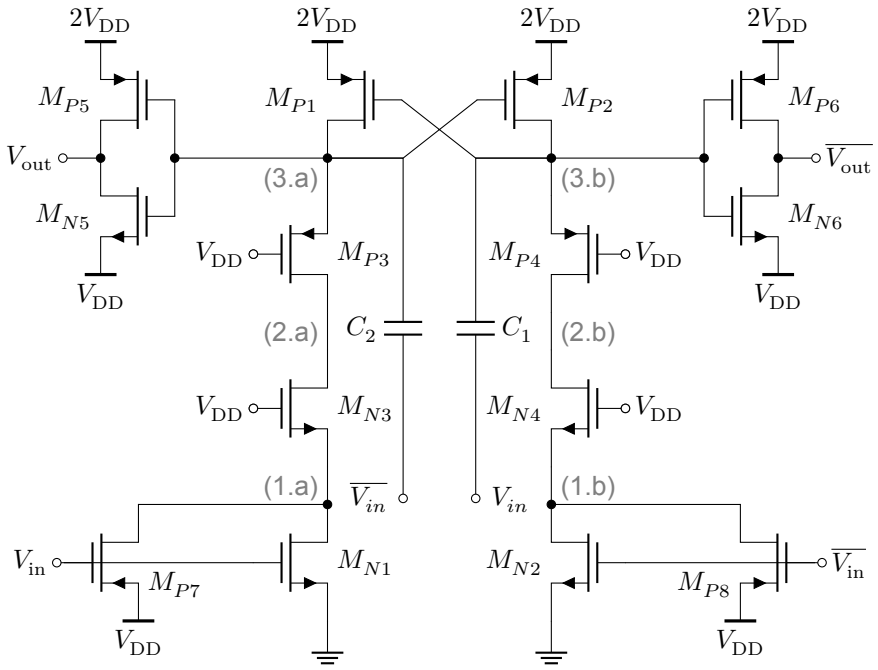



Figure 3.13: Level shifter

| Device | Width |
|---|---|
| $M_{N1,2}$ | W |
| $M_{N3,4}$ | W |
| $M_{N5,6}$ | αW |
| $M_{P1,2}$ | $\beta_1$W |
| $M_{P3,4}$ | W |
| $M_{P5,6}$ | W |
| $M_{P7,8}$ | $\beta_2$W |

Table 3.4: Relative sizing of the devices.

Table 3.5: Final sizing of the high-voltage output buffer.

| Device | Finger width (µm) | Number of fingers | Total width (µm) |
|---|---|---|---|
| $M_{N1}$ | 0.9 | 16 | 14.4 |
| $M_{N2}$ | 0.9 | 16 | 14.4 |
| $M_{N3}$ | 1.5 | 6 | 4.5 |
| $M_{P1}$ | 1.6 | 64 | 102.4 |
| $M_{P2}$ | 1.6 | 64 | 102.4 |
| $M_{P3}$ | 0.9 | 3 | 2.7 |

The effective input capacitances of the high-voltage output buffer are estimated using Eq. (3.19). The following capacitances are estimated with the help of a transient simulation. $C_{in,low}$ = 10.69 fF and $C_{in,high}$ = 64.46 fF. Although the 40 nm TSMC process offers a minimum device with of 120 nm, a unit inverter with $W_N$ = 270 nm $W_P$ = 590 nm ($\beta \approx 2.2$) is chosen instead. This sizing is inspired by the sizing of the standard cells provided within the TSMC 40 nm PDK. The input capacitance of such unit inverter is similarly estimated and $C_{in}$ = 515.8 aF. The fan-out is generally motivated by the desired number of stages in a chain, but the drive capability can be equally important. Therefore, post-layout simulation is needed to get a better estimation of the input capacitances. The layout parasitics result in the following values: $C_{in}$ = 919.8 aF, $C_{in,low}$ = 17.60 fF and $C_{in,high}$ = 112.6 fF. A stage fan-out of 4 is conventionally chosen, but a fan-out of 2 proved to be more practical in terms of drive capability.

The largest chain, the top one, has a fan-out of roughly 125 and is designed first. To effectively buffer the level shifted signals, the design procedure dictates a chain of 6 stages. As long as the inverter chains achieve sufficient synchronization of $V_{in,low}$ and $V_{in,high}$, some flexibility in the design is afforded. The remaining chain, the bottom one, has a fan-out of roughly 21. Stage fan-outs of 2 and 4 dictate at least 4 and 2 number of stages, respectively. Nevertheless, a fan-out of 21 is relatively low and a tapered chain of only two stages offers sufficient drive capability. To synchronize the signals, the bottom inverter is preceded by a chain of 6 unit inverters forming a delay cell. The sizing of the unit inverter is listed in Table 3.6.

Table 3.6: Final sizing of the unit inverter.

| Device | Finger width (µm) | Number of fingers | Total width (µm) |
|---|---|---|---|
| $M_{N1}$ | 0.27 | 1 | 0.27 |
| $M_{P1}$ | 0.59 | 1 | 0.59 |

Table 3.7: Final sizing of the level shifter.

| Device | Finger width (µm) | Number of fingers | Total width (µm) |
|---|---|---|---|
| $M_{N1}$ & $M_{N2}$ | 0.12 | 2 | 0.24 |
| $M_{N3}$ & $M_{N4}$ | 0.12 | 2 | 0.24 |
| $M_{N5}$ & $M_{N6}$ | 0.19 | 2 | 0.38 |
| $M_{P1}$ & $M_{P2}$ | 0.625 | 2 | 1.25 |
| $M_{P3}$ & $M_{P4}$ | 0.50 | 2 | 1.0 |
| $M_{P5}$ & $M_{P6}$ | 0.12 | 2 | 0.24 |
| $M_{P7}$ & $M_{P8}$ | 0.45 | 2 | 0.90 |

A unit inverter is essentially a good starting point for sizing the level shifter, but its sizing can be more compact. The sizing summarized in Table 3.7 follows from selecting a unit width of 240 nm instead of 270 nm. The parameters α, $\beta_1$, $\beta_2$ are found in an iterative fashion. Finally, the capacitors $C_1$ and $C_2$ are sized to provide sufficient capacitive coupling and to be compact.

The driver achieves duty cycle extension through sizing. It receives two commentary signals, a 25% duty cycle signal and its 75% complement. Two inverter chains are designed such that the 25% duty cycle pulses are stretched and the 75% duty cycle pulses are shrunk. This is achieved by asymmetric inverters, this is, the propagation delays $t_{pHL}$ and $t_{pLH}$ are unequal. The same is done in the HoC. The relative sizing of these inverter chains is listed in Table 3.9.

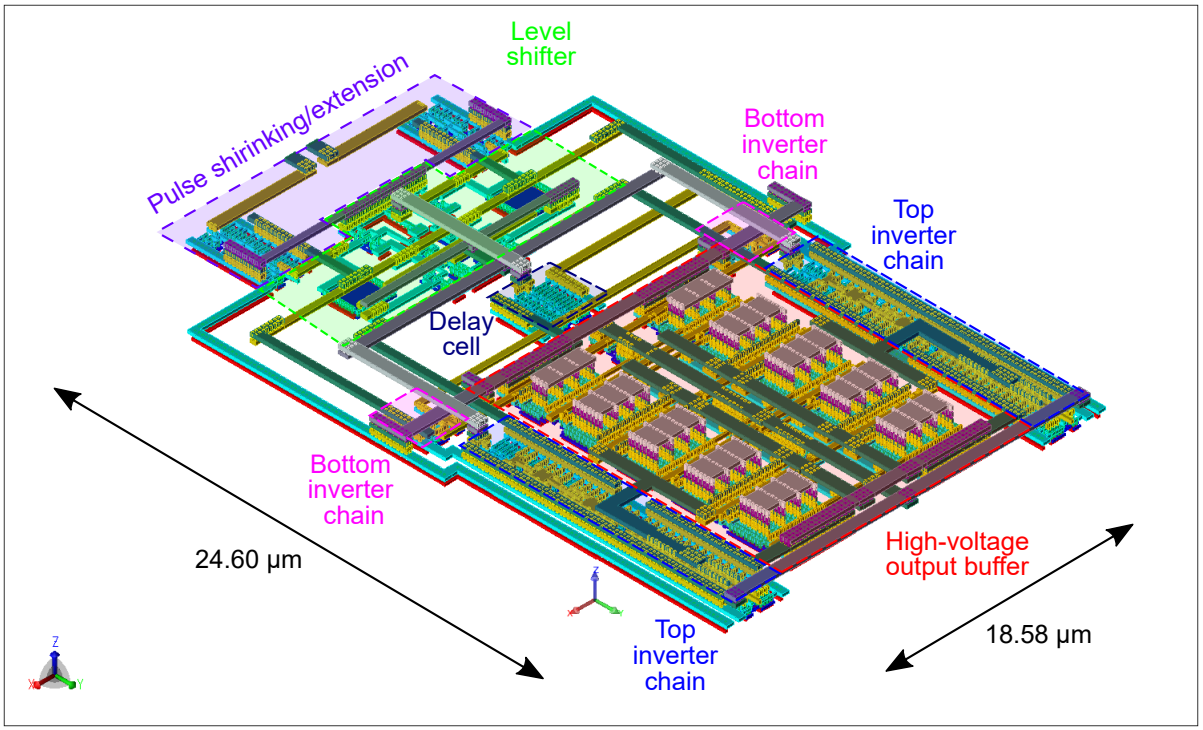



Figure 3.14: A 3D visual of the layout.

Table 3.8: Final capacitors in the level shifter.

| Device | Width (µm) | Length (µm) | Capacitance (fF) |
|---|---|---|---|
| $C_1$ & $C_1$ | 1.5 | 1.5 | 18.2 |

Table 3.9: Relative sizing the pulse stretching/shrinking inverter chain.

| | $\beta_1$ | $\beta_2$ | $\beta_3$ | $\beta_4$ |
|---|---|---|---|---|
| Stretch | 1.01 | 3.80 | 1.52 | 1.52 |
| Shrink | 2.28 | 0.61 | 3.04 | 1.52 |

The complete driver including extra logic for pulse shrinking and extension fits within a rectangle of 18.58 µm × 24.60 µm. This area is nearly 30% of the 40 µm × 40 µm allocated to the design. A 3D visual of the layout is provided in Fig. 3.14. The different components are highlighted here to show their position and size relative to one another. Symmetry in the layout is carefully considered to minimize delay mismatch and area. The HoC structure comprises two identical halves connected in parallel, with the assisting devices in the middle. Each half has its own tapered inverter chain. Furthermore, both $V_{\text{in,low}}$ and $V_{\text{in,high}}$ are tapped from a point on the axis dividing the HoC in half. This way, the physical distance signals have to travel to either half is (nearly) equal.

## 3.11. Results

The driver is tested using post-layout simulations. A 3.5 GHz 25% duty pulsed signal is fed into the driver that in turn is connected to a capacitive load of 150 fF. The input and output voltages of the high-voltage output buffer are captured in Fig. 3.16. The propagation delays $t_{\text{pLH}}$ and $t_{\text{pHL}}$ of the driver are 237.9 ps and 196.1 ps, respectively. The resulting average propagation delay is 216 ps. Furthermore, the rise and fall times are 47.31 ps and 77.99 ps. These delays and transition times are defined based on the 50%-mark and the 10%-90% marks, respectively. The $V_{\text{T}}$ of LDMOS is 0.7 V, therefore the effective part of the drive signals is above the 0.7 V-line. To improve the drain efficiency, a digital signal is subjected to pulse stretching/shrinking to increase the effective duty cycle seen at the gate of the LDMOS, and ultimately the duty cycle of its drain current. This effective duty ($d^*$) is defined by the pulse width at the 1.45 V-line (50%-mark of the swing between 0.7 V and 2.2 V). The realized duty cycle is nearly 33% as shown in Fig. 3.17.

The total power consumption averages at 3.60 mW when unloaded and 6.14 mW with a loaded ($fCV^2$ = 2.54 mW). Fig. 3.15 shows a detailed breakdown of the power consumption. Furthermore, power consumption and relevant delays following from a corner analysis are summarized in Table 3.10.

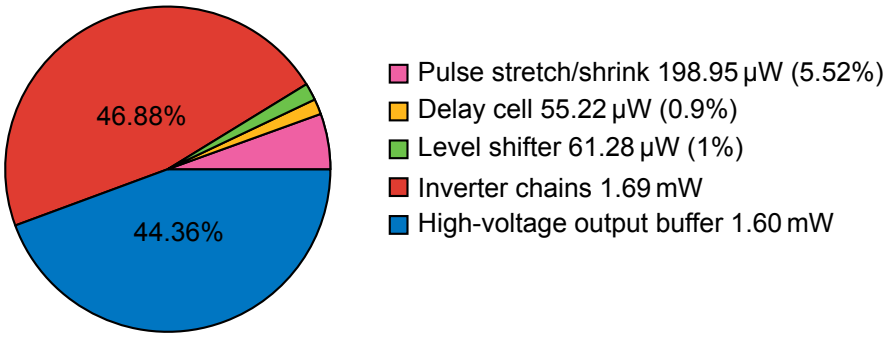



Figure 3.15: A detailed breakdown of the power consumption of driver post-layout with no load.

The delay variations caused by fixing one supply and varying the other and the corresponding phase shifts at 3.5 GHz($\Delta t_{\text{p}} \times f \times 360°$) are shown in Fig. 3.18. It is worth noting that the $2V_{\text{DD}}$-rail causes more

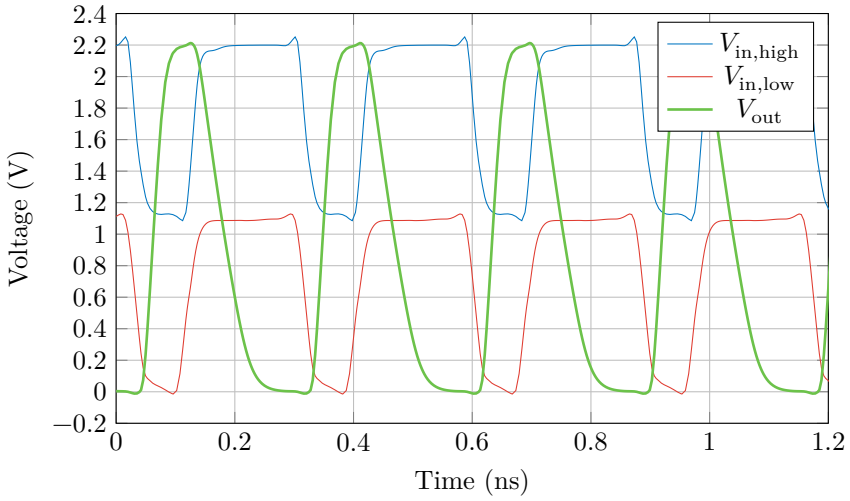



Figure 3.16: The input/output voltages of the high-voltage output buffer post-layout.

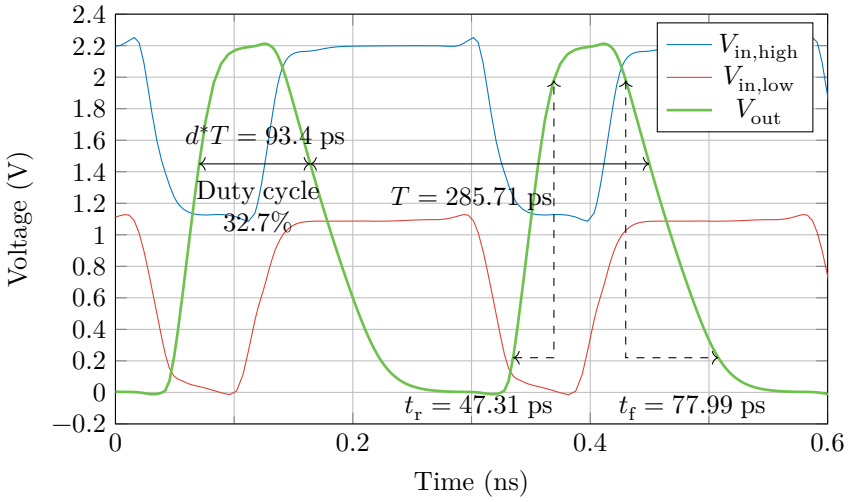
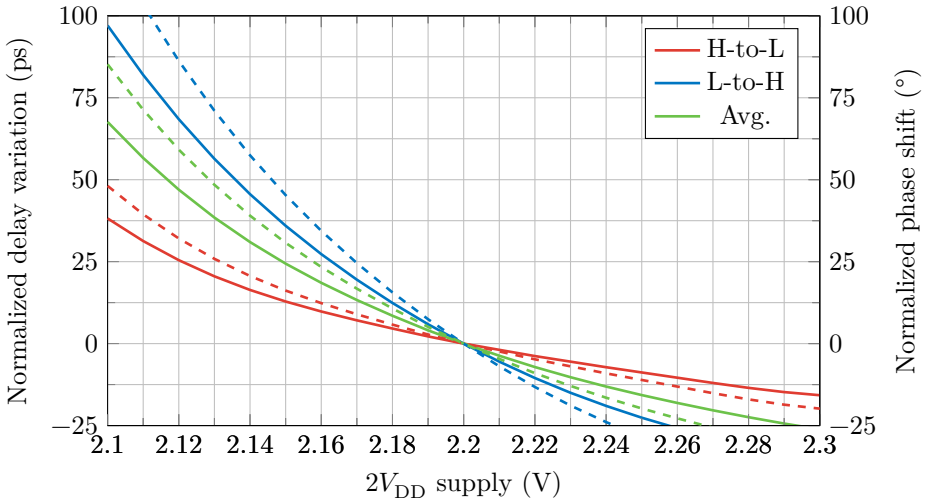



Figure 3.17: The input/output voltages of the high-voltage output buffer post-layout (annotated).

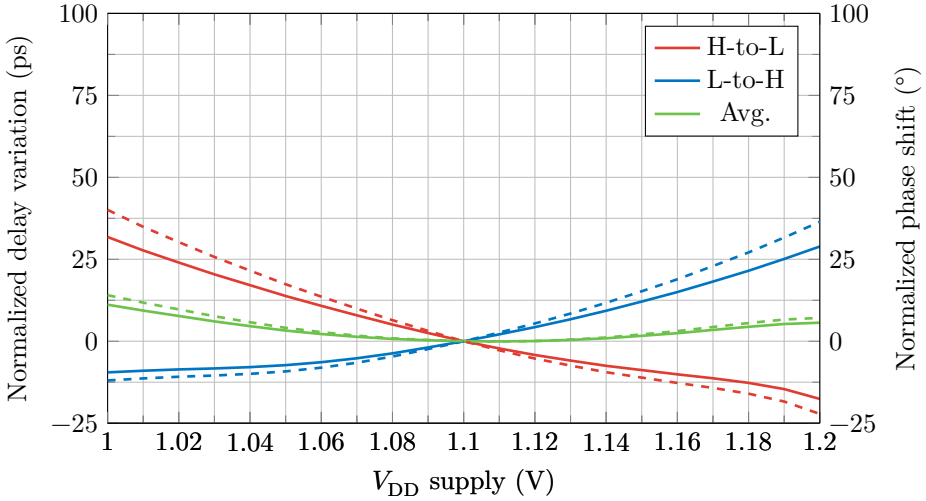
delay variations than the $1V_{\text{DD}}$-rail. This is highlighted by comparing Fig. 3.18a and Fig. 3.18b. Another remarkable observation is that the low-to-high transition becomes slower with increasing bottom rail. On the one hand, the bottom inverter chain experiences a delay reduction due to its increased supply. On the other hand, the top inverter chain experiences a delay increment due to its reduced supply.

The driver's output voltage waveform is used to fit a model in Keysight Advanced Design System (ADS). In an ADS simulation, this model is used in conjunction with a model of the segmented LDMOS to evaluate pertinent metrics such as output power and efficiency. This simulation does not account for the full DTX. Only drivers and LDMOS segments with suitable output matching and optimal load conditions are considered. Fig. 3.19 shows the gate voltage and drain current of a single segment at 3.5 GHz.[2] When compared to the gate voltage waveform, the duty cycle of the drain current waveform shrinks by nearly 1.3 percentage points. The DPA is at full power, i.e., all 512 segments are active. The simulation is executed with two distinct LDMOS models.[3] Model 1 is non-empirical and model 2 is based on measurements of the $V_{\text{T}}$-shifted LDMOS devices. Table 3.11 lists the relevant powers and efficiencies, as well as the power consumption of a single driver.

[2]Simulation results provided by R. J. Bootsman.
[3]Models are developed and provided by Ampleon.

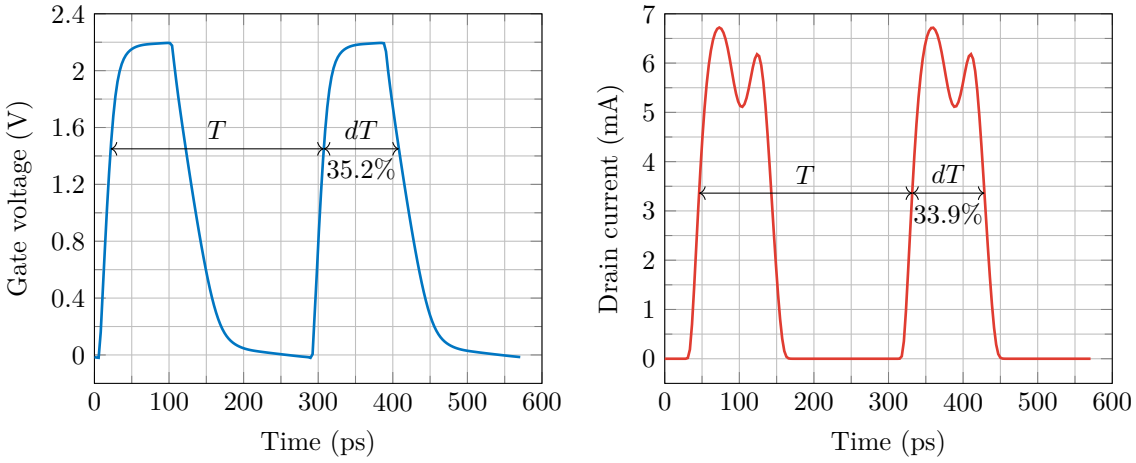



(a) $1V_{DD}$ is fixed and $2V_{DD}$ varies.




(b) $1V_{DD}$ varies and $2V_{DD}$ is fixed.

Figure 3.18: Delay variations and phase shift vs. supply variation.




(a) (b)

Figure 3.19: Gate voltage and drain current waveforms of one LDMOS segment.

Table 3.10: Corner analysis of relevant delays and power consumption.

| Corner | $T$ (°C) | $t_r$ (ps) | $t_f$ (ps) | $t_{pHL}$ (ps) | $t_{pLH}$ (ps) | $t_p$ (ps) | $d$ (%) | Power* (mW) |
|---|---|---|---|---|---|---|---|---|
| TT | 27 | 34.18 | 78.00 | 194.60 | 237.70 | 216.15 | 32.28 | 3.633 |
| TT | 150 | 36.86 | 87.14 | 205.20 | 255.40 | 230.30 | 33.23 | 3.728 |
| TT | −40 | 32.27 | 71.61 | 183.73 | 224.73 | 204.23 | 34.89 | 3.024 |
| SS | 27 | 39.85 | 91.61 | 263.76 | 266.20 | 264.98 | 34.04 | 2.635 |
| SS | 150 | 42.54 | 100.90 | 273.86 | 289.90 | 281.88 | 35.24 | 3.485 |
| SS | −40 | 37.84 | 84.65 | 253.05 | 266.20 | 259.63 | 33.52 | 2.029 |
| FF | 27 | 29.93 | 66.47 | 152.30 | 188.60 | 170.45 | 31.54 | 3.701 |
| FF | 150 | 32.72 | 75.50 | 165.20 | 144.10 | 154.65 | 33.21 | 3.701 |
| FF | −40 | 28.09 | 60.74 | 208.10 | 175.90 | 192.00 | 30.52 | 3.404 |
| SF | 27 | 32.00 | 87.10 | 202.55 | 249.09 | 225.82 | 33.78 | 3.608 |
| SF | 150 | 35.11 | 96.02 | 214.38 | 266.63 | 240.51 | 35.13 | 3.692 |
| SF | −40 | 29.86 | 80.31 | 192.45 | 234.53 | 213.49 | 32.84 | 3.300 |
| FS | 27 | 37.43 | 70.27 | 187.24 | 230.06 | 208.65 | 32.51 | 3.603 |
| FS | 150 | 39.67 | 79.44 | 197.26 | 246.76 | 222.01 | 34.26 | 3.767 |
| FS | −40 | 35.77 | 64.44 | 179.00 | 218.09 | 198.55 | 31.61 | 3.006 |
| Mean | | 34.94 | 79.61 | 204.85 | 232.93 | 218.89 | 33.24 | 3.354 |
| Std | | 4.16 | 11.76 | 34.58 | 38.71 | 34.20 | 1.39 | 0.492 |

*The 2.541 mW attributed to switching $C_L$ at 3.5 GHz is excluded.

Table 3.11: Relevant powers and efficiencies corresponding to a DPA at full power.

| | $P_{drivers}$ (W) | $P_{DC}$ (W) | $P_{OUT}$ (W) | $\eta_D$ (%) | $\eta_S$ (%) | $P_{driver}$ (mW) | $C_{L,unit}$ (fF) |
|---|---|---|---|---|---|---|---|
| Model 1 | 3.38 | 29.41 | 19.79 | 67.28 | 60.34 | 6.61 | 178.69 |
| Model 2 | 3.44 | 39.57 | 23.43 | 59.22 | 54.48 | 6.72 | 193.64 |

# 4

# Driver for GaN-Based RF-DACs

Gallium nitride (GaN) is an III-V wide bandgap semiconductor. In the 1990s, it was deemed excellent for high-power/high-frequency transistors based on material properties such as electron mobility and saturated electron velocity [43]. As of today, it has become an undeniable competitor to state-of-the-art laterally-diffused metal-metal oxide semiconductor (LDMOS) technology for wireless communications. The high power density, high efficiency, wide bandwidth, high breakdown electric field, and superior thermal conductivity make GaN notably suited for massive multiple-input multiple-output (mMIMO) base stations [44, 45]. Original equipment manufacturers (OEM) such as Huawei, Nokia, and Samsung have already made it their choice for 5G mMIMO infrastructures [45]. The radio frequency GaN market is expected to reach over $2.4 billion by 2026 [45]. Charts like Fig. 4.1 are frequently used to compare RF technologies [44]. It should be noted, however, that Fig. 4.1 does not represent the theoretical limits of any of the included technologies.

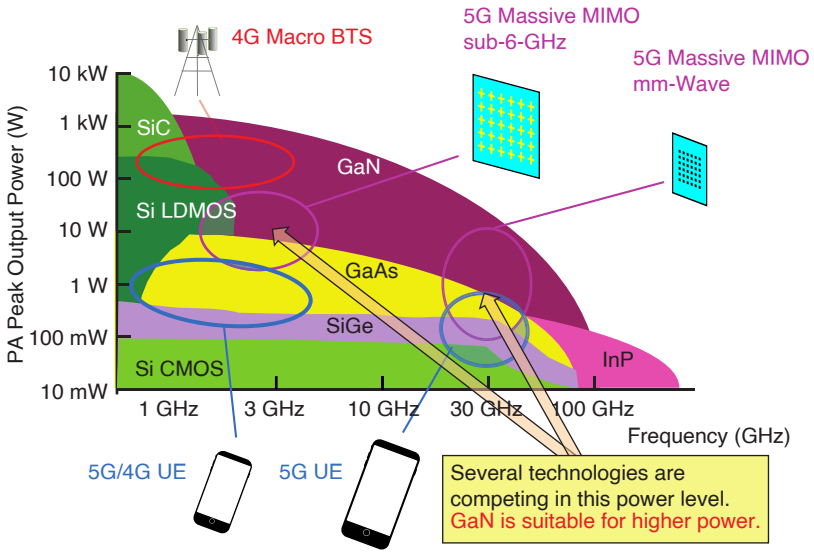



Figure 4.1: Technology comparison in terms of output power and operating frequency.

As GaN technology continues to outperform LDMOS in the 5G market [45], it is worth considering when designing a high power RF-DAC for 5G base stations. A GaN-based RF-DAC may not be as straightforward as the LDMOS-based version though. GaN high-electron-mobility transistors (HEMTs) are known for being “normally on” and requiring a negative gate-to-source voltage to turn off. Early generations of GaN HEMTs require gate voltages ranging from −8 to −4 V to shut off completely. Research has shown that a positive shift of the threshold voltage is possible nonetheless. The threshold voltage could be increased to −1.5 V [46]. Although there is no GaN technology suitable for replac-

ing the LDMOS in the RF-DACs proposed in [15, 26, 27, 29], still a CMOS driver is proposed here in anticipation of future developments.

## 4.1. Design Considerations

The driver for GaN-based RF-DACs must generate voltage swings between the $-2V_{DD}$-rail and ground-rail. To facilitate the negative voltages the driver requires for its operation with a grounded p-type substrate, it is necessary to use the triple well option usually available in modern CMOS processes. As shown in Fig. 4.2, the triple well option provides an isolated p-well. The latter can be biased to a negative voltage without causing any of the p-n junctions to be forward-biased. Based on Table 4.1 [47], biasing the isolated p-well to $-2V_{DD}$ and the deep n-well to ground while keeping the substrate biased to the ground potential is well within the safe operating region of the body diodes.

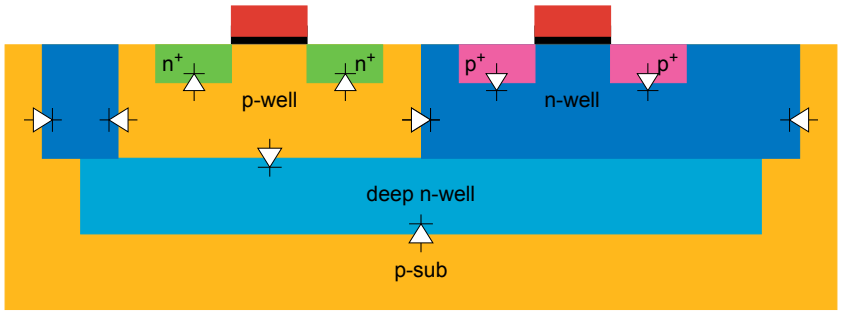



Figure 4.2: A simplified cross-section of triple well process.

Table 4.1: Breakdown voltages for the different substrate diodes nanometer CMOS technology.

| Symbol | Value (V) | Description |
|---|---|---|
| $V_{NP}$ | 8 | n+/p-well diode |
| $V_{PN}$ | 10 | p+/n-well diode |
| $V_{NW}$ | 12 | n-well/p-sub diode |
| $V_{PW}$ | 10 | p-well/deep n-well diode |
| $V_{DNW}$ | 12 | deep n-well/p-sub diode |

## 4.2. Driver Topology

In a polar DTX, the DPA comprises an array of sub-power amplifier cells [34]. The IQ baseband data is converted to an Amplitude Code Word (ACW) and its digital phase representation [28], which are bit-wise mixed through logic gates [26]. For base station applications, the DPA is a segmented high-power output stage driven by a CMOS chip. A CMOS driver provides a high-speed interface between a digital CMOS IC and a gate-segmented GaN die. Assuming the GaN technology is optimized to have a $V_T$ above −2.2 V and a fully-on state as its gate-to-source voltage nears 0 V, it is possible to recycle the driver proposed for LDMOS-based RF-DAC in Section 3.3, albeit with minor changes.

The driver for GaN-based RF-DACs, much like the CMOS driver for LDMOS-based RF-DACs, has an NMOS pull-down network (PDN) and a PMOS pull-up network (PUN). The PUN is driven by a level-shifted version of the signal driving the PDN, or vice-versa. The main difference is that the driver for GaN-based RF-DACs must generate voltage swings between $-2V_{DD}$ and ground. To achieve this, digital signals must be level-shifted down towards negative voltages. The signal driving the PMOS pull-up network swings between $-V_{DD}$ and ground while the signal driving the NMOS pull-down network swings between $-2V_{DD}$ and $-V_{DD}$. Two level shifters are utilized to create these level-shifted signals. To simplify the design, the first level shifter generates the $-V_{DD}$ to 0 swings for the pull-up network and the second level shifter. The latter, in turn, generates the $-2V_{DD}$ to $-V_{DD}$ swings for the pull-down network. The feasibility of this approach is demonstrated in [48, 49].

The driver comprises two level shifters, two tapered inverter chains, and a high-voltage output buffer as illustrated in Fig. 4.3. Since the design of the two tapered inverter chains, and high-voltage output buffer can be identical to those from Chapter 3, they can be designed in a similar fashion. For the sake of brevity, only the level shifter is discussed in this chapter.

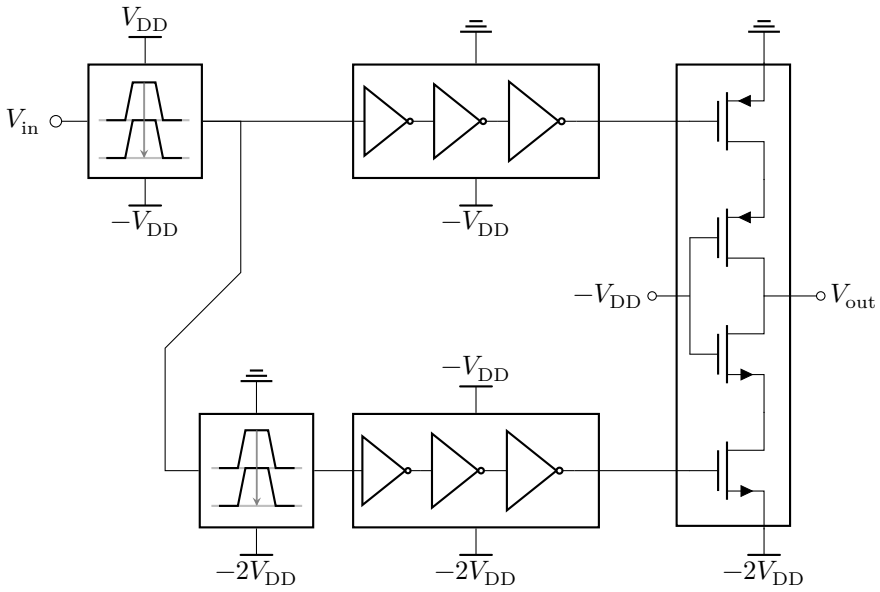



Figure 4.3: Topology of the proposed CMOS driver.

## 4.3. Level Shifter

The high to low level shifter in Figs. 4.4 and 4.5 is a modified version of the low to high level shifter introduced in Section 3.6 and extensively discussed in Chapter 3. Similarly, it requires two complementary input signals, $V_{in}$ and $\overline{V_{in}}$, whose swing is $V_{DD}$. Complementary output signals switching between $-V_{DD}$ and ground are generated at node (3.a) and (3.b) by taking advantage of the cross-coupling of $M_{N1}$ and $M_{N2}$ as illustrated in Fig. 4.5. To improve the speed of this level shifter, its inputs are capacitively coupled to the gate of $M_{N1}$ and $M_{N2}$ using $C_1$ and $C_2$ [35, 36]. The operation of this level shifter is illustrated in Fig. 4.4 where these capacitors are left out for simplicity.

Level-shifting complementary digital signals result in $\overline{V_{LS1}}$ and $V_{LS1}$ shown in Fig. 4.6. Feeding these signals into a additional level shifter results in $\overline{V_{LS2}}$ and $V_{LS2}$. Finally, $V_{LS1}$ and $V_{LS2}$ are buffered with tapered inverter chains driving and aligned to drive a high-voltage output buffer as shown in Fig. 4.3.

## 4.4. Charge Recycling

The $2V_{DD}$ driver implies stacked logic. More specifically, simple inverters are stacked on top of each other between the $2V_{DD}$-rail and ground-rail with the $V_{DD}$-rail as the mid-rail. This concept is discussed among others in [50–52]. Charge recycling aims to improve the system efficiency of a system on a chip (SoC) by reducing the losses associated with power conversion losses [50]. When two voltage domains are stacked, the current is drawn from the $2V_{DD}$-rail and sunk into $V_{DD}$-rail by the logic in the top domain. This current is drawn from the $V_{DD}$-rail, i.e., the mid-rail, and sunk into the ground rail by the logic in the bottom domain. Hence, the current is recycled.

Stacking two voltage domains offers an implicit DC–DC conversion of 2:1 [52]. For a GaN-based RF-DAC, this could reduce the number of supplies from four (i.e., $-2_{DD}$, $-V_{DD}$, ground, and $V_{DD}$) to three (i.e., $-2V_{DD}$, ground, and $V_{DD}$). The $-V_{DD}$ could be derived from $-2V_{DD}$. However, current from one voltage domain is not (always) fully recycled in the other. Therefore, it is most likely to have a mismatch between the currents flowing into and out of the mid-rail. This current mismatch causes the mid-rail voltage to stray from its ideal value, i.e., $-1 \times V_{DD}$. A compact voltage regulator can be

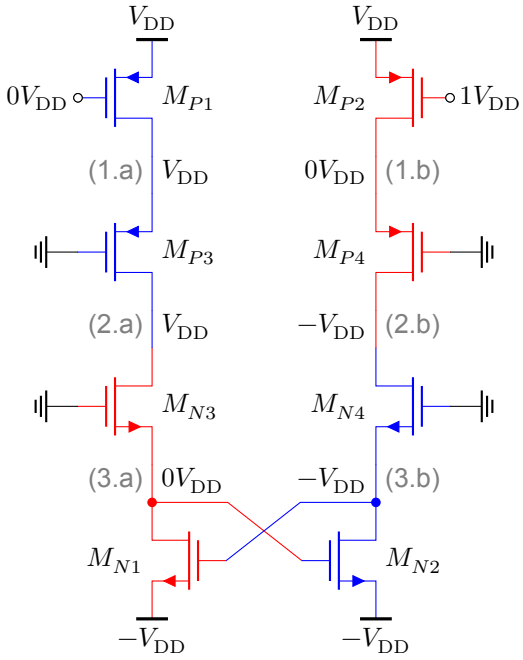



Figure 4.4: A simplified high to low level shifter and a description of operation.

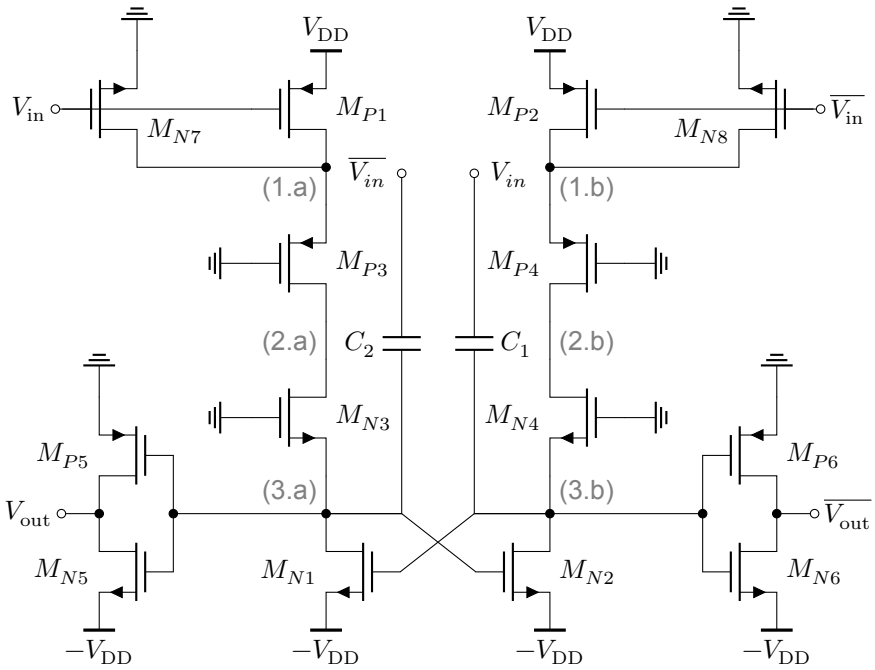



Figure 4.5: A simplified high to low level shifter and a description of operation.

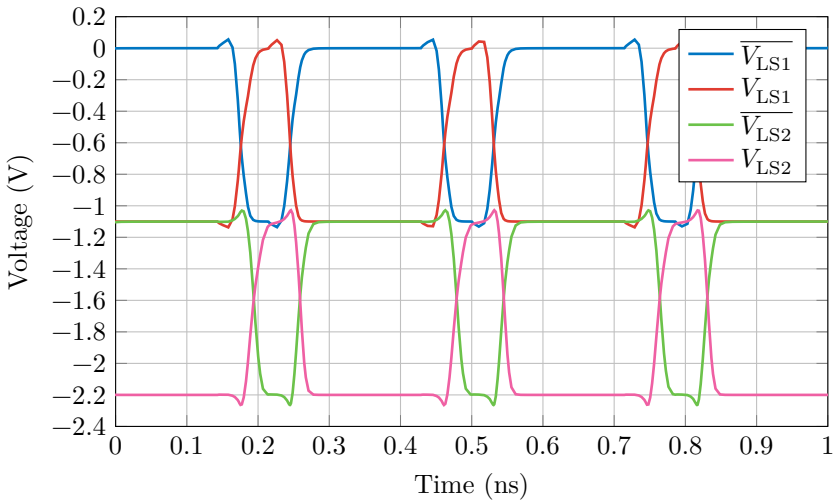



Figure 4.6: Output of two high to low level shifters.

integrated to account for this current mismatch [51, 52]. Furthermore, it is worth noting that the current mismatch could be minimized by balancing the pull-up and pull-down networks of the driver.

## 4.5. Implementation Challenges

The design of a driver for GaN-based RF-DACs essentially follows the same design procedure of a driver for LDMOS-based RF-DACs. But in contrast to the latter, access to the deep n-well and isolated P-well is crucial for drivers for GaN-based RF-DACs. Although the TSMC process design kit (PDK) used to implement the driver in Chapter 3 offers an NMOS with a deep n-well, its isolated p-well is inaccessible. Therefore, the level shifter from Section 4.3 is implemented with the 6-terminal NMOS and 5-terminal PMOS devices. These devices, however, are optimized for RF applications. Moreover, they do not offer the same flexibility in sizing and layout as the core thin-oxide devices.

Another challenging aspect is the number of power rails. The driver needs four power rails: $-2V_{\mathrm{DD}}$, $-V_{\mathrm{DD}}$, ground, and $V_{\mathrm{DD}}$. Supplying these voltages externally requires more pins/pads and more area to be allocated for routing the power rails. This complicates the design. The concept of charge recycling, introduced in Section 4.4, can be leveraged to get rid of $-V_{\mathrm{DD}}$-supply.

Lastly, the design of integrated circuits with negative voltage domains with a grounded p-type substrate is not very common. As a result, details concerning IC design aspects like electrostatic discharge (ESD) and latch-up are insufficiently reported. As matter of fact, the ESD protection circuit that operates under a negative voltage supply with a grounded p-type substrate was never reported before [48]. To prevent latch-up, the positioning of the $p^+$ guard rings around the deep n-well should be carefully considered [53]. Also, PMOS devices whose n-well is biased to $V_{\mathrm{DD}}$ should be placed far enough from the grounded deep n-well to avoid latch-up [53].

# 5

# Conclusion & Future Work

## 5.1. Conclusion

A hybrid-approach fully digital transmitter (DTX) for 5G mMIMO base stations combines high-speed digital CMOS with high-voltage high-power RF technology to achieve high integration and scalability. In this DTX, the RF-DAC comprises a CMOS controller and a gate-segmented LDMOS digital power amplifier (DPA) operating in digital class-C. The CMOS controller includes a driver capable of generating a sufficiently high voltage swing to activate the custom $V_T$ LDMOS segments.

The theoretical normalized output power and drain efficiency of digital class-C is analyzed. This analysis assumes trapezoidal drain currents to investigate the impact of the non-zero rise and fall times. The drain efficiency is maximized when the rise and fall times are minimized. In this case, the DPA operating in digital class-C has high drain efficiency. However, the DTX has low system efficiency because the CMOS driver activating the DPA is oversized and power-hungry.

The custom $V_T$ LDMOS technology can be activated by a gate-to-source voltage ($V_{GS}$) of 2.2 V. To achieve this, a driver implemented in TSCM 40 nm bulk CMOS is proposed. It comprises inverter chains, a level shifter, and a high-voltage output buffer. The level shifter has a low to high operation. It DC-shifts digital signals upwards by $1 \times V_{DD}$. The high-voltage output buffer is a house-of-cards (HoC) structure, which is a cascode inverter with assisting devices to address cascode device reliability issues.

A simulation of the DPA and its driver in Keysight ADS confirms the analysis of non-zero rise/fall time. A rise/fall time of around 20% of the RF cycle ($t_r = t_f = 0.2/f_c$) is most suitable in terms of form factor, power consumption, and ultimately system. Furthermore, while a 25% duty cycle simplifies DTX design, real segmented LDMOS performs better when activated by a 30% duty cycle. These findings inspire the driver's final design specifications.

The CMOS driver receives complementary digital signals (25% and 75% duty cycle) with a swing of $1 \times V_{DD}$ and generates an output signal with an effective duty cycle of 33% and a swing of $2 \times V_{DD}$. It is operated at 3.5 GHz and has a 150 fF capacitive load. The propagation delays $t_{pLH}$ and $t_{pHL}$ of the driver are 237.9 ps and 196.1 ps, respectively. Furthermore, the rise and fall times are 47.31 ps and 77.99 ps. The driver fits within a rectangle of 18.58 µm × 24.60 µm, a mere 30% of 40 µm × 40 µm allocated to the design. When unloaded, its overall power consumption averages 3.60 mW and 6.14 mW when loaded.

A simplified version of the DTX is simulated in ADS to evaluate output power, drain efficiency, and system efficiency. This simulation does not account for the entire DTX. It only contains a fitted model of the driver and models of the LDMOS with appropriate output matching and optimal load conditions. The latter is simulated using two models: (1) theoretical and (2) empirical. When compared to the gate voltage waveform, the duty cycle of the drain current waveform shrinks by nearly 1.3 percentage points. The DTX achieves an output power of 19.79 W/23.43 W, a drain efficiency of 67.28%/59.22% and system efficiency of 60.34%/54.48% with models 1 and 2, respectively.

As GaN technology continues to outperform LDMOS in the 5G market, it is worth considering when designing a high power RF-DAC for 5G base stations. However, there is no GaN technology suitable

for replacing the LDMOS in the RF-DACs, yet. Research has shown that a positive shift of the threshold voltage is possible with GaN HEMTs. The threshold voltage could be increased to −1.5 V. Finally, a CMOS driver capable of generating an output swinging between −2.2 V and 0 V is proposed here in anticipation of future developments.

## 5.2. Recommendations for Future Works

The proposed driver is implemented in TSMC 40 nm bulk CMOS. Although this process node offers good performance at the targeted operating frequency ($f_c$ = 3.5 GHz), this 40 nm CMOS technology limits the driver's performance in terms of its operating frequency and power consumption. Enfin, the system efficiency of DTX deteriorates. It is therefore worth considering more advanced process nodes for future implementations, e.g., the GlobalFoundaries 22 nm FD-SOI process technology.

Fully-depleted silicon-on-insulator (FD-SOI) technology offers an enhanced circuit performance. Notably, the operating frequency is substantially higher at the same energy, besides the energy-delay product (EDP) is better [54]. FD-SOI demonstrates a reduction in power consumption of around 50% at all voltages compared to bulk CMOS operating at the same speed [55]. A case study assuming similar operating conditions for both the 40 nm bulk CMOS and the 22 nm shows power savings of at least a factor 2. The system efficiency at 3.5 GHz full power goes from 60.79% to at least 63.88% based on simulation results with the non-empirical model (model 1) from Section 3.11.

# Bibliography


[1] P. Baudin, *Wireless Transceiver Architecture: Bridging RF and Digital Communications*. Chichester, United Kingdom: John Wiley & Sons, Dec. 2014.

[2] I. Chih-Lin, S. Han, and S. Bian, "Energy-efficient 5G for a greener future," *Nature Electronics*, vol. 3, pp. 182–184, Apr. 2020.

[3] L. Belkhir and A. Elmeligi, "Assessing ICT global emissions footprint: trends to 2040 & recommendations," *Journal of Cleaner Production*, vol. 177, pp. 448–463, Mar. 2018.

[4] L. Williams, B. K. Sovacool, and T. J. Foxon, "The energy use implications of 5G: reviewing whole network operational energy, embodied energy, and indirect effects," *Renewable and Sustainable Energy Reviews*, vol. 157, p. 112033, Apr. 2022.

[5] R. B. Staszewski, "Digital RF and digitally-assisted RF (invited)," in *Proc. IEEE Intern. Symp. on Radio-Frequency Integration Technology*, IEEE, Nov. 2011.

[6] R. B. Staszewski, J. L. Wallberg, S. Rezeq, C.-M. Hung, O. E. Eliezer, S. K. Vemulapalli, C. Fernando, K. Maggio, R. Staszewski, N. Barton, M.-C. Lee, P. Cruise, M. Entezari, K. Muhamma, and D. Leipold, "All-digital PLL and transmitter for mobile phones," *IEEE Journal of Solid-State Circuits*, vol. 40, pp. 2469–2482, dec 2005.

[7] R. B. Staszewski, K. Muhammad, D. Leipold, C.-M. Hung, Y.-C. Ho, J. L. Wallberg, C. Fernando, K. Maggio, R. Staszewski, T. Jung, J. Koh, S. John, I. Y. Deng, V. Sarda, O. Moreira-Tamayo, V. Mayega, R. Katz, O. Friedman, O. E. Eliezer, E. de Obaldia, and P. T. Balsara, "All-digital TX frequency synthesizer and discrete-time receiver for Bluetooth radio in 130-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 39, pp. 2278–2291, Dec. 2004.

[8] R. B. Staszewski, *Digital deep-submicron CMOS frequency synthesis for RF wireless applications*. PhD thesis, University of Texas, Dallas, TX, Aug. 2002.

[9] M. S. Alavi, J. Mehta, and R. B. Staszewski, *Radio-Frequency Digital-to-Analog Converters*. Amsterdam: Elsevier, 2017.

[10] J. S. Walling, S.-M. Yoo, and D. J. Allstot, "Digital power amplifier: A new way to exploit the switched-capacitor circuit," *IEEE Communications Magazine*, vol. 50, pp. 145–151, Apr. 2012.

[11] T. L. Marzetta, "Massive MIMO: An Introduction," *Bell Labs Technical Journal*, vol. 20, pp. 11–22, 2015.

[12] E. G. Larsson, O. Edfors, F. Tufvesson, and T. L. Marzetta, "Massive MIMO for next generation wireless systems," *IEEE Communications Magazine*, vol. 52, pp. 186–195, Feb. 2014.

[13] S. M. Alavi, *All-Digital I/Q RF-DAC*. PhD thesis, Delft University of Technology, Delft, Netherlands, Jun. 2014.

[14] R. J. Bootsman, "Power RF-DAC: the design of a LDMOS class-E SMPA DRAC with a CMOS driver," Master's thesis, Delft University of Technology, Delft, Netherlands, Jan. 2018.

[15] R. J. Bootsman, D. P. N. Mul, Y. Shen, M. Hashemi, R. M. Heeres, F. van Rijs, M. S. Alavi, and L. C. N. de Vreede, "High-power digital transmitters for wireless infrastructure applications (a feasibility study)," *IEEE Trans. on Microwave Theory and Techniques*, vol. 70, pp. 2835–2850, May 2022.

[16] S. C. Cripps, *RF Power Amplifiers for Wireless Communications*. Boston, MA: Artech House, May 2006.

[17] A. Grebennikov, *RF and Microwave Power Amplifier Design*. New York: McGraw Hill, 2nd ed., Feb. 2015.

[18] B. Razavi, *RF Microelectronics*. Upper Saddle River, NJ: Prentice Hall, Sep. 2011.

[19] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge, UK: Cambridge University Press, 2 ed., Dec. 2003.

[20] G. Gonzalez, *Microwave transistor amplifiers: Analysis and Design*. Upper Saddle River, NJ: Prentice Hall, 2 ed., 1997.

[21] E. McCune, "A technical foundation for RF CMOS power amplifiers: part 3: power amplifier 3-port characteristics," *IEEE Solid-State Circuits Magazine*, vol. 8, pp. 44–50, Jan. 2016.

[22] E. McCune, "The gain game: using the four principal amplifier gain metrics," *IEEE Microwave Magazine*, vol. 19, pp. 134–139, nov 2018.

[23] M. Vigilante, E. McCune, and P. Reynaert, "To EVM or two EVMs?: an answer to the question," *IEEE Solid-State Circuits Magazine*, vol. 9, pp. 36–39, Aug. 2017.

[24] L. C. Nunes, P. M. Cabral, and J. C. Pedro, "AM/PM distortion physical origins in Si LDMOS Doherty power amplifiers," in *Proc. IEEE MTT-S Intern. Microwave Symp.*, May 2016.

[25] E. McCune, "A technical foundation for RF CMOS power amplifiers: part 1: key power amplifier issues," *IEEE Solid-State Circuits Magazine*, vol. 7, pp. 81–85, Sep. 2015.

[26] R. J. Bootsman, D. P. N. Mul, Y. Shen, R. M. Heeres, F. van Rijs, M. S. Alavi, and L. C. N. de Vreede, "An 18.5 w fully-digital transmitter with 60.4 % peak system efficiency," in *Proc. IEEE/MTT-S Intern. Microwave Symp.*, Aug. 2020.

[27] L. de Vreede, S. Alavi, R. Bootsman, M. Beikmirza, D. Mul, R. Heeres, and F. van Rijs, "Digital transmitter with high power output." Netherlands Patent NL2024903, Sep., 19, 2021.

[28] D. P. N. Mul, R. J. Bootsman, Q. Bruinsma, Y. Shen, S. Krause, R. Quay, M. J. Pelk, F. van Rijs, R. M. Heeres, S. Pires, M. Alavi, and L. C. N. de Vreede, "Efficiency and linearity of digital "class-C like" transmitters," in *Proc. European Microwave Confer. (EuMC)*, Jan. 2021.

[29] R. Bootsman, Y. Shen, D. Mul, M. Rousstia, R. Heeres, F. van Rijs, J. Gajadharsing, M. S. Alavi, and L. C. N. de Vreede, "A 39 W fully digital wideband inverted Doherty transmitter," in *Proc. IEEE MTT-S Intern. Microwave Symp.*, Jun. 2022.

[30] H. Xu, Y. Palaskas, A. Ravi, M. Sajadieh, M. A. El-Tanani, and K. Soumyanath, "A flip-chip-packaged 25.3 dBm class-D outphasing power amplifier in 32 nm CMOS for WLAN application," *IEEE Journal of Solid-State Circuits*, vol. 46, pp. 1596–1605, Jul. 2011.

[31] H. M. Nguyen, J. S. Walling, A. Zhu, and R. B. Staszewski, "A mm-wave switched-capacitor RF-DAC," *IEEE Journal of Solid-State Circuits*, vol. 57, pp. 1224–1238, Apr. 2022.

[32] J. Rabaey, A. Chandrakasan, and B. Nikolić, *Digital Integrated Circuits: A Design Perspective*. Upper Saddle River, NJ: Pearson, 2003.

[33] L. Dai and R. Harjani, "Design of low-phase-noise CMOS ring oscillators," *IEEE Trans. on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 49, pp. 328–338, May 2002.

[34] M. Hashemi, Y. Shen, M. Mehrpoo, M. S. Alavi, and L. C. N. de Vreede, "An intrinsically linear wideband polar digital power amplifier," *IEEE Journal of Solid-State Circuits*, vol. 52, pp. 3312–3328, Dec. 2017.

[35] B. Serneels, M. Steyaert, and W. Dehaene, "A high speed, low voltage to high voltage level shifter in standard 1.2 V 0.13 µm CMOS," *Analog Integrated Circuits and Signal Processing*, vol. 55, pp. 85–91, Mar. 2008.

[36] B. Serneels and M. Steyaert, *Design of High Voltage xDSL Line Drivers in Standard CMOS*. Dordrecht, Netherlands: Springer, 2008.

[37] P.-I. Mak and R. P. Martins, "High-/mixed-voltage RF and analog CMOS circuits come of age," *IEEE Circuits and Systems Mag.*, vol. 10, pp. 27–39, Nov. 2010.

[38] J. Fritzin, C. Svensson, and A. Alvandpour, "A +32 dBm 1.85 GHz class-D outphasing RF PA in 130nm CMOS for WCDMA/LTE," in *Proc. Eur. Conf. on Solid-State Circuits (ESSCIRC)*, pp. 127–130, IEEE, Sep. 2011.

[39] L. G. Salem, J. F. Buckwalter, and P. P. Mercier, "A recursive switched-capacitor house-of-cards power amplifier," *IEEE Journal of Solid-State Circuits*, vol. 52, pp. 1719–1738, Jul. 2017.

[40] N. H. E. Weste and D. Money Harris, *CMOS VLSI Design*. Boston, MA: Pearson, 4 ed., 2011.

[41] S. Henzler, *Time-to-Digital Converters*. Dordrecht, Netherlands: Springer, 2010.

[42] S. Sidiropoulos, D. Liu, J. Kim, G. Wei, and M. Horowitz, "Adaptive bandwidth DLLs and PLLs using regulated supply CMOS buffers," in *Proc. Symp. on VLSI Circuits*, Jun. 2000.

[43] D. W. Runton, B. Trabert, J. B. Shealy, and R. Vetury, "History of GaN: high-power RF gallium nitride (GaN) from infancy to manufacturable process and beyond," *IEEE Microwave Magazine*, vol. 14, pp. 82–93, May 2013.

[44] A. Inoue, "Millimeter-wave GaN devices for 5G: massive MIMO antenna arrays for sub-6-GHz and mm-wave bandwidth," *IEEE Microwave Magazine*, vol. 22, pp. 100–110, May 2021.

[45] E. Dogmus, S. Sejil, and P. Chiu, "GaN RF market: applications, players, technology, and substrates 2021," Jun. 2021. Yole Développement.

[46] B.-J. Godejohann, *GaN-based High Electron Mobility Transistors with high Al-content barriers*. PhD thesis, University of Freiburg, Freiburg, Germany, Sep. 2017.

[47] Y. Ismail, *High-Voltage Generation and Drive in Low-Voltage CMOS Technology*. PhD thesis, University of California, Los Angeles, 2015.

[48] R.-K. Chang and M.-D. Ker, "Design of high-voltage-tolerant power-rail ESD protection circuit for power pin of negative voltage in low-voltage CMOS processes," *IEEE Trans. on Electron Devices*, vol. 67, pp. 40–46, Jan. 2020.

[49] C.-C. Hsieh and M.-D. Ker, "Monopolar biphasic stimulator with discharge function and negative level shifter for neuromodulation SoC integration in low-voltage CMOS process," *IEEE Trans. on Biomedical Circuits and Systems*, vol. 15, pp. 568–579, Jun. 2021.

[50] K. Blutman, A. Kapoor, A. Majumdar, J. G. Martinez, J. Echeverri, L. Sevat, A. P. van der Wel, H. Fatemi, K. A. A. Makinwa, and J. P. de Gyvez, "A low-power microcontroller in a 40-nm CMOS using charge recycling," *IEEE Journal of Solid-State Circuits*, vol. 52, pp. 950–960, Apr. 2017.

[51] Y. Liu, P.-H. Hsieh, S. Kim, J.-s. Seo, R. Montoye, L. Chang, J. Tierno, and D. Friedman, "A 0.1pJ/b 5-to-10Gb/s charge-recycling stacked low-power I/O for on-chip signaling in 45nm CMOS SOI," in *Proc. Intern. Conf. on Solid-State Circuits*, IEEE, Feb. 2013.

[52] S. Rajapandian, K. L. Shepard, P. Hazucha, and T. Karnik, "High-voltage power delivery through charge recycling," *IEEE Journal of Solid-State Circuits*, vol. 41, pp. 1400–1410, Jun. 2006.

[53] Z.-H. Jiang and M.-D. Ker, "The parasitic latch-up path from substrate $p^+$ guard ring to the NMOS in deep n-well operating with negative voltage sources," *IEEE Electron Device Letters*, vol. 43, pp. 604–606, Apr. 2022.

[54] J. Makipaa and O. Billoint, "FDSOI versus BULK CMOS at 28 nm node which technology for ultra-low power design?," in *Proc. IEEE Inter. Symp. on Circuits and Systems*, IEEE, May 2013.

[55] B. Pelloux-Prayer, M. Blagojevic, O. Thomas, A. Amara, A. Vladimirescu, B. Nikolic, G. Cesana, and P. Flatresse, "Planar fully depleted SOI technology: the convergence of high performance and low power towards multimedia mobile applications," in *Proc. IEEE Faible Tension Faible Consommation*, IEEE, Jun. 2012.

CMOS Drivers for RF-DACs

TU Delft Delft University of Technology

ELCA Electronic Circuits and Architectures

Challenge the future