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***Abstract*— This paper presents a scalable cryogenic readout solution for Superconducting Nanowire Single-Photon Detectors (SNSPDs) tailored for the readout of color-center-based qubits. The readout circuit, wire-bonded directly to the SNSPD, utilizes high input impedance to boost the signal amplitude, hence reducing the power consumption, and active quenching to prevent the latching induced by the high impedance. Fabricated in 40-nm CMOS in a 0.14-mm^2 active area, the proposed system demonstrates competitive performance at 0.1 K, featuring low jitter [$<$60 ps Full Width at Half Maximum (FWHM)], high speed (dead time $\approx$5 ns) and low dark count rate ($<$1 Hz), while dissipating only 20 µW. Such an ultra-low power and compact area enables the readout integration within a large-scale color-center quantum computer.**

***Index Terms*—SNSPD, cryo-CMOS, quantum computing.**

I. Introduction

Although Quantum Computers (QCs) promise unprecedented speed-up compared to classical computers, today's QC prototypes have not yet demonstrated enough computational power for practical applications. Among the several hurdles in scaling up QCs, developing a scalable electronic interface to control and read out the cryogenic qubits is still a major challenge. Compared to other qubit platforms, color-center qubits, such as the Nitrogen-Vacancy (NV) centers in diamond, have shown great potential for scalability thanks to their high-fidelity quantum operations, relatively higher operating temperatures ($\sim$1 K) and the ability to interact remotely via optical links. The increased cooling power available in cryostats at higher temperatures, along with the ability to space qubits by a few millimeters, facilitates the 3D integration of qubits and their cryogenic electro-optical interface (Fig. 1) [1]. While some of the required cryogenic CMOS (cryo-CMOS) functionalities have already been demonstrated [2], others, such as switch driving and readout, remain unexplored. In this paper, we present for the first time the successful integration of a single-photon readout architecture essential for NV-center readout and entanglement. Such a readout must have high detection efficiency at a count rate beyond 20 MHz to ensure high computational speed by reducing photon losses that can cause repeated quantum operations. Low timing jitter [$<$100 ps Full Width at Half Maximum (FWHM)] is essential to reduce false detection by photon time filtering. Furthermore, the area and the power consumption of the detector and its cryo-CMOS interface must be minimized to comply with the integration requirements. Superconducting Nanowire Single-Photon Detectors (SNSPDs) meet these requirements by providing high detection efficiency and precise photon timing at Cryogenic Temperatures (CT) compatible with color-center operation [3]. SNSPDs are typically read out by cryogenic or room-temperature Low-Noise Amplifiers (LNAs) connected by a long coaxial cable, thus requiring 50-Ω input matching [4]. Low input impedance attenuates the signal, making the readout amplifier dissipate significant power due to increased noise and gain requirements. Since the co-integration shown in Fig. 1 relaxes the input matching requirement, a high input impedance can be adopted to ease the amplifier specification. Yet, a too high SNSPD load impedance can cause the detector to latch, i.e., the SNSPD is locked in the triggered state and cannot reset [5]. To circumvent latching, an active quenching circuit can be used to force the SNSPD to reset [6]. Despite the potentiality of this approach, prior work still required a power consumption beyond 100 µW for specifications comparable to this work's target application, even when adopting low-noise SiGe BiCMOS technology.

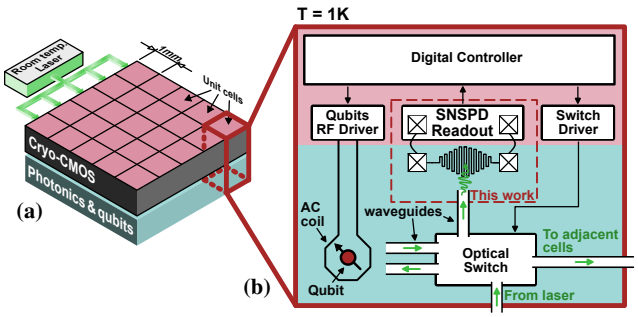

Fig. 1. Architecture of a quantum computer based on color centers: *a)* 3D-integrated cryo-CMOS electrical interface, photonic interface and qubits; *b)* Unit cell with one color center, qubit driver, switch driver, optical switch, and single-photon detector (one per unit cell, with one readout circuit per detector).

To bridge the gap between prior work and the requirements of color-center QCs, this work presents a fully integrated 40-nm cryo-CMOS readout circuit that achieves a 5 × reduction in power consumption compared to the state-of-the-art. By optimizing the load resistance, the active quenching resistance, and the recovery time, the proposed design minimizes the required readout gain and power, while maintaining jitter and dead time within limits.

II. System Design

A. SNSPD design

The SNSPD, with kinetic inductance L_k, is biased just below its critical current I_c, so that the absorption of an incident photon can create a hotspot. This localized region temporarily disrupts superconductivity, causing the SNSPD to transition into a resistive state at that spot. The bias current flowing through the nanowire then generates heat via the Joule effect, which expands the resistive region and increases the internal resistance $R_n(t)$ until it reaches its maximum

$$R_{n,max} = \rho_n \times \frac{L_{wire}}{A_{wire}}, \tag{1}$$

where ρ_n is the resistivity of the wire, while L_{wire} and A_{wire} are the length and cross-section of the wire, respectively. The time constant $\tau_h = L_k/R_{n,max}$ associated with the hotspot growth is typically in the order of hundreds of picoseconds [7], [6]. When the resistive region is formed, the SNSPD bias current I_{bias} (typically in the order of 10 µA to 20 µA) produces a voltage drop on the parallel of the SNSPD resistance $R_{n_{max}}$ and the readout input impedance R_L, resulting in a voltage pulse at the output of the SNSPD. After detection, the SNSPD returns to its superconducting state with a recovery time constant $\tau_r = L_k/R_L$ [5]. However, if R_L is too large, the bias current keeps flowing mostly in the SNSPD generating excessive Joule heating that prevents it from resetting, leading to latching. Thus, while a large R_L would be preferred to optimize the detection performance and accelerate the recovery, it may prevent the reset. To break this trade-off, active quenching can be introduced, allowing for the optimal choice of R_L [6].

The fabricated SNSPD consists of a NbTiN nanowire on top of a stoichiometric Si_3N_4, achieved via Low-Pressure Chemical Vapor Deposition (LPCVD), a thermal SiO_2 layer, and a silicon substrate. Detector size (see Fig. 3) and material properties indicate a kinetic inductance near 1 µH, verified by reset time analysis using a passive 50-Ω termination, as elaborated in the results section. Preliminary tests show the critical current at the operating temperature to be around 22 µA.

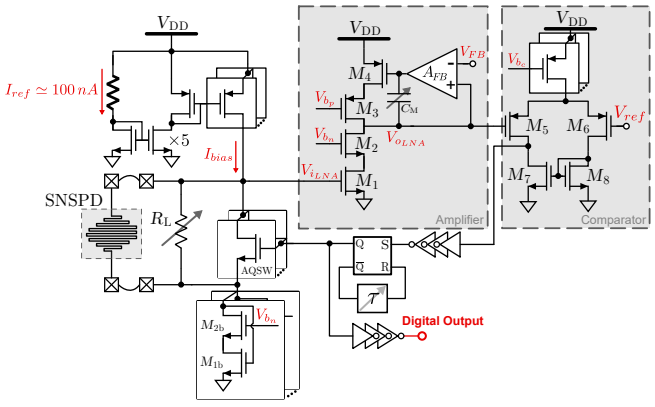

Fig. 2. Schematic of the cryo-CMOS readout circuit.

B. CMOS readout circuit

Fig. 2 illustrates the schematic of the cryo-CMOS readout design. The CMOS circuit provides the SNSPD biasing current I_{bias}, and amplifies the SNSPD pulse, which is subsequently detected by a comparator. After a detection event, the SNSPD is reset by an active-quenching switch (AQSW). A balance is needed when selecting the input resistance R_L: increasing R_L reduces its thermal noise, improves the readout gain and reduces the SNSPD rising time constant ($\tau_R \approx \frac{L_K}{R_{n_{peak}}+R_L}$, with $R_{n_{peak}}$ being the off-superconductivity resistance of the SNSPD at the detection instant), thus improving the total jitter of the readout chain. However, a high R_L might cause the SNSPD to latch, necessitating the activation of the quenching switch to recover the superconductivity by redirecting the SNSPD current. To experimentally explore this trade-off, R_L can be selected from a set of 5 resistors (50 Ω, 500 Ω, 2 kΩ, 10 kΩ, 100 kΩ) and their parallel combinations.

With the nominal 100 kΩ, the SNSPD signal requires 30 dB gain to reliably trigger the comparator and reduce the impact of the comparator noise. This can be achieved by a single-stage cascoded common-source amplifier (M_{1-4}) biased with ≈7 µA to meet the jitter specifications. A slow feedback amplifier (A_{FB}), consisting of a PMOS differential input pair loaded by an NMOS current mirror, ensures proper bias of the amplifier active load M_{3-4}, and sets the amplifier DC output $V_{o_{LNA}}$≈400 mV using an externally provided reference V_{FB}. A_{FB} must detect the DC drift at the amplifier output while maintaining a narrow bandwidth to filter out high-frequency components. This is crucial for preventing LNA bias drift at high event rates. A programmable Miller compensation capacitance C_M ensures the loop stability. Although this feedback loop slightly reduces the amplifier gain, it does not affect the detection or the jitter. To ensure correct biasing of the V_{gs} of M_1, a 7-bit programmable current mirror ($M_{1b,2b} - M_{1,2}$) reuses the SNSPD current I_{bias}, which is set by a 7-bit PMOS current DAC with a 0.5 µA LSB, thus reducing the total current consumption. The bias current of the SNSPD and the amplifier can then be independently set.

The comparator consists of a PMOS differential input pair

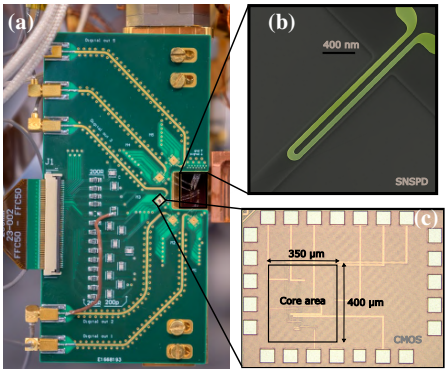

Fig. 3. Measurements setup: *a)* Test PCB mounted on the cold finger of the refrigerator; *b)* Micrograph of the SNSPD. *c)* Micrograph of the CMOS readout chip.

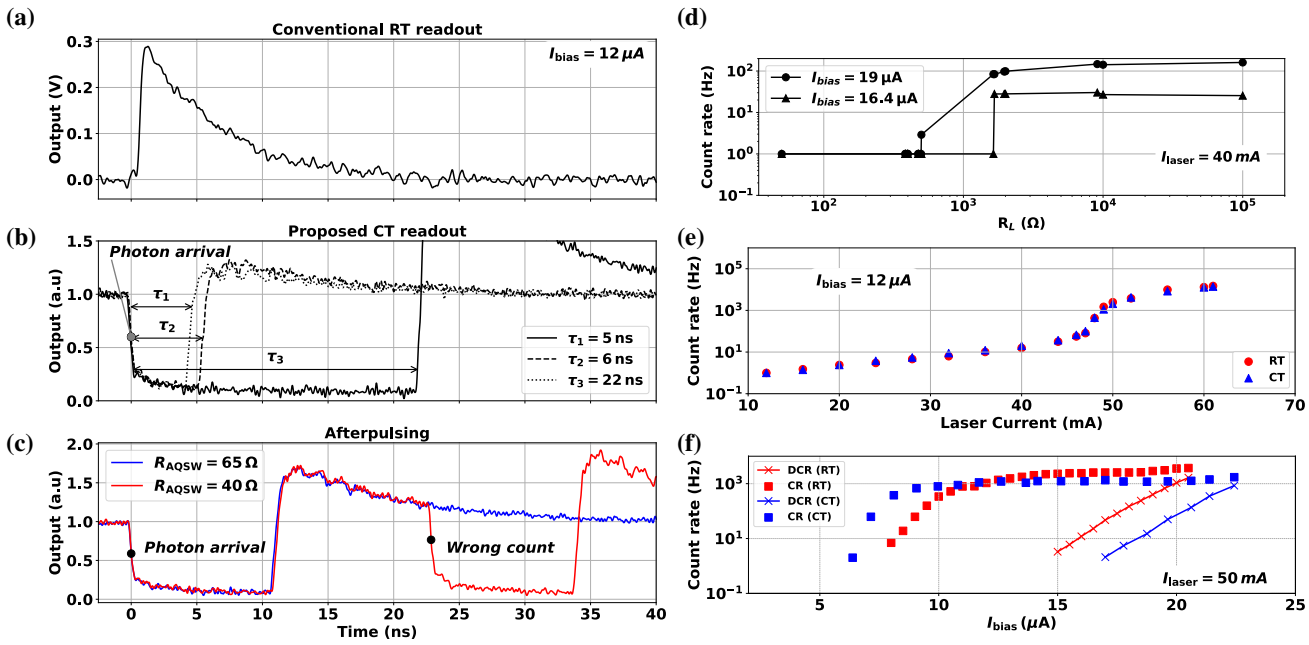

Fig. 4. Measurement results. All the measurements have been done with the same settings, namely $R_L = 100\,\mathrm{k}\Omega$ and $R_{AQSW} = 65\,\Omega$, unless differently specified: *a)* Analog waveform using the RT readout. *b)* Normalized cryo-CMOS digital output showing reset tunability. The digital output of the chip exhibits reversed polarity, meaning that the falling edge of the signal corresponds to the detection event. Overshoot and ringing on the rising edge are due to the combined effect of a non-matched driver driving a $\sim$4 m-long 50-Ω line with a 50-Ω load and an excessive external resistance on the output driver supply. *c)* Impact of active quenching resistance on afterpulsing. *d)* Count rate vs. load resistance. *e)* Count rate vs. laser current showing immunity to false counts. *f)* CR and DCR vs. bias current for cryo-CMOS and RT readout.

with an NMOS current-mirror load. For a given total current, the comparator speed is optimized by sizing the current in $M_{6,8}$ $4\times$ smaller than the current in $M_{5,7}$, which directly affects the signal path. Choosing a sufficiently low comparator threshold is essential to detect all photons at low SNSPD bias while avoiding noise-induced false counts. Testing flexibility is improved through external adjustability of the trigger voltage V_{ref}. The comparator buffered output is recorded by a SR latch. The latch Q output serves both as the readout output and the driving signal for AQSW, whereas the $\overline{Q}$ output drives a current-starved inverter-based delay chain that resets the latch. This delay chain controls the output pulse width and defines the AQSW on-time during the SNSPD post-detection cool-down. The delay can be programmed from 5 ns to 75 ns since a too short delay can lead to non-proper quenching while a longer delay limits the count rate. The AQSW employs 7 programmable parallel NMOS with binary-weighted widths, adjusting its resistance R_{AQSW} from $40\,\Omega$ to $6\,\mathrm{k}\Omega$. This enables analyzing the impact of R_{AQSW}: on one hand, a large switch resistance keeps the bias current flowing into the SNSPD, making the quenching ineffective; on the other hand, a small resistance coupled with an insufficient quenching time can lead to an excessive current overshoot resulting in afterpulsing. The NMOS AQSW employs cryogenic-aware forward body biasing [8] by connecting the body contact to an external 1-V bias to offset the cryogenic V_{th} increase, ensuring sufficient overdrive for complete switch activation during quenching.

III. Experimental Results

Fabricated in a 40-nm CMOS process with an active area of $0.14\,\mathrm{mm}^2$, the circuit draws $29\,\mu\mathrm{A}$ ($38\,\%$ for the SNSPD, $42\,\%$ for the amplifier, $20\,\%$ for the comparator and the digital section) from a 1.1-V supply. A preliminary performance evaluation in a liquid Helium bath with an emulated SNSPD pulse generated by a Tektronix® AWG5014C showed a jitter of approximately $60\,\mathrm{ps}_{\mathrm{FWHM}}$ at $4\,\mathrm{K}$.

Thanks to the low power consumption, the system could be operated at sub-K temperature for the following tests, so as to push the SNSPD performance and highlight the capability of the cryo-CMOS readout. The CMOS chip is mounted on a PCB and wirebonded to the SNSPD chip (Fig. 3). The SNSPD chip is mounted on a copper cold finger attached to the bottom flange of a BlueFors® SD cryostat. Multiple detectors have been integrated on the same chip: One SNSPD interfaces with the cryo-CMOS readout, while the other connects via a coaxial line to a conventional Room-Temperature (RT) amplification scheme (employing two ZFL-1000LN+ amplifiers) used for reference. All I/O's of the chip are routed to the RT instrumentation via a high-density FFC connector and a flex-PCB; the instrumentation includes an SPI module for programming the chip's shift registers, LDO regulators, and a Keithley® 2636B SourceMeter to supply the SNSPD used for the RT readout. The cryo-CMOS chip directly supplies the bias current for its own SNSPD. For proof-of-concept tests, the SNSPD is excited through flood illumination by a CW 520-nm laser with adjustable power.

TABLE I
PERFORMANCE COMPARISON OF CRYOGENIC SNSPD READOUT

Parameter	Peng et al. [9]	Niu et al. [10]	Li et al. [7]	Ravindran et al. [6]	This work
Technology	130-nm SiGe BiCMOS	130-nm SiGe BiCMOS	130-nm SiGe BiCMOS	130-nm SiGe BiCMOS	40-nm CMOS
Temperature (K)	3.6	4.2	4.2	2.8	0.1
Active Quenching	No	No	No	Yes	Yes
Internal SNSPD Bias	No	No	No	No	Yes
Dark Count rate (Hz)	–	–	–	–	<1 [a]
Area (mm^2)	0.038	0.5	0.073 [b]	0.46	0.14
Power (µW)	8200 [c]	1800 [c]	3100 [c]	100 [c]	20 (+13 µW SNSPD bias)

[a] At the optimal detection efficiency bias point. [b] Core area only. [c] SNSPD bias not included.

The cryo-CMOS output waveform is recorded via a Lecroy waveMaster® 813Zi-B oscilloscope.

Fig. 4(a) presents the SNSPD output acquired by the RT readout. In contrast, Fig. 4.(b) showcases the digital output produced by our custom cryogenic readout circuit. This interface enables adjustable reset times ranging from 5 ns to 72 ns, offering dynamic control over the detector's maximum count rate and allowing the system to adapt to varying photon flux conditions. Thanks to this fast quenching operation, the readout could potentially support count rates up to 200 MHz. The impact of R_{AQSW} on afterpulsing behavior is depicted in Fig. 4(c). Three distinct operational regimes emerge: when R_{AQSW} is too low (R_{AQSW}=40 Ω), a sharp reinjection of the entire bias current at the end of the recovery phase leads to pronounced afterpulses, as clearly visible in the figure. Conversely, when R_{AQSW} is too high (not shown), the circuit behaves similarly to a high-impedance readout, causing latching and preventing proper operation. An optimal intermediate resistance value (R_{AQSW}=65 Ω) results in clean output pulses without afterpulses, thus demonstrating stable and efficient quenching behavior.

Fig. 4(d) underscores the importance of an appropriate input load for effective signal discrimination. An excessively low input load produces output pulses with amplitudes insufficient to trigger the digital discriminator, resulting in a sudden and sharp drop in the count rate. This highlights the necessity of fine-tuning the load conditions to maintain detection fidelity.

Fig. 4(e) further validates the system's reliability by illustrating photon detection at varying optical powers. As the laser current – and consequently the optical power – is increased, the count rate remains consistent between the RT readout and the cryo-CMOS readout for the same bias current. This confirms that the detected events originate solely from genuine photon absorption in the SNSPD, with no spurious counts arising from circuit-level artifacts such as afterpulsing. This result substantiates the robustness of the readout architecture under realistic operating conditions.

Finally, both the count rate (CR) and the dark count rate (DCR) for the full range of SNSPD bias currents show a similar response trend for the cryo-CMOS and RT readout (Fig. 4.f). The observed variations between RT and CT are attributed to the fabrication-related spread between the two individual detectors used for the RT readout and the cryo-CMOS readout, respectively. Those results indicate that the proposed readout does not limit the SNSPD performance, thereby validating its suitability for low-power cryogenic quantum applications without compromising performance. When compared to state-of-the-art cryogenic SNSPD readouts in Table I, this works achieves the lowest power dissipation.

IV. CONCLUSIONS

This work demonstrates a low-power cryo-CMOS circuit that uses a high-impedance input together with active quenching for reading out SNSPDs. The measurements demonstrate that the fabricated SNSPDs can be biased and read out to perform high-fidelity photon detection. Thanks to its compactness and its low power, the proposed solution can be efficiently integrated into scalable color-center quantum computer, leaving a significant power budget available for other more power-demanding critical blocks.

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