Wideband Hybrid-Class Power Amplifier for Base Station Applications Using LDMOS with Envelope Tracking System

By
T. Zhang

TU-Delft Mentors:
Dr. ing. L.C.N. de Vreede
S.M. Alavi

NXP Mentors:
Edmund Neo
John Gajadharsing

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Abstract

Conventional RF power amplifiers are normally designed for peak efficiency at maximum output power. However, for WCDMA application, the power amplifier often operates at 6-8 dB power back-off. Consequently, when the power is backed-off from its peak point, the efficiency of conventional power amplifier drops sharply.

The envelope elimination and restoration (EER) and envelope tracking (ET) systems are two of the most promising techniques that can provide high efficiency at power back-off point. In this project, a RF power amplifier optimized for average efficiency according to the PDF of WCDMA signal has been designed using NXP generation 7 LDMOS.

In addition, to meet the increasing demand for wireless communication terminals to handle wideband operation, a 1GHz bandwidth power amplifier optimized for efficiency at power back-off has been designed and fabricated. The measurement results are proved to have a good agreement with simulation results.

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Content

Introduction

The function of a power amplifier is to take a RF input signal and transfer it to an output signal with significantly larger amplitude. This is only possible at the cost of DC power, which is converted to the RF / microwave domain. There are a great variety of different PA operating classes in use, e.g. class-A, class-B, class-C and etc., as well as, high complexity amplifier architectures that can improve the efficiency-linearity trade-off of the power amplifier (e.g. envelope elimination, envelope tracking, Doherty, out-phasing etc.).

Recently, due to the development of high data rate wireless systems, the power amplifier is more and more required to have different operation modes and operating frequencies (e.g. WCDMA, WiMAX etc.). So, wideband operation has now become an important design parameter as well. In this thesis, we aim for an octave bandwidth power amplifier, optimized for supply voltage modulation. In view of this the outline of the thesis is as follows.

In chapter 1, we discuss the principles of class A/AB/B/C/E and F operation and introduce some higher complexity amplifier concepts currently in use to improve the efficiency performance in power back-off operation.

In chapter 2 we will introduce the principles of class-J operation. Class-J is a relative of new class of device operation, which is gaining interest due to its better wideband capabilities.

Since the focus of this project is to design a power amplifier suitable for an envelope tracking system, using NXP's latest generation 7 of LDMOS technology, in chapter 3 we invest, which class of device operation is the most suitable for application. With this information an initial power amplifier design has been defined.

In chapter 4, wideband amplifier design is introduced; three different versions with slightly different bandwidths are evaluated for their performance.

In chapter 5, the final design, layout and testing results are presented of the octave wideband power amplifier.

Chapter 1 Principle of class A/AB/B/C/E/F

In this chapter, we well discuss the principles of some basic operation classes of power amplifiers, as well as the concept of amplifier operation in power back-off. The principles of envelope elimination and restoration and envelope tracking system will also be introduced in this chapter.

Operation classes for power amplifiers:

For different ways of device operation, people classify the power amplifiers to different classes. Class A/AB/B/C can be classified to one category. When the power amplifier operates at class A/B/C/AB, the transistor operates like a current source. Class E/F/J can be classified to another category. In these classes the transistor operates like a switch.

Section1: Reduced conduction angle power amplifier

Let's first talk about the class A/B/C/AB power amplifier. The difference of these classes is the conduction angle (figure 1.1).

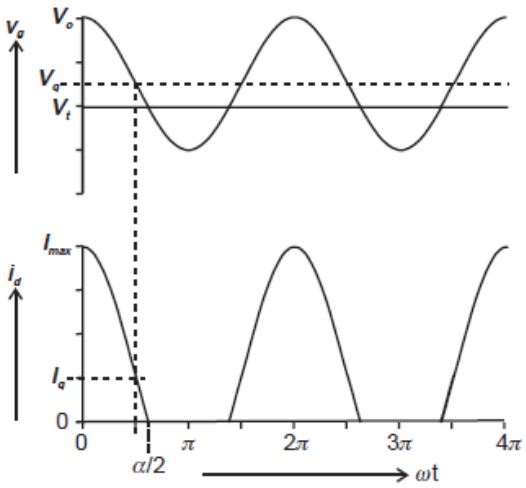


Figure 1.1 Reduced conduction angle when operating as a power amplifier α represents the conduction angle of power amplifier [1]

Class	Gate bias point	Current	Conduction angle
A	0.5	0.5	2pi
AB	0-0.5	0-0.5	Pi-2pi
B	0	0	pi
C	<0	0	0-pi

Table 1.1 Bias point and conduction angle of different classes (the signal voltage and current swing are normalized to 1) [1]

Class-A:

From these classes, class-A has the highest linearity and the transistor is equivalent to a current source. The drain current and voltage waveforms of class-A operation are given in figure 1.2:

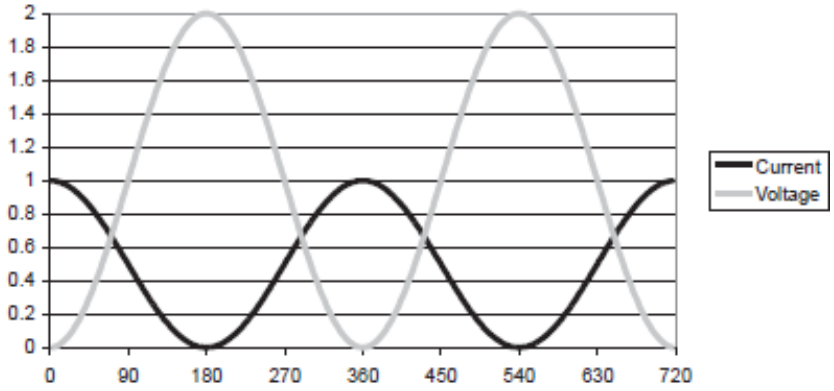


Figure 1.2 (b) Drain voltage and Drain current in class-A operation [1]

In order to enable the power amplifier operate in its linear region, the amplifier's gate and drain bias voltage should be chosen properly. The swing of the drain current for class-A operation should be between zero and Imax (with Imax being the saturation current of the transistor.). The swing of the drain voltage should be between zero and breakdown voltage of the device. The conduction angle is 2π for class-A operation means the device is on all the times. It also means that the device loses power all the times.

Let's calculate the maximum efficiency and output power of class-A operation:

The drain current for an amplifier with reduced conduction angle:

$$i_d(\theta) = I_q + I_{pk}\cos\theta, -\alpha/2 < \theta < \alpha/2;$$

$$= 0, -\pi < \theta < -\alpha/2; -\alpha/2 < \theta < \pi \qquad [1] \qquad (1)$$

Where id is the drain current, Iq is the quiescent current, Ipk is the amplitude of drain current, Imax is the peak value of drain current, α is the conduction angle.

$$\cos(\alpha/2) = -\frac{I_q}{I_{pk}} \quad \text{and} \quad I_{pk} = \mathrm{I}_{max} - I_q \qquad (2)$$

So,
$$i_d(\theta) = \frac{\mathrm{I}_{max}}{1-\cos(\alpha/2)}(\cos\theta - \cos(\alpha/2)) \qquad (3)$$

The DC component is as follows:

$$I_{dc} = \frac{1}{2\pi} \int_{-\alpha/2}^{\alpha/2} \frac{I_{max}}{1-\cos(\alpha/2)} (\cos\theta - \cos(\alpha/2)) d\theta$$
$$= \frac{I_{max}}{2\pi} \frac{2\sin(\alpha/2) - \alpha\cos(\alpha/2)}{1-\cos(\alpha/2)} \quad (4)$$

The magnitude of nth harmonic is:

$$I_n = \frac{1}{\pi} \int_{-\alpha/2}^{\alpha/2} \frac{I_{max}}{1-\cos(\alpha/2)} (\cos\theta - \cos(\alpha/2)) \cos(n\theta) d\theta \quad (5)$$

The fundamental harmonic component of drain current is:

$$I_1 = \frac{I_{max}}{2\pi} \frac{\alpha - \sin\alpha}{1-\cos(\alpha/2)} \quad (6)$$

For class-A operation, the conduction angle is 2π. So, the dc component of drain current is:

$$I_{dc}(class\ A) = \frac{I_{max}}{2} \quad (7)$$

The fundamental harmonic component of drain current:

$$I_1(class\ A) = \frac{I_{max}}{2} \quad (8)$$

The DC and fundamental harmonic component of drain voltage:

$$V_{dc}(class\ A) = \frac{V_{max}}{2} \quad (9)$$

$$V_1(class\ A) = \frac{V_{max}}{2} \quad (10)$$

The DC dissipation power of class-A operation power amplitude:

$$P_{dc} = V_{dc} I_{dc} = \frac{V_{max} I_{max}}{4} \quad (11)$$

The output power for class-A operation:

$$P_{out} = \frac{1}{2} V_1 I_1 = \frac{V_{max} I_{max}}{8} \quad (12)$$

The maximum drain efficiency of class-A operation:

$$\eta = \frac{P_{out}}{P_{dc}} = \frac{1}{2} = 50\% \quad [1] \quad (13)$$

So, for class-A operation, the maximum drain efficiency 50%.

Class B:

The class B amplifier has half-sine drain current waveform and the drain voltage waveform is full-sine wave. Obviously, the overlap of the drain current and voltage is less, which means the dc power dissipation is less and therefore its efficiency is higher. However, the linearity of class-B operation is not as good as class-A operation.

The voltage and current waveform of class B amplifier is in figure 1.3:

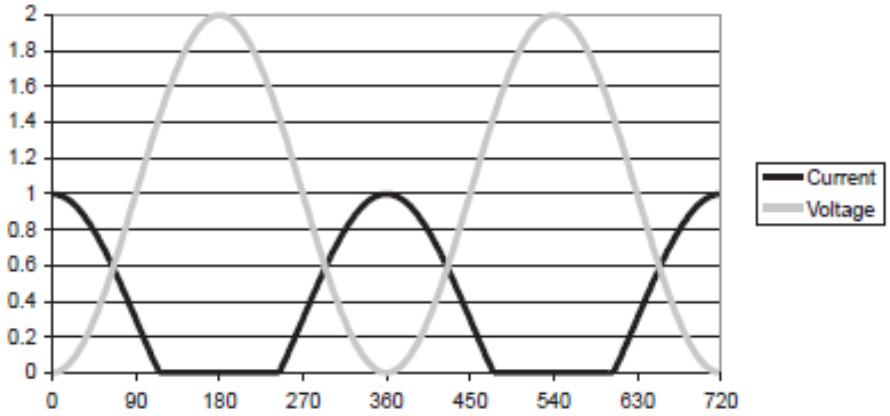


Figure 1.3 Drain voltage and Drain current of class-B operation [1]

The efficiency of class-B operation:

From equations (4) to (6), we can obtain the dc and fundamental harmonic components of drain current. The conduction angle of class-B operation is π.

$$I_{dc}(class\ \mathrm{B}) = \frac{\mathrm{I}_{max}}{\pi} \qquad [1] \qquad (14)$$

$$I_1(class\ \mathrm{B}) = \frac{\mathrm{I}_{max}}{2} \qquad (15)$$

The dc and fundamental harmonic components of drain voltage:

$$V_{dc}(class\ \mathrm{B}) = \frac{V_{max}}{2} \qquad (16)$$

$$V_1(class\ \mathrm{B}) = \frac{V_{max}}{2} \qquad (17)$$

The dc and output power:

$$P_{dc} = V_{dc} \cdot I_{dc} \qquad (18)$$

$$P_{out} = \frac{1}{2} \cdot I_1 \cdot V_1 \qquad (19)$$

The maximum drain efficiency for class-B operation:

$$\eta = \frac{P_{out}}{P_{dc}} = \frac{\pi}{4} \approx 78.5\% \qquad [1] \qquad (20)$$

The theoretical maximum class-B operation is 78.5%.

Class AB:

Class AB is a compromise between class A and B. The conduction angle for class-AB operation is between π and 2π. The larger the conduction angle is typically the better the linearity is, but the lower the efficiency is, and vice versa. So, the theoretical maximum drain efficiency is between 50% and 78.5%.

Class C:

In Class C operation the conduction angle is between 0 and π. Using equation (4) to (6), we can calculate the drain efficiency of class-C operation. It isn't a constant and depends on the conduction angle. If the conduction angle is 0, theoretically we can

obtain 100% drain efficiency. However, this also means that there is no power deliver to the load. So, 0 conduction angle is meaningless. In this class of operation we need to make a trade –off between efficiency and output power. The lower the conduction angle is, the higher the efficiency is and less output power is.
The waveforms of class-C operation:

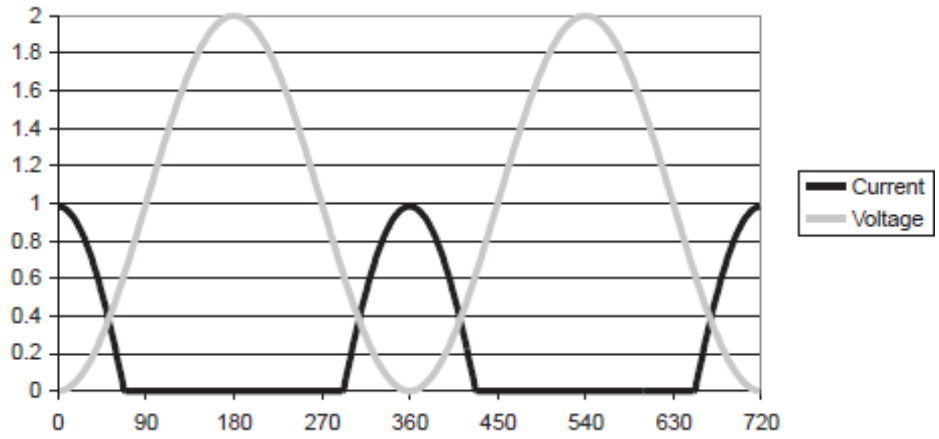


Figure 1.4 Drain voltage and Drain current of class-C operation [1]

The drain efficiency and output power versus conduction angle (figure 1.5):

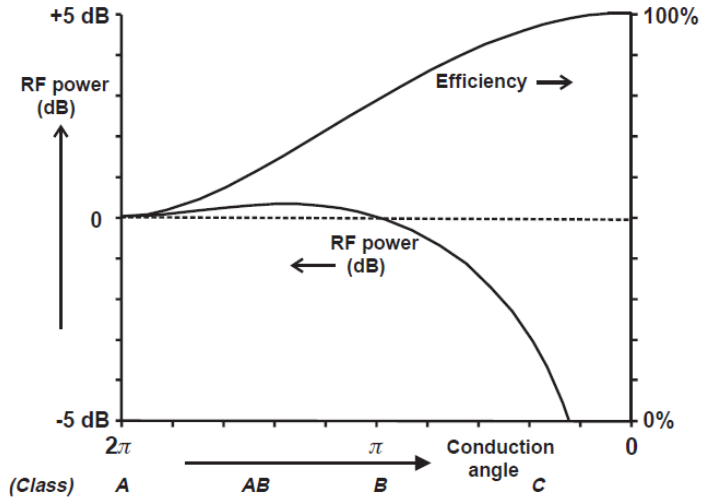


Figure 1.5 The drain efficiency and output power versus conduction angle [1]

Section 2: Switching mode power amplifier

Class-E and class-F power amplifiers are switching mode power amplifier. The transistor acts like a switch. The theoretical maximum drain efficiency for both classes can be as high as 100%. However, due to the non-ideal conditions of device (limited switching time, parasitics and etc), 100% drain efficiency is difficult to reach [2]. Comparing with class-C operation, class-E and class-F power operation don't need to make a compromise between efficiency and output power.

Class F:

For an ideal class-F power amplifier, the voltage waveform should be an ideal square waveform. When the transistor on, the drain voltage is zero. In other words, the drain voltage is shaped to minimize the overlap of drain voltage and current. However, normally the ideal square waveform condition is hard to meet and drain voltage waveform is a sub-optimum square waveform. The waveforms of sub-optimum class-F power amplifier are:

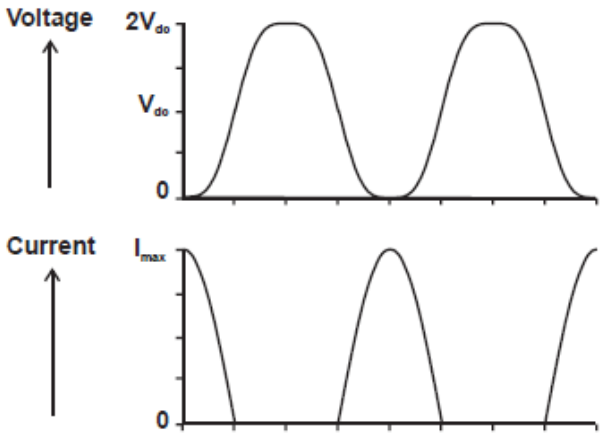


Figure 1.6 Drain current and voltage of sub-optimum class-F power amplifier

The square waveform only contains odd-order harmonics. There are three factors which influent the shape of waveform.

1. The phase relations between fundamental and higher order harmonics. For ideal square waveform, the peak of fundamental and the valleys of higher order harmonics should be synchronized.
2. The amplitude relations of fundamental and higher order harmonics.

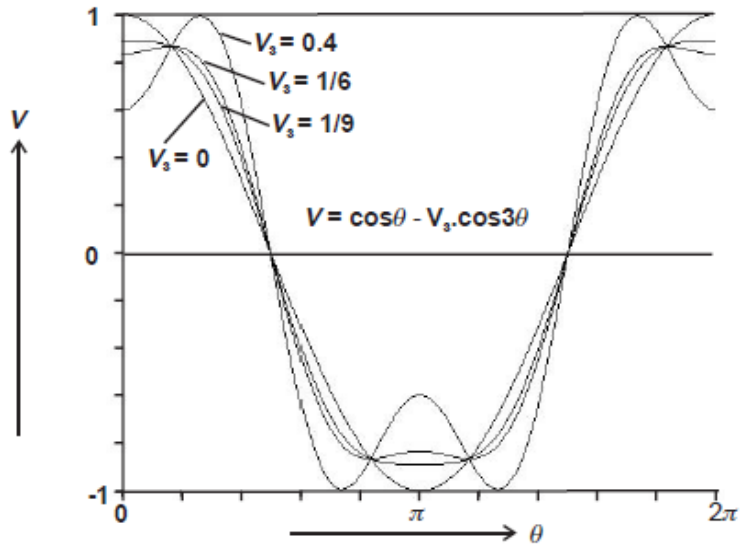


Figure 1.7 Third order harmonic shaped waveform (different amplitude of third harmonic) [1]

The fundamental harmonic is:

$$\cos\theta \qquad [1] \qquad (21)$$

The third harmonic is:

$$-V_3\cos(3\theta) \qquad (22)$$

The superimposition of these two harmonics:

$$V = \cos\theta - V_3\cos(3\theta) \qquad (23)$$

The amplitude ratio of fundamental and third harmonic is very important too. As shown in figure 1.7, when the ratio is 1/6, the superimposited waveform is very flat. When the ratio is less than 1/9, the superimposition is still looks like a sinusoid.

3. The number of harmonics:

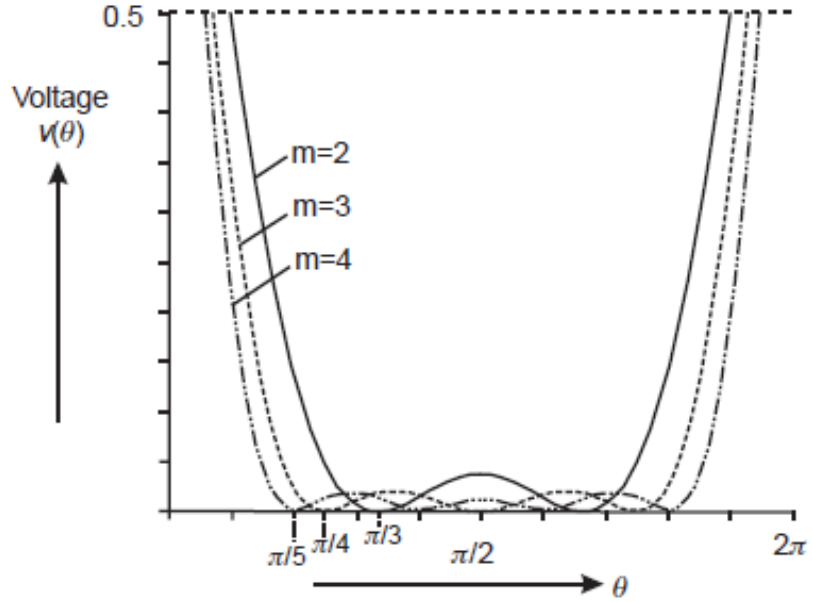


Figure 1.8 Square waveform with different number of odd-order harmonics. m represents the number of odd-order harmonics [1]

We can see from figure 1.8 that when the number of odd-order harmonics increases, the waveform becomes more and more like an ideal square waveform.

So, with finite number of harmonics or other non-ideal conditions, the efficiency of class-F power amplifier drops from theoretical value of 100%

Class-E:

Class-E power amplifier is also a kind of switching mode amplifier. For an ideal class-E operation, three requirements for drain voltage and current should be meet [2]:

(1) The rise of the voltage cross the transistor at turn-off should be delayed until after the transistor is off.
(2) The drain voltage should be brought back to zero at the time of transistor turn-on.
(3) The slope of the drain voltage should be zero at the time of turn-on.

These conditions can only be met by controlling an infinite number of harmonics.

When the number of harmonics is limit, the efficiency drops from theoretical value of 100% and we call that kind of operation sub-optimum class-E. The drain voltage waveform varies with different number of harmonics are shown in figure 1.9.

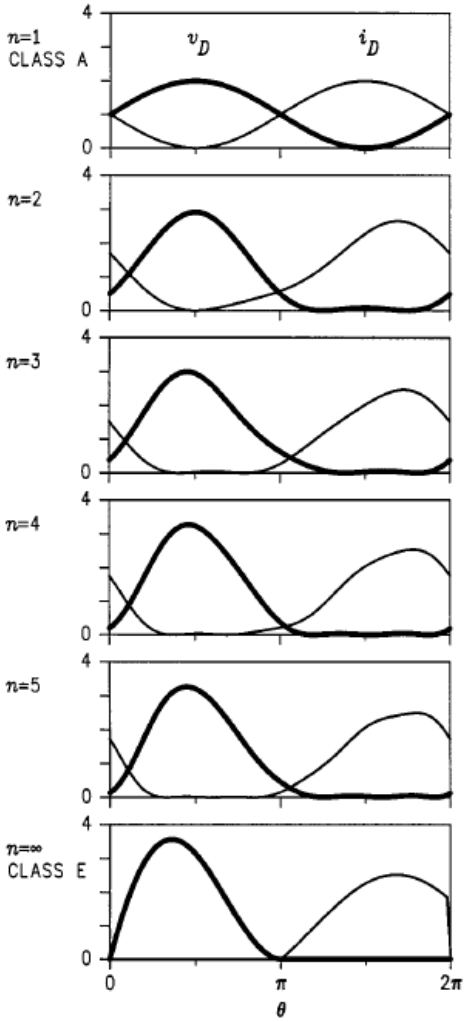


Figure 1.9 The drain voltage waveform varies with different number of harmonics. n represents the number of harmonics [3]

When the harmonic number is 2, the drain voltage only contains fundamental and second harmonic components. We call it class-J operation. The detail discussion on class-J operation is in next chapter. So, class-J is also a kind of sub-class E operation. When the number of harmonic increases to infinite, there is no overlap of drain voltage and current (figure 1.9) and 100% efficiency can be achieved. However, in practical situations, it's a very hard task due to the existence of on resistor or other parasitics of the transistors. Basically, the class-E power amplifier we call is in sub-class E operation.

The equations to calculate the optimum fundamental load for class-E operation:

$$R = \frac{0.58 \times V_{DD}^2}{P_{out}} \tag{24}$$

The table of optimum harmonics load for ideal class-E operation [3]:

k	$\lvert V_k \rvert$	$\lvert I_k \rvert$	Z_k for R=1	Z_k for R_1=1
0	1.000	0.5762		
1	1.639	0.8691	1.5260 + j1.1064	1 + j0.725
2	0.8477	0.3120	$-j$2.7233	$-j$1.7846
3	0.2222	0.1224	$-j$1.8155	$-j$1.1897
4	0.1433	0.1056	$-j$1.3616	$-j$0.8923
5	0.08001	0.07344	$-j$1.0893	$-j$0.7138
6	0.05907	0.06536	$-j$0.9038	$-j$0.5923
7	0.04082	0.05246	$-j$0.7781	$-j$0.5099
8	0.03236	0.04774	$-j$0.6778	$-j$0.4448
9	0.02470	0.04081	$-j$0.6052	$-j$0.3966
10	0.02045	0.03773	$-j$0.5420	$-j$0.3552

Figure 1.10 Table of optimum load for class-E operation harmnics

Section 3: Harmonic tuned waveform

Actually, as we have shown above, we can use different harmonics to tune the full-sine drain voltage waveform. In this way, we are able to shape the drain voltage waveform and get desired operation classes. We summarize the relation of harmonics and operation classes as follows [3]:

Class-F: Drain voltage is a square waveform which contains only odd order harmonics. Drain current is a half-sine wave which contains only even order harmonics.

Class-C: All harmonics reactance are shorted. The drain current is shaped to a narrow pulse.

Class-E: The reactance for all harmonics are negative and comparable in magnitude to the fundamental frequency load resistance.

Section 4: Efficiency in power back-off operation

In WCDMA system, the power amplifier typically operates most of the time at 6 to 11 dB power back-off of the peak power point (high peak to average ratio for output power). All the efficiency considerations we have discussed above relate to the efficiency at peak output power. So it is also important to define the efficiency if we decrease the input power so that the power amplifier operates at its power back-off point.

For this purpose we take class-B as an example. The optimal load for class-B power amplifier to reach the peak power and still maintain the linearity for power amplifier is:

$$R_{opt} = \frac{2 \times V_{dc}}{\mathrm{I}_{max}} \qquad [1] \quad (25)$$

Imax is the maximum drain current and Vdc is the drain supply voltage.

The amplitude of fundamental drain voltage is:

$$V_{fund} = V_{dc} \qquad (26)$$

The amplitude of fundamental drain current is:

$$I_{fund} = \frac{\mathrm{I}_{max}}{2} \qquad (27)$$

The output power is:

$$P_{fund} = \frac{1}{2} \times \mathrm{Re}(V_{fund} \times I_{fund}) = \frac{V_{dc} \times \mathrm{Im}\,ax}{4} \tag{28}$$

The DC power dissipation is:

$$P_{DC} = V_{dc} \times I_{dc} = \frac{V_{dc} \times \mathrm{Im}\,ax}{\pi} \tag{29}$$

The maximum drain efficiency is:

$$eff = \frac{P_{fund}}{P_{DC}} = \frac{\pi}{4} \quad [1] \tag{30}$$

So, the maximum drain efficiency is (78.5%) as we have previously found.

Now, if we reduce the amplitude of the input voltage by a factor of 2 (6 dB power back-off), the drain current also reduces by a factor of 2 (the drain current is well below the saturation current). The drain supply voltage keeps a constant. The amplitude of fundamental drain voltage becomes:

$$V_{fund} = \frac{\mathrm{Im}\,ax}{2 \times 2} \times R_{opt} = \frac{V_{dc}}{2} \tag{31}$$

The output power becomes:

$$P_{fund} = \frac{1}{2} \times \mathrm{Re}(V_{fund} \times I_{fund}) = \frac{V_{dc} \times \mathrm{Im}\,ax}{16} \tag{32}$$

The DC power dissipation becomes:

$$P_{DC} = V_{dc} \times I_{dc} = \frac{V_{dc} \times \mathrm{Im}\,ax}{2\pi} \tag{33}$$

So, the maximum efficiency:

$$eff = \frac{P_{fund}}{P_{DC}} = \frac{\pi}{8} \quad [1] \tag{34}$$

The maximum drain efficiency also reduces by a factor of 2.It becomes 39.5%. We can see the drain efficiency drops a lot at 6 dB power back-off point (factor four lower output power).

Figure 10 shows us the reason for why the efficiency drops quickly. The load is optimized for a certain value of input power (drain current). When the drain current reduces from Imax and load remain constant, the drain voltage can't reach the rail-to-rail swing (dotted line in figure 1.11). So, the output power and drain efficiency drop a lot.

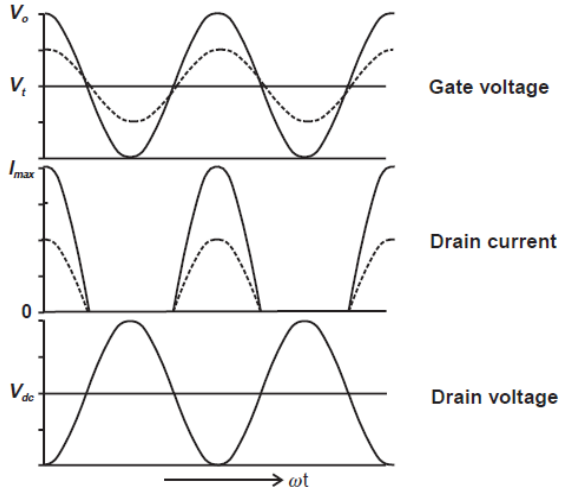


Figure 1.11 Drain voltage and current (Solid line at peak power, dotted line at power back off point) [1]

Now we discuss how to keep the efficiency at power back-off point. From the equations above, we can conclude that we have two ways to keep the efficiency at the power back-off point. One is we have a varying load with time at the output. When the power amplifier operates at a power which is much lower than the peak power, the load should increase corresponding to keep the efficiency:
If the load increases by a factor 2, the drain voltage becomes:

$$V_{fund} = \frac{\mathrm{Im}\,ax}{2 \times 2} \times 2 \times R_{opt} = V_{dc} \qquad [1] \quad (35)$$

The output power:

$$P_{fund} = \frac{1}{2} \times \mathrm{Re}(V_{fund} \times I_{fund}) = \frac{V_{dc} \times \mathrm{Im}\,ax}{8} \qquad (36)$$

The DC power dissipation:

$$P_{DC} = V_{dc} \times I_{dc} = \frac{V_{dc} \times \mathrm{Im}\,ax}{2\pi} \qquad (37)$$

The drain efficiency:

$$eff = \frac{P_{fund}}{P_{DC}} = \frac{\pi}{4} \qquad [1] \quad (38)$$

So, the drain efficiency keeps the same. However, the output power drops only by a factor of 2. From the derivation above, a varying load with time can keep the efficiency at power back-off point. This is the principle of a Doherty power amplifier.

Another way to keep the efficiency is we modulate the supply voltage according to the envelope of input signal. If the supply voltage has the same envelope as input power when the input power varies, the efficiency can be maintained.

Section 5: EET and ET system

There are two similar systems for this ideal: Envelope Elimination and Restoration (EER) system and Envelope tracking (ET) system. We introduce both of them here.
EER system: Envelope Elimination and Restoration (Figure 1.12):

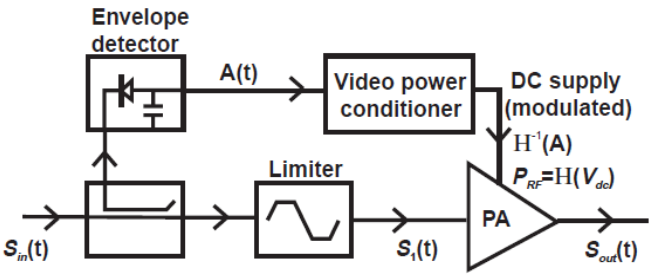


Figure 1.12 Envelope Elimination and Restoration System

EER system is able to provide high power efficiency without compromising linearity. In EER system, a modulated RF signal is split into its polar components, envelope and phase, by a phase detector and a limiter respectively. The input signal is a constant envelope signal that can be amplified by a well-saturated amplifier. A well-saturated amplifier can be approximated by an RF voltage generator whose output amplitude is proportional to the dc supply voltage. On the other hand, the input signal only contains phase information. The limiter eliminates the possibility of AM-PM distortion so that the output of the PA still retains the undistorted phase characteristic of the input. The envelope information can be restored at the output by supply voltage modulation. The modulating signal is derived from an envelope detector. If the envelope of the input single can be restored perfectly at the output and there is no other power dissipation of components in the system (like the envelope detector), the efficiency can be maintained over a wide range of output power. However, there is always some power dissipation in the other components in the system [1] [4] [5].

ET system:

Envelope tracking system is similar to the envelope elimination and restoration system. The ET system differs from the EER system in two ways: 1. The RFPA in the system is a linear PA. 2. The input signal of the RFPA contains both amplitude and phase information [6] (figure 1.13). In ET system, the supply voltage increases in proportion to the increasing drive voltage. So, maximum efficiency is maintained and the output power increases linearly with input drive power. Comparing with ET system, the modulation control voltage of ET system doesn't have to be an exact replica of the signal envelope. The supply voltage could be tracked for just the upper few dB of the signal envelope range [1] [4].

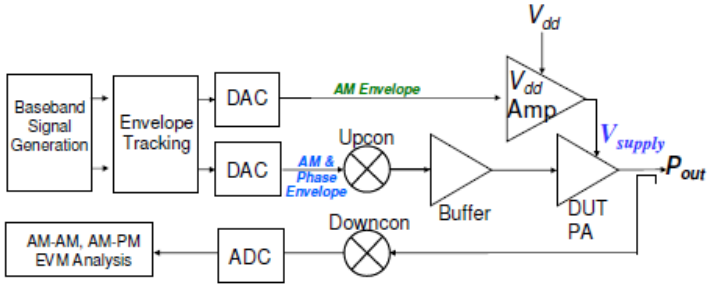


Figure 1.13 Envelope tracking system [4]

Section 6 Conclusion:

In this chapter, we introduced the principle of different operation classes and the systems to improve the performance of power amplifier at power back-off point. In chapter 3, we will design a power amplifier for different operation classes with NXP new generation LDMOS and find out which class is the most suitable one for our device.

Chapter 2 Harmonic Tuned Class-J Power Amplifier

In the previous chapter, we have discussed the principles of conventional operation classes for power amplifiers. In this chapter we will discuss the principles of class-J operation. The definition of class-J operation is we use a second harmonic termination to tune the shape of drain voltage waveform. In this way, we can improve the performance of power amplifier. Let's discuss it in more detail.

Section 1: Improvement of the efficiency of power amplifier

When we design a power amplifier, efficiency (drain efficiency, PAE) is an important performance. The equation for calculating the drain efficiency is:

$$Drain\_eff = \frac{P_{fund}}{P_{dc}} \tag{1}$$

Drain_eff represents the drain efficiency. P_{fund} and P_{dc} represent fundamental harmonic power and DC power respectively.

From the equation, we find that there are two ways to improve the efficiency performance.

(1) One is to increase the fundamental harmonic power. This means that all the output power should be at the fundamental frequency and there is no power dissipation at higher order harmonics. So, even if we want to use the harmonics to tune the waveform of drain voltage or drain current, the higher order harmonics' loads (higher than order 2) should be pure reactive. However, because of some parasitic resistance of the device, there is always some loss of at these higher order harmonics. But, this loss is typically small compared with the fundamental harmonic power. So, what we need to do is to keep all the higher order harmonics' loads reactive to minimize this loss.

(2) The second way to improve the efficiency is to minimize the dc power dissipation. The DC power is as follow:

$$P_{dc} = \frac{1}{T}\int I_d \times V_d \, dt \tag{2}$$

From equation 2, we can learn that if we want to reduce the DC power dissipation, we need to reduce the product of current and voltage, consequently we should make the overlap of the drain current and voltage as low as possible at all times (Figure 2.1 and 2.2):

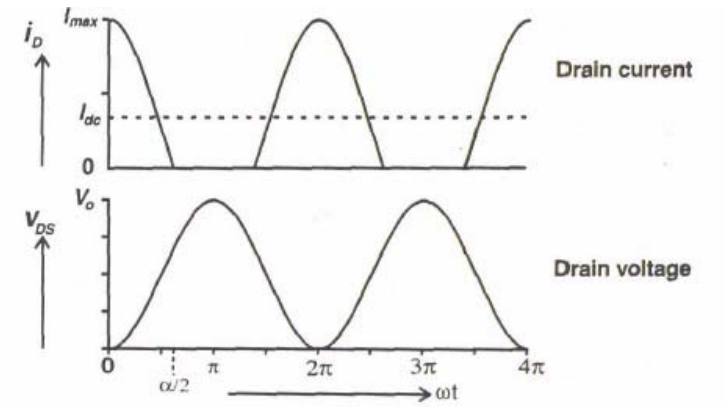


Figure 2.1 Drain current and voltage of class-AB/B PA

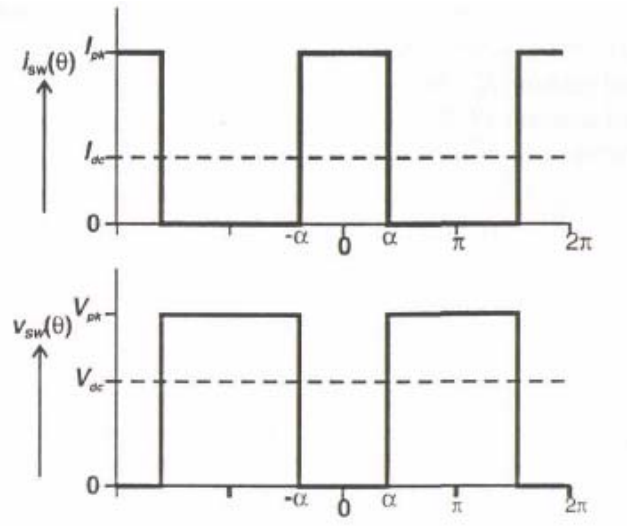


Figure 2.2 Drain current and voltage of an ideal switching PA [1]

We can perform the Fourier transform for the waveform in figure 2.1 and get the DC components of drain current and voltage. If the current and voltage are both high across the active device, DC components always exist at the same time and there will be power dissipation. Note that in figure 2.2, the ideal switching mode power amplifier has no drain current and voltage simultaneous, that means there is no power dissipation. All the DC power is transformed to signal power. For this ideal switching PA, the efficiency is 100%. But, this kind of PA is not easy to realize, what we can do is to use the harmonics to tune the waveform in figure 2.1 and make the overlap of drain current and voltage as small as possible.

Section 2: Short all the harmonics: Class-AB/B operation:

Before we invest the influence of harmonics on the efficiency performance of power amplifier, we first study the operation of class-AB/B. For class-AB/B power amplifier, all the harmonics are shorted except the fundamental harmonic. The drain current and drain voltage of class-AB/B power amplifier are as follow:

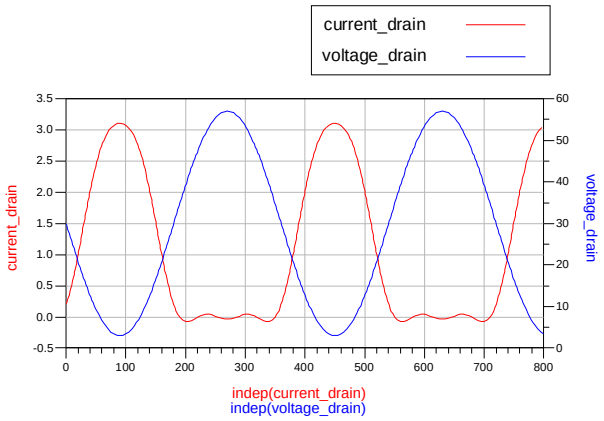


Figure 2.3 Drain voltage and current of class-AB/B operation (blue, drain voltage, red, drain current. X axis is phase of waveforms in degrees. Y axis is in Amperes and volts for current and voltage respectively)

The drain current of the class-AB/B power amplifier is half-sine wave. The equation for the half-sine wave is as follow:

$$\text{half\_sin}(\theta) = 1 + \frac{\pi}{2} \times \sin(\theta) + \sum_{n=1}^{\infty} -2 \times \frac{1}{n^2 - 1} \times \cos(n\theta), n = 2k, \forall n, k \in N \quad [6]\ (1)$$

Here we normalize all the currents to the DC component. So, the DC current equals 1, the amplitude of fundamental harmonic current will be $\frac{\pi}{2}$. The amplitudes for higher order harmonics are defined as $-\frac{2}{n^2 - 1}$. From the equation we can see the half-sine wave contains only even-order harmonics and the fundamental harmonic. θ represents the phase angle. The drain voltage of class-AB/B operation contains only the fundamental harmonic since all harmonics except the fundamental harmonic are shorted.

Obviously, if we can use the harmonics to make the drain voltage sharper, the overlap of the drain current and voltage can be reduced and the efficiency will increase.

Section 3: How the harmonics tune the fundamental frequency waveform

For class-F operation, the odd order harmonics are used to shape the drain voltage to a square waveform. For class-E operation, the drain voltage waveform is shaped by the harmonics so that the drain voltage and the slope of drain voltage is zero when the transistor is on. However, the harmonic tune conditions for ideal class-E/F operations are difficult to meet. Due to the existence of output capacitance of transistor, higher order harmonics are therefore difficult to tune. So, typically we can just tune the second harmonic in a practical matching network. This is main motivation for the use of class-J operation. The question is now how does the second harmonic affect the

performance of PA. Let's discuss it step by step.

First, we show how the second harmonic affects the drain voltage waveform (figure 2.4):

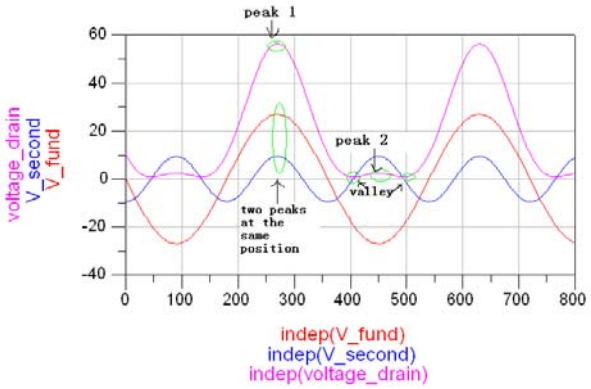


Figure 2.4 Phase relation of fundamental and second harmonic waveforms (x axis, phase angle in degree, y axis, voltage in V. Red, fundamental harmonic voltage. Blue, second harmonic voltage. Pink, superimposition of these two voltage)

Figure 2.4 shows us that the drain voltage becomes shaper after tuning by second harmonic. This is what we want. For our first impression, the efficiency performance will be improved. However, is the problem really so simple? Let's calculate the theoretical efficiency of class-J operation.

Section 4: Solutions for class-J operation

If the waveform only contains dc, fundamental and second harmonic components, we call it pseudo half sinusoidal (PHS) [6]. The PHS of drain current is as follow:

$$\begin{aligned} PHS\_I_{sin}(\theta) &= I_{dc}+I_{fund}+I_{second} \\ &= I_{dc}\times\left(1+\frac{\pi}{2}\times\sin(\theta)-\frac{2}{3}\times\cos(2\theta)\right) \end{aligned} \qquad [6] \quad (4)$$

PHS_Isin(θ) is the drain current, Idc is the dc current, Ifund is the fundamental harmonic current and Isecond is the second harmonic current. For simplicity, we normalize the currents to DC current:

$$I_{dc} = 1 \qquad (5)$$

$$I_{fund} = \frac{\pi}{2}\times\sin(\theta) \qquad (6)$$

$$I_{second} = -\frac{2}{3}\times\cos(2\theta) \qquad (7)$$

Now we have knowledge on the composition of current, in order to obtain the loads, we also need to know the composition of voltage. From figure 2.8, it works out that the voltage waveform and current have reverse sign (fundamental component of drain voltage has a 180 degrees phase reversal with the drain current and the second harmonic component of drain voltage has a 360 degrees phase reversal of drain

current), which is due to the nature of the schematic (see figure 2.5).

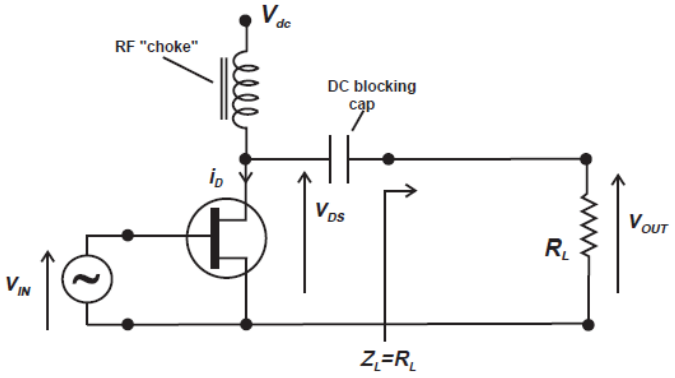


Figure 2.5 The drain current and voltage have reversed phase relation intrinsically. (see ID and Vds in the graph)

In the previous expressions of drain current and voltage, this phase reversal hasn't been taken into account yet.

The load for the second harmonic: on first sight it might seems that the second harmonic load can be arbitrary value. Actually, as we discussed in section 1, in order to transform as much power from dc to fundamental frequency as more as possible, we should minimize the power dissipation at higher order harmonics. Therefore, the second harmonic load we used should be pure reactive. It can be inductive or capacitive. Inductive load means the second harmonic voltage will lead 90 degrees with the drain current. And a capacitive load means the second harmonic voltage will lag 90 degrees with the drain current. So, if we want to synchronize the peak of the fundamental and second harmonic waveform like that in figure 2.4, the fundamental load should make the fundamental voltage lead or lag 45 degrees with the drain current. This also means that: for the typical class-J operation, there are two solutions for the fundamental and second harmonic loads. Let's discuss both of them.

The pseudo half sine (PHS) form of drain voltage:

$$\mathrm{PHS\_Vsin}(\theta) = 1 + \mathrm{A} \times \sin(\theta) - \mathrm{B} \times \cos(2\theta) \qquad [6] \quad (8)$$

A and B is the amplitude of fundamental and second harmonic voltage respectively. All of the amplitudes are normalized to Vdc.

If we obtain the derivative of this equation and make it equal to zero, we can get the two peaks and two valleys of PHS_Vsin [1]:

$$peak_{1,2} = 1 \pm A + B \,@\, \theta_1 = \frac{\pi}{2}, \theta_2 = \frac{3\pi}{2} \qquad [6] \quad (9)$$

$$\min_{1,2} = 1 - B - \frac{A^2}{8B} @ \theta_1 = \pi + \arcsin(\frac{A}{4B}) \quad @ \theta_2 = 2\pi - \arcsin(\frac{A}{4B}) \qquad (10)$$

The minimum value of PHS waveform should be zero:

$$\min_{1,2} = 0 \Rightarrow 1 - B - \frac{A^2}{8B} = 0 \Rightarrow A^2 = 8B(1-B) \tag{11}$$

$$A^2 = 8B(1-B) \Rightarrow B = \frac{1}{2} + \frac{1}{2}\sqrt{1 - \frac{A^2}{2}} \tag{12}$$

From equation 17, we can get the maximum and minimum values of A and B respectively:

$$1 - \frac{A^2}{2} \geq 0 \Rightarrow \frac{A^2}{2} \leq 1 \Rightarrow A \leq \sqrt{2} \tag{13}$$

$$A_{Max} = \sqrt{2} \ \ \& \ \ B_{Min} = \frac{1}{2} \tag{14}$$

[6]

The first solution: we can get the first solution by check the drain current and voltage relationship.
From equation 9 we get the drain current equation:

$$I_{drain}(\theta) = \frac{I_{Peak}}{\pi} + (\frac{I_{Peak}}{2}) \times \sin(\theta)$$
$$- \frac{2 \times I_{Peak}}{3 \times \pi} \times \cos(2\theta)$$

(15)

$$I_{dc} = \frac{I_{Peak}}{\pi} \tag{16}$$

$$I_{fund} = \frac{I_{Peak}}{2} \times \sin(\theta) \tag{17}$$

$$I_{\sec ond} = -\frac{2 \times I_{Peak}}{3 \times \pi} \times \cos(2\theta) \tag{18}$$

For the first solution, if the load for second harmonic is capacitive. The second harmonic voltage should lead 90 degrees with the phase of drain current：

$$V \sec ond = -B\cos(2\theta + \pi - \frac{\pi}{2}) = -B\cos(2(\theta + \frac{\pi}{4})) \tag{19}$$

B is amplitude of Vsecond, the pi in the equation is caused by the reverse phase relation of drain current and voltage as shown in figure 2.5.

In order to synchronize the peaks of the fundamental and second harmonic voltage wave, the fundamental harmonic voltage waveform should lags 45 degrees with the phase of drain current:

$$V_{fund} = A \times \sin(\theta + \pi + \frac{\pi}{4}) \tag{20}$$

Where A is the amplitude of Vfund. The pi is caused by the reverse phase relation of drain current and voltage as shown in figure 2.5.

Now we calculate the drain efficiency. The output voltage and on the load is Vout and Iout (see figure 2.5):

$$\begin{aligned} V_{out}(\theta) &= V_{fund\_out} + V_{second\_out} \\ &= A \times Vdc \times \sin(\theta + \frac{\pi}{4}) - B \times Vdc \times \cos(2\theta - \frac{\pi}{2}) \end{aligned} \tag{21}$$

$$\begin{aligned} I_{out}(\theta) &= I_{fund\_out} + I_{second\_out} \\ &= (\frac{I_{Peak}}{2}) \times \sin(\theta) - \frac{2 \times I_{Peak}}{3 \times \pi} \times \cos(2\theta) \end{aligned} \tag{22}$$

The output voltage and the current flow into the load have in-phase relation and they don't contain DC component.

Now, we can calculate the output power and efficiency of class J operation. The DC power dissipation can be calculated from the DC components of drain voltage and current:

$$P_{dc} = I_{dc} \times V_{dc} = \frac{I_{Peak}}{\pi} \times V_{dc} \tag{23}$$

The output power can be calculated from the output voltage and current on the load:

$$\begin{aligned} P_{out} &= \frac{1}{2} \times \mathrm{Re}[\dot{V}_{fund\_out} \times conj(\dot{I}_{fund\_out})] \\ &= \frac{1}{2} \times \mathrm{Re}[AV_{dc} e^{j\omega(\frac{\pi}{4})} \times \frac{I_{Peak}}{2}] = \\ &\frac{I_{Peak} \times V_{dc}}{4} \times \cos(\frac{\pi}{4}) \times A \end{aligned} \tag{24}$$

The drain efficiency:

$$\eta = \frac{P_{out}}{P_{dc}} = \frac{\pi}{4} \times \frac{1}{\sqrt{2}} \times A \tag{25}$$

The maximum efficiency can be obtained when A reaches its maximum value. We have found that the maximum value for A is $\sqrt{2}$. So, the maximum efficiency is:

$$\eta_{\max} = \frac{P_{out}}{P_{dc}} = \frac{\pi}{4} \times \frac{1}{\sqrt{2}} \times \sqrt{2} = \frac{\pi}{4} \approx 78.5\% \qquad [6] \tag{26}$$

So, the theoretical highest drain efficiency of class-J operation is 78.5% and if we want to achieve this peak efficiency, we need to choose A as $\sqrt{2}$ and B as1/2.

$$A = \sqrt{2} \qquad [6] \tag{27}$$

$$B = \frac{1}{2} \tag{28}$$

Therefore, the drain voltage is:

$$V_{drian}(\theta) = V_{dc} + \sqrt{2} \times V_{dc} \times \sin(\theta + \pi + \frac{\pi}{4}) - \frac{1}{2} \times V_{dc} \times \cos(2\theta + \pi - \frac{\pi}{2}) \tag{29}$$

$$V_{fund} = \sqrt{2} \times V_{dc} \times \sin(\theta + \pi + \frac{\pi}{4}) \tag{30}$$

$$V_{\sec ond} = -\frac{1}{2} \times V_{dc} \times \cos(2\theta + \pi - \frac{\pi}{2}) \tag{31}$$

The pi in equations (29) and (30) is due to the nature of schematic (see figure 2.5). So, it should be eliminated when we calculate the loads. From equations (16) to (17) and equations (30) to (31), we can calculate the fundamental and second harmonic loads:

$$Zload_{fund} = \frac{2\sqrt{2} \times V_{dc}}{I_{Peak}} \angle \frac{\pi}{4} \tag{32}$$

$$Zload_{\sec ond} = \frac{3 \times V_{dc} \times \pi}{4 \times I_{Peak}} \angle -\frac{\pi}{2} \tag{33}$$

We can choose the values of Vdc and Ipeak to check the loads on the Smith chart. We assume Vdc=30 V and Ipeak=2.5 A.

$$Zload_{fund} = 34 \times \angle \frac{\pi}{4} \tag{34}$$

$$Zload_{\sec ond} = 28.3 \angle -\frac{\pi}{2} \tag{35}$$

[6]

The loads on the Smith chart (figure 2.6):

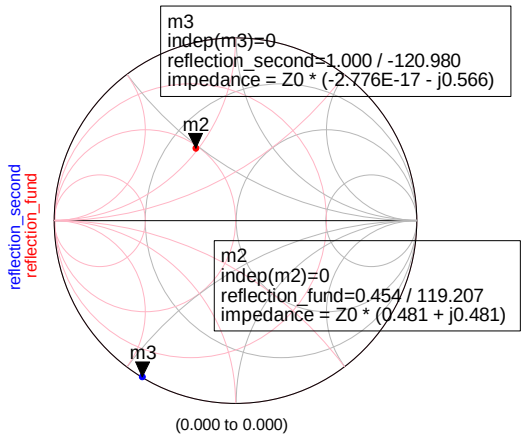


Figure 2.6 The fundamental and second harmonic loads (red, fundamental harmonic, blue, second harmonic, normalized to 50 Ohms)

We can get an alternative solution on the Smith chart, where the load for second

harmonic of solution 2 is inductive (figure 2.7):

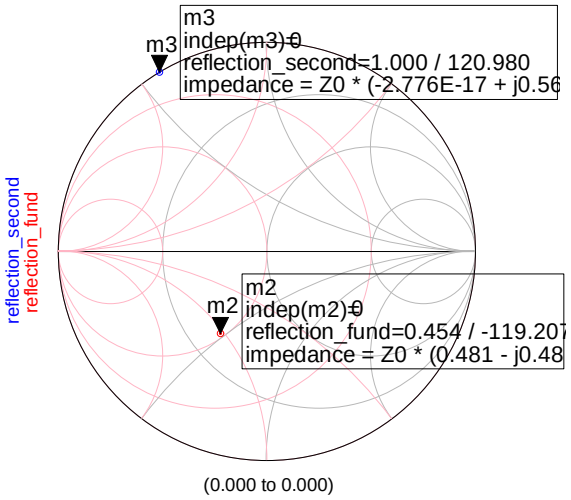


Figure 2.7 The loads of solution 2 (red, fundamental harmonic, blue, second harmonic, normalized to 50 Ohms)

The drain voltage and current waveform for solution 1 and 2:

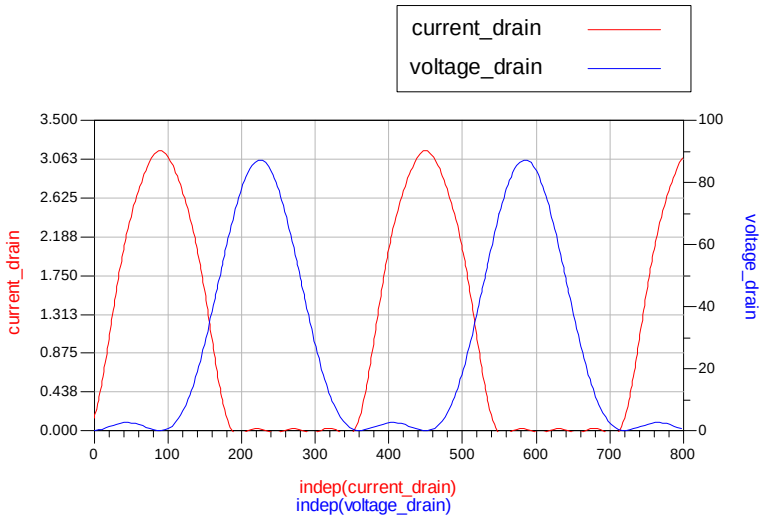


Figure 2.8 (a) Drain voltage (blue) and current (red) waveforms for solution 1of class-J operation

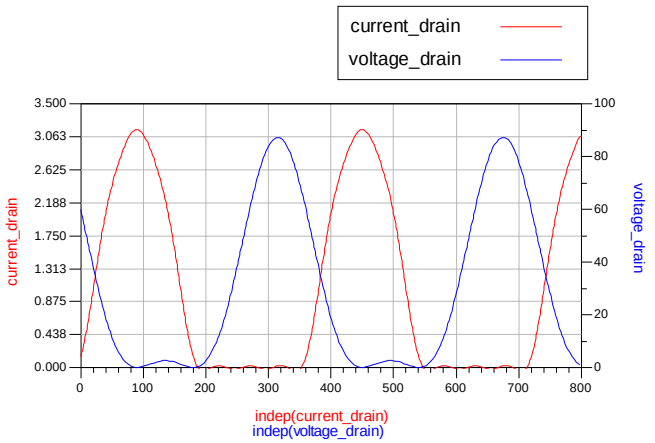


Figure 2.8 (a) Drain voltage (blue) and current (red) waveforms for solution 2of class-J operation

So, the two solutions for class-J operation are:

$$Zload_{fund} = \frac{2\sqrt{2} \times V_{dc}}{I_{Peak}} \angle \pm \frac{\pi}{4} \tag{36}$$

$$Zload_{\sec ond} = \frac{3 \times V_{dc} \times \pi}{4 \times I_{Peak}} \angle \mp \frac{\pi}{2} \tag{37}$$

$$P_{outpeak} = \frac{1}{4} \times V_{dc} \times I_{peak} \tag{38}$$

The loads in terms of peak power are:

$$Z_{fund} = \frac{{V_{dc}}^2}{\sqrt{2} \times P_{outpeak}} \angle \pm \frac{\pi}{4} \tag{39}$$

$$Z_{\sec ond} = \frac{3\pi \times {V_{dc}}^2}{16 \times P_{outpeak}} \angle \mp \frac{\pi}{2} \quad [6] \tag{40}$$

Vdc is the dc voltage component of drain voltage and Ipeak is the peak amplitude of drain current.

In this section, we have discussed the efficiency that class-J operation can provide together with the optimal loads for fundamental and second harmonics. We can call this ideal class-J operation. For ideal class-J operation, the maximum drain efficiency is 78.5%, which is the same as that of class-B operation. However, this efficiency is reached without providing a perfect short for the second and higher order harmonics, something that is not always practical (for example, there is a series inductor of package) in wideband design. So, for single frequency design, we should test which class is works best for our device. While for wideband design, we can make use of the 2^{nd} harmonic termination to achieve better results, when second harmonic shorts are not practical. In the next section, we will discuss some practical considerations.

Section 5: Sub-optimum class-J operation

In section 4, we have obtained the solutions for ideal class-J operation. From equations (36) to (40) we can see: for fixed values of dc voltage and Ipeak or a peak output power, the optimal loads for fundamental and second harmonics are constants for a given operating frequency.

But if we want to design a wideband power amplifier, we will have constant values for the components of our matching network (for example, an fixed inductor, capacitor or transmission line). Use of these components will result in a not constant reactance versus frequency. For example, when we have an inductive load, the load is given by:

$$G_{loadfund} = g_{fund} + \frac{1}{j\omega L_{fund}} \tag{41}$$

gfund is the conductance of the load, and with the frequency changes, the imaginary part $\frac{1}{j\omega L f_{und}}$ will shift on the smith chart (figure 2.9):

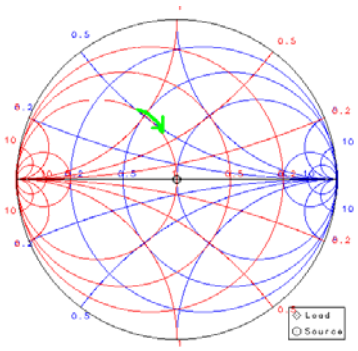


Figure 2.9 With increasing frequency, the imaginary part of the load will shift on the smith chart in the direction of the green arrow

Another complication is that the reactance of parasitic output capacitance of the device $j\omega C_{parasitic}$ will also change with frequency. Even worse this parasitic output capacitance is not a linear capacitor with supply voltage. In fact it is a very strong function of supply voltage, which will cause the optimum load shift on the Smith chart with supply voltage modulation as well. So, for a wideband power amplifier with supply voltage modulation, it's almost impossible to match every load of different frequency to the optimum load. This is the reason why we discuss here sub-optimal class-J operation.

For optimum class-J, two conditions should be met:

(1) The peak of the fundamental voltage waveform should synchronize with the second harmonic voltage waveform (as shown in figure 2.4). And only this condition is met, the superimposition of these two waveforms will have two peaks and two valleys.

(2) The amplitude ratio of fundamental and second harmonic voltage should be a certain value. From equation (35) we know the amplitude ratio of fundamental and second harmonic voltage is A/B. For the optimal load, A=$\sqrt{2}$, B=$\frac{1}{2}$. So,

$$\frac{A}{B} = 2\sqrt{2} = 2.828$$

For sub-optimal class-J operation, we indeed have used the second harmonic to tune the drain voltage waveform, but we don't meet the two conditions above exactly.

First, as we have discussed above, for wideband power amplifier, the fundamental loads for every frequency can't be matched to the optimal load. So, let's discuss how are the waveforms like, if the load deviates from the optimum value. For example:

When it's the optimum load is give by: $Zload_{fund} = \frac{2\sqrt{2} \times V_{dc}}{I_{Peak}} \angle \frac{\pi}{4}$

The waveform is:

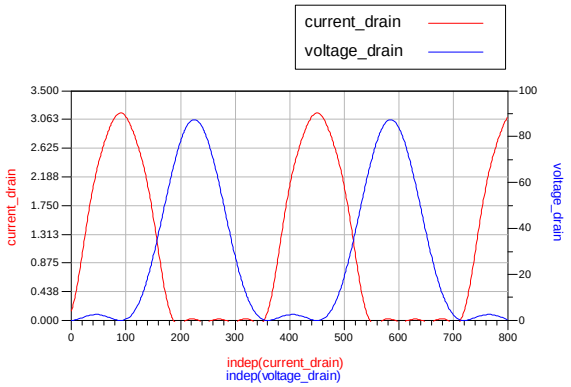


Figure 2.10 Drain current and voltage waveforms for optimal load

When the phase angle changes to $\frac{\pi}{5}$ and $\frac{\pi}{3}$, the waveforms are:

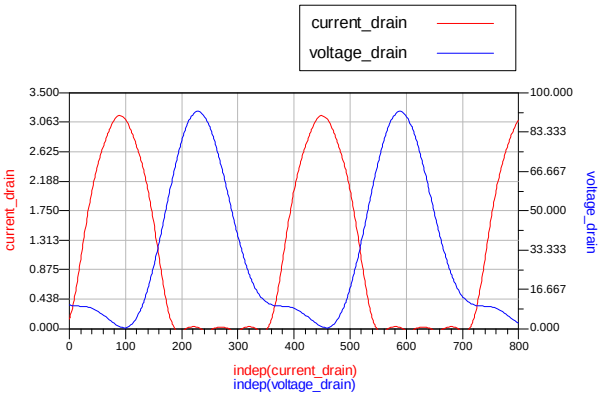


Figure 2.11 (a) Drain current and voltage waveforms when the phase angle of fundamental harmonic load is $\frac{\pi}{5}$

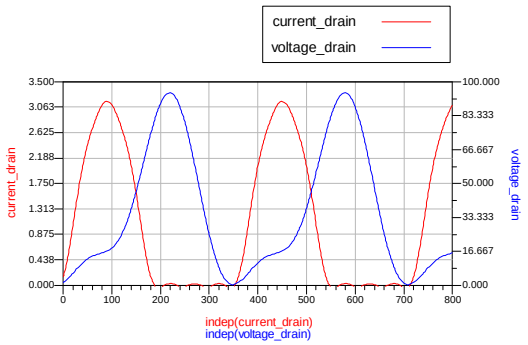


Figure 2.11 (a) Drain current and voltage waveforms when the phase angle of fundamental harmonic load is $\frac{\pi}{3}$

Phase angle of fundamental load	Drain efficiency
Pi/5	69.2%
Pi/4	78.5%
Pi/3	62.4%

Table 2.1 Phase angle of fundamental load versus drain efficiency

We can see, when the fundamental load have phase angle different from the optimal load, the waveforms of drain voltage also differ (compare figure 2.11). The related drain efficiency performance for different phase angles of fundamental load are shown in table 2.1.

Because of some parasitical series resistance of device, the second harmonic load is also not pure reactive. This will also change the phase angle of second harmonic voltage and causing similar problems as above.

Second, as we have previously discussed above, another factor which affect the shape of drain voltage waveform is amplitude ratio of fundamental and second harmonic voltage. The ratio for optimal class J is $\frac{A}{B} = 2\sqrt{2} = 2.828$. What happens if we change this ratio? To investigate this we choose the ratio as 9, 3, 1 respectively and check the drain voltage waveform:

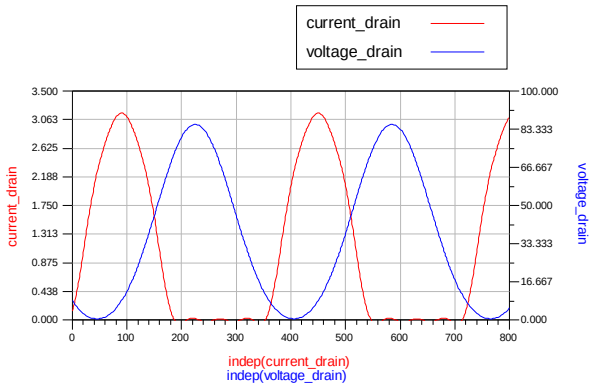


Figure 2.12 (a) The influence of amplitude ratio of fundamental and second harmonic voltage. A/B=9. The DC voltage is adjusted to 38.5 V to make the drain voltage valley reach 0.

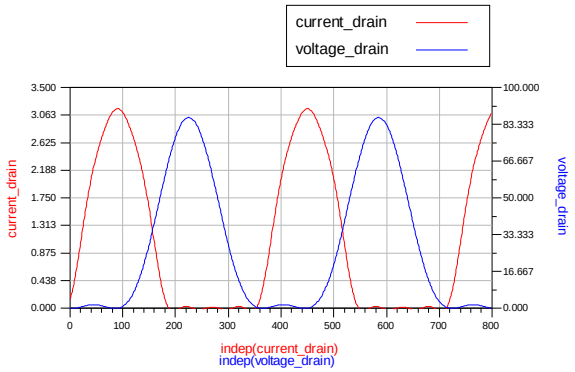


Figure 2.12 (b) The influence of amplitude ratio of fundamental and second harmonic voltage. A/B=2. The DC voltage is 30 V to make the drain voltage valley reach 0.

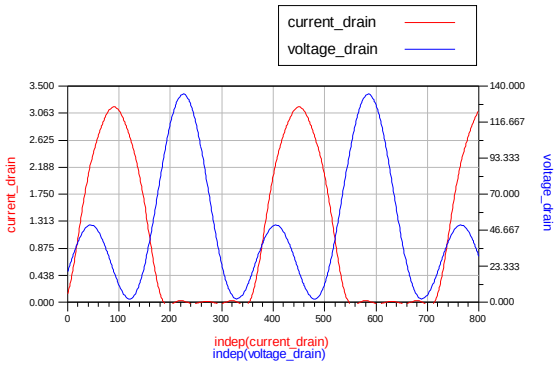


Figure 2.12 (c) The influence of amplitude ratio of fundamental and second harmonic voltage. A/B=1. The DC voltage is adjusted to 50 V to make the drain voltage valley reach 0.

We calculate the efficiency of the efficiency from different ratio of A and B and get

the following results:

Ratio of A/B	Drain efficiency
9	64.9%
3	76.2%
1	56.5%

Table 2.2 Ratio of A/B versus drain efficiency

We can see: when the ratio is 9, the amplitude of second harmonic voltage is much smaller than that of fundamental harmonic voltage. The drain voltage is almost the same as the waveform of class-AB/B. When the ratio decreases to 3, the voltage waveform is more flat in this lower range, so. it's close to the optimal class-J waveform. When the ratio reduces to 1, the amplitudes of the fundamental and second harmonic voltage waveform are equal. The lower peak of the drain voltage becomes higher. The higher peak of fundamental voltage becomes shaper, which will exceed the breakdown voltage when the supply voltage of PA is high.

When the ratio of A/B is around 3, the efficiency performance is the best. When the ratio becomes higher or lower, the efficiency drops.

Two factors will affect the amplitude ratio. One is the phase angle and load value of fundamental harmonic load. The other is the value of second harmonic reactive load. If we have an inductive load, the imaginary part of the load will shift with frequency on the smith chart as shown in figure 2.12.

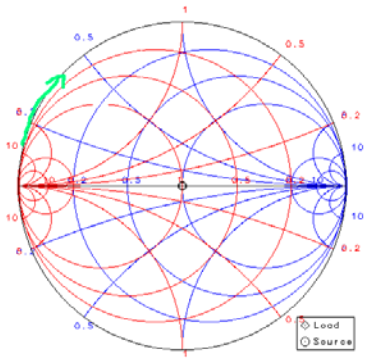


Figure 2.13 Imaginary part of load shifts with frequency (green arrow)

The amplitude of second harmonic voltage is determined by the values of second harmonic load: jwL. When w or L increases, the amplitude of second harmonic voltage will increase. So, we can choose the value of L to tune the ratio A/B.

We discussed the sub-optimal class J operation above. It's will prove to be applicable for supply voltage modulation and wideband design. For other practical problems of sub-optimum class-J, we will discuss them in next chapter when we realize the circuit.

Section 6 Conclusion:

In this chapter, we discussed the principles of class-J and sub-optimum class-J operation. The optimum class-J operation can give us a peak drain efficiency of 78.5%.We can obtain class-J waveform if we use second harmonic to tune the drain voltage waveform of class-AB/B operation. This kind of operation is meaningful when we can't perfectly short the second harmonic. In next chapter, we will discuss how to realize a class-AB/B and class-J power amplifier.

Chapter 3 Design of a “Narrowband” Hybrid Class Power Amplifier for EER or ET system operation

In this chapter, we will discuss the optimum loading for a power amplifier using hybrid-class operation and its related matching network.

The definition of hybrid-class power amplifier in this work refers to the situation that the power amplifier changes operation class with frequency, or time-varying supply voltage. A narrowband power amplifier in an EER (Envelope Elimination and Restoration) or ET (Envelope Tracking) system, can operate at different classes at different supply voltages. For our design in this chapter, the power amplifier operates in class-J/E at lower supply voltages and in class-AB/B at higher supply voltages. We will discuss this operation in more detail in the following sections. For the wideband power amplifier, the amplifier does not only change operation class with supply voltage modulation, but also with frequency. We will talk about the wideband hybrid class PA in the next chapter.

In this chapter we first discuss a “narrowband” hybrid power amplifier design. As we have discussed in chapter 2, we short all the harmonics except the fundamental to make a class-AB/B power amplifier. Or, we can use the second harmonic to tune the drain voltage waveform to make a class-J power amplifier. Both of them have a theoretical peak efficiency of 78.5%. But, due to device parasitics behave differently. Which class operation is more suitable for our device, still needs to be investigated. Of course, the efficiency is only one of the specifications. The other specifications, like power gain, peak output power, peak drain efficiency, etc, are also very important. So, we will realize both classes to find the best operation for our device.

Before beginning our design, we should first have some knowledge of the device we use. So, in section 1, we discuss the device properties and package parasitics.

In section 2, we design two “narrowband” power amplifiers optimized for fixed supply voltage operation.

We design a “narrowband” power amplifier optimized for the efficiency at power back-off in section 3 and comment on the advantages and disadvantages of it.

In Section 4 and 5, we use lumped elements and transmission lines to complete the PA design.

Section 1: Device properties:

Before we start to design, we first should know the properties of the device. The device properties are as follows:

1. Device: NXP's latest generation 7 LDMOS technology, (12 W output power).
2. Channel length: 750 um
3. Cell pitch: 250 um
4. Cells: 7
5. Drain breakdown voltage: 65 V
6. Gate breakdown voltage: Larger than 20 V
7. Threshold voltage: 2.25volts (figure 3.1):

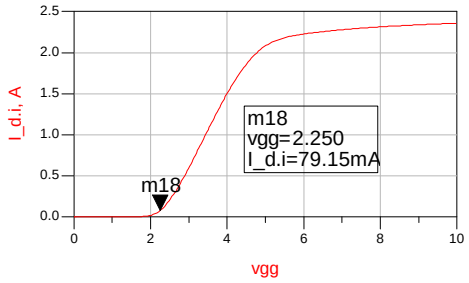


Figure 3.1 The threshold voltage of the LDMOS (I_d represents drain current and vgg is the gate voltage).

8. Saturation drain current: For different drain supply voltages, the saturation drain current is different. It's between 1.7 (@6V vdd) to 2.2 (@30 V vdd) Amperes, and the corresponding gate voltage is around 5 to 6 volts (figure 3.2). The maximum linear output power of the device is determined by the saturation currents.

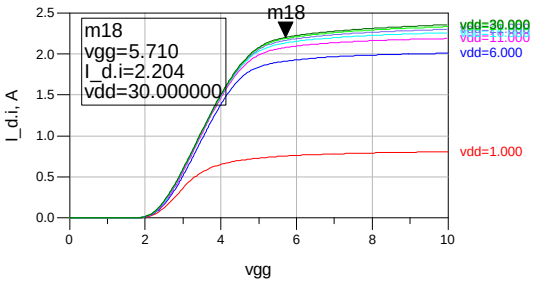


Figure 3.2 Saturation currents of the device. Different colors represent different drain supply voltages. Vgg is the gate voltage (in Volts) and I_d (in Amperes) is the drain current.

9. Parasitic capacitance and resistance of the device: The parasitic components of the device will affect the input and output matching. Especially, the output capacitor of the device has non-linear relation with the supply voltage. The reactance value of this output capacitor will also shift with frequency, which will make the wideband matching more complicated.

We choose the central frequency (2.14 GHz) for testing and check how the parasitic capacitances and resistances vary with the supply voltage (Vdd).

Drain capacitance (figure 3.3):

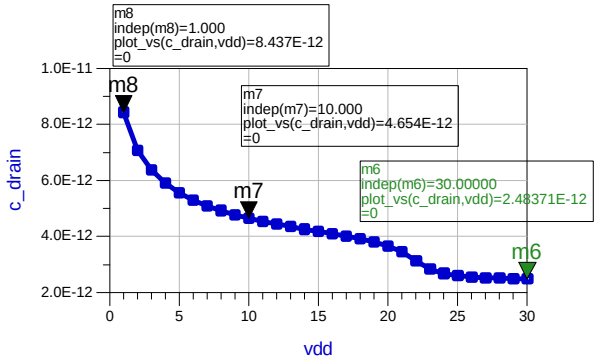


Figure 3.3 Drain parasitic capacitance versus supply voltage (The units are F and V respectively)

We can see from figure 3.3 that the drain parasitic capacitance is 8.43 pF at 1 volt and strongly decreases with rising vdd.

For the gate parasitic capacitance consider (figure 3.4):

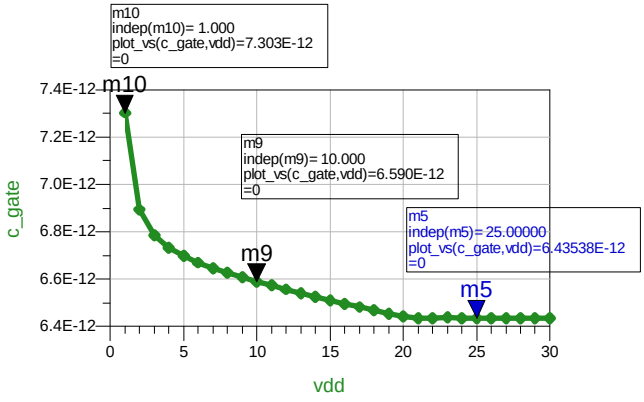


Figure 3.4 Gate parasitic capacitance versus supply voltage (The units are F and V respectively)

When the supply voltage varies from 10 V to 30 V, the gate parasitic capacitance doesn't change so much (6.59 pF to 6.43 pF, Figure 3.4). So, for operation with supply voltage modulation, the gate parasitical capacitance is not a big problem.
The output capacitance affects the matching. For example, if we want to design a

class-B power amplifier, the optimum load for this PA is Zload, which should be a purely resistive load. However, due to the existence of output capacitance, we need an inductive load to compensate this capacitor. See figure 3.5.

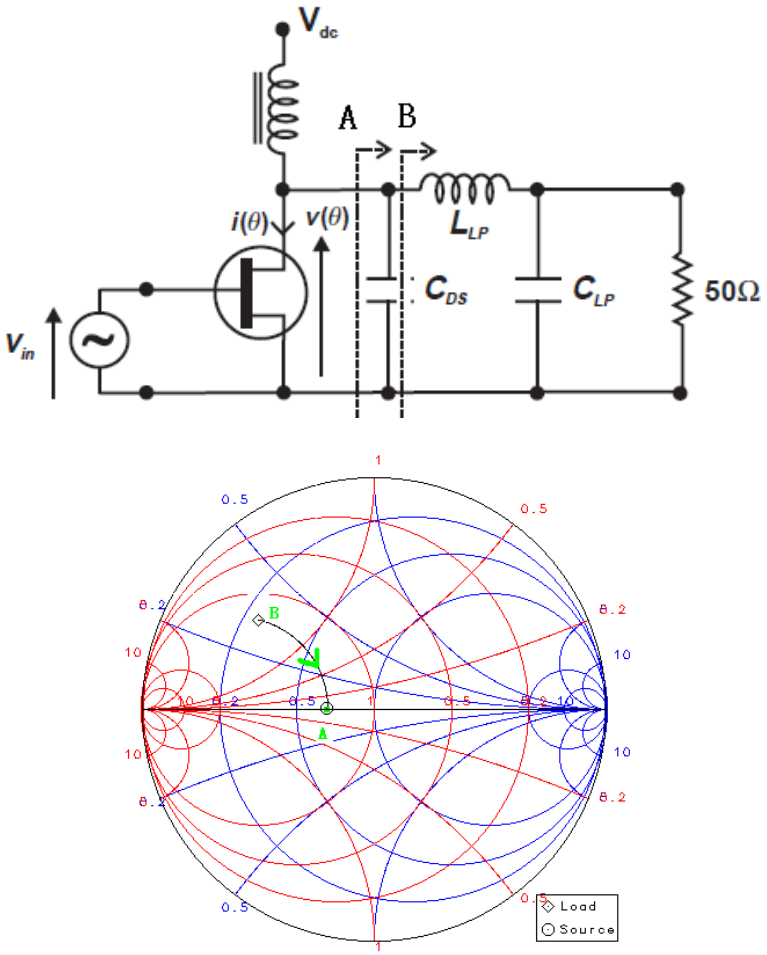


Figure 3.5 The load seen from reference plane A and B

In the above graph of figure 3.5, from reference plane B we get an inductive load as shown in lower graph of figure 3.5. Cds is the output capacitor. So, seen from reference plane A, the load should be pure resistive (point A on the Smith chart). This kind of compensation for single frequency design is easy to do. But, when applying supply voltage modulation and wideband operation, it becomes more difficult since the reactance value of this capacitor will change a lot with supply voltage and frequency. In addition we want a simple matching topology with fixed value components to compensate it. The method to solve this problem will be discussed in the later sections.

The gate and drain parasitic conductance will also vary with supply voltage (figure 3.6):

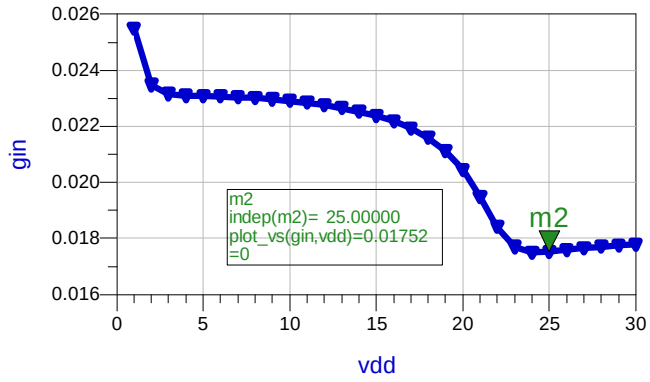


Figure 3.6 (a) Gate (gin) parasitic conductance vary with supply voltage (The units are S and V respectively)

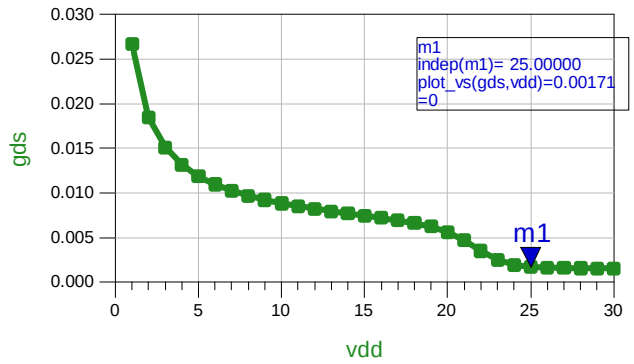


Figure 3.7 (b) Drain (drain) parasitic conductance vary with supply voltage (The units are S and V respectively)

The gate conductance is around 0.02 S which is equivalent to a shunt resistance of 50 Ohms for different supply voltage values. And, the drain conductance reduces from 0.025 to 0.0017 S (resistance from 50 Ohms to 500 Ohms) with supply voltage increases from 10 to 30 volts. This parasitic conductance will cause power dissipation. So, the device will have more power loss, lower efficiency and lower power gain at lower supply voltage than that at higher supply voltage.

When we design the input and output matching network, we should take these parasitic components into account:

$$Y_{opt} = \frac{1}{Z_{opt}} = g_{opt} + jb_{opt} \quad (1)$$

$$g_{opt} = g_{load} + g_{parasitic} \quad (2)$$

$$b_{opt} = b_{load} + b_{parasitic} \tag{3}$$

So, the loads we want to design:

$$g_{load} = g_{opt} - g_{parasitic} \tag{4}$$

$$b_{load} = b_{opt} - b_{parasitic} \tag{5}$$

$$Y_{load} = g_{load} + jb_{load} = \frac{1}{Z_{load}} \tag{6}$$

10. Parasitic of package: The package used in our design is NXP SOT 467 package. In order to include the effect of the package in our design, we should model the parasitical components of the package.

As shown in Figure 3.8, the drain, gate and source bond wires have been modeled:

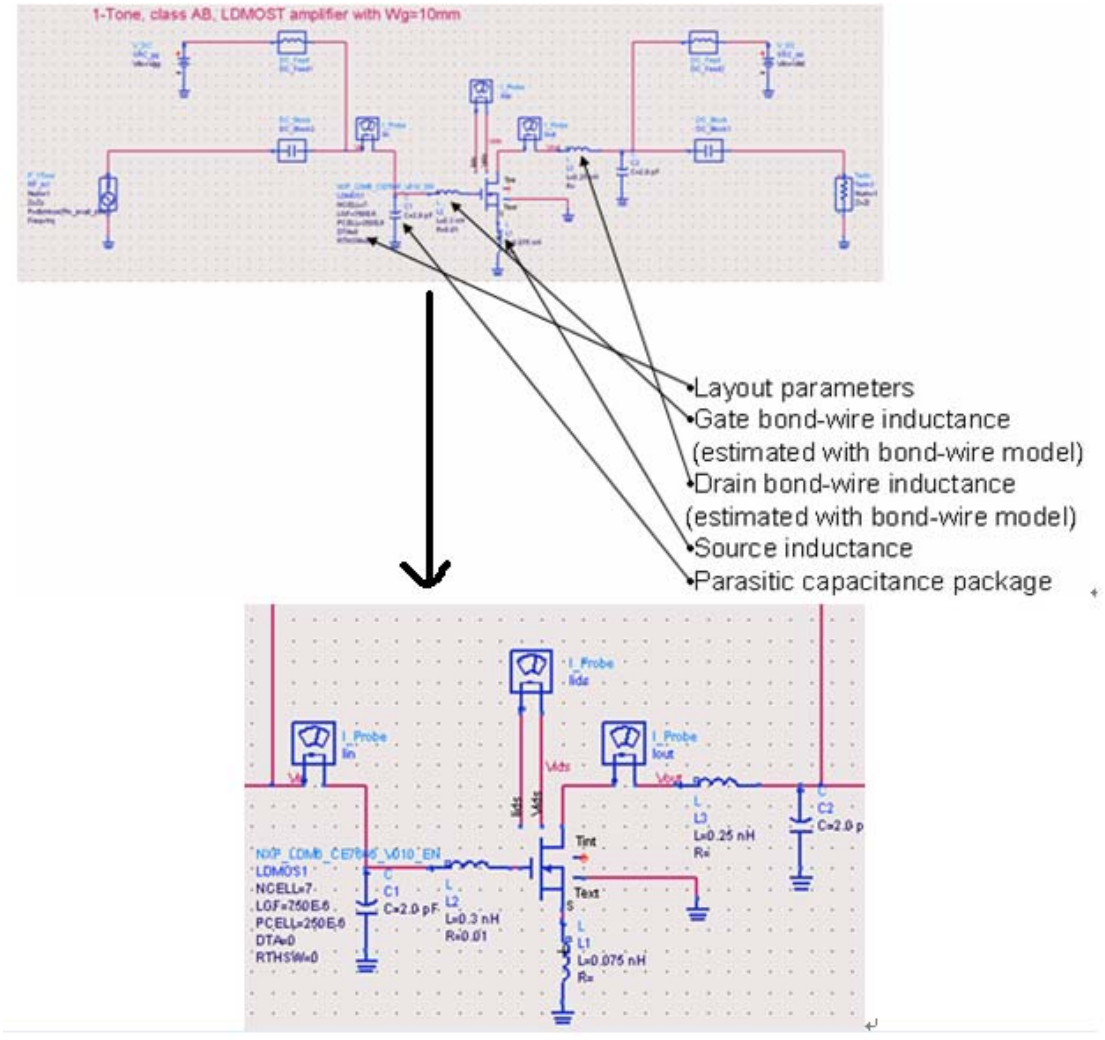


Figure 3.8 The modeled components of package parasitic

The parasitic inductance at source is 0.075 nH. The parasitic inductance, resistance and capacitance at gate are 0.075 nH, 0.01 Ohm and 2.0 pF respectively. The parasitical inductance and capacitance at drain is 0.25 nH and 2.0 pF respectively.

For the gate and drain package parasitics, we can absorb them in our matching design. As long as we achieve the optimum load, the performance will be the same.

Suitable operation class for NXP LDMOS: Due to the existence of parasitics of device and package, we need to identify, which class of operation is more suitable for this device. Typically, we can improve the efficiency with harmonic tuning. However, if the frequency is very high, the loss of parasitics will become significant. There will also be some loss at the harmonics. In this case, we can get higher efficiency when the harmonics are shorted.

Performance at power back-off: In addition, to find the optimum operation conditions we should consider the fact that in an operation with a WCDMA signal, the supply voltage varies a lot with time. In terms of output power, the power amplifier will operate most of the time at 6 to 11 dBm power back off. So, our target will be not to get the highest efficiency at a single supply voltage point, but, obtain the highest average efficiency according to the PDF of WCDMA signal (appendix 1).

Section 2: Optimizing the load condition for single supply voltage

Before considering the optimum load condition for power back-off, we first discuss how to optimize the load condition for single supply voltage with class-AB/B and class-J operations.

Class-AB/B operation optimized for single supply voltage: For class-AB/B operation, we should short the harmonics and only emphasis on the fundamental frequency load. We summarize the steps to find the optimum load of class-AB/B operation for single supply voltage.

1. The first step is to choose the input power. The input of power amplifier is a large signal which will change its bias condition. Each device has its own 1 dB compression point in terms of output power for a single supply voltage value, the corresponding input power we call it input 1 dB compression point. Mostly, the input power should be chosen as the input 1 dB compression point. Otherwise, the power amplifier can’t achieve the maximum output power. But, if we choose the input power much higher than the input 1 dB compression point, the device will be over-driven too much, which will make the power amplifier degrade or will yield even device failure over time. We don't know the 1dB compression point before we finish our design. So, the strategy is we first estimate the input power value according to the gain of the device technology. After finish the matching network, we check the 1 dB compression point and adjust the input power.

2. The second step is the design of input matching. In order to guarantee we can transform the highest power from source to the transistor, the input of the transistor should be conjugate matched. The stability issue will be discussed in the following sections.

3. The third step is to estimate the optimum output load. For class-AB/B power amplifier, the equation for calculating the optimum load is $\frac{Vdd^2}{2 \times P_{out}}$, where Vdd is the supply voltage, Pout is the output power you want to obtain. Normally, it's the maximum linear output power for a device for a given voltage as we discussed previously. However, this equation can only be used to calculate the optimum load for ideal device (no parasitic). The real device always contains some parasitic capacitance and resistance and we should compensate for them. So, we can get a load whose real part is the optimum resistor for class-AB/B and imaginary part can compensate the output capacitance of the device (as shown in equation 1 to 6).

4. In step 3, we should have a good estimation for the optimum load. But, there are still some non-ideal situations of the device which can't be predicted. So, load-pull simulations are necessary. So, in step 4, we do the load-pull simulation to find out the point on the Smith chart where the efficiency is the highest. Notice that the peak efficiency and the peak output power do not necessarily are at the same point in the Smith chart. We should make a compromise between them to make sure we can achieve a good efficiency performance and peak output power simultaneous.

Now, we start the test to find the optimum load of class-AB/B operation with single supply voltage:

1. These are the simulation parameters:

(1). Drain supply voltage: 30 Volts;
(2). Gate voltage: 2.25 Volts (the threshold voltage of this device)
(3). Design frequency: central frequency of WCDMA signal, 2.14 GHz
(4). Input power: the input power are chosen as 23 dBm. The reason is: normally, the base station power amplifier has a gain of 15 to 20 dB, and this device's maximal linear output power is 12W (40.7 dBm). Thus, the input power should be output power minus power gain, which is between 20 to 25 dBm. Here, we make a compromise to choose 23 dBm as our input power. After finishing the matching for the device, we can check the 1 dB compression point to modify the input power.

2. The test schematic for input and output matching (Figure 3.9):

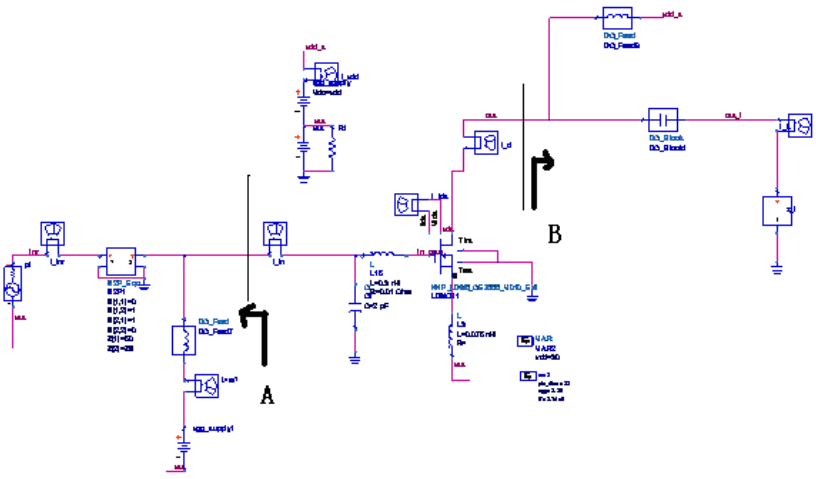


Figure 3.9 Testing schematic for input and output matching. The arrows represent the reference planes and direction we see the loads of matching networks.

We use the ideal equations components of ADS to find the optimum loads for input and output matching before we realize it. The reference planes and direction we see the loads are shown in figure 3.9 (position A and B). All the load conditions we will discuss later are all seen from this direction. Here we don't include the drain parasitics of package because we can include these in the load realization after we have found the optimum load.

3. Input matching: conjugate match the input (figure 3.10 and 3.11):

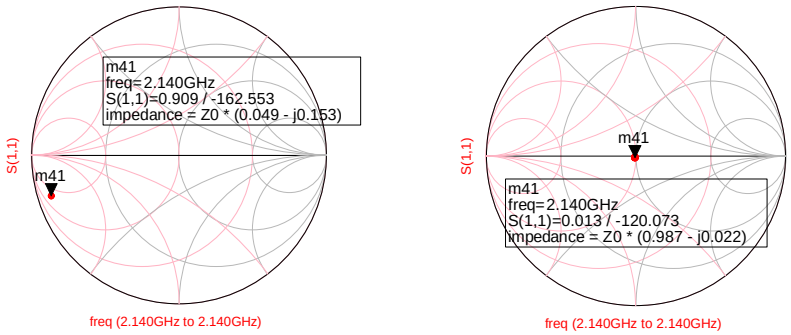


Figure 3.10 S11 parameter of the device before (left) and after (right) input matching. (Normalized to 50 Ohms)

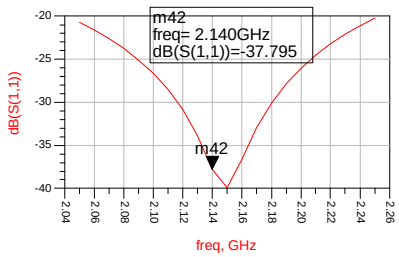


Figure 3.11 S 11 of the device after input matching

Figure 3.11 shows that the device has been conjugate matched at 2.14 GHz

4. Base on this conjugate input match, we do the output matching. The power amplifier operates at class-AB/B, so, the second harmonic (4.28 GHz) and higher order harmonics (6.42GHz, 8.56 GHz, etc.) should be shorted (Figure 3.12). Then, we estimate the optimum value of fundamental load for 30 V supply voltage. The equation to calculate the optimum load:

$$\frac{VDD^2}{2\times pout} = \frac{30^2}{2\times 12} = 37.5Ohm\,\mathrm{s} \qquad (7)$$

Vdd is the supply voltage and pout represents the peak output power (for this device, it's 12 W). So, for convenience, the Smith chart for load matching can be normalized to 30 Ohms.

Then, we check the drain output capacitor of this device: It's around 2.5 pF and –j*29.7 Ohm / j*0.034 S at 2.14 GHz. We need an inductive imaginary part of the output load to compensate the effect of drain parasitical capacitor. The inductive part should be j*29.7 Ohms/ -j*0.034 S. When it normalizes to 30 Ohms, it's around 1.

So, the estimated optimum output load should be around 0.027–j*0.034 S (0.8–j*1 S, when normalized to 30 Ohms). In order to find the true optimum output load in this case, we must do the load-pull simulations based on the estimated value. The load-pull simulation results are as shown in figure 3.12:

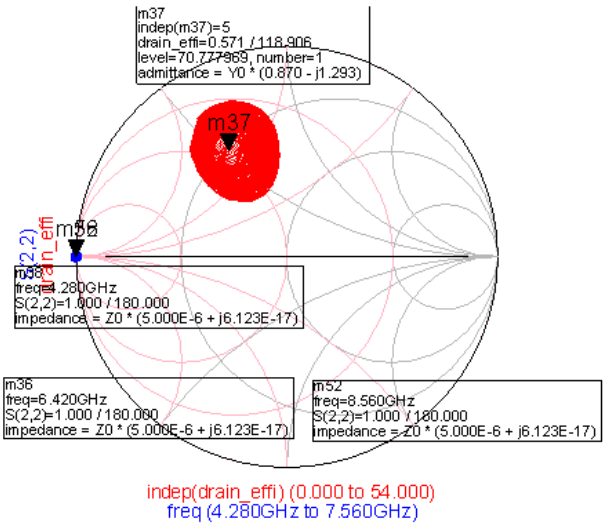


Figure 3.12 Load- pull simulation results for class-AB operation

The Smith chart is normalized to 30 Ohms (blue, higher order harmonics loads. Red, fundamental harmonic efficiency contours. The contours represent the region where efficiency is higher than 60%)

From figure 3.12, we can see the second and higher order harmonics are shorted (blue). The optimum fundamental harmonic load can be found from efficiency contours on the Smith chart (red). At the same time, we should consider whether the

power amplifier reaches the peak power (40.7 dBm). So, we also need to check the power contours on the Smith chart (Figure 3.13)

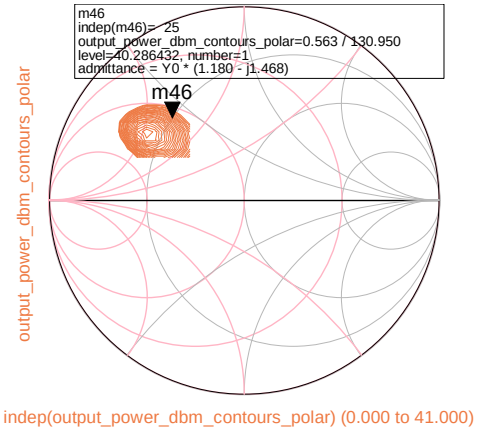


Figure 3.13 Output power contours (contours for output power higher than 40 dBm). The Smith chart is normalized to 30 Ohms

The peak drain efficiency and peak output power point are not at the same position. Trade-off should be made between efficiency and output power. The highest efficiency point is 0.87-j*1.29 S which is very close to the estimated value (0.8 – j*1 S). Here, we choose load value 1-j*1.25 S. With this load, the drain efficiency is around 65% and the peak power is 40.7 dBm. We match the output to this optimum load using ADS ideal components and check the performance (Figure 3.14).

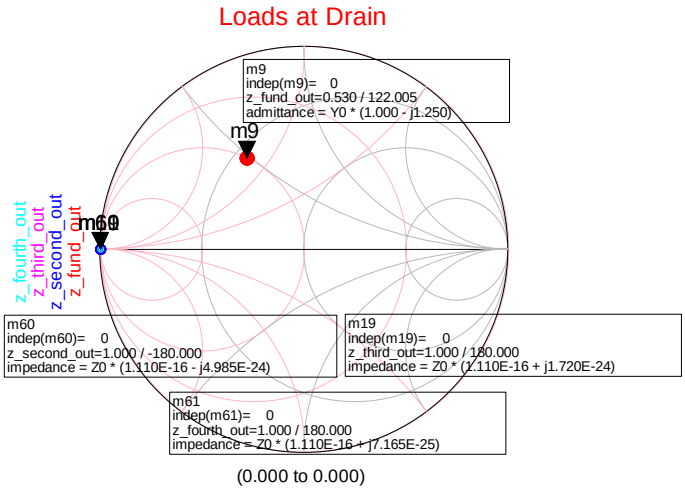


Figure 3.14 (a) The optimum output load seen from external drain (including package parasitics and excluding device parasitics) for 2.14 GHz and 30 V supply voltage. The Smith chart is normalized to 30 Ohms

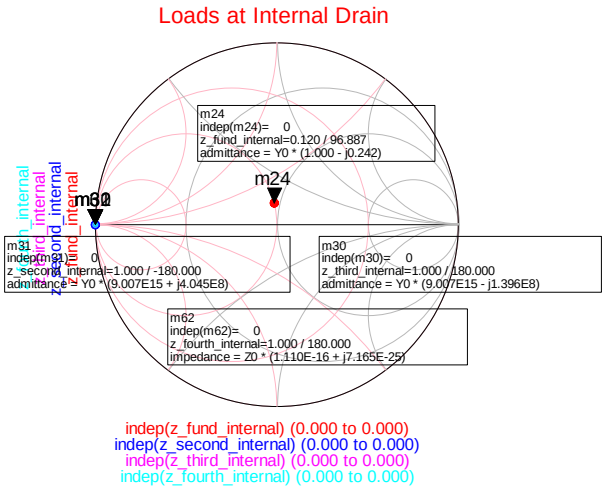


Figure 3.14 (b) The optimum output load seen from internal drain (including both package and device parasitics) for 2.14 GHz and 30 V supply voltage. The Smith chart is normalized to 30 Ohms

The performances of the load condition in figure 3.14 are as follows:

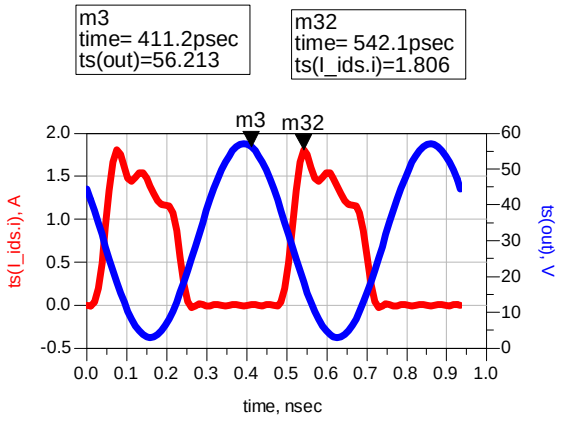


Figure 3.14 (a) Drain current (red) and voltage (blue).

drain_efficiency	..._added_efficiency	output_power_dbm	power_gain
70.489	69.391	40.870	18.075

Figure 3.14 (b) Simulation results of load condition in figure 3.14

The peak drain voltage is 56 V which is lower than the drain breakdown voltage (65

V). The peak drain current is 1.8 A which is also below the saturation current. The output power is 40.87 dBm which approximates the peak power and the drain efficiency is 70.5%. PAE is 69.3%. The output power gain is 18 dB.

As we have mentioned previously, in WCDMA system, the power amplifier often operates 6 dB or more from the peak power. So, we should check how this output load performs at power back-off point if we vary the supply voltage.

Class-J operation optimized for single supply voltage: Both the class-E and class-J power amplifiers use the harmonics to tune the drain voltage to obtain better efficiency performance. The difference is ideal class E power amplifier use infinite harmonics (2^{nd} ,3^{rd},4^{th},5^{th}……harmonics) to tune the drain voltage. For ideal class E operation, the drain voltage should meet two requirements: 1. Drain voltage should be zero when the transistor on. 2. The slope of the drain voltage should be zero when the transistor on. But, due to the non-ideal conditions of the device (parasitic capacitances and resistances), the ideal class E requirements are difficult to meet. So, we often only tune the 2^{nd} and 3^{rd} harmonic to get sub-optimum class-E power amplifier solutions.

Class-J can be considered as the middle class Between class-AB and sub-optimum class-E. For class-J operation, we only tune the second harmonic. In this way, we can make our matching network simpler and the performance isn't in practice much lower than for class E.

The steps to find out the optimum load of class-J operation with single supply voltage:

1. Input power is chosen as 24 dBm. The reason is similar to class-AB/B operation.
2. Again, the same, we conjugate match the input of the transistor.
3. For class-J operation, we should estimate the loads for both fundamental harmonic and 2nd harmonic. We have discussed in chapter 3: for class-J operation, there are 2 solutions for the load. The fundamental load is inductive (capacitive) and the second harmonic load is capacitive (inductive). For our design we choose capacitive fundamental load and inductive 2^{nd} harmonic load. The reason is we have an output capacitor of the device. If we choose inductive fundamental load, it should be more inductive for output capacitance compensation consideration. The fundamental load may be very near the edge of the Smith chart. It's not convenient for our design.

   The equation to calculate the fundamental harmonic load is:

$$Z_{fund} = \frac{V_{DD}{}^2}{\sqrt{2} \times P_{peak}} \angle -\frac{\pi}{4} = \frac{30^2}{\sqrt{2} \times 12} \times (\cos(-\frac{\pi}{4}) + \sin(-\frac{\pi}{4})) = 37.5(1-j)$$

(8)

When it's normalized to 30 Ohms, it's 1.25*(1-j).

$$Y_{fund} = \frac{1}{Z_{fund}} = 0.4 + j0.4 \qquad (9)$$

The output parasitical capacitor is around 2.5 pF at 30 supply voltage. It's j*0.034 S at 2.14 GHz, and j*1 S when normalized to 30 Ohms.

Thus, the fundamental harmonic load on the Smith chart should be:

0.4+j*0.4-j*1=0.4-j*0.6 S. (normalized to 30 Ohms) (10)

And the second harmonic load is:

$$Z_{second} = \frac{3\pi \times V_{DD}^2}{16 P_{peak}} \angle \frac{\pi}{2} = j44.2Ohms \quad (11)$$

$$Y_{second} = \frac{1}{Z_{second}} = -j0.0226S \quad (12)$$

When it's normalized to 30 Ohms, it's –j*0.68 S.

The output parasitical capacitor is around 2.5 pF at 30 supply voltage. It's j*0.068 S at 4.28 GHz, and j*2 S when normalized to 30 Ohms.

Thus, the second harmonic load on the Smith chart should be:

-j*0.68-j*2=j*2.68 S (normalized to 30 Ohms) (13)

4. Load-pull simulation: Now, we have three variables: real and imaginary part of fundamental harmonic load and imaginary part of second harmonic load (the second harmonic load should be a pure reactance to minimize the loss at second harmonic load). We choose a second harmonic load value and do the load-pull simulations for fundamental load (figure 3.15).

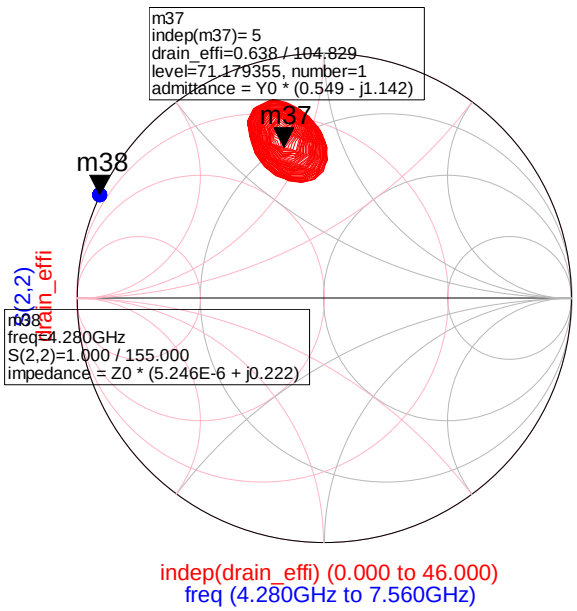


Figure 3.15 High efficiency region by load-pull. (the Smith chart is normalized to 30 Ohms. Red, high efficiency region for fundamental load. Blue, second harmonic load)

5. From figure 3.15 and based on the estimation of fundamental harmonic load, we choose 0.4-j*1 S (normalized to 30 Ohms) as our fundamental harmonic load. And then, we sweep the second harmonic load (Figure 3.16).

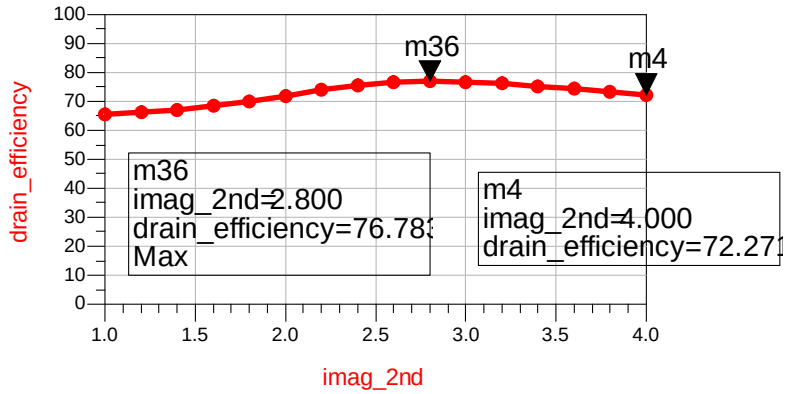


Figure 3.16 Sweep second harmonic loads (the second harmonic reactance is normalized to 30 Ohms)

6. We choose the optimum load for second harmonic we repeat step 4 and 5 twice or three times, we can find the optimum loads for both fundamental and second harmonic.

The optimum load condition of class-J operation for 30 V supply voltage:(Figure 3.17):

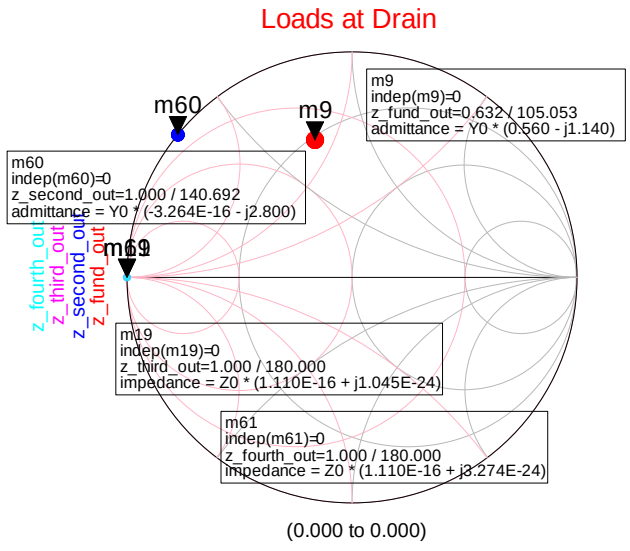


Figure 3.17 (a) Optimum loads for 2.14 GHz, 30 V supply voltage class-J power amplifier (normalized to 30 Ohms, seen from external drain)

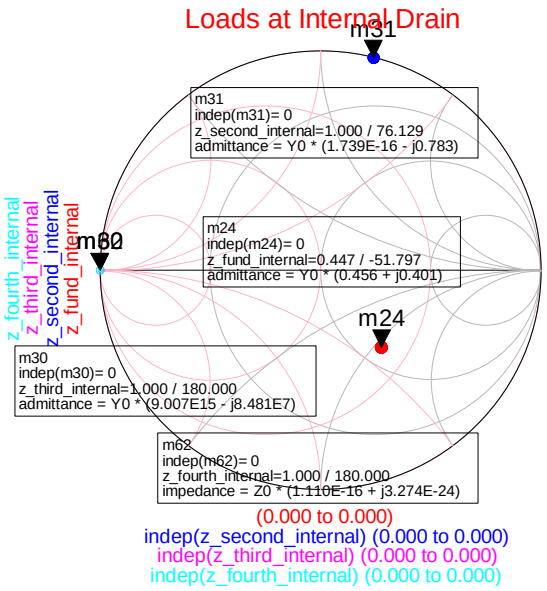
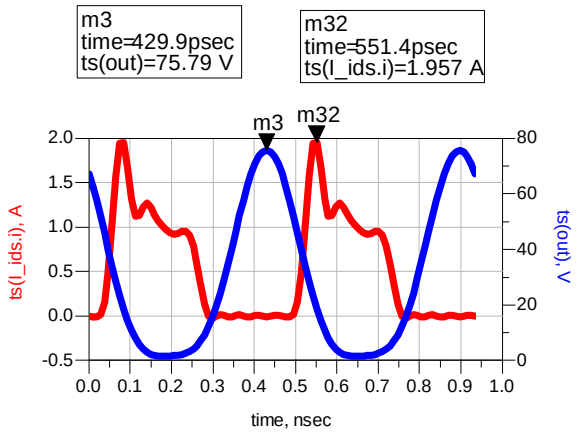


Figure 3.17 (b) Optimum loads for 2.14 GHz, 30 V supply voltage class-J power amplifier (normalized to 30 Ohms, seen from internal drain)

The load seen from external drain:
Fundamental load: 0.56-j*1.14 S (normalized to 30 Ohms, the same for the follows)
Second harmonic load: -j*2.8 S

The load seen from internal drain:
Fundamental harmonic load: 0.46+j*0.4 S
Second harmonic load: -j*0.78 S
These two values are very close to the values we estimate from the equations.

The other simulation parameters are the same as those of class- AB/B operation. The simulation results (Figure 3.18):



drain_efficiency	power_added_efficiency	output_power_dbm	power_gain
77.282	76.291	41.089	18.923

Figure 3.18 Simulation results of load condition in figure 3.17. Upper graph, blue and red represents drain voltage and current respectively.

For class-J operation, the drain efficiency rises to 77.3%. The gain is 18.9 dB (all other test conditions are the same except the load condition compared with class-AB/B). We see from figure 3.18, the drain voltage waveform is more flat at lower drain voltage compared with class-AB/B and its peak is more shaper. But, we also notice that the peak drain voltage is 75.8 V, which is much higher than the drain breakdown voltage (65 V). This is a restriction for class-J.

Hybrid-class PA for varying supply voltage: The class-J operation can provide higher efficiency with this LDMOS but it has a risk of exceeding the breakdown voltage at higher supply voltages. If we can use class-J operation at lower supply voltage and class-AB/B at higher supply voltage, we can increase the efficiency at power back-off and don't exceed the breakdown voltage at higher supply voltage. In chapter 2, we have discussed that when the ratio of amplitudes for second and fundamental component of drain voltage is less than 1/10, the drain voltage waveform is almost like a class-AB/B waveform. When this ratio rises to 1/3, the drain voltage waveform becomes like a class-J waveform. So, we can choose the second harmonic load to tune this ratio at lower and higher supply voltages so that the power amplifier operates at class-J at lower supply voltage and class-AB/B at higher supply voltage. This is the main idea of hybrid-class power amplifier.

Section 3 Optimizing load condition for efficiency at power back-off:

As we have mentioned previously, in WCDMA system, the power amplifier often operates 6 dB or more from the peak power. So, in this section we try to find the optimum load condition for average efficiency (according to the PDF of WCDMA signal, appendix 1).

Class-AB/B operation optimized for the efficiency at power back-off: Since we have knowledge on the PDF of the WCDMA signal we know that the supply voltage varies between 15 to 20 V most of time. So, we need modify our design steps for class-AB/B operation in section 1 to meet the requirement for supply voltage modulation.

2. Input powers are chosen at 1 dB compression points for each supply voltage (figure 3.19):

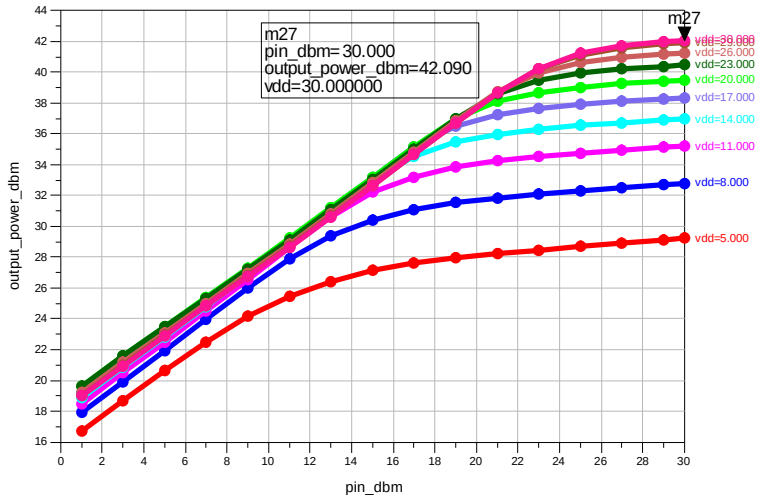


Figure 3.19 Input power (dBm) vs. output power (dBm) at 2.14 GHz class-AB/B operation. Different colors represent different supply voltages (from 5 V to 30 V)

3. Conjugate match the input
4. Estimating the load for 10 V, 20 V, 30 V supply voltage as we did previously for 30 V supply voltage.
5. Do load-pull simulations to find the common high efficiency region (larger than 60%) for different supply voltage values (figure 3.20). We have estimate the optimum load for 30 V, the optimum loads for other supply voltage values should be near it.

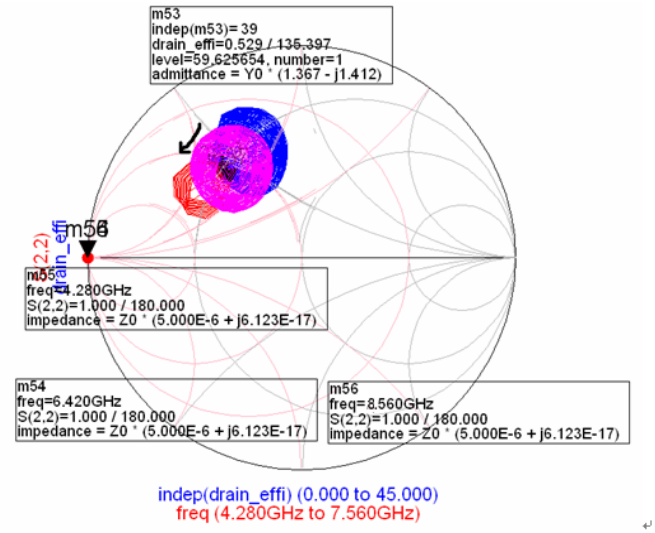


Figure 3.20 (a) Load-pull simulations for different supply voltage (Red, pink, blue represent 10 V, 20 V and 30 V respectively, the Smith chart is normalized to 30 Ohms. The contours represent the regions where the drain efficiency is higher than 60%)

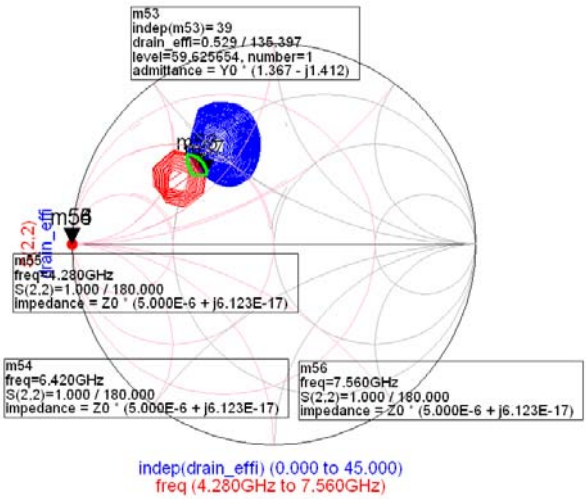


Figure 3.20 (b) Load-pull simulations for different supply voltages (Red, blue represent 10 V and 30 V respectively, green region represents common high efficiency region, where the efficiency is higher than 60% for all the supply voltage values. The Smith chart is normalized to 30 Ohms)

Figure 3.20 (a) represents the high efficiency contours for different supply voltages (10V, 20V, 30V). All the contours represent the region where the drain efficiency higher than 60%. We should notice that the high efficiency contours shift in the anti-clockwise direction and the common high efficiency region is always contained in the 20 V high efficiency region. So, we only need to find the common high efficiency region for 10 and 30 V, then, the efficiency will be high for all supply voltage values (green region in figure 3.20 (b)).

6. Choose the most promising values for the load and calculate the average efficiency according to the PDF of WCDMA signal. Pick out the load value which gives us the highest average efficiency. A good load condition of class-AB/B operation for power back-off is as follow (figure 3.21):

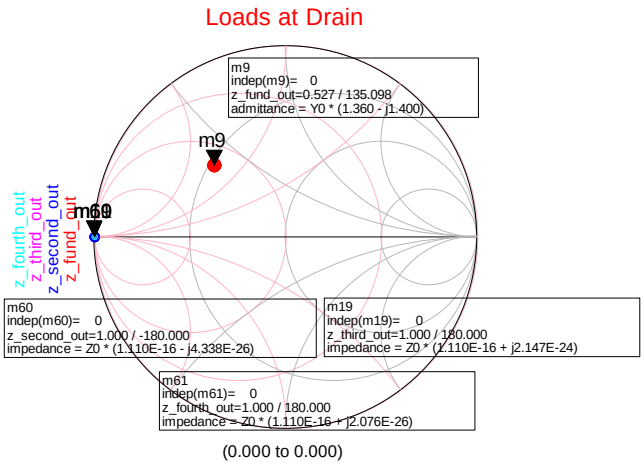


Figure 3.21 Load for high average efficiency (the Smith chart is normalized to 30 Ohms)

The simulation parameters are:

1. Input powers are chosen at 1 dB compression points for each supply voltage.
2. Operation frequency: 2.14 GHz.
3. Gate bias: 2.25 V.
4. Drain supply voltage: 1 to 30 V.

The performances of the load condition in figure 3.21 are as follows:

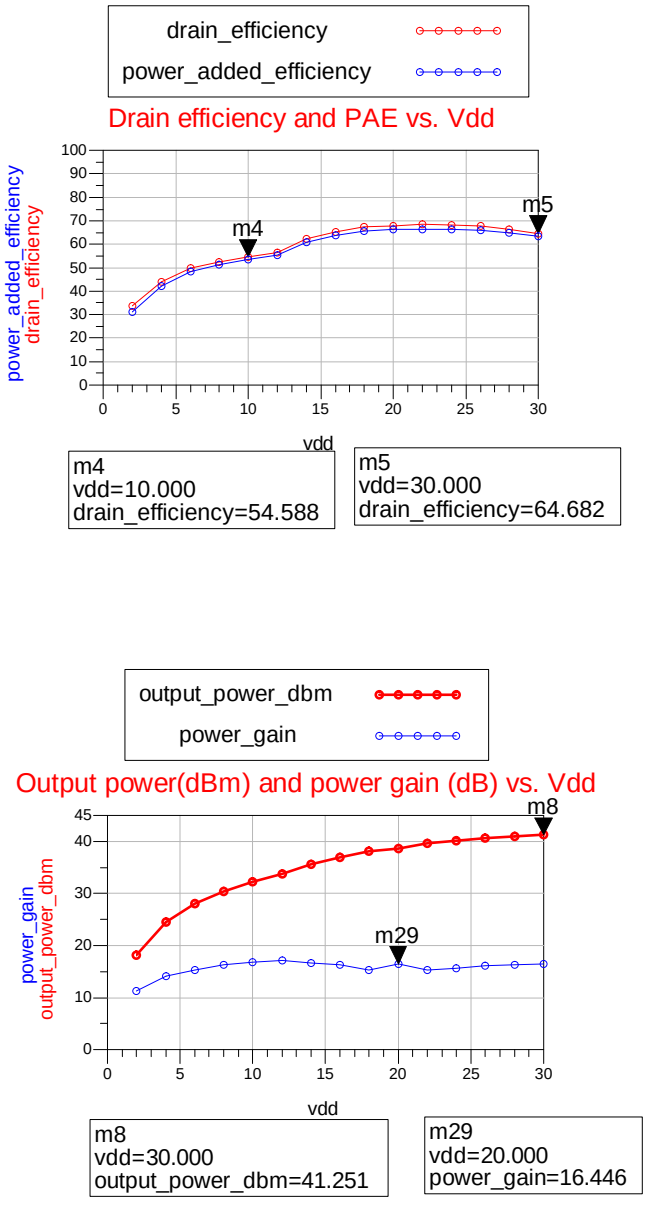


Figure 3.22 (a) Performances of the load optimized for efficiency at power back-off

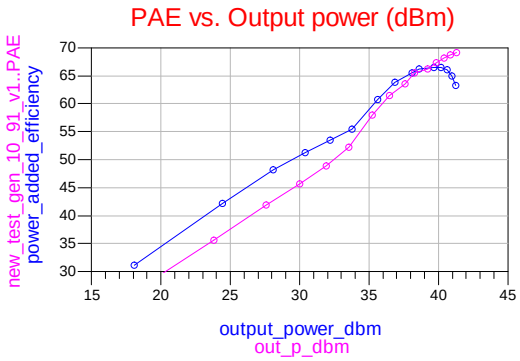


Figure 3.22 (b) Comparison of the PAE versus output power, loading optimized with a 30V supply voltage (pink) and loading optimized for max efficiency at power back-off (blue) (the input is biased below or at the 1dB compression point for each supply voltage)

We can conclude from figure 3.22: The efficiency is fairly flat versus supply voltage and it peaks at 20 volts. From figure 3.22 (b), the PAE is lower at higher supply voltage when load is optimized to the efficiency at power back-off. But, it's higher at power back-off point.

We can check also the performance of other loads. However, fundamental load 1.36-j*1.4 S (normalized to 30 ohms) gives one of the best result, which makes a good compromise between average efficiency and peak output power.

Hybrid-class operation optimized for the efficiency at power back-off:
The definition of hybrid-class operation has been introduced in section2.There are two different ways to design a hybrid class power amplifier:

1. The first one is to optimize the fundamental load at 30 V supply voltage and choose the optimum second harmonic load to improve the efficiency at lower supply voltage.
2. The second one is to choose the fundamental load from the common high efficiency region as shown in figure 3.20. At the same time, the second harmonic load is chosen to improve the efficiency at lower supply voltage. This method will sacrifice the efficiency at higher supply voltage, but obtain better efficiency at power back-off. This method can also maintain the efficiency at power back-off when the second harmonic load has no influence on the performance. It's important when we design wideband PA. We will discuss both of them to find out which method is better.

The steps to design a hybrid class power amplifier:
1. The input powers are chosen at 1 dB compression point for each supply voltage.
2. Conjugately match the input.
3. Estimate the optimum load. We estimate the optimum load for 30 V supply voltage. Optimum loads for other supply voltages are close to it.

4. Do load-pull simulation for fundamental harmonic load. We choose one of the better results as the fundamental harmonic load and sweep the second harmonic load. Then we do the load-pull simulation for fundamental harmonic load again. After repeating this process twice or three times, basically we can find the optimum loads.

The simulation parameters are:
1. Gate bias voltage: 2.25 V
2. Frequency: 2.14 GHz
3. Drain voltage: 1 V to 30V
4. Input power: the input powers are chosen at 1 dB compression points for each supply voltage
5. The input of the power amplifier is conjugately matched.

Optimum fundamental load: The load-pull simulation to find the common high efficiency region for fundamental load (figure 3.23):

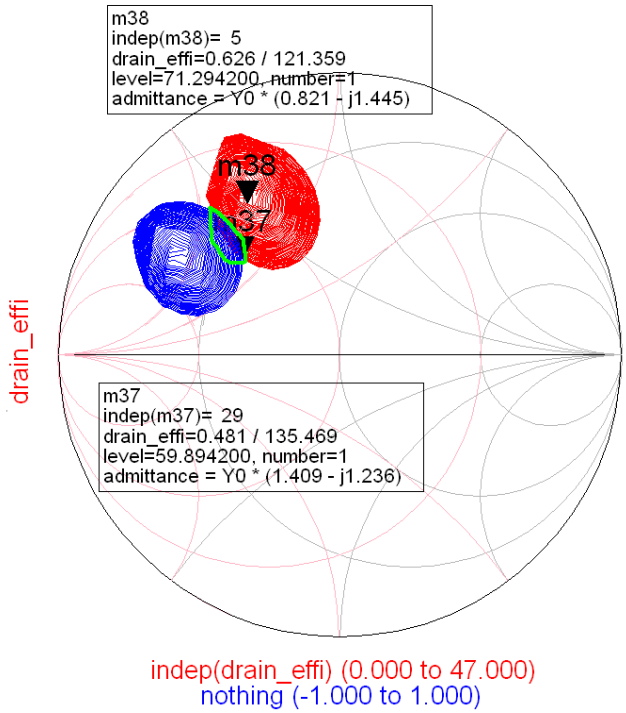


Figure 3.23 Region for high average efficiency. (The contours represent the region where the drain efficiency is larger than 60%. Blue, high efficiency for 10 V supply voltage, red, high efficiency for 30 V supply voltage, green circle, common high efficiency region. The Smith chart is normalized to 30 Ohms. The input power is chosen at 1dB compression for 30 V supply voltage for all load-pull simulations)

The optimum fundamental load for 30 V supply voltage and average efficiency are shown in Figure 3.24.

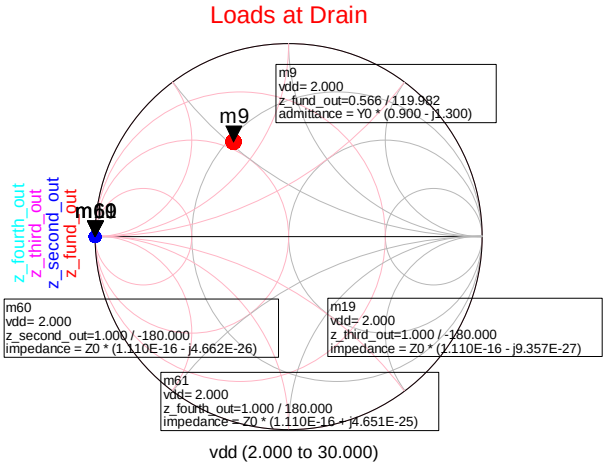


Figure 3.24 (a) The optimum fundamental load for 30 V supply voltage (the Smith chart is normalized to 30 Ohms)

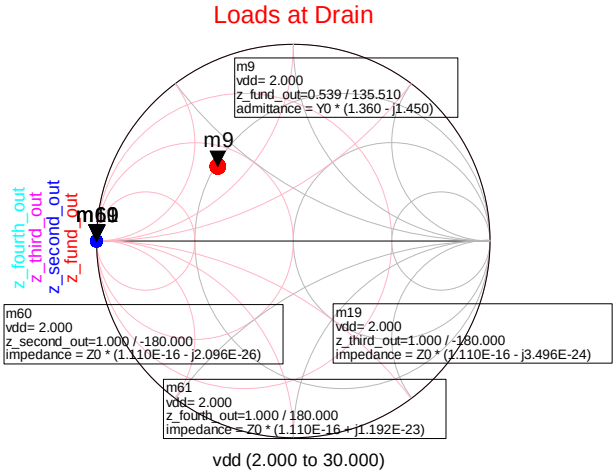


Figure 3.24 (b) The optimum fundamental load for average efficiency (the Smith chart is normalized to 30 Ohms)

Optimum second harmonic load: The way to choose the second harmonic load based on the fundamental load in figure 3.24 (b) is as follow: If we transfer the second harmonic load to polar format (1,angle) (1 and angle represents the magnitude and phase angle of second harmonic load respectively. The magnitude is 1 means that the second harmonic load is pure reactive), we can sweep the phase angle of the second harmonic load to find the optimum value. The result is as follow (figure 3.25):

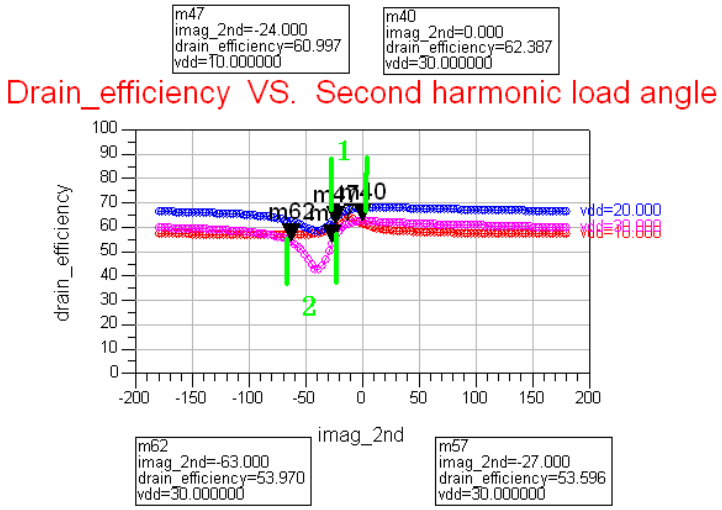


Figure 3.25 (a) Sweep the angle of second harmonic load (polar format). (different colors represent different supply voltage. The input power is chosen at 1dB compression for 30 V supply voltage for the sweep)

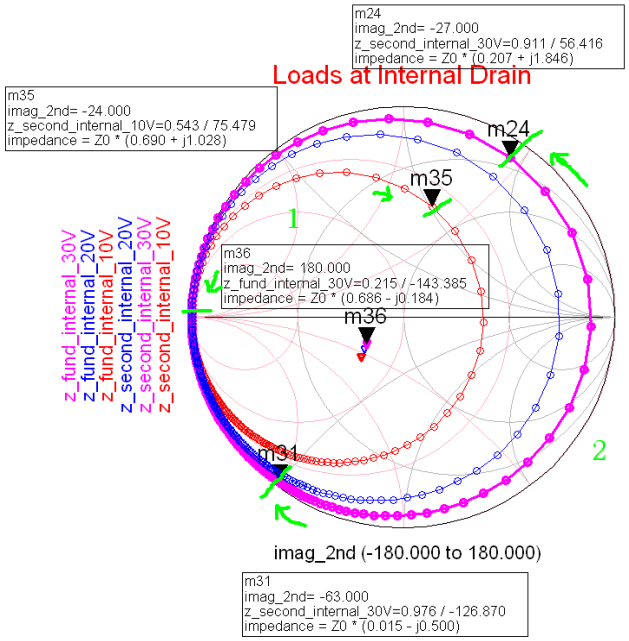


Figure 3.25 (b) Load condition seen from internal drain. Sweep the angle of second harmonic load (polar format). (Pink, 30 V. Blue, 20 V. Red, 10 V. The triangles in the middle of Smith chart represent the fundamental load. The circles represent second harmonic load shift with sweeping angles. The input power is chosen at 1dB compression for 30 V supply voltage for the sweep)

The influence of second harmonic: We can see from (figure 3.25 (a)) that at -12 degree (12.7 S, when in reactance format, normalized to 30 Ohms) we can have an efficiency improvement. When the phase angle is between 0 to-24 degrees (see the green region 1 in figure 3.25), the efficiency performances are improved for all supply voltages. When it's between -27 and -63 degrees (green region 2 in figure 3.25), the second harmonic load for 20 and 30 V supply voltages are almost open or become capacitive which will reduce the efficiency performance (for class-J operation, when

the fundamental load is inductive, the second harmonic should be capacitive and vice versa. If both of them are inductive or capacitive, the efficiency will reduce). The parasitic conductance at 10 V supply voltage is relatively large. So, the second harmonic load has less negative influence on the efficiency when it becomes capacitive. For other angle values, the second harmonic is almost shorted and has no influence on the performance. All of the following discussions on the influence of second harmonic are similar to this discussion. We don't repeat them.

Another thing should be notice is that we use 24 dBm input power (1 dB compression point for 30 V supply voltage) to do load-pull simulation and second harmonic load angle sweep. All the results we get at lower supply voltage are with over-drive condition. Although the optimum load conditions with or without over-drive are the same, whether we can get an efficiency improvement without overdrive are still need to be investigated.

Optimum load condition: The optimum load conditions are like follows (Figure 3.26):

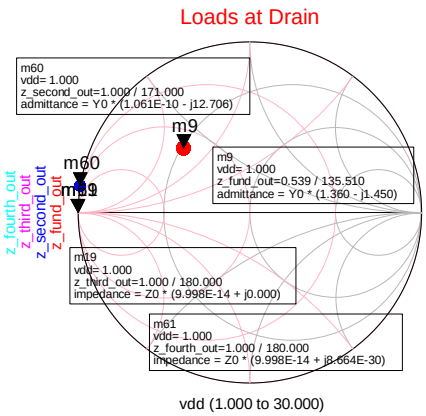


Figure 3.26 (a) Optimum loads for hybrid class power amplifier seen from external drain (including package parasitics and excluding device parasitics. Red and blue represent fundamental and second harmonic load respectively. The Smith chart is normalized to 30 Ohms.)

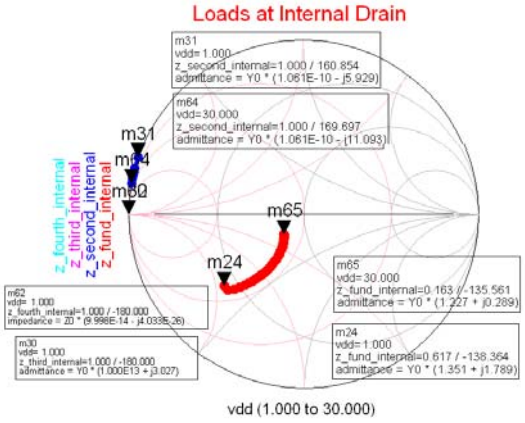


Figure 3.26 (b) Optimum loads for hybrid class power amplifier seen from internal drain (including both package and device parasitics. Red and blue represent fundamental and second harmonic load respectively. The loads are shift with supply voltage from 1 to 30 V. The Smith chart is normalized to 30 Ohms.)

The figure 3.26(b) shows how the loads shift with supply voltage. The parasitic capacitor of the device is strong function of supply voltage. So, the loads seen from internal drain are also a strong function of supply voltage. And these loads are reasonable according to the solution of class-J we discussed previously.

The process of choose second harmonic load for fundamental load in figure 3.24 (a) is similar (figure 3.27). We don't repeat the process here.

Conclusion of optimum load condition:

1. Load condition optimized for 30 V supply voltage without 2nd harmonic tune (figure 3.24 (a)). 2. Load condition optimized for efficiency at power back-off without 2nd harmonic tune (figure 3.24 (b)). 3. Load condition optimized for 30 V supply voltage with 2nd harmonic tune (figure 3.27). 4. Load condition optimized for efficiency at power back-off with2nd harmonic tune (figure 3.26 (a))

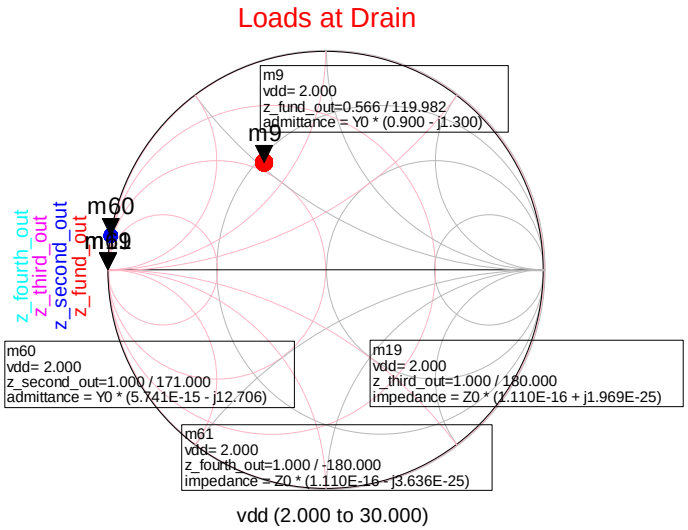
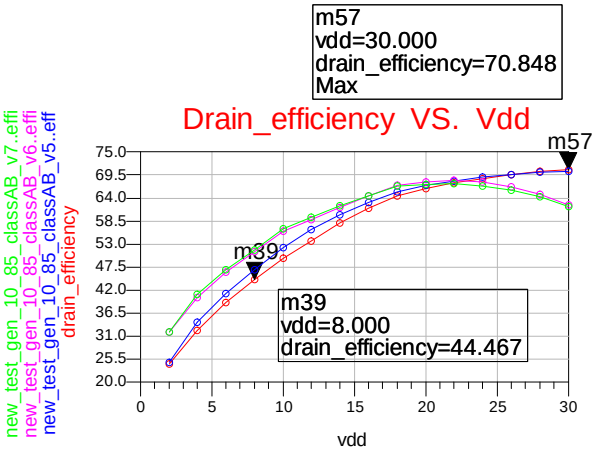
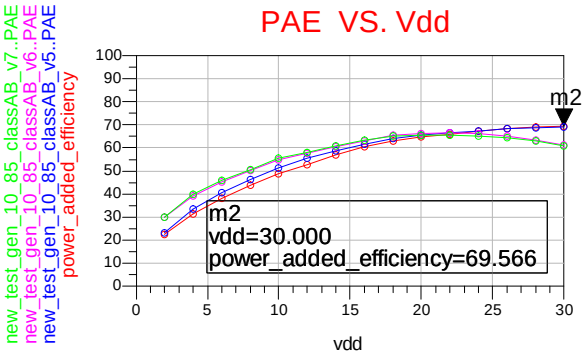
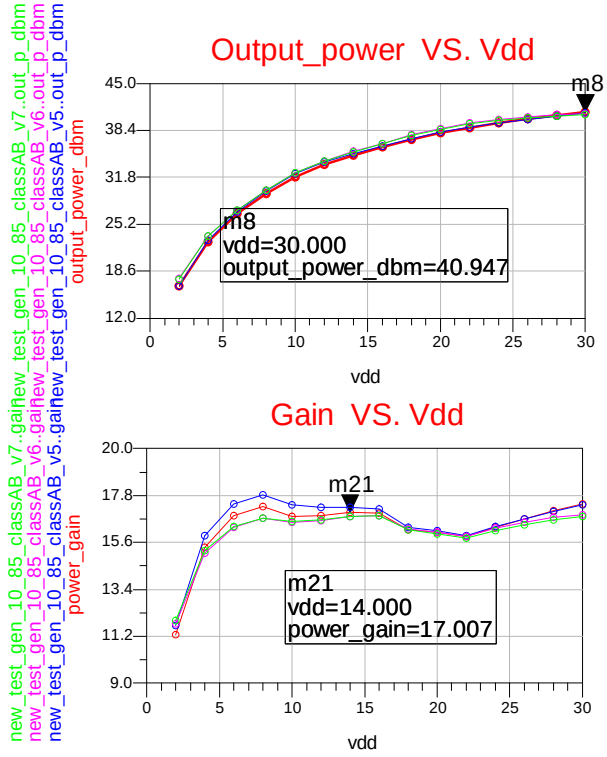


Figure 3.27 The optimum fundamental load (red)for efficiency at 30 V supply voltage with 2nd harmonic (blue) tuned (the Smith chart is normalized to 30 Ohms)

Performance: Now, we can compare the performance of class-AB/B and hybrid-class operation. The results are as follows


m57
vdd=30.000
drain_efficiency=70.848
Max
Drain_efficiency VS. Vdd
new_test_gen_10_85_classAB_v7..effi
new_test_gen_10_85_classAB_v6..effi
new_test_gen_10_85_classAB_v5..eff
drain_efficiency
m57
m39
m39
vdd=8.000
drain_efficiency=44.467
vdd


PAE VS. Vdd
new_test_gen_10_85_classAB_v7..PAE
new_test_gen_10_85_classAB_v6..PAE
new_test_gen_10_85_classAB_v5..PAE
power_added_efficiency
m2
m2
vdd=30.000
power_added_efficiency=69.566
vdd


Output_power VS. Vdd
new_test_gen_10_85_classAB_v7..out_p_dbm
new_test_gen_10_85_classAB_v6..out_p_dbm
new_test_gen_10_85_classAB_v5..out_p_dbm
output_power_dbm
m8
m8
vdd=30.000
output_power_dbm=40.947
vdd
Gain VS. Vdd
new_test_gen_10_85_classAB_v7..gain
new_test_gen_10_85_classAB_v6..gain
new_test_gen_10_85_classAB_v5..gain
power_gain
m21
m21
vdd=14.000
power_gain=17.007
vdd

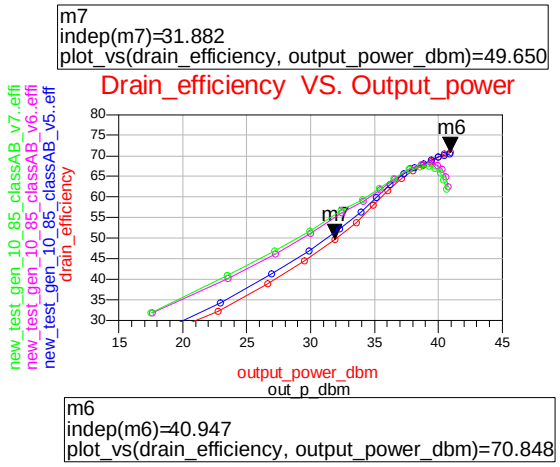


Figure 3.28 (c) Comparison of simulation results of class-AB/B and hybrid-class operations. Red and blue represent the fundamental load is optimized for efficiency at 30 V supply voltage. Red, without 2nd harmonic tune. Blue, with 2nd harmonic tune. Pink and green represent the fundamental load is optimized for average efficiency. Pink, without 2nd harmonic tune. Green, with 2nd harmonic tune.

From figure 3.28, when the fundamental load is optimized for the efficiency at power back off, the performances of class-AB/B (pink) and hybrid-class operations (green) have very little difference. If the fundamental load is optimized for the efficiency at power back-off (pink and green), the efficiency will be higher at power back-off compared with the load which is optimized for 30 V supply voltage (red and blue). But, the efficiency is lower at higher supply voltages.

We can also check the drain voltage waveform and spectrum of loads optimized for efficiency at power back-off with 2nd harmonic tune (figure 3.29).

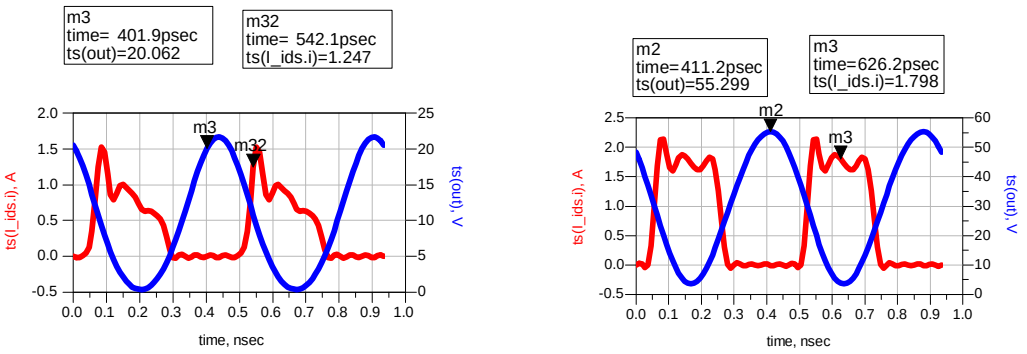


Figure 3.29 (a) Drain voltage waveform of hybrid class (Left one is 10 V supply voltage and right one is 30 V)

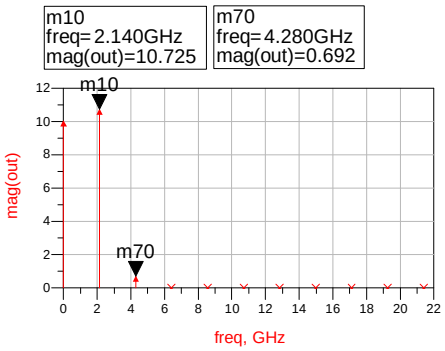
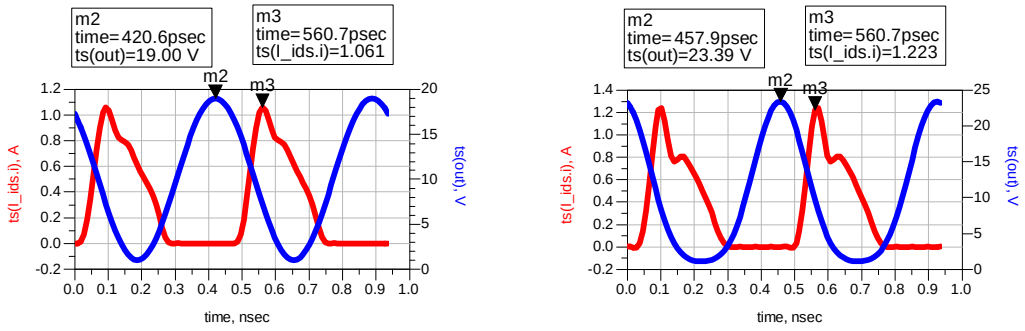


Figure 3.29 (b) The drain voltage waveform at 10 V supply voltage

We can see the amplitude of second harmonic voltage is only 0.69 V, which is less than 1/10 of that of fundamental harmonic voltage (10.7 V). This shows the second harmonic load is almost short. If you still remember the amplitude problem we have discussed in chapter 2, the answer for why the second harmonic load has very little influence on the drain voltage is obvious (see figure and table 2.12 in chapter 2). These optimum loads are found out by load-pull simulation and second harmonic load angle sweep. They show that the power amplifier can provide better performance when operate close to class-AB rather than class-J.

Power dissipation at parasitics:

In section 2, we have found that the performance of this device in class-J is better than that of class-AB operation at 30 V supply voltage and 2.14 GHz. However, class-AB operation can provide us better results at 10 V supply voltage and 2.14 GHz (figure 3.30).



drain_efficiency	output_power	dc_supply_power
57.032	1.823	3.196

drain_efficiency	output_power	dc_supply_power
48.859	1.656	3.389

Figure 3.30 (a) Simulation results of class-AB (left) and class-J (right) at 10 V, 2.14 GHz

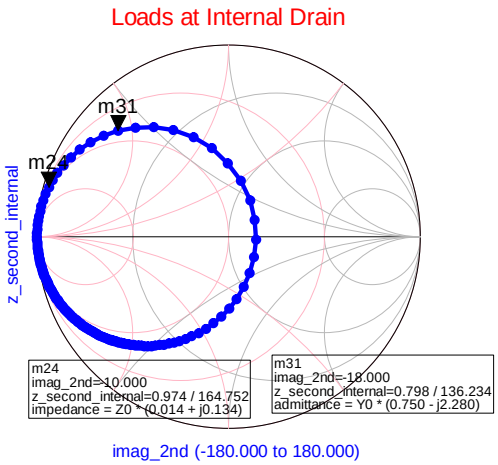


Figure 3.30 (b) Sweep the second harmonic load angle (in polar format, the Smith chart is normalized to 30 Ohm)

We transform the second harmonic load to polar format: (admittance, angle). If admittance isn't 1, it represent the second harmonic load is not a pure reactance and will cause loss at second harmonic. Angle represents the angle of second harmonic load. Previously, when we consider the load condition seen from internal drain, we ignore the parasitic conductance of the device. However, at 10 V supply voltage and 2.14 GHz, the parasitic conductance will reduce our performance a lot. So, we should take it into account. In figure 3.30 (b), we estimate the total parasitic conductance is 0.025 S. Figure 3.30 (b) shows us the sweeping of the second harmonic load angle (from -180 degrees to 180 degrees). Mark "m31" represents the angle we use in figure 3.30 (a) (the waveforms are shown in figure 3.30 (a) class-J operation). From figure 3.30 (a), we can see the DC power dissipation of class-J operation is higher than that of class-AB at 2.14 GHz. In contrast, the output power of class-J operation at fundamental frequency is smaller than that of class-AB operation at 2.14 GHz. This proves that the power loss at second harmonic (due to parasitics) becomes significant at 2.14 GHz for this 12 W LDMOS. So, when we do load-pull simulation and 2^{nd} harmonic load sweep, the results show the efficiency will be higher when we almost short the second harmonic (the region near mark 24 in figure 3.30 (b)).
Since the problem is caused by parasitics, we should be able to get a better performance with 2^{nd} harmonic tune at lower fundamental frequency or with small parasitic device. In order to verify this, we can check the performance of hybrid class and class-AB/B operation at 1.5 GHz. The performances with smaller parasitic device are shown in appendix 4.

Performances at 1.5 GHz:
Load conditions are as follows:

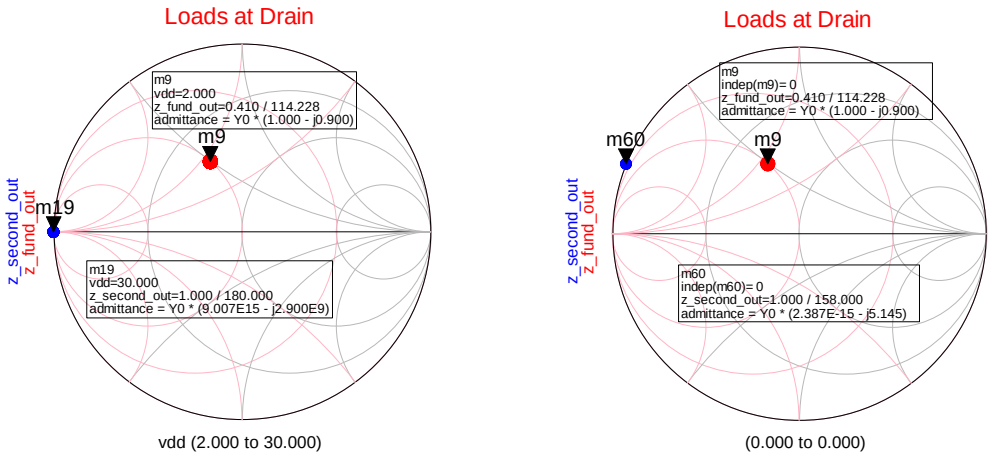


Figure 3.31 (a) Fundamental load is optimized for efficiency at 30 V supply voltage (left, without 2nd harmonic tuned, right, with 2nd harmonic tune , red, fundamental frequency load, blue, second harmonic load. The Smith chart is normalized to 30 Ohms)

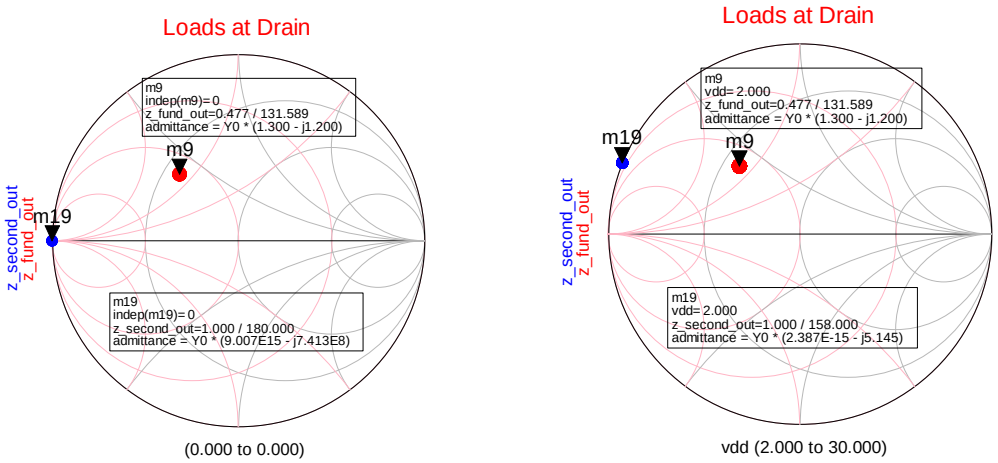
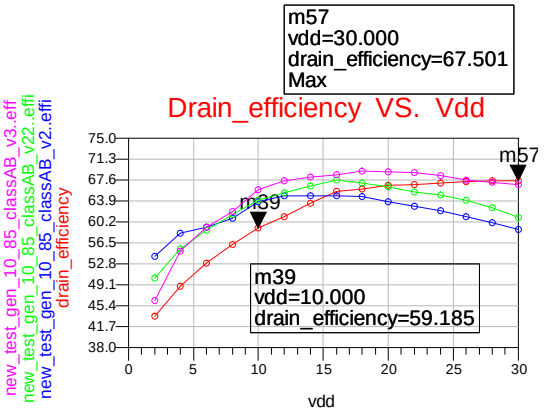


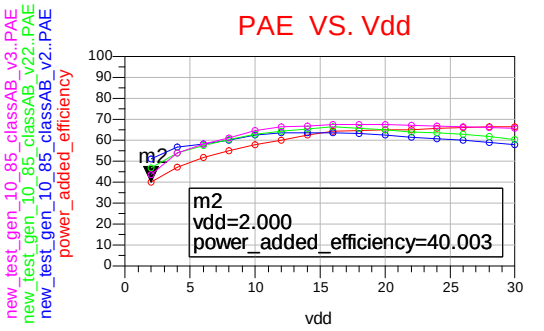
Figure 3.31 (b) Fundamental load is optimized for efficiency at power back-off (left, without 2nd harmonic tuned, right, with 2nd harmonic tune , red, fundamental frequency load, blue, second harmonic load. The Smith chart is normalized to 30 Ohms)

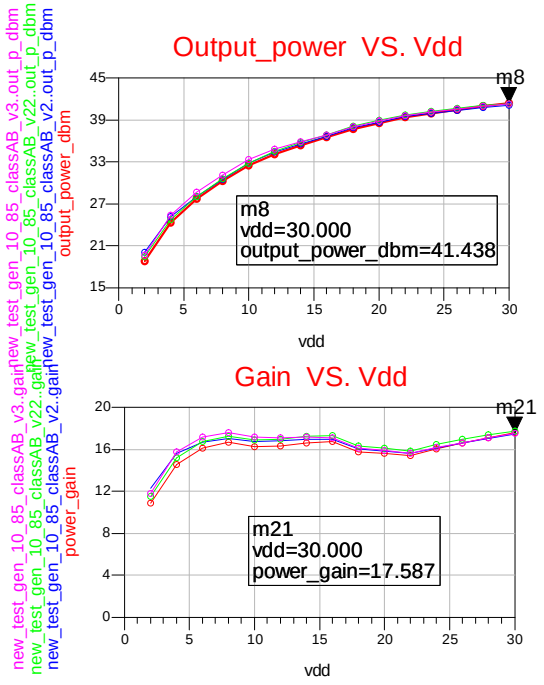
The simulation parameters are:

1. Gate bias voltage: 2.25 V
2. Frequency: 1.5 GHz
3. Drain voltage: 1V to 30V
4. Input power: the input powers are chosen at the 1 dB compression point for each supply voltage
5. Input of the transistor is conjugate matched

The results are as follows (figure 3.32):


m57
vdd=30.000
drain_efficiency=67.501
Max
Drain_efficiency VS. Vdd
new_test_gen_10_85_classAB_v3..eff
new_test_gen_10_85_classAB_v22..effi
new_test_gen_10_85_classAB_v2..effi
drain_efficiency
m57
m39
m39
vdd=10.000
drain_efficiency=59.185
vdd


PAE VS. Vdd
new_test_gen_10_85_classAB_v3..PAE
new_test_gen_10_85_classAB_v22..PAE
new_test_gen_10_85_classAB_v2..PAE
power_added_efficiency
m2
m2
vdd=2.000
power_added_efficiency=40.003
vdd


Output_power VS. Vdd
new_test_gen_10_85_classAB_v3..out_p_dbm
new_test_gen_10_85_classAB_v22..out_p_dbm
new_test_gen_10_85_classAB_v2..out_p_dbm
output_power_dbm
m8
m8
vdd=30.000
output_power_dbm=41.438
vdd
Gain VS. Vdd
new_test_gen_10_85_classAB_v3..gain
new_test_gen_10_85_classAB_v22..gain
new_test_gen_10_85_classAB_v2..gain
power_gain
m21
m21
vdd=30.000
power_gain=17.587
vdd

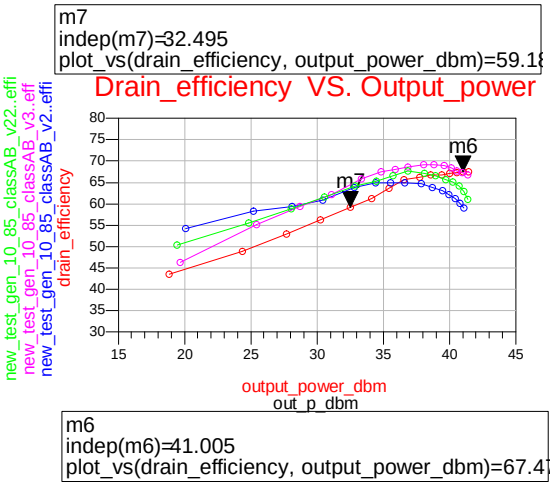


Figure 3.32 Comparison of simulation results of class AB and hybrid class operations at 1.5 GHz. Red and pink represent the fundamental load is optimized for efficiency at 30 V supply voltage. Red, without 2nd harmonic tune. Pink, with 2nd harmonic tune. Blue and green represent the fundamental load is optimized for efficiency at power back-off. Green, without 2nd harmonic tune. Blue, with 2nd harmonic tune

From the results in figure 3.32, we can see that when both the fundamental load and 2nd harmonic load are optimized for efficiency at power back-off, the slope of curve (efficiency vs. output power in dBm, figure 3.32) is the lowest. But, the efficiency at higher supply voltages is sacrificed. When the fundamental load is optimized for 30 V supply voltage and the 2nd harmonic load is used to improve the efficiency at power back (pink), the efficiency at higher supply voltages can be maintained. But, the slope is larger. Obviously, the second harmonic has more positive and obvious influence on the performance at 1.5 GHz comparing with that at 2.14 GHz.

We check the drain voltage spectrum of load in figure 3.31 (b) (figure 3.33):

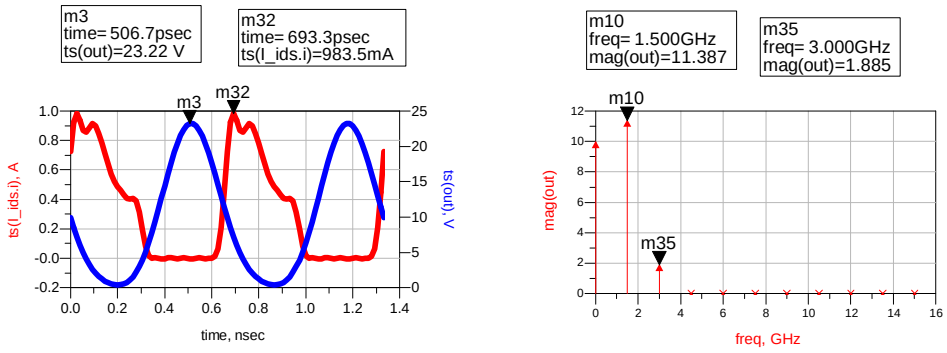


Figure 3.33 (a) The drain voltage and spectrum at 10 V supply voltage

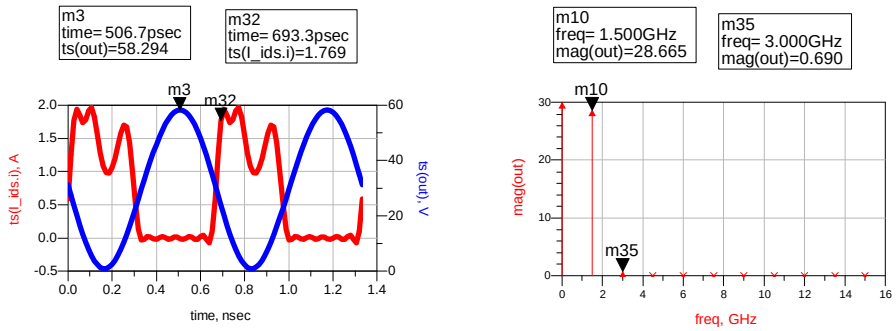


Figure 3.33 (b) The drain voltage and spectrum at 30 V supply voltage

In figure 3.33, the second harmonic voltage is 1/5.5 of the fundamental harmonic voltage at 10 V supply voltage and 1/41.5 at 30 V supply voltage. So, the power amplifier operates at class-J at 10 V and at almost class-AB/B at 30 V. The peak drain voltage is around 58 V, which is below the breakdown voltage (65 V): this is the main reason why we make hybrid class power amplifier.

Best operation class for our LDMOS: The performances at 1.5 GHz verify that the parasitic capacitances have less influence on the power amplifier. We can check other frequencies. The results show that: below 2.0 GHz, hybrid class has better performance than class-AB/B operation. But, when the frequency rises to 2.0 GHz, the performances for both operations are almost the same.

This conclusion gives us two hints. One is when we choose device before we start to design, we should choose the device whose parasitic capacitances are small. The other one is when we want to design a wideband hybrid class PA, we should focus on and optimize the second harmonic load at lower operation frequency. I will analyze this problem more when we design a wideband hybrid class PA.

Since we have found the optimum load conditions, the nest step is to realize it with lump elements or transmission line. But, before doing that, we should first check the stability issue.

Section 4. The stability issue:

The stability issue is very important for power amplifier design. If it's possible, we should make the power amplifier unconditional stable. But, the reality is we will lose a lot of gain if we make it unconditional stable. So, our strategy is to make the source and load stability circles outside the main area of the Smith chart and match the input and output outside the stability circles.

Stability circles: First, we draw the source and load stability circles on the Smith chart (Figure 3.34, from 1 Hz to 10 GHz, supply voltage we choose 3 points, 10 V, 20V, 30V)

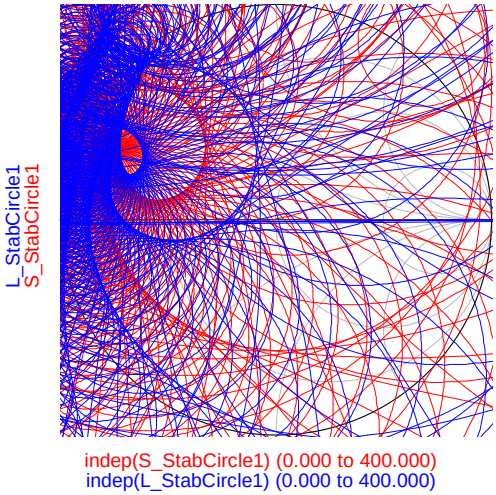


Figure 3.34 (a) Red, source stability circles. Blue, load stability circles. (From 1 Hz to 10 GHz, vdd, from 1 to 30 V, step 10 V)

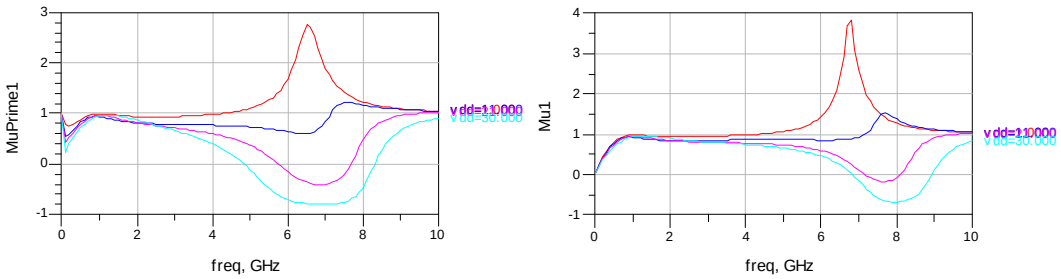


Figure 3.34 (b) Left, source mu factor, right, load mu factor (different colors represent different supply voltages, 1V to 30 V, step, 10 V)

We can see from Figure 3.34 that the source mu factor is below 0 between 5 and 8 GHz. And the load mu is also below 0 between 7 and 8 GHz. I tried every method to stabilize it. But, none of them can make it unconditional stable. (I contact the model group of NXP, their opinion is this model can't be used at very high frequency. So, we only check the stability from 1 Hz to 4 GHz in our later design)

The network used to stabilize the power amplifier: (see the red region in figure 3.35)

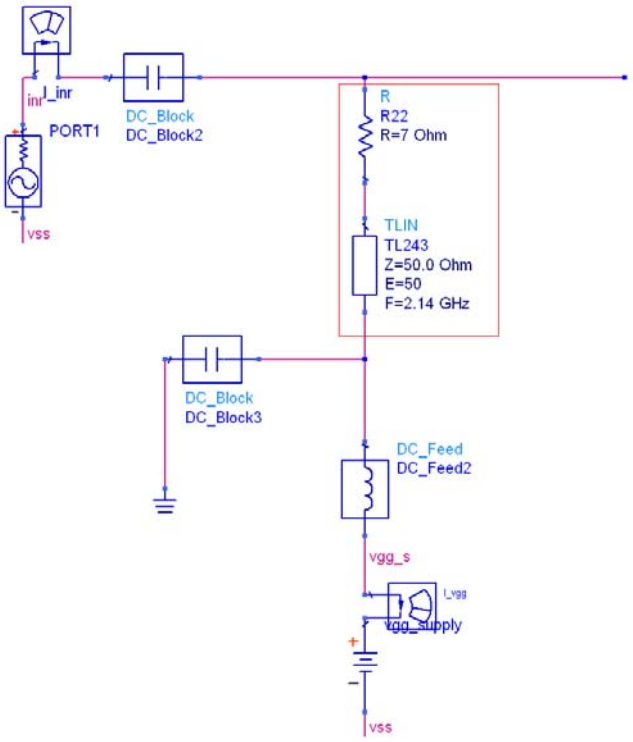


Figure 3.35 (a) Proposed network to stabilize the power amplifier

The transmission line here is a non-ideal RF choke. We use a resistor to stabilize the power amplifier.

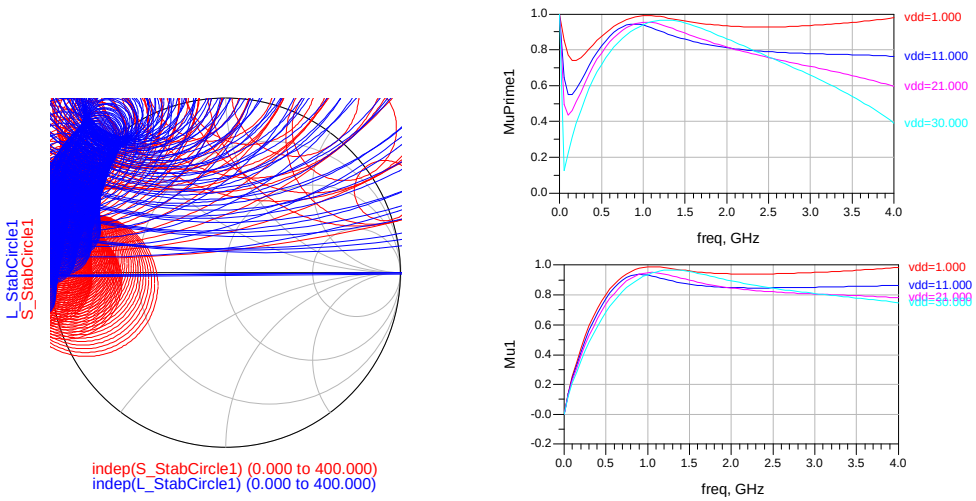


Figure 3.35 (b) Before stabilization. Left, stability circles (red, source stability circles, blue, load stability circles). Right, mu factor of source and load (Muprime1, source mu factor, mu, load mu factor)

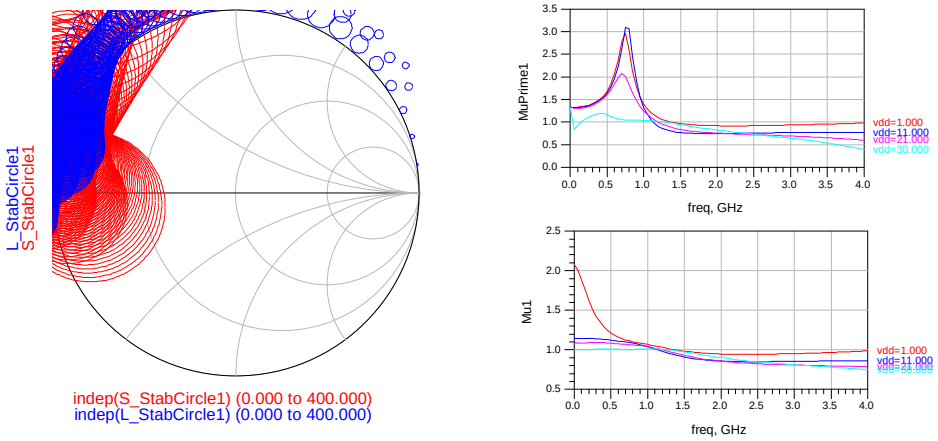


Figure 3.35 (c) After stabilization. Left, stability circles (red, source stability circles, blue, load stability circles). Right, mu factor of source and load (Muprime1, source mu factor, mu, load mu factor)

We compare figure 3.36 (b) and (c). These graphs show the proposed network can stabilize the power amplifier.

Input matching in stable region: I have tried if we want to make the power amplifier unconditional stable between 1 Hz to 4GHz, we will lose a lot of gain. The gain will decrease to 10 dB. A power amplifier which is stable but has no gain is also meaningless for us. So, our strategy is to design the input and output matching outside the stability circles, instead of making it unconditional stable.

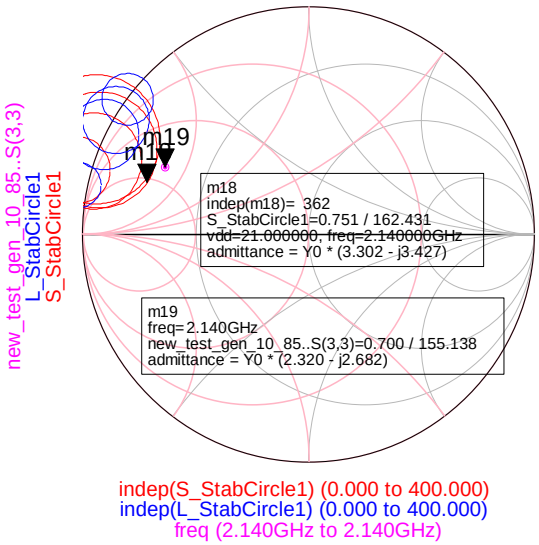


Figure 3.36 Stability circles and input matching at 2,14 GHz. Red, source stability circles. Blue, load stability circles. Pink, input matching (the reference and direction to see the load is plane A shown in figure 3.9)

Unfortunately, the conjugate match for the input at 2.14 GHz is in the unstable region. So, we choose a position near the conjugate match position but outside the stability circles (pink dot in figure 3.36)

Section 5. Realization:

Here, we choose the realization of hybrid power amplifier at 2.14 GHz (load condition in figure 3.26 (a)) as an example. For other load conditions, we can use the same topology and tune the values of components to match to their optimum loads.

First we need to choose the matching topology. The steps to choose it are as follows:

1. Because we want to realize a hybrid class power amplifier, we should choose a topology which allows easy tuning of the second harmonic load. Normally, the output of the power amplifier is connected to a 50 Ohms load and the optimum load for second harmonic load purely inductive. So, we can use a inductive component and second harmonic short part to realize the second harmonic load:

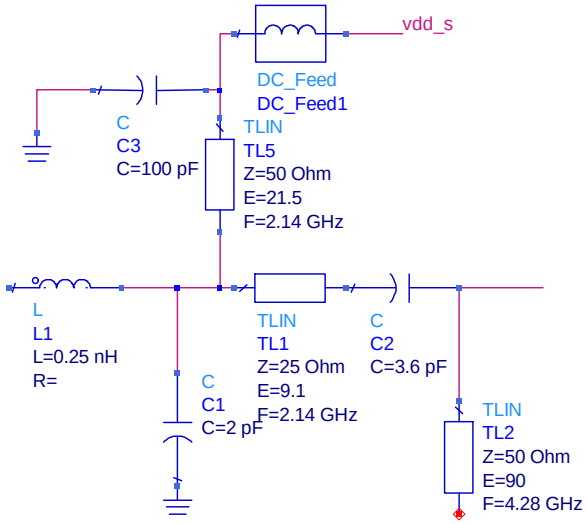


Figure 3.37 The second harmonic load part

In figure 3.37, L1 and C1 are the parasitical components of package. The left node of L1 in the graph connects to the drain of transistor. TL2 is the second harmonic short part. It's a quarter-wave transmission line at 4.28 GHz. The input impedance of this transmission line is:

$$Z_{input} = \frac{Z_0^2}{Z_L} \tag{14}$$

Z0 is the characteristic impedance of transmission line and ZL is the load at the end of the transmission line. It's an open stub. So, ZL is infinite and the input impedance of transmission line is 0. That means other components behind this transmission will not affect the second harmonic load. So, if we only use reactive components before this transmission line, we can get a pure reactive load for second harmonic load.

For the fundamental frequency (2.14 GHz), TL2 is like a capacitor:

$$Z_{input} = Z_0 \times \frac{1}{j \times \tan \beta l} = -jZ_0 \frac{1}{\tan \beta l} = -jZ_0 \frac{1}{\tan 45^\circ} = -jZ_0 \quad (15)$$

So, we can use the characteristic impedance of TL2 to tune the fundamental load and don't affect the second harmonic load simultaneous.

In figure 3.37, we use transmission line L1 and capacitor C2 to tune the value of the reactive load for second harmonic load.

And, we should notice that the ideal RF choke is not a practical thing. We can use an inductor which has finite value and finite Q factor as a RF choke. Here we use a transmission line to realize a finite Q RF choke (TL5 in Figure 3.37). The input impedance of this transmission line is:

$$Z_{input} = Z_0 \times \frac{Z_L + j \times Z_0 \times \tan \beta l}{Z_0 + j \times Z_L \times \tan \beta l} \quad (16)$$

C3 is used to short the RF signal at bias path. So, it's a very large value. For impedance, it's a very small value. So, for TL5, the load of TL5 is 0. The input impedance is:

$$Z_{input} = j \times Z_0 \times \tan \beta l \quad (17)$$

When $0 + 2n\pi < \beta l < \frac{\pi}{2} + 2n\pi$ and $\pi + 2n\pi < \beta l < \frac{3\pi}{2} + 2n\pi$, $n \in N$,

$\tan \beta l$ is positive and the transmission line is inductive.

When $\frac{\pi}{2} + 2n\pi < \beta l < \pi + 2n\pi$ and $\frac{3\pi}{2} + 2n\pi < \beta l < 2\pi + 2n\pi$, $n \in N$,

$\tan \beta l$ is negative and the transmission line is capacitive.

Here, we need this transmission line to replace an inductor. So, we make this transmission line inductive.
We should notice that the transmission line is like a finite value inductor. So, we should take it into account when we tune the loads.

1.TL 2 blocks the influence of other components behind TL2 for second harmonic load. We need other components to match the fundamental harmonic load. Normally, the output load of power amplifier is 50 Ohms and the load we need is smaller than 50 Ohms. So, we can use a low pass matching network to transform the 50 Ohms load to the load we need (Figure 3.38):

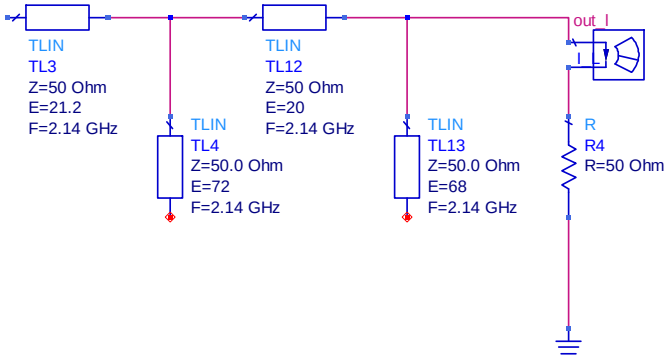


Figure 3.38 Low pass matching network used to transform the 50 Ohms load

Notice that, the second harmonic tuning also affects the fundamental load. So, our strategy is we first tune the second harmonic load to the value we want and tune the low-pass network to match the fundamental harmonic load. If we can't tune low-pass matching network to match the fundamental harmonic load, we can re-tune the second harmonic load part (achieve the second harmonic load but have different components values). And try to tune the low pass network again.

2. In our previous design (using equation components of ADS), we have shorted all the higher order harmonics and only worked with the fundamental and second harmonic. But, this is not very practical when we realize it. We can use many branches to short the higher order harmonics. However, due to the existence of series parasitical components of the package, even this complicated topology can't give us the perfect short for higher order harmonics short.

So, our strategy is we only consider how to tune the second harmonic load and fundamental harmonic load. The higher order harmonics can be suppressed by the low pass matching network.

But, if we have higher order harmonics, is this power amplifier still operating at class-J? Actually, the difference between sub-optimum class-J and sub-optimum class E is not very obvious. When we design sub-optimum class E power amplifier we pay more attention to the load of higher order harmonics. But, for sub-class-J power amplifier, we only consider the second harmonic load. However, if you like, you can also call it sub-optimum class-E power amplifier.

All the descriptions above are the design ideals to choose the matching topology. So, now, we realize it and check the simulation results.

The overall circuit (Figure 3.39):

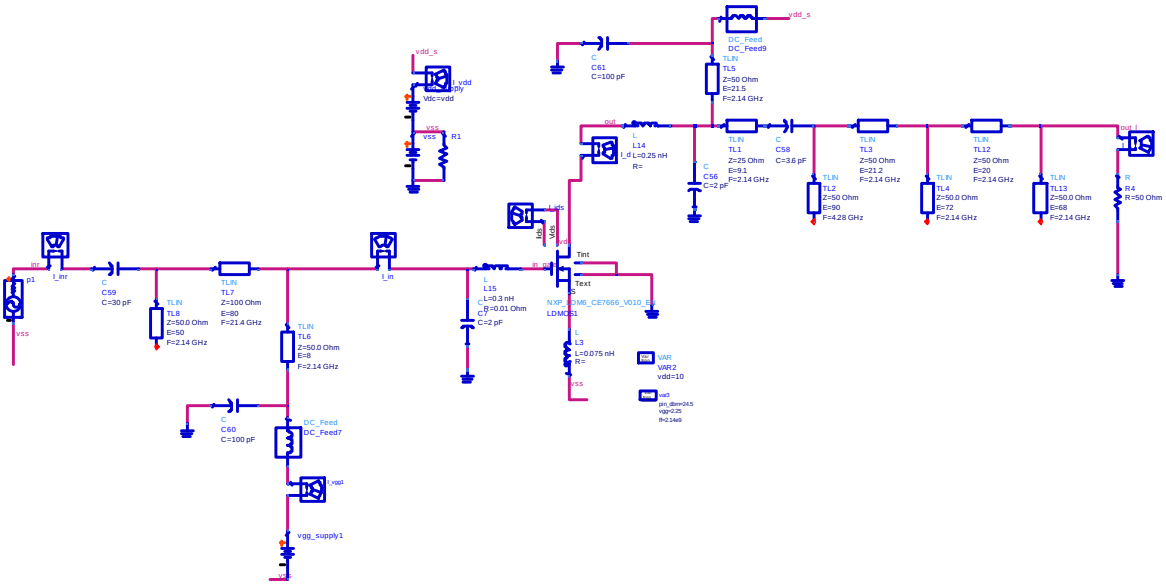


Figure 3.39 The overall matching network

The middle part is the transistor with package. Left part is the input matching network, right part is the output matching network.
We summarize the functions of the components of the matching network:
Input matching:

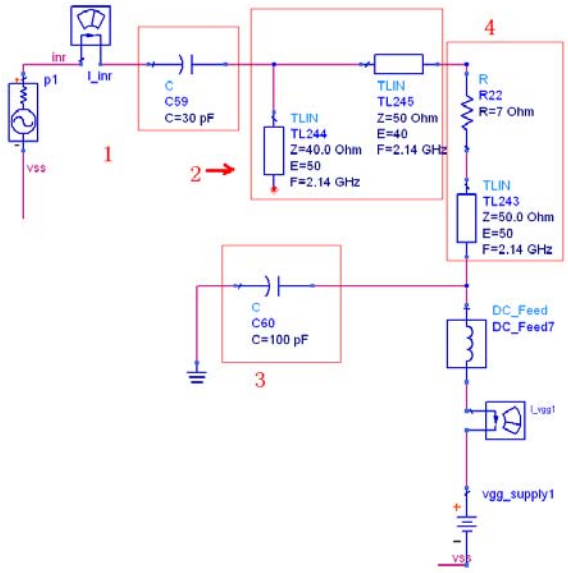


Figure 3.40 Input matching network

The components function in figure 3.40:

1. Dc block
2. Transform the 50 Ohms source impedance to match the input of the transistor
3. AC short for the gate bias path.
4. Non-ideal RF choke and stabilization part. These components are absorbed in the input matching design.

Output matching:

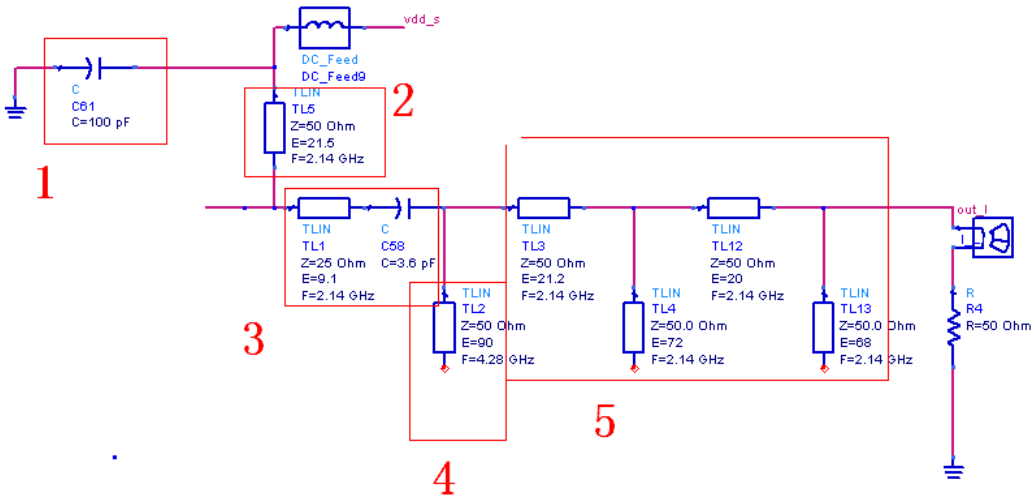


Figure 3.41 Output matching network

The components function in figure 3.41:

1. AC short for the bias path.
2. Non-ideal RF choke, this component is absorbed in the loading design
3. The component 4 shorts the second harmonic. We can use components 3 to tune the reactance of second harmonic load.
4. Short the second harmonic. If we short the second harmonic here, the component 5 will not affect the second harmonic load. We can tune the second harmonic load using components 3 easily. At the same time, it's a capacitor for fundamental frequency. We can tune the characteristic resistance to tune the fundamental load.
5. Providing a matching to transform 50 Ohms load to match the output of the transistor.

Simulation results:

The simulation parameters are:

1. Gate voltage: 2.25 V
2. Drain supply voltage: 1-30 V
3. Input power: the input powers are chosen at or below the 1 dB compression point for supply voltages.
4. Frequency: 2.14 GHz.

The performances are as follows:

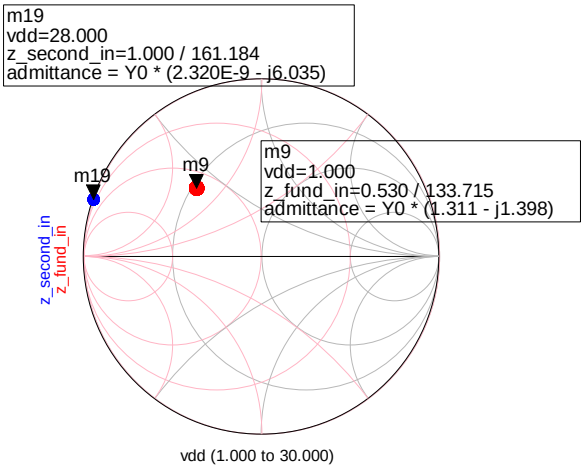
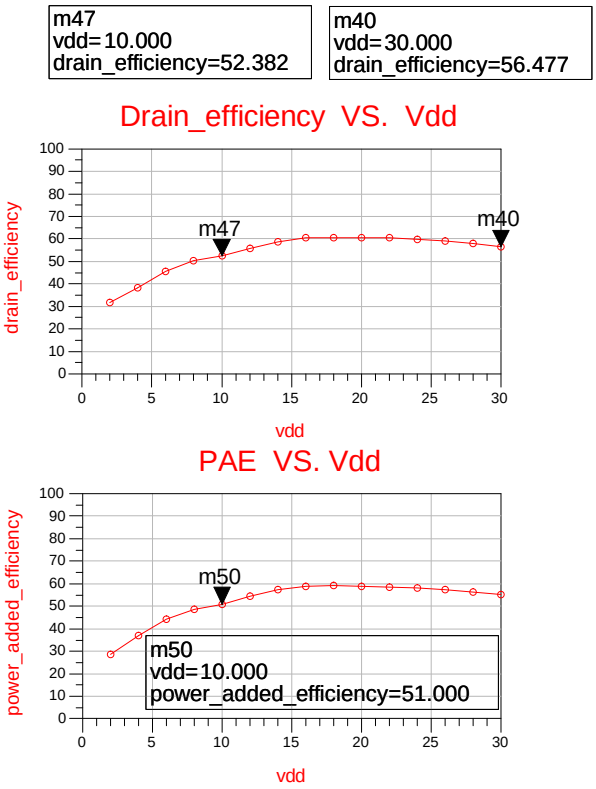


Figure 3.42 Output load condition for the realized hybrid class PA (normalized to 30 Ohms, red, fundamental frequency load, blue, second harmonic load)



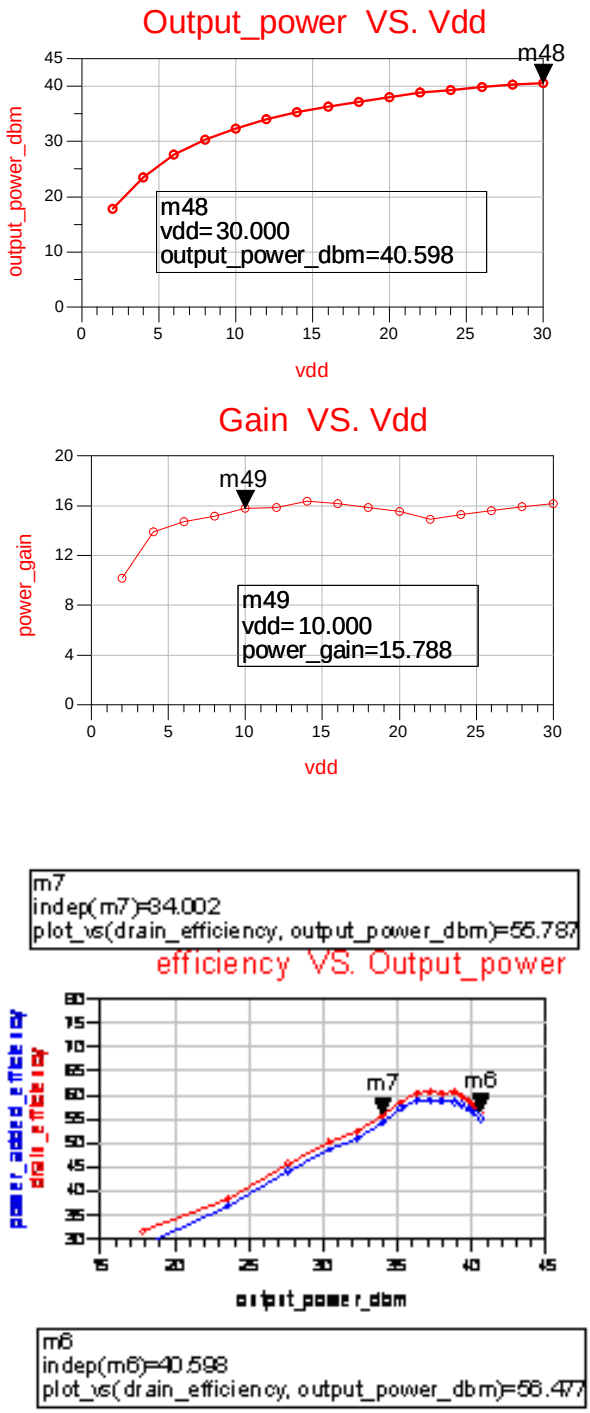


Figure 3.43 Simulation results after redesign the input matching

Here, the efficiency performance is worse than the one realized with ideal components. At high supply voltage, the efficiency drops to 55%. At 6 dB power back off point, the efficient drops below 55%.

The waveforms of the drain voltage and current (see figure 3.44):

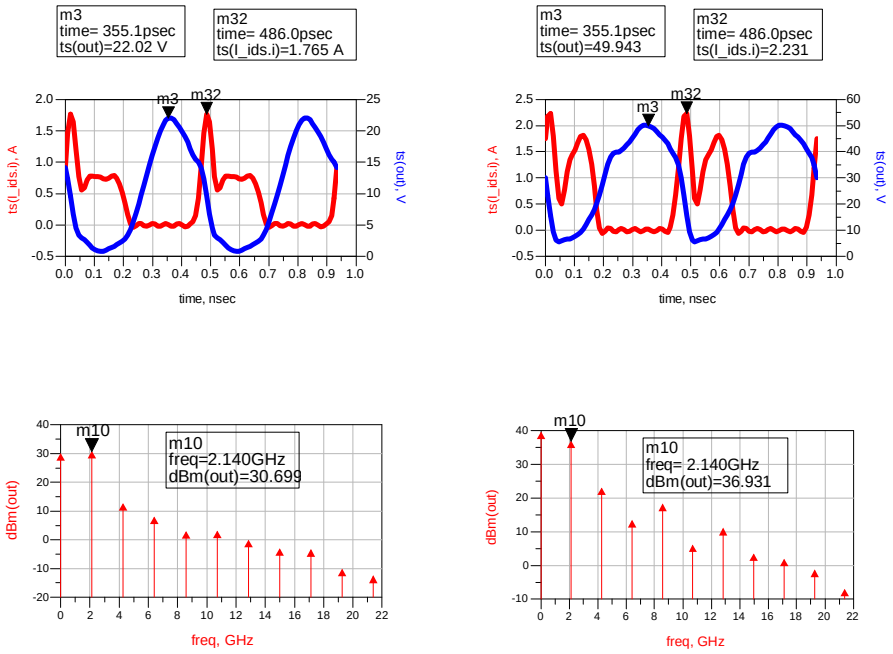


Figure 3.44 The drain current, voltage waveform and frequency spectrum at 10 V and 30 V (left one, 10 V. Right one, 30 V. Red, drain current, blue, drain voltage)

The waveforms are different form those realized with ideal components. The reason is there are some higher order harmonics (see figure 3.44).

Section 6: Conclusion

This NXP LDMOS is suitable for hybrid class operation at lower frequency (lower than 2.0 GHz). For higher frequency, there is seems to be almost no big different for this packaged device between class-AB/B and hybrid class operations.

After realizing the hybrid power amplifier at 2.14 GHz, we can achieve 15-16 dB gain, higher than 55% drain efficiency and PAE at around 6 dB power back-off point as well as reach 40.7 dBm peak output power.

Chapter 4 Wideband Hybrid-Class Power Amplifier for EER and ET Systems

In this chapter, we design a wideband power amplifier. For a wideband power amplifier, the performance at a single frequency point may be not as good as in a narrowband power amplifier design. But, it can keep its efficiency and output power performance over a wideband. Let's describe the method how to design a wideband hybrid-class amplifier step by step.

In section 1, we discuss the performances differences between narrowband and wideband power amplifiers, as well as, the reasons causing these differences. This section will provide us the ideas how to design a wideband power amplifier.

In section 2, the design steps for a wideband power amplifier will be introduced.

In section 3, some practical issues will be discussed. For example, what are the functions of components in our matching network? How change these components with frequency and how effect they the performance of the wideband power amplifier.

In the following sections, a 1GHz bandwidth hybrid-class power amplifier optimized for supply voltage modulation will be introduced

Section 1. Wideband power amplifier design

We have discussed in chapter 3 how to design a narrowband hybrid power amplifier for EER or ET system. So, as first step we can check the wideband performance of this amplifier design and find the reasons why the narrowband power amplifier can't keep the performance over a wide frequency region.

Parameters for simulation:

(1) Gate voltage: 2.25 V

(2) Frequency region: 1.7 to 2.4 GHz

(3) Drain supply voltage: 10 to 30 V, step is 10 V

(4) Input power: The input powers are chosen at 1dB compression point for each supply voltage.

The performances of narrowband power amplifier are as follows:

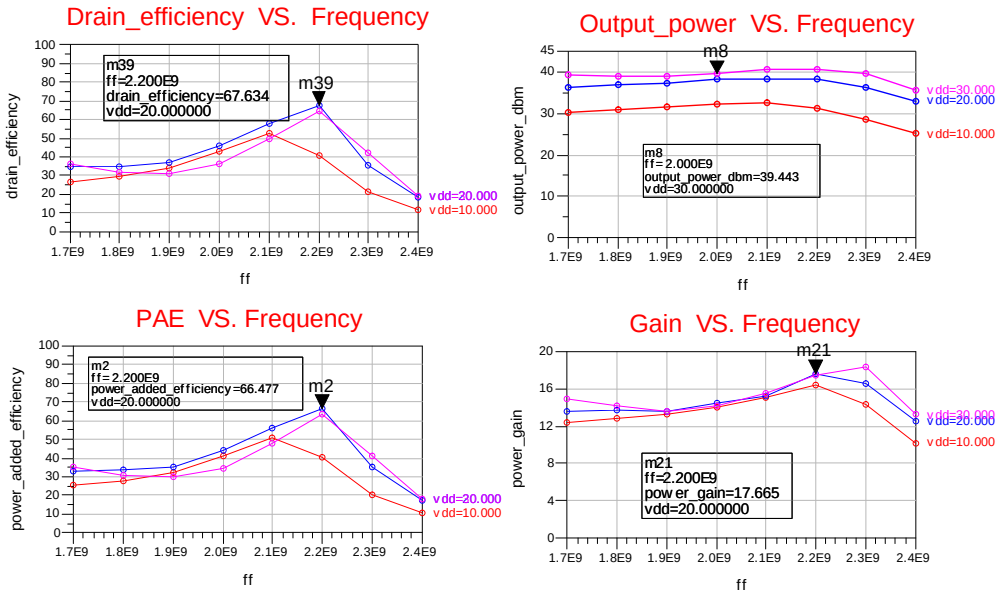


Figure 4.1 Performance vs. frequency of the narrowband (2.14GHz) optimized power amplifier. The different colors represent the various supply voltages, red, 10V, blue, 20 V, pink, 30 V)

We can see that: the drain efficiency, PAE, output power and power gain drop quickly when the frequency deviates from the central frequency (2.14 GHz). The reason is: the previous design is just optimized for a single frequency (2.14 GHz). So, the loads will quickly deviate on the Smith chart vs. frequency (figure 4.2). The reference plane and direction to see the load is shown in figure 3.9 in chapter 3. All the input and output load discussed in the following sections are the same.

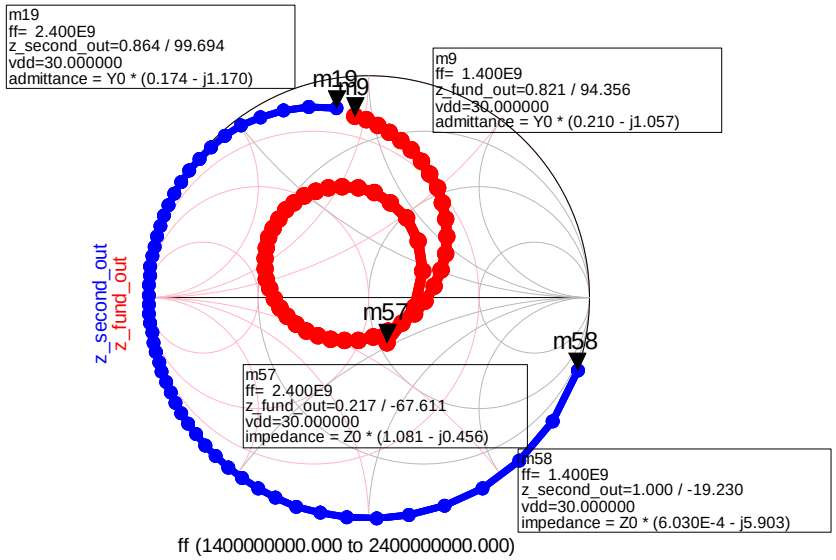


Figure 4.2 Reflection coefficients offered by the output matching networks of the "narrowband" 2.14 GHz power amplifier vs. frequency (1.4 GHz to 2.4 GHz). Red: fundamental load. Blue: second harmonic load. The Smith chart is normalized to 30 Ohms.

Analyzing the reasons for these simulation results would help us to design a wideband power amplifier. We have mentioned in chapter 3 that the optimal loads have been determined by the supply voltage and the output power.

$$\text{For class-AB/B:}\quad Z_{opt} = \frac{Vdd^2}{2 \times P_{out}} \tag{1}$$

$$\text{For class-J:}\quad Z_{fund} = \frac{V_{DD}{}^2}{\sqrt{2} \times P_{peak}} \angle \pm \frac{\pi}{4},\quad Z\,\text{sec}\,ond = \frac{3\pi \times V_{DD}{}^2}{16 P_{peak}} \angle \mp \frac{\pi}{2} \tag{2}$$

So, if the supply voltage and output power remain unchanged, the optimal loads should stay constant in value for an ideal device (no parasitics). But in practice there are always some parasitical components in the device. The most important one is the output capacitance. For example, if we want to design a class-AB power amplifier, according to the optimal load equation, the load should be a pure resistive load. However, due to the presence of output capacitance, we need an inductive load to compensate for this. We can review a graph of chapter 3 (figure 4.3):

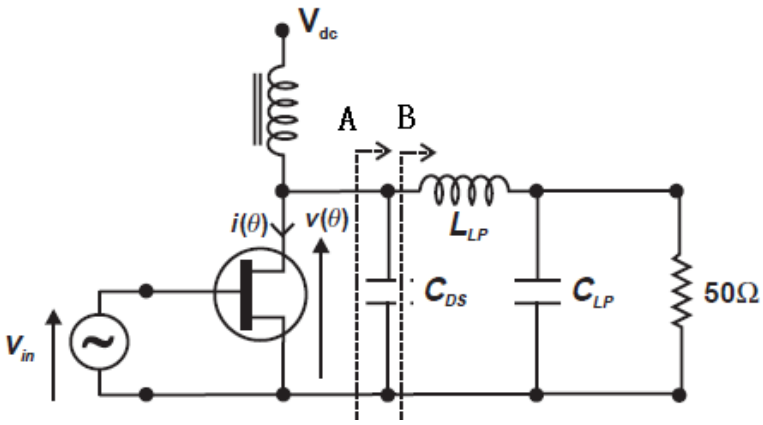


Figure 4.3 (a) Reference plane A and B of the output matching network (Cds is the output capacitance of device)

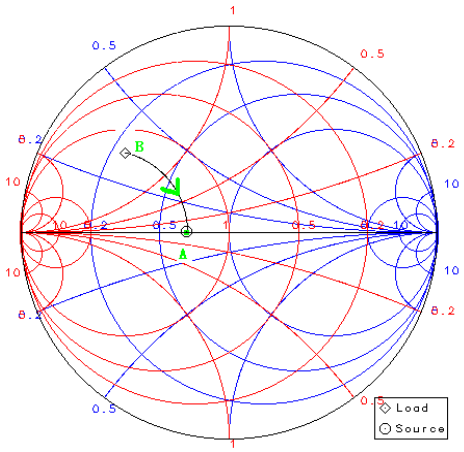


Figure 4.3 (b) Load seen from plane A and B

For a wideband design, this compensation becomes more difficult. Normally, the susceptance of the output parasitical capacitor ($j\omega C_{parasitcial}$) will increase with the frequency increases. But, the compensating suceptance of the load $\frac{1}{j\omega L_{load}}$ will decrease with frequency. So, when we want to use a fixed value component, the compensation versus frequency proves to be very difficult.

For EER or ET applications, the compensation will be even more difficult, because the parasitic output capacitance will also vary with supply voltage. So, our strategy is that we don't match the load to its optimum value, but match it to a value which is close to the optimum one.

We can also notice that the optimum load for different frequency is confined to a limited area in the Smith Chart (only the reactive parts of the loads are different). So, we need to find a loading network that does not vary too much with frequency.

We summarize the requirements for wideband power amplifier loads as follows:

(1) Due to the output capacitance of device, the optimum loads for power amplifier will shift with frequency. Perfectly compensating for output capacitance over a wideband frequency region is not practical. So, we match the loads to the values which are close to optimal values.

(2) Although the optimum loads will vary with frequency due to the output capacitance of the device. The optimum loads for different frequency are still very close to each other (in a certain small region). So, it's necessary for us to choose a matching network which can make the loads values vary only little with the frequency (low Q matching).

(3) Since matching the optimum loads for each frequency is not a practical thing, we should focus on the performance of the whole band, not a single frequency.

Section 2. Optimum load conditions for wideband power amplifier:

We have found the requirements for wideband power amplifier design in section 1. In this section we will discuss the design strategies to meet these requirements and summarize the design steps at the end of this section.

In chapter 3, we have discussed the fundamental load can optimized for the efficiency at 30 V supply voltage or for efficiency at power back-off. The later one will sacrifice the efficiency at higher supply voltage, but, have better efficiency at power back-of. At the same time, we can tune the 2^{nd} harmonic load to improve the efficiency at power back-off. For wideband design, it's not easy to tune the 2^{nd} harmonic load over a wideband region. So, we choose to optimize the fundamental load for efficiency at power back-off and sacrifice some efficiency at higher supply voltage. In this way, we can maintain the efficiency at power back-off even if the second harmonic load can't improve it.

Optimum load conditions: So, now we find optimal loads for wideband power amplifier. We can redo the design process as we did in chapter 3 for the central frequency (2.14 GHz) now also for the other frequencies. The process is similar. So, we don't repeat the process here. The optimal loads for wideband power amplifier are as follows (figure 4.4):

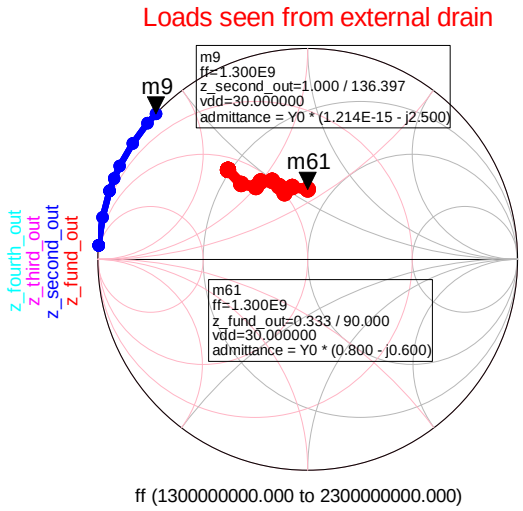


Figure 4.4 (a) Optimum load trajectory for the wideband power amplifier seen form external drain (including package parasitics and excluding device parasitics) from 1.3 to 2.3 GHz. Red :fundamental load. Blue: second harmonic load. (The Smith chart is normalized to 30 Ohms)

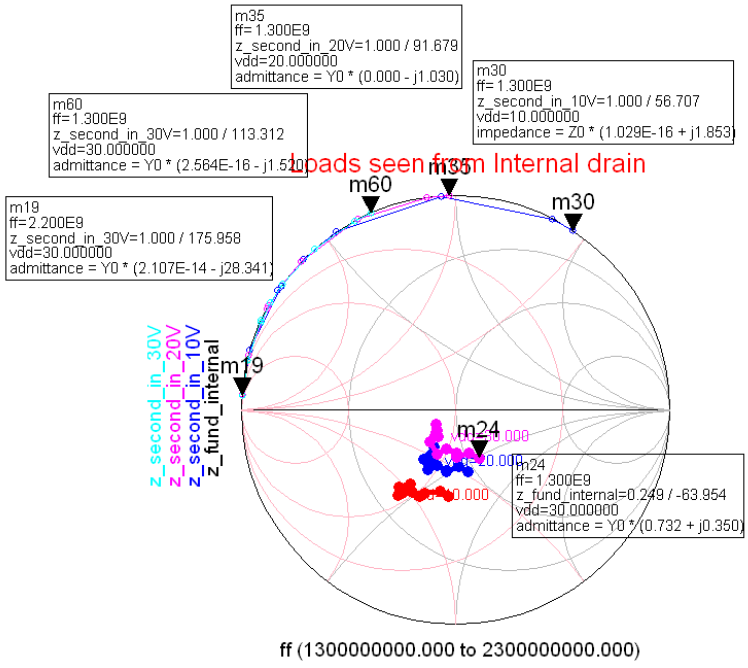


Figure 4.4 (a) Optimum load trajectory for the wideband power amplifier seen form internal drain (including both package and device parasitics) from 1.3 to 2.3 GHz. Red :fundamental load. Blue: second harmonic load. (The Smith chart is normalized to 30 Ohms)

The fundamental loads chosen are optimized for the efficiency at power back-off (see theory is in chapter 3). The second harmonic loads are also optimized to improve for the average efficiency. It proves that the optimum fundamental and 2nd harmonic loads are close to that of the second solution found for class-J operation

We can see from figure 4.4, the optimal loads for second harmonic should rotate along the impedance chart anti-clockwise. But, if we have an inductive component for tuning the second harmonic load, it will rotate along the impedance chart clockwise. So, these optimal loads for second harmonic are not very practical. But, as we said previously, we can match the loads as close as possible. The narrower the bandwidth is, the easier the match is.

It worth to check how is the performance if we short the second and higher-order harmonics and only match the fundamental load to the optimal values. The wideband power amplifier operates at class-AB/B operation (Figure 4.5).

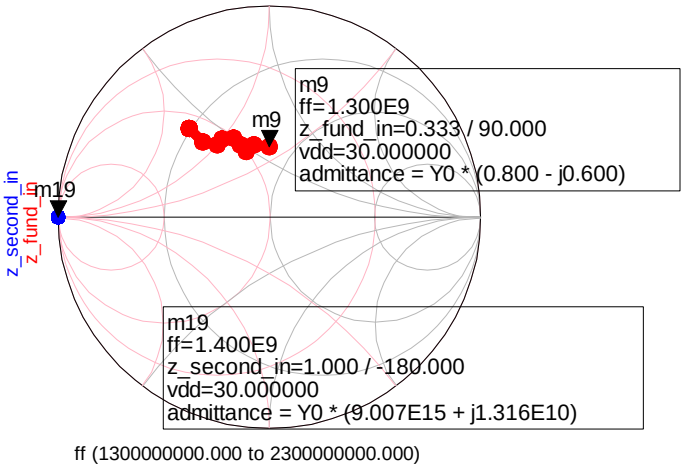


Figure 4.5 (a) Matching of the fundamental to the optimum load vs. frequency, while short circuiting the second and higher order harmonics (The Smith chart normalized to 30 Ohms)

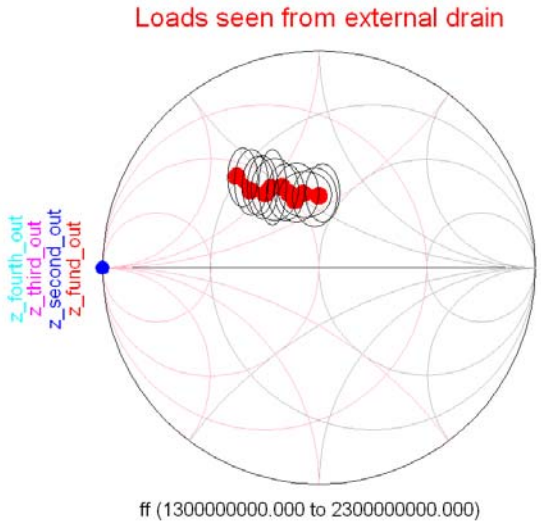


Figure 4.5 (b) The common high efficiency region (drain efficiency is around 60%) for different supply voltage values versus frequency. The black circles represent the high efficiency regions found by load-pull simulations (The Smith chart is normalized to 30 Ohms)

Performance with optimum load conditions: We use the ideal equation components of ADS to test the performance of the optimum loads we found (figure 4.5):

The simulation parameters:

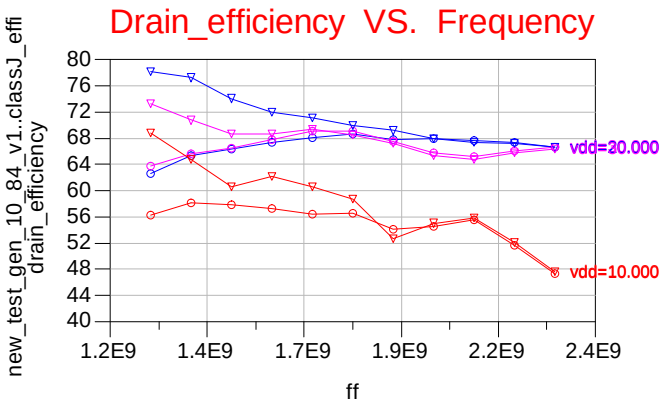
(1) Gate voltage: 2.25 V

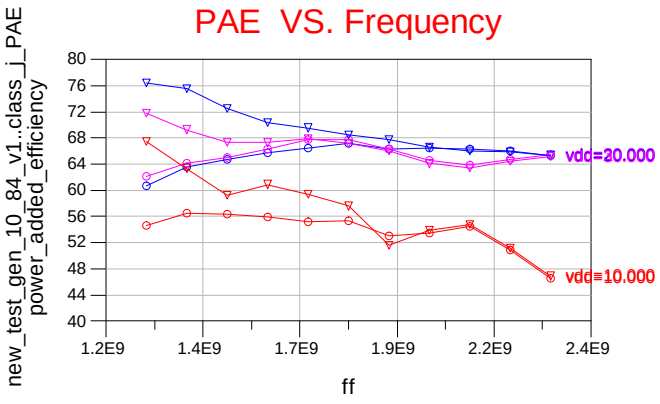
(2) Drain voltage: 10 to 30 V, step is 10 V

(3) Frequency: 1.3 to 2.3 GHz

(4) Input power: the input powers are chosen at 1 dB compression point for each supply voltage.

(5) The input is conjugate match





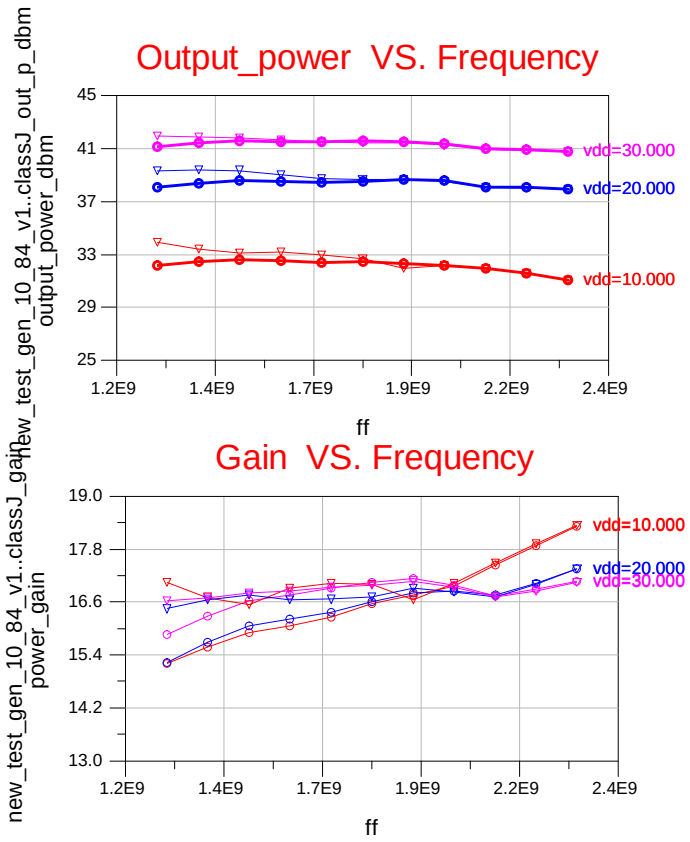


Figure 4.6 The performance of optimum loads found for the wideband power amplifier (Triangles represents: using 2nd harmonic tune. Circles represents: don't use 2nd harmonic tune. The different colors represent the supply voltage. Red, 10 V. Blue, 20V. Pink, 30V)

The drain efficiency proves to be higher than 50% for all supply voltage over 1 GHz of bandwidth. The power gain for the 30 V supply voltage is around 15-18 dB over this 1 GHz bandwidth. The efficiency performance is significantly better within the bandwidth from 1.3 to 1.9 GHz. But, there is no big performance difference when the frequency is higher than 2.0 GHz. The reason for this has been already discussed in chapter 3. We repeat it here briefly: the influence of device parasitics become significantly when the frequency is very high (higher than 2.0 GHz). The power amplifier almost the same performance when operates at class-AB/B and hybrid class. So, we should pay our attention to the tuning of the second harmonic between 1.3 to 1.9 GHz. Another conclusion is even without 2nd harmonic tune, we can get acceptable results. So, the fundamental loads are the most important.

So, we summarize the matching strategies:

1. First, we find the optimal loads for all frequency within the band we want to design.

2. We perform a load-pull simulation to define the high efficiency regions for all frequencies.
3. We choose a matching topology that provides low load variation with frequency changes and matches the optimum values as close as possible, followed by a 2nd harmonic optimization.

Section 3. Matching network for realization

In section 1 and 2, we have discussed the design strategies for a wideband power amplifier. In this section, we consider the problem how to realize it.

we need to choose a matching network which can make the loads vary little with the frequency. The matching network we use for narrowband power amplifier is a good candidate. Because we can tune the second harmonic easily and the matching network for fundamental harmonic load is a low Q matching.

However, the functions of some components have changed. First, we have a look at the overall circuit of output matching network:

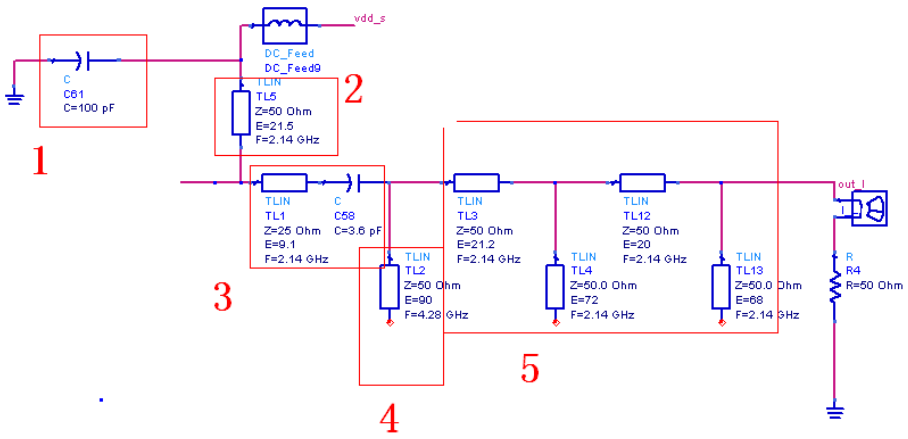


Figure 4.7 Output matching network for narrowband power amplifier

1. Component 1 is the AC short for bias path. For wideband version, its function is the same.
2. Component 2 is like an inductor for narrowband power amplifier. The electric length is chosen for 2.14 GHz. When we decrease the design frequency, the wavelength of the signal will become longer and for the same physical dimensions of component 2, the electric length of this component will become less. This means the inductive reactance of this component will become less. And vice versa, when the frequency increases, the inductive reactance will become larger. We should notice that the electric length should be less than 90 degrees. If it's higher than 90 degrees, the component will be capacitive. So, for wideband design, the inductive reactance of component 2 will affect the load vs. frequency.
3. Component 3 provides the reactance for second harmonic loads, as well as, fundamental harmonic loads. It rotates the loads around the centre of the smith

chart.

4. Component 4 is the second harmonic short for the narrowband power amplifier. But, for wideband design, it can't be a perfect short for every frequency, because it just has a fixed electric length for one frequency. Let's exam how the value of the component vary with frequency:

$$Z_{input} = \frac{Z_0}{\tan \beta l} \tag{3}$$

If the electric length is less than 90 degrees, the input impedance of this component will be capacitive. Normally, we choose the electric length according to the second harmonic of design frequency. So, component 4 should be a capacitor at fundamental frequency. But, for second harmonic, it could be a capacitor or inductor according to their frequency.

5. Part 5 is the low Q matching network for fundamental harmonic load. This is the key part which can make the loads shift little with frequency. However, the loads can also shift significantly even with this low Q matching network. The reason is the components values of the low Q matching network are also important. We can see two matching cases:

Case 1 High Q matching with low Q matching network (figure 4.8):

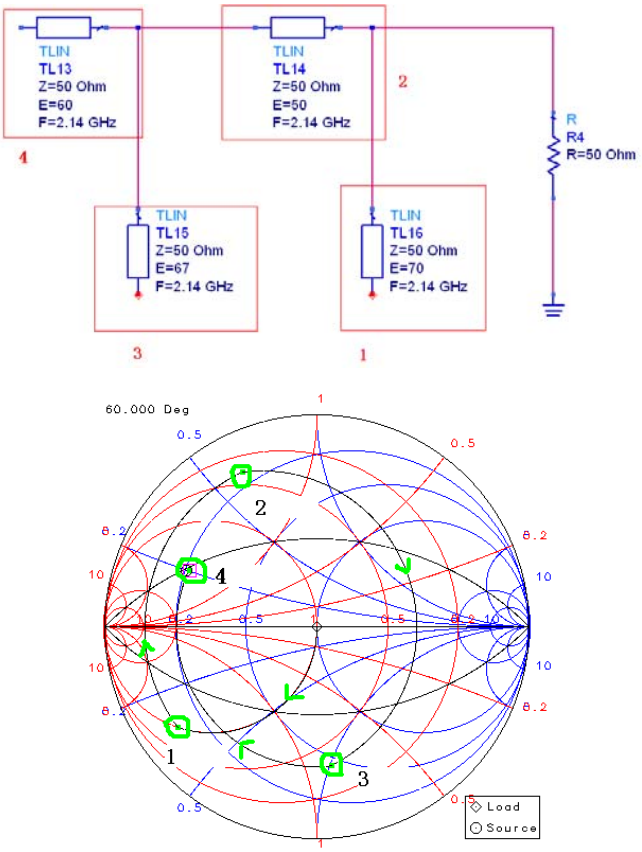


Figure 4.8 Matching of case 1. (The upper graph shows the component values of this matching. The numbers in the lower graph represent the matching path corresponding to number of components in the upper graph)

Case 2 Low Q matching with low Q matching network (figure 4.9):

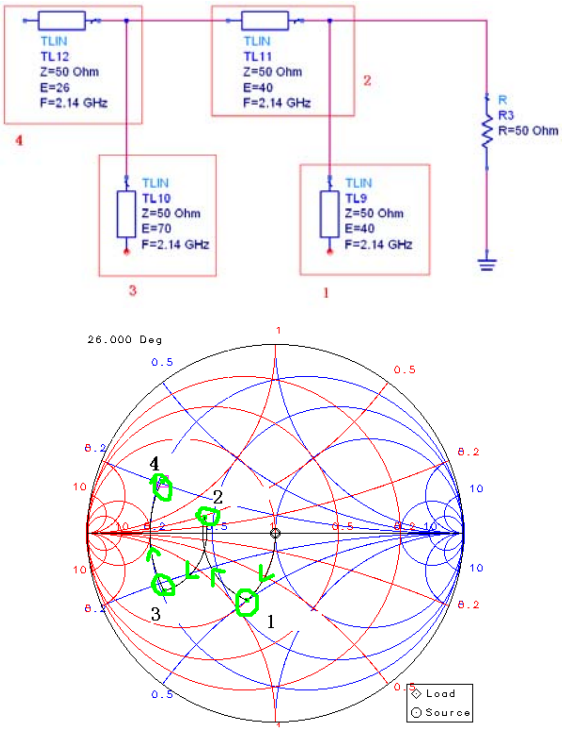


Figure 4.9 Low Q matching. (The upper graph shows the component values of this matching. The numbers in the lower graph represent the matching path corresponding to number of components in the upper graph)

We can check how this impedance varies with frequency (figure 4.10):

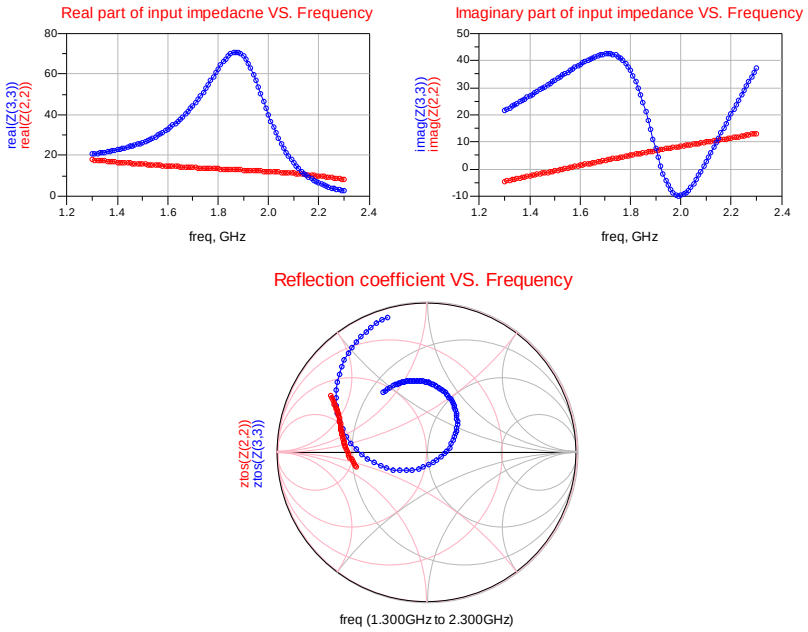


Figure 4.10 Real and imaginary part of the input impedance of network in figure 4.8 and 4.9.

Reflection coefficient vs. Frequency in the Smith chart (Blue, case 1 matching network in figure 4.8. Red, case 2 matching network in figure 4.9. The Smith chart is normalized to 50 Ohms)

The input impedance of matching network of case 2 varies much less than that of case 1 with the same matching topology. This gives us an important hint: the components values should be tuned carefully even we use a low Q matching network (compare the components values in figure 4.8 and 4.9). The matching path should be chosen along the low Q path in the Smith chart (like figure 4.9).

Section 4. Design bandwidth for wideband power amplifier

We have discussed the components characters for wideband power amplifier design in last section. Now, we need to choose the design bandwidth. There are two considerations for our choice: operation class of wideband PA and device characters.

Operation class:

Here, in this project, we want to design a wideband class-J power amplifier. For class-J operation, we need to tune the second harmonic load. This fact will restrict the upper bandwidth which we can achieve. For example, the second harmonic of 1.3 GHz is 2.6 GHz, which should be terminated purely reactive. Therefore simultaneous fundamental matching (which requires an ohmic part) at a frequency of 2.6 GHz is not possible. So, there will be a practical bandwidth limitation for our design. Normally, for class-J operation, the relative bandwidth for central frequency is 50% (e.g. 1 GHz for 2.0 GHz).

Device characteristics:

Based on the optimum loads and load-pull simulation results we found in section 2, we know that the device is not suitable for class-J operation at high frequency (higher than 2.0 GHz). Moreover, the higher the frequency is, the larger influence the parasitics of the device have. We can’t even get a good performance with class-AB/B operation at a frequency which is higher than 2.6 GHz (due to the parasitics of device, the power amplifier actually doesn't operate at class-AB/B seen from internal drain). In addition, the central frequency for WCDMA application is 2.14 GHz.

So, we choose 1.3 to 2.3 as our design bandwidth (50% relative bandwidth for central frequency)

Section 5. Device class of operation for the wideband power amplifier

Before we start our design, we should discuss something about what class the wideband power amplifier operates at.

Wideband class-AB/B power amplifier: If we want to design a wideband class-AB/B power amplifier, the harmonics except the fundamental should be shorted. But, perfect wideband short is not a very practical thing, especially when the

bandwidth is very wide.

Wideband class-J power amplifier:
For ideal class-J operation, we control the second harmonic to tune the drain voltage.

In chapter 3, we discussed the solutions of ideal class-J. There are 2 solutions for ideal class-J: 1.Inductive load for fundamental harmonic and pure capacitive load for second harmonic. 2. Capacitive load for fundamental harmonic and pure inductive load for second harmonic.

But, also here in practical design, the output parasitic capacitor will vary a lot with supply voltage. The reactance of the output parasitical capacitor also varies a lot with frequency. So, it's difficult to make all the fundamental and second harmonic loads meet these two solutions.

Wideband class-E power amplifier:
With the experience of designing a narrowband power amplifier, we often have some third or even higher order harmonics. So, the operation class is more like sub class-E operation with solution 1 of class-J operation. For class-E operation, we should have an inductive fundamental load (R+j*x). The loads for second and higher order harmonics should be pure capacitive (-j*x).

However, the same as class-J operation, the output loading due to the reactance of output parasitical capacitor changes a lot with frequency and supply voltage. It's very difficult to meet the class-E operation requirement for all frequencies, especially when the bandwidth is very wide.

From the above, we can conclude that a single-ended wideband power amplifier will be not a pure class-AB/B, J or E PA in practical design. It may change the operation classes when the frequency changes even if our initial intention is to design a wideband class-J power amplifier. For this reason, we will call it a wideband hybrid class PA (different definition for hybrid-class from narrow band PA)

We give the design of 3 wideband power amplifiers:
1. The first one is a wideband power amplifier (1.5 – 2.25 GHz) without optimization for supply voltage modulation. In this version, the power amplifier should have a peak efficiency more 65% over a wide bandwidth at 30 V supply voltage.
2. The second one is a 600 MHz bandwidth power amplifier with optimization for supply voltage modulation. In this version, because of the supply voltage modulation requirement, the tune of the load becomes more difficult than version 1.
3. In version 3, we design a 1 GHz bandwidth hybrid power amplifier optimized for supply voltage modulation. This version is a big challenge for us.

Form version 1 to version 3, the difficulty increases step by step. The 1 GHz

bandwidth version will be shown in next section. Version 1 and 2 are shown in appendix.

Section 6 A 1 GHz bandwidth hybrid power amplifier optimized for supply voltage modulation

Input matching network: In chapter 4, we have found that the conjugate input matching can be unstable at 2.14 GHz. So, for this wideband version, we also check the stability. The topology of the input matching network is as follows (figure 4.11):

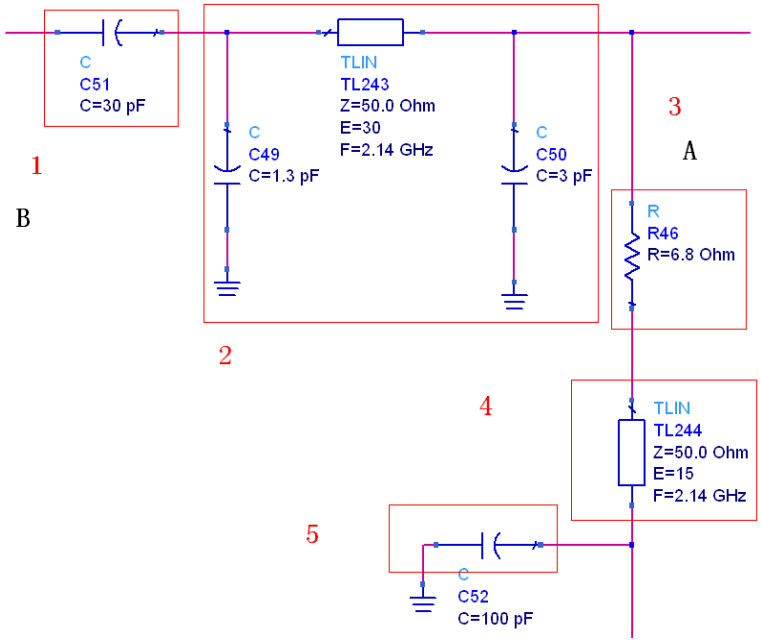


Figure 4.11 Input matching network for 1 GHz bandwidth hybrid class power amplifier

The functions of the components in figure 4.11:

1. DC block.
2. Match the 50 ohms source load to the input of the transistor.
3. A resistor used to stabilize the device.
4. Non-ideal RF choke realized by a piece of transmission line.
5. RF short.

We have discussed the stability issue already in chapter 4. The results are as follows:

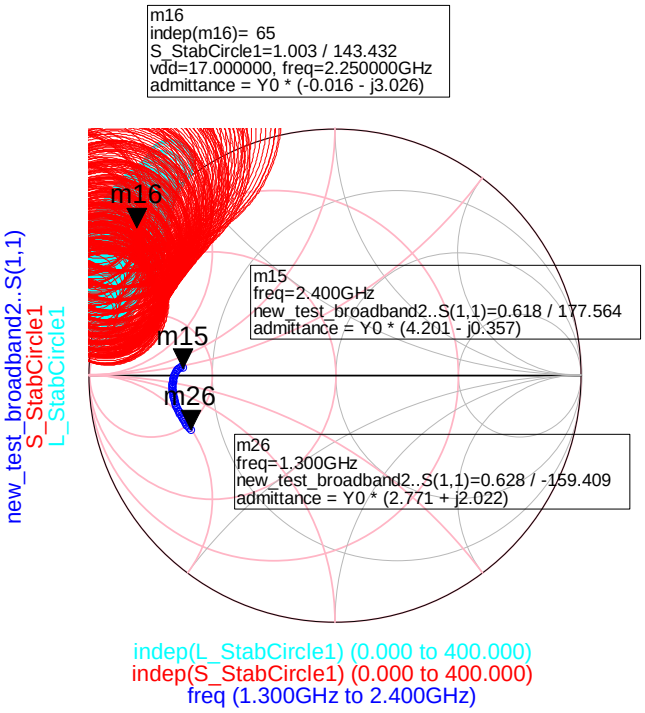


Figure 4.12 The stability circles and input reflection coefficient of input matching from 1.35 GHz to 2.35 GHz (normalized to 50 Ohms)

In figure 4.12, the blue line represents how the reflection coefficient varies with frequency (seen from A to B in figure 4.12). The red circles represent the source stability circles. We can see the blue line is outside the source stability circles. The light blue circles represent the load stability circles.

Output matching network:

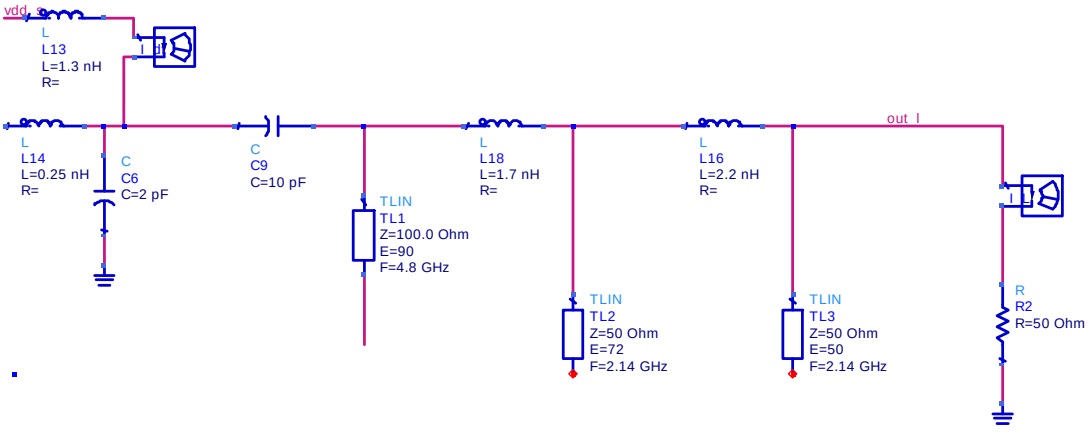


Figure 4.13 Output matching network for 1GHz hybrid class power amplifier

The load condition:

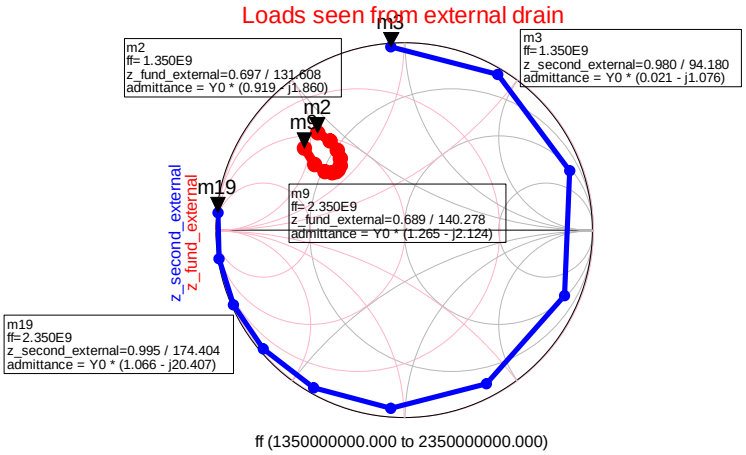


Figure 4.14 Fundamental (red) and second harmonic (blue) loads for 1GHz hybrid class power amplifier (from 1.35 to 2.35 GHz, normalized to 30 Ohms)

So, the output loads are also outside the output stability circles.

Input matching network realized with micro-strip line:

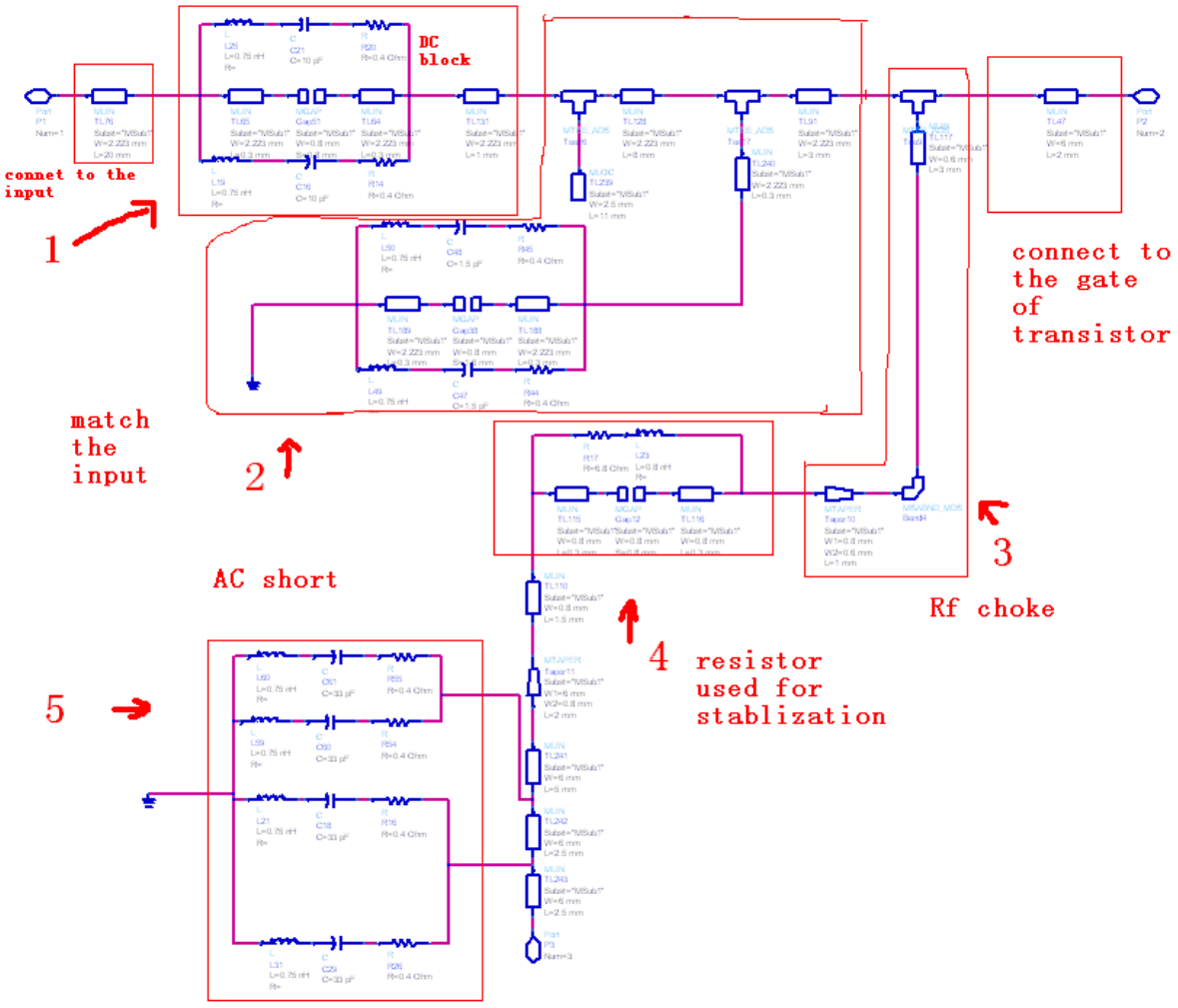


Figure 4.15 Input matching realized with micro-strip line

The components in figure 4.11 have been replaced by the components using the same numbering as in figure 4.15. Other small pieces of transmission line are used to connect the source, gate bias and transistor gate.

Output matching network realized with transmission line:

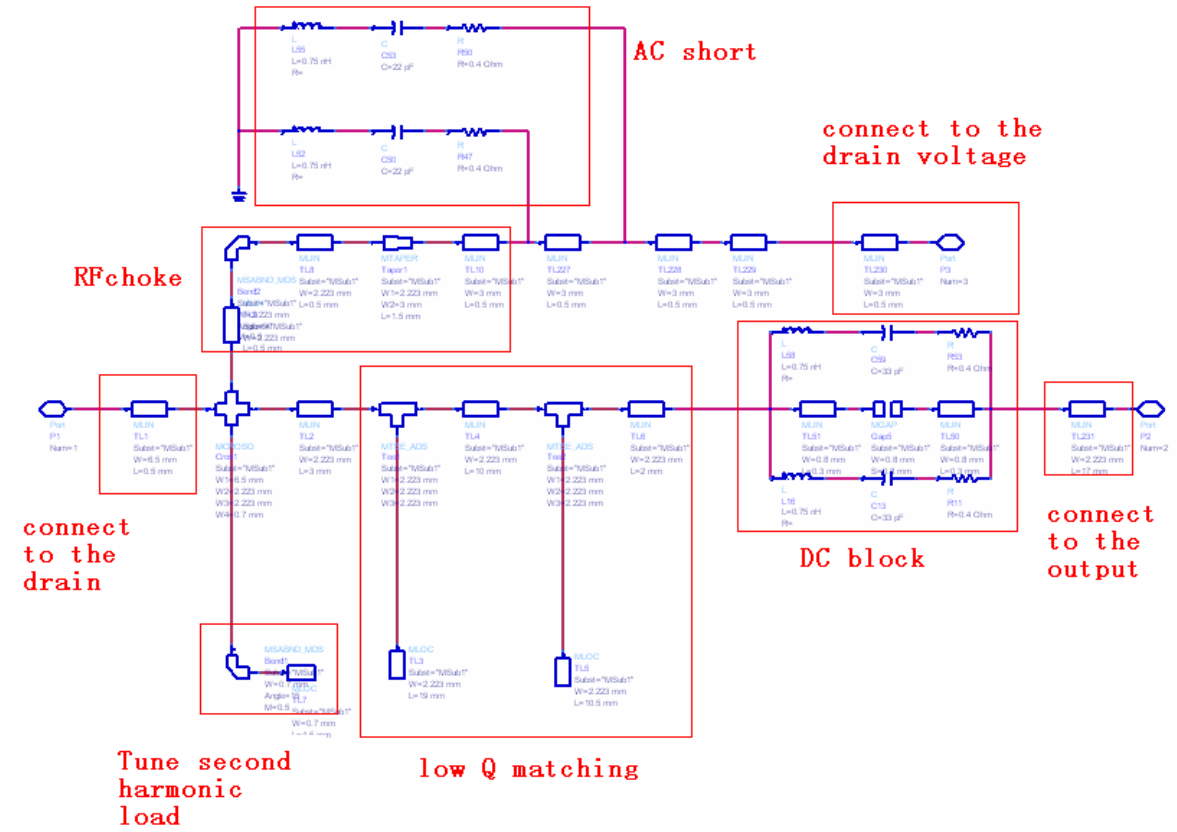


Figure 4.16 Output matching network realized with micro-strip line

The component values are in figure 4.16 are tuned to achieve similar load condition of the matching network in figure 4.13.

Simulation results:

After matching the input and realize the matching network with transmission lines we start to test the performance of this implementation. The simulation parameters are:

1. Frequency bandwidth: 1.35 to 2.35 GHz

2. Gate voltage: 2.25 V

3. Drain supply voltage: 10 to 30 V

4. Input power: The input powers are chosen at 1 dB compression points for each

supply voltage and frequency.

The simulation results are as follows:

1. The load trajectory as seen from internal drain (including both package and device parasitics) (Figure 4.17)

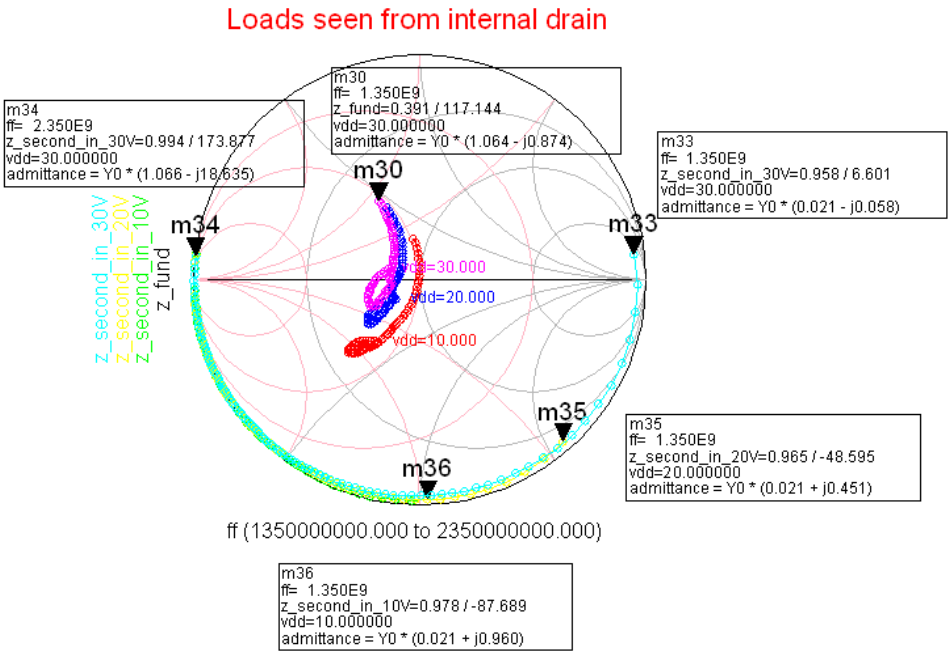


Figure 4.17 The output loading as seen from the internal drain (including both package and device parasitic, the Smith chart is normalized to 30 Ohms). Red, blue, pink line represents the fundamental harmonic loads at 10 V, 20 V and 30 V respectively. Green, yellow, light blue line represents the second harmonic loads at10 V, 20 V and 30 V respectively.

We can see from figure 4.17, some of the loads meet the solution 1 of sub-optimal class-J or class-E (inductive fundamental harmonic load and capacitive second harmonic load). Some meet the solution 2 of sub-optimal class-J.

2. Efficiency, output power and power gain:

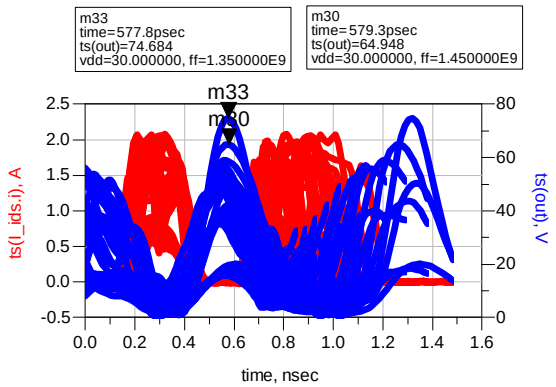


Figure 4.18 (a) Drain voltage (blue) and current (red) for different supply voltage and frequency

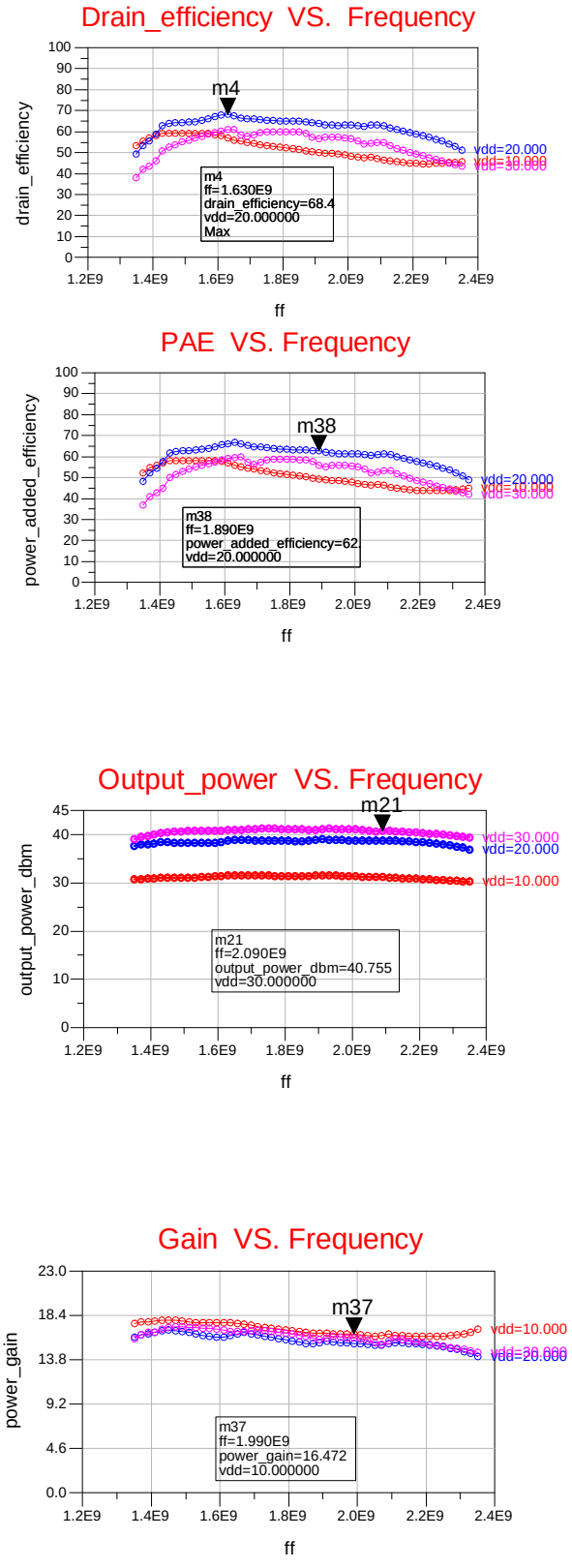


Figure 4.18 (a) The performance of 1 GHz bandwidth hybrid class power amplifier. Red, blue and pink represents 10 V, 20 V and 30 V supply voltage respectively.

The drain efficiency and PAE are around 50%-65% for the different supply voltage values. The power gain is 16-17 dB for different supply voltages. The peak output power remains around 40- 41 dB over the bandwidth. The peak drain voltage from 1.35 to 1.45 GHz have exceed the breakdown voltage (figure 4.18 (a)). So, it's not practical for the PA operates at this frequency region.

3. Performance versus power back-off when applying voltage modulation.

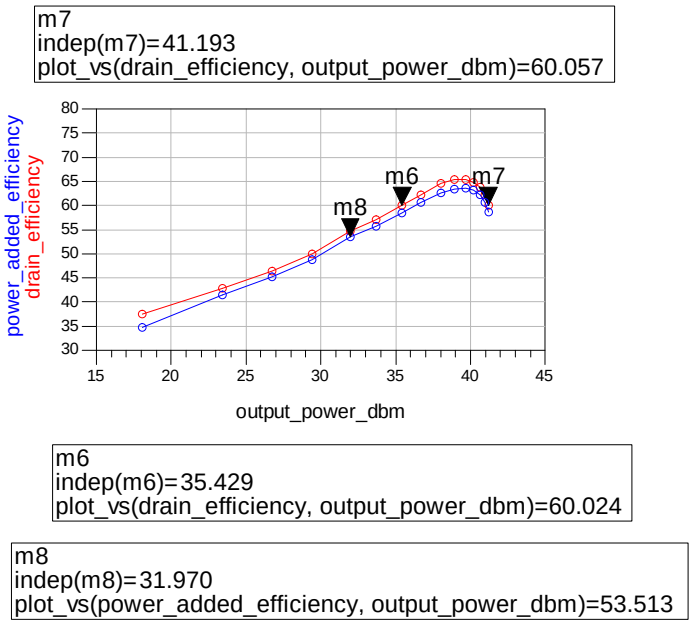


Figure 4.19 The efficiency performance without over-drive as function of supply voltage modulation at the center frequency of the band (1.8 GHz)

If we don't over-drive the power amplifier at low supply voltage (the input power are chosen below the 1 dB compression point for each supply voltage), the power amplifier can keep its drain efficiency and PAE around 55% at 8-9 dB power back-off point.

Except at the edge of the bandwidth (2.3 GHz) for all other frequencies the performance of the amplifier is quite similar. At higher frequencies the performance degrades somewhat.

4. Operation class.

We can check the operation class at 1.8 GHz as an example. The loads seen from the external and internal drain at 10 V are as follows (figure 4.20):

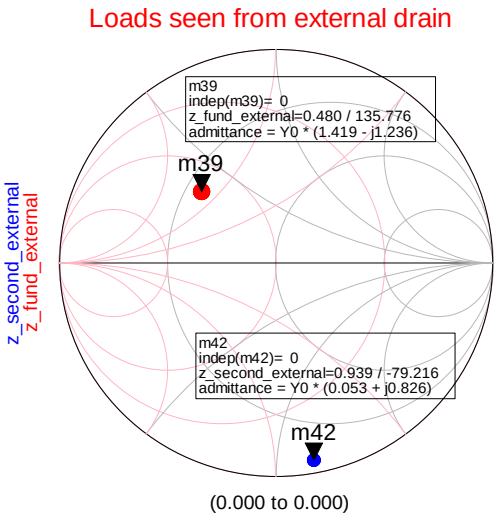


Figure 4.20 (a) The fundamental (red) and second (blue) harmonic load seen from external drain (including the package parasitic and excluding the device parasitic, normalized to 30 Ohms)

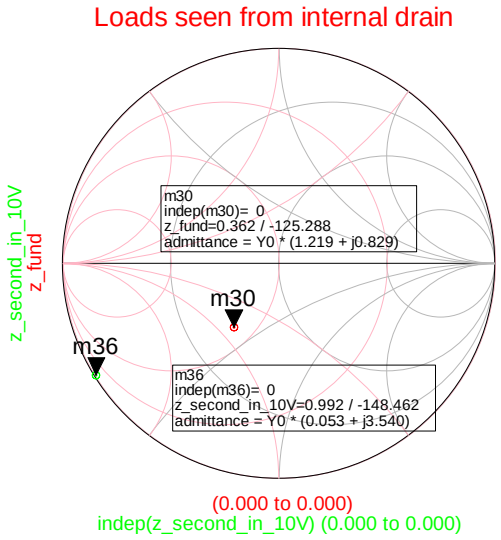


Figure 4.20 (b) The fundamental (red) and second (blue) harmonic load seen from internal drain (including the package parasitic and device parasitic, normalized to 30 Ohms)

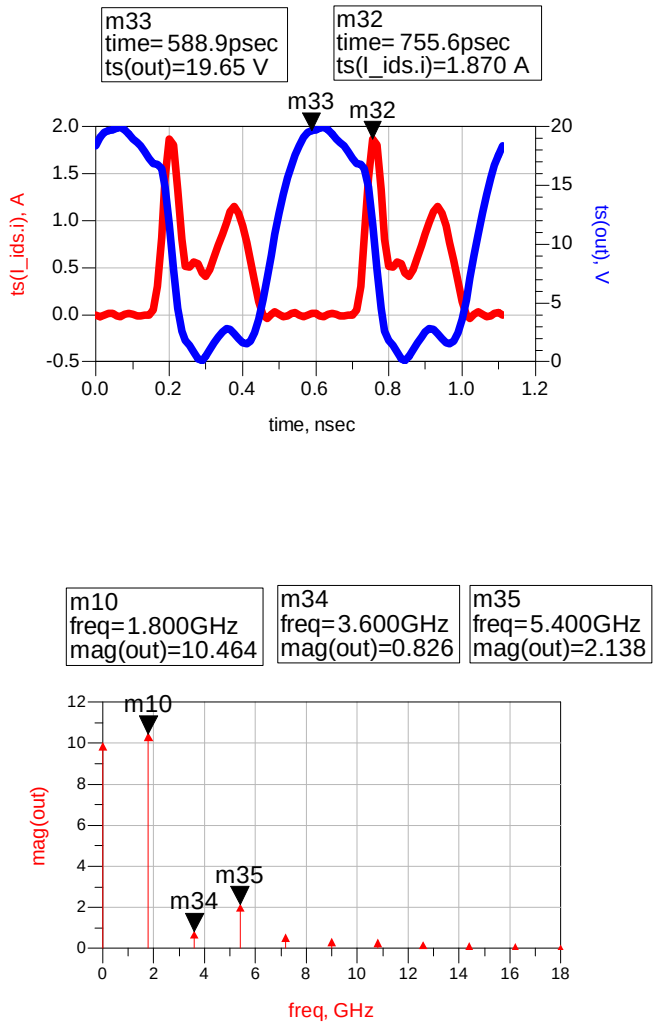


Figure 4.20 (c) The drain current (red) , voltage (blue) and drain voltage spectrum

When we see the loads from the internal drain, the fundamental and second harmonic loads are both capacitive. So, they don't meet the solution of class-J or class-E. However, the amplitude of second harmonic voltage is less than 1/10 of the amplitude of fundamental harmonic voltage (the 2nd harmonic is almost shorted). The amplitude of third harmonic voltage is even larger. So, the waveform is more like a sub-optimum class-F power amplifier. Whatever, the loads don't meet the loads solutions of optimal class-J/E/F. This is why the efficiency is only around 50-55%.

The loads seen from the external and internal drain at 30 V are as follows (figure 4.21):

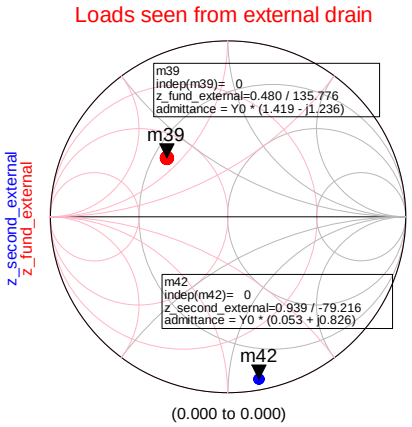


Figure 4.21 (a) The fundamental (red) and second (blue) harmonic loads seen from external drain (include the package parasitic and exclude device parasitic, normalized to 30 Ohms)

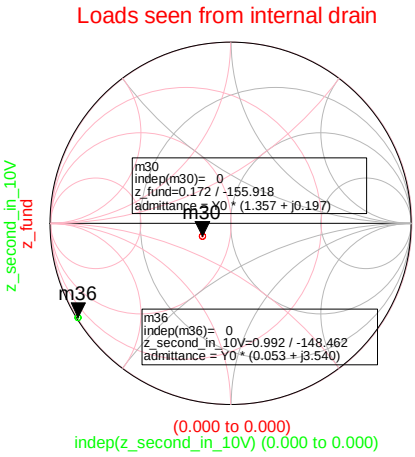
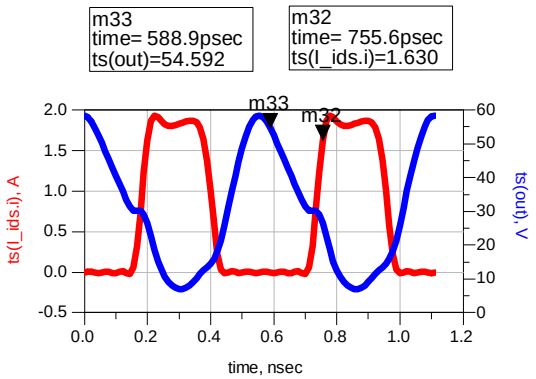


Figure 4.21 (b) The fundamental (red) and second (blue) harmonic loads seen from internal drain (include both the package parasitic and device parasitic, normalized to 30 Ohms)



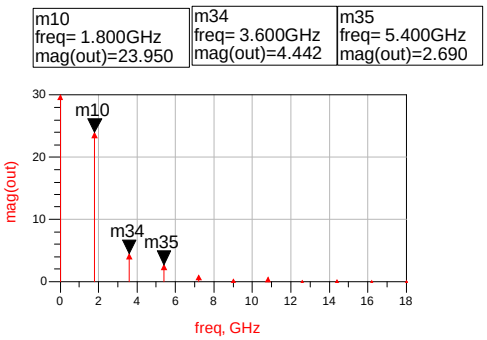


Figure 4.21 (c) The drain current (red) , voltage (blue) and drain voltage spectrum

For the loads at 30 V supply voltage and 1.8 GHz, the fundamental load is almost resistive. We still have some second and third harmonics. So, the operation class is more like a non-ideal class-AB.

We can do the same analysis for other frequencies. We find that: with the changing frequency, also the operation class of the power amplifier is changing. Operating in some situations like class-E, sometimes like class-J, sometimes like class-AB and sometimes like class-F. If we take a pragmatic attitude in this we can say that the actual operating class of the power amplifier is not so important as long as we get an acceptable to good performance.

5. Influence of second and third harmonics:
We check the influence of second and third harmonics at 1.8 GHz. The loads at 1.8 GHz are as follows:

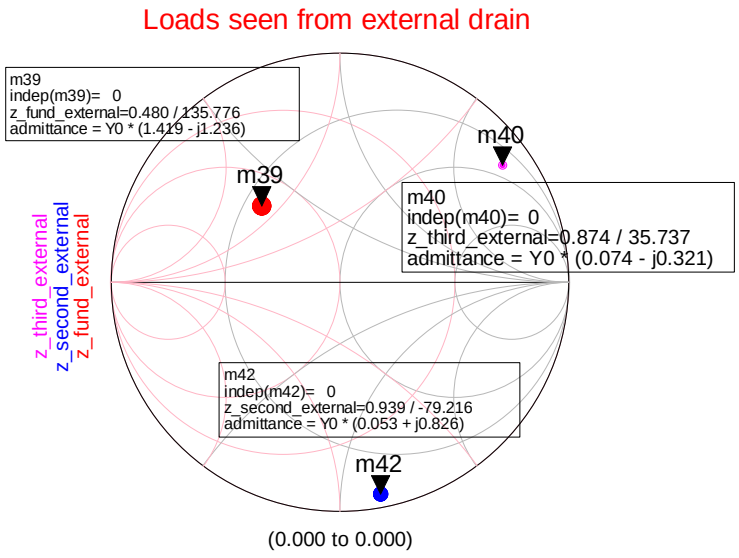
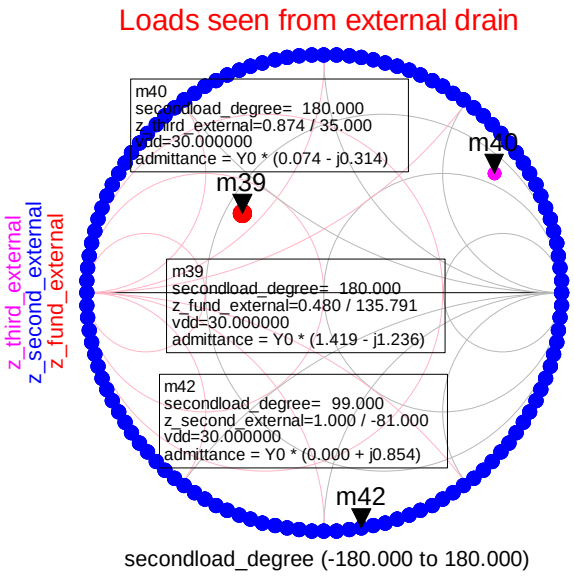


Figure 4.22 (a) The fundamental (red), second (blue) and third (pink) harmonic loads seen from external drain (include the package parasitic and exclude device parasitic, normalized to 30 Ohms)

We fix the fundamental and third harmonic load and sweep the second harmonic load angle (in polar form as we did previously. Ignore the loss at harmonics).



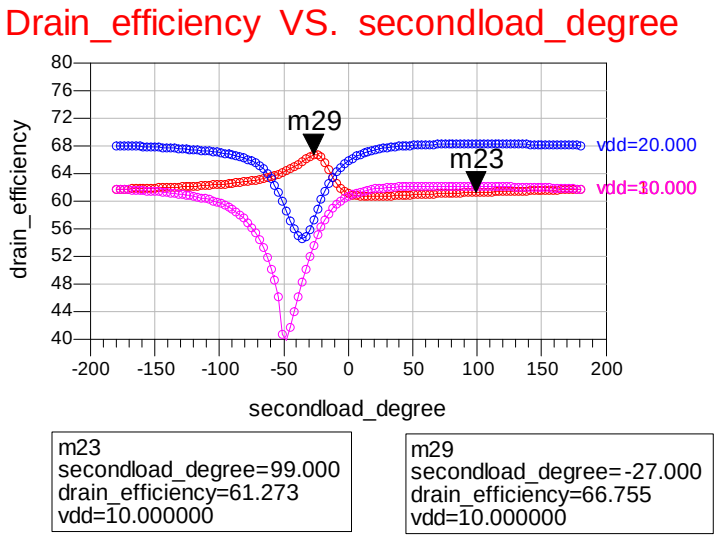


Figure 4.22 (b) Sweep the angle of second harmonic load (in degrees) Red, blue and pink represent 10V, 20 V and 30 V supply voltage respectively.

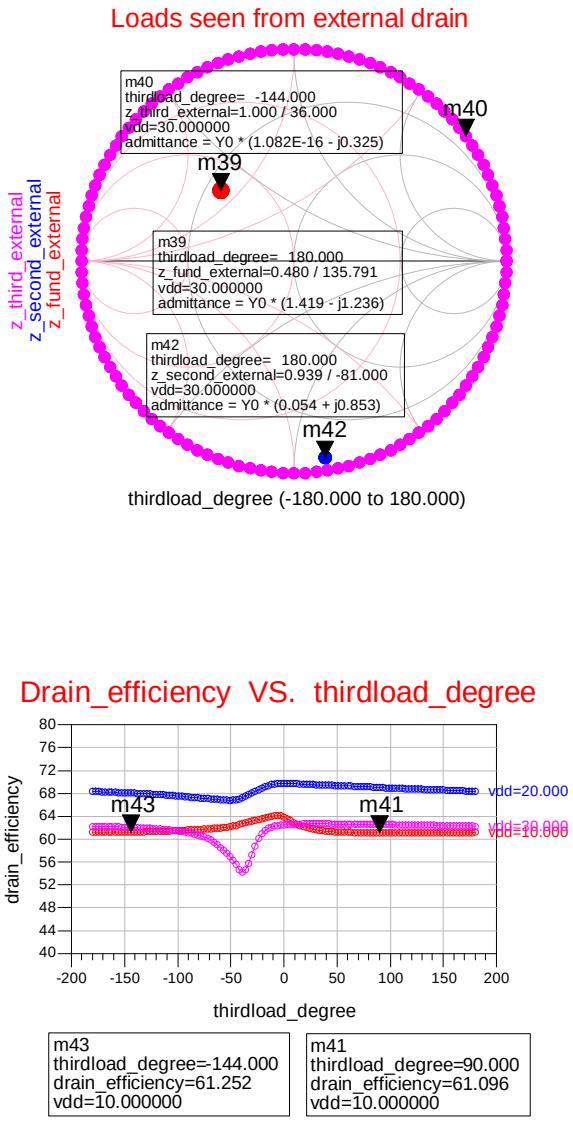


Figure 4.22 (c) Sweep the angle of third harmonic load (in degrees) Red, blue and pink represent 10V, 20 V and 30 V supply voltage respectively.

The reason for why the efficiency goes high and low with load angle has been shown in chapter 3 (figure 3.25).

The loads for second and third harmonic are 0.826 and -0.321 S (normalized to 30 Ohms) respectively. The corresponding degrees for them are 99 and -144 degrees respectively. We can see from figure 4.22, the second and third harmonic don't improve the efficiency too much. However, at least, they don't degrade the performances. For wideband power amplifier design, harmonics shorts over a wide bandwidth region is not practical. So, to some degree, it's a positive influence if the harmonics don't have a negative influence on the performance. So, for this 1 GHz version the fundamental loads are tuned properly to make the PA can maintain the

efficiency at power back-off. The second harmonic doesn't play an important role.

For the 600MHz and 750 MHz (see appendix) version hybrid-class PA, we successful use the second harmonic to improve the performance at some frequency region. This proves what we have predicted previously: when the bandwidth becomes very large, the effective tuning of second harmonic is very difficult.

Section 7 Conclusion

In this chapter, we have described the design process for wideband PA and presented a 1 GHz bandwidth hybrid-class PA. The overall conclusion is we can obtain 1 GHz bandwidth and keep the efficiency around 45%-65% when using supply voltage modulation with NXP latest generation LDMOS.

Chapter 5 Layout and Testing

In last chapter we have designed a 1 GHz bandwidth hybrid class power amplifier for an EET or ET system. The next step is to draw a layout

Section 1: Layout of 1 GHz bandwidth hybrid class power amplifier:

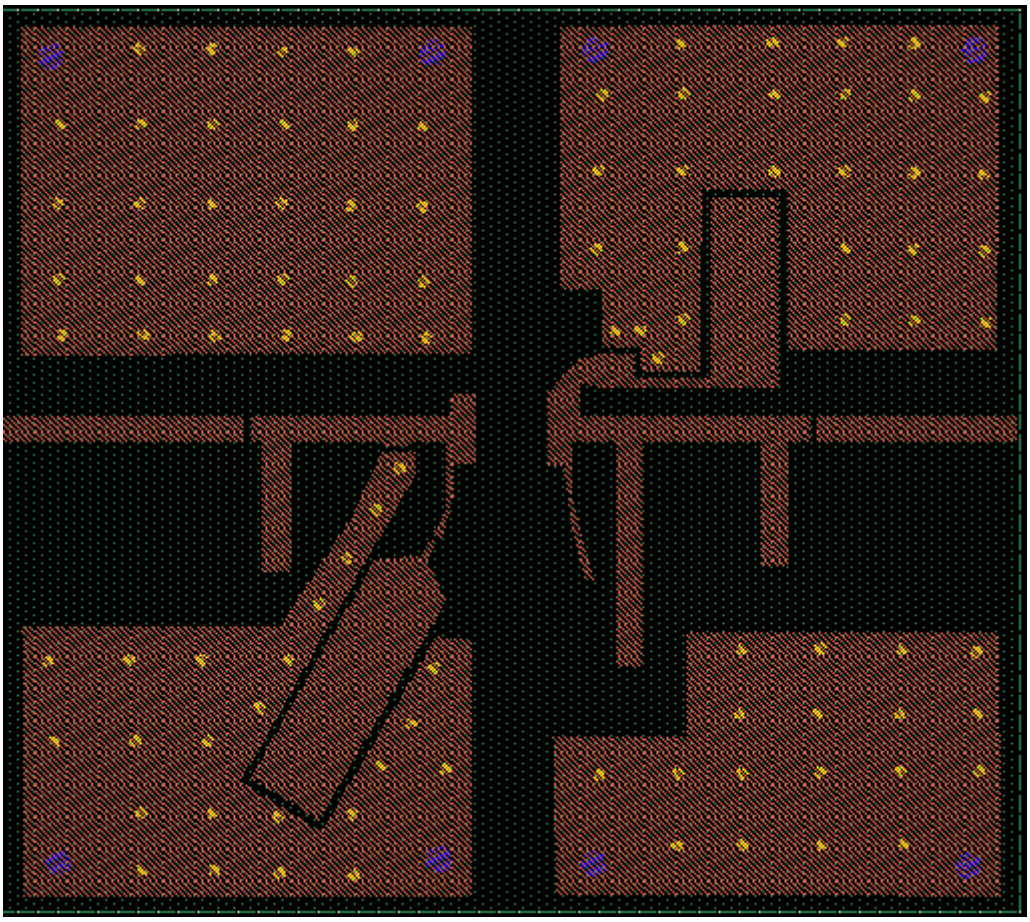


Figure 5.1: Layout of the 1 GHz bandwidth hybrid class power amplifier

1. The small yellow circles represent via holes
2. Purple circles represent the screw holes used to connect PCB board and heat sink.
3. The four brown rectangles represent ground on the PCB (connect the heat sink through yellow holes)
4. The package of capacitors used for AC short at gate and drain contain will have some paracitics. If we can mount more capacitors in parallel, the parasitics can be minimized. So, the gate and drain bias terminals are extended to have more room for decoupling.

Section 2: Momentum simulation results:

We can perform momentum simulation with the layout above. Using the S-parameters we obtained from this momentum simulation, we can check that whether the

momentum simulation has similar results as found from the simulation using the component models. Since we cannot accurately model capacitors and resistor in the layout, we use momentum to simulation the layout in parts (Figure 5.2):

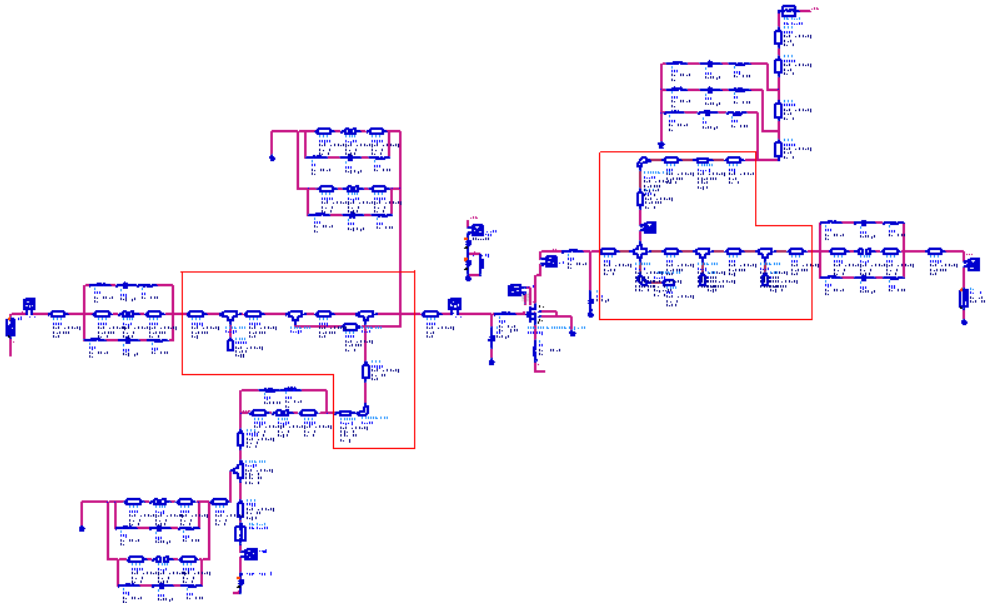


Figure 5.2 (a) Power amplifier implemented with micro-strip line

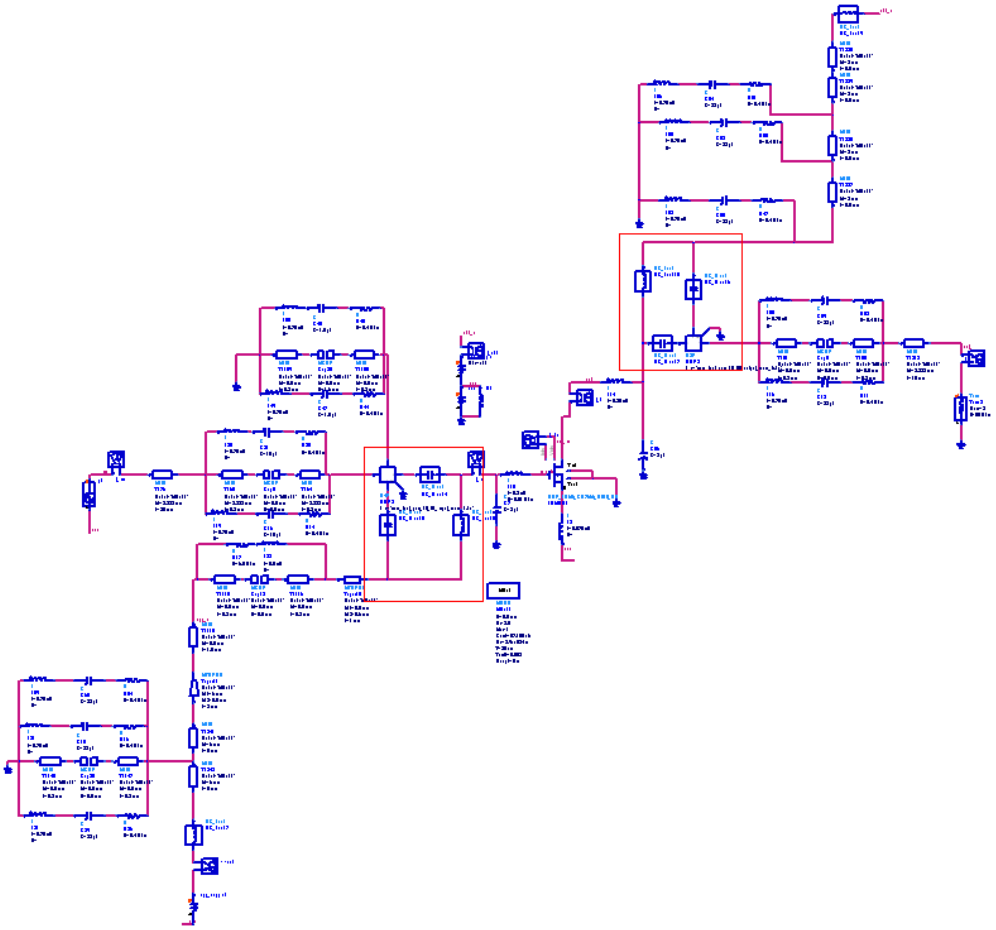


Figure 5.2 (b) Simulation setup where the red region of figure 5.2 (a) is replaced with S-parameters from the momentum simulation for this part (red region in figure 5.2 (b))

We replace the red region of figure 5.1 (a) with S-parameters data (red region in figure 5.2 (b)), obtained by momentum simulation for these parts).
There are some differences between momentum and schematic simulations. It's difficult to indicate, which one is more accurate. So, our basic strategy is making these two simulation results as close as possible.
The load conditions of two simulations are as following:

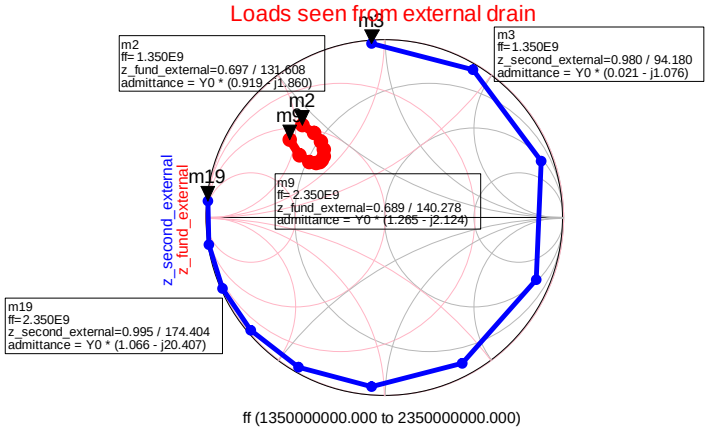


Figure 5.3 (a) Load condition of schematic simulation seen form external drain (From 1.4 to 2.3 GHz. Red, fundamental load. Blue, second harmonic load. The Smith chart is normalized to 30 Ohms)

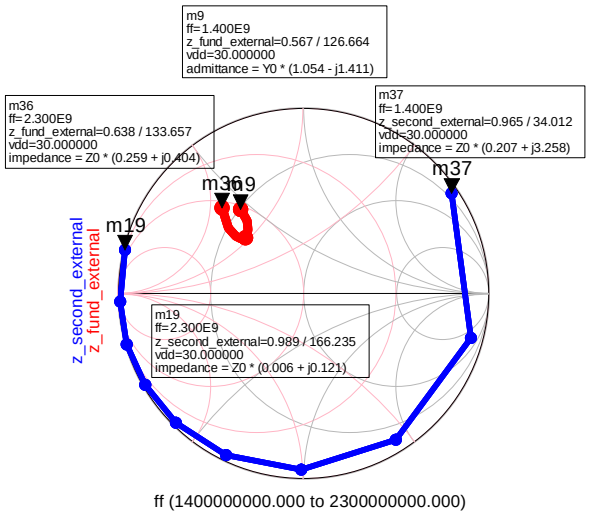
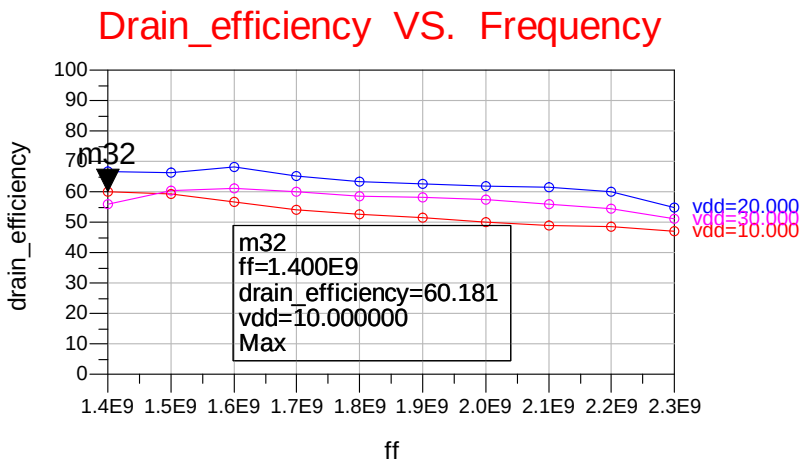


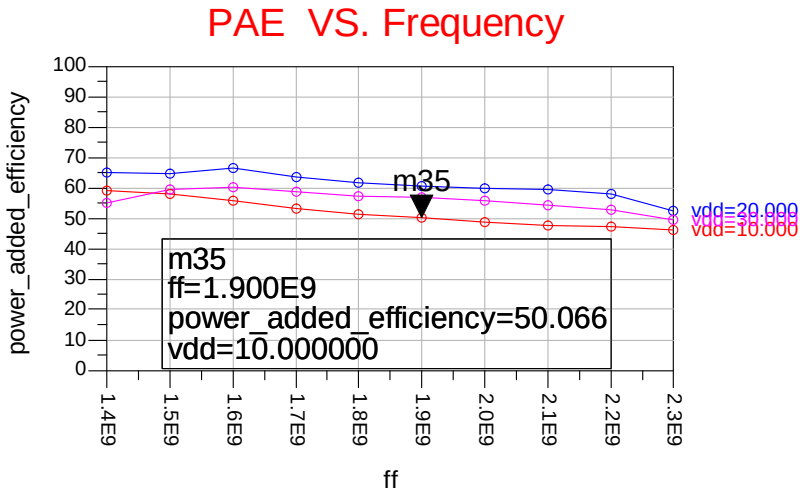
Figure 5.3 (a) Load condition of Momentum simulation seen from the external drain (From 1.4 to 2.3 GHzRed, fundamental load. Blue, second harmonic load. The Smith chart is normalized to 30 Ohms)

From figure 5.3, we can see the differences are quite small. The amplifier performance using the Momentum simulated data is as follows:

Simulation parameters:

1. Bandwidth: 1.4 to 2.3 GHz. Between 1.3 GHz and 1.4 GHz, the drain voltage exceeds the breakdown voltage. So, we abandon this region. The bandwidth decreases to 900 MHz.
2. Gate bias: 2.25 V
3. Drain voltage: 10 V to 30 V, supply voltage step is 10V
4. Input powers: All the input powers are chosen below or at the 1 dB compression point for each supply voltage.





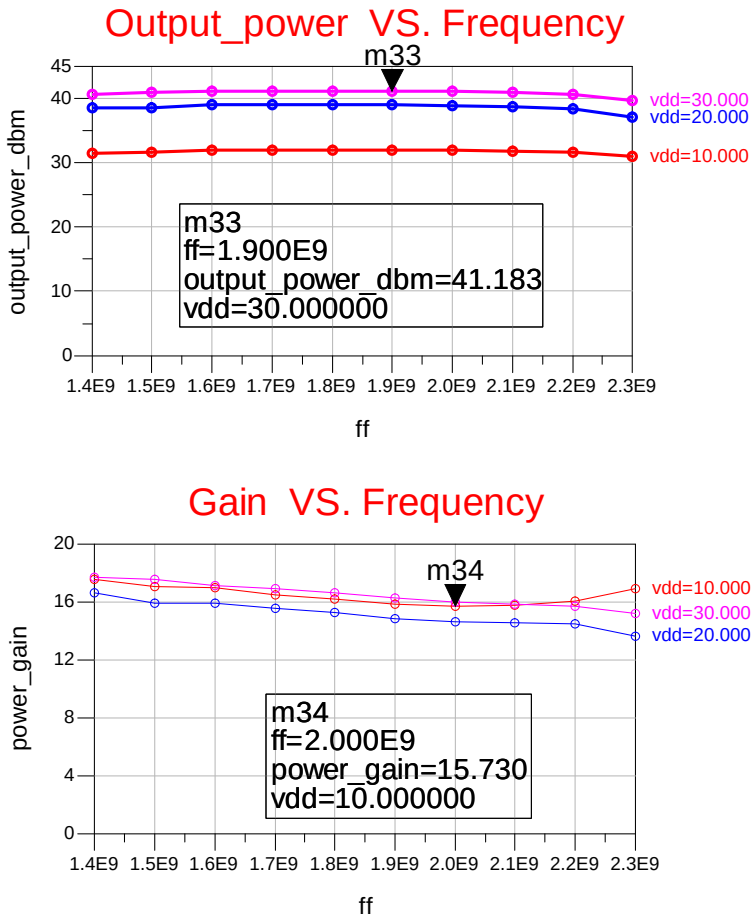


Figure 5.4 Simulated performance using the Momentum s-parameter data

We can compare the results with that of schematic simulation in chapter 4. These two performances are similar.

Section 3: Measurement results:

The Measurement parameters are as follows:

1. The input powers are chosen at 1dB and 3dB compression points. The performances at 1 dB and 3 dB compression points are measured. The drain efficiency vs. frequency plot is as follow (the index of x axis represent the index of frequency. 0 is 1.4 GHz, 20 is 2.3 GHz, step is 50 MHz):
2. Gate voltage: 2.2 V, which is slightly different from the one used in the simulation (2.25 V).
3. Drain voltage: 5 V, 7 V, 12 V, 16V, 22 V, 25 V and 30 V (the marks representing different supply voltages are shown in the graphs)
4. Bandwidth: 1.4GHz to 2.3 GHz. From simulation results, we notice that the drain

voltage at 1.3 GHz is very close to the breakdown voltage. So, for safety considerations, we only test the realized amplifier 1.4 GHz to 2.3 GHz..

The measurment results at 1dB compression point are as follows:

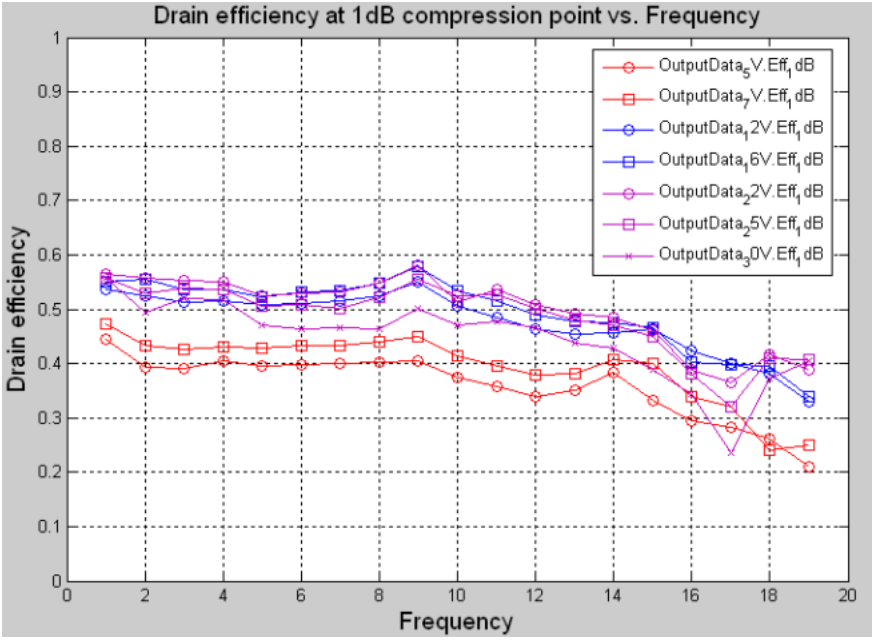


Figure 5.5 (a) Drain efficiency vs. Frequency (from 1.4 to 2.3 GHz, step 50MHz)

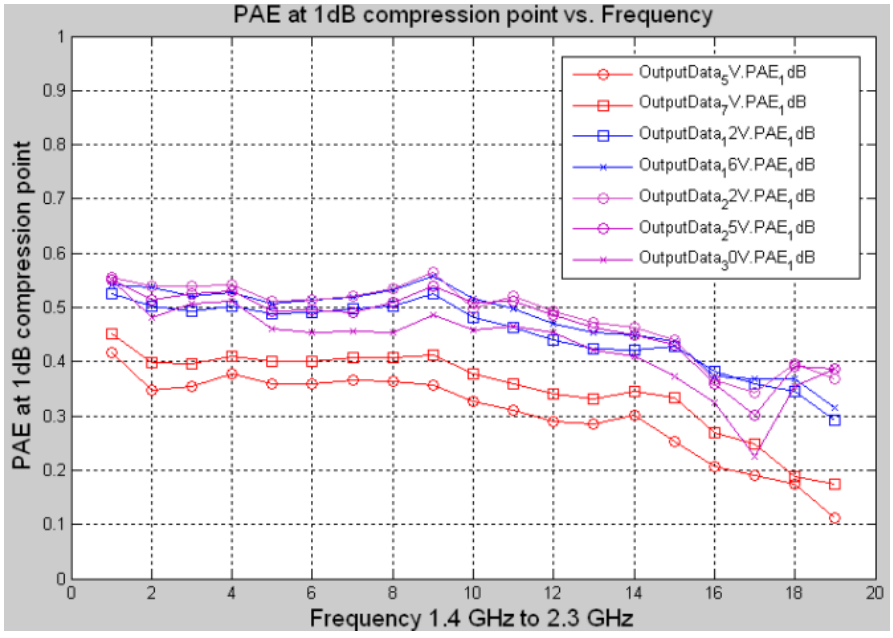


Figure 5.5 (b) PAE vs. Frequency (from 1.4 to 2.3 GHz, step 50MHz)

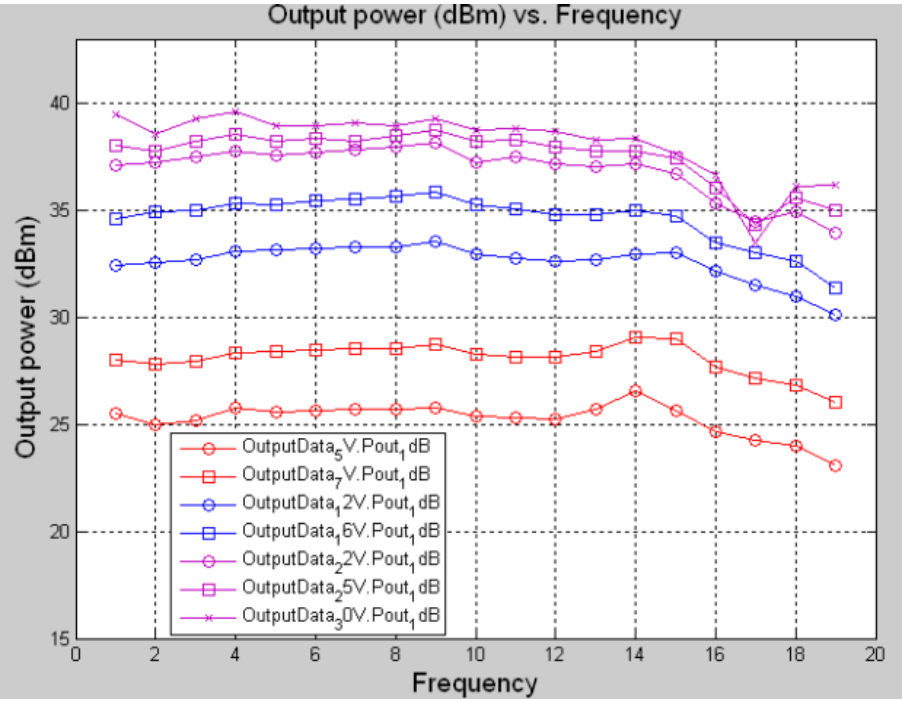


Figure 5.5 (c) Output power (dBm) vs. Frequency (from 1.4 to 2.3 GHz, step 50MHz)

We can see that the power amplifier can't reach the peak power at 1 dB compression point. So, the drain efficiency and PAE are not so good at 1 dB compression point.

The measurement results at 3 dB compression point:

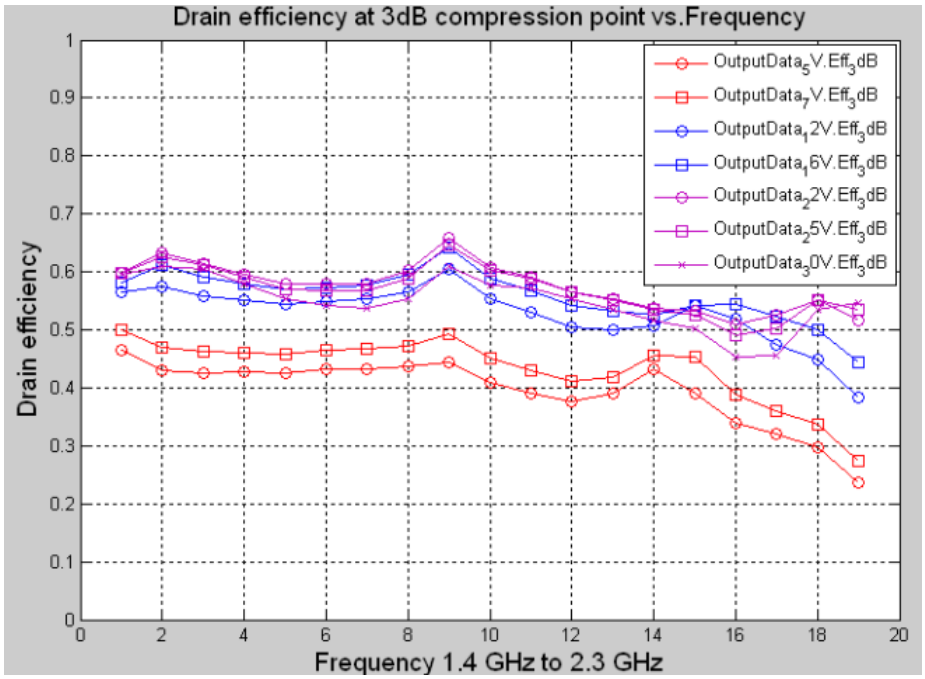


Figure 5.6 (a) Drain efficiency vs. Frequency (from 1.4 to 2.3 GHz, step 50MHz)

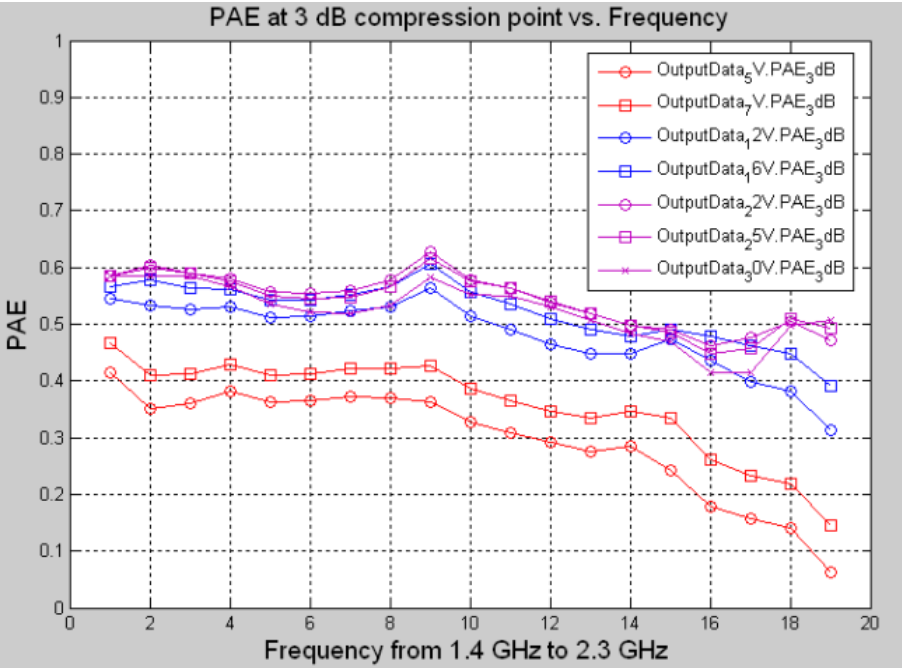


Figure 5.6 (b) PAE vs. Frequency

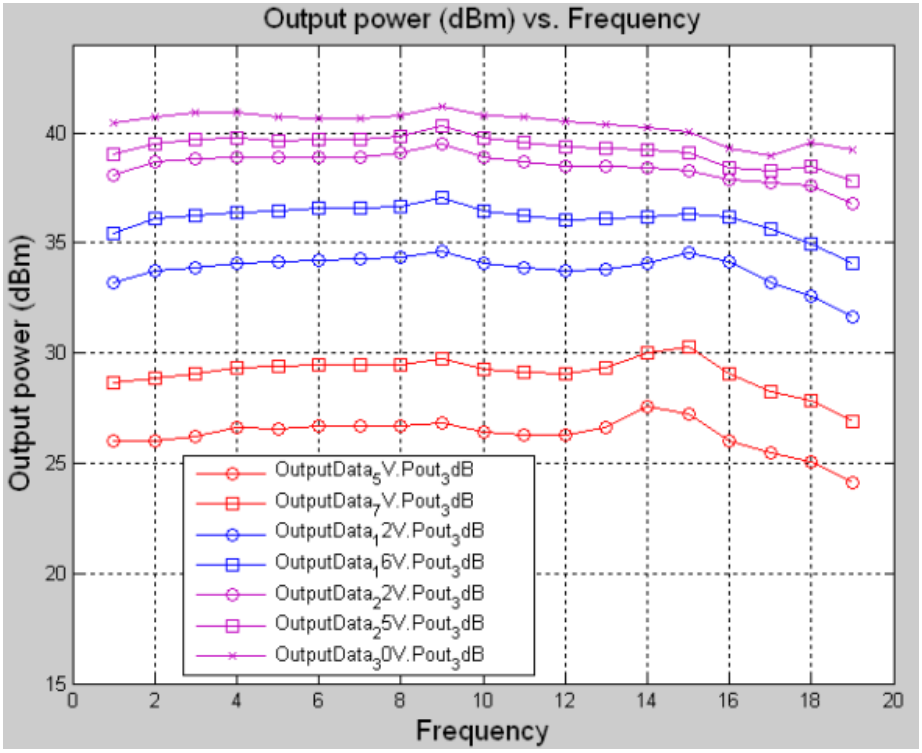


Figure 5.6 (c) Output power (dBm) vs. Frequency (from 1.4 to 2.3 GHz, step 50MHz)

In figure 5.6, we see that at 3 dB the drain efficiencies at 20 V and 30 V supply voltage are between 55% to 65% except at 2.2 GHz. The drain efficiency at 10 V supply voltage is between 45% to 55% except at frequencies higher than 2.15 GHz. We can compare this result to figure 5.4-5.6 and figure 4.42 in chapter 4. The measured data is closer to the schematic simulation results than the Momentum based simulation. The dip at 2.2 GHzis due to the influence of second harmonic load. In chapter 4, when we sweep the phase angle of second harmonic load, we had seen such

kind of dip. For simulation results, there is no such kind of dip. So, the reason for this dip may be: 1. The model of the device is not accurate enough. 2. The fabrication of the matching network is not accurate enough. 3. The position we place the capacitors in the matching network is not accurate enough.

The performances for 1.5 GHz, 1.8 GHz and 2.1 GHz at power back-off (figure 5.7):

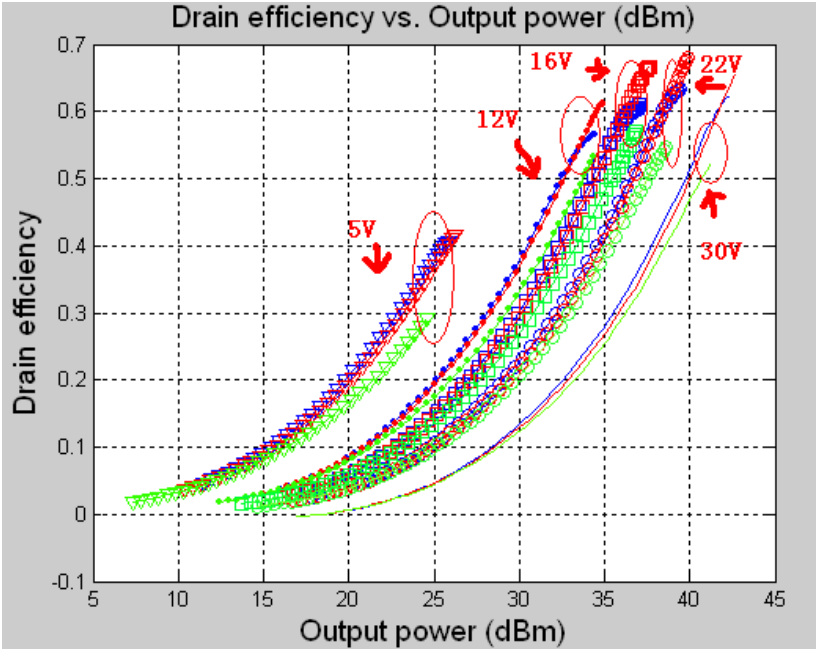


Figure 5.7 (a) Drain efficiency vs. output power (dBm)

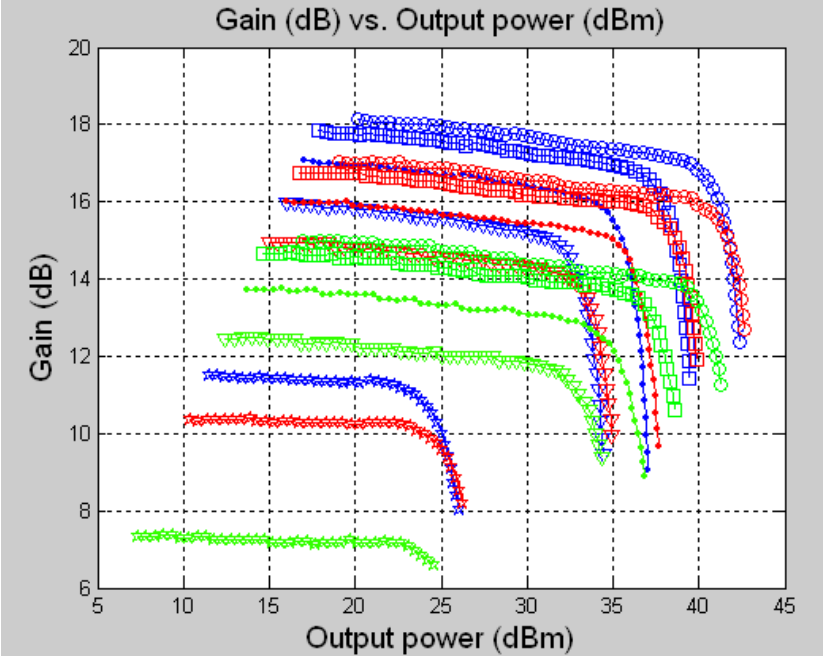


Figure 5.7 (b) Gain (dB) vs. output power (dBm)

In figure 5.7, the mark of circles, squares, dots, triangles and stars represents 30 V, 22 V, 16 V, 12 V and 5 V supply voltage respectively. Blue, red and green represent the performances at 1.5 GHz,

1.8GHz and 2.1 GHz respectively.

From figure 5.6, we can conclude that we can only get a good efficiency performance when we over-drive the power amplifier to the 3dB compression point. Comparing with it, we can get the same performance at 1 dB compression point for simulation results. That means the fabricated PA compresses faster. The reason for this may be due to the fact the model is not accurate enough.; The fabrication of the matching network is not accurate enough; Or, the position we place the drain AC short capacitors in the matching network is not properly (the package parasitics of the capacitor will affect the load condition).

The gain at high supply voltage is around 14 to 17 dB. At low supply voltage, like 5 V, the gain decreases to 7 to 11 dB. The reason for this is that at lower supply voltage, the parasitics are larger as is the case with higher supply voltage. So, we need more input power to drive the power amplifier which will reduce the gain.

Section 4 Conclusion:

In this chapter, we have given the layout for the 1 GHz bandwidth hybrid class power amplifier. After fabrication, we have tested its performance. The testing results are similar to the simulation results.

Chapter 6 Conclusions

In this project, we have designed “narrowband” and wideband power amplifiers for envelope tracking system applications, using second harmonic tuning for the active device.

The simulation results show that the packaged 12 W NXP generation 7 LDMOS is not suitable for hybrid-class operation at high frequency (higher than 2.0 GHz) due to the influence of parasitics of device (chapter 3). With a 2 W NXP 7 LDMOS on wafer device, which has smaller parasitics, we also get good performance at 2.14 GHz (appendix 4). However, the 12 W LDMOS is still suitable for hybrid-class operation at lower frequencies (as shown in chapter 3).

For wideband design, we successfully use the second harmonic to improve the efficiency when we design a 750 MHz bandwidth power amplifier optimized for single supply voltage (appendix 2). However, when we increase the bandwidth and use supply voltage modulation, effective 2^{nd} harmonic tuning becomes, more and more, difficult. For the 600 MHz bandwidth PA, optimized for efficiency in power back-off operation, the second harmonic has only little influence. For the 1GHz bandwidth amplifier version, the second harmonic has almost no impact, as long as, the phase range around -50^{o} for the 2^{nd} harmonic is avoided. The reason that efficiency can be maintained in power back-off operation is due to the proper choice of fundamental load, and scarifying somewhat the efficiency at higher supply voltages. This is still meaningful, because the PA is designed for WCDMA applications in which the signal rarely reaches its peak power conditions.

In chapter 5, we have given the final layout of the 1GHz bandwidth power amplifier and its measured performance. The measurement results are found to be in agreement with the simulation results.

Future work: If we can find a matching topology which can tune the second harmonic more effectively or we can make use of the computer to help us match the load trajectory to the optimum values, the performance will be much better.

Appendix 1 PDF of WCDMA signal for 12 W power amplifier

The PDF of WCDMA signal can be approximated by:

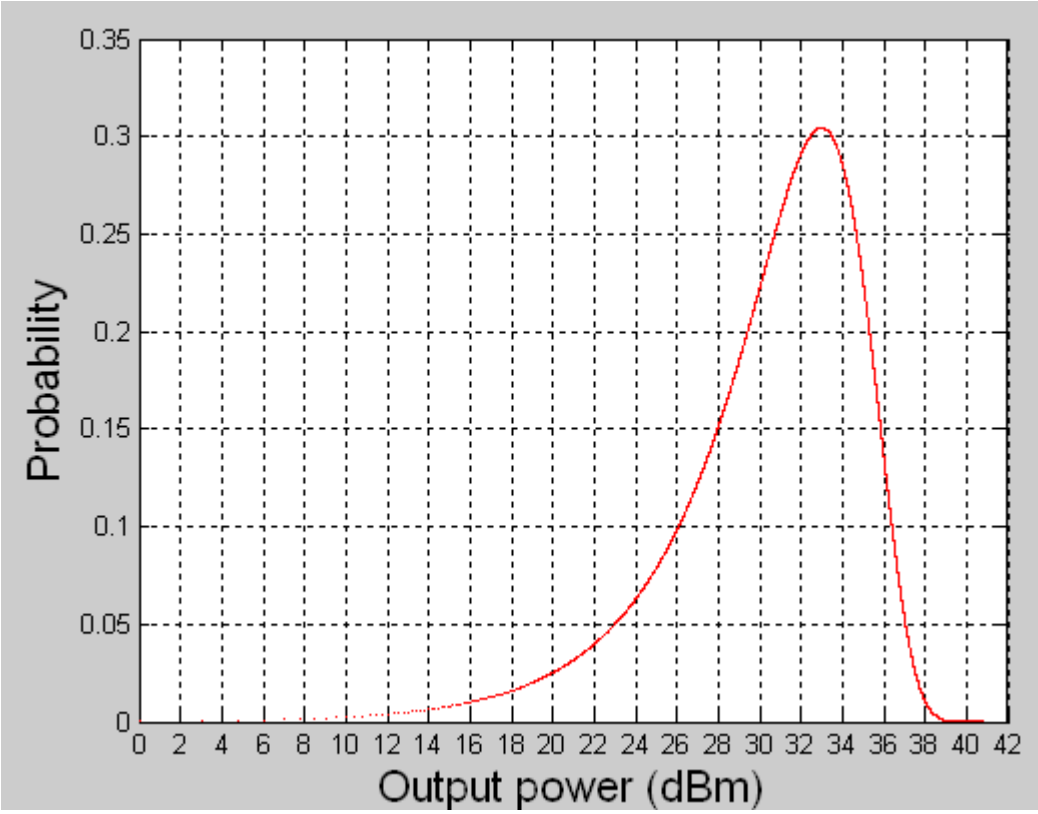
$$pdf\,(P_{out},\varepsilon) = K \times P_{out} \times \varepsilon^2 \times \exp(-(P_{out} \times \varepsilon)^2 \times \frac{1}{2})$$

Where Pout is output power in watts, K is a constant factor which can be calculated from the cumulative distribution function (CDF) of the signal. The CDF of the signal in entire span of output power should be unity. ε is peak to average ratio (PAR):

$$\varepsilon = \frac{10^{(\frac{PAR}{10})}}{P_{Max}}$$

Where PMax is maximum output power in watts. The PAR for W-CDMA signal is considered about 7.8dB [6].

The PDF plot by MATLAB:



The peak power for 12 W power amplifier is 40.7 dBm. The maximum probability is around 30% at 33 dBm which is at 7 dB power back-off from the peak power.

Appendix 2 A 750 MHz Bandwidth Class-J Power Amplifier for Single Supply Voltage

In this wideband version, we don't consider supply voltage modulation. We optimize the output loads for 30 V supply voltage only.

The simulation parameters are as follows:

1. Frequency region: 1.5 to 2.25 GHz, 750 MHz bandwidth.
2. Conjugate match the input
3. Gate voltage: 2.25 V
4. Drain supply voltage: 30 V
5. Input power: 24 dBm (below 1 dB compression point of 30 V drain supply voltage)

Output matching network:

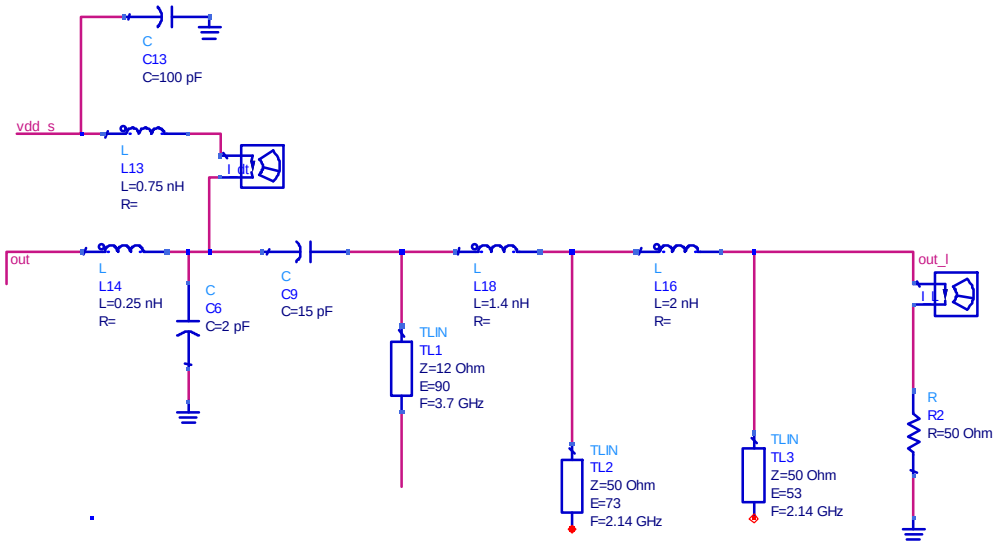


Figure Appendix 2.1 Output matching circuit of 750 MHz bandwidth power amplifier optimized for 30 V supply voltage.

We carefully tune the components values to match the load vs. frequency to the high efficiency region on the Smith chart (see figure Appendix 2.2 (a)). The load condition is shown in figure Appendix 2.2 (b)

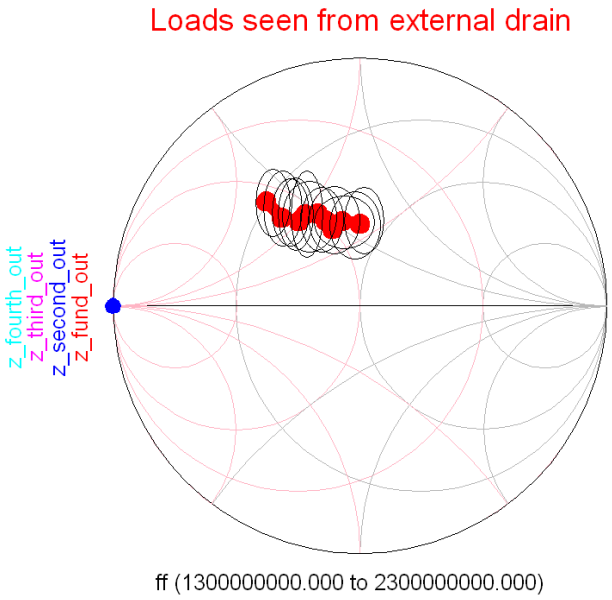


Figure Appendix 2.2 (a) High efficiency region for fundamental load (The Smith chart is normalized to 30 Ohms).

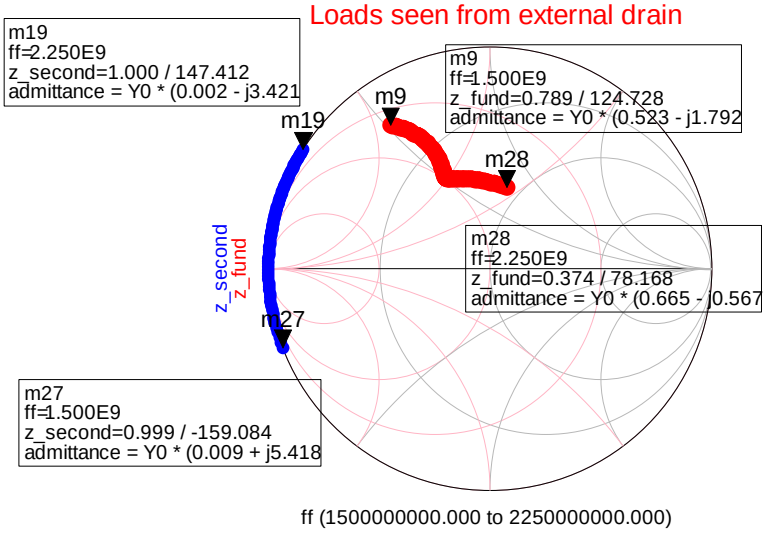


Figure Appendix 2.2 (b) Fundamental (red) and second harmonic (blue) loads over a 750 MHz bandwidth, reference plane is the external drain this includes package parasitic and exclude the device parasitic (The Smith chart is normalized to 30 Ohms).

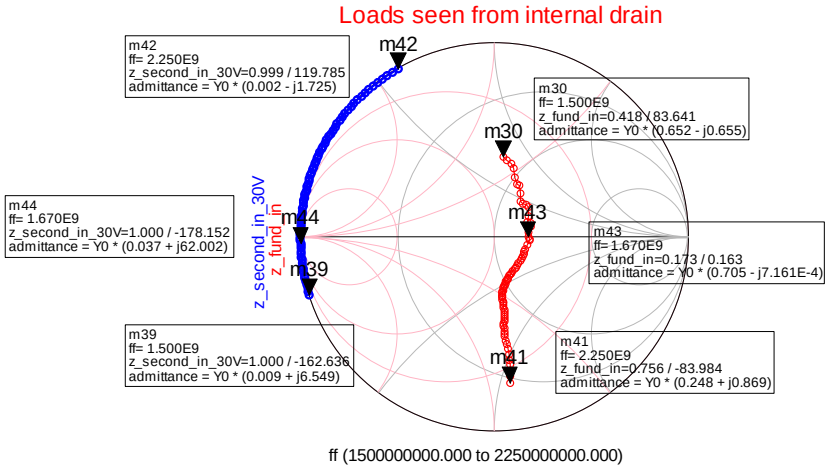


Figure Appendix 2.2 (c) Fundamental (red) and second harmonic (blue) loads over a 750 MHz bandwidth, reference plane is the internal drain this includes both package and device parasitics (The Smith chart is normalized to 30 Ohms).

Comments on the results:

1.From figure Appendix 2.2 (c) we note that, in the middle of the band (1.67 GHz, as shown in the graph), the second harmonic is almost a perfect short and the fundamental load is a pure resistor. So, at the middle of the bandwidth, the power amplifier should operate at class-AB. But, from figure Appendix 2.3 (a) we can see the drain voltage waveform is not a pure full-sine waveform and more like a class-F waveform. The reason for this is obvious when we see the spectrum of drain voltage: clearly the second harmonic is shorted but do we have some third harmonic.

In the lower frequency region of the band (1.5 to 1.6 GHz), the fundamental loads are inductive and the second harmonic loads are capacitive. They meet the first solution of class-J operation (sub-optimal solution). From figure appendix 2.3 the phase relation between drain voltage and current is the same as that of solution 1 of class-J operation (peak of drain voltage synchronizes the first valley of current, see chapter 2). But, the amplitude of second harmonic voltage is only 1/10 of that of fundamental harmonic voltage (see the spectrum of figure appendix 2.3 (b)). So, the waveform is different from the optimal class-J operation.

At higher frequency region of the bandwidth (1.75 to 2.25 GHz), the fundamental loads are capacitive and the second harmonic loads are inductive. They meet the second solution of class-J operation (sub-optimal solution). From figure appendix 2.3 (c) the phase relation between drain voltage and current is the same as that of solution 2 of class-J operation (peak of drain voltage synchronizes the second valley of current, see chapter 2). Again, the amplitude of second harmonic voltage is only 1/10 of that

of fundamental harmonic voltage (see the spectrum of figure appendix 2.3 (a)).

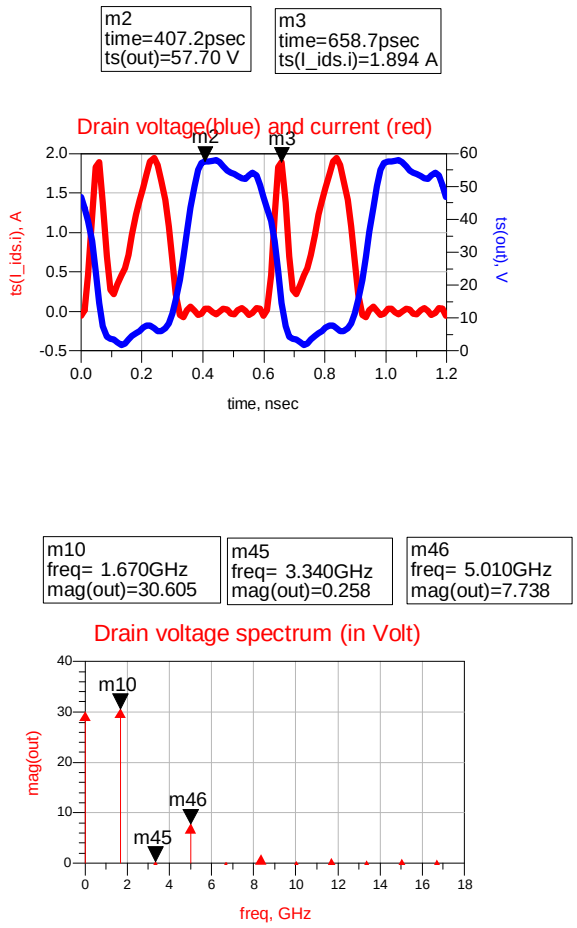
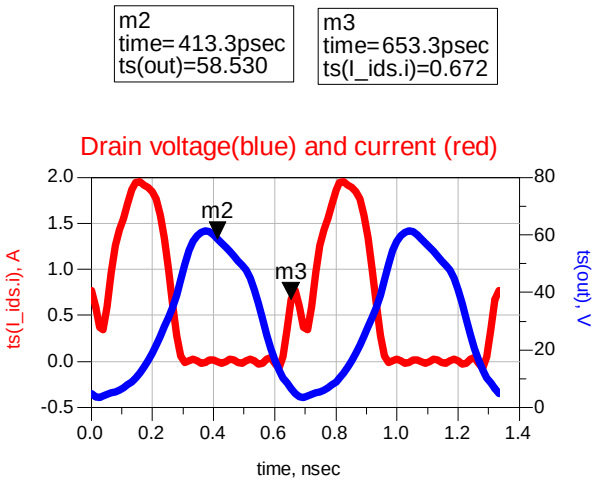


Figure Appendix 2.3 (a) Drain voltage (blue line), current (red line) and drain voltage spectrum at 1.67 GHz.



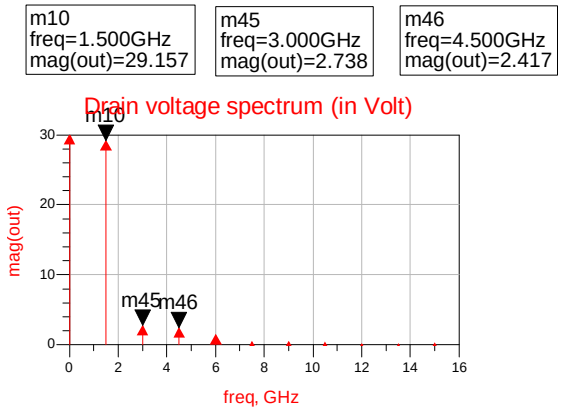
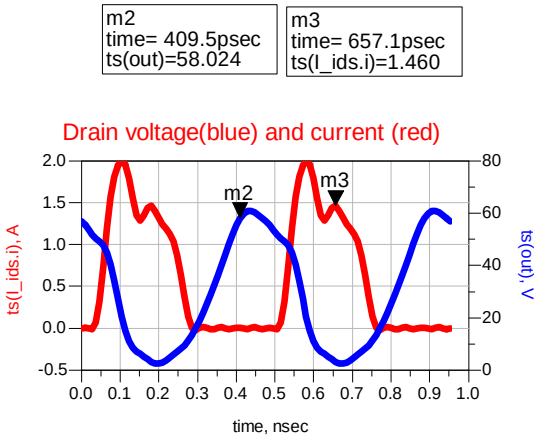


Figure Appendix 2.3 (b) Drain voltage (blue line), current (red line) and drain voltage spectrum at 1.5 GHz.



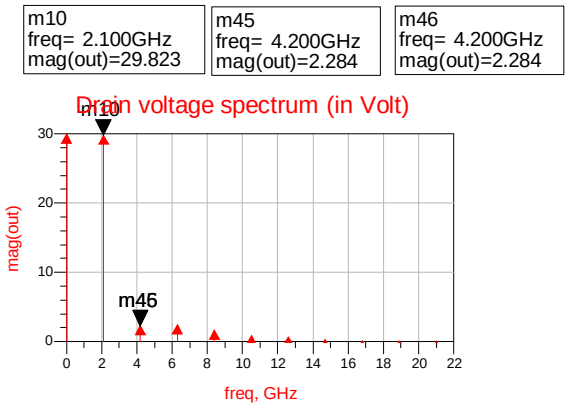


Figure Appendix 2.3 (c) Drain voltage (blue line), current (red line) and drain voltage spectrum at 2.1 GHz.

2. The performances are as follows:

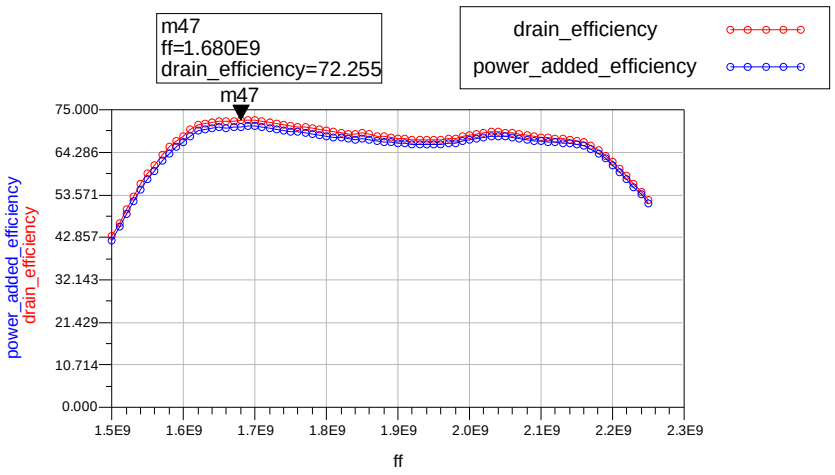


Figure Appendix 2.4 (a) Drain efficiency (red) and PAE (blue) versus frequency

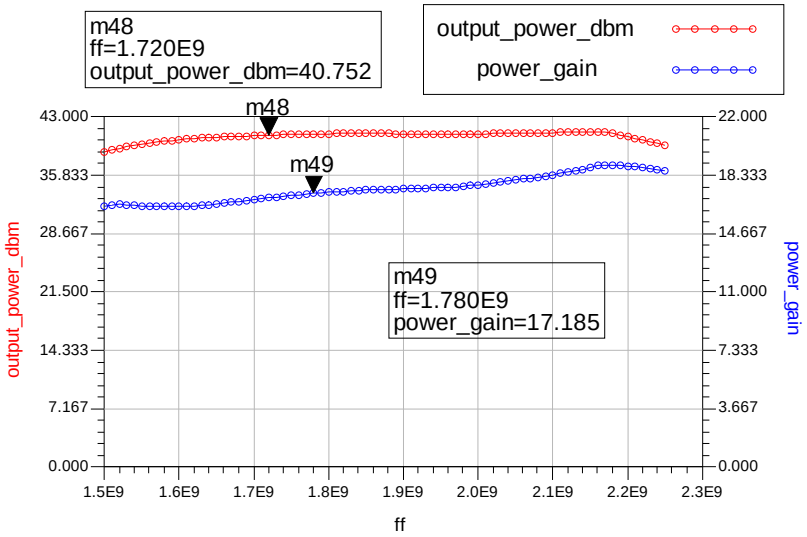


Figure Appendix 2.4 (b) Output power (in dBm, red) and power gain (in dB, blue) versus frequency

Between 1.6 and 2.2 GHz, the drain efficiency and PAE are around 65% to 72%. The output power is around 40 to 41 dBm (reaches the peak power). The power gain is around 16- 18 dB.

3. The influence of second and third harmonics.

For simplification, we transform the second and third harmonic load to a polar form

(z_secondload_polar (amplitude, angle)). We fix the amplitude of the loads and sweep the angle to check the influence on performance. We take some frequency as an example.

The loads at 2.0 GHz:

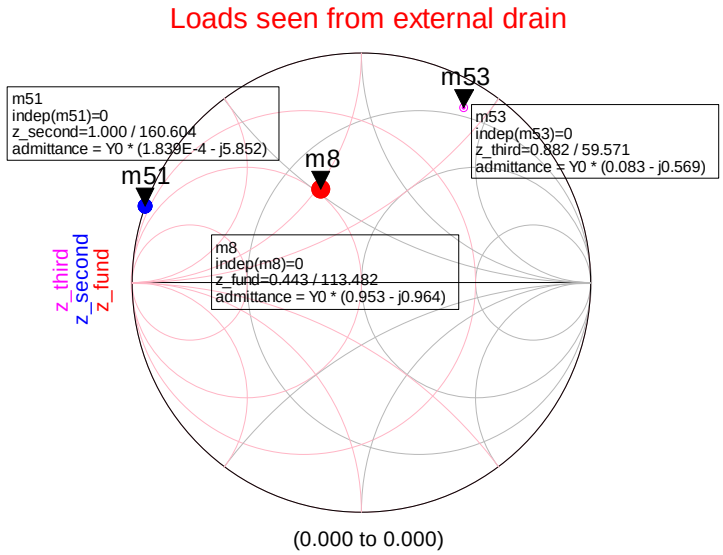


Figure Appendix 2.5 The loads seen from external drain plane (including package parasitics and excluding device parasitics) Red, blue, pink represent fundamental, second harmonic and third harmonic load respectively.

We fix the fundamental and third harmonic loads and sweep the second harmonic load

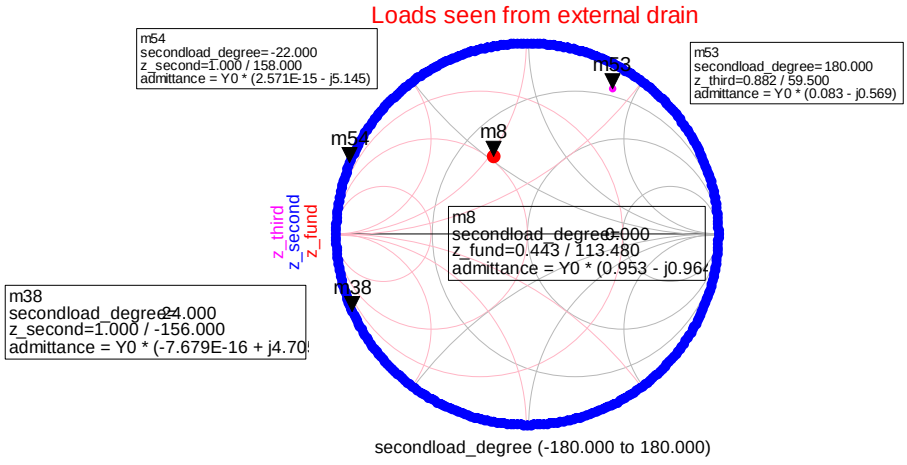


Figure Appendix 2.6 (a) Sweep the second harmonic load angle (in polar format) at 2.0 GHz The loads seen from external drain plane (including package parasitics and excluding device parasitics) Red, blue, pink represent fundamental, second harmonic and third harmonic load respectively

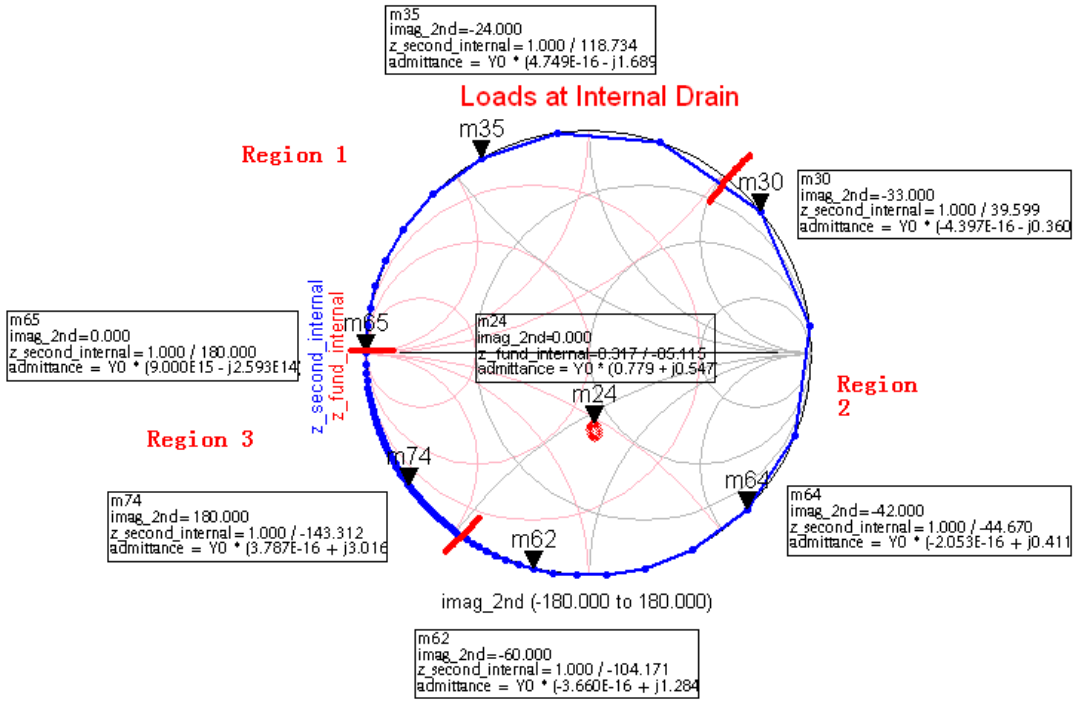


Figure Appendix 2.6 (b) Sweep the second harmonic load angle (in polar format) at 2.0 GHz The loads seen from internal drain plane (including both package parasitics and device parasitics) Red, blue represent fundamental and second harmonic load respectively

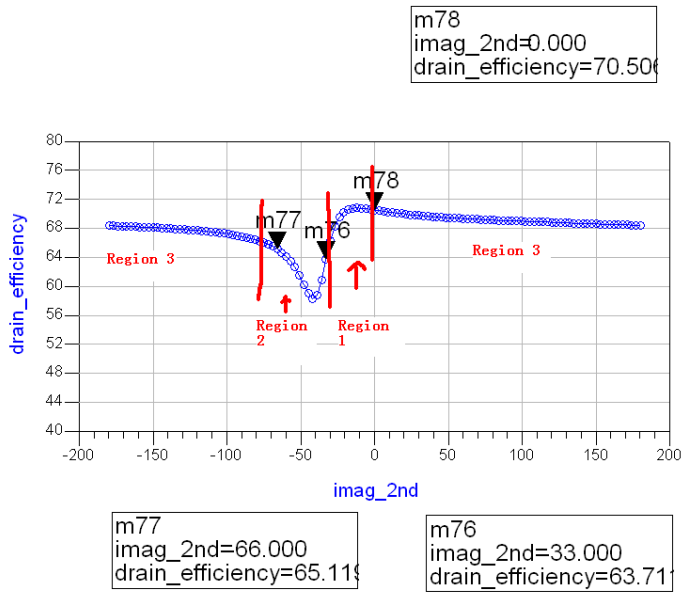


Figure Appendix 2.6 (c) Sweep the second harmonic load angle (in degrees) at 2.0 GHz

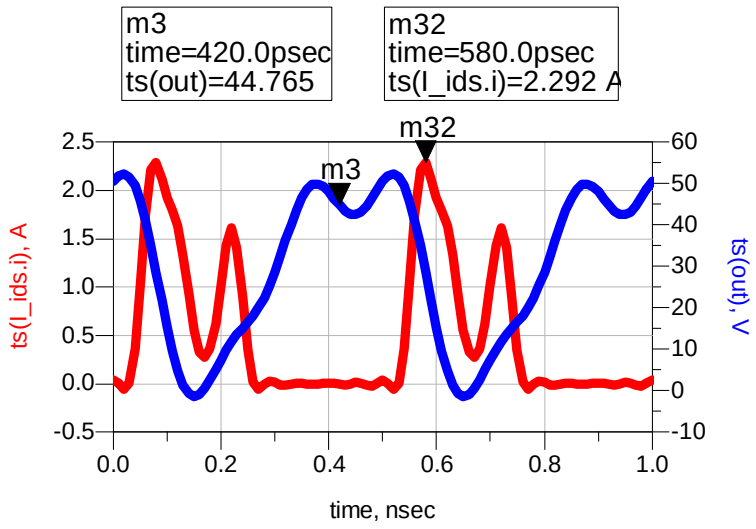


Figure Appendix 2.6 (d) Drain voltage (blue) and current (red) when the phase angle of 2nd harmonic load is-40 degrees at 2.0 GHz.

From figure appendix 2.6 (c), region 1 represent a region where the second harmonic load is capacitive and can positively affect the efficiency (see the fundamental in figure appendix 2.6 (b) and second harmonic load in region 1. They meet the requirement of the second solution for class-J operation). In region 2, the second harmonic load is almost open or have an inductive value (both the fundamental and 2nd harmonic load are inductive. This will cause that the peak of fundamental voltage waveform synchronizes the valley of 2nd harmonic voltage waveform and reduce the efficiency (figure appendix 2.6 (d))). When the second harmonic load angle (in polar format) is between -22 and 24 degrees, the drain efficiency is better. The corresponding reactance values are between -5.15 to 4.7 S when normalized to 30 Ohms. In our design, the reactance of second harmonic load is -5.85, which is in this region. The second harmonic has successfully improved the efficiency in this case. All the following discussions about the influence of 2nd or 3rd harmonic load phase angle are similar to the discussion here. So, we don't repeat them any more in our following discussion.

The same as did for second harmonic load, we fix the fundamental and second harmonic loads and sweep the third harmonic load angle (we ignore the loss of the third harmonic):

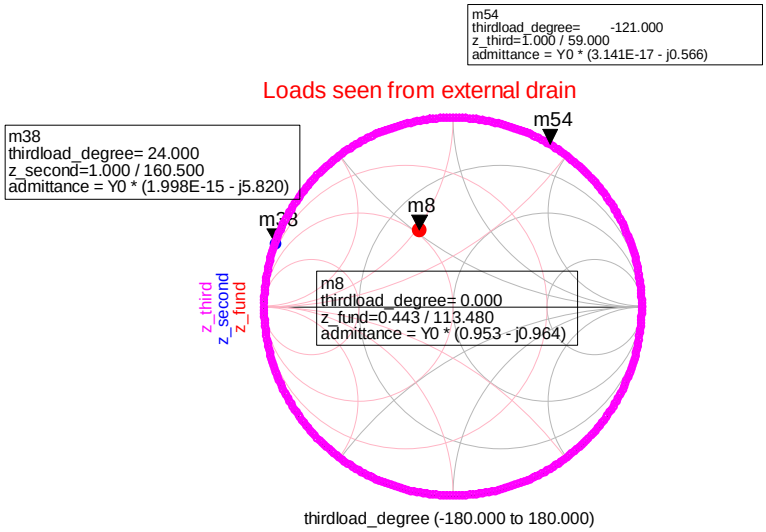


Figure Appendix 2.7 (a) Sweep the third harmonic load angle (in polar format) at 2.0 GHz The loads seen from external drain plane (including package parasitics and excluding device parasitics) Red, blue, pink represent fundamental, second harmonic and third harmonic load respectively

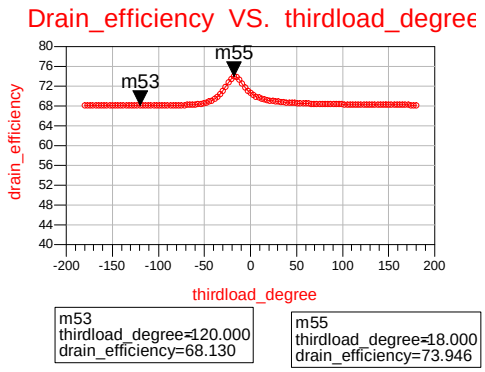


Figure Appendix 2.7 (b) Sweep the third second harmonic load angle (in degrees) at 2.0 GHz

In our design, the third harmonic load is -0.57 S when normalized to 30 Ohms. The corresponding degree in polar format is -121 degree (figure appendix 2.6 (a)). From figure appendix 2.6 (b) we know that, at -121 degrees, the third harmonic doesn't do any efficiency improvement.

So, for 2.0 GHz, the second harmonic load have a positive influence on the performance and the third harmonic don't have any influence.

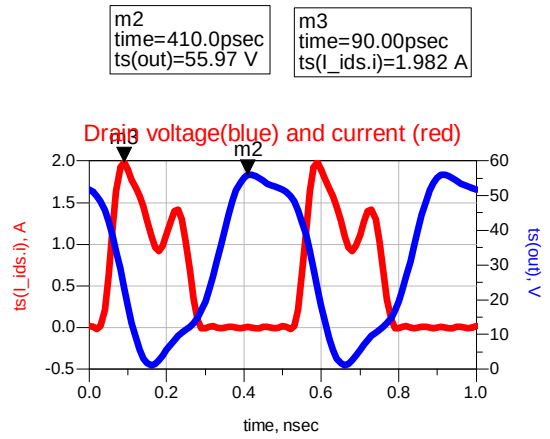


Figure Appendix 2.7 (c) Drain voltage (blue) vs. current (red) at 2.0 GHz

The situation is quite different at other frequency. For example, at 1.6 GHz, the second harmonic is almost shorted and the third harmonic has more influence on the performance.

We first fix the fundamental and third harmonic load and sweep the second harmonic load (figure 4.18):

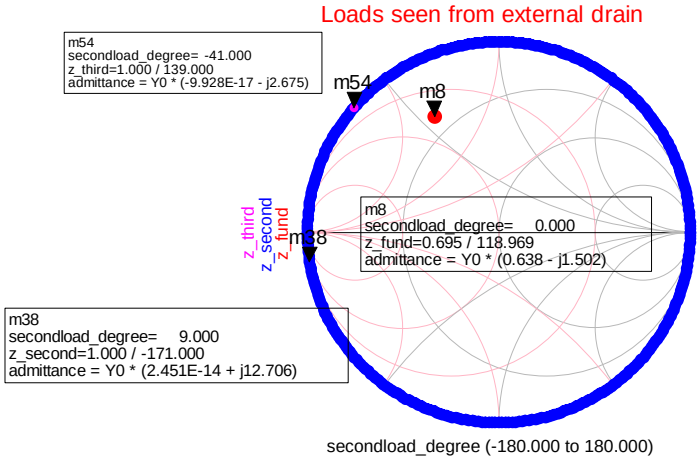


Figure Appendix 2.8 (a) Sweep the second harmonic load angle (in polar format) at 1.6 GHz The loads seen from external drain plane (including package parasitics and excluding device parasitics) Red, blue, pink represent fundamental, second harmonic and third harmonic load respectively

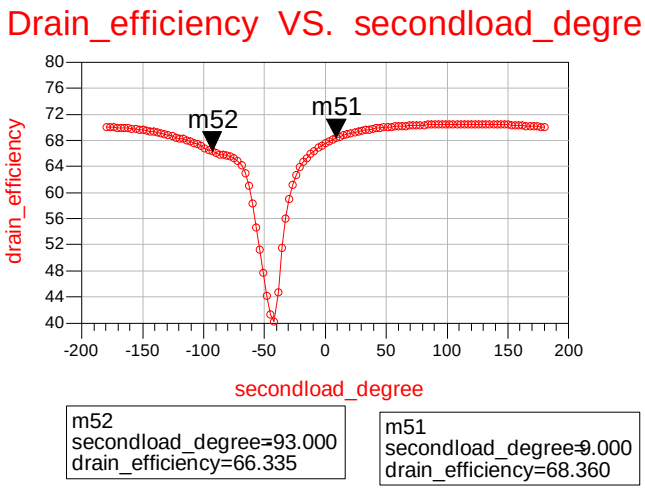


Figure Appendix 2.8 (b) Sweep the second harmonic load angle (in degrees) at 1.6 GHz

Then , we fix the fundamental and second harmonic load and sweep the third harmonic load (Figure Appendix 2.9):

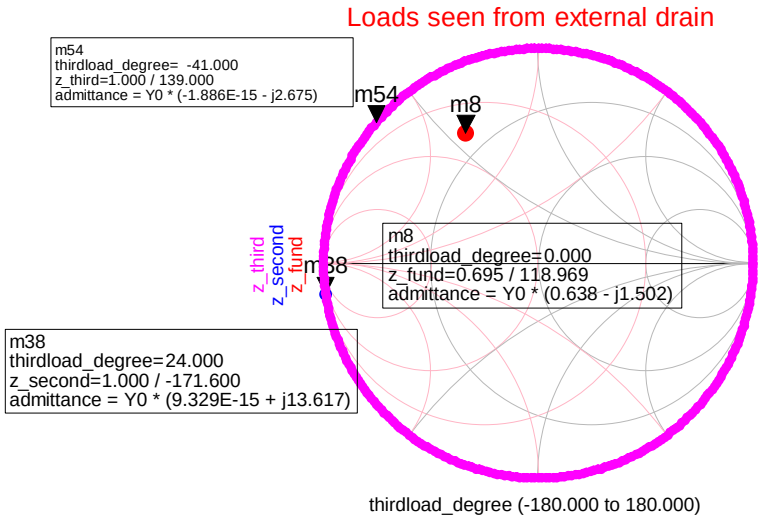


Figure Appendix 2.9 (a) Sweep the third harmonic load angle (in polar format) at 1.6 GHz The loads seen from external drain plane (including package parasitics and excluding device parasitics) Red, blue, pink represent fundamental, second harmonic and third harmonic load respectively

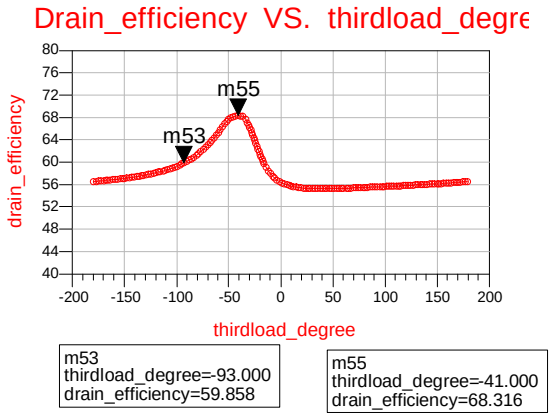


Figure Appendix 2.8 (b) Sweep the third harmonic load angle (in degrees) at 1.6 GHz

We can see that: when the angle of third harmonic load is -41 degrees (-2.67 S when normalized to 30 Ohms), we get an efficiency improvement. The second harmonic load don't improve the performance too much (figure 4.18).
The drain voltage and current waveforms and drain voltage spectrum are as follows:

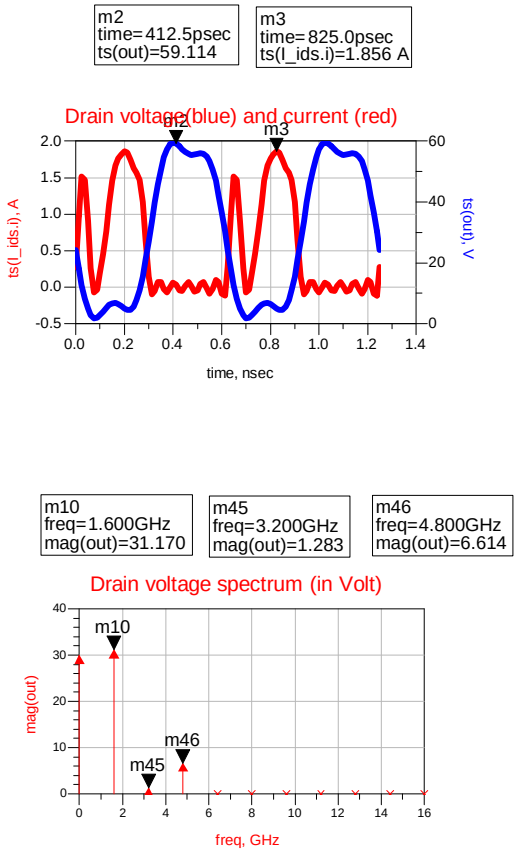


Figure Appendix 2.9 Drain voltage (blue) vs. current (red) and drain voltage spectrum at 1.6 GHz

The power amplifier is more like a sub-class-F power amplifier at 1.6 GHz.
The situations of power amplifier at other frequency are similar to the two examples shown above. So, initially we want to design a wideband class-J power amplifier, however, the power amplifier is more like a sub-class-F PA at some frequency. But, this doesn't deviate from our original purpose as long as we can improve the performance with harmonic tuning.

4. This version of wideband power amplifier is optimized for 30 V supply voltage. However, we still check the performance at power back-off point with a constant input power (24 dBm) (1.6GHz)

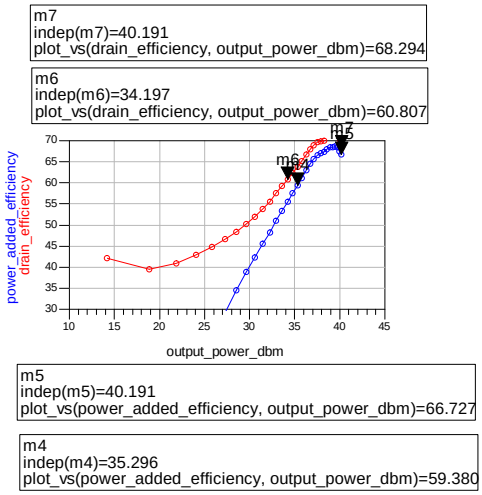


Figure Appendix 2.10 Drain efficiency and PAE versus output power (in dBm) at 1.6 GHz when varying the supply voltage. The power amplifier is over-driven at lower supply voltage

.

The power amplifier can only keep the efficiency higher than 60% at 5-5.5 dB power back-off point in over-drive condition. This performance is not very good because this design is just optimized for 30 V supply voltage.

Conclusion: we can get very good efficiency, output power and power gain performance at 30 V supply voltage over a bandwidth of 750 MHz. But, the performance at power back-off point is not very good. So, this design is just suitable for the situation that the supply voltage doesn't vary too much.

Appendix 3 A 600MHz Bandwidth Hybrid-class Power Amplifier Optimized for Supply Voltage Modulation

Simulation parameters:

1. Input is conjugate matched.
2. Frequency bandwidth: 1.55 to 2.15 GHz
3. Gate voltage: 2.25 V
4. Drain supply voltage: 1 to 30 V
5. Input power: input powers are chosen at 1 dB compression points for each supply voltage

The overall circuit and output matching network are as follows:

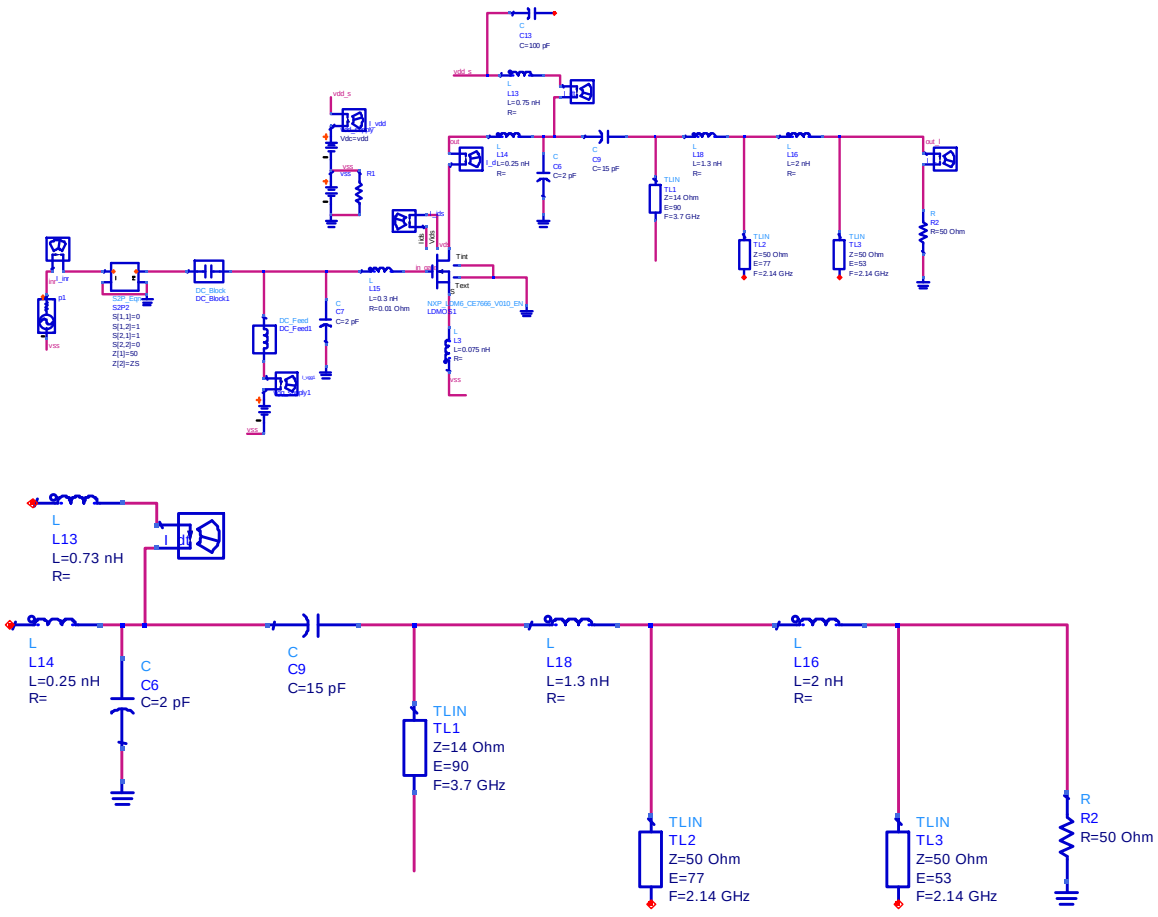


Figure appendix 3.1 Overall and output matching circuit of 600 MHz bandwidth hybrid class power amplifier.

The functionality of the components in the matching network are the same as that we discussed in chapter 4. The difference is that here we use an inductor to replace the series transmission line for simplicity. The load vs. frequency we get with this output matching network is given below (figure appendix 3.2):

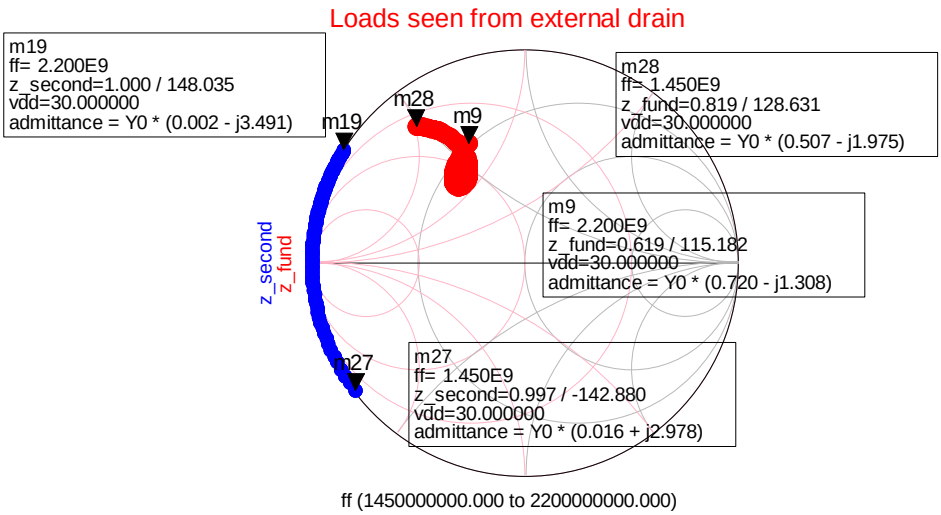


Figure appendix 3.2 The load vs. frequency as seen from external drain (this includes package parasitic but exclude the output capacitance of the device, Smith chart is normalized to 30 Ohms)

The loads seen from internal drain:

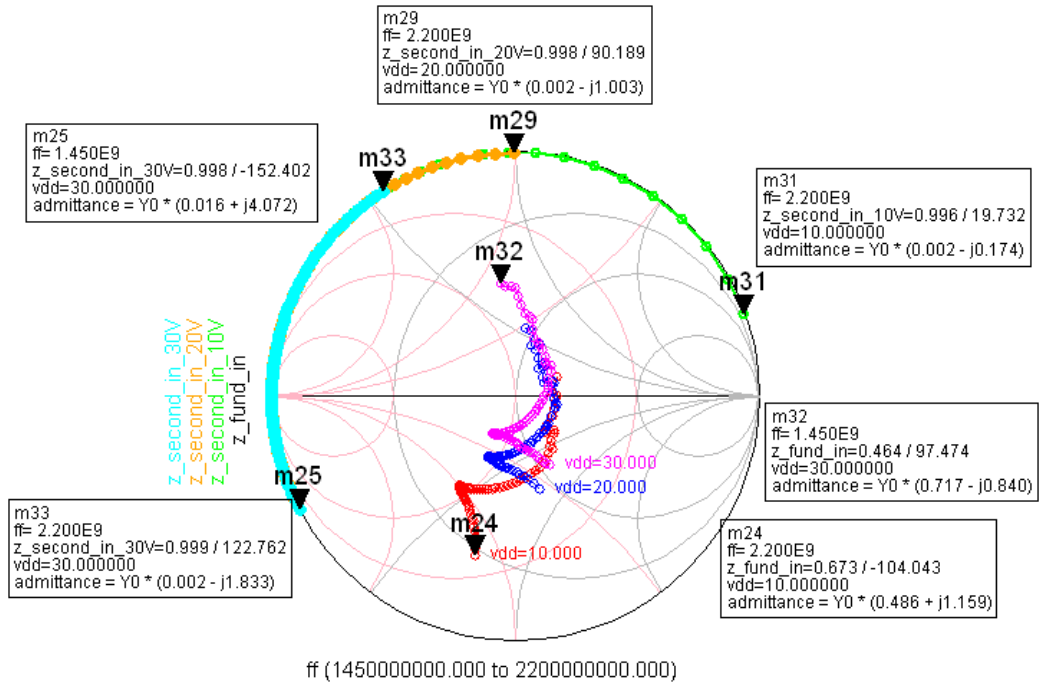
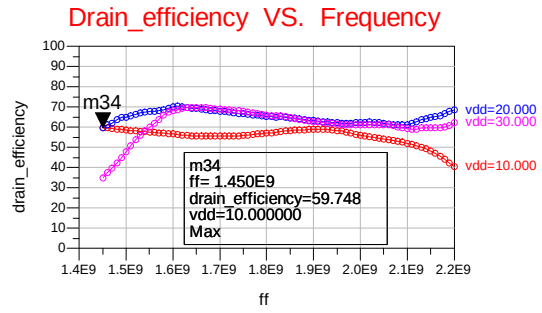
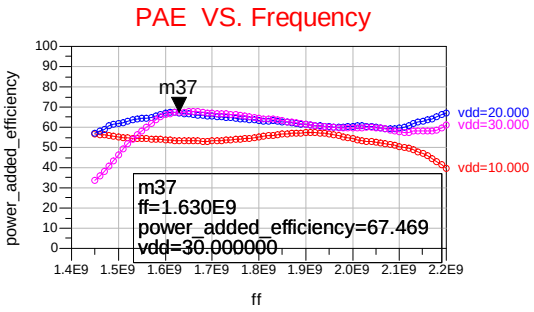


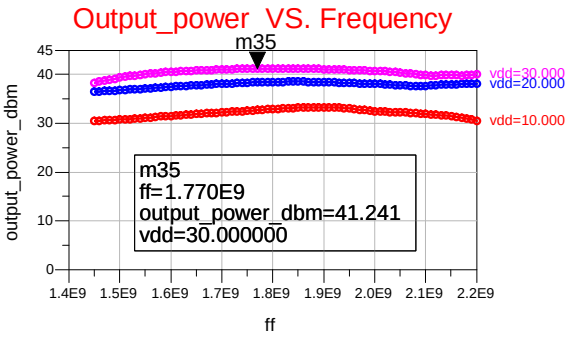
Figure appendix 3.3 Loads seen from internal drain plane (including both package parasitic and device parasitic, the Smith chart is normalized to 30 Ohms). Red, blue, pink symbol represents fundamental harmonic loads at 10 V, 20 V and 30 V supply voltage respectively (from 1.45 to 2.2 GHz). Light blue, brown, green symbol represents the second harmonic loads at 10 V, 20 V and 30 V supply voltage respectively (from 1.45 to 2.2 GHz).

From figure appendix 3.3, we can see some of the loads for fundamental and second harmonic meet are similar to the second solution of class-J operation (capacitive load for fundamental load and inductive second harmonic load) and some meet the first solution of class-J operation.

Now, we check the performance:







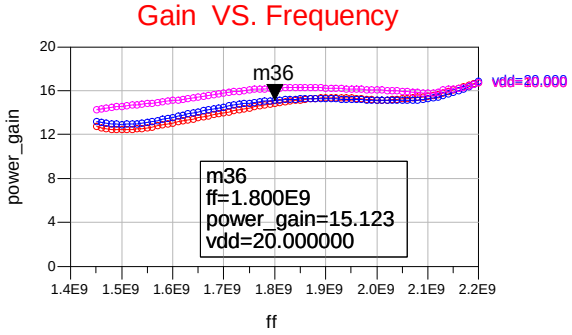


Figure appendix 3.4 The performance of a 600 MHz bandwidth hybrid class power amplifier The drain efficiency, output power (in dBm), PAE and power gain (in dBm) performance versus Frequency are shown in this graph. Red, blue, pink line represents the performance at 10 V, 20V, 30V supply voltage respectively.

We can see the performance between 1.9 GHz and 2.1 GHz is the best. When the frequency increases or decreases the achieved performance becomes worse. We can conclude these results as follows:

1. Between 10 and 30 V supply voltage, the drain efficiency is around 55%-60% for most of the frequency except at the edge of bandwidth.
2. PAE is around 3% lower than drain efficiency. We bias all the input powers for different supply voltages below 1 dB compression point. So, the PAE is almost the same as drain efficiency.
3. For most frequencies, the power amplifier reaches the peak output power (40.7 dBm with 25.5 dBm input power). We can increase the input power if it doesn't reach the peak power.
4. The power gain for 10 to30 V supply voltage is around 15-16 dB. We don't over-drive the power amplifier at lower supply voltage. So, the power remains constant for all supply voltages.
5. We can check the performance at power back-off point at some frequency. We choose one frequency at the middle of the band and one at the edge of the band---1.95 and 2.2 GHz.
   Power back-off performance at 1.95 GHz (figure appendix 3.5):

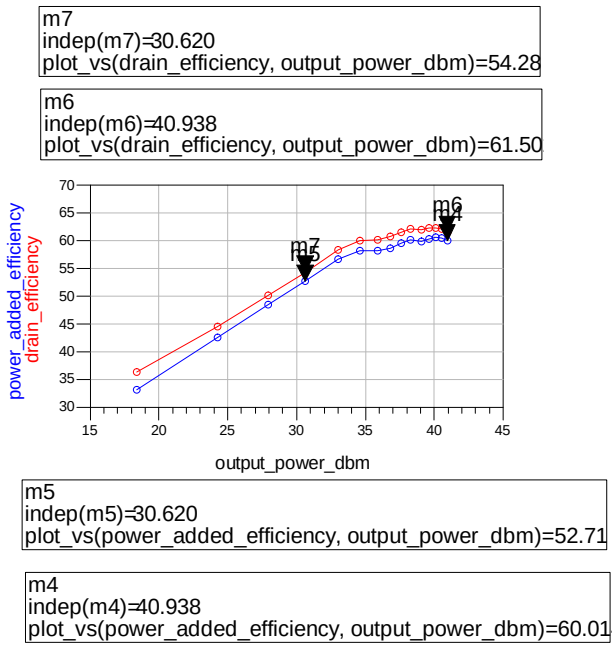


Figure appendix 3.5 Performance of 1.95 GHz frequency at power back off point. Red, blue represents drain efficiency and PAE versus frequency respectively.

So, at 1.95 GHz, the power amplifier can keep the drain efficiency and PAE higher than 55% over a 8.5-9.5 dB power back-off point.
Power back-off performance at 2.2 GHz (figure appendix 3.6):

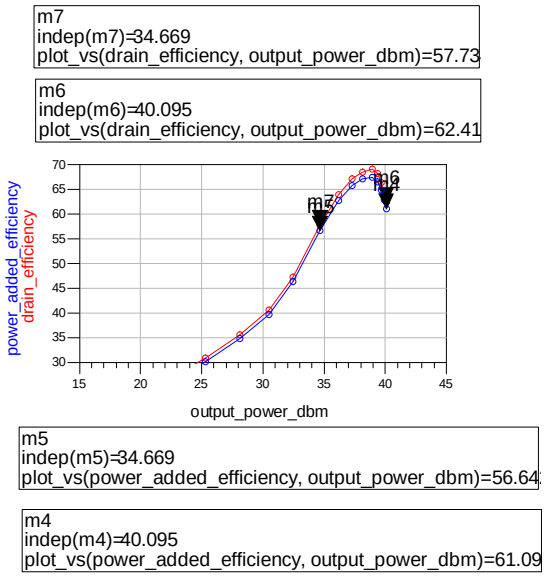


Figure appendix 3.6 Performance at 2.2 GHz frequency versus power back off. The red and blue curves represents drain efficiency and PAE versus output power (in dBm) respectively.

At 2.2 GHz (the edge of bandwidth), the performance at power back-off point is much worse than that at 1.95 GHz (central of the bandwidth). The power amplifier can only keep its efficiency higher than 55% over a 5 to 6 dB power back-off range.

6. Next we check the operation class of the wideband power amplifier:
Load of fundamental and harmonic at 1.95 GHz operating at 10 V supply voltage

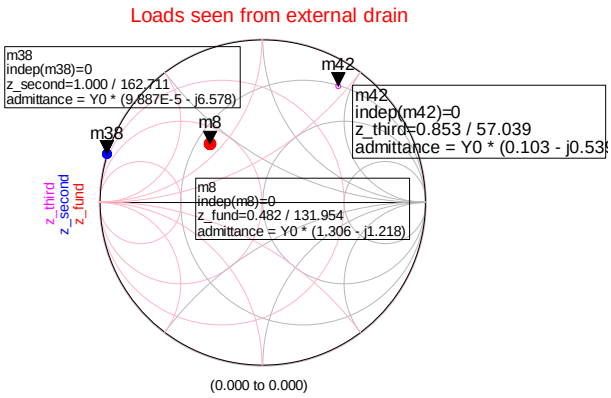


Figure appendix 3.7 (a) The loads at 1.95 GHz frequency seen from external drain (normalized to 30 Ohms). Red, blue, pink represents fundamental, second harmonic and third

harmonic load

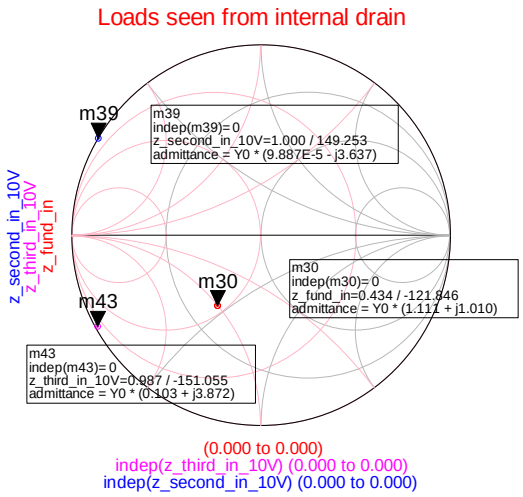


Figure appendix 3.7 (b) The loads at 1.95 GHz frequency seen from internal drain (normalized to 30 Ohms) Red, blue, pink represents fundamental, second harmonic and third harmonic load

Drain voltage and current waveform at 1.95 GHz and 10 V supply voltage:

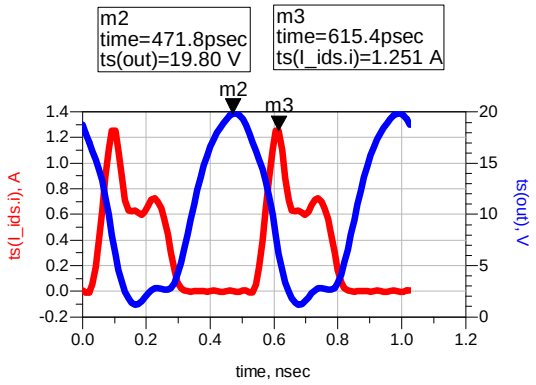


Figure appendix 3.8 Drain voltage and current waveform at 1.95 GHz and 10 V supply voltage. Blue and red represents drain voltage and current respectively

The drain voltage waveform is very close to the second waveform solution of class-J operation (see chapter 2). For other frequency and supply voltage, we can do the same analysis.

7. We can check the influence of second and third harmonic load as we did in chapter 4 and appendix 2. We don't repeat the process here. The results show that at some frequency region, the second harmonic can improve the efficiency at power back-off slightly. For other frequency region, the influence of second harmonic is small.

Appendix 4 Hybrid-Class Power Amplifier Realized with 2W LDMOS

The specifications of 2 W LDMOS:
1. Channel length: 300 um
2. Cell pitch: 90 um
3. Cells: 3

The estimated drain parasitic capacitance and conductance:

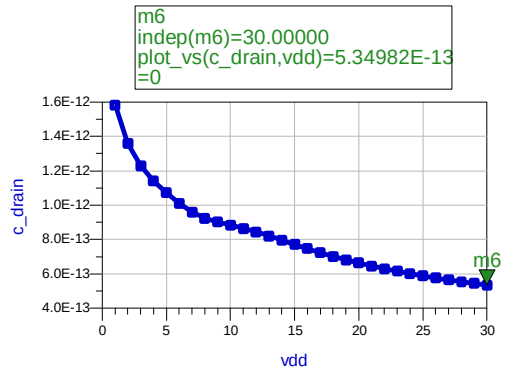


Figure appendix 4.1 Output capacitance of 2 W LDMOS vs. supply voltage (in volts)

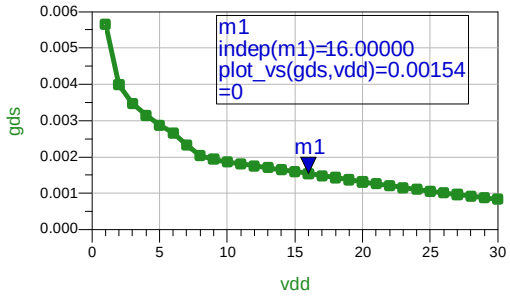


Figure appendix 4.2 Drain parasitic conductance of 2 W LDMOS vs. supply voltage (in volts)

Comparing with figure 3.3 and 3.6 in chapter 3, we find that the parasitic capacitance and conductance are much smaller than that of 12 W LDMOS.

The performance of class-AB and hybrid-class power amplifier realized with 2W LDMOS at 2.14 GHz:

Simulation parameters:
1. Input is conjugate matched.
2. Frequency : 2.14 GHz
3. Input power: the input powers are chosen at 1dB compression point for each

supply volage

4. The fundamental loads are optimized for 30 V supply voltage and second harmonic load is optimized for 5V supply voltage.

Performances:

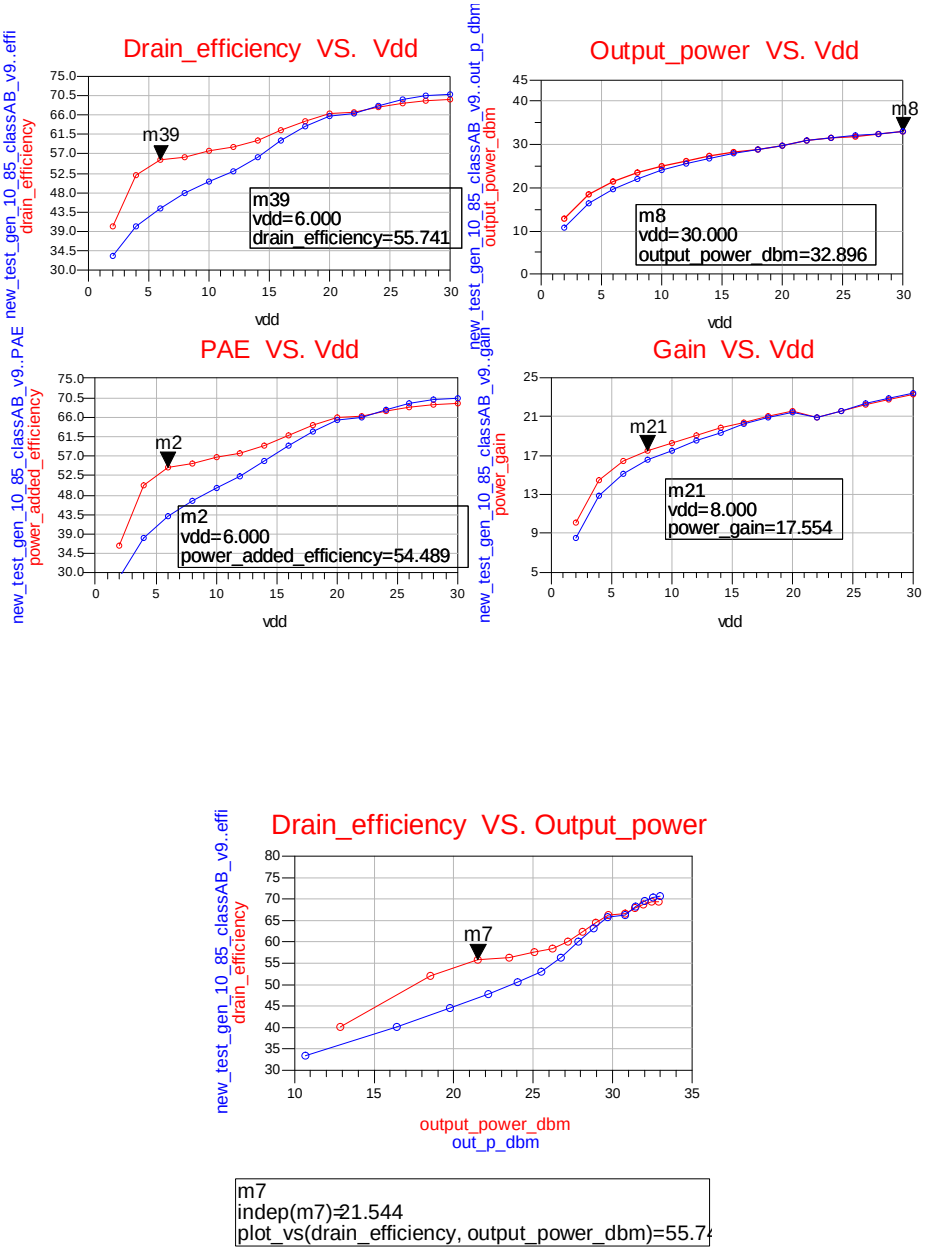


Figure appendix 4.3 Performances of class-AB (blue) and hybrid-class (red) power amplifier realized with 2W LDMOS.

The improvement of efficiency at power back-off is more obvious compared with 12 W LDMOS. This proves that class-J operation needs a device with relative small

parasitics.

If we use a constant input power (1 dB compression point at 30 V supply voltage. Over-drive the PA at lower supply voltage), the difference of these two classes becomes more obvious:

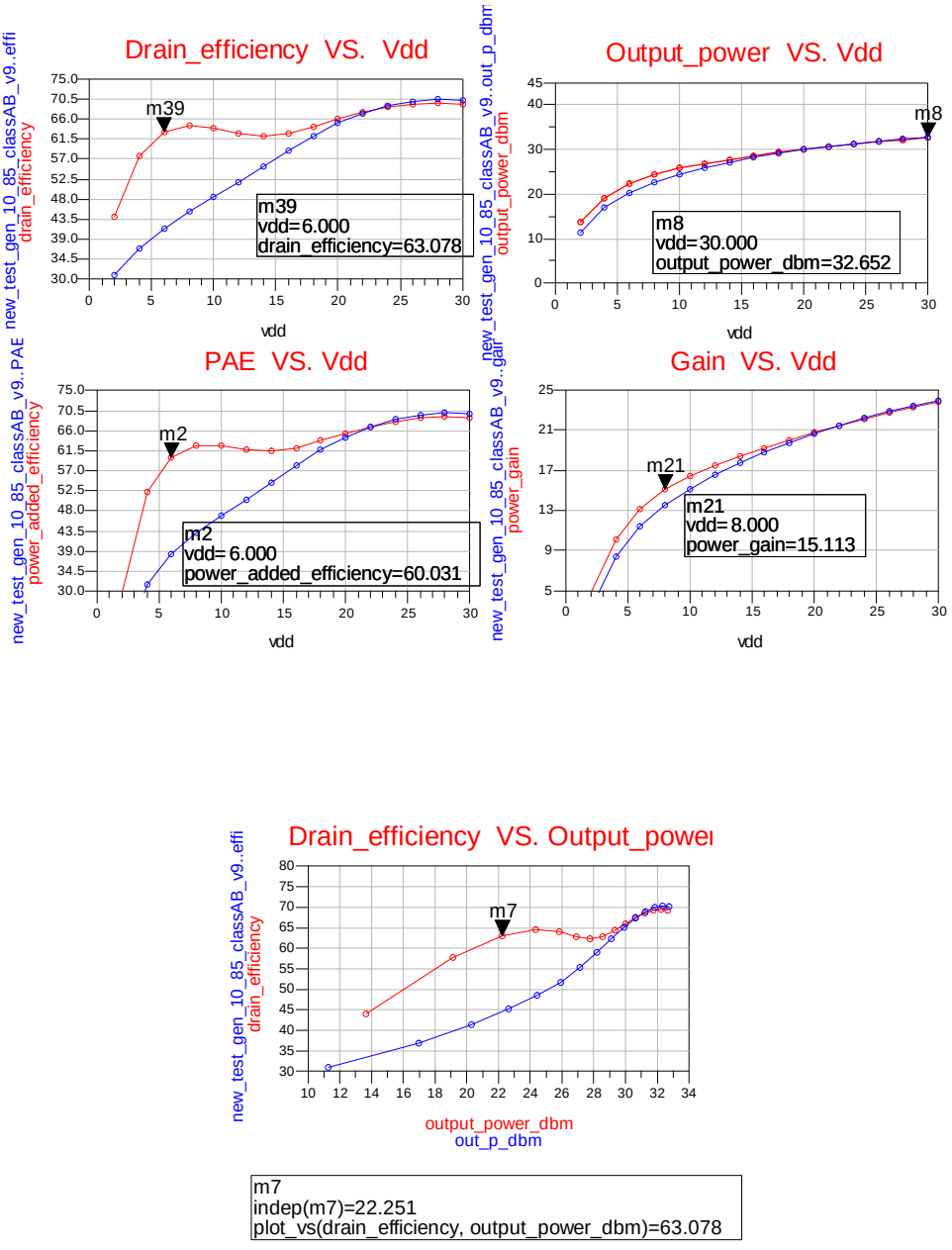


Figure appendix 4.4 Performances of class-AB (blue) and hybrid-class (red) power amplifier realized with 2W LDMOS under over-drive condition.

Under over-drive condition, hybrid-class can deliver more power than class-AB. This is the reason why the efficiency improvement is bigger under over-drive condition.

Bibliography

[1] S. C. Cripps," RF Power amplifier for wireless communication", 2nd ed, 2006.

[2] Frederick H. Raab, "Idealized Operation of the Class E Tuned Power Amplifier". IEE Transactions on Circuits and Systems, VOL.CAS-24, no.12, pp.725-735, December 1977.

[3] Frederick H. Raab, "Class-E, Class-C, and Class-F power amplifiers Based Upon a Finite Number of Harmonics". IEEE Transactions on Microwave Theory and Techniques, VOL.49, NO.8, pp.1462-1468, August 2001.

[4] Timo Rautio, Henri Harju, Simo Hietakangas and Timo Rahkonen, "Effects of Different VDD- drives in ET and EER transmitters". In Norchip, 2007, pages 1-4, 19-20 Nov. 2007

[5] Ildu Kim, Yong Yun Woo, Jangheon Kim, Junghwan Moon, Jungjoon Kim and Bumman Kim. "High-Efficiency Hybrid EER transmitter Using optimized Power Amplifier". IEEE Transactions on Microwave Theory and Techniques, VOL.56, No.11, November 2008.

[6] S.M.lavi, M.Marchetti, L.C.N.de.Vreede, Fred van Rijs. "High-Efficiency Envelope Tracking operation through Second Harmonic Manipulation"

[7] Frederick H. Raab, Peter Asbeck, Steve Cripps, Peter B. Kenington, Zoya B.Popovic, Nick Pothecary, John F.Sevic, Nathan O.Sokal. "Power Amplifiers and Transmitters for RF and Microwave". IEEE Transactions on Microwave Theory and Techniques, VOL.50, No.3, pp.814-826, March 2002.

[8] Donald F. Kimball, Jinho Jeong, Chin Hsia, Paul Draxler, Sandro Lanfranco, Walter Nagy, Kevin Linthicum, Lawrence E.Larson and Peter M.Asbeck. "High-Effienciency Envelope-Tracking W-CDMA Base-Station Amplifier Using GaN HFETs". IEEE Transactions on Microwave Theory and Techniques, VOL.54, No.11, pp.3848-3856, November 2006.

[9] Andrew J. Wilkinson and Jeremy K.A.Everard, "Transmission-Line Load-Network Topology for Class-E Power Amplifiers". IEEE Transactions on Microwave Theory and Techniques, VOL.49, No.6, pp.1202-1210, June 2001

[10] Peter Wright, J.Lees, P.J.Tasker, J.Benedikt and Steve C.Cripps. "An Efficient, Linear, Broadband Class-J-Mode PA Realised Using RF Waveform Engineering".