CMOS circuits and systems for cryogenic control of silicon quantum processors

Patra, B

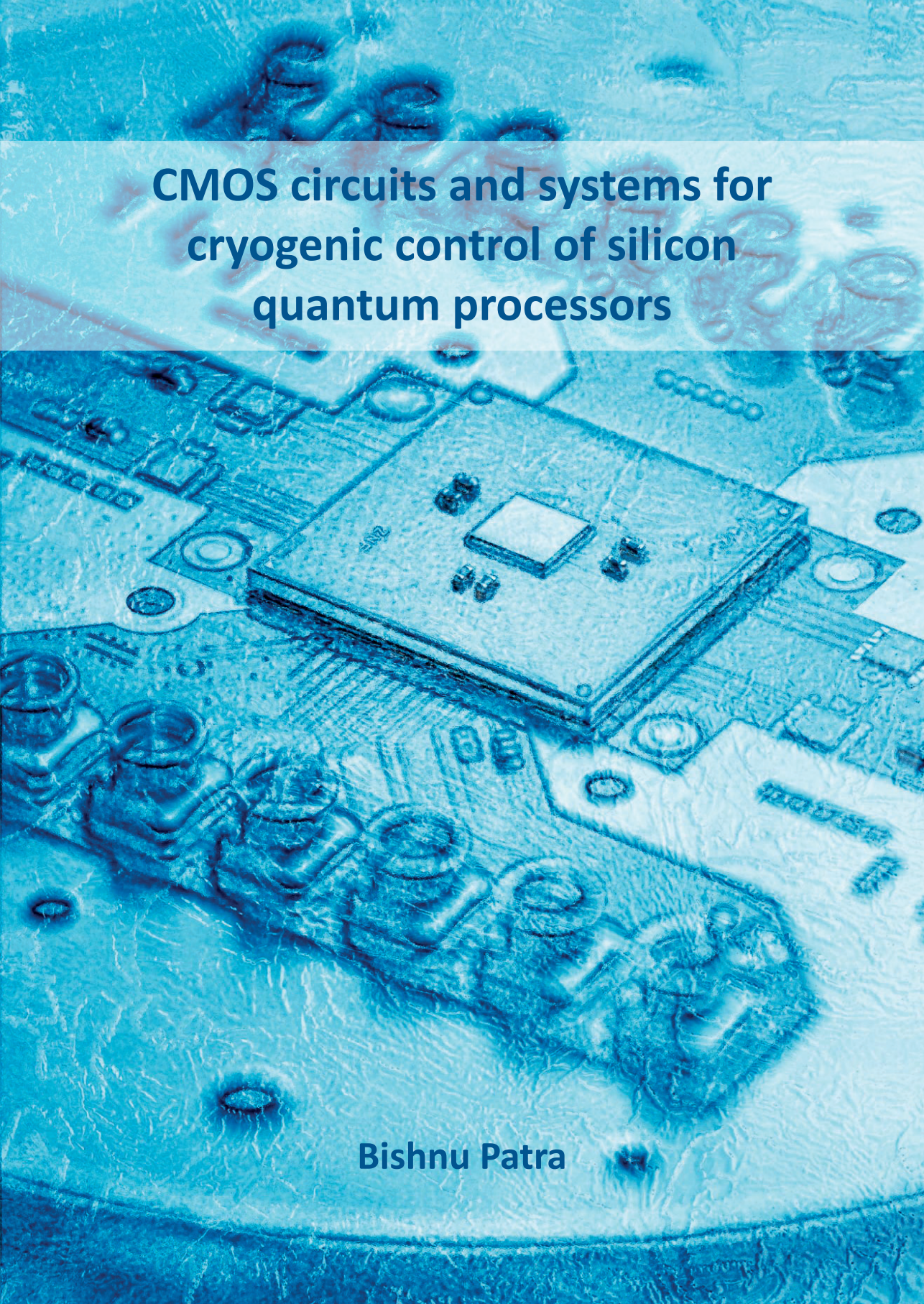
DOI
10.4233/uuid:cea59727-fda2-41e1-ba87-9404ef22202d

Publication date
2021

Document Version
Final published version

Citation (APA)
Patra, B. (2021). *CMOS circuits and systems for cryogenic control of silicon quantum processors*. [Dissertation (TU Delft), Delft University of Technology]. https://doi.org/10.4233/uuid:cea59727-fda2-41e1-ba87-9404ef22202d

CMOS circuits and systems for cryogenic control of silicon quantum processors



Bishnu Patra

CMOS circuits and systems for cryogenic control of silicon quantum processors

CMOS circuits and systems for cryogenic control of silicon quantum processors

Dissertation

for the purpose of obtaining the degree of doctor
at Delft University of Technology,
by the authority of the Rector Magnificus Prof.dr.ir. T.H.J.J. van der Hagen,
chair of the Board for Doctorates,
to be defended publicly on
Monday 22 November 2021 at 15:00

by

Bishnu Prasad PATRA

Master of Science in Electrical Engineering,
Delft University of Technology, the Netherlands
born in Rourkela, India.

This dissertation has been approved by

Promotor: Prof.dr.ir. E. Charbon
Copromotor: Dr. M. Babaie

Composition of the doctoral committee:

Rector Magnificus,	Chairperson
Prof.dr.ir. E. Charbon	Delft University of Technology, Promotor
Dr. M. Babaie	Delft University of Technology, Copromotor
Independent members:	
Prof.dr.ir. L.M.K. Vandersypen	Delft University of Technology
Prof.dr. D.P. DiVincenzo	Forschungszentrum Jülich, Germany
Prof.dr.ir. B. Nauta	University of Twente
Prof. J.J.L. Morton	University College London, United Kingdom
Dr. J. Craninckx	IMEC, Leuven, Belgium
Prof.dr. K.A.A. Makinwa	Delft University of Technology, reserve member

Keywords: Cryogenic electronics, Cryo-CMOS integrated circuits, quantum computing, microwave passive components, cryogenic device modeling, oscillators, controller specifications, wideband RF front-end, scalable qubit controller, spin qubits, fidelity, quantum algorithm.

Printed by: Gildeprint

Cover Photo: Marieke de Lorijn.

Casimir PhD Series, Delft-Leiden 2021-36

ISBN 978-90-8593-501-8

An electronic version of this dissertation is available at
http://repository.tudelft.nl/.

When you have exhausted all possibilities,
remember this: you haven't.

Thomas Edison

Contents

Summary **xi**

1 Introduction **1**
1.1 The pursuit of scalability . . . 2
1.1.1 Superconducting qubits . . . 2
1.1.2 Spin qubits . . . 2
1.2 Motivation of this work . . . 3
1.3 Scope of this work . . . 5
1.4 Organization of the dissertation . . . 5
1.5 Original contributions . . . 7

2 Cryogenic passive devices and impact on RFIC design **9**
2.1 Introduction . . . 10
2.2 Cryo-CMOS devices . . . 10
2.2.1 Active devices . . . 10
2.2.2 Passive devices . . . 12
2.3 Test structures and measurement setup . . . 13
2.4 MoM capacitance . . . 15
2.5 Inductance . . . 17
2.5.1 Lumped element model . . . 20
2.5.2 EM model . . . 22
2.6 Impact on RFICs . . . 22
2.7 Conclusion . . . 26

3 Cryogenic RF oscillator: Characterization and analysis **27**
3.1 Introduction . . . 28
3.2 Specifications . . . 28
3.2.1 Impact of cryogenic operation . . . 29
3.3 Digitally Controlled Oscillator . . . 30
3.4 Conclusion . . . 37

4 System-level modeling of a single-qubit gate controller **39**
4.1 Introduction . . . 40
4.2 Control Signal specifications . . . 40
4.2.1 Basics of spin qubit control . . . 40
4.2.2 System requirements . . . 42
4.2.3 Signal specifications . . . 44

4.3 System Architecture Evolution . . . 46
4.3.1 Analog/RF Section . . . 46
4.3.2 Digital Signal Synthesis . . . 49
4.3.3 Final Architecture . . . 50
4.3.4 System simulation . . . 51
4.4 Circuit Specifications . . . 51
4.4.1 Sampling rate . . . 52
4.4.2 Numerically Controlled Oscillator . . . 52
4.4.3 NCO phase truncation . . . 53
4.4.4 LUT number of bits . . . 54
4.4.5 Envelope memory . . . 55
4.4.6 Digital correction network . . . 56
4.4.7 Complete digital system . . . 57
4.4.8 Power consumption estimate . . . 58
4.5 Conclusion . . . 59

5 Cryogenic controller: Design and Characterization 61
5.1 Introduction . . . 62
5.2 Design Challenges . . . 62
5.3 Reference clock and power consumption . . . 64
5.3.1 Reference clock specifications . . . 64
5.3.2 Power consumption estimate of the RF front-end . . . 65
5.4 Digital circuit design . . . 66
5.5 RF front-end . . . 69
5.5.1 Mixer . . . 70
5.5.2 Output driver . . . 72
5.5.3 Auxiliary circuits . . . 75
5.6 Cryogenic Electrical Performance . . . 78
5.6.1 Measurement setup . . . 81
5.6.2 Electrical characterization . . . 81
5.6.3 Quality of modulation . . . 87
5.6.4 Comparison with state-of-the-art . . . 89
5.7 Conclusion . . . 89
5.7.1 Future improvements . . . 91

6 Cryogenic control of a two-qubit processor 93
6.1 Introduction . . . 94
6.2 Interfacing the cryo-controller with qubits . . . 94
6.3 The quantum processor . . . 96
6.3.1 Si/SiGe heterostructure . . . 96
6.3.2 Quantum dot device fabrication . . . 97
6.3.3 Micro-magnet . . . 97

6.4 Qubit control and readout mechanism . . . 99
6.4.1 Pulsing scheme for qubit experiments . . . 99
6.4.2 Qubit control . . . 100
6.4.3 Qubit readout . . . 100
6.4.4 Electron temperature . . . 101
6.5 Calibration of pulses . . . 102
6.5.1 Finding the qubit resonance frequency . . . 102
6.5.2 Rabi oscillation . . . 103
6.5.3 Ramsey experiment . . . 103
6.5.4 AllXY . . . 105
6.5.5 Calibration Routine . . . 106
6.6 Single qubit experiments . . . 106
6.6.1 Ramsey-style experiment . . . 107
6.6.2 Crosstalk in FDMA . . . 107
6.6.3 Pulse shaping . . . 109
6.6.4 Characterizing the unintended Z-rotation . . . 109
6.6.5 Quantum-State Tomography . . . 110
6.6.6 Randomized Benchmarking . . . 111
6.6.7 Simultaneous Rabi . . . 112
6.7 Two-qubit experiments . . . 112
6.7.1 Gate definition in coupled regime . . . 113
6.7.2 Deutsch-Jozsa Algorithm . . . 115
6.8 Conclusion . . . 116

7 Conclusion 117
7.1 Thesis outcome . . . 117
7.2 Outlook . . . 119

Bibliography 123

Acknowledgements 137

List of Publications 141

About the author 145

Summary

Quantum computers can provide exponential speedup in solving certain computational problems pertaining to drug discovery, cybersecurity, weather forecasting, etc. Although a quantum computer with just 50-qubits has been shown to surpass the computing power of the best supercomputers in specific applications, millions of qubits would be required for useful practical applications. One of the biggest obstacles in scaling from 50 qubits to millions of qubits is the interconnect bottleneck between solid-state qubits operating at 20 milliKelvin inside a dilution refrigerator and control electronics outside the dilution refrigerator connected via long coaxial cables. A 50-qubit processor requires hundreds of cables, digital to analog converters, mixers and amplifiers, clearly challenging the scalability of the system. The goal of this research is to build scalable quantum computers by operating CMOS control electronics inside the dilution refrigerator in proximity to quantum processors. The dissertation covers a broad aspect of cryogenic integrated circuit design spanning across devices, circuits and systems.

Due to the limited cooling power of the dilution refrigerator, integrated circuits operating at cryogenic temperatures should consume very low power. The design of power-efficient integrated circuits requires accurate device models, which are only valid in the standard military temperature range down to -55 Celsius (218 Kelvin). Several on-chip microwave passive devices were characterized in a cryogenic probe station at 4 Kelvin operating at frequencies up to 30 GHz. Lumped-element models and electromagnetic models of these devices were developed compatible with standard circuit simulators to accurately predict the behavior of cryogenic integrated circuits. Consequently, standard CAD tools can be used to simulate integrated circuits such as oscillators and low noise amplifiers, operating down to 4 Kelvin. A cryogenic radio frequency oscillator operating at 4 Kelvin was characterized to validate the effectiveness of the cryogenic models.

The design of cryogenic qubit controllers is challenging due to the lack of concrete signal specifications and limited power dissipation allowed in dilution refrigerators. Accurate modeling of the qubit controllers and qubit gate operations is essential to build circuits for high-fidelity control. It would enable the design of application-specific integrated circuits with low power dissipation. We co-simulated a Hamiltonian-based model of the quantum processor and a behavioral model of a microwave signal generator to obtain specifications for the accuracy and tolerable noise of the signals for high-fidelity qubit control. Furthermore, we used these specifications to derive the circuit specifications of a direct digital synthesizer based wideband multi-qubit controller.

The developed system architecture was designed and fabricated in Intel 22nm FinFET technology named 'Horse Ridge'. The chip constituted a direct digital synthesizer back-end and a radio frequency front-end to generate signals in the frequency

range of 2 to 20 GHz while meeting the stringent signal-to-noise ratio and spurious-free dynamic range required for qubit control. The chip could control multiple qubits over the same channel using frequency multiplexing and targeted for both spin qubits and transmons. This chip with an area of 16 square millimeters can control up to 128 qubits while operating at 4 Kelvin inside a dilution refrigerator.

We evaluated the performance of the chip in controlling spin qubits compared to room temperature control electronics by conducting extensive experiments including electron temperature measurement, randomized benchmarking, quantum state tomography and Deutsch-Jozsa quantum algorithm, all implemented for the first time using a cryogenic integrated circuit. The comparable gate fidelity obtained with the cryo-controller proves the effectiveness of cryogenic integrated circuits in addressing the interconnect bottleneck to build large-scale quantum computers.

1

Introduction

In classical computing, the basic unit of information i.e. *bit* (originates from **bi**nary digi**t**) can store 0 *or* 1. However, in a quantum computer, the fundamental computation unit i.e. a *qubit* (**qu**antum **bit**) can attain 0 *and* 1 state at the same time, thus allowing parallelism thanks to the superposition property of qubits [1]. This allows an N-qubit computer to encode 2^N bits of information simultaneously, compared to N bits of information in an N-bit classical computer.

Another property of qubits that is different from classical bits is entanglement or the inseparability of the state of two or more qubits [2]. Usually the classical bits are uncoupled and isolated from each other since coupling could *adversely* affect the state of one bit due to unwanted noise from the other bits. However, when two qubits are coupled or entangled their behaviors are correlated i.e. any variation in the state of one qubit affects the state of another qubit *predictably*. A quantum algorithm leverages such distinctive properties of qubits i.e. superposition and entanglement, to achieve exponential speed-up over classical computers in certain computations.

Short-term applications of a quantum computer include quantum chemistry, where the electronic structure of molecular orbitals can be mapped onto a quantum processor to simulate the interaction between molecules. As a result, new molecules and reactions can be designed, and industrial chemical processes can be optimized [3]. Similarly, the process of biological nitrogen fixation in plants enzyme nitrogenase (FeMo cofactor) could be simulated using a quantum computer [4].

The computing power of a quantum computer is directly related to the quality and *quantity* of its qubits. Although a quantum computer with only 53 qubits has surpassed the capability of even the most powerful supercomputers [5], for such practical applications, large-scale quantum computers with thousands – or even millions – of qubits would be required. This demands a scalable architecture for the implementation of qubits as well as the control electronics, the two building blocks of a quantum computer.

1

1.1. The pursuit of scalability

Although qubits' physical implementation started with trapped ions [6] and bulk nuclear magnetic resonance (NMR) [7], it was soon realized that a scalable qubit architecture is required to realize quantum computers with hundreds of qubits. The demonstration of quantum effects in solid-state qubit technologies, such as superconducting qubit [8] paved the way towards a scalable architecture not because of their form factor but mostly because they could leverage the semiconductor fabrication process, thus facilitating scalability. These qubits are leading the way since then [5]. In a parallel path, demonstration of quantum dots in silicon allowed the development of qubits using spins of a single electron [9] or hole [10].

1.1.1. Superconducting qubits

Quantum properties can be observed in subatomic particles such as electrons. However, one can replicate this quantum behavior by designing an artificial atom, as in the case of superconducting qubits [8], which employ a macroscopic number of paired electrons known as Cooper pairs, to form a single collective ground state. Superconducting electrical circuits exhibit quantum behavior with energy levels set by their geometric parameters. A lossless superconducting qubit with discrete energy states can be formed using the energy level of non-dissipative elements i.e. an inductor and capacitor. However, if both elements are linear, it would behave as a harmonic oscillator owing to evenly spaced energy levels. To create a non-uniform separation between the energy levels, a non-linear non-dissipative inductor i.e. a Josephson junction is used along with a capacitor to form a tank. The bottom energy levels are used as state 0 and 1 and the higher energy level transitions are avoided. The qubit states are manipulated by applying a microwave pulse corresponding to the resonance frequency of the qubit. Similarly, the qubit states are read out by probing a state-dependent phase shift in the applied microwave pulse. These qubits need to operate at cryogenic temperatures around $\sim 10\,\mathrm{mK}$, achieved inside a dilution refrigerator. This temperature is necessary to operate the Josephson junction correctly and thus to ensure the quantum properties of the qubit.

1.1.2. Spin qubits

In contrast to superconducting qubits where an artificial atom is built, spin qubits encode the information in the spin of a single electron. The application of an external magnetic field to a single electron confined in a quantum dot splits the spin states by the Zeeman energy, forming a natural two-level quantum system [9]. These qubits can be fabricated in a Si/SiGe heterostructure [11] or Silicon Metal-Oxide-Semiconductor [12] using lithography, similar to the one used in commercial CMOS electronics. The qubit states are manipulated by applying a microwave pulse with a frequency corresponding to the Zeeman energy. The states can be read out using spin-to–to-charge conversion either by spin-selective tunneling between a dot and the reservoir [13] or by Pauli spin blockade [14]. These qubits also need to operate at cryogenic temperatures, however, the temperature range in which they operate is larger, reaching up to $5\,\mathrm{K}$ [15, 16, 17].

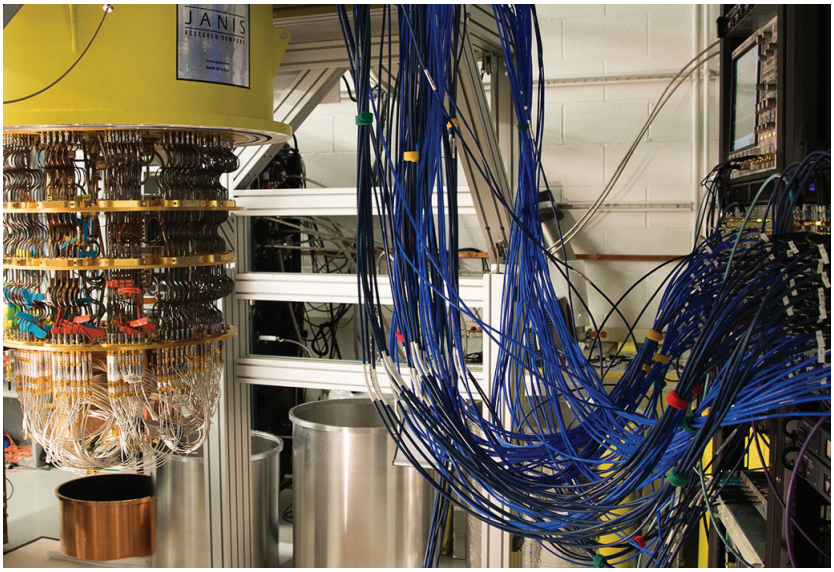


Figure 1.1: State-of-the-art quantum computer with 72 superconducting qubits [5].

1.2. Motivation of this work

Similar to the scalability of qubits, it is essential to implement a scalable architecture for control electronics. Qubits typically operate inside a dilution refrigerator, while the control electronics is implemented with off-the-shelf equipment operating at room temperature (RT) and connected via at least a single RF cable per qubit.

Such control setups hinder scalability both because of the excessive complexity of an equipment-based control and because it is impractical to fit thousands of cables inside a dilution refrigerator while minimizing the heat load in the fridge and ensuring the reliability of the interconnects. The most complex state-of-the-art quantum computer (with 72 qubits) requires tens of bulky custom-made electronic modules (DAC, LNA, ADC, etc.) operating at RT and connected to cryogenic qubits via 168 long and lossy coaxial cables [5], as shown in Fig. 1.1. Although it is an impressive engineering feat, such a complex approach is hardly scalable, especially due to the very limited reliability and compactness of the large number of wires required in a million-qubit computer.

Looking back into history, the first general-purpose computer built using vacuum tubes was the ENIAC [18] which occupied a large area as shown in Fig. 1.2 (left). Soon it was realized that such a system is not scalable with increasing demand for computational power. The first step towards scalability was miniaturization, i.e., replacement of vacuum tubes with transistors [19], which allowed the second generation computers. The next step towards scalability was integration, i.e., the invention of the integrated circuit (IC), which allowed all the devices such as transistors, resistors, capacitors to be integrated on the same chip [20]. This allowed fitting the same computing power into a few mm size chip compared to what was occupying the area

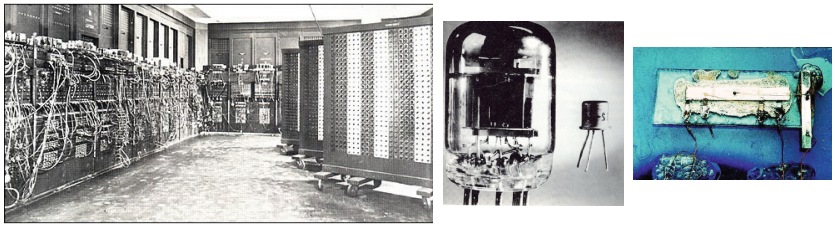


Figure 1.2: From vacuum tubes in ENIAC to the development of transistor and integrated circuit.

of a room.

Analogous to the evolution of integrated circuits, the current state-of-the-art quantum computers occupying a large area are limited mostly by the interconnect between the qubits operating inside a dilution refrigerator and bulky signal generators operating at RT. Although several setups have migrated from the use of generic equipment to custom-made electronics operating at RT, the specifications of such systems are not tailor-made for qubit control. Their main goal is to reduce the amount and cost of equipment/interconnect used to interface qubits with control electronics [21].

The ideal solution for large-scale quantum computers would be to operate both qubits and control electronics at the same cryogenic temperature [22]. Moving from the vacuum tube era to the IC era, leveraging 60 years of development in IC design technology, complex circuits can be designed using CMOS. However, the challenge is to operate these ICs at deep-cryogenic temperatures and consuming power within the limitations of the refrigerator to allow them to be integrated along with the qubit chip as shown in Fig. 1.3. Along such direction, custom-made PCBs with commercial off-the-shelf components operating at cryogenic temperatures have been designed to interface several control and read-out channels, thus minimizing cabling [23, 24].

In this thesis, we address several key issues related to the control of spin and superconducting qubits, primarily addressing the interconnect bottleneck between qubits and control electronics. We propose, analyze, and test systems designed for the control of large arrays of qubits always from a perspective of scalability, where low power is a key element. Although most of the quantum processors currently operate at milliKelvin temperatures, the cooling power of a dilution refrigerator is not sufficient to support complex CMOS circuits required to control thousands of qubits at these temperatures. Hence as an intermediate step, we target the design of cryogenic control electronics at $3\,\mathrm{K}$ due to higher available cooling power up to few Watts. This improves scalability by reducing the interconnect between RT and the $3\,\mathrm{K}$ plate of a dilution refrigerator [25, 26, 27]. Moreover, with the advent of high-temperature qubits operating above $1\,\mathrm{K}$ [15, 16, 17], our approach of would allow integration of control electronics and qubits on a single die/package in the near future.

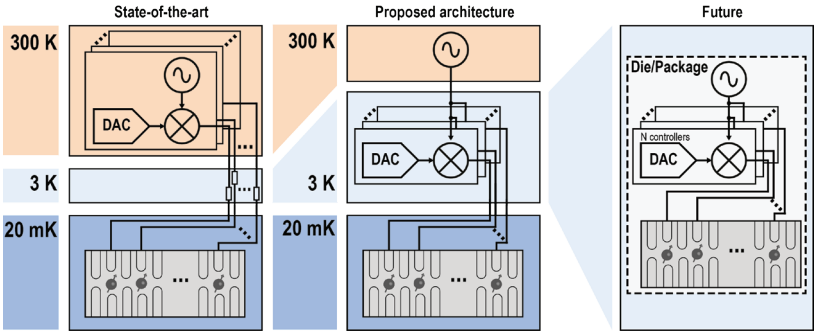


Figure 1.3: Three stages of development of the qubit control system towards full integration. Left, RT instruments connected to qubits via coaxial lines and attenuators. Middle, cryo-controller at 3 K directly connected to the qubits, which brings a considerable reduction in the wire count from RT to 3 K when targeting many qubits. Right, a future perspective of fully integrated control electronics and qubits on the same package/die, eliminating dense wiring all the way down to the package/die.

1.3. Scope of this work

To design CMOS ICs for qubit control, operating at cryogenic temperatures in proximity to the qubits, several key questions need to be addressed:

1. How do existing devices in CMOS technology designed to operate in the military temperature range i.e. $-55\,°C$ to $100\,°C$ behave at cryogenic temperatures $\sim 4\,K$?
2. How can we accurately predict the behavior of CMOS circuits based on the cryogenic device characteristics? How essential is a cryogenic model to predict the performance of complex CMOS integrated circuits?
3. What are the signal specifications necessary to achieve high-fidelity qubit control? What would be a scalable architecture to design a cryogenic multi-qubit controller?
4. What are the challenges in the practical realization of a scalable cryogenic multi-qubit controller?
5. How does the controller performance compare to the existing experimental setups?

Since cryogenic CMOS ICs for qubit control are in the initial development stages, there exist no research methodologies to address these issues. In this dissertation, each of these key questions is thoroughly addressed in individual chapters including a thorough analysis of the problem, the proposed ideas, and concluding results.

1.4. Organization of the dissertation

To design complex CMOS circuits operating at cryogenic temperatures, it is essential to have device models at those temperatures. The existing literature of cryogenic

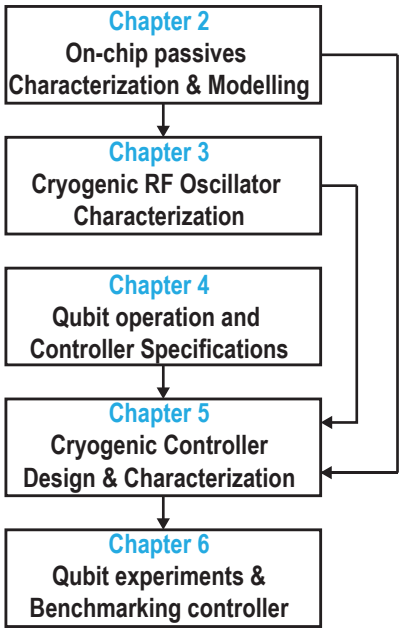


Figure 1.4: Link between various chapters in the thesis.

models is discussed and the knowledge gap in this area is indicated in **Chapter 2**. To close this gap, on-chip passive devices in 40-nm CMOS technology are characterized and modeled at $4\,\mathrm{K}$.

In **Chapter 3**, an RF oscillator is thoroughly characterized at cryogenic temperature and the results are predicted based on existing active device models as well as the passive devices characterized in Chapter 2.

Chapter 4 elaborates the various techniques used for control and readout of qubits to pave the way for the architecture definition of a qubit controller. The required signal specifications are analyzed in terms of signal power, tolerable noise levels, etc. Co-simulation of qubit operations (quantum gates) and behavioral model of the controller is used to obtain detailed circuit-level specifications necessary to design a high-fidelity multi-qubit controller.

The specifications obtained in Chapter 4 are used as the basis for designing a scalable cryogenic CMOS multi-qubit controller in 22-nm FinFET technology, presented in **Chapter 5**. The detailed design techniques and thorough cryogenic characterization of the controller are presented.

All the pieces are put together in **Chapter 6** to show the validity of the obtained specifications and circuit performance of the qubit controller, by using the designed cryogenic controller operating inside the dilution refrigerator, to control a two-qubit quantum processor. The functionality and efficacy of the controller are analyzed, giving way to ideas about future generations of qubit controllers as presented in **Chapter 7**. The chapters and their dependencies are shown in Fig. 1.4.

1.5. Original contributions

- On-chip passive components are characterized for the first time at $4.2\,\mathrm{K}$.
- A cryogenic RF oscillator is shown to operate at $4.2\,\mathrm{K}$, forming a key part of the first proposal to use cryo-CMOS circuits for qubit control.
- Key system and circuit-level specifications of a power-efficient qubit controller are derived from signal specifications necessary to realize high-fidelity quantum gates.
- The first cryogenic CMOS controller for spin qubits is developed.
- For the first time, a cryogenic controller performance is extensively benchmarked using parameters and techniques that are well-known in the quantum computing community.

2

Cryogenic passive devices and impact on RFIC design

Background: *In the previous chapter, the essence of using a cryogenic CMOS-based controller for a scalable quantum computer is described. The design of such a controller requires the characterization and modeling of active and passive devices at cryogenic temperatures.*

Abstract: *This chapter reviews the cryogenic characteristics of active devices from prior-art data, and presents the characterization and modeling of on-chip microwave passive components in TSMC 40-nm bulk CMOS, including metal-oxide-metal (MoM) capacitors, inductors, and resonators, at deep cryogenic temperatures (*$4.2\,\mathrm{K}$*). The variations in capacitance, inductance and quality factor are explained concerning the temperature dependence of the physical parameters. The resulting insights are utilized for modeling the characteristics of on-chip passive components, for the first time down to* $4.2\,\mathrm{K}$*.*

Summary: *This chapter comprises 6 sections. The need for cryogenic device modeling is highlighted in Section 2.1. The characteristics of active device parameters at cryogenic temperatures are derived from the prior-art in Section 2.2. The cryogenic measurement setup for a wide set of on-chip passive components is shown in Section 2.3. The design, characterization and modeling of an on-chip capacitor and inductor are elaborated in Section 2.4 and Section 2.5, respectively. Finally, the impact of cryogenic device performance on RFICs is analyzed in Section 2.6 using the developed cryogenic passive device models; followed by a conclusion in Section 2.7.*

Parts of this chapter have been published in *IEEE Journal of the Electron Devices Society* [28]. M. Mehrpoo designed the transformer and A. Ruffino designed the resonator. The author was involved in the design of capacitor and inductor as well as cryogenic characterization and modeling of all passive components.

2

2.1. Introduction

Solid-state circuits operating at cryogenic temperatures have been used for several applications. In quantum computing, as the number of qubits starts growing [5], it becomes infeasible to fit the cables between cryogenic quantum bits (qubits) and room-temperature control electronics into a standard cryogenic refrigerator. Thus, we advocate the integration of qubits and control electronics inside the refrigerator [22]. Complementary Metal Oxide Semiconductor (CMOS) circuits operating at cryogenic temperatures (Cryo-CMOS) have been proposed for the implementation of a scalable control and readout interface of cryogenic quantum processors [27, 29].

The design of solid-state electronics at cryogenic temperatures has triggered the need for the characterization of active and passive components as required to reliably predict the performance of cryogenic radio-frequency integrated circuits (RFIC) [30]. In this chapter, the cryogenic characteristics of devices from prior-art is summarized in the following section and the remaining sections focus on the characterization and modeling of a wide set of on-chip microwave passive components.

2.2. Cryo-CMOS devices

The characterization and modeling of CMOS devices have been pursued by the scientific community in the case of active devices, which is evident from papers that show DC characterization [31, 32], RF and noise characterization [33], device mismatch [34, 35] of bulk CMOS, as well as DC characterization [36, 37], small-signal and noise characterization [38] of SOI CMOS devices in different technology nodes.

2.2.1. Active devices

DC characterization

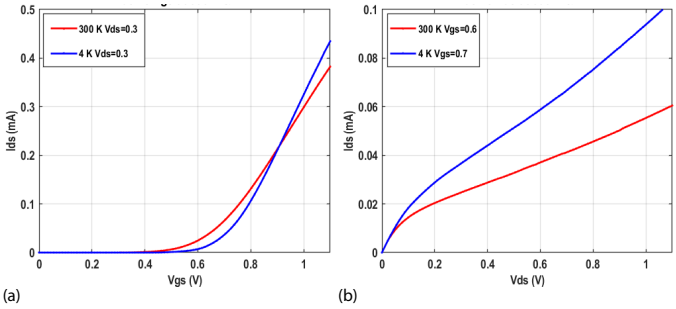


Figure 2.1: DC transfer characteristics of an NMOS transistor: (a) I_D versus V_{GS} and (b) I_D versus V_{DS} (W/L = 1.2 µm/40 nm).

DC characterization results of 40-nm bulk CMOS devices at $300\,\mathrm{K}$ and $4\,\mathrm{K}$, obtained from [35], are shown in Fig. 2.1. From the drain current (I_D) versus gate-to-source voltage (V_{GS}) characteristics, it can be observed that the threshold voltage (V_{TH}) at $4\,\mathrm{K}$ increases by almost $100\,\mathrm{mV}$ compared to room temperature (RT) [39, 40]. This presents a challenge for voltage headroom, especially in the case of stacked

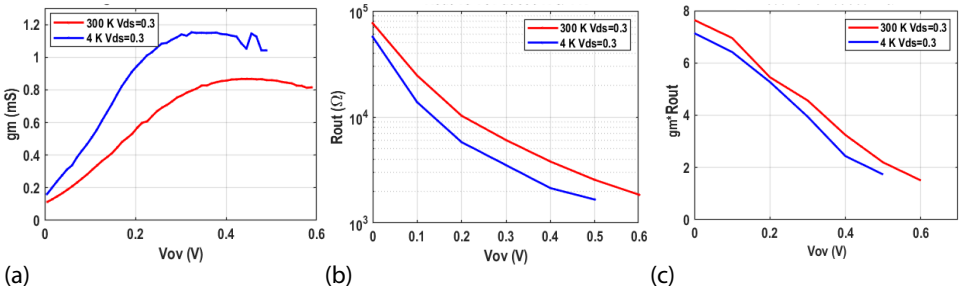


Figure 2.2: Derived circuit parameters from DC characteristics: (a) g_m, (b) R_{out} and (c) $g_m \times R_{out}$.

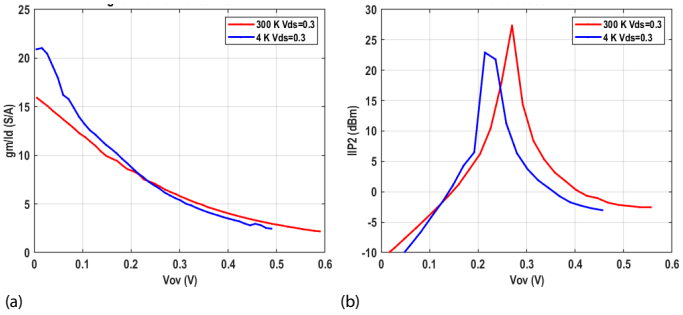


Figure 2.3: Circuit optimization parameters: (a) g_m/I_D and (b) IIP2.

transistor-based circuit topologies with demanding high linearity requirements. Hence, there is an urge to use low V_{TH} devices and constant current biasing. As shown in I_D versus drain-to-source voltage (V_{DS}) characteristics of Fig. 2.1, there is an increase in the current driving capability of the device. This is mainly caused by an increase in mobility of the devices at $4\,\mathrm{K}$ due to a decrease in electron scattering [39].

The DC measurement results of the MOS can be translated into design-oriented parameters, as shown in Fig. 2.2, to analyze how cryogenic CMOS affects RF circuit design choices and strategies. To ensure the same operating region, the plots are made with the same overdrive voltage (V_{ov}) and hence $100\,\mathrm{mV}$ increase in V_{GS} at $4\,\mathrm{K}$ compared to RT. Fig. 2.2 shows the transconductance (g_m) as a function of V_{ov}, suggesting that there is an increase in g_m by almost a factor of 2 in the strong inversion region. Fig. 2.2 shows the output resistance (R_{out}) of the devices at RT and $4\,\mathrm{K}$, suggesting that the R_{out} decreases by a factor of 2 in the strong inversion. Finally, from Fig. 2.2, one can infer that there is no increase in the intrinsic gain of the device at $4\,\mathrm{K}$ compared to RT. From Fig. 2.3, it can be observed that the transconductance efficiency (g_m/I_D) shows a slight improvement at $4\,\mathrm{K}$ in the weak-inversion region and remains unaffected in the other biasing regions. In contrast, the second-order input intercept point (IIP2) does not show any improvement at $4\,\mathrm{K}$.

RF performance

Based on the small-signal characterization of 32-nm SOI CMOS presented in [38], it can be concluded that the gate capacitance i.e. (C_{gs}, C_{gd}) shows a negligible change from $293\,\mathrm{K}$ to $6\,\mathrm{K}$. An increase in g_m, while no change in gate capacitance (gate oxide/metallization variation) points to an increase in device transit frequency (f_T). Moreover, due to the combined effect of increased g_m and reduced series resistance, the frequency where unilateral gain becomes unity (f_{max}) increased from $289\,\mathrm{GHz}$ to $511\,\mathrm{GHz}$.

Noise performance

The thermal noise at the drain current of a transistor should reduce almost 75x when cooling from $300\,\mathrm{K}$ to $4\,\mathrm{K}$. However, based on the measurement results in [38], the actual reduction is about one order of magnitude. This could be attributed to the actual channel temperature, which is much higher than the ambient temperature. On the other hand, no change is observed for the input-referred flicker noise at cryogenic temperatures [41]. However, it should be noted that at these temperatures i.e.$\sim 4\,\mathrm{K}$, defects are the dominant source of 1/f noise, as can be observed from the Lorentzian feature in the measurement results presented in [41].

Effect on circuit performance

Based on the device parameter variations, the operation of a highly linear class-A Cryo-CMOS (power) amplifier can be analyzed as follows. The voltage gain of such an amplifier is governed by

$$A_v = g_m \times R_L = \frac{g_m}{I_D} \times (R_L \times I_D), \tag{2.1}$$

where R_L ($R_L << r_{out}$) is the load resistance seen by the amplifier and is fixed by the matching network, I_D is the current of the amplifier and is determined by the output power (P_{OUT}) required to drive the qubits. As can be gathered from Fig. 2.3, to obtain the best linearity, the device should be biased in the strong inversion region at an overdrive voltage of $\sim$0.25 V, for both $4\,\mathrm{K}$ and RT. The device can then be sized based on the calculated load current and overdrive voltage. From Fig. 2.3, it can be observed that in moderate and strong inversion, g_m/I_D remains almost the same over temperature. Consequently, the voltage gain of the amplifier would be the same over temperature for large-signal operations where linearity is crucial. However, if the linearity requirements are more relaxed in blocks such as readout low noise amplifiers, it is suggested to bias the transistor towards the weak-inversion, where g_m/I_D is higher at $4\,\mathrm{K}$, and thus the circuit can be more power-efficient at cryogenic temperatures.

2.2.2. Passive devices

In the case of passive devices, cryogenic characterization of *off-chip* discrete commercial *off-the-shelf* capacitors and resistors [42, 43] proved that the capacitance and resistance could change drastically at those temperatures depending on the material, thus affecting circuit performance. In the case of *on-chip* passive devices,

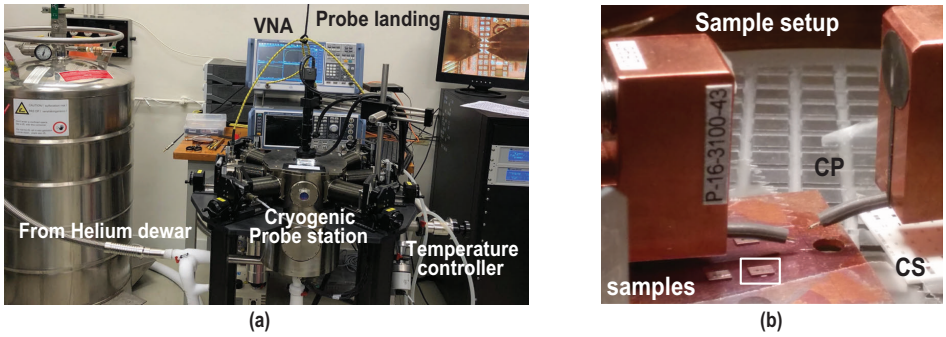


Figure 2.4: (a) Cryogenic probe station measurement setup. (b) Sample setup inside the 4 K chamber.

prior work is limited to the measurement of capacitor and resistor values [44, 45]. Consequently, there is a lack of cryogenic models for on-chip inductive/capacitive components predicting their behavior, variation and quality factor.

In the following sections, for the first time, we have modeled the characteristics of a wide set of *on-chip* passive components in bulk CMOS at cryogenic temperatures, which would complement active device models for accurate prediction of the behavior of RFICs at cryogenic temperatures.

2.3. Test structures and measurement setup

Several test structures were fabricated in the 1P7M-4X1Z1U TSMC 40-nm bulk CMOS with an ultra-thick metal layer to characterize passive components both at 300 K, and 4 K, comprehensively. A high-density rotative MoM capacitor with a poly shield was chosen from the library provided by the foundry. For the inductance and metal resistance characterization, an inductor with high-inductance windings was designed to be less sensitive towards calibration errors. Finally, a resonator was also fabricated to validate the cryogenic model of the inductor and capacitor. The substrate was left floating for all the test structures.

The measurements were done using ground-signal-ground (GSG) probes in a 40 GHz Lakeshore CPX cryogenic probe station with R&S ZNB40 vector network analyzer (VNA) (see Fig. 2.4 (a)). To ensure proper thermalization, the dies were mounted with conductive glue on a copper plate (CP), which was securely taped to the sample holder (see Fig. 2.4 (b)).

The thermal conductivity of the chip substrate (boron-doped silicon) at temperatures below 20 K is comparable to that at 300 K [46], while thermal conductivity of copper remains the same or improves depending on its purity at 4 K [47], suggesting a good thermal link between the sample holder and device under test (DUT). Since all the measured test structures were passive components and the measurements were done by applying small AC signals, the self-heating should be negligible. During the measurement, it was ensured that the temperature sensor mounted on the sample holder was at 4.2 K. Consequently, although the die temperature was not measured directly, considering the large area under the DUT, no static power dissipation and

large copper mass below the dies, it can be concluded that the DUT was at $4.2\,\mathrm{K}$. Moreover, the probes were thermally anchored with thick copper wires to the $4\,\mathrm{K}$ stage of the probe station.

Due to the variation in the GSG probe electrical characteristics over temperature, short-open-load-through (SOLT) calibrations were done right before the measurement using a Picoprobe calibration substrate (CS-5) at the measurement temperature. Although the load standards in the CS-5 are accurately trimmed to their $50\,\Omega$ stated value at room temperature, their absolute value at cryogenic temperature is not specified, and therefore, it was measured by injecting a DC signal. The resistance of the short fixture was measured and it was subtracted from the measurement of the load, to remove the effect of cable and GSG probe and to yield the absolute resistance of the load fixture. At $300\,\mathrm{K}$, the measured load was $50.55\,\Omega$, while at $4.2\,\mathrm{K}$, its value was $49.91\,\Omega$, showing a negligible ($\sim 1\,\%$) change. The measured value of the load was then used as part of the cal kit file for VNA calibration.

For probing, all the components were connected to a $100\,\mu\mathrm{m}$ GSG pad without electrostatic discharge (ESD) protection diodes to minimize parasitic capacitance (see chip micrographs in Fig. 2.7, Fig. 2.10, and Fig. 2.19 (b)). The two ground pads in the GSG structure are shorted to each other at metal-1 (M1) level after using vias from AlCu pad (AP) layer to M1 layer, thus creating the signal-to-ground parasitic capacitance of $60\,\mathrm{fF}$. Finally, the pad parasitics were de-embedded from the measurement results of the test structures by using an open test fixture [48].

Since the DUT dimensions were quite small, the coupling between the probes was simulated to ensure that it does not affect the accuracy and negligibly affect the precision of measurement results between several probe landings. Although the coupling between the probes can be both electrical and magnetic, below $30\,\mathrm{GHz}$, the dominant effect is due to electrical coupling [49].
The capacitance between the probes with an area of 50 μm $\times$ 20 μm can be roughly calculated as follows:

$$\begin{aligned} C &= \frac{\epsilon_0 \times \epsilon_r \times Area}{D} \\ C &= \frac{8.85 \times 10^{-12} \times 3 \times 50 \times 10^{-6} \times 20 \times 10^{-6}}{100 \times 10^{-6}} \\ C &= 265\,aF \end{aligned} \tag{2.2}$$

where D denotes the distance between probes.

To consolidate this result, 3D EM simulation was done in CST studio Suite®, consisting of both probes landed on open pad test structures with the same dimensions and separation as the capacitor test structure. As shown in Fig. 2.5, the ports are placed at the end of the probe tips.

Figure 2.6 shows the simulated coupling between the probes. From the plot, it can be observed that at the frequency where the capacitance is extracted i.e., $100\,\mathrm{MHz}$, the capacitive coupling between the probes is $\sim 0.2\,\mathrm{fF}$ (close to the initial estimate from the calculation). Assuming the error in landing is in the order of $50\,\mu\mathrm{m}$, the maximum measurement error would be below $0.1\,\mathrm{fF}$. This is negligible compared

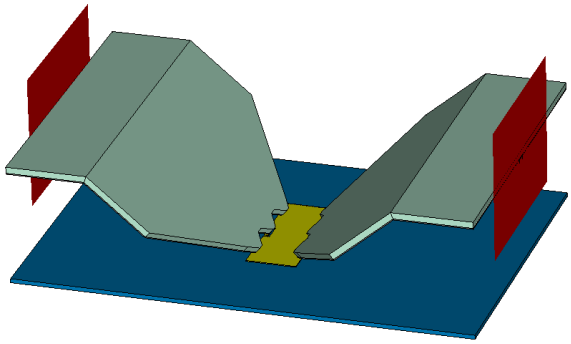


Figure 2.5: Probe coupling simulation setup

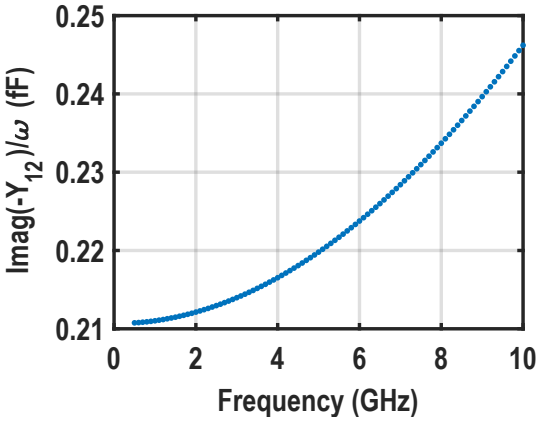


Figure 2.6: Capacitive coupling between the probes

to the DUT capacitance of $\sim 200\,\mathrm{fF}$. Consequently, measurement precision is negligibly affected by probe landing error that occurs between consecutive measurements.

2.4. MoM capacitance

A high-density rotative MoM capacitor with a poly shield was taped out using stacked inter-digitated metal fingers in layers 1 to 5 with a finger width of $100\,\mathrm{nm}$ and a spacing of $90\,\mathrm{nm}$. To increase the capacitance to a measurable value and in order for it not to be dominated by the parasitics of pads, 10 such capacitors were connected in parallel, with 6 horizontal and 38 vertical fingers. This provides a capacitance of $202\,\mathrm{fF}$ for an area of $150\,\mu\mathrm{m}^2$ ($7.97\,\mu\mathrm{m} \times 1.89\,\mu\mathrm{m} \times 10$). The pitch for landing the probes is $100\,\mu\mathrm{m}$ and the estimated capacitive coupling between the probe tips based on 3D EM simulation is $\sim 0.2\,\mathrm{fF}$, hence neglected.

The MoM capacitor can be modeled by a frequency-independent π-network [50],

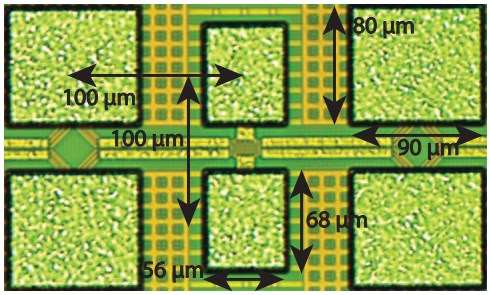


Figure 2.7: MoM capacitor micrograph.

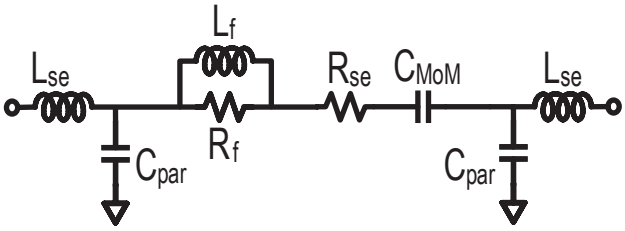


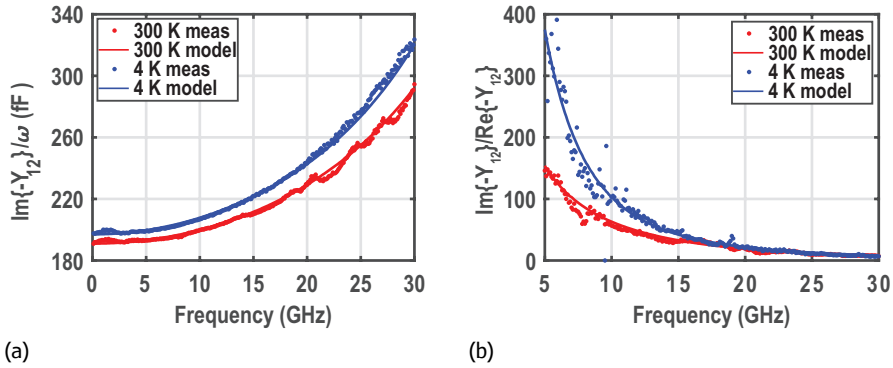
Figure 2.8: Lumped-element model of MoM capacitor.

as shown in Fig. 2.8, where C_{MoM} is the actual capacitance due to the interdigitated metal fingers across an extra low-k inter-metal dielectric [51], and C_{par} represents the parasitic capacitance between terminals and ground plane (poly shield). R_{se} and L_{se} represent the equivalent series resistance and inductance, respectively, of the traces and vias from the pad to the device terminals.

Since the GSG pads were not abutted to the capacitor, the open test-fixture is not sufficient to completely de-embed the trace connecting the pads to the capacitor. Hence, the measurement results of -imag$\{Y_{12}\}/\omega$ show frequency dependence (similar to the process design kit data) and is modeled as a series parasitic inductance (L_{se}) in the model. Hence, R_{se} and L_{se} must be included in the model. The effect of R_{se} is negligible since the top metal layer was used for interconnection to the pad. At low frequencies, the L_{se} acts as a short and the extraction of capacitance is accurate without de-embedding this inductance. However, L_{se} affects the self-resonance frequency (SRF) of the structure. The frequency-dependent losses are modeled using R_f and L_f, which constitute both metal loss (skin effect) and dielectric loss. L_f is not a physical parameter, but a fitting parameter used to model the frequency-dependent loss. The quality factor of the capacitor above $10\,\mathrm{MHz}$ is limited by the series resistance [52], and hence, the leakage resistance (modeled as a very high resistance across the capacitor terminals at DC) due to the interface traps [53] is ignored in the model.

The parameters in the model can be extracted using Y-parameters.

Fig. 2.9 (a) shows the measured $Im\{-Y_{12}\}/\omega$ (ω is the angular frequency), from which the C_{MoM} can be extracted at the lowest measured frequency (i.e., $100\,\mathrm{MHz}$),



(a) (b)

Figure 2.9: Extraction of MoM (a) capacitance and (b) quality factor.

where the effect of parasitic inductance is negligible [54]. The capacitance incurs a slight change at $4\,\mathrm{K}$ compared to room temperature (RT) due to variation in the dielectric constant, as the thermal contraction of metals is negligible [47]. Based on several measurements, the precision error in C_{MoM} value was obtained to be less than $1\,\%$ (i.e., $\sim 0.5\,\mathrm{fF}$ variation in $200\,\mathrm{fF}$).

For the quality factor measurement, the uncertainty increases when the desired real impedance is negligible compared to the VNA reference impedance of $50\,\Omega$ [55]. Hence, at frequencies below $5\,\mathrm{GHz}$ (where the quality factor tends towards infinity), the error in the determination of the equivalent series resistance and capacitor's quality factor ($Im\{-Y_{12}\}/Re\{-Y_{12}\}$) would be significant and is excluded from Fig. 2.9 (b). Due to the reduction of dielectric and metal loss at lower temperatures, there is a boost in the quality factor at frequencies below $10\,\mathrm{GHz}$. However, the dielectric loss does not improve over temperature above a certain frequency. This is also in line with the measurement results of capacitors in the military temperature range in a similar technology, as presented in [52]. Consequently, a negligible quality factor improvement is observed above $15\,\mathrm{GHz}$, as can be gathered from Fig. 2.9 (b). Table 2.1 concludes the discussion on MoM capacitors and summarizes the change of the model parameters over temperature.

2.5. Inductance

To characterize the inductance and quality factor variation over temperature, a multi-turn transformer featuring a two-turn primary winding with $190\,\mu\mathrm{m}$ diameter and $8\,\mu\mathrm{m}$ trace width was designed using the ultra-thick metal layer, as illustrated in Fig. 2.10. The GSG pad parasitics were de-embedded from the measurement results of the test structures by using an open test fixture. An open-structure de-embedding is sufficient for this test structure since the DUT plane is at the pads. The Y-parameters of the open structure were subtracted from the Y-parameters (Y_{11} and Y_{22}) of the test structure measurement results to obtain the Y-parameters of the

Table 2.1: Model parameters of MoM capacitor at RT and 4 K.

Parameter	Units	RT	4 K
C_{MoM}	fF	191	197
R_{se}	Ω	0.5	0.1
C_{par}	fF	28	26.5
L_{se}	pH	20	20
R_f	Ω	3	3
L_f	pH	17	24

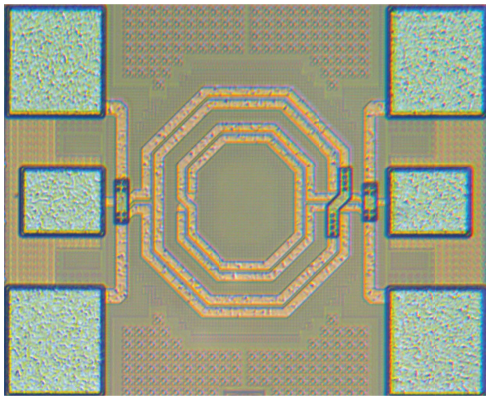


Figure 2.10: Transformer micrograph.

device under test (DUT).

The dotted lines in Figs. 2.11 to 2.13 show the extracted parameters of the inductor versus frequency based on the S-parameter measurement at both RT and 4 K. At first glance, it can be observed that there is a slight reduction in inductance and a substantial improvement in the quality factor of the inductor windings at 4 K compared to RT. To gain more insight and to track the changes in various parameters over temperature, a lumped-element model is presented in Section 2.5.1. Based on the developed model, some modifications in the physical parameters of the metal stack provided by the foundry are suggested in Section 2.5.2. The measurement results are also replicated by using EM simulation. Note that, the inductor SRF is at 21 GHz, as can be gathered from Fig. 2.12a. Hence, Figs. 2.11a and 2.13 have been plotted up to 21 GHz. To keep the visibility, the zoomed-in version of $\mathrm{Im}\{Z_{11}\}/\omega$ and $Re\{Z_{11}\}$ are shown up to 10 GHz.

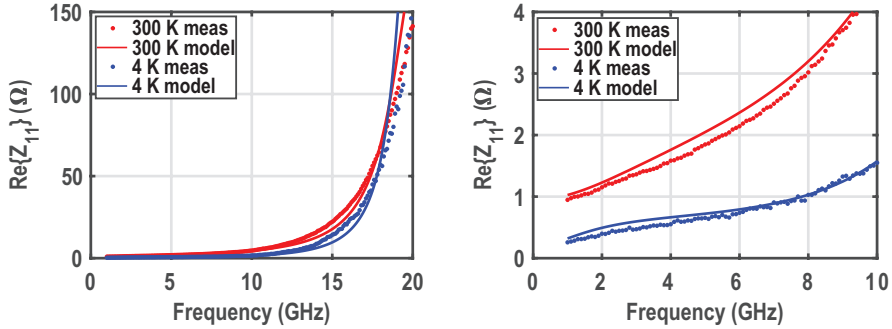


Figure 2.11: Extraction of (a) series resistance and (b) series resistance (zoomed in), from measurement and lumped-element model of inductor.

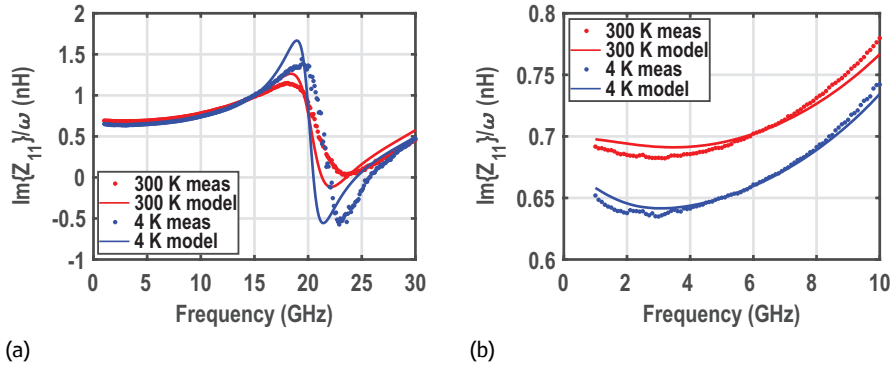


Figure 2.12: Extraction of (a) inductance and (b) inductance (zoomed in), from measurement and lumped-element model of inductor.

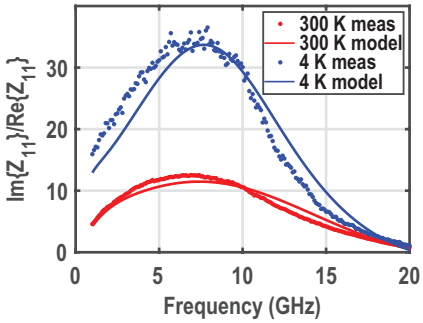


Figure 2.13: Extraction of quality factor from measurement and lumped-element model of inductor.

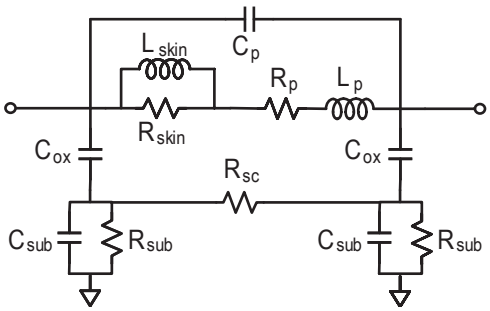


Figure 2.14: Inductor model.

2.5.1. Lumped element model

The inductor can be modeled using the well-known frequency independent lumped model for on-chip spiral inductors [56], as depicted in Fig. 2.14, where L_p represents the inductance, R_p describe the DC ohmic loss. C_{ox} denotes the oxide capacitance, while C_p represents the capacitance between the metal lines. C_{sub} and R_{sub} model the substrate capacitance and resistance, respectively. R_{skin} and L_{skin} model the frequency-dependent losses (skin effect) in the inductor windings.

R_p (extracted from $Re\{Z_{11}\}$ shown in Fig. 2.11 at $1\,\mathrm{GHz}$ where the skin effect is negligible) is ~5× lower at $4\,\mathrm{K}$ compared to RT, due to the increase in copper conductivity [47]. Note that the resistivity of copper does not reduce proportionally with temperature until $4\,\mathrm{K}$ but it saturates at certain temperatures, due to impurities and crystallographic defects in the metal layers [30]. At higher frequencies, the skin effect dominates and the loss becomes proportional to $1/\sigma_{cu}\delta$, in which the skin depth $\delta = \sqrt{2}/\sqrt{\omega\mu\sigma_{cu}}$, where μ and σ_{cu} represent the magnetic permeability and conductivity of copper respectively. Since the conductivity increases by 5×, skin depth and thus the inductor loss at higher frequencies decreases by $\sim\sqrt{5}$ [57], as confirmed by Fig. 2.11a for frequencies above $10\,\mathrm{GHz}$.

The inductance associated with a loop has two components; internal (L_{int}) and external (L_{ext}) inductance [58]. L_{ext} dominates the total inductance and is dictated by the currents flowing on the surface of the conductor. Its value is determined by the phase velocity and characteristic impedance of the inductor trace and hence, is a strong function of the coil dimension. L_{int}, the non-dominant component, is associated with the internal current of the inductor and can be calculated by

$$L_{int} = \frac{R_{ac}}{\omega}, \tag{2.3}$$

where ω is the angular frequency and R_{ac} represents the frequency-dependent losses. Further, R_{ac} can be calculated as

$$R_{ac} = \frac{l}{\sigma w \delta}, \tag{2.4}$$

where σ is the metal conductivity, δ is the skin depth, l and w are the length and width of the trace respectively [58]. Replacing skin depth $\delta = \sqrt{2}/\sqrt{\omega\mu\sigma}$ in the above

Table 2.2: Lumped-element model parameters of inductor at RT and 4 K.

Parameter	Units	RT	4 K
L_p	pH	691	650
R_p	Ω	0.95	0.22
R_{skin}	Ω	1.2	0.53
L_{skin}	pH	48	48
C_p	fF	18	19
C_{ox}	fF	50	52
C_{sub}	fF	19	22
R_{sub}	kΩ	1.24	1000
R_{sc}	kΩ	2	2000

equation, the final value of L_{int} can be obtained as

$$L_{int} = \frac{R_{ac}}{\omega} = \frac{l}{2w}\sqrt{\frac{\mu}{\sigma\pi f}} \tag{2.5}$$

Intuitively, an increase in conductivity would reduce the skin depth and force the current to flow in the boundary of the conductor. Consequently, the current flowing in the conductor interior reduces, decreasing L_{int}, and thus, the total inductance. This phenomenon is also observed in our measurement results; the 5× increase in conductivity led to a $\sim 5\,\%$ reduction in inductance (extracted from $Im\{Z_{11}\}$ at the lowest measured frequency), as shown in Fig. 2.12.

Fig. 2.13 reveals that the peak quality factor of the inductor (extracted from $Im\{Z_{11}\}/Re\{Z_{11}\}$) increases by 2.7× from RT to 4 K. The improvement is partially contributed (1.6× as verified from EM simulation in Section 2.5.2) by the increase in conductivity and partly due to the reduction of tangential electric field losses in the silicon substrate, as it becomes highly resistive due to dopant freeze-out.

Table 2.2 summarizes the values of model parameters at RT and 4 K. R_{sub} and substrate coupling resistance (R_{sc}) increases by 3 orders of magnitude at 4 K mainly due to substrate freeze out [59]. For low resistive substrates, the capacitance from the windings to the ground plane is dominated by C_{ox} [60, 61], while for highly resistive substrates, the effective capacitance is lowered by C_{sub} in series with C_{ox}, resulting in a slight increase in the frequency where peak quality factor occurs.

The self-resonance frequency of the inductor increases by $5\,\%$, due to the decrease in both inductance and effective parasitic capacitance to ground. The change in parasitic capacitance to ground can be explained as follows. In the lumped element model of an inductor, the capacitance from the transformer windings to the substrate is represented by a series combination of C_{ox} and $C_{sub}||R_{sub}$. At 300 K,

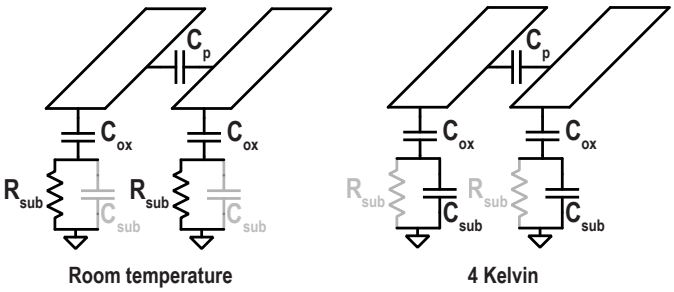


Figure 2.15: Parasitics of the inductor at room temperature and 4 K

in a low resistive substrate, the effective capacitance from the windings to ground is dominated by C_{ox}. However, at 4 K, since the substrate becomes highly resistive, the effective capacitance to ground is dictated by the series combination of C_{ox} and C_{sub}, thus reducing the total value of the winding capacitance to ground.

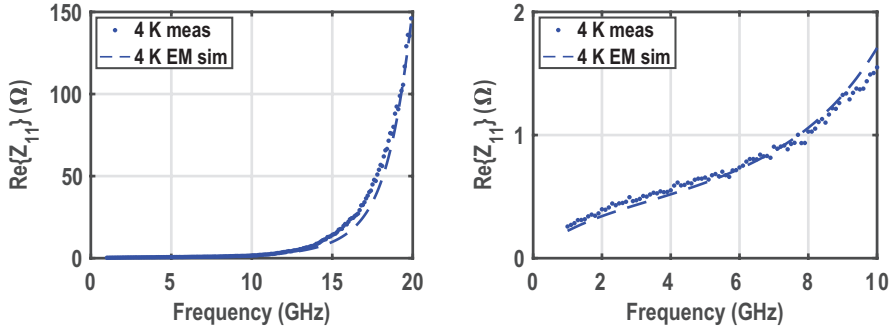
2.5.2. EM model

Besides using lumped-element models of integrated passives, it is convenient for circuit designers to perform EM simulations to generate S-parameters of inductors/transformers and use them for circuit design. For this reason, and to extend the scope of this work towards the design of cryogenic custom integrated passive networks (e.g., hybrid coupler, power splitter, etc.), the metal stack provided by the foundry was modified to enable EM simulations, predicting cryogenic operation.

Based on the performed measurements, the following material properties have been modified in the foundry metal stack: the conductivity of metal-7 (M7) layer was incremented 5×, to reproduce the copper conductivity increase, while the substrate resistivity was increased 1000×, to reproduce the effect of carrier freeze-out. The obtained modified metal stack was used to perform EM simulations in Keysight ADS® Momentum®, with an infinite conductive plane beneath the substrate as the current return path, while the simulator temperature was kept at 300 K. The obtained results could accurately predict the performance of the inductor at 4 K, as can be gathered from Figs. 2.16 to 2.18. The measured quality factor of the windings was slightly different from the simulation results at 4 K. This is attributed to the exclusion of metal fill in EM simulations, which is required to satisfy the metal density rules provided by the foundry [62].

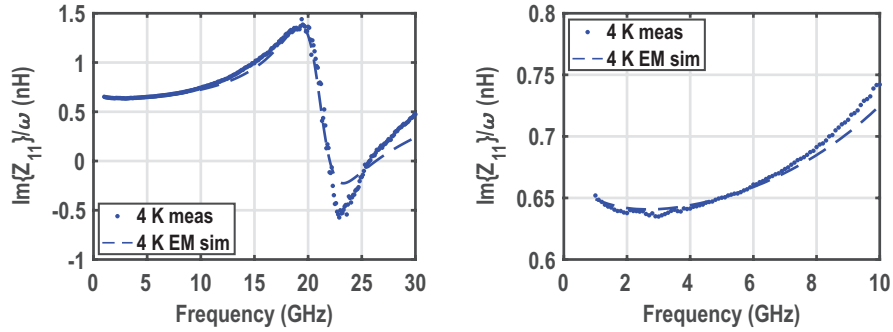
2.6. Impact on RFICs

In Section 2.2.1, several design parameters are derived from primary characteristics of CMOS transistors at cryogenic temperatures [63], to analyze the benefits and challenges of cryogenic RFIC design. Similarly, the impact of cryogenic behavior of passive devices on circuit design is analyzed and the developed model is validated using a resonator in this section.



(a) (b)

Figure 2.16: Extraction of (a) series resistance and (b) series resistance (zoomed in), from measurement and EM simulation of inductor.



(a) (b)

Figure 2.17: Extraction of (a) inductance and (b) inductance (zoomed in), from measurement and EM simulation of inductor.

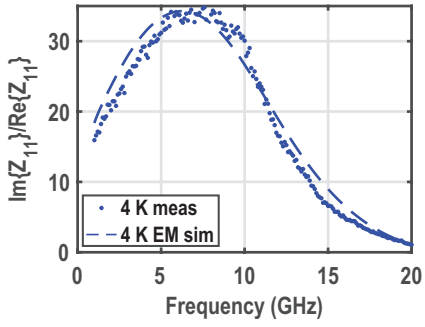


Figure 2.18: Extraction of quality factor from measurement and EM simulation of inductor.

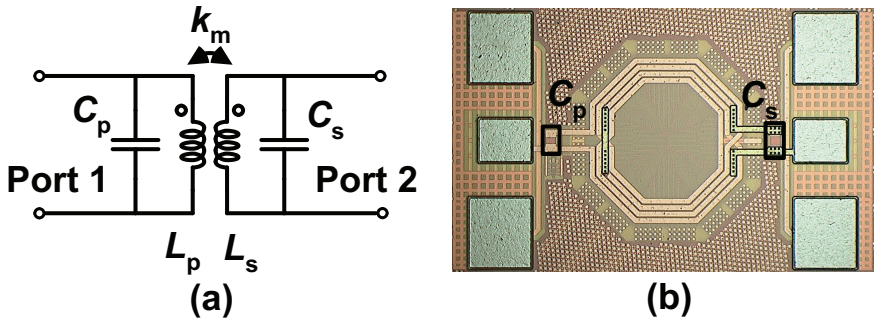


Figure 2.19: Tank (a) schematic and (b) micrograph.

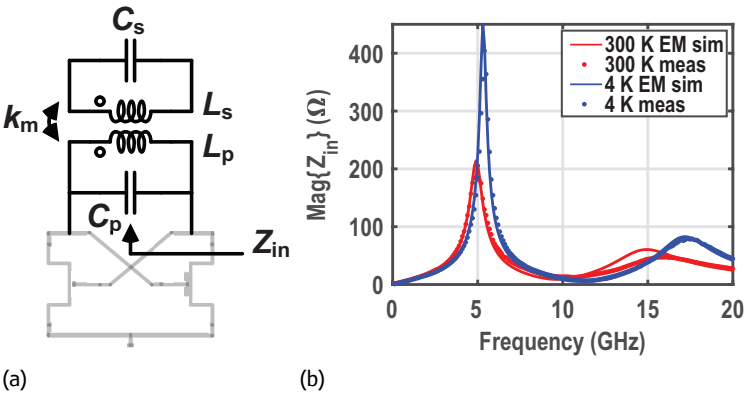
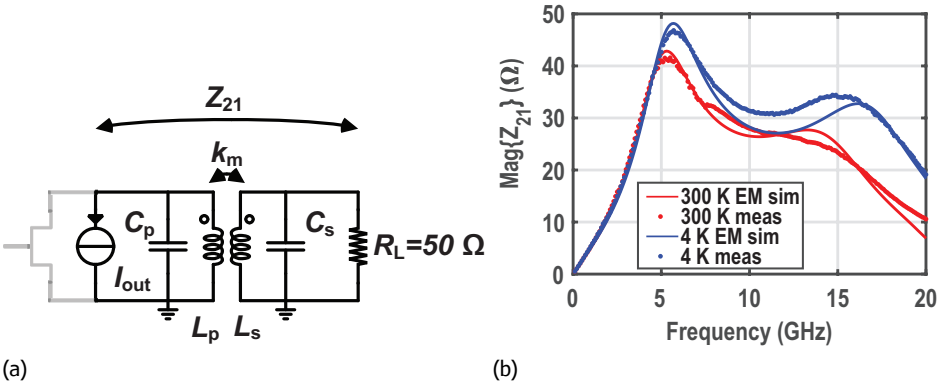


Figure 2.20: (a) Schematic of transformer-based resonator used in an oscillator, (b) Tank input impedance (Z_{in}).

To validate the developed models and combine the use of modified EM simulation for inductor, with the cryogenic lumped-element model of capacitors, a custom transformer-based resonator (matching network), shown in Fig. 2.19, was designed. The tank is also used to analyze the impact of the cryogenic operation of passive components on the performance of RFIC blocks like oscillators [64], power amplifiers (PAs) [65], and wideband LNAs [66]. The application of the transformer-based resonator in such circuits is shown in Figs. 2.20a, 2.21a and 2.22a.

The custom transformer was realized by an interwinding multiturn spiral inductor in the ultra-thick metal-7 layer with metal-6 underpass and AlCu pad (AP) overpass, while capacitors were implemented as design kit rotative MoM capacitors. The resonator parameters are L_p = 1.25 nH, L_s = 1.07 nH, k_m = 0.72, C_p = 340 fF, and C_s = 385 fF. Its performance at 4 K was estimated by combining EM simulation of the developed cryogenic metal stack for the spiral transformer and the modified cryogenic model for the capacitors, through layout abutment. The simulation results are compared with the measurement results in Figs. 2.20b, 2.21b and 2.22b.



(a) (b)

Figure 2.21: (a) Schematic of transformer-based resonator used in output driver, (b) Tank trans-impedance (Z_{21}).

Fig. 2.20b shows the input impedance of the resonator with Port-2 open ($|Z_{\mathrm{in}}|$), which is inversely proportional to the power consumption of a transformer-based oscillator [64]. There is an increase in the impedance peak of the resonator, from RT to $4\,\mathrm{K}$, due to the overall increase in quality factor, which is well predicted by the cryogenic models. Thanks to this improvement, one can obtain the same output voltage swing for smaller current consumption, thus improving the oscillator's power efficiency. The reduction in inductance and the effective parasitic capacitance causes the first resonance to shift towards higher frequencies by $8\,\%$. The ratio of the resonant frequencies (i.e., the frequency separation between the impedance peaks in $Re\{Z_{\mathrm{in}}\}$) merely depends on the coupling factor (k_{m}), which increases by $8\,\%$ as predicted by the model.

Fig. 2.21b shows the trans-impedance Z_{21} of a matching network, where the tank in Fig. 2.21a is terminated with a $50\,\Omega$ load resistance. This parameter is widely used in calculating the output transfer function when designing wideband PAs [65]. It can be observed that there is a substantial increase in the Z_{21} at $4\,\mathrm{K}$ compared to RT, especially at higher frequencies. Moreover, there is a slight increase in bandwidth due to the increase in k_{m} and an overall shift of the poles of the transfer function towards higher frequencies, due to the decrease in inductance of the windings. Such improvements can be exploited to deliver larger output power for the same current, and over a larger bandwidth at $4\,\mathrm{K}$ compared to RT. So, this is a considerable advantage for PA design at cryogenic temperatures.

Fig. 2.22b shows the measured S_{21} of the tank, which is required to predict the insertion loss (IL) of input/output or inter-stage matching networks in LNAs/PAs. At cryogenic temperatures, the S_{21} improves, consequently reducing the insertion loss. Note that, for an LNA, the insertion loss of the input matching network directly adds to the overall noise figure. Therefore, such an improvement represents a clear advantage in designing multi-stage LNAs with large bandwidth operating at cryogenic temperatures. As can be gathered from Figs. 2.20b, 2.21b and 2.22b, the developed

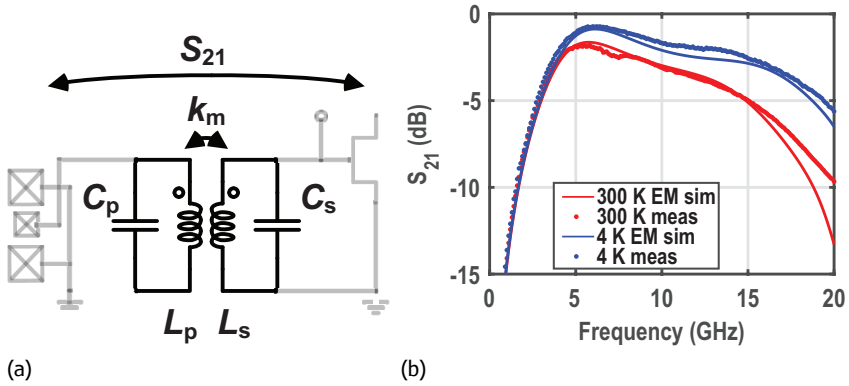


Figure 2.22: (a) Schematic of transformer-based resonator used in low-noise amplifier, (b) Tank insertion loss (S_{21}).

models can fairly predict the cryogenic performance of the passive network in such circuits.

Such models have also been employed to design more complex circuits, such as a cryogenic CMOS circulator [67], based on LC first- and second-order all-pass filters, and a parametric CMOS LNA [68], with transformer-based passive amplification. The developed models were used to predict the performance of such circuits at $4\,\mathrm{K}$, leading to more optimized designs and gaining more insights about the cryogenic operation of the circuits.

2.7. Conclusion

Passive components at cryogenic temperatures show in general higher quality factor ($\sim$2$\times$) due to higher metal conductivity and lower loss in the substrate. However, the value of inductive and capacitive on-chip components changes slightly ($\sim$ 5%) from RT to $4\,\mathrm{K}$. These variations can be replicated in an EM simulation by manipulating the resistivity of metals and substrate. As a result, RFIC designers can predict the performance of cryogenic passive devices both by using EM simulation and/or by scaling the presented lumped model parameters. This enables, in combination with active device models, the reliable design of cryogenic RFICs.

3

Cryogenic RF oscillator: Characterization and analysis

Background: *In the previous chapter, on-chip microwave passive components were characterized and modeled at* $4\,\mathrm{K}$ *to simulate the performance of the resonator used in several RF circuits such as oscillators, low noise amplifiers and output drivers.*

Abstract: *The main aim of this chapter is to prove the validity of the passive device models and understand several device level phenomena at cryogenic temperatures by characterizing a CMOS RF oscillator from* $300\,\mathrm{K}$ *to* $4\,\mathrm{K}$*. This chapter presents a cryogenic oscillator as part of the first proposal for using cryo-CMOS circuits and systems for quantum computing applications [26, 27]. The class-*$F_{2,3}$ *6-GHz oscillator achieves an integrated frequency noise of* $3.4\,\mathrm{kHz}_{RMS}$ *over* $\sim 10\,\mathrm{MHz}$ *bandwidth, which when integrated in a PLL can drive state-of-the-art qubits without limiting their performance.*

Summary: *This chapter is comprised of 4 sections. After a brief introduction in Section 3.1, circuit specifications of a PLL and oscillator are derived from qubit control requirements in Section 3.2. Thorough characterization results of an RF oscillator using a dipstick in the liquid helium barrel provides insights about device-level variations at cryogenic temperatures, as presented in Section 3.3; followed by a conclusion in Section 3.4.*

Parts of this chapter have been published in *IEEE Journal of Solid-State Circuits* [27]. The author was responsible for the design of the measurement setup, characterization of the chip at cryogenic temperatures and data analysis. The chip was designed by M. Shahmohammadi.

3.1. Introduction

Control and read-out of solid-state qubits require the generation and acquisition of specific electronic signals. Typically, for the manipulation of a single qubit, microwave bursts with a short duration ($<1\,\mu s$) must be applied, e.g., 4–$8\,GHz$ bursts for transmons [69, 70] and $>6\,GHz$ bursts for spin qubits [71, 16]. The application of microwave bursts for qubit control requires the generation of a carrier using an oscillator in a phase-locked loop (PLL).

As proposed in Chapter 1, an integrated cryogenic controller is necessary to address the interconnect complexity between the qubits and control electronics. A cryogenic oscillator integrated with the controller would further reduce the cabling requirement between room temperature and cryogenic controller. Prior-art applications of cryogenic oscillators include atomic fountain clocks employing sapphire oscillators with high frequency-stability [72] and electron spin resonance detectors employing inductor-capacitor (LC) tank-based CMOS oscillators [73]. In this chapter, a class-$F_{2,3}$ CMOS oscillator operating at $4.2\,K$ is described, achieving the required frequency noise specification for qubit control when integrated in a phase-locked loop (PLL).

3.2. Specifications

In order not to disturb the quantum state of the qubit, the controller must generate accurate and extremely low-noise signals. However, even if an ideal control signal is applied, the state of the qubit is destined to be lost in a relatively short time, usually characterized by the dephasing time T_2^* [74], which is much shorter than the duration of practical quantum algorithms. Therefore, the controller is also responsible for implementing qubit corrections, such as echo techniques [75] and quantum error correction (QEC) schemes [76], designed to maintain the quantum state over longer periods. In order not to reduce the dephasing time ($T_2^* = 120\,\mu s$ for state-of-the-art spin qubits in purified silicon [77]), the frequency noise should be lower than $1.9\,kHz_{RMS}$ over a bandwidth with the upper bound set by the qubit operation speed (up to $10\,MHz$) and the lower bound set by the echo-period [78, 79]. Achieving such a frequency noise would ensure that the qubit control fidelity is not limited by the performance of the cryogenic oscillator but by the qubit device itself.

The tolerable frequency noise (FN) of a PLL-stabilized oscillator for qubit control should be lower than $1.9\,kHz_{RMS}$ for a $6\,GHz$ carrier. Since the total integrated phase noise (PN) is crucial for this application, the PLL's bandwidth (f_{PLL}) should be optimized for the in-band and out-of-band PN performance. Beyond the PLL's bandwidth, the PN is dominated by the oscillator, and can be expressed as $\mathcal{L}_{osc}(\Delta f) = \alpha/\Delta f^2$, where Δf is the frequency offset from the carrier and α is a constant coefficient in Hz^2/Hz. Note that the oscillator's $1/f^3$ corner is assumed to be below the PLL's bandwidth.

The PLL's in-band PN is constrained by the PN of phase detector and reference clock, which should be roughly equal to the oscillator's PN at f_{PLL}. Consequently, the PLL's PN can be expressed by

$$\mathcal{L}_{PLL}(\Delta f) \approx \begin{cases} \alpha/f_{PLL}^2 & \Delta f \leq f_{PLL} \\ \alpha/\Delta f^2 & \Delta f \geq f_{PLL} \end{cases}. \tag{3.1}$$

Furthermore, the integrated frequency noise of the PLL can be estimated by [80]

$$\mathrm{FN}_{PLL} = \sqrt{2 \cdot \int_{f_a}^{f_b} (\Delta f)^2 \cdot \mathcal{L}_{PLL}(\Delta f) \cdot d(\Delta f)}. \tag{3.2}$$

The lower integration bound f_a is set by the quantum operation cycle (worst-case: $1/T_2^* \approx 8.3\,\mathrm{kHz}$) and the higher limit is determined by the qubit operation speed (e.g. $10\,\mathrm{MHz}$). From Eqs. (3.1) and (3.2), the FN can be calculated as:

$$\mathrm{FN}_{PLL} = \sqrt{\alpha \cdot \left(2f_b - f_{PLL}\left[\frac{4}{3} + \frac{2}{3}\left(\frac{f_a}{f_{PLL}}\right)^3\right]\right)} < 1.9\ \mathrm{kHz} \quad (f_a < f_{PLL} < f_b). \tag{3.3}$$

By considering a typical PLL bandwidth of $300\,\mathrm{kHz}$ and exploiting Eq. (3.3), α is calculated to be lower than $0.2\,\mathrm{Hz}^2/\mathrm{Hz}$. This translates to the in-band PN of $-115\,\mathrm{dBc/Hz}$ and oscillator's PN of $-147\,\mathrm{dBc/Hz}$ at $10\,\mathrm{MHz}$ offset from the carrier. The in-band phase noise can be easily achieved by employing an integer-N sub-sampling PLL architecture [81] with a $50\,\mathrm{MHz}$ reference clock ($-155\,\mathrm{dBc/Hz}$ noise floor).

3.2.1. Impact of cryogenic operation

The advantages of operating an oscillator at cryogenic temperatures have been outlined in Chapter 2. Due to the increase in the quality factor of the tank by a factor of two and the reduction in thermal noise of the active devices by one order of magnitude, one can achieve better phase noise performance. Even by considering these advantages, achieving the required out-of-band phase noise performance is challenging with traditional MOS cross-coupled LC oscillators [73].

Moreover, as indicated in Chapter 2, it has been observed that the input-referred flicker noise of MOS transistors remains unaffected at cryogenic temperatures. This effect in combination with the reduction in the thermal noise floor will increase the $1/f$ corner of transistors. Consequently, this may result in a much higher $1/f^3$ PN corner that can exceed the PLL's bandwidth, thus degrading the integrated FN. Therefore, an oscillator topology with a low $1/f^3$ PN corner is desired. Finally, as mentioned before, the power consumption of the control electronics is severely limited by the cooling power of the dilution refrigerator. Hence, a power-efficient oscillator topology with a high figure-of-merit (FoM[1]) is essential.

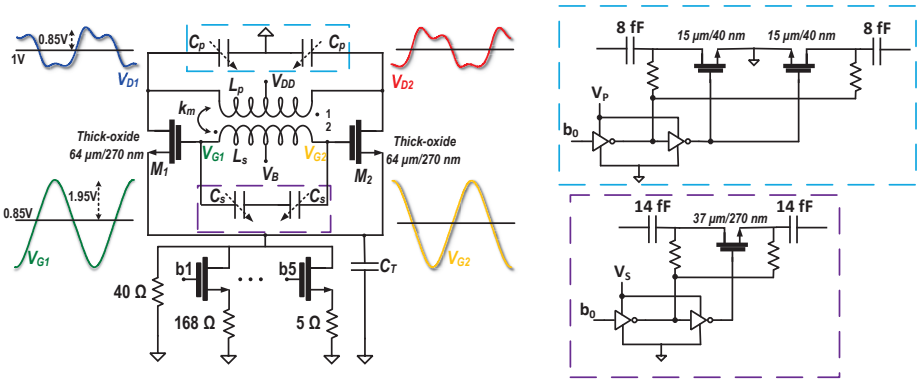


Figure 3.1: Class-$F_{2,3}$ oscillator with simulated waveforms. Switched capacitors are shown in detail.

3.3. Digitally Controlled Oscillator

The aforementioned issues can be addressed using a transformer-based class $F_{2,3}$ oscillator [82]. It is an extension of a class-F_3 oscillator [64] which introduces an auxiliary impedance peak $\omega_{1,DM}$ around the third harmonic of the fundamental differential mode (DM) oscillation frequency ($\omega_{1,DM} = 3\omega_{0,DM}$) in order to convert the third harmonic of the active device current into voltage, thus creating a pseudo-square oscillation waveform. As a result, the oscillator's impulse sensitivity function is reduced especially when the g_m-devices enter the triode region and inject large noise into the tank. Consequently, thermal-to-phase noise upconversion is lower in this operation. On the other hand, to reduce the flicker noise upconversion, the oscillator tank should exhibit an auxiliary common-mode (CM) resonance at the second harmonic of the fundamental DM oscillation frequency $\omega_{CM} = 2\omega_{0,DM}$ [82, 83]. As discussed in [84], this class-F_2 operation can be realized by exploiting the different behavior of the transformer at CM and DM excitation.

To exploit the advantages of both operations, a class-$F_{2,3}$ oscillator exhibiting two DM resonances and one CM resonance was thus designed. This was achieved by careful design of the inductance values of the primary (L_p) and secondary (L_s) windings of a step-up (1:2) transformer, along with single-ended primary (C_p) and differential secondary capacitor banks (C_s). In the proposed transformer, the common-mode input signal can neither see the secondary winding of the transformer nor the C_s tuning capacitors. Consequently, single-ended switched capacitors are required to obtain the desired CM resonance. However, differential capacitors are employed at the secondary, due to their higher Q-factor in the ON-state. For this particular design, the class-$F_{2,3}$ operation is satisfied with $L_s C_s = 3.8 L_{p,d} C_p$ for a coupling factor (k_m) of 0.67.

The channel resistance of long-channel-length MOS devices significantly reduces

[1] FoM = $|PN| + 20 \cdot \log_{10}\left(\frac{f_0}{\Delta f}\right) - 10 \cdot \log_{10}\left(\frac{P_{DC}}{1\,\text{mW}}\right)$

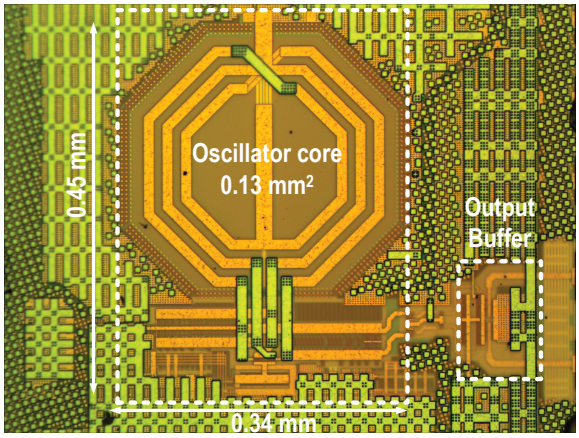


Figure 3.2: Chip micrograph of the 40-nm CMOS class-$F_{2,3}$ oscillator.

in the kink region observed in various CMOS technology nodes including 160-nm[27]. If the g_m-devices are biased in this region, they significantly load the tank at the oscillation zero-crossings, degrading the effective Q-factor and PN of the oscillator. Even though the nominal V_{DD} of thick-oxide devices is 2.5 V in this technology, the oscillator's V_{DD} is chosen as 1 V to limit the oscillation swing at the drain nodes to avoid this probable kink region. However, a 1:2 step-up transformer is employed to boost the oscillation voltage at the gate nodes where most of the tank capacitance is located, consequently improving the oscillator's PN and its start-up margin. The schematic and the oscillation waveforms are shown in Fig. 3.1. At the bottom of the core g_m transistors, a 5-bit binary-weighted switchable resistor with an LSB of $5\,\Omega$ is implemented to roughly control the oscillator current. The single-ended primary and differential secondary capacitor banks are realized using two 6-bit switchable metal-oxide-metal (MoM) capacitors with an LSB of $5\,\mathrm{fF}$ and $10\,\mathrm{fF}$, respectively. Due to the class-F operation, a pseudo-square waveform is realized at the drain of the g_m-devices. However, the transformer filters out the harmonic components of the drain oscillation voltage and so a sinusoidal waveform is restored at the gate.

The oscillator was prototyped in a 40-nm 1P7M CMOS process with an ultra-thick metal layer. The chip micrograph is shown in Fig. 3.2. The oscillator performance was characterized across a wide temperature range from $300\,\mathrm{K}$ to $4\,\mathrm{K}$. As illustrated in Fig. 3.3, the measurement setup consists of a hollow steel pipe where the device under test is mounted at one end, while the other end features the connectors to interface with the instruments at room temperature. This pipe is dipped into a helium barrel and its immersion depth inside the barrel is adjusted to obtain the required temperature. The oscillator's temperature is monitored using a sensor mounted on the backside of the PCB, right under the chip. A comprehensive investigation of discrete components on the PCB was done for proper measurement of the chip at cryogenic temperatures. As outlined in Chapter 2, the capacitance of widely used X5R and X7R capacitors would reduce by almost $90\,\%$ and their effective series resistance would

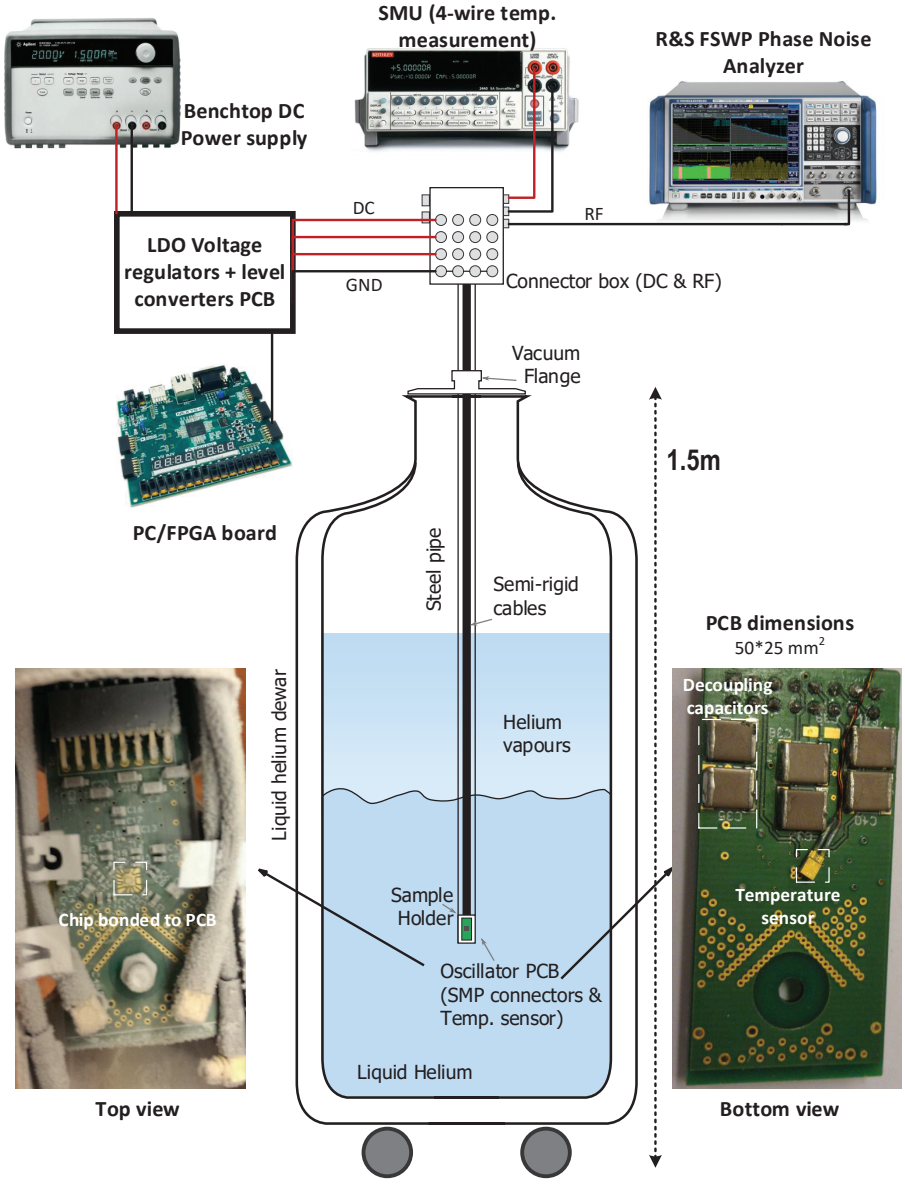


Figure 3.3: Oscillator measurement setup for temperature sweep.

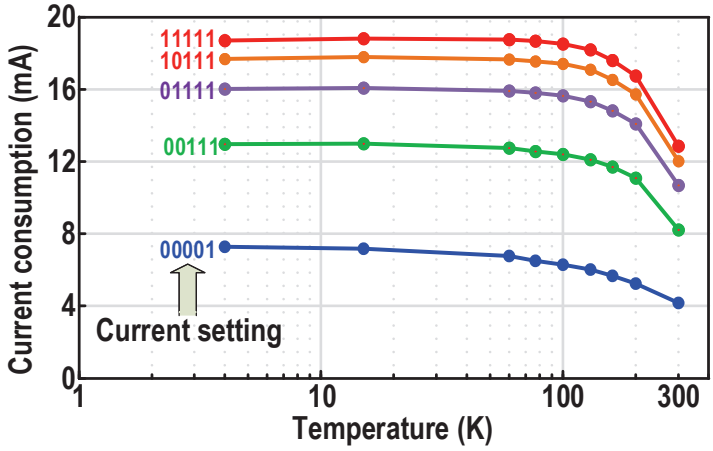


Figure 3.4: Oscillator current consumption versus temperature.

increase at least 10×. Hence, NP0 and COG type capacitors are employed on this PCB (see Fig. 3.3) with values ranging from $47\,\mathrm{pF}$ to $100\,\mu\mathrm{F}$, apart from an on-chip decoupling capacitor of $27\,\mathrm{pF}$. NP0/COG capacitors are available up to a value of $1\,\mu\mathrm{F}$ and are much larger in dimension than commercially available X5R or X7R capacitors, due to lower dielectric constant. Moreover, due to internal space constraints of the dilution refrigerator, capacitors above $1\,\mu\mathrm{F}$ have to be electrolytic, although they work rather poorly at cryogenic temperatures [85].

Fig. 3.4 reveals that, for any fixed switched-resistor configuration, the oscillator dissipates more power at lower temperatures. One of the reasons is the increase in electron mobility at colder temperatures, as justified in Chapter 2. Another reason is a reduction in resistance of the poly resistors ($10\,\%$ from $300\,\mathrm{K}$ to $4\,\mathrm{K}$) that are used

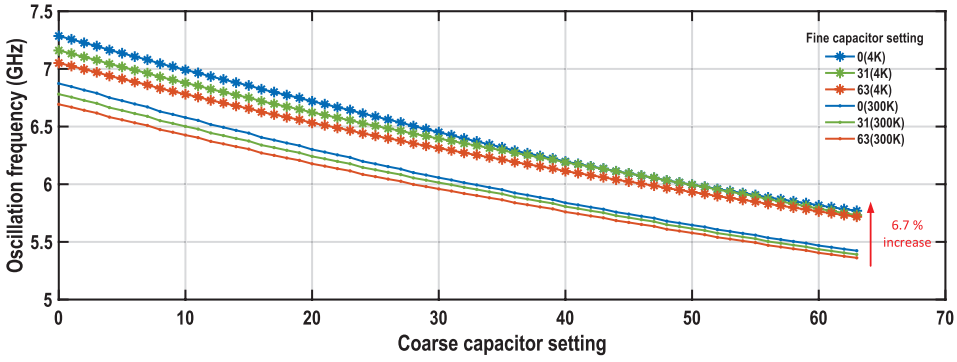


Figure 3.5: Oscillation frequency versus coarse tuning capacitor setting at $300\,\mathrm{K}$ and $4\,\mathrm{K}$.

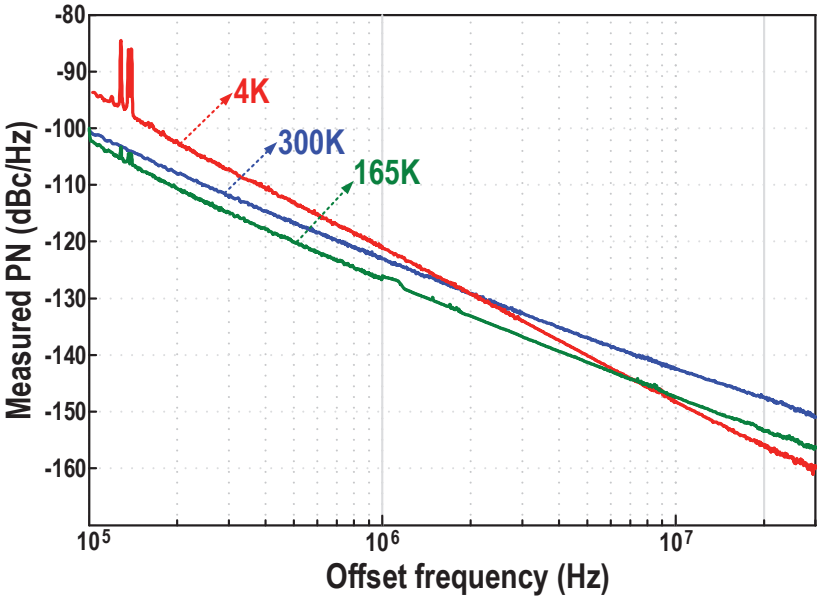


Figure 3.6: Measured phase noise at 6.3 GHz at various temperatures.

to control the oscillator's current. It is also observed that the oscillation frequency shifts up $\sim 7\,\%$ from $300\,\mathrm{K}$ to $4\,\mathrm{K}$, although the frequency span is largely maintained, as shown in Fig. 3.5 for different values of the coarse and fine-tuning capacitance. This complies with the measurement results of a resonator wherein the resonance peak shifts towards higher frequencies by $8\,\%$, as described in Chapter 2.

The measured PN plot is shown in Fig. 3.6 for different temperatures at the same power consumption, P_{DC}. The level of the spurs, especially at low offset frequencies, increases at cryogenic temperatures, indicating the inability of on-board decoupling capacitors to filter supply noise [86]. This issue has been addressed in future designs by implementing discrete component based LDOs on PCB and using additional decoupling capacitors to compensate for the capacitance degradation at $4\,\mathrm{K}$ [85], as will be described in Chapter 5.

Fig. 3.7 shows the oscillator PN in the thermal noise region at $\Delta f = 30\,\mathrm{MHz}$ offset frequency versus temperature, again at a constant P_{DC}. To better understand this plot, it is instructive to analyze the variation of temperature-dependent terms in the PN equation [87]

$$\mathcal{L}(\Delta\omega) = 10 \cdot \log_{10}\left(\frac{k_B T}{2} \cdot \frac{1}{Q^2 \cdot \alpha_V \cdot \alpha_I \cdot P_{DC}} \cdot \left(\frac{f_0}{\Delta f}\right)^2 \cdot (1+\gamma)\right) \tag{3.4}$$

where, α_I and α_V are the oscillator's current and voltage efficiency, respectively. Note that these parameters are mainly dependent on the oscillator topology; they are

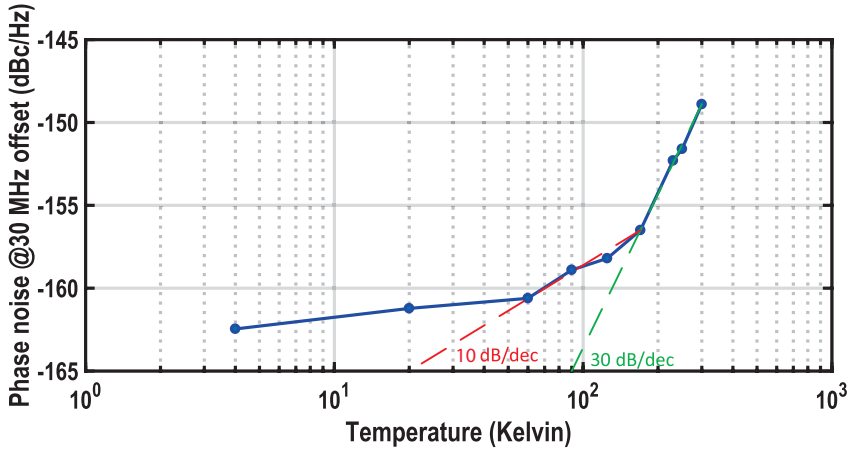


Figure 3.7: Phase noise at 30 MHz offset from a 6.3 GHz carrier versus temperature.

only weakly dependent on temperature. From 300 K to 170 K, the PN improves by 30 dB/dec, out of which 10 dB/dec is attributed to the temperature reduction, while the tank's Q-factor enhancement realizes the remaining 20 dB/dec. At room temperature, magnetically induced image currents from the tank flow in the low-resistive substrate, reducing the quality factor. A higher metal conductivity and consequently, a quality factor improving linearly with lowering of temperature is expected. Based on the measurement results of an inductor in Chapter 2, at cryogenic temperatures, a highly resistive substrate and a reduced metal resistance boost the tank's Q-factor. However, from 300 K to 4 K, the increase in conductivity of metal is only a factor of 5× and consequently a peak Q-factor improvement of 2.7× only. These factors highly depend on the purity of the metal used for the design of inductors [88]. Hence, the PN improvement as a function of temperature reduces below 170 K. Moreover, it can be observed that the phase noise at 30 MHz offset does not improve linearly with the temperature below 70 K. This could be attributed to a higher temperature in the conductive channel of the devices than the ambient temperature, as explained in Chaper 2.

Even though the flicker noise upconversion is significantly suppressed by virtue of the chosen topology, the oscillator's $1/f^3$ PN corner increases dramatically at lower temperatures, as shown in Fig. 3.8. As mentioned in Chapter 2, due to a reduction in thermal noise floor and no change in flicker noise, a larger 1/f noise corner for MOS transistors at cryogenic temperatures is expected. Another reason could be the worsening of mismatch [63] between the two core transistors at cryogenic temperatures, resulting in an asymmetric rise/fall times of oscillation waveforms and, consequently, resulting in a larger DC value of the impulse sensitivity function and higher flicker noise upconversion [89].

As discussed in Chapter 2, the parasitic capacitance of MoM capacitor and inductor varies at cryogenic temperature due to a highly resistive substrate. Consequently, although all the MoM capacitors employed would change by the same factor, due to

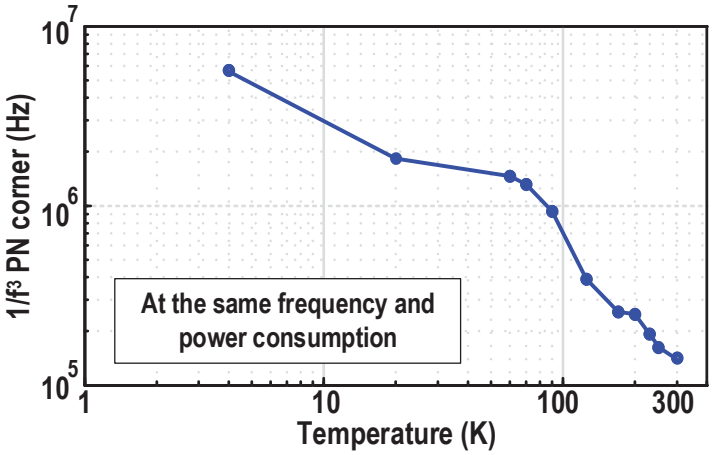


Figure 3.8: Oscillator 1/f³ phase noise corner versus temperature for a carrier frequency of 6.3 GHz

the variation in single-ended parasitic capacitances, the possibility of violation of class-F2 operation due to an imbalance between single-ended and differential capacitance cannot be neglected. Note that the common-mode resonance was adjusted by manually controlling the ratio of single-ended to differential mode capacitance. This is cumbersome to achieve while tracking PVT variation in harsh conditions such as cryogenic temperatures.

For completeness, the phase noise values at $4\,\mathrm{K}$ at different offset frequencies across the tuning range are plotted in Fig. 3.9.

Even without a PLL, the FN of the proposed oscillator is as low as $3.4\,\mathrm{kHz}RMS$, over a worst-case integration bandwidth of $8.3\,\mathrm{kHz}$ to $10\,\mathrm{MHz}$. Hence, by using, for example, a sub-sampling (digital or analog) PLL with a bandwidth of $\leq 1\,\mathrm{MHz}$, the

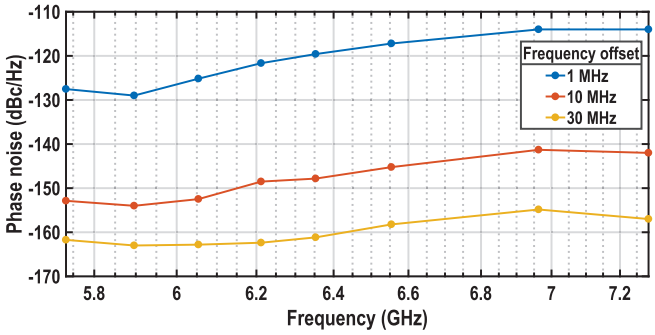


Figure 3.9: Phase noise at $4\,\mathrm{K}$ across tuning range at different offset frequencies from the carrier.

desired integrated FN of $1.9\,\mathrm{kHz}_{RMS}$ can be easily achieved.

3.4. Conclusion

This chapter describes the experimental validation of a cryogenic oscillator critical for the implementation of a CMOS classical electronic controller to operate at cryogenic temperatures. We have demonstrated a 4-K 40-nm 6-GHz class-$F_{2,3}$ oscillator with integrated frequency noise of $3.4\,\mathrm{kHz}_{RMS}$ over $\sim 10\,\mathrm{MHz}$ bandwidth, which is low enough to drive state-of-the-art qubits without limiting their performance.

Following this work, several cryogenic oscillators have been proposed for quantum computing applications. A ring oscillator operating at $110\,\mathrm{mK}$ and has been used for the excitation of quantum dots [90]. To tackle the challenge of manual capacitance ratio adjustment for optimum phase noise performance while tracking PVT variation in harsh conditions, an automated common-mode resonance calibration technique has been shown to work at $4.2\,\mathrm{K}$ [91]. Moreover, a dynamic amplifier based PLL has been shown to operate at $4.2\,\mathrm{K}$ [92].

4

System-level modeling of a single-qubit gate controller

Background: *In the previous chapter, the essence of cryogenic CMOS device modeling for optimized circuit design was proved by predicting the performance of a cryogenic RF oscillator. Similarly, to design a power-optimized qubit controller, the signal specifications need to be analyzed and the controller should be modeled with qubit Hamiltonian to obtain accurate controller specifications for the required gate fidelity.*

Abstract: *The main aim of this chapter is to obtain the detailed system-level specifications for a qubit controller to design a power-efficient chip while achieving a* $99.99\,\%$ *control fidelity. This work presents the first systematic design of a power-optimized controller for high-fidelity multi-qubit control. Signal specifications necessary for high-fidelity qubit control are outlined from the prior art. A controller model with various non-idealities (quantization, noise, linearity) is developed and simulated with a qubit Hamiltonian simulator to obtain a single-qubit gate fidelity of* $99.99\,\%$*.*

Summary: *This chapter is comprised of 5 sections. The performance of various types of qubit control systems is elaborated in Section 4.1. Section 4.2 elaborates on qubit control signal requirements using a microwave drive focusing on spin qubits and transmons. Next, the trade-offs between several transmitter/signal generator architectures are considered in Section 4.3, to assess the compatibility with qubit control requirements. A qubit control architecture is proposed and the system level specifications of each circuit block are derived in Section 4.4, followed by a conclusion in Section 4.5.*

Parts of this chapter have been published in *IEEE Transactions on Circuits and Systems I: Regular Papers* [93]. This work is equally contributed by J. van Dijk and the author to develop the models used for simulation.

4.1. Introduction

As discussed in Chapter 1, spin qubits encode the quantum state in the spin of a single electron and are realized in quantum processors operating at mK temperatures. Hence, quantum states are quite fragile and susceptible to thermal noise from the environment. Consequently, the signals provided to control these qubits should adhere to strict specifications to avoid the demolition of quantum state by control electronics.

Control and readout integrated circuits implemented in standard CMOS technology and operating at cryogenic temperature (cryo-CMOS) as low as 4 K and even below, promise a scalable solution to tackle the interconnect bottleneck between qubits and control electronics [27, 29]. However, the operation of a controller at cryogenic temperatures imposes restrictions on the power consumption of the chip, limited by the cooling power of a dilution refrigerator. Hence, the control electronics not only has to adhere to the strict signal specifications but also be power-efficient to scale up to a controller for millions of qubits while operating inside a dilution refrigerator. To design such systems, accurate circuit specifications need to be estimated/simulated to produce a power-efficient design.

In this chapter, the above-mentioned issues are addressed by proposing a systematic design technique of the electronic controller. First, a design guide is offered to map the signal specifications for high-fidelity single-qubit operations to a power-efficient direct digital synthesizer (DDS) based controller architecture. A co-simulation between the model of the controller and a 32-qubit quantum processor provides accurate circuit specifications to achieve a single-qubit gate fidelity up to 99.99 %.

4.2. Control Signal specifications

Before diving into the signal and circuit specifications required for spin qubit control, a basic understanding of the operation of spin qubits is required as summarized in the following subsection.

4.2.1. Basics of spin qubit control

Coherent control of spin qubits in silicon can be realized using several methods such as single electrons confined in Si/SiGe [94] or SiMOS quantum dots [77], single electrons bound to phosphorus dopants [95], etc. In the case of Si/SiGe quantum dots, electrons are confined as two-dimensional electron gas (2DEG) at the interface of two different materials (semiconductor *heterostructure*), leveraging the difference of the level of conduction band minima [96]. The application of voltages to the surface gate electrodes creates additional confinement potential within the 2DEG, thus realizing *quantum dots*, which are isolated areas where an electron/electrons can be confined. The realization of a spin qubit device using quantum dots will be elaborated in Chapter 6.

The complete operation of a spin qubit processor can be divided into three steps. First, the qubit is initialized to a known state, followed by manipulation of the state or execution of a quantum gate, and finally, the readout of the state using projective

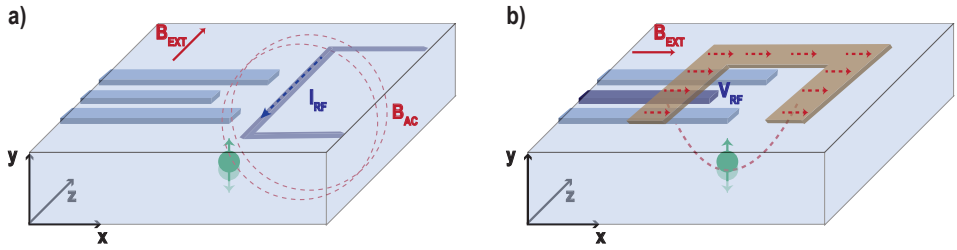


Figure 4.1: Manipulation of spin qubit using two different methods. An oscillating magnetic field (B_{AC}) is produced perpendicular to an external magnetic field (B_{EXT}) using (a) a microwave current (I_{rf}) applied to a looped transmission line in ESR or (b) a microwave voltage signal (V_{rf}) applied to an open-ended transmission line in EDSR.

measurement.

Electron spin states can be manipulated using two different methods (see. Fig. 4.1):

- **Electron Spin Resonance (ESR)**: The transition between two spin states (up/down) is induced by applying an alternating current (I_{RF}) which produces an oscillating magnetic field (B_{AC}) orthogonal to the external magnetic field (B_{EXT}) with an energy equal to the difference between the two spin states i.e. Zeeman energy.
- **Electron Dipole Spin Resonance (EDSR)**: The application of a microwave signal (V_{RF}) to an open-ended transmission line induces a local oscillating electric field. If the frequency of the microwave signal is on resonance with the qubit frequency determined by B_{EXT} and micromagnet (brown region in Fig. 4.1b), the electron is subjected to an oscillating magnetic field in the y-direction, which induces EDSR.

To independently address each qubit in a multiple quantum dot array, the Zeeman energy (E_z) of each electron should differ given as $E_z = g\mu_B B_0$, where g is the g-factor of the electron, μ_B represents the Bohr magneton, B_0 is the external static magnetic field. The g-factor is defined as the index of the ratio of the electron's magnetic moment to its spin angular momentum. A gradient in E_z can be achieved by creating a gradient either in the g-factor of each electron by exploiting the Stark shift [71] or the local magnetic field felt by each electron. Micromagnets implanted on the device (brown region in Fig. 4.1b) can produce such a magnetic field gradient and hence the associated qubit resonant frequency given as $\nu = E_z/h$, where h is the Planck constant (see. Fig. 4.1).

Frequency multiplexing

Controlling multiple qubits by way of using the same driveline can decrease the number of interconnects and potentially reduce the area and power consumption of the control electronics. This would require the implementation of various multiplexing techniques both at the qubit level and interface electronics. Frequency multiplexing enables multi-qubit control without introducing any latency between the execution of qubit gates as in the case of time-domain multiplexing. However, it demands careful

frequency planning and modulation techniques to contain the energy applied to driven qubits in the required band. Pulse shaping can be used to minimize spectral leakage into adjacent qubits and prevent unintended X/Y rotations on the victim qubit [97].

Although pulse shaping can prevent the energy from leaking into adjacent qubit channels, off-resonance pulses also causes an unintended Z-rotation on the victim qubit known as AC-Stark shift. This unintended Z-rotation is equivalent to a phase offset and can be corrected by applying additional compensating phases to the consequent pulses *if* the victim qubit is in an idle state [97]. However, when multiple qubits are addressed simultaneously using the same driveline it is not sufficient to apply a compensating Z-rotation *after* the operation. Considering an example of two qubits, if both qubits are operating at the same time, two tones are simultaneously applied. As the Z-rotation on qubit-1 is incurred during its own operation due to the simultaneous application of an off-resonance pulse (drive pulse on qubit-2), the driving pulse of qubit-1 should be engineered to compensate for the Z-rotation *incurred during the operation*. This would demand complex pulse engineering when microwave pulses are applied to simultaneously execute quantum gates on multiple qubits [97].

4.2.2. System requirements

The typical frequency and duration of microwave pulses for spin qubit control are 12-40 GHz and $\sim 1\,\mu$s, respectively. To obtain a Rabi frequency[1] of 1 MHz, ~ -45 dBm power is required [98, 99, 100, 12]. Qubits operating at a higher temperature ~ 1 K promise integration with cryogenic control electronics, require relatively lower operating frequency [16]. Future systems would target higher Rabi frequencies for faster qubit gates [16]. Hence, the system presented here targets an output frequency range of 5-20 GHz, and Rabi frequencies in the range of 1-10 MHz, with a maximum rotation angle of π. Consequently, the nominal duration of a π-rotation is 50-500 ns and output power ranges from -45 dBm to -25 dBm. The use of cryogenic attenuators to reduce the noise temperature at various stages of a dilution refrigerator and the inherent loss of microwave cables attenuate the signal by around 6 dB from control electronics to qubits. Moreover, due to chip-to-chip mismatch between qubit devices, the response of the qubits to microwave signal power can vary causing a Rabi frequency variation of $\pm$50%. To compensate for the losses and variations, the required output power range is extended as -48 dBm to -16 dBm ($50\,\mathrm{mV}_p$).

Most single-electron spin-qubit processors typically do not employ frequency multiplexing, and hence, rectangular envelopes are used for microwave pulses [12, 98]. However, to support frequency multiplexing in this system, more complex pulse shaping e.g., Gaussian envelopes, is targeted. The use of I/Q modulation facilitates the flexibility to have X/Y rotation using the same envelope.

The gate fidelity metric quantifies the accuracy of a qubit operation. Single-qubit control has been demonstrated to achieve gate fidelities exceeding 99.9 % [99]. Moreover, fault-tolerant quantum computing employs error-correcting algorithms which require a minimum qubit fidelity of around 99.9 % [76]. Assuming a perfect qubit, the proposed electronic interface targets a fidelity of 99.99 % for a π-rotation (which

[1] The speed of qubit rotation around X/Y axis. Refer Section 4.2.3.

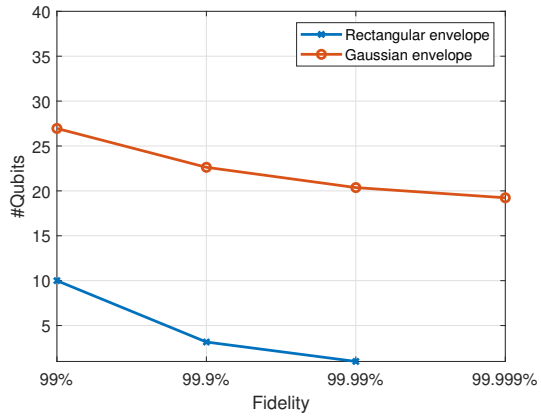


Figure 4.2: The effect of pulse shaping on the number of addressed qubits in a 1 GHz band, for frequency-multiplexed control at $10\,\mathrm{MHz}$ Rabi frequency.

generally gives the lowest fidelity [96]), taking into account only the errors due to the electronic interface. To support frequency multiplexing, the control fidelity is targeted for a π-rotation on the addressed qubit while the unaddressed qubits reach a $99.99\,\%$ for identity (idle) operation.

Frequency multiplexing demands a wide data bandwidth for the controller to support multiple qubits while minimizing crosstalk. Fig. 4.2 shows the number of qubits that can be multiplexed in a $1\,\mathrm{GHz}$ bandwidth for different microwave pulse envelopes, assuming uniformly distributed qubit frequencies, π-rotation at a Rabi frequency of $10\,\mathrm{MHz}$ and corrections of the unintended Z-rotation caused by AC-Stark shift [97]. To achieve a $99.9\,\%$ fidelity using a rectangular envelope, less than 5 qubits can be accommodated in such a bandwidth. Pulse shaping e.g. Gaussian pulses can be used to minimize the spectral leakage, accomodating ~20 qubits in a $1\,\mathrm{GHz}$ bandwidth. For easier addressing of qubits in a digitally programmable system and a theoretical fidelity $>99.999\,\%$, 32 qubits ($32 = 2^5$) are targeted in a $2\,\mathrm{GHz}$ bandwidth.

Simultaneous high-fidelity control of multiple qubits using the same driveline requires complex pulse engineering apart from Z-correction, as mentioned in Section 4.2.1. Hence, the system specifications are optimized assuming sequential operations on different qubits. However, the system architecture is developed to support simultaneous excitation of multiple qubits.

Transmon control pulse requirements

Although the signal specifications for the control of transmons are quite similar to spin qubits, there are a few key differences. The frequency of microwave pulses for manipulating the state of transmons is typically around 6 GHz, with a pulse duration of ~20 ns and a signal power of ~ -60 dBm. Consequently, the duration and output power specifications of the system are extended to support transmons. Moreover, pulse shaping i.e. Derivative Removal by Adiabatic Gate (DRAG) is typically used to minimize spectral leakage to higher energy levels of the same qubit. DRAG pulses

Table 4.1: Requirements of the multi-qubit controller.

Qubit	Technology	Target single electron spin-qubits while supporting transmons
	Frequency range	5 GHz to 20 GHz
	Rabi frequency range	1 MHz to 10 MHz
	Output power range	-60 dBm to -16 dBm
FDMA	Bandwidth	2 GHz
	Number of qubits	32
	Parallel operations	Supported
Operation	Maximum angle	π
	Duration	50 ns to 500 ns
	Modulation	I/Q-modulation with any envelope
Fidelity	Addressed qubit	99.99 % for a π-rotation on a spin-qubit
	Idle qubit	99.99 % for identity operation
	Power consumption	Minimize

require I/Q modulation, which is already supported by the system. Finally, as state-of-the-art transmons typically achieve gate fidelities lower than $99.99\,\%$ [101], the control system will still not limit the achievable fidelity.

The final requirements of the system targeting both spin-qubits and transmons are summarized in Table 4.1.

4.2.3. Signal specifications

The specification of the microwave signals required to achieve high-fidelity single-qubit gates has been derived in [102]. The procedure of obtaining those specifications is summarized in this subsection.

The time-dependent Schrodinger equation describes the evolution of the quantum state of a physical system as:

$$i\hbar \frac{\partial \left|\psi(t)\right\rangle}{\partial t} = H \left|\psi(t)\right\rangle \tag{4.1}$$

where $\hbar$ is the reduced Planck constant, $\left|\psi(t)\right\rangle$ is the wave function representing the probability amplitude of the quantum state, $i\hbar \frac{\partial}{\partial t}$ is the energy operator and H is the Hamiltonian operator.

The Hamiltonian of single electron under microwave excitation in the lab frame is given as:

$$H_{lab} = \omega(t).\frac{\sigma_x}{2} - \omega_0.\frac{\sigma_z}{2} \tag{4.2}$$

where ω_0 is the Larmor frequency, σ_x and σ_z are the Pauli matrices, $\omega(t)$ is a microwave signal applied to the qubit described as $\omega(t) = 2.\omega_R.\cos(\omega_{mw}t + \phi)$. ω_{mw}, ϕ and ω_R are the frequency, phase and amplitude of the microwave signal respectively. For static control signals, the Hamiltonian is time-independent, which can be obtained by moving to a reference frame that rotates with a frequency ω_{mw} around

the z-axis. In this rotating frame, the time-independent system Hamiltonian can be described as [96]:

$$H = \omega_R \left(\cos\phi . \frac{\sigma_x}{2} - \sin\phi . \frac{\sigma_y}{2} \right) + (\omega_{mw} - \omega_0) . \frac{\sigma_z}{2} \tag{4.3}$$

A unitary operation (U) describing the evolution of the qubit state can be computed from the Hamiltonian as $U = e^{-\mathrm{i}.H.T}$. For an ideal microwave signal (ω_{mw}=ω_0) after time T, U can be computed as:

$$\begin{aligned} U_{ideal} &= e^{-\mathrm{i}.H_{ideal}.T_{ideal}} = e^{-i.\theta} \left(\cos\phi . \frac{\sigma_x}{2} - \sin\phi . \frac{\sigma_y}{2} \right) \\ &= \left(\cos\frac{\theta}{2} . I - \mathrm{i}.\sin\frac{\theta}{2} \right) (\cos\phi . \sigma_x - \sin\phi . \sigma_y) \end{aligned} \tag{4.4}$$

where I is the identity matrix and $\theta = \omega_R . T$ is the rotation angle and ϕ is the rotation axis. An inaccuracy in the Hamiltonian or the timing would result in a non-ideal unitary operation given as $U_{real} = e^{-\mathrm{i}.H_{real}.T_{real}}$. This could be due inaccuracy in amplitude (ω_R), phase (ϕ), frequency (ω_{mw}) or duration (T) of the microwave signal and would result in $H_{real} = f(\omega_0 + \Delta\omega_{mw}, \omega_{R,ideal} + \Delta\omega_R, \phi_{ideal} + \Delta\phi, T_{ideal} + \Delta T)$ and can be derived from Eq. (4.3).

To quantify the accuracy of a quantum operation, gate-fidelity is used as the metric which characterizes the agreement between actual operation (U_{real}) and desired result (U_{ideal}) of the operation acting on a specific pure state ρ. The state fidelity for comparing U_{real} and U_{ideal} is defined as [96]:

$$F = Tr|U_{real}(\rho), U_{ideal}(\rho))| \tag{4.5}$$

where Tr denotes trace of the matrix.

As an example, the gate fidelity due to an error in the microwave pulse amplitude which would cause an over or under rotation of the desired angle θ can be derived by substituting $\omega_R = \omega_{R,ideal} + \Delta\omega_R$ in Eq. (4.3) to obtain U_{real} and consequently calculating Eq. (4.5) using U_{real} and Eq. (4.4) as:

$$F = \cos^2 \left(\frac{\theta}{2} . \frac{\Delta\omega_R}{\omega_{R,ideal}} \right) \approx 1 - \frac{1}{4} . \theta^2 . \left(\frac{\Delta\omega_R}{\omega_{R,ideal}} \right)^2 \tag{4.6}$$

Similarly, the effect of other errors in the microwave pulse on gate fidelity has been derived in [102].

Following the above procedure, a MATLAB model is developed to simulate the system Hamiltonian with several non-idealities added to the microwave signal. The gate-fidelity is simulated for each of these non-idealities to compute the maximum tolerable noise and inaccuracies in the signal parameter for a certain target fidelity. In particular, the effect of noise and inaccuracies in microwave carrier frequency and phase as well as envelope amplitude and duration is considered. Moreover, since the system targets control of multiple qubits over a single cable using FDMA, the effect of an off-resonance tone on an idle unaddressed qubit is simulated to obtain the

Table 4.2: Signal specifications to achieve a 99.99 % control fidelity for a π-rotation

	Specifications	Rabi frequency	
		1 MHz	10 MHz
Addressed qubit	Phase imbalance (degrees)	0.20	0.20
	Frequency inaccuracy (kHz)	3.5	35
	Frequency noise (kHz_{rms})	3.5	35
	Duration inaccuracy (ns)	1.1	0.11
	Timing jitter (ns_{rms})	1.1	0.11
	Amplitude inaccuracy (mV)	0.011	0.11
	Amplitude noise (dB)	50	50
	Wideband additive noise ($nV/\sqrt{Hz}$)	5.6	18
Idle qubit	SFDR (dB)	-44	-44

required spurious-free dynamic range (SFDR) of the signal spectra for high fidelity single-qubit gates.

Signal specifications have been estimated for performing a π-rotation using a rectangular envelope at two different Rabi frequencies, as shown in Table 4.2. Equal contributions were assumed from all error sources, and the value given for the amplitude inaccuracy assumes a peak amplitude of $50\,\mathrm{mV}$ corresponding to the maximum required output power. These preliminary specifications can be used to assess the feasibility of various controller architectures. In a frequency-multiplexed control architecture, the most notable requirement is a high SFDR to prevent interference with unaddressed (idle) qubits.

Based on these signal specifications, we dive into the development of the system architecture and circuit specifications of the qubit controller in the rest of the chapter.

4.3. System Architecture Evolution

Based on the signal requirements for qubit control (Table 4.2), the feasibility of several architectures is discussed and the chosen architecture is presented in this section.

4.3.1. Analog/RF Section

To generate the required envelopes for frequency-multiplexed qubits, the simplest architecture would be to design a digital-to-analog converter (DAC) operating at $40\,\mathrm{GS/s}$, as shown in Fig. 4.3(a). However, the power consumption would be too high due to its large data bandwidth [103] since the sampling frequency is determined by the carrier frequency. For example, a $56\,\mathrm{GS/s}$ 6-bit DAC in $65\,\mathrm{nm}$ CMOS technology consumes around $0.75\,\mathrm{W}$ [103], which would consume almost one-third of the cooling power ($2\,\mathrm{W}$) provided by state-of-the-art dilution refrigerators at $4\,\mathrm{K}$. Hence, such a solution is not scalable to control millions of qubits.

A multiple-return-to-zero (MRZ) DAC [Fig. 4.3(b)] exploiting higher Nyquist zones is capable of synthesizing frequencies up to $20\,\mathrm{GHz}$ [104] using a sampling frequency

of $4\,\mathrm{GHz}$. Compared to the previous approach, this architecture decouples the sampling frequency from the carrier frequency thereby reducing the DAC sampling frequency and consequently, the power consumption. However, limited flexibility in choosing the output frequency band (centered around $N \cdot f_s$) and an output spectrum corrupted by DAC replicas does not make this a good candidate.

To overcome this, several low-speed DACs along with I/Q mixers can be used to generate envelopes at distinct frequencies [29] as shown in Fig. 4.3(c). This would severely reduce the sampling frequency which is determined by the bandwidth of one qubit and provide the possibility of having an individual RF channel/output per qubit. However, this would require multiple local oscillator (LO) signals, thus making it power/area inefficient for multi-qubit control. Moreover, on-chip implementation of multiple LOs can cause frequency pulling and affect the spectral purity of the synthesizers, thus degrading the transmitter SFDR. Instead, a very high-speed DAC at $4\,\mathrm{GS/s}$ and a single mixer can be used for controlling multiple qubits from a single RF cable [Fig. 4.3(d]). Such an architecture demands a DAC operating at twice the frequency of the required data bandwidth and produces an unwanted image tone due to double-sideband (DSB) modulation.

Single-sideband (SSB) modulation can be implemented instead of DSB modulation to obtain the same bandwidth with half the DAC sampling frequency at the cost of increased circuit complexity. This can be achieved by filtering each of the upper/lower sidebands (USB/LSB) and combining them at the output, as shown in Fig. 4.3(e). To achieve an image rejection ratio (IRR) $> 44\,\mathrm{dB}$ for output frequencies close to the carrier (as required by the SFDR specification), filters with very high order or quality factor are essential. Instead, image rejection can be achieved using a Hartley modulator with I/Q DAC and mixer at the cost of requiring an LO with quadrature phases. At the circuit level, instead of cascading the DAC and the mixer, a better solution would be to use a mixing-DAC, i.e. combining the DAC and mixer, for power efficiency and linearity [105]. Note that such an architecture does not contain a reconstruction filter. However, in a wideband system architecture when the data bandwidth is comparable to the carrier frequency, the sampling replicas at negative frequencies could fold back to positive frequencies and fall in-band, demanding a reconstruction filter with stringent specifications as addressed below.

Sampling replicas in wideband systems

To generate a tone at the lowest operating frequency of $5\,\mathrm{GHz}$, the lower sideband output can be used with a carrier frequency of $6\,\mathrm{GHz}$ and a data bandwidth of $1\,\mathrm{GHz}$. The simulated output spectrum of such a system is shown in Fig. 4.4. Positive and negative frequencies are indicated with blue and red dotted lines respectively to illustrate the origin of the unwanted tones that could fall in-band. It can be observed that for the chosen output frequency band, negative sampling replicas fold back to positive frequencies and can eventually fall in-band, dominating the output SFDR. Depending on the output frequency, the inherent filtering provided by the ZOH can only suppress these replicas by $21\,\mathrm{dB}$, in the worst-case scenario. To obtain the required SFDR of $54\,\mathrm{dB}$ corresponding to $99.999\,\%$ fidelity, an additional suppression of $33\,\mathrm{dB}$ is required at $11\,\mathrm{GHz}$. Note that, to obtain a $10\times$ smaller error, the required SFDR is $10\,\mathrm{dB}$ higher than the value mentioned in Table 4.2.

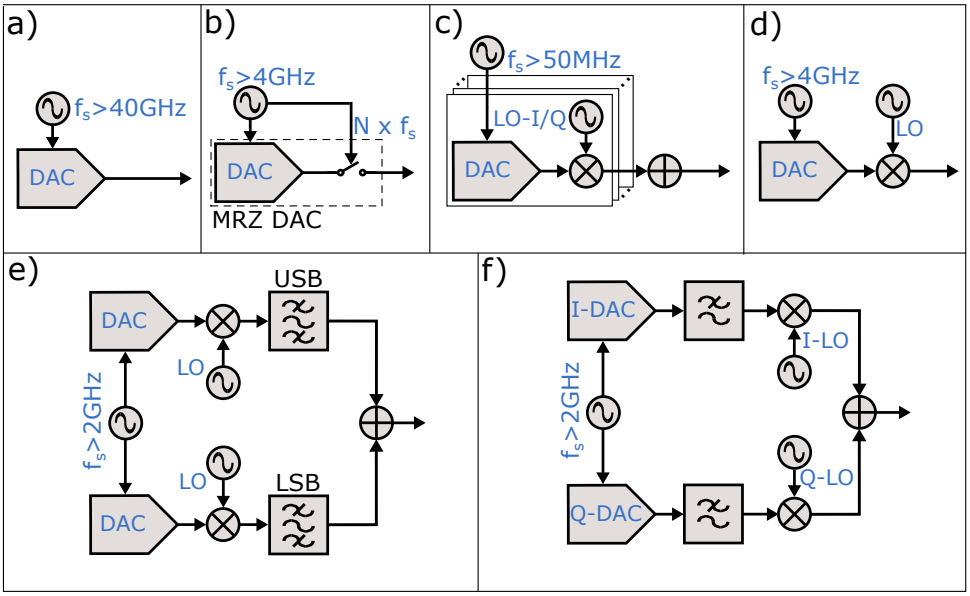


Figure 4.3: Possible transmitter architectures: (a) Very high-speed DAC, (b) MRZ DAC, (c) low-speed DAC with mixer, (d) high-speed DAC with mixer (e) SSB modulation with bandpass filters for the sidebands, (f) high-speed DAC with reconstruction filter and I/Q mixer.

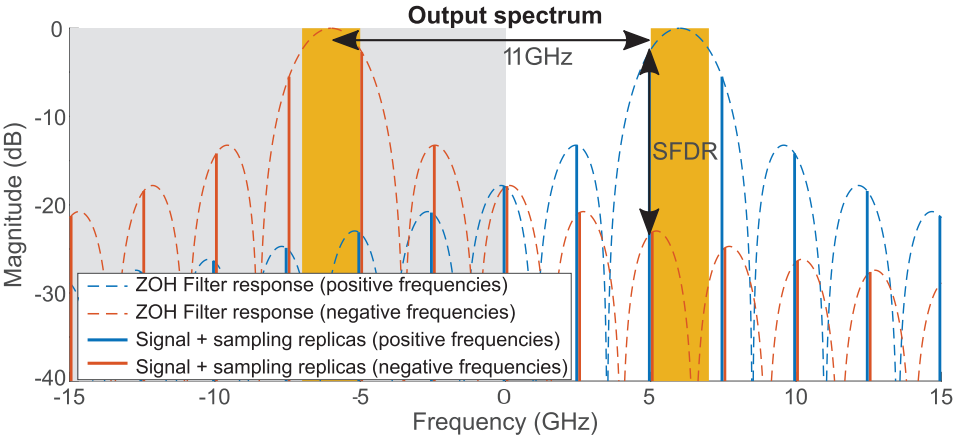


Figure 4.4: Output spectrum at the desired output frequency around 5 GHz without reconstruction filter, using a carrier frequency of 6 GHz and a sample rate of 2.5 GHz.

The required suppression can be achieved by using a 2nd order Chebyshev -I filter with a 3-dB passband ripple and a 1.8 GHz corner frequency. In combination with the ZOH, the filter provides an SFDR better than 58 dB in all conditions, resulting in a simulated fidelity >99.9996% for the idle qubit. To compensate for the sinc shaping of the ZOH and extend the usable bandwidth, wideband architectures use predistortion

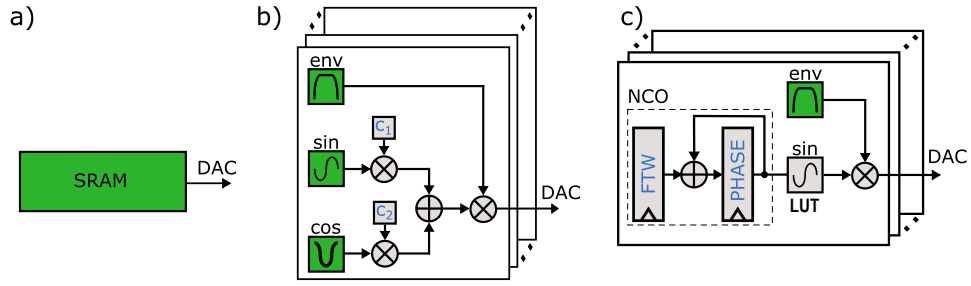


Figure 4.5: Possible backends: (a) SRAM for all possible instructions, (b) Reduced memory for on-chip modulation, (c) NCO-based modulation. The green blocks indicate programmable memories.

block at the input of the transmitter. Instead, an inverse sinc transfer function can be produced by the filter resulting in an in-band flatness of $0.14\,\mathrm{dB}$ in the $2\,\mathrm{GHz}$ data band.

Following the analysis above, a high-speed DAC followed by a reconstruction filter and a mixer is preferable for better spectral purity in wideband systems [Fig. 4.3(f)].

4.3.2. Digital Signal Synthesis

To generate multiple SSB-modulated tones with this front-end design, a digital back-end is required. This work assumes the availability of a reprogrammable on-chip memory to store calibrated waveforms for each of the desired qubit rotations. A qubit algorithm is then executed by playing the various stored waveforms in the desired order. The most straightforward approach is to store all possible combinations of qubits' instructions in an SRAM, as shown in Fig. 4.5(a). The required memory of such an SRAM can be estimated as $SRAM_{mem} = N \times f_s \times t_{pulse} \times m^n$, where N and f_s are the number of bits and the sampling frequency of the DAC, respectively, t_{pulse} is the pulse duration, m the number of possible instructions per qubit and n the number of qubits. Assuming an 8-bit DAC operating at $2.5\,\mathrm{GS/s}$ to address 32 qubits and a maximum pulse duration of 500 ns, it would require an impractically large memory of $3.7{\times}10^{19}$ bits, considering merely 3 instructions per qubit. Moreover, since qubits require coherent control, intermittent sequential operations on any qubit demand keeping track of the phase of all qubits. Consequently, an individual reference clock would be required for each qubit.

To reduce the required memory, an alternative approach is to store only the amplitude information in the SRAM, which can modulate the amplitude of a sinusoidal waveform with a programmable phase, as shown in Fig. 4.5(b). Under the mentioned assumptions, this would require less than 1-Mbit SRAM instead (scaling as $m \times n$ instead of m^n), consequently saving area at the cost of higher power consumption. To update the phase for each qubit and ensure coherent control, sine and cosine waveforms scaled by appropriate coefficients can be combined to generate the required phase offset. However, this adds an overhead of 2 multipliers per qubit running at the full sampling speed.

A power-efficient approach would be to use a Numerically Controlled Oscillator

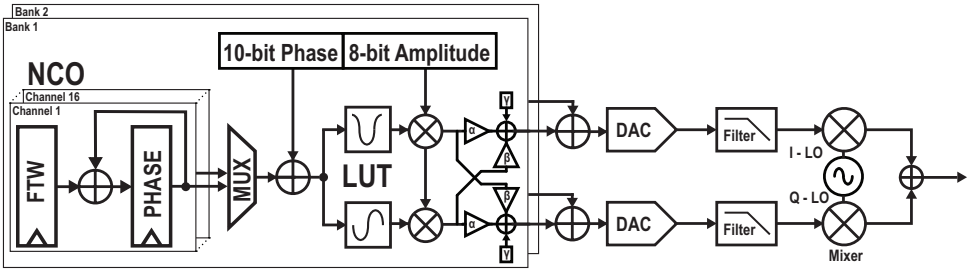


Figure 4.6: Block diagram of the proposed controller.

4

(NCO) for each qubit to generate both the required frequency and the phase offset [106]. An NCO consists of a phase accumulator running at f_s. An input frequency tuning word (FTW) defines the step size of the phase accumulator to generate the desired output frequency $f_{out} = FTW \times f_s/2^N$, where N is the number of bits in the phase accumulator. The sine Look-Up Table (LUT) generates a sinewave corresponding to the output phase of the NCO, which is then multiplied with an envelope (stored in the SRAM) to obtain the necessary modulated signal, as shown in Fig. 4.5(c). This allows for fewer multipliers and the same number of adders compared to Fig. 4.5(b), thereby saving substantial power, i.e., 2 multipliers per qubit running at $2.5\,\mathrm{GHz}$. Another advantage of such a system is that the NCO can keep track of the phase of individual qubits, thus allowing coherent operation [107].

4.3.3. Final Architecture

Considering the above-mentioned trade-offs, a digitally intensive architecture based on direct digital synthesis (DDS) with digital modulation, as shown in Fig. 4.6, has been selected. Such an architecture benefits from the scaling advantage of advanced CMOS technology nodes in terms of speed and power efficiency and offers the flexibility and robustness of digital signal processing.

Multiple NCOs are used to enable frequency multiplexing where each NCO keeps track of the phase evolution of a particular qubit. However, the NCO outputs are time-multiplexed (16:1) to allow operation on one qubit at a time to reduce the system complexity, as mentioned in Section 4.2. The multiplexed output from the NCOs containing phase information of a particular qubit is fed into LUTs to generate the respective sinusoidal signals. The envelope of output signals from the LUTs is then modulated by the amplitude memory and phase memory for various gate operations and pulse shaping [108, 109], providing flexibility in qubit control. Polar modulation is adopted as it allows to reduce the power consumption by saving two multipliers and an adder compared to quadrature modulation. Note that the LUTs can be implemented using ROM as they contain a sinusoidal amplitude value corresponding to a phase value.

Because of the stringent IRR requirement of $44\,\mathrm{dB}$ (originating from SFDR) corresponding to a maximum phase and gain imbalance of $0.3°$ and $0.1\,\mathrm{dB}$, respectively, an I/Q digital correction network (α, β) is required to compensate for the analog I/Q

mismatch. Moreover, a DC offset correction (γ) is added to cancel the LO feed-through to the output. The coefficients used in the I/Q calibration network are selected based on the active qubit channel, i.e. based on the output frequency band, to compensate for the frequency-dependent phase and gain imbalances in the analog circuit. The entire DDS block is replicated to two banks to allow for the simultaneous excitation of two qubits. The optimization of bit-widths of all the blocks is discussed in the following section.

Finally, the same transmitter as in Fig. 4.3(f), comprising I/Q DACs, a reconstruction filter, and an I/Q mixer, translates the digital input to the RF band. The only required analog input is then a quadrature LO signal to drive the mixers.

4.3.4. System simulation

In nanometer CMOS technologies, digital circuits dissipate relatively low power compared to analog circuits while increasing the signal dynamic range in a specific system architecture [110]. Alternatively, adding one-bit of amplitude information to a digital system dissipates less power compared to doubling the signal amplitude using the analog circuitry [110]. Hence, the error budget of the digital section can be set to a higher threshold (99.999%) to minimize its contribution towards the target fidelity.

A MATLAB simulation model of the system is developed, including several non-idealities in the digital circuitry such as quantization, bit-width rounding effects, and ideal analog circuit blocks. This is used to drive a Hamiltonian-based model of a 32-qubit quantum processor, to quantify the effect of each error source on the gate fidelity. All the fidelity calculations presented in this work are based on a rectangular envelope, while the simulations consider both rectangular and Gaussian envelopes. Since a higher Rabi frequency (f_R) usually demands more stringent specifications on the controller, all calculations/simulations assume $f_R = 10\,\mathrm{MHz}$, unless specified otherwise. Additionally, as the adverse effect of DAC sampling replicas worsens at low frequencies, the simulator uses the lowest output frequency band i.e. 5-7 GHz. As unintended Z-rotations can be corrected in software [111], such errors are ignored while simulating idle qubits.

4.4. Circuit Specifications

The back-end of the controller architecture is made digitally intensive for flexibility in programming and to leverage power consumption scaling in lower technology nodes. The operation of each digital circuit block is simulated to obtain the required specifications. The commonly used technique of limiting the bit-width in a digital system to reduce the power consumption comes at the cost of spectral purity. This is quantified by simulating the effect of a limited bit-width of each digital cell on the gate fidelity while keeping all other cells ideal. Finally, the obtained specifications of each cell are included in the final system to verify whether the target fidelity can be achieved at the system level, as shown in sub-section Section 4.4.7.

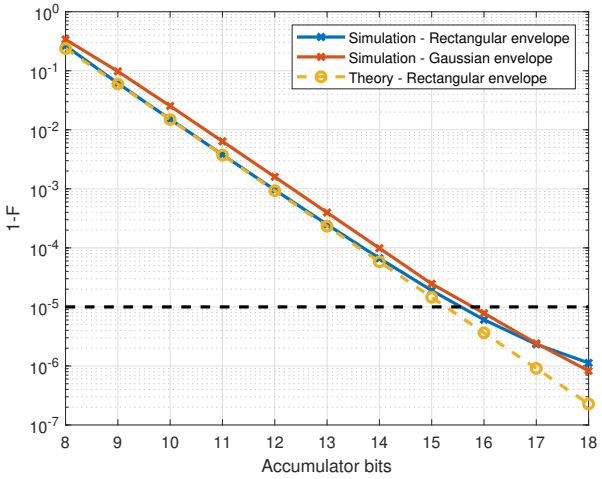


Figure 4.7: Infidelity of a π-rotation versus the number of bits in the phase accumulator register. Comparison between theory and simulation is presented for Gaussian and rectangular envelopes.

4.4.1. Sampling rate

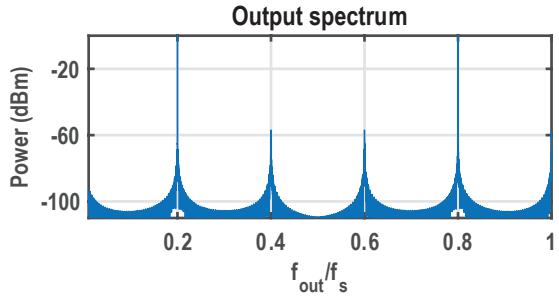
Due to the use of an SSB architecture, a $1\,\mathrm{GHz}$ baseband bandwidth would result in a $2\,\mathrm{GHz}$ RF bandwidth thanks to individual control over upper and lower sidebands. As per the Nyquist criteria, to achieve a $1\,\mathrm{GHz}$ data bandwidth, a DAC sampling rate of at least $2\,\mathrm{GS/s}$ is required. However, the inherent zero-order hold (ZOH) operation in a DAC imposes a 3-dB bandwidth of 0.4 $\times$ sampling rate. To compensate for the ZOH a sampling rate of $2.5\,\mathrm{GHz}$ is chosen. This would result in a timing resolution of $400\,\mathrm{ps}$ for the microwave envelopes. Such a system cannot provide a duration inaccuracy specified in Table 4.2. However, as the total rotation angle for a certain gate/operation is determined by both amplitude and duration, the inaccuracy specification can be met by a finer amplitude resolution.

4.4.2. Numerically Controlled Oscillator

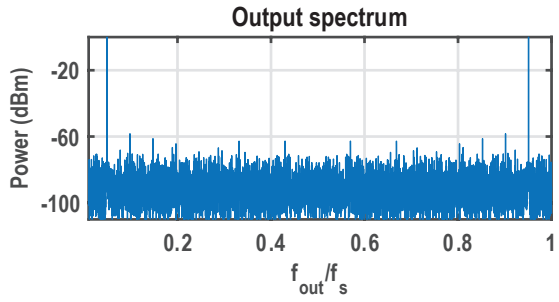
The frequency resolution (f_{res}) of the numerically controlled oscillator (NCO) is set by the number of bits in the phase accumulator register b_{acc} [106] given as $f_{res} = f_{clk}/2^{b_{acc}}$. Consequently, when performing a π-rotation using a rectangular envelope, the maximum frequency error can be $\Delta f = f_{res}/2$, resulting in a theoretical infidelity of

$$1 - F = \left(\frac{\Delta f}{f_R}\right)^2 = \left(\frac{1}{2^{b_{acc}+1}} \frac{f_{clk}}{f_R}\right)^2 . \tag{4.7}$$

The theoretical infidelity obtained in Eq. (4.7) is compared with the simulated infidelity for a π-rotation using both rectangular and Gaussian envelope as shown in Fig. 4.7. To emulate the worst-case scenario, the target frequency is chosen to be the value that produces the maximum frequency error. To obtain the same rotation angle,



(a)



(b)

Figure 4.8: The effect of phase truncation of the NCO on the output spectrum. Depending on the ratio N = f_s/f_{out}, the spectrum will either show (a) spurious tones when N is an integer (e.g. $N = 5$ in the plot) due to the repetitive behavior of errors, or (b) a white spectrum when N is not an integer, due to non-periodic behavior of the errors.

a Gaussian envelope requires a relatively longer duration compared to a rectangular envelope, thus accumulating a larger frequency error. Based on the simulation results, it can be observed that at least 16 accumulator bits are required to achieve $99.999\,\%$ fidelity. Note that, due to the limitations of the practical reconstruction filter, the simulated infidelity can deviate from the expected infidelity at very small frequency errors.

4.4.3. NCO phase truncation

To reduce the power consumption of digital cells, a minimum number of entries ($2^{b_{lut}}$) should be used in the sine/cosine look-up table (LUT). This can be achieved by truncating the least significant bits of the phase accumulator at the cost of periodic errors, resulting in spurious tones in the output spectrum. The output spectrum depends on the generated frequency as shown in Fig. 4.8, and the resulting SFDR can be calculated as SFDR = $6\,b_{lut}$ dB.

A spurious tone at the frequency of an idle qubit causes unintended rotation and its infidelity for a no-operation gate can be calculated as [102]:

$$1 - F = \frac{\theta^2}{4} \cdot 10^{-SFDR/10} \approx \frac{\theta^2}{4^{b_{lut}+1}}. \tag{4.8}$$

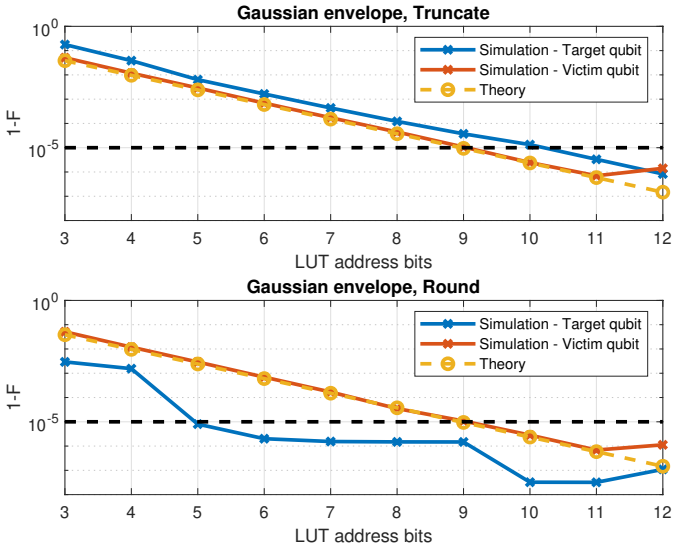


Figure 4.9: Infidelity of both target and victim qubit versus the number of LUT entries after truncation (top) and rounding (bottom) of the phase accumulator output.

The effect of the spurs on the infidelity of ideal qubits can be simulated as shown in Fig. 4.9. Since rectangular and Gaussian envelopes result in similar infidelity, the simulation results for a Gaussian envelope are presented. The frequency of the idle (victim) qubit is set at the largest spur to emulate the worst-case scenario. The effect of truncation and rounding on infidelity is considered for the output of the phase accumulator. Note that Eq. (4.8) predicts the infidelity of the idle qubit in both cases i.e. rounding or truncation. To obtain a fidelity of $99.999\,\%$, at least 9 bits are required in the case of rounding whereas 10 bits are required in the case of truncation. Hence rounding reduces the required b_{lut} by 1 bit compared to truncation, thus halving the required number of LUT entries.

4.4.4. LUT number of bits

A sine/cosine lookup table with a finite number of data bits (b_{data}) incurs quantization error. This error can be modeled as white noise spread over the full Nyquist bandwidth $f_s/2$ with a Signal-to-Quantization-Noise Ratio (SQNR) = $4^{b_{data}} \times 1.5$. However, the qubit is only sensitive to the noise in a certain bandwidth determined by the intrinsic filtering of the qubit. This effective noise bandwidth of the target qubit is given as $ENBW = f_R \cdot \frac{\pi}{\theta}$ [102] and results in an infidelity of:

$$1 - F = \frac{\theta^2}{4} \cdot \frac{1}{SQNR} \cdot \frac{ENBW}{BW} = \frac{\pi\theta}{3} \cdot \frac{f_R}{f_s} \cdot \frac{1}{4^{b_{data}}}. \tag{4.9}$$

The quantization noise also affects the victim qubits. The effect of tonal behavior of the quantization noise (tonal behavior shown in Fig. 4.8) can be simulated by

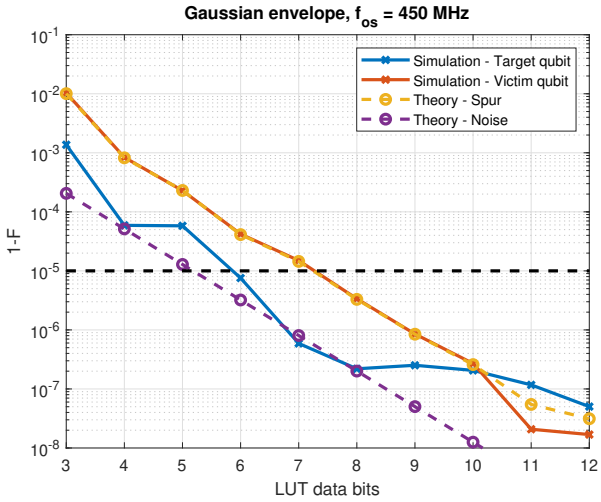


Figure 4.10: The simulated infidelity versus the number of data bits in the LUT when using a Gaussian envelope at an NCO frequency of $450\,\mathrm{MHz}$.

generating output at various NCO frequencies and locating the victim qubit at the highest spur frequency. To achieve $99.999\,\%$ fidelity, at least 8 data bits are required based on simulations at various NCO frequencies. As an example, Fig. 4.10 shows the simulated infidelity of both target and victim qubits versus LUT data bits, using a Gaussian envelope at an NCO frequency of $450\,\mathrm{MHz}$. This is well predicted by theoretical spur and noise estimation in Eq. (4.8) and Eq. (4.9), respectively.

4.4.5. Envelope memory

The envelope modulation is determined by the amplitude and phase memory. The finite resolution of the amplitude memory (b_{env}, signed) can cause amplitude errors (ΔA). The maximum amplitude inaccuracy for a rectangular envelope is given as $\Delta A/A = 1/2^{b_{env}}$, leading to an infidelity of [102]:

$$1 - F = \frac{\theta^2}{4} \cdot \left(\frac{\Delta A}{A}\right)^2 = \frac{\theta^2}{4^{b_{env}+1}}. \tag{4.10}$$

For a rectangular envelope, quantization noise can affect the amplitude but not the shape of the envelope. The worst-case scenario can be simulated by setting the qubit properties such that the required amplitude to perform the π-rotation using a rectangular envelope lies between two quantization levels. However, for a Gaussian pulse, quantization can lead to envelope distortion, degrading the purity of the output spectrum. Hence, a Gaussian envelope is used to simulate the effect of quantization noise on the target as well as the victim qubit as shown in Fig. 4.11. It can be observed that quantization noise has a negligible effect on the infidelity of victim qubits, and to obtain a $99.999\,\%$ fidelity, 9 bits are required for the envelope memory. For the

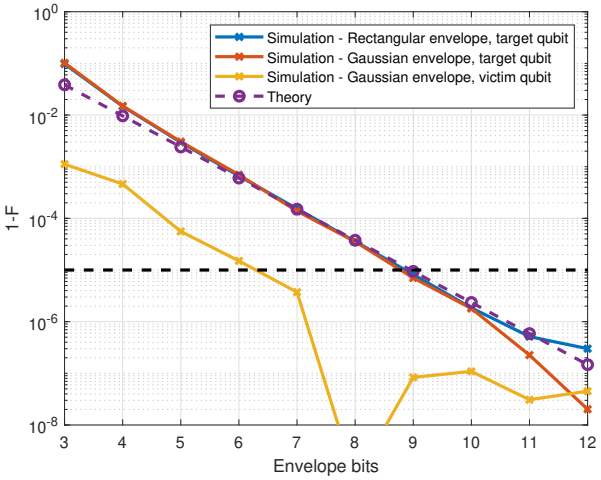


Figure 4.11: Infidelity versus the number of envelope bits using a rectangular and Gaussian envelope at an NCO frequency of 500 MHz.

phase memory, the bit-width was chosen equal to the bit-width of the NCO output to maintain the SFDR (Section 4.4.3).

The size of the envelope memory can be chosen based on the duration of qubit operation and the timing resolution (400 ps determined by the sampling rate. Assuming four instructions for each of the 32 qubits, a minimum memory of 160 kSa is required to support the longest operation duration of 500 ns.

4.4.6. Digital correction network

Single sideband transmitter architecture suffers from the issue of image tone at the output. Following the SFDR specifications, to achieve a gate fidelity of 99.999 %, the image rejection ratio (IRR) should be better than 54 dB. Such an IRR would require a gain imbalance (ϵ) and phase imbalance (ϕ) better than 0.4% (0.035 dB) and 0.23°, respectively following the equation:

$$IRR \approx \frac{4}{\epsilon^2 + \phi^2}. \tag{4.11}$$

Achieving such stringent phase imbalance specifications at RF frequencies is quite challenging in the analog domain. Hence a digital correction network (Fig. 4.6) is introduced to compensate for inaccuracies in the analog circuit blocks. The correction coefficients α_I, α_Q, β_I and β_Q are unsigned fractions with bit-widths (b_{frac}) determined by the maximum tolerable phase and gain imbalance. Since different corrections might be required at different frequencies, each NCO should have its own IRR coefficients.

For a maximum tolerable gain imbalance of 0.4 %, at least 7 bits are required for the gain compensation coefficients i.e. α_I or α_Q, given by $\Delta A/A = 1/2^{b_{frac}+1}$. For the

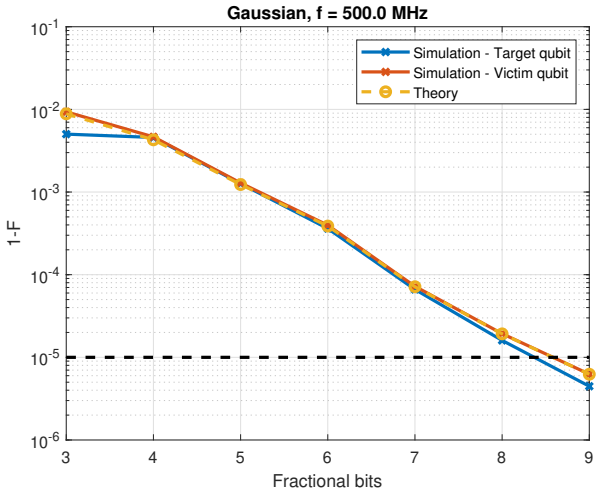


Figure 4.12: Simulated infidelity versus the number of fractional bits in the I/Q-correction network to correct for errors in the worst-case scenario. A Gaussian envelope at an NCO frequency of $500\,\mathrm{MHz}$ is used to drive the qubits while placing the victim qubit at the image frequency.

phase imbalance, the relation is non-linear and hence, both the α and β coefficients need to be adapted. To emulate the worst-case scenario, a system-level simulation is performed to correct the phase imbalance from -25° to +25° using a finite number of bits. Furthermore, this is co-simulated with the quantum processor using a Gaussian envelope as shown in Fig. 4.12. Both the target and the victim qubit are affected similarly and the infidelity is well-predicted by the power of the spurs in Eq. (4.8). Based on simulation results, to achieve a $99.999\,\%$ fidelity, at least 9 fractional bits in the fixed-point number are required.

4.4.7. Complete digital system

Based on the bit widths obtained for each of the circuit blocks, a full system simulation was done to execute a π-rotation on each of the 32 qubits evenly spaced over a $2\,\mathrm{GHz}$ band. The amplitude of Gaussian-modulated microwave pulses were set to obtain $10\,\mathrm{MHz}$ Rabi frequency under the condition of worst-case phase and gain imbalance. In this scenario, the infidelity of both addressed and unaddressed qubits was simulated along with placing one of the unaddressed qubits at the highest spurious tone.

The total system fidelity was limited to ~99.996% by the unaddressed qubit at the image frequency due to the truncation of the output bits of the multiplier used for amplitude modulation. This was improved to ~99.998% by rounding the multiplier outputs of the I/Q correction network, eventually limited by the unaddressed qubit at the highest spur frequency. When increasing the number of LUT entry bits (b_{lut}) by 1, we are at the edge of achieving the desired fidelity. The simulation results are shown in Fig. 4.13 and the final specifications are provided in Table 4.3.

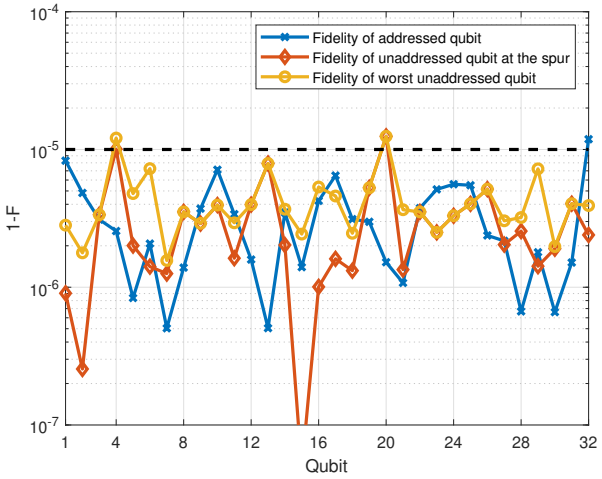


Figure 4.13: The simulated infidelity of the complete system with specifications in Table 4.3.

Table 4.3: Final system specifications.

Digital cell	Specification
Phase accumulator of the NCO	19 bits
LUT entries	10 bits (rounded)
LUT data	8 bits
Envelope	9 bits
Envelope multiplication output	9 bits (truncated)
I/Q correction coefficients	9 bits
Output of I/Q correction network	9 bits (rounded)
Envelope memory	~100 kSamples

4.4.8. Power consumption estimate

A rough estimate of the power consumption can be derived based on the obtained specifications and implementation examples found in the literature. A direct digital synthesizer with similar specifications (9-bit amplitude, 2-GHz clock and 55—dB SFDR) implemented in 55-nm CMOS consumes $25\,\mathrm{mW}$ in the 32-bit NCO and $37\,\mathrm{mW}$ in the phase-to-amplitude conversion [112]. Extrapolating these values for our system, 32 19-bit NCOs operating at $2.5\,\mathrm{GHz}$ and a single phase-to-amplitude conversion block would consume around $640\,\mathrm{mW}$. Similarly, a 10-bit multiplier in 65-nm CMOS operating at $2.5\,\mathrm{GHz}$ consumes $25\,\mathrm{mW}$ [113]. Extrapolating these values would result in a power consumption of $112\,\mathrm{mW}$ in our digital modulation and I/Q correction network (8 multipliers). This would result in a total digital power consumption of $\sim 750\,\mathrm{mW}$. Scaling these values to a lower technology node based on the study presented in [114], a power consumption of $\sim 160\,\mathrm{mW}$ is expected in a 22-nm CMOS node.

4.5. Conclusion

Deriving the system specifications of the classical electronic controller for qubits and determining the optimal error budget is crucial in designing power-efficient circuits. To meet these specifications, design trade-offs between several system architectures have been compared in this chapter, resulting in the proposal of an efficient architecture exploiting frequency multiplexing for multi-qubit control. Co-simulation of the proposed electronic system with qubits was used to assess the effect of non-idealities of each circuit block on the qubit fidelity. Based on such analysis, the design specifications of each block have been determined to achieve the required gate fidelity while minimizing the bit-widths of various digital blocks to optimize power consumption. As a result of the proposed design methodology, we have obtained the blueprint for a power-efficient integrated electronic controller to realize single-qubit operations for practical large-scale quantum computers.

5

Cryogenic controller: Design and Characterization

Background: *In the previous chapter, the specifications of a power-optimized qubit controller were derived from the signal specifications required for high-fidelity qubit control.*

Abstract: *In this chapter, a cryo-CMOS microwave signal generator for frequency-multiplexed control of 4×32 qubits (32 qubits per RF output) is presented. A digitally intensive architecture offering full programmability of phase, amplitude and frequency of the output microwave pulses and a wideband RF front-end operating from* $2\,\mathrm{GHz}$ *to* $20\,\mathrm{GHz}$ *allows targeting both spin qubits and transmons. Fabricated in Intel 22-nm FinFET technology, it achieves a 48-dB SNR and 45-dB SFDR in a 1-GHz data bandwidth when operating at* $3\,\mathrm{K}$*, thus complying with the specifications presented in the previous chapter.*

Summary: *This chapter is comprised of 7 sections. After a concise introduction, Section 5.2 elaborates on the challenges of designing a cryogenic controller for qubit control. The specifications of the reference clock and power consumption estimate of the analog/RF system is presented in Section 5.3. The design of the digital circuitry is explained in Section 5.4. The design of the analog circuit blocks has been briefly summarized and the RF front-end is thoroughly explained in Section 5.5. Section 5.6 shows the measurement setup and elaborates on the cryogenic electrical characterization of the chip ending with a comparison with state-of-the-art qubit controllers. Further improvements in the design and a conclusion are provided in Section 5.7.*

Parts of this chapter have been published in *IEEE International Solid-State Circuits Conference* [115] and *Journal of Solid-State Circuits* [116]. J. P. G. van Dijk has designed the analog blocks and the author has designed the RF blocks of the controller. Both have contributed towards the cryogenic measurements of the controller.

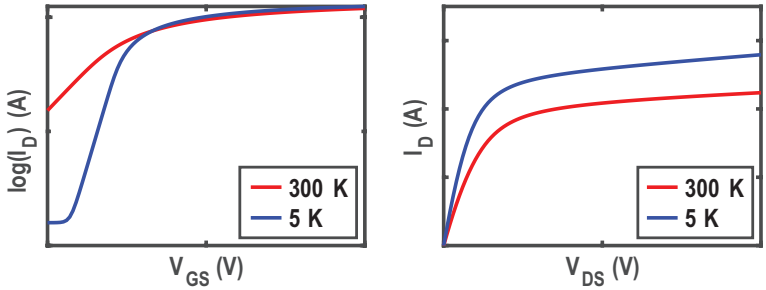


Figure 5.1: FinFET NMOS device characteristics at room temperature versus 5 K (temperature of the sample holder): drain current (I_D) versus gate-source voltage (V_{GS}) at drain-source voltage V_{DS} = 1 V (left) and I_D versus V_{DS} at V_{GS} = 0.4 V(right).

5.1. Introduction

Designing a cryogenic controller for large-scale quantum computing comes with several challenges. Firstly, qubits require highly accurate and low-noise microwave control signals to ensure high-fidelity single-qubit operations. For instance, to execute a π-rotation in 50 ns with 99.99 % fidelity, a carrier with 35-kHz frequency accuracy is required with a signal-to-noise ratio (SNR) of 50 dB in a 10-MHz band around the carrier [102]. Besides that, accurate control of the phase of the microwave signal ($< 0.2°$) with respect to the qubit's phase is essential to perform coherent qubit operations, i.e. rotations around a well-controlled axis, over the entire duration of the quantum algorithm.

Furthermore, the cooling power available at cryogenic temperatures in typically employed dilution refrigerators is strictly limited to a few Watts at 3 K and less than 1 mW at temperatures below 100 mK, thus complicating the integration of a large number of high-performance microwave signal generators. In this thesis, the focus is on the design of a controller operating at 3 K, because of the higher available cooling power. This does not restrict a future co-integration with qubits at the same temperature as the electronics, since 'hot' qubits operating at temperatures above 1 K have recently been demonstrated and are likely to evolve further in the next few years [117, 16].

5.2. Design Challenges

The variations in characteristics of CMOS devices operating at cryogenic temperatures compared to room temperature (RT) have been extensively analyzed in Chapter 2 for 40-nm CMOS technology. In this paragraph, we briefly discuss the variations in device characteristics for Intel 22-nm FinFET technology. Since mature models were unavailable at the design time to accurately predict the behavior of passive and active devices at cryogenic temperatures, the circuits had to be designed to compensate for these variations using additional tuning circuitry. Fig. 5.1 shows the NMOS transistor characteristics in 22-nm FinFET technology at 300 K and 5 K. The 5 K simulation models were developed from preliminary device characterization

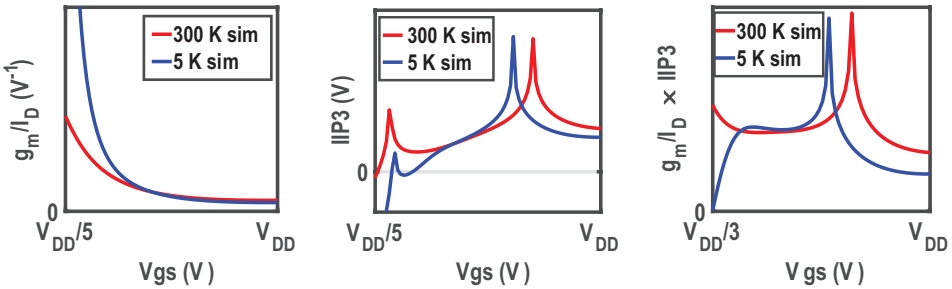


Figure 5.2: Simulated (a) g_m/I_D, (b) IIP3 & (c) $g_m/I_D \times$IIP3 at $300\,\mathrm{K}$ and $5\,\mathrm{K}$ for the adopted 22-nm FinFET CMOS technology.

performed at $5\,\mathrm{K}$ instead of $3\,\mathrm{K}$ due to limitations in the probe station temperature control, and are expected to be valid from $3\,\mathrm{K}$ to $20\,\mathrm{K}$, as demonstrated in [35] for another CMOS node. These models can be used to derive the various design parameters as follows. Fig. 5.2 demonstrates the expected change in g_m/I_d and linearity of an NMOS FET over temperature. It has been shown that device matching degrades at cryogenic temperatures [63]. This directly impacts the linearity of ADCs and DACs, and leads to increased offset in differential amplifiers. Furthermore, due to mismatch in the switching devices of a mixer, the degraded matching allows the second-order nonlinearity of the transconductance device to propagate to the output. On the contrary, carrier mobility increases, offering higher driving currents [118], and thermal noise is lower, potentially allowing a lower power consumption. However, the noise power spectral density does not scale linearly with temperature and is only expected to be approximately $10\times$ lower at $3\,\mathrm{K}$ as compared to $300\,\mathrm{K}$ [119]. Some devices are not strongly affected by the cryogenic operation, e.g. the thin film resistors used in this work show negligible change at $5\,\mathrm{K}$ compared to $300\,\mathrm{K}$. The capacitance of metal-oxide-metal capacitors and the inductance of on-chip inductors are expected to slightly change at cryogenic temperatures, while the inductor quality factor can double [28].

As discussed in the previous chapter, this design leverages the use of qubit frequency division multiple access (FDMA) [94] to obtain a power-efficient multi-qubit controller. However, employing FDMA introduces several additional challenges. Firstly, the required data bandwidth scales with the number of qubits and the qubit operation speed, ultimately requiring a data bandwidth in the order of $1\,\mathrm{GHz}$. To pack more qubits in the available frequency spectrum, pulse shaping needs to be applied to optimize the spectral content of the microwave pulses. Moreover, a high spurious-free dynamic range (SFDR) is required to ensure that no power is delivered to the qubits that are not addressed at a given time, and a mechanism should be incorporated to efficiently track the phase of all qubits to ensure coherent operations. In addition, phase-corrections must be applied to all qubits after every operation to compensate for the AC-Stark shift in a frequency multiplexing scheme [111].

5.3. Reference clock and power consumption

The specifications of various blocks in the digital system have been calculated in the previous chapter. In this section, the reference clock specifications are calculated and the minimum power consumption of the analog/RF front-end is estimated before diving into the design details of the chip in the following sections.

5.3.1. Reference clock specifications

A stable digital clock frequency can guarantee the accuracy of the output frequency, I/Q phase imbalance, and pulse duration to be generated in the digital section. As mentioned in Chapter 4, the frequency accuracy of $3.5\,\mathrm{kHz}$ (for a $1\,\mathrm{MHz}$ Rabi frequency and a $20\,\mathrm{GHz}$ output) requires a 0.18 ppm frequency stability. A crystal oscillator [120] can provide such a frequency stability as well as satisfy the required duration accuracy of $0.11\,\mathrm{ns}/50\,\mathrm{ns} = 0.22\%$. Consequently, the contribution of duration inaccuracy towards infidelity is negligible.

Since the frequency accuracy can be achieved with a commercial crystal oscillator, the remaining contributor to infidelity is the frequency noise and timing jitter. Let us assess which among these two is the tougher specification when using a common frequency synthesizer to derive the clock and the LO. The required clock jitter (σ_t) can be calculated as

$$\sigma_t = \frac{1}{2\pi f_0}\sqrt{\int_{f_a}^{f_b} \mathcal{L}(\Delta f)\, d(\Delta f)} \tag{5.1}$$

where f_0 is the clock frequency, $\mathcal{L}(\Delta f)$ represent the power spectral density of phase noise at a frequency offset Δf from the carrier. Assuming, a phase noise profile of a narrowband PLL with $\sim 1/f^2$ roll-off over the frequency range of interest i.e. f_a to f_b ($f_a \ll f_b$); $\mathcal{L}(\Delta f) = \alpha/(\Delta f)^2$, where α is a constant coefficient. Consequently, the frequency noise can be expressed as:

$$\sigma_f = \sqrt{\int_{f_a}^{f_b} (\Delta f)^2 . \frac{\alpha}{(\Delta f)^2}\, d(\Delta f)} \tag{5.2}$$

From the above equation, α can be calculated as $\alpha = \sigma_f^2/f_b$. Substituting $\mathcal{L}(\Delta f) = \alpha/(\Delta f)^2$ in Eq. (5.1), the required clock jitter can be calculated as:

$$\begin{aligned}\sigma_t &= \frac{1}{2\pi f_0}\sqrt{\int_{f_a}^{f_b} \frac{\sigma_f^2}{f_b} . \frac{1}{(\Delta f)^2}\, d(\Delta f)} \\ &= \frac{1}{2\pi f_0}\sqrt{\frac{f_b}{f_a}\frac{\sigma_f}{f_b}}\end{aligned} \tag{5.3}$$

While executing a π-rotation at a Rabi frequency of f_R, the qubit is only sensitive to noise in a bandwidth of $f_b = f_R \cdot \frac{\pi^2}{4}$, as mentioned in chapter 4. In case of 1-MHz Rabi oscillation ($\sigma_f = 3.5\,\mathrm{kHz_{rms}}$) with a system clock of $2.5\,\mathrm{GHz}$, an absolute

jitter of $\sigma_t < 0.9\,\mathrm{ps_{rms}}$ is required for a total duration of ~ 100 quantum operations ($f_a = f_b/100$) . Consequently, the timing jitter requirement of $0.11\,\mathrm{ns_{rms}}$ can be achieved resulting in negligible contribution towards infidelity. However, achieving the required frequency noise of $3.5\,\mathrm{kHz_{rms}}$ is not trivial. Assuming the above-mentioned profile, the frequency noise translates to a single-sideband phase noise specification of $-116\,\mathrm{dBc/Hz}$ at $1\,\mathrm{MHz}$ offset from the carrier.

5.3.2. Power consumption estimate of the RF front-end

Assuming the maximum output swing of $-16\,\mathrm{dBm}$ ($50\,\mathrm{mV_p}$) is directly generated by the DAC, no gain is required in the following stages. Hence, each stage contributes equally to the noise and distortion. These stages can be represented by a single-stage CMOS class-A resistive-loaded common source amplifier serving as the 50-Ω output driver. Note that the DAC quantization noise is already accounted for in the digital specifications presented in Chapter 4.

The maximum RMS output voltage of the driver is given by

$$V_{out} = \frac{I_d \cdot R_L}{\sqrt{2}}, \tag{5.4}$$

and the RMS output noise voltage by

$$v_n = \sqrt{4 \cdot k_B \cdot T \cdot \gamma \cdot g_m \cdot BW} \cdot R_L, \tag{5.5}$$

where I_d is the bias current, R_L is the load resistance, k_B is Boltzmann's constant, T the absolute temperature, $\gamma \sim 2$ is the excess noise factor for sub-micron devices and g_m the device transconductance. The Signal-to-Noise Ratio can be calculated as

$$SNR = \frac{V_{out}^2}{v_n^2} = \frac{I_d}{8 \cdot k_B \cdot T \cdot \gamma \cdot \left(\frac{g_m}{I_d}\right) \cdot BW}. \tag{5.6}$$

At $T = 300\,\mathrm{K}$, biasing the transistor to obtain $\left(\frac{g_m}{I_d}\right) \sim 10\,\mathrm{V^{-1}}$, a bias current $I_d > 0.66\,\mu\mathrm{A}$ is required to achieve the 50-dB SNR specification with a 10-MHz Rabi frequency (f_R). As mentioned earlier, the bandwidth for which the qubit is sensitive to amplitude noise for a π-rotation is $BW = f_R$. The bias current to obtain the required SNR is already satisfied, as achieving the desired output voltage swing over a 50-Ω load requires $I_d > 1\,\mathrm{mA}$.

After estimating the current consumption to achieve the required SNR, let us calculate the current needed to meet the linearity specifications. Assuming an ideal square law CMOS device used as single-ended amplifier, the 2nd-order distortion is given by (Section 5.7 of [121])

$$HD2 = \frac{1}{4} \cdot \frac{V_{in}}{V_{gs} - V_T}, \tag{5.7}$$

where V_{in} is the input voltage, V_{gs} is the gate-to-source voltage and V_T is the device threshold voltage. To meet the requirement of HD2 $< -44\,\mathrm{dB}$ without any gain

($V_{in,max}$ = 50 $\mathrm{mV_p}$), an impractical overdrive voltage $V_{gs} - V_T > 2\,\mathrm{V}$ is required. In order not to be limited by HD2, a differential circuit topology can be considered with a 3rd-order distortion of (Section 5.7 of [121])

$$HD3 = \frac{1}{18}\left[\frac{V_{out,p}}{(V_{gs} - V_T)\cdot g_m \cdot R_L}\right]^2, \tag{5.8}$$

where $V_{out,p}$ is the peak amplitude. Achieving HD3 $< -44\,\mathrm{dB}$ requires an overdrive $V_{gs} - V_T > 0.15\,\mathrm{V}$ (assuming the gain $g_m \cdot R_L = 1$). A device operating in saturation region with a g_m of $\frac{1}{50\,\Omega}$ requires a bias current larger than $1.5\,\mathrm{mA}$ [1] as $V_{gs} - V_T = 2\cdot\left(\frac{g_m}{I_d}\right)^{-1}$. Finally, an SFDR $< -44\,\mathrm{dB}$ requires a DAC with an effective number of bits (ENOB) of 7.

As mentioned in the beginning of the subsection, all the calculations above assume that the complete controller comprising of the DAC, filter, mixer and output driver is represented by a single CMOS class-A resistive loaded common source amplifier. However, in reality each of the circuit block have their own purpose such as filtering, frequency unconversion, etc and will be integrated in the final system. Consequently, the equivalent linearity of the cascaded system with a unity gain in each circuit block is given as (Section 2.5 of [121])

$$\frac{1}{A^2_{IP3,system}} = \frac{1}{A^2_{IP3,DAC}} + \frac{1}{A^2_{IP3,filter}} + \frac{1}{A^2_{IP3,mixer}} + \frac{1}{A^2_{IP3,driver}} \tag{5.9}$$

where A_{IP3} represents the third intercept point (IP3). Hence to obtain a total HD3 $< -44\,\mathrm{dB}$, each block in the cascaded system should have 4× better linearity i.e. HD3 $< -56\,\mathrm{dB}$. This would increase the power consumption of each block to 4×1.5 = $6\,\mathrm{mA}$ and consequently $24\,\mathrm{mA}$ for the total system.

The proposed design requirements are summarized in Table 5.1.
Amongst all requirements, LO frequency noise appears the most stringent. Since the duration accuracy, timing jitter, and amplitude noise specifications are easily satisfied, their error contribution can be minimized to relax the circuit specifications of power-hungry blocks. Note that, the SFDR specification cannot be relaxed as it is the only error source considered affecting idle qubits.

5.4. Digital circuit design

The top-level simplified architecture of the qubit controller discussed in the previous chapter is shown in Fig. 5.3. The architecture employs two banks of digital signal generation unit in the back-end and single-sideband (SSB) modulation in the analog front-end for controlling 32 frequency-multiplexed single-electron spin qubits or transmons. Such a system requires only a single external LO, setting the desired output frequency band, while supporting multiple qubits at different frequencies in the $2\,\mathrm{GHz}$ output band, thanks to the direct digital synthesizer (DDS) containing numerically-controlled oscillators (NCO) to keep track of the phase of each qubit.

[1] In case of simultaneous excitation of multiple qubits, an IM3 = 3 HD3 < -44 dB is required and consequently a bias current larger than $2.6\,\mathrm{mA}$.

Table 5.1: Final system specifications.

Parameter	Value
Clock sample rate (f_s)	2.5 GHz
Reference clock stability	0.18 ppm
Clock jitter	0.9 ps_{rms}
LO frequency range	6-19 GHz
LO phase noise	-116 dBc/Hz at 1 MHz offset
DAC Resolution	9 bit
Reconstruction filter	2nd-order Chebyshev-I at 1.8 GHz
Analog gain stability	0.22%
Analog gain control	44 dB
SNR	50 dB ($I_d > 0.66\,\mu$A)
HD3	-44 dB ($I_d > 1.5$ mA)

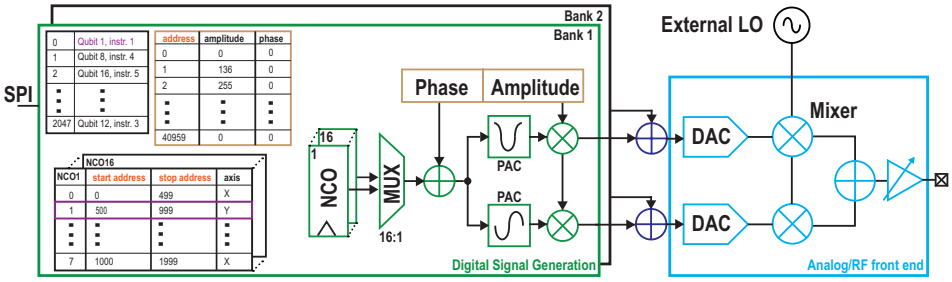


Figure 5.3: Architecture of the controller employing digital signal generation and analog front-end.

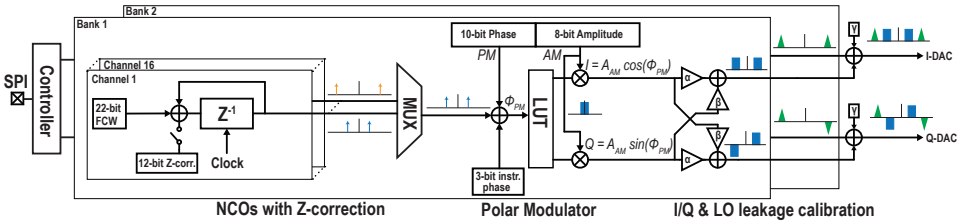


Figure 5.4: Digital signal generation schematic employing DDS and modulators with a controller for algorithm execution and memory management.

The digital signal generation unit employs a direct digital synthesizer (DDS) with amplitude and phase modulation along with a controller for algorithm execution and memory management, as shown in Fig. 5.4. Each bank contains 16 NCOs to keep track of the phase evolution of individual qubits. The outputs of the 16 NCOs are time-multiplexed to allow operation on a single qubit at a time to reduce system complexity. However, the replication of DDS with modulator into two banks allows simultaneous control of two qubits. The operation and justification of the bit-width used in individual blocks have been elaboration in chapter 4.

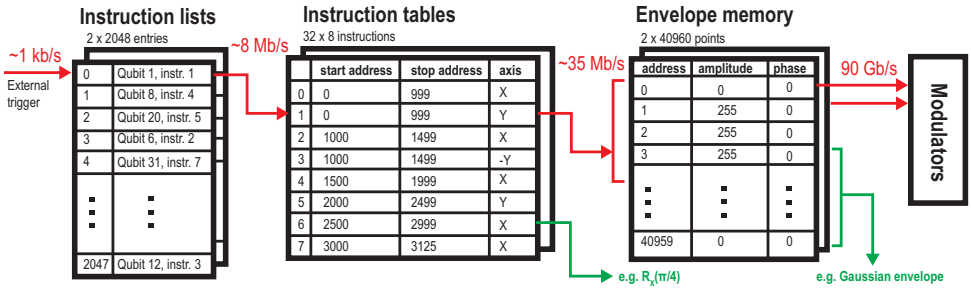


Figure 5.5: Memory organization of the integrated controller comprising instruction lists, instruction tables and envelope memories to gradually reduce the data rate.

As the two signal-generation units require an input data rate of $(8\,\text{bit} + 10\,\text{bit}) \cdot 2.5\,\text{GHz} \cdot 2 = 90\,\text{Gb/s}$, a quantum algorithm execution controller has been integrated, comprising an envelope memory containing the desired pulse envelopes, an instruction table for each qubit referencing the envelopes, and an instruction list containing the sequence of instructions to be executed (Fig. 5.3). Since a pulse of $500\,\text{ns}$, or 1250 samples at $2.5\,\text{GHz}$, is required for the lowest operating speed of $1\,\text{MHz}$ and the largest rotation angle of π, 2560 samples are available per qubit in the envelope memory (40960 samples are shared over 16 qubits in each bank). The envelopes can be efficiently reused for rotations around different axes, as the axis, and the respective phase shift, are defined in the instruction table, which has 8 entries per qubit to define the instructions. This is expected to be sufficient, as a typical instruction set will contain a limited set of rotations, e.g. a π, $\pi/2$, and $\pi/4$, around the X and Y axis. Moreover, the controller automatically performs the qubit Z-rotations required to compensate for the AC-Stark shift in a frequency multiplexing scheme [97, 102], by applying a phase shift defined from a programmable Z-correction table to all NCOs after each generated pulse. Thanks to this level of digital integration, the requirement of $90\,\text{Gb/s}$ external data rate can be replaced with a $\approx 1\,\text{kHz}$ trigger using the instruction list for the execution of a quantum algorithm.

The external interface consists of two separate interfaces i.e. a slow and a fast interface with dedicated shift registers to program and control the chip operation. The *slow* interface is used for programming the various internal memories and triggering the start of execution of the instruction list. In contrary, the *fast* interface with a dedicated $150\,\text{Mb/s}$ shift register can execute a single instruction, as often as every $\approx 75\,\text{ns}$. A single instruction sent to the fast interface contains the start and stop

address of the envelope memory and the NCO to be used, thus enabling the execution of a single gate operation on a specific qubit. Hence, the *fast* interface can be used as an alternative to the execution of the pre-programmed instruction list (see Fig. 5.5), to facilitate fast feedback if needed during the execution of a quantum algorithm.

Since a cryogenic model of the standard-cell library was not available at the time of design to close timing for synthesis and automated place-and-route (APR), derating factors were implemented to extrapolate the timing behavior at $3\,\mathrm{K}$ from the room-temperature models of the standard cell library. The derating factor for the delay of sequential gates is extracted by comparing the simulated oscillation frequency of a 9-inverter ring oscillator at room temperature (using the standard foundry device models) and at $5\,\mathrm{K}$ (using a preliminary cryogenic DC device model). Similarly, the derating factors for set-up and hold times are extracted by transistor-level simulations of a standard D Flip Flop. A common derating factor of $\sim$1.3 is determined for all cases, implying about 30% reduction in gate delay and set-up/hold times. Using such derating factor for gate delays for synthesis and APR results in effective timing slacks at $5\,\mathrm{K}$ for both min and max delay, i.e. timing margins for hold and set-up violations, equal or greater than the values targeted for room temperature. Interconnect delay should also be scaled accordingly when using room temperature models to predict $5\,\mathrm{K}$ behavior. From transistor measurement de-embedding data, it is evident that interconnect capacitance does not change significantly at $5\,\mathrm{K}$, while resistance is reduced by about 50%. A $0.5\times$ derating factor is therefore used for the room temperature extracted resistances during APR to model $5\,\mathrm{K}$ interconnect delays.

The SoC is implemented as a digital-on-top system with 4 transmitters sharing one common I/O block. Timing is resolved at $2.5\,\mathrm{GHz}$, with the SRAMs for the envelope memory operating at $1.25\,\mathrm{GHz}$ with $2\times$ time-interleaving. The SRAM supply voltage can be controlled independently to ensure correct operation in the presence of an increased threshold voltage at cryogenic temperatures. Standard digital-circuit design-optimization techniques, such as pipelining and time interleaving, along with the aforementioned derating, were used to achieve timing closure at $2.5\,\mathrm{GHz}$.

5.5. RF front-end

For the analog/baseband circuitry, current-mode architectures were adopted to prevent the transconductance non-linearity, as the system requires a fairly high bandwidth and linearity ($> 44\,\mathrm{dB}$). The baseband circuitry comprises a current-steering DAC and a current-mode gm-C reconstruction filter as shown in Fig. 5.6.

From the system specifications presented in the previous section, it was concluded that a 10-bit current-steering DAC (9-bit for single tone) is required to translate the two simultaneous tones from the digital to analog domain. Based on the filter architecture a unit current of $125\,\mu\mathrm{A}/2^{10} = 122\,\mathrm{nA}$ from a PMOS current source [116] is produced. The DAC is segmented in 5-bit unary and 5-bit binary sections as a trade-off between DNL and decoder complexity.

A 2nd-order Chebyshev-I filter with 1.8 GHz cut-off frequency is chosen as it meets the stopband requirement, while its peaking results in the required improved inband flatness near the end of the passband by compensating for the DAC zero-order-hold filter response [116].

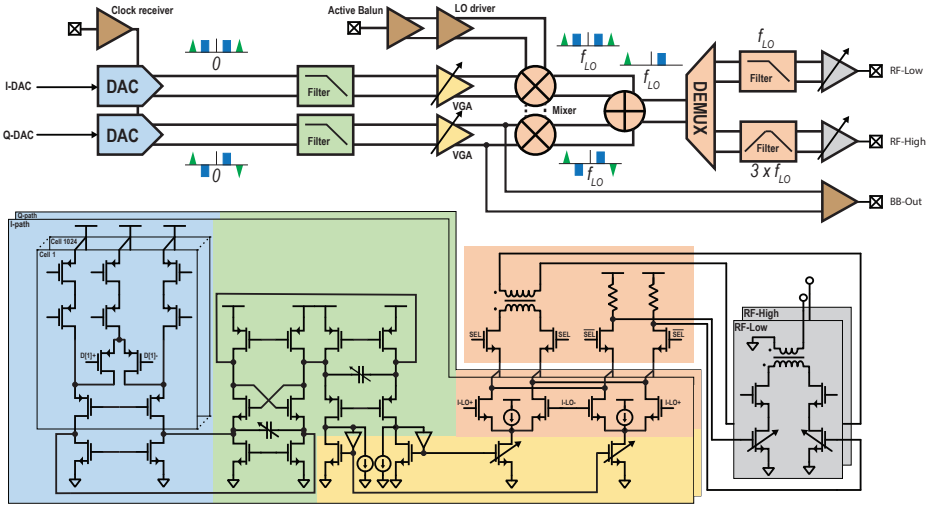


Figure 5.6: Analog RF front-end schematic.

The variable gain amplifier (VGA) is implemented as a tunable current mirror used to provide a 4-bit tunable gain up to 15×. As the filter bias current is much higher than the mixer bias current, part of it is sunk at the filter output (represented by current sources to ground in Fig. 5.6), while maintaining sufficient VGA linearity. The remaining excess bias current from the filter is removed from the transconductance devices (represented by current sources to the power supply in Fig. 5.6) of the mixer using current bleeding technique as elaborated in Section 5.5.1. Both of these current-bleeding sources are tunable to ensure optimal performance at 3 K.

5.5.1. Mixer

Figure 5.7a shows the schematic of the dual-frequency-band mixer. The fundamental and third harmonic output current (obtained by hard switching) of the mixer are used to extend the operating frequency range compared to a traditional double-balanced Gilbert cell I/Q mixer as shown in Fig. 5.7b. Cascode devices are added at the output of the switching devices to steer the output current into either a resistive load for the lower frequency band (OUT-LOW), i.e. 2-15 GHz, or an inter-stage matching transformer for the higher frequency band (OUT-HIGH), i.e. 15-20 GHz.

Lower frequency band

The required bandwidth (e.g., 15 GHz), and the parasitic capacitance of the output driver, mixer, and their interconnection sets a maximum limit on the load resistance (e.g., $\leq 70\,\Omega$). On the other hand, based on the linearity requirements of the output driver (as will be discussed in Section 5.5.2), the output swing ($V_{out,mixer}$) of the mixer has to be less than 35 mV. Hence, the required current swing (I_{sw}) to be fed

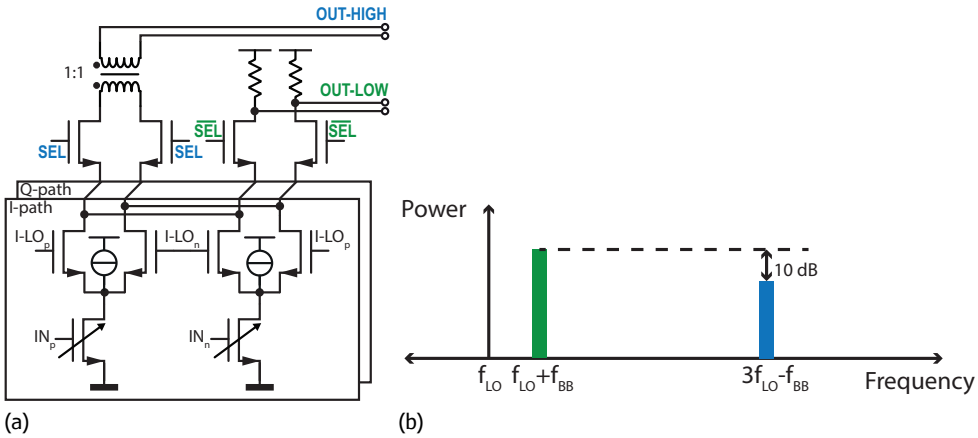


Figure 5.7: (a) Double balanced Gilbert cell I/Q active mixer [122], with two output frequency bands, (b) Output spectrum of the mixer when hard switching produces upconverted tones at f_{LO} and $3xf_{LO}$.

from the VGA to the switching devices of the mixer can be estimated by

$$V_{out,mixer} = \sqrt{2} \times 2 \times \frac{2}{\pi} \times I_{sw} \times R_L. \tag{5.10}$$

The voltage to current conversion non-linearity in the transconductance stage of a typical active mixer is avoided by using a high-speed current amplifier or the VGA (Fig. 5.6). The VGA not only amplifies the current swing from the filter but also acts as a current mirror with the same gain ratio for the DC bias current fed into the switching devices of the mixer. During the ON period of the switching devices, they should operate in saturation region to completely steer the current from the transconductance devices acting as a cascode for high linearity. Hence, the minimum bias current should be the same as the current swing calculated from Eq. (5.10). Operation as a cascode also ensures that minimum noise is contributed by the switching devices to the mixer output. Since the mixer topology requires 4 stacked devices all operating in saturation region (two in VGA, 1 switching device, 1 output path selection device), the maximum bias current is determined by the voltage headroom required to operate these devices in saturation region.

Due to low current swing ($125\,\mu A_p$) and high bias current ($1.25\,mA$) in the filter, a gain ratio of 4× from the VGA required to get the necessary mixer output voltage swing results in excessive bias current in the switching devices causing voltage-headroom issue. Note that a $70\,\Omega$ load resistance at the mixer would result in I_{sw} of $275\,\mu A$ (Eq. (5.10)) demanding a 2.2× gain from the VGA for a filter current swing of $125\,\mu A$. However, a higher gain (4×) is required to compensate for non-hard switching (lower LO swing results is $2\,dB$ lower power) of the mixer and to obtain the required swing at $3\,dB$ bandwidth.

To tackle the voltage-headroom issue, current bleeding is implemented using current-sinking sources to the supply voltage (represented as two current sources in Fig. 5.7a). This enables to lower the current in the switching devices, cascodes,

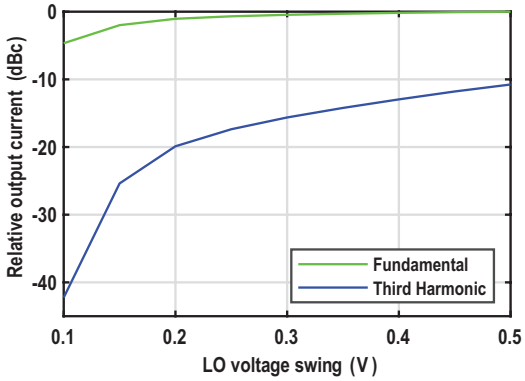


Figure 5.8: Schematic level simulation of fundamental and third harmonic output current from the mixer versus LO swing at 300 K.

and resistor, without sacrificing the required linearity in the VGA [123]. After partially sinking ($1\,\mathrm{mA}$) the bias current at the filter output, $0.375\,\mathrm{mA}$ current is sunk through mixer bleeding current sources. Thus the remaining bias current through the switching devices is $625\,\mu\mathrm{A}$ to steer $500\,\mu\mathrm{A}$ current swing with some extra headroom. Moreover, steering lower current through the switching devices requires smaller transistors for a constant gate-source bias voltage. This in turn presents a lower load capacitance to the LO driver, thus enabling lower power consumption for the LO driver. Finally, the switching devices are biased at the edge of saturation region for efficient switching with low LO voltage swing.

Higher frequency band

The output current of the mixer at $3 \times f_{LO} - f_{BB}$ versus the LO swing is shown in Fig. 5.8. The LO swing is chosen to be $300\,\mathrm{mV}$ since a further increase in swing does not significantly improve the conversion gain at the cost of higher power consumption in the LO driver. Note that the third harmonic output current is $15\,\mathrm{dB}$ lower than the fundamental at $300\,\mathrm{mV}$ LO swing, which is compensated by amplification in the following stages. A tuned inter-stage matching network is designed to amplify the third harmonic while attenuating the fundamental tone. To boost the mixer gain at the third harmonic, a relatively narrow-band design is chosen, which is more susceptible to unwanted variation at cryogenic temperatures. Hence, switchable resistor and capacitor tuning networks are employed to compensate for this variation.

5.5.2. Output driver

Figure 5.9 shows the schematic of the output driver consisting of a class-A amplifier with an output matching network. This design is used for both lower- and higher-frequency-band outputs with different device sizing and matching networks.

The specification of the output driver is to deliver two simultaneous tones each with $-16\,\mathrm{dBm}$ output power (P_{out}) to a $50\,\Omega$ load, with 50 dB SFDR setting an OIP3

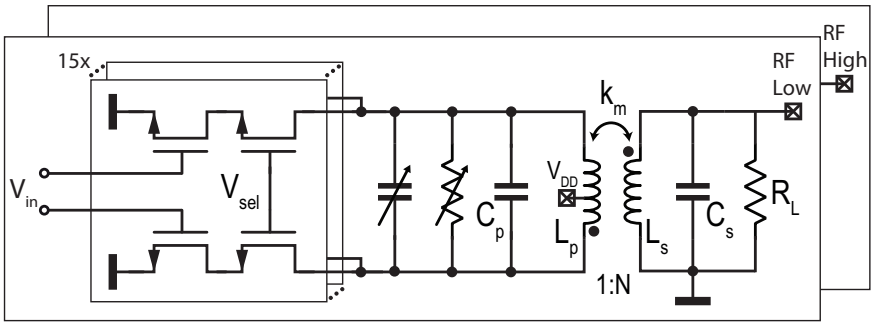
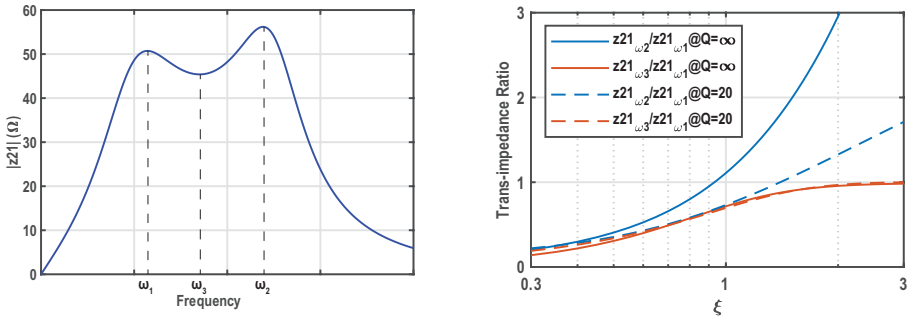


Figure 5.9: Output driver schematic



(a) (b)

Figure 5.10: Optimization of matching networks: (a) Transfer function (b) Trans-impedance ratio.

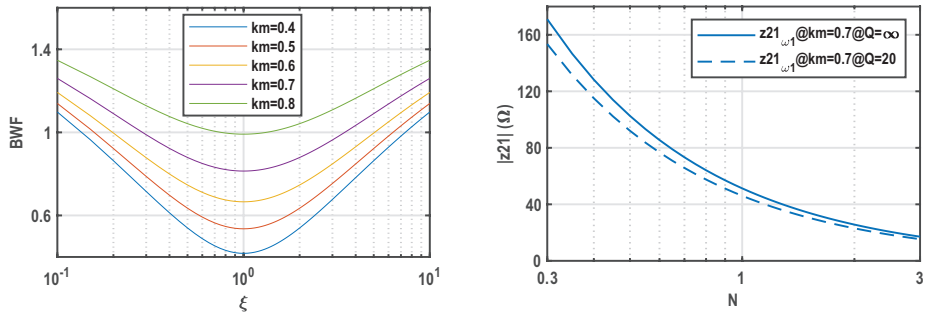
requirement of 9 dBm.

$$OIP3 = P_{out} + IM3/2 = -16 + 25 = +9\,dBm \tag{5.11}$$

Since, $V_{OIP3} = V_{IIP3} \times g_m/I_D \times I_D \times R_L$, and both V_{IIP3} and g_m/I_D are determined by the intrinsic device characteristics, the maximum point of this product ($V_{IIP3} \times g_m/I_D$) at 3 K is chosen to obtain the required linearity at the lowest power consumption, while taking into account voltage headroom and signal swing, as shown in Fig. 5.2c. Thus, an overdrive voltage V_{gt} =0.25 V has been chosen, leading to V_{IIP3} =0.63 V and g_m/I_D = 8. Consequently, the maximum input swing ($V_{in,max}$) to obtain an IM3 of 50 dB can be calculated as

$$V_{in,max} = \frac{V_{IIP3}}{10^{IM3/40}} = \frac{0.63V}{10^{50/40}} = 35\,mV \tag{5.12}$$

The output matching network can be analyzed as a trans-impedance (Z_{21}) network to convert the drain-current swing of the driver transistor to the required voltage swing at the output. The pole/peaks ($\omega_{1,2}$) and minima/trough (ω_3) frequencies



(a) (b)

Figure 5.11: Optimization of matching networks: (a) BWF, (b) Trans-impedance vs N.

of a matching network can be derived from the local maxima and minima of Z_{21}, respectively, given as [124, 64]

$$\omega_{1,2} = \sqrt{\frac{1+\xi \pm \sqrt{1-2\xi+4k_m^2\xi+\xi^2}}{2C_sL_s - 2C_sk_m^2L_s}}$$
$$\omega_3 = \sqrt{\frac{1+\xi+\sqrt{1+14\xi-12k_m^2\xi+\xi^2}}{6C_sL_s - 6C_sk_m^2L_s}} \tag{5.13}$$

where L_s is the secondary inductance, C_s is the secondary capacitance, $\xi = \frac{L_sC_s}{L_pC_p}$, L_p is the primary inductance, C_p is the primary capacitance and k_m is coupling factor. In a wideband design, both poles should lie in the bandwidth of interest, and, to obtain a flat transfer function, the transimpedance at these poles should be equalized, i.e. $|Z_{21}(\omega_2)/Z_{21}(\omega_1)| = 1$. For a lossless matching network, this can be obtained by setting ξ=1 [124]. However, with practical quality factors for the inductors, ξ needs to be increased to e.g. 1.5 as shown in Fig. 5.10b to achieve $|Z_{21}(\omega_2)/Z_{21}(\omega_1)|$ =1.06 and $|Z_{21}(\omega_3)/Z_{21}(\omega_1)| = 0.9$. Note that the effect of a practical quality factor on the transimpedance ratio between the poles and the minima (i.e. $|Z_{21}(\omega_3)/Z_{21}(\omega_1)|$) is negligible. For a lossless matching network, the bandwidth factor ($BWF = \frac{\omega_1-\omega_2}{\omega_3}$) is minimum at ξ = 1, as shown in Fig. 5.11a. Hence, to obtain a flat transfer function (ξ ~1) and high BWF, one has to maximize k_m, which is ultimately limited by the physical realization of the transformer. To further increase the BWF for the maximum attainable k_m, ξ should be increased at the cost of flatness in the transfer function as shown in Fig. 5.10b. However, the flatness can be restored by lowering the quality factor at the cost of passive efficiency.

The value of k_m and ξ can be determined using the procedure in the previous paragraph. The next step is to compute the ratio of the inductances of the primary and secondary windings of the transformer. Figure 5.11b shows the dependency of

$|Z_{21}|$ on N ($N = \sqrt{\frac{Ls}{Lp}}$) at a constant ξ and k_m. A higher $|Z_{21}|$ or lower N increases the equivalent resistance seen by the driver transistors. Hence, a relatively lower current swing can produce the same output voltage swing. This, in turn, would demand a lower DC bias current and improve the efficiency, as long as the transistor does not enter the triode region, affecting the linearity. This leads to smaller transistors and consequently, higher bandwidth of the mixer due to lower input capacitance presented by the output driver. Since ξ is already fixed by the flatness and BWF, minimizing N would require maximizing C_s and minimizing C_p, as $N = \sqrt{\xi \frac{C_p}{C_s}}$. The minimum value of C_p is determined by the parasitic capacitance of the output driver, while the optimum C_s can be obtained from the value of loaded quality factor of the secondary side ($Q_L = R_L C_s \omega$) that maximizes the passive efficiency of the matching network at a given frequency [125]. Finally, N = 0.8 is obtained.

An increase in the quality factor (Q) of a transformer by a factor of ~2 expected at cryogenic temperatures, due to lower substrate losses and a higher metal conductivity [28], can affect the flatness of the transfer function. The transfer function can shift towards higher frequencies due to a reduction in effective inductance and capacitance of the transformer at cryogenic temperatures [28]. To compensate for these variations, that are not well predictable, capacitor and resistor tuning networks were implemented at the windings of all matching networks.

To maintain a better efficiency at lower output voltage swing, a gain control of $24\,\mathrm{dB}$ is achieved by selectively switching 15 unit cells, each consisting of a cascoded class-A amplifier. To further improve the power efficiency, the supply voltage of the driver is lowered without significant impact on linearity, since the required output voltage swing is significantly lower than the supply voltage.

5.5.3. Auxiliary circuits

An LO driver and a clock receiver are also implemented in each transmitter (TX). Four transmitters are integrated into a single chip to increase the number of qubits that can be controlled, and to allow for the simultaneous control of 4 qubits at the same frequency through individual transmitter outputs.

LO driver

An LO driver with $20\,\mathrm{dB}$ voltage gain and $15\,\mathrm{GHz}$ bandwidth is designed to deliver the required voltage swing to the mixer, while incorporating single-ended to differential conversion. On-chip co-planar waveguide transmission lines are used to connect the input of the LO driver to the I/O bumps. This allows to reduce phase and gain imbalance by allowing the LO driver output to be abutted to the mixer switches.

Fig. 5.12 shows the schematic of the LO driver. The first stage serves as an active balun converting a single-ended signal to a differential signal while providing wideband input-impedance matching [126]. For proper operation, the input matching is achieved by adjusting M_1 gate bias such that $1/g_{m,M_1} = 50\,\Omega$ and by setting the gain of the common-gate (CG) path $g_{m,M_1} R_{CG}$ equal to the gain of the common-source (CS) path $g_{m,M_2} R_{CS}$.

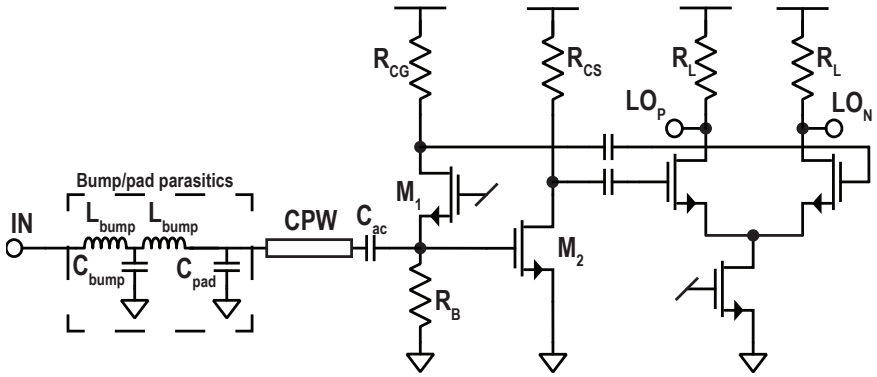


Figure 5.12: Schematic of the LO driver.

The required gain of 5× at $15\,\mathrm{GHz}$ sets the required gain-bandwidth (GBW) to be $75\,\mathrm{GHz}$. For the active balun to directly drive the mixer switches, a load capacitance C_L = 40 fF (due to parasitic capacitance of mixer switches, M1/M2 devices, and routing traces) limits the maximum load resistance to 180 Ω and consequently, the gain to 3.6. Hence, to achieve the required GBW, a high-speed differential CML amplifier stage is cascaded to the first stage.

The required phase noise specification of -116 dBc/Hz at $1\,\mathrm{MHz}$ offset from the carrier is achieved over the entire frequency range with a power consumption of $7\,\mathrm{mW}$ for both I&Q branches. The simulated phase noise of the LO driver at $12\,\mathrm{GHz}$ carrier frequency results in a thermal noise floor of $-148\,\mathrm{dBc/Hz}$ with a flicker noise corner at $5\,\mathrm{MHz}$.

The top-level RF layout was designed using layout abutment, wherein the interconnect lines between high-frequency blocks were minimized by careful planning at the top level, as shown in Fig. 5.13.

Clock receiver

A clock-receiver circuit provides the rail-to-rail-swing clock signals for the DAC and the digital blocks, powered using the digital supply. To share a single external clock signal between all 4 transmitters, each transmitter is AC coupled with an input termination of $200\,\Omega$ (R_T) to present an equivalent input impedance of $50\,\Omega$. A self-biased inverter with power-down option and a transmission gate are employed to individually switch off the clock receiver in each transmitter while preventing feed-through during the off state. A half-period time shift can be introduced between the clock fed to the digital circuits (DIGITAL) with respect to the DAC (DAC_I, DAC_Q), enabled by a digitally controlled on-chip register PH via an XOR gate, as shown in Fig. 5.14. This can address any potential data timing issue at the digital/DAC interface due to layout mismatch and changes in digital propagation delay at $3\,\mathrm{K}$. A fan-out of 3 is maintained at each stage to obtain the required jitter.The simulated phase noise of the clock receiver at $2.5\,\mathrm{GHz}$ output frequency results in a thermal noise floor of $-123\,\mathrm{dBc/Hz}$ with a flicker noise corner at $2\,\mathrm{MHz}$. Integrating the phase noise over $2.5\,\mathrm{MHz}$ bandwidth

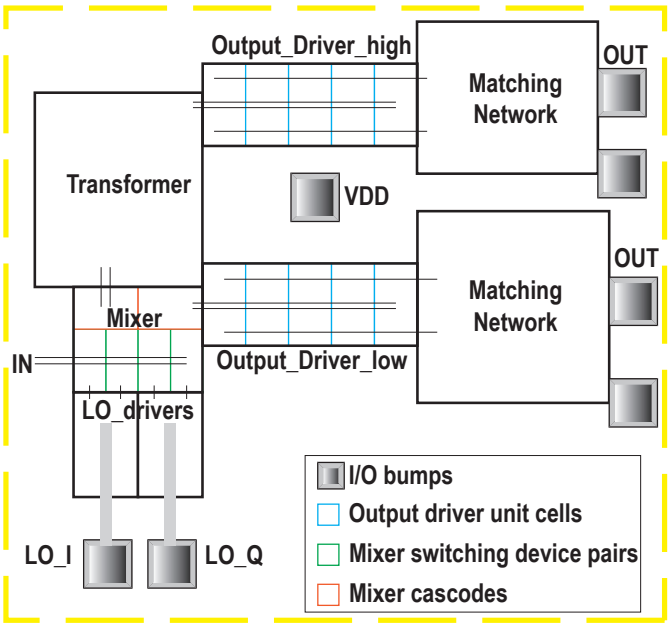


Figure 5.13: Representation of RF circuit blocks' layout at the top-level.

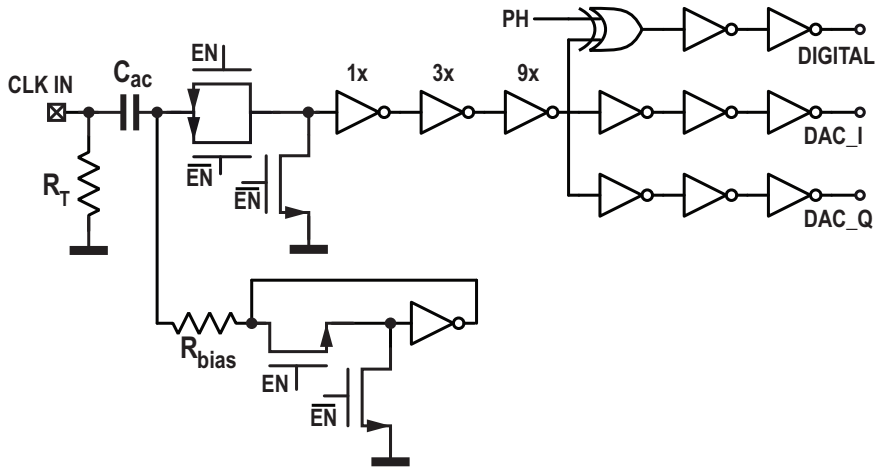


Figure 5.14: Schematic of the clock receiver.

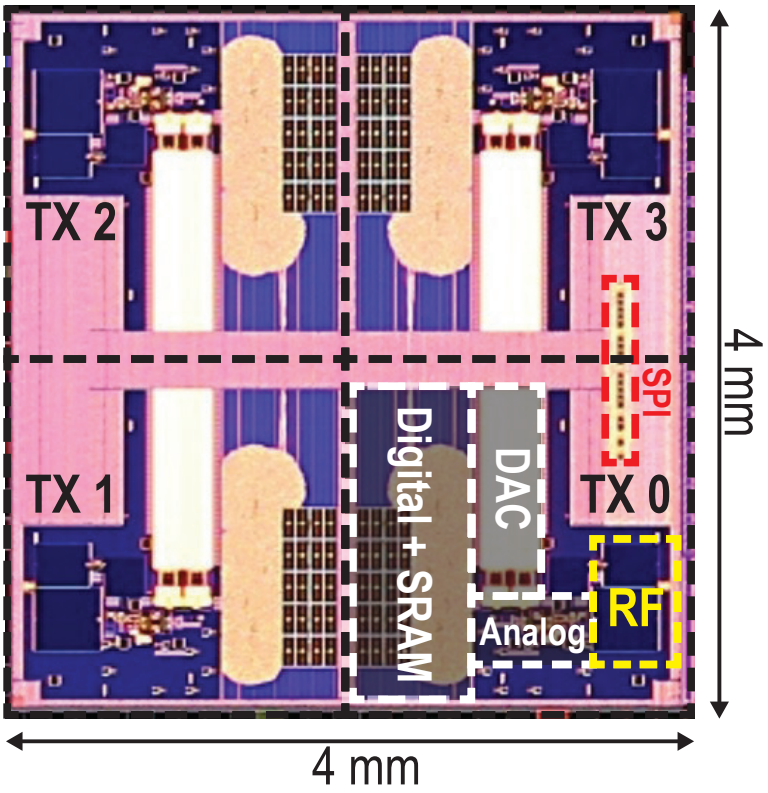


Figure 5.15: Chip micrograph.

(for 1 MHz Rabi) produces a jitter level of 0.25 ps.

5.6. Cryogenic Electrical Performance

Figure 5.15 shows the micrograph of the chip fabricated in Intel 22 nm FinFET (22FFL) technology [127]. The transmitter architecture shown in Fig. 5.3 is replicated 4 times (TX0...TX3) with each instance occupying an area of $4\,\mathrm{mm}^2$ with a single shared SPI controller on the die.

The die is flip-chip bonded to a BGA324 package with impedance-matched traces and on-package discrete capacitors for supply decoupling as shown in Fig. 5.16. Note that all supplies are substantially decoupled on-chip to reduce the supply noise feedthrough between different circuit blocks. A 6-layer PCB is designed to route the RF signals on the top layer with RT/duroid 6002 microwave substrate and DC signals on the bottom layers with FR4 dielectric. The solder-mask areas on the top and bottom layers are minimized to allow better heat transfer. To reduce the number of cables between the room-temperature LO generator and the chip inside the dilution refrigerator, each LO line is shared between two transmitters. A custom-designed Wilkin-

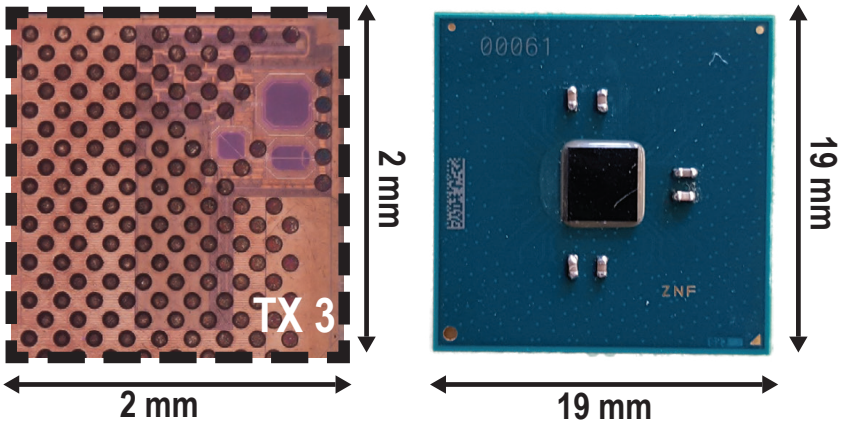


Figure 5.16: On-chip solder bumps (left) and BGA 324 package (right).

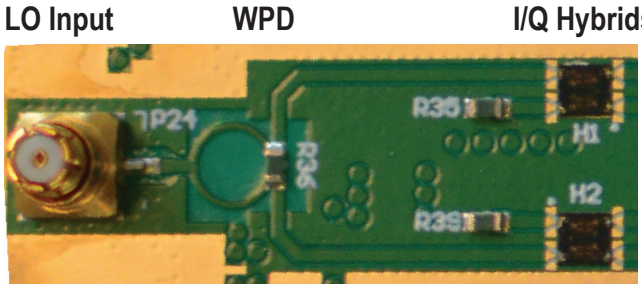


Figure 5.17: A zoom-in on the PCB showing the WPD and discrete hybrids (Marki MQS-0418) for splitting the LO input.

son power divider (WPD) on the PCB with discrete wire-bonded quadrature hybrids (Marki MQS-0418) were used to generate the required LO signals for the transmitters, as shown in Fig. 5.17. The WPD was separately designed on a RT6002 PCB substrate and characterized in a cryogenic probe station at $4.2\,\mathrm{K}$ as shown in Fig. 5.18. The measurement of the gain and phase imbalance of the hybrid at $3\,\mathrm{K}$ stage of a dilution refrigerator is shown in Fig. 5.19.

Several commercial off the shelf low dropout (LDO) voltage regulators have been tested to be non-functional at cryogenic temperatures in [59]. A compensated version of the custom-made LDO functional at cryogenic temperatures [59] was employed on the PCB using discrete components (AD8608 opamp with TSM2314 MOSFET). The opamp drives the transistor so as to make the voltage at its negative input terminal equal to V_{REF} using the resistor feedback network of R_1 and R_2. The value of R_1 is chosen to obtain the required output voltage V_{OUT} proportional to V_{REF}. C_C is used as a compensation capacitor. Different output voltages for the various supply domains can be obtained using a single reference by varying the ratio of R_1 and R_2.

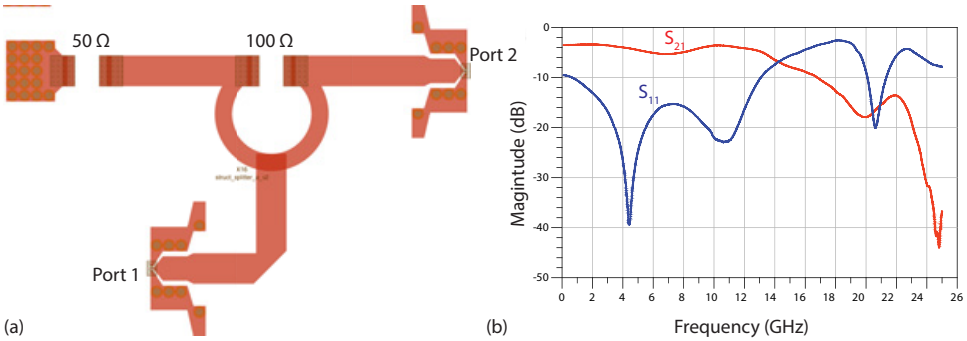


Figure 5.18: (a) WPD layout with 50 Ω and 100 Ω discrete resistors. (b) S-parameter measurement of the WPD.

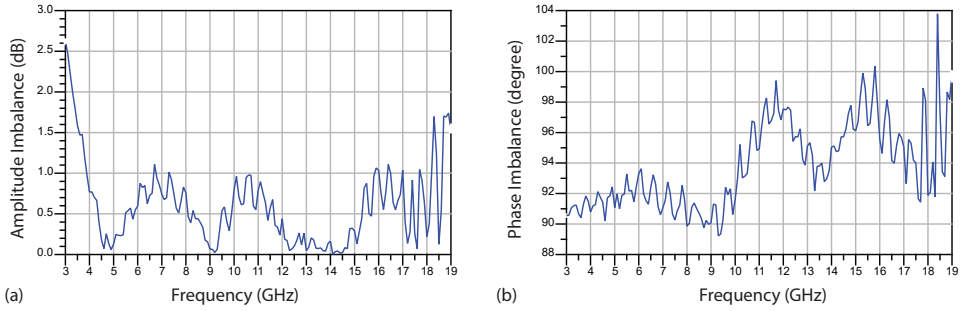


Figure 5.19: IQ hybrid measurements at 3 K showing (a) gain imbalance and (b) phase imbalance. Ripples in the measurement trace are due to uncalibrated cables as the hybrids were measured inside the dilution refrigerator.

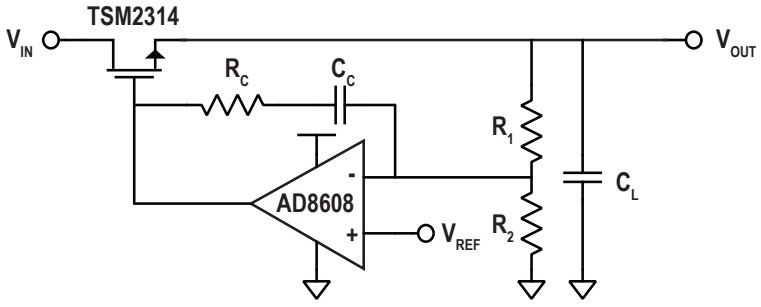


Figure 5.20: LDO voltage regulator with discrete components operating at 3 K.

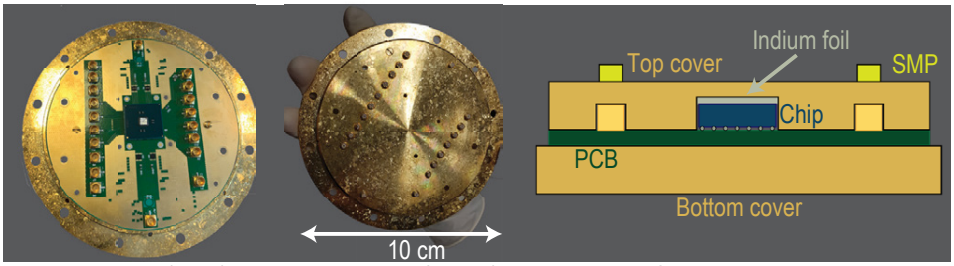


Figure 5.21: From left-to-right: the bottom view of the opened and closed gold-plated copper enclosure and a drawing of the cross-section of the full enclosure with PCB.

5.6.1. Measurement setup

A gold-plated copper enclosure housing the PCB acts as a heat sink for proper thermalization of the chip to the $3\,\mathrm{K}$ plate in the fridge, as shown in Fig. 5.21. Indium foils were sandwiched between the die and the enclosure to maximize the contact surface area and minimize thermal resistance. Thanks to its high malleability compared to other metals, Indium can compensate for the mismatch of the thermal expansion between the two mating surfaces (silicon and gold) at cryogenic temperatures. The chip is placed on the $3\,\mathrm{K}$ plate of a dilution refrigerator as shown in Fig. 5.22.

To monitor the die temperature, on-chip diodes were placed across the chip, as shown in Fig. 5.23. These are calibrated using an external silicon diode temperature sensor (with an accuracy of $0.25\,\mathrm{K}$) mounted close to the enclosure, with the chip powered down. Figure 5.23 shows the junction and plate temperature as a function of the chip power consumption, which is varied by changing the clock frequency and the supply voltage of the digital circuitry. Although the die self-heating increases significantly with power consumption, the plate temperature is only slightly affected. As the dilution unit is connected to a separate plate with an independent pulse tube cooler, the qubit temperature is not affected.

5.6.2. Electrical characterization

While the functionality of all four transmitters has been verified, the performance of one transmitter is reported in the following.

Figure 5.24 shows the power consumption of the various circuit blocks at $1\,\mathrm{GHz}$ clock frequency, $6\,\mathrm{GHz}$ and $18\,\mathrm{GHz}$ output frequency using the low frequency and high frequency path respectively. The digital back-end dominates the power consumption due to the lack of clock gating in a substantial part of the memory and would increase further with clock speed. Hence, to limit the temperature increase of the fridge plate, the chip is operated at a maximum clock frequency of $1\,\mathrm{GHz}$, limiting the available data bandwidth to $1\,\mathrm{GHz}$. The analog power consumption is dominated by the output drivers due to high-linearity requirements and the support of a $50\,\Omega$ load. The total power consumption of 12 mW/qubit would allow the control of > 320 qubits in a state-of-the-art dilution refrigerator, over only 10 RF lines, with a single SPI interface wired to room temperature. This is well beyond the number of qubits

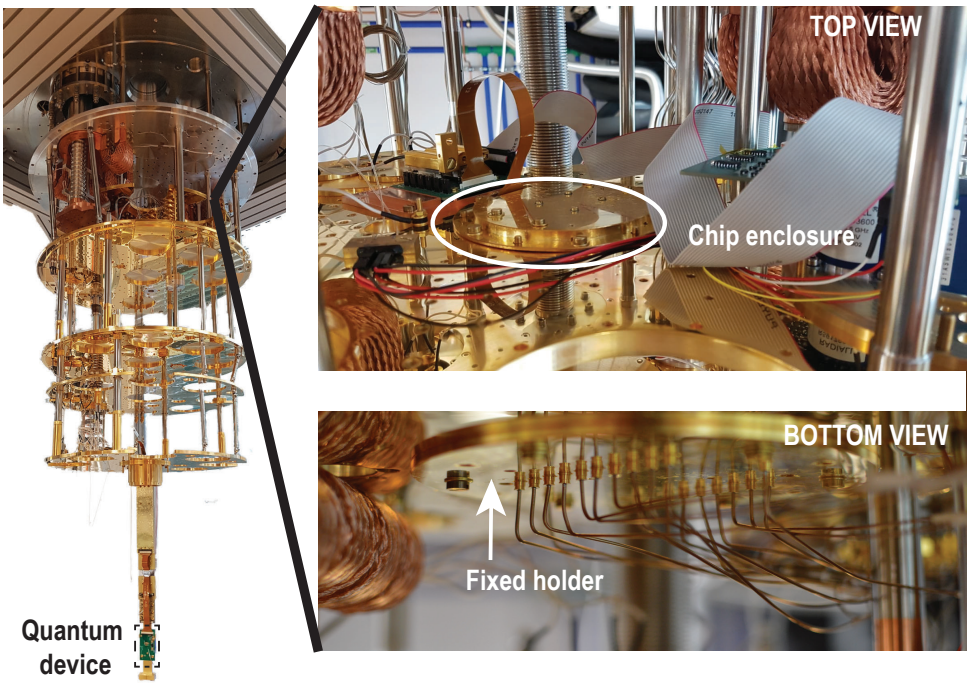


Figure 5.22: Placement of the chip enclosure at the 3 K plate of the dilution refrigerator.

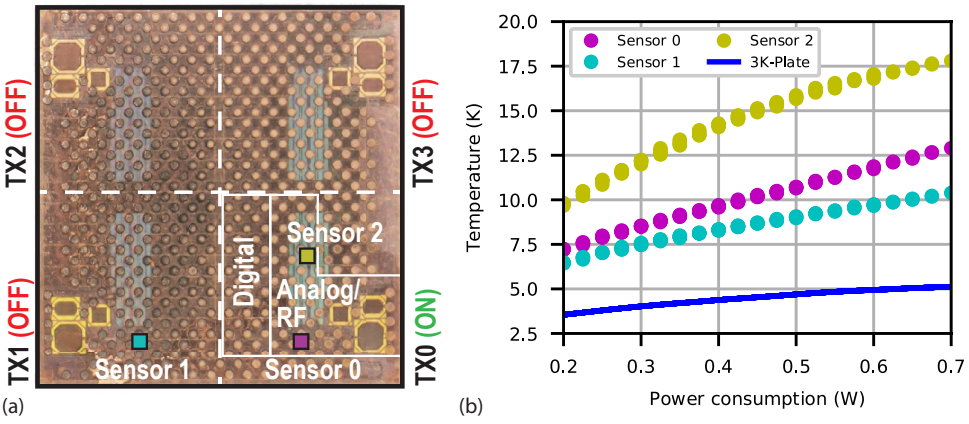


Figure 5.23: (a) Placement of on-chip diodes and (b) measured die temperature versus power consumption.

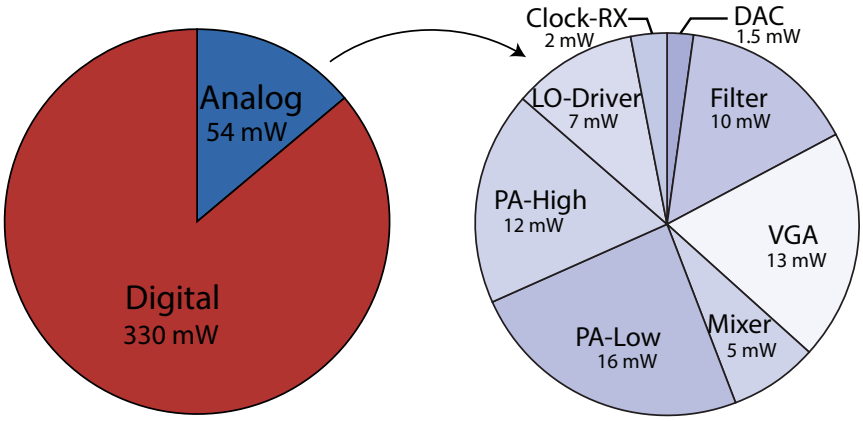
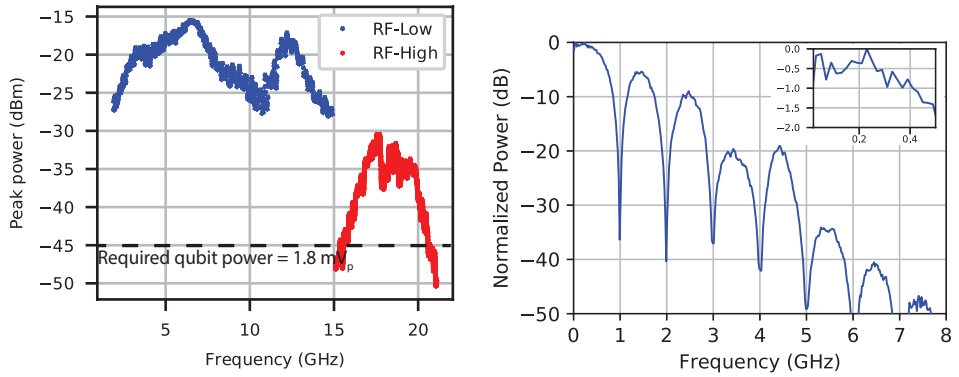


Figure 5.24: Power consumption breakdown at system and circuit level.

available in the largest solid-state quantum processor today [5]. Moreover, this work presents a first implementation of the controller, and further power reduction is possible as 1) significant margins were taken during the design to ensure functionality, 2) large output power and frequency ranges were included to support multiple qubit technologies, and 3) the currently dominating digital power consumption could be reduced by e.g. clock gating. With such optimizations (more suggestions in the conclusion of this chapter), scaling to thousands of qubits is expected to be possible in the near term, while a larger cooling power is expected to extend the scaling in the longer term [128]. Thanks to the integrated digital controller, an external $1\,\mathrm{kHz}$ trigger signal can execute instructions on the qubits, allowing scaling to a large number of controllers sharing a single high-speed connection to room temperature. Moreover, thanks to the use of FDMA in this work, the number of connections to the quantum processor is reduced by 32×. However, supporting millions of qubits in the future with the proposed approach would still require a large number of connections to the quantum processor, but this could be eased by co-integrating the controller and the qubits on the same package or die at the same temperature.

The frequency resolution of the NCO follows from $f_{res} = f_{clk}/2^{NCO_{res}}$, where f_{clk} is the $1\,\mathrm{GHz}$ clock frequency, and NCO_{res} is the 22-bit resolution of the NCO, resulting in a frequency step of ∼238 Hz. Such a frequency step implies a maximum frequency inaccuracy of $238/2 = 119$ Hz. The frequency step was measured to be $\sim 237\,\mathrm{Hz}$.

Figure 5.25a shows the measured output power versus frequency at $3\,\mathrm{K}$ for both output paths. Compared to the simulation of the matching network shown in the previous section, the flatness of the transfer function for the low frequency output path is deteriorated due to the additional ground inductance introduced in the layout between the secondary winding of the output matching network and the on-chip solder bumps. This creates an imbalance in the ratio of the windings required to achieve a flat transfer function as elaborated in the previous section. Moreover, due to these additional routing with narrow metal lines, the quality factor of the secondary winding of both the output matching networks were degraded. For the high frequency



(a) (b)

Figure 5.25: (a) Measured RF bandwidth, (b) Transfer function of the baseband output (inset: zoomed in from 0 to 0.5 GHz).

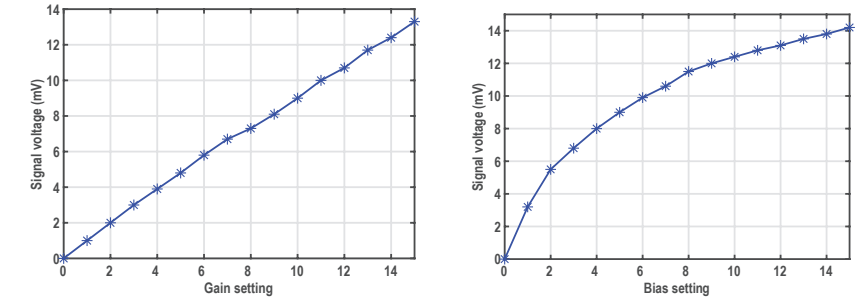
output path (RF-High), this effect was severely observed in the form of much lower output power than the low frequency path (RF-low).

To quantify the attenuation of the sampling replicas and flatness of the baseband transfer function, the measured output at the baseband monitoring node is shown in Fig. 5.25b. An in-band flatness of 1.5 dB is obtained up to 500 MHz as shown in the inset of Fig. 5.25b.

Fig. 5.26 shows the gain control of the output driver either by varying the number of activated unit cells or by varying the bias current of the driver. Fig. 5.26a demonstrates a linear gain control with minor deviation at gain setting 8 where the 4x, 2x, 1x gain cells are deactivated and 8x gain cell is activated.

The SFDR obtained for single and two-tone signals at various output frequencies is shown in Fig. 5.27 and Fig. 5.28. From the single-tone spectra, it can be observed that the SFDR is limited by the image-rejection ratio (IRR) of 45 dB obtained after calibration. The SFDR measured for various NCO frequencies over the entire data bandwidth is better than 42 dB as shown in Fig. 5.29a. The achieved LO rejection does not affect the SFDR, since it can be avoided by proper choice of the LO frequency.

The SFDR of the two-tone spectrum with a tone spacing of 19 MHz shown in Fig. 5.27 and Fig. 5.28 is limited by the second-order intermodulation (IM2) component. Such IM2 can be attributed to the integral non-linearity (INL) of the DAC that shows a quadratic behavior [116]. This is due to a linear gradient, i.e. systematic mismatch, in the DAC layout that does not use a fully common-centroid layout due to practical layout constraints, but an arrangement only similar to a common-centroid one. This systematic mismatch increases at 3 K. Moreover, random mismatch is degraded at 3 K [35], as can be seen in the differential non-linearity (DNL) [116]. The measured third-order intermodulation (IM3) component with a two-tone spacing of 10 MHz is better than 47 dBc at the highest output power over the entire RF-Low bandwidth as shown in Fig. 5.29b. The measured SNR at the maximum output power over a 25 MHz bandwidth is greater than 48 dB as shown in Fig. 5.29a complying



(a) (b)

Figure 5.26: Gain control at 6.5 GHz (a) by varying the number of activated unit cells in the output driver at a fixed bias current. (b) by varying the bias current of the output driver unit cell with all the unit cells activated.

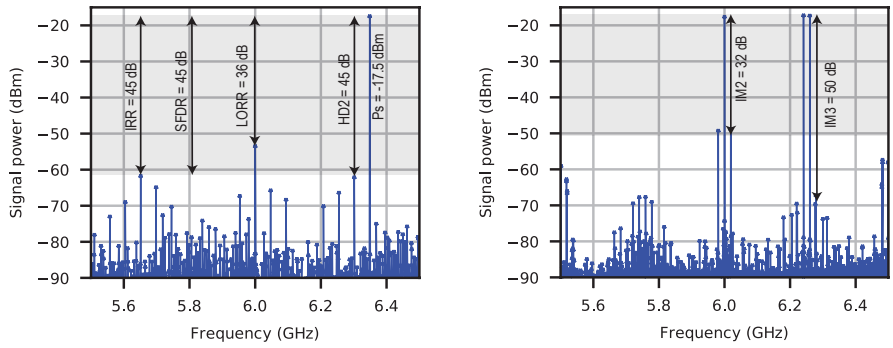


Figure 5.27: (Left) Single-tone SFDR at 6.35 GHz highlighting the IRR, SFDR, LORR, HD2 and output tone power; (Right) Two-tone output at the maximum output power with NCOs operating at 241 MHz and 260 MHz and LO frequency of 6 GHz highlighting IM2 and IM3.

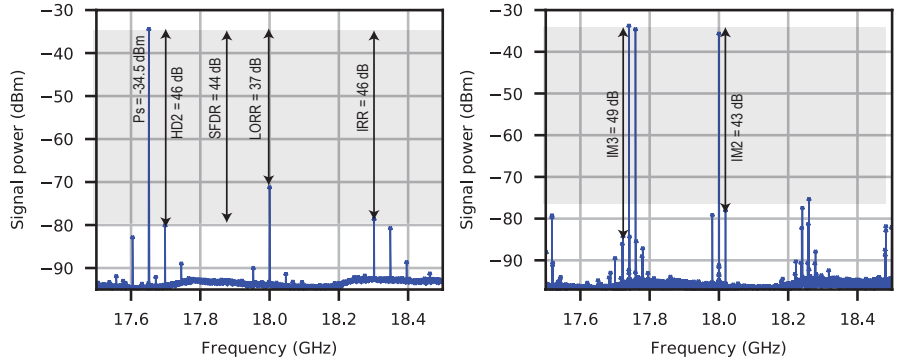
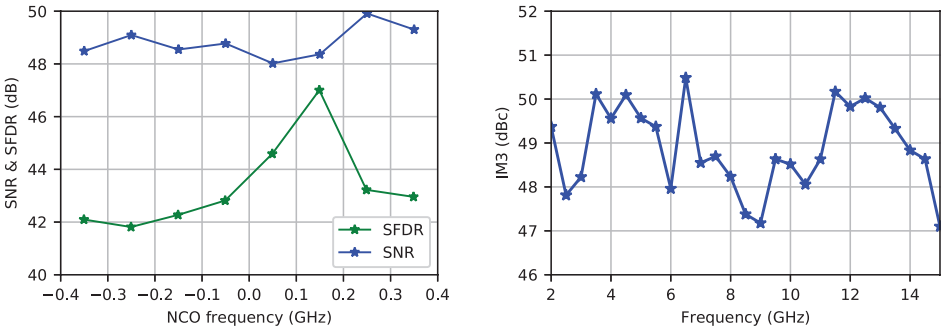


Figure 5.28: (Left) Single-tone SFDR at 17.65 GHz highlighting the IRR, SFDR, LORR, HD2 and output tone power; (Right) Two-tone output at the max output power with NCOs operating at 241 MHz and 260 MHz and LO frequency of 6 GHz highlighting IM2 and IM3.



(a) (b)

Figure 5.29: (a) SNR & Single-tone SFDR versus NCO frequencies at 5 GHz, (b) IM3 for a fixed NCO frequency over the entire RF-Low band.

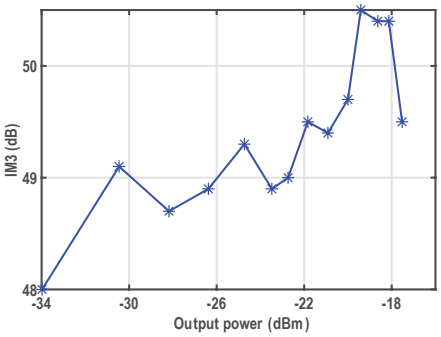


Figure 5.30: IM3 versus output power at 6.5 GHz

with the system requirements presented earlier.

The IM3 versus the output power is shown in Fig. 5.30. It can be observed that the IM3 shows negligible variation (few dB) with lowering the output power by 17 dB indicating that the linearity of complete transmitter chain is not limited by the output driver.

Engineering the pulse shape is critical for addressing multiple qubits over a frequency multiplexed line [97, 102] as the shape of the pulse provides a trade-off between the speed of operation on the addressed qubit versus unwanted energy leaking into the unaddressed qubits. To demonstrate the pulse shaping capabilities of the chip, various pulse envelopes were generated at different offset frequencies as depicted in Fig. 6.17, which shows the time domain (at baseband frequency) and frequency domain response of the chip output.

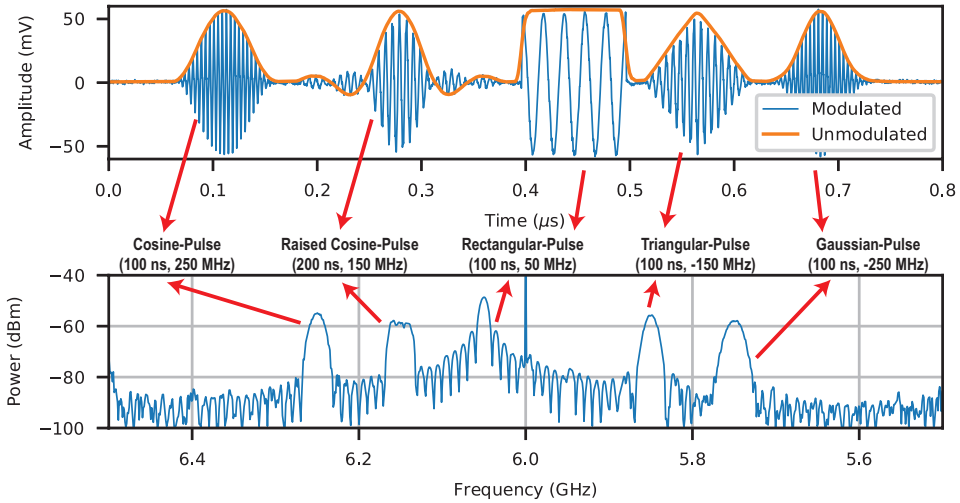


Figure 5.31: Pulse shaping; Top: measured time-domain signal at baseband output, Bottom: upconverted output spectrum.

5

5.6.3. Quality of modulation

The previous subsections show the spectral purity of continuous-wave tone measured at cryogenic temperatures. In this subsection, the modulation quality of the controller is evaluated for pulsed mode operation using the standard metric for evaluation of a transmitter i.e. error vector magnitude (EVM).

The EVM is a comprehensive measurement figure for determining the overall quality of signal modulation at the output of the controller. In this method, the controller produces a signal constellation defined in a specific modulation scheme such as quadrature amplitude modulation (QAM). The quality of this generated signal in compared against an ideal signal to produce a single metric to quantitatively measure the combined effect of all the impairments that corrupt the signal. For a multi-level QAM, this parameter considers all the phase and amplitude distortions and noise. Fig. 5.32 shows the constellation diagram of the 16-QAM modulated signal wherein each symbol is encoded with certain phase and amplitude information.

To measure the modulation quality using the EVM metric, raised cosine pulses with a roll-off factor (β) of 0.5 are used to avoid error caused due to Inter Symbol Interference (ISI) in a 16-QAM modulation scheme. The spectrum of 16-QAM signal using raised cosine pulses is shown in Fig. 5.33.

Fig. 5.34 shows the measured constellation and modulation error summary for a 16-QAM signal with raised cosine pulses at $6.4\,\mathrm{GHz}$. The summary in the figure lists the measured gain imbalance of $0.04\,\mathrm{dB}$ and quadrature error of $0.03°$ resulting in an I/Q imbalance of $\sim -53\,\mathrm{dB}$, thus meeting the required specifications.

The total EVM can be calculated as [129]:

$$EVM_{total} = \sqrt{10^{IRR} + 10^{LOFT} + 10^{PN} + 10^{SNR} + 10^{SFDR} + 10^{IM3}} \tag{5.14}$$

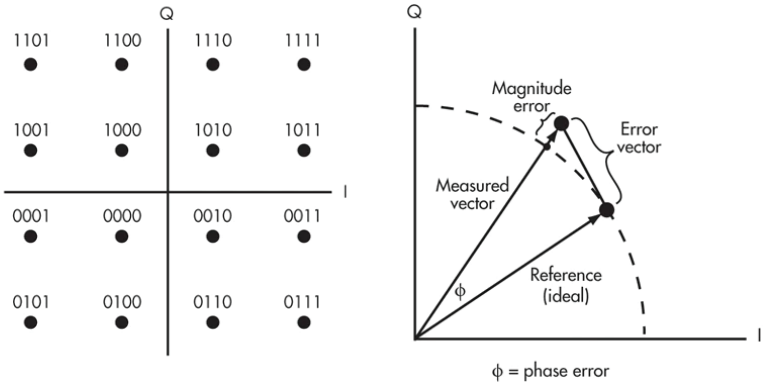


Figure 5.32: 16QAM modulation and EVM

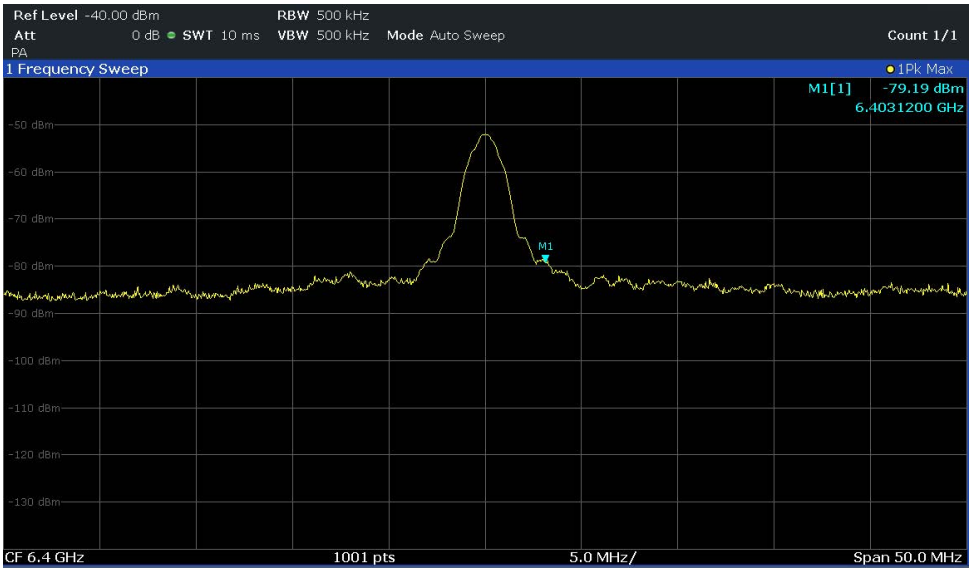


Figure 5.33: Spectrum of 16-QAM signal using raised cosine pulses with a 0.5 roll-off factor.

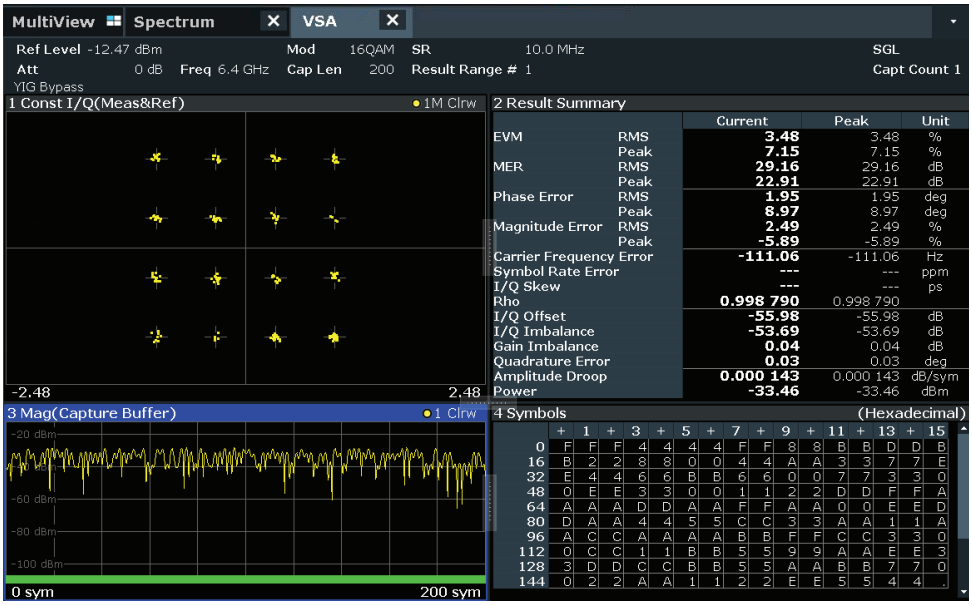


Figure 5.34: Measured constellation for 16-QAM using raised cosine pulses.

where IRR, LOFT, PN, SNR, SFDR, IM3 represents the image rejection ratio, LO feed-through, integrated SSB phase noise, signal-to-noise ratio, spurious free dynamic range (dominated by DAC HD2) third-order intermodulation all expressed in dBc. Using the values from the previous measurements, an IRR of $-42\,\mathrm{dBc}$, LOFT of $-36\,\mathrm{dBc}$, PN $-50\,\mathrm{dBc}$, SNR $-48\,\mathrm{dBc}$, SFDR $-42\,\mathrm{dBc}$, IM3 $-47\,\mathrm{dBc}$ results in an EVM of $2\,\%$. However, the measured EVM is $3.48\,\%$ corresponding to an equivalent magnitude error ratio (MER) of $29\,\mathrm{dB}$. The measured EVM deviates from the calculated value due to excessive phase error of $1.95°$ and magnitude error of $2.49\,\mathrm{dB}$ dominated by the non-linearity of the DAC.

5.6.4. Comparison with state-of-the-art

Table 5.2 summarizes the performance of the chip. Compared to the state-of-the-art [130], this work incorporates a wideband RF output to support multiple qubit technologies, frequency multiplexing for scalability with low power consumption and a digitally intensive back-end with an arbitrary-waveform generation memory of >40k points and the support of an instruction set for low-latency quantum-algorithm execution.

5.7. Conclusion

The cryogenic microwave signal generator demonstrated in this work comprises an integrated digital controller that can translate qubit gate operations into the microwave signals necessary for the execution of quantum algorithms. The chip is

Table 5.2: Comparison table

Parameter	This work	JSSC'19[130]	RSI'17[21]	RT setup
Operating temperature	3 K	3 K	300 K	300 K
Compatible qubit platforms	Spin qubits & Transmons	Transmons$	Transmons$	Spin qubits$
Qubit frequency	2-20 GHz	4-8 GHz	-	<20 GHz
Channels	32 (128 with 4 TX)	1	4	1
FDMA	Yes, SSB	No	Yes, SSB	No
Data Bandwidth	1 GHz	400 MHz	960 MHz	520 MHz
SFDR*	>42 dB	N/A	-	70 dB
IM3 (Δf = 10 MHz)	>47 dB	N/A	-	-
SNR (BW=25 MHz)	48 dB	N/A	-	-
Image & LO leakage calibration	On-chip	Off-chip	Yes	-
Phase correction	Yes	No	No	No
Fidelity (expected&)	99.99 %	-	-	-
Waveform/ Instructions	Upto 40960 pts AWG	Fixed 22 pts symmetric	-	16M points AWG
Instruction set	Yes	No	Yes	Yes
Power/TX	Analog:1.7 mW/qubit@ Digital:330 mW#	Analog <2 mW/qubit	-	850 W
Chip area/TX	4 mm^2	1.6 mm^2	Discrete	Rack-mount
Technology	Intel 22 nm FinFET CMOS	28 nm bulk CMOS	-	-

* single tone excluding residual LO leakage
@ including LO & clock driver, only RF-Low active (f_{LO} = 6 GHz)
# can be reduced with clock gating
$ no information is available regarding compatibility with other qubit technologies
& extrapolated from electrical performance and simulations
SFDR, IM3 and SNR values are valid for the entire 2-20 GHz range

capable of controlling 128 qubits with a $99.99\,\%$ theoretical fidelity thanks to the spectral purity of the generated signals. The achieved power efficiency $330\,\mathrm{mW}$ for the digital blocks and $1.7\,\mathrm{mW}$ per qubit for the analog blocks enabled by a digitally intensive architecture and the frequency multiplexing allows for operating the chip at 3 K within the cooling capabilities of standard cryogenic refrigerators.

5.7.1. Future improvements

All memory blocks except NCO phase update registers (Z-corr.) are implemented using SRAM. The high power consumption of the digital circuitry of the cryo-controller is caused due to the lack of clock gating in registers, thus causing them to continuously operate instead of just during the read/write cycle. This could easily be reduced by further optimizations (e.g. by replacing more registers with SRAM memory and by adding clock gating), that were not yet included in the first generation cryo-controller and has been implemented in the next-generation design [131]. Based on the Cadence simulation with clock-gating, the power consumption of the digital circuitry should be lower than $40\,\mathrm{mW}$ instead of $330\,\mathrm{mW}$ in the current design. Migrating to a finer technology node would result in further substantial power savings [93].

Moreover, this chip was designed to address both transmons and spin qubits and hence an ultra-wide output frequency range was supported i.e. 2 to $20\,\mathrm{GHz}$ with an LO frequency of 2.5 to 14.5 GHz. Once the qubit frequency is fixed within a few GHz range, the power consumption of the analog circuitry can be significantly reduced to limit the power consumption to $\sim 20\,\mathrm{mW}$ instead of $54\,\mathrm{mW}$. In the current architecture, such power savings can be achieved by: (1) Eliminating the output drivers and compensating the gain loss by increasing the matching network impedance transformation, as allowed by the reduced frequency range, which also results in a higher mixer load and consequently lower VGA bias current (2) Replacing the folded-current topology of the anti-aliasing filter with a stacked topology. (3) Replacing the active balun before the LO drivers with a passive matching network. Further power savings could be achieved by architecture improvements, e.g. by replacing the gm-C filter with a passive filter, thus eliminating the power consumption of the filter [93]. Moreover, the integration of a PLL can eliminate I/Q active baluns completely.

6

Cryogenic control of a two-qubit processor

Background: *In the previous chapter, experimental results indicated that the signal specifications required to achieve a gate fidelity of 99.99% are met by the controller. However, those specifications were obtained from the Hamiltonian simulation of the qubits together with the system-level model of the controller. To reinforce this claim, the controller should be used to directly control the qubits.*

Abstract: *This chapter presents the first demonstration of a CMOS-based cryogenic controller for spin qubits operating at* $4\,\mathrm{K}$*. We find that the performance of the cryo-controller is similar to the current room temperature qubit control electronics with a gate-fidelity of* $\sim$ *99.7%, limited by the qubits.*

Summary: *After a concise introduction, Section 6.2 describes the measurement setup of the cryogenic controller and qubit device. Section 6.3 elaborates on the fabrication details of the two-qubit quantum device. Next, the biasing, control and readout implementation specific to this qubit sample is shown in Section 6.4. Microwave pulses for qubit control are calibrated using Rabi oscillation, Ramsey and AllXY experiment, presented in Section 6.5. Several single qubit experiments such as two-axis control using a Ramsey-style experiment, Quantum State Tomography, Randomized Benchmarking are implemented using the cryo-controller as shown in Section 6.6. Two-qubit experiments including the execution of the Deutsch-Jozsa algorithm using the controller are presented in Section 6.7.*

Parts of this chapter have been published in *Nature* [132]. J. P. G. van Dijk and the author have built the experimental setup for cryogenic qubit control and programmed the experiments on the controller. X. Xue and the author have executed the experiments and analyzed the data.

6.1. Introduction

CMOS-based circuits operating at cryogenic temperatures have been shown successfully interface with quantum processors for qubit control. Towards that goal, a cryogenic pulse modulator for controlling superconducting qubits was presented in [130]. However, the experiments were limited to Rabi oscillation and Ramsey pulsing, along with the requirement for one controller per qubit. Instead of modulating the pulses at cryogenic temperatures, a cryogenic de-multiplexer chip has been presented to route the control signals to the quantum dots inside the dilution refrigerator [133]. The chip is based on switched capacitors and wire-bonded to a quantum dot chip to time demultiplex a single room temperature (RT) control signal to several quantum dots. Similarly, switched capacitors circuits were integrated on the same die as the Si/SiGe-based quantum dots for biasing the gates, leveraging the capacitors' lower leakage at cryogenic temperature $\sim 2.8\,\mu\mathrm{V/s}$ [134] which is almost 6 orders of magnitude lower than the leakage rate at RT. At a similar integration level, a ring oscillator has been fabricated with quantum dots on a single chip to generate microwave signals [90]. However, no qubit measurements have been presented to validate the functionality of the chip.

Although the above-mentioned work show CMOS-based integrated circuits targeting spin-qubit control, the presented experimental results are limited to measurement with quantum dots and proposals for future integration with qubits. In this work, we use the cryogenic controller operating at $3\,\mathrm{K}$ and demonstrate extensive experiments with qubits operating at $20\,\mathrm{mK}$, both inside a dilution refrigerator. With the advent of qubits operating at $1\,\mathrm{K}$[16], this work is a major step towards the integration of control electronics and qubits on the same chip/package to realize an integrated quantum computer.

6.2. Interfacing the cryo-controller with qubits

The qubit is placed at mK temperature to have the best possible performance, implying the most stringent specifications for the control signals, thus helping to benchmark the controller. The measurement setup is shown in Fig. 6.1. A Niobium Titanium (NbTi) coax cable, without attenuators, is used between the $3\,\mathrm{K}$ and $20\,\mathrm{mK}$ stages.

The quantum dot device is placed at the mixing chamber ($\sim 20\,\mathrm{mK}$) of a dilution refrigerator (Bluefors XLD). Voltage pulses onto gates RP and LP are generated by the AWG at room temperature (RT) and go through a low-pass filter (Minicircuits) and attenuators before reaching the device. These pulses are used to control the electrochemical potentials of the quantum dots and load/unload electrons from/to the electron reservoir (elaborated in Section 6.4.1). A programmable Dual-pole-dual-throw (DPDT) microwave switch at $3\,\mathrm{K}$ is used to connect gate MW either to a vector signal generator (VSG) at RT or to the cryo-controller at $3\,\mathrm{K}$ (represented as two boxes next to the switch) through a 12-$14\,\mathrm{GHz}$ band-pass filter to filter out wide-band noise. The mechanical switch can also be configured to send the output signals from the cryo-controller to the oscilloscope and the spectrum analyzer at RT for electrical characterization in time and frequency domain. This enables proper characterization of the chip performance and the comparison of the qubit control by the

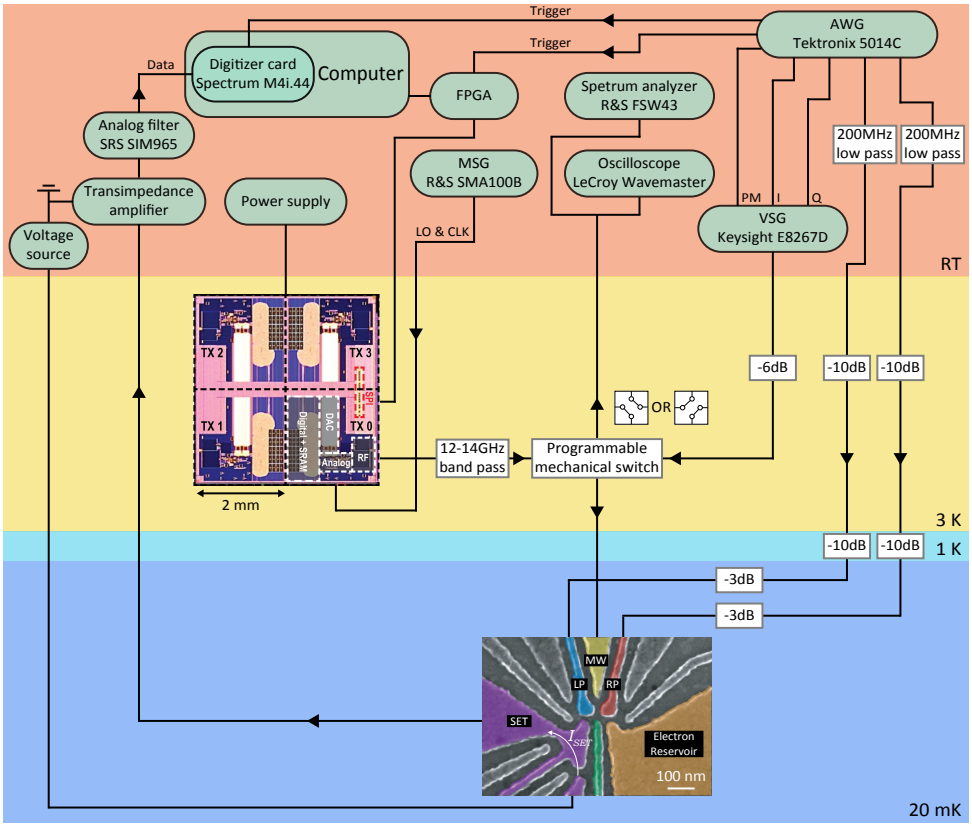


Figure 6.1: Experiment setup showing the placement of the cryogenic controller, qubit device and peripheral devices used for qubit control and readout.

room-temperature equipment and the designed chip. The single electron transistor (SET) next to the quantum dots is voltage biased and the current signal (I_{SET}) through it is converted to a voltage signal through a transimpedance amplifier and digitized by a digitizer card after an analog low-pass filter employed to remove out-of-band ($> 10\,\mathrm{kHz}$) noise. I_{SET} is sensitive to the charge occupation of the quantum dots, allowing binary single-shot readout of the qubit states via spin-to-charge conversion (elaborated in Section 6.4.1).

The cryo-controller is programmed via a field-programmable gate array (FPGA) placed at RT to generate the microwave bursts using an external local oscillator (LO) signal and a clock (CLK) signal from a microwave signal generator (MSG) at RT. The FPGA is used as the master to synchronize the chip with the other instruments used for qubit readout/initialization and is connected to the host PC, which sends the data that needs to be uploaded to the cryo-controller over the SPI. The FPGA configures the cryo-controller (e.g. frequency tuning word of the numerically controlled oscillators), programs the various memories inside the cryo-controller (e.g. envelope memories,

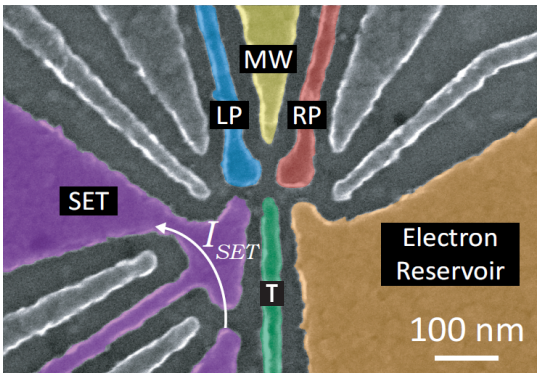


Figure 6.2: SEM image of the two-qubit processor with two quantum dots located underneath gates LP (blue) and RP (red). Multiplexed microwave signals are sent to gate MW (yellow) to control both qubits. Gate T (green) is used to tune the coupling between the qubits.

instruction tables and instruction lists), and controls the start of the execution of the instruction list (for memory information, see Chapter 5). The instruction list integrated in the cryo-controller does not support classical instructions that allow for e.g. branching or wait statements, as required for performing certain qubit experiments and for synchronization with other equipment. Therefore, switching between different instruction lists and synchronization with the rest of the equipment is controlled by two trigger lines from the AWG to the FPGA (shown in Fig. 6.1). The application of the *execute* trigger starts the execution of the instruction list that is programmed in the cryo-controller, for performing repeated measurements. The application of the *sweep* trigger loads the next instruction list from the FPGA SRAM into the cryo-controller's instruction list.

6.3. The quantum processor

The quantum processor used in this work is made of a double quantum dot (DQD) electrostatically confined in a $10\,\mathrm{nm}$-thick Si/SiGe quantum well as shown in Fig. 6.2.

6.3.1. Si/SiGe heterostructure.

In Si/SiGe heterostructures, the 2DEG is accumulated at the buried interface between a tensile strained Silicon quantum well and a $Si_{1-x}Ge_x$ barrier. The silicon quantum well is isotopically enriched to ^{28}Si for long quantum coherence, where the electrons populate the quantum well via top-gates. To accommodate for the lattice mismatch between Si and Ge, the silicon quantum well is deposited on a strain-relaxed SiGe buffer obtained by gradually increasing the Ge concentration in the SiGe alloy [135].

The quantum processor is made by gate-confined quantum dots in an undoped ^{28}Si/SiGe heterostructure, which is grown using a reduced pressure chemical vapor deposition reactor (ASM Epsilon 2000). First, a $Si_{1-x}Ge_x$ buffer layer (with x linearly

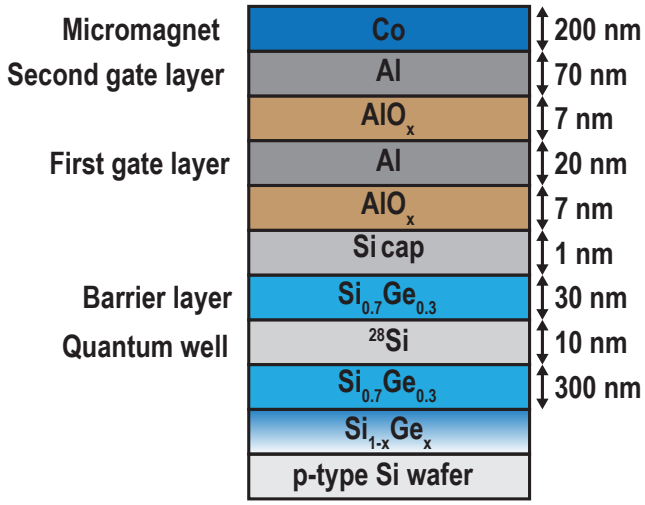


Figure 6.3: Wafer stack cross-section schematic with corresponding layer thicknesses.

increasing from 0 to 0.3) is grown on top of a p-type natural Si wafer, followed by a 300 nm strain-relaxed $Si_{0.7}Ge_{0.3}$ layer. Then a 10 nm isotopically purified tensile-strained ^{28}Si (with 800 ppm residual ^{29}Si concentration) quantum well is grown, followed by a 30 nm strain-relaxed $Si_{0.7}Ge_{0.3}$ barrier layer. Finally, a 1 nm sacrificial Si cap is grown on top, as shown in Fig. 6.3.

6.3.2. Quantum dot device fabrication

Fabrication of quantum dots relies on overlapping gate structures for tightly spaced quantum dots with gate tunable tunnel barriers. On top of the heterostructure, a 7 nm AlO_x layer is deposited using atomic layer deposition (ALD), followed by a 20 nm Al metal film, which is patterned using electron beam lithography to define a first gate layer. This layer (green in Fig. 6.4 (left)) is used to populate electrons and shape the potential landscape at the buried interface between the barrier layer and quantum well. Next, another 7 nm AlO_x layer is deposited, followed by a 70 nm Al layer which uniformly covers the tightly-spaced quantum dot area. This Al layer (purple in Fig. 6.4 (left)) forms the screening gate and acts as a capacitor to absorb charge jumps and hence, protect the sample from charge noise. Finally, a 200 nm Co film is deposited and patterned into a micro-magnet, as shown in Fig. 6.3.

6.3.3. Micro-magnet

The micro-magnet on top of all the metallic gates is made of cobalt for convenience of fabrication and high enough maximum permeability. The magnet is designed to induce a spatially inhomogenous stray field at the quantum dots when magnetized along an external magnetic field (B_{EXT}) (in $\hat{z}$ direction) [99]. It is magnetized by

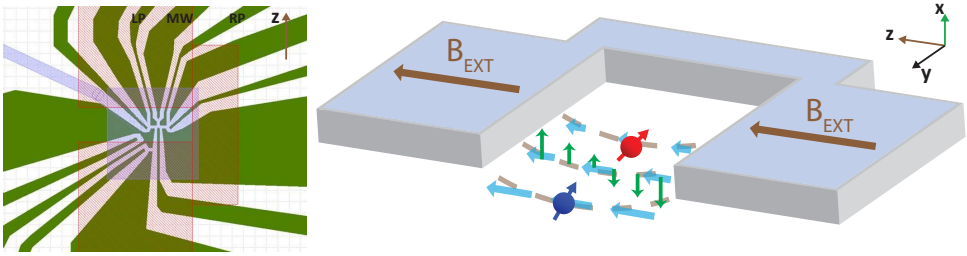


Figure 6.4: Schematic (left) showing the first and second Al gate layers in green and purple, respectively. A Cobalt micro-magnet is located on top of the metallic gates (light red shaded area). The micromagnet and the corresponding spin-coupling fields generated is shown on the right.

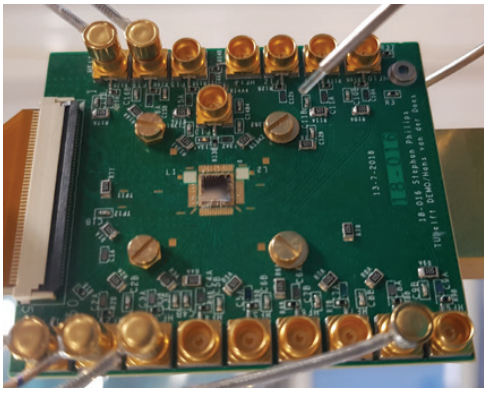


Figure 6.5: PCB hosting the qubit chip.

sweeping B_{EXT} from 0 to $3\,\mathrm{T}$ and then swept down to be kept at $380\,\mathrm{mT}$. The magnetized micro-magnet provides a magnetic field (brown dashed lines) which has a longitudinal ($\hat{z}$) component (light blue arrows) with a field gradient along the double quantum dots. This magnetic field gradient makes the Zeeman splittings (resonance frequencies) of the two qubits different by $\sim 110\,\mathrm{MHz}$. When a microwave pulse is sent to the device through the gate MW, the wave functions of the electrons are oscillating in the $\hat{z}$ direction. Additionally, the micro-magnet also induces a transverse ($\hat{x}$) magnetic field gradient (green arrows). If the microwave frequency is in resonance with the qubit's frequency, the electron feels an effective oscillating magnetic field in the $\hat{x}$ direction, which induces electron dipole spin resonance (EDSR).

The qubit device is wire-bonded onto a printed circuit board (PCB) and placed at the mixing chamber ($\sim 20\,\mathrm{mK}$) of a dilution refrigerator as shown in Fig. 6.5 A Flexible Flat Cable (FFC) connector is used for the DC bias, while several SMP connectors are used to inject the RF signals.

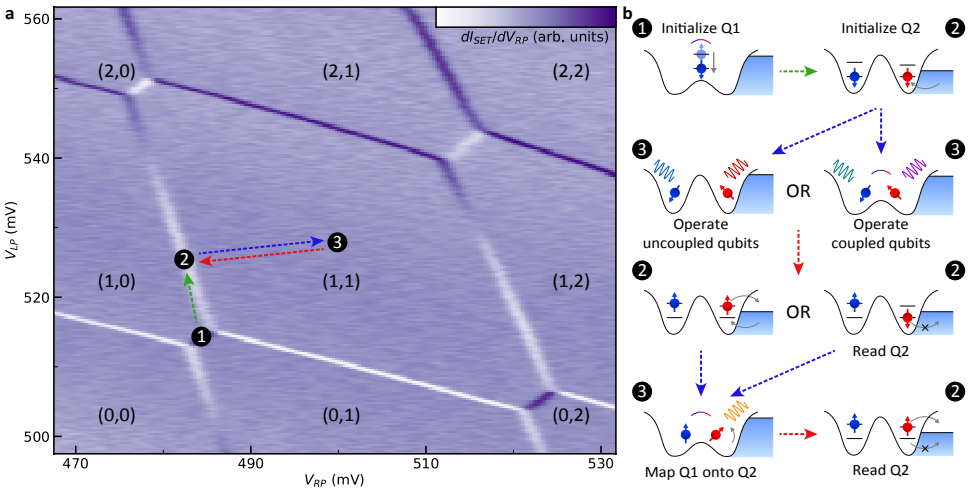


Figure 6.6: Pulsing scheme in qubit experiments showing charge stability diagram (left) and corresponding schematic representation (right) of the DQD system during the experimental cycle.

6.4. Qubit control and readout mechanism

The basics of spin-qubit control have been presented in Chapter 4. In this section, device-specific qubit control information is provided. In this device, two single electrons are locally accumulated underneath LP and RP plunger gates, shown in blue and red in the scanning electron microscope (SEM) image in Fig. 6.2.

6.4.1. Pulsing scheme for qubit experiments

Fig. 6.6 (left) shows the charge stability diagram of the DQD system, depicting the differential current signal (dI_{SET}/dV_{RP}) and charge occupation ((M, N), indicating M electrons in the dot below LP and N electrons in the dot below RP) as a function of the voltages applied to gate LP (V_{LP}) and gate RP (V_{RP}). The three main stages of a typical pulse sequence are marked by the numbered circles.

Fig. 6.6 (right) shows the schematic representations of the DQD system during the experiment cycle. Q_1 is initialized by pulsing the DQD to the charge transition line between (1,0) and (0,1) (stage-1). As this is a spin-relaxation hotspot, it enables fast relaxation of Q_1 to its ground state (spin-down) [136]. Then Q_2 is initialized by pulsing it to the transition line between (1,0) and (1,1) (stage-2), where the Fermi energy of the electron reservoir is placed in between the two spin states of Q_2. It allows a spin-down electron to tunnel into the dot but forbids spin-up electrons from tunneling in, a mechanism called spin-selective tunneling. During the qubit operations, the system is pulsed to the middle of the (1,1) region (stage-3) so both electrons are well-confined inside the DQD. The barrier (gate T) voltage is used to turn off the exchange coupling between the two spins in the operation of uncoupled qubits (all measurements in Section 6.6) and to turn on the coupling for two-qubit logic operations (all measurements in Section 6.7). After the operations, Q_2 state is read out via

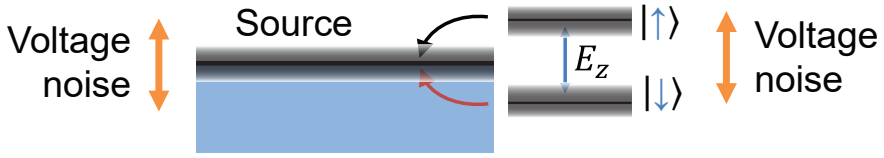


Figure 6.7: Readout visibility affected by noise on the source contact.

spin-selective tunneling and reinitialized into the spin-down state (stage 2). The state of Q_1 is read out by mapping its state onto Q_2 via a two-qubit $CROT$ gate (stage-3), followed by Q_2 readout again (stage-2).

6.4.2. Qubit control

By applying an external magnetic field of $380\,\mathrm{mT}$, combined with the longitudinal magnetic field induced by a micro-magnet on top of the DQD, we can encode the qubit states into the Zeeman split states of the two electrons, where spin-up is defined as $|1\rangle$ and spin-down is defined as $|0\rangle$ Fig. 6.4. The resonance frequencies of Qubit 1 (Q_1, underneath gate LP) and Qubit 2 (Q_2, underneath gate RP) are $13.62\,\mathrm{GHz}$ and $13.51\,\mathrm{GHz}$, respectively. Rotations around the $\hat{x}$ and $\hat{y}$ axes are implemented by sending microwave bursts through gate MW (yellow), which drives electric dipole spin resonance (EDSR) enabled by the transverse magnetic field gradient from the micro-magnet [137, 138], while the rotation around the $\hat{z}$ axis (phase control) is achieved by changing the reference frame in software [139].

6.4.3. Qubit readout

The readout scheme is described in Fig. 6.6. After each operation sequence, Q_2 is measured by spin-selective tunnelling to the electron reservoir, where a spin-up ($|1\rangle$) electron can tunnel out and a spin-down ($|0\rangle$) electron is blockaded from tunnelling out. Such a spin-to-charge conversion changes the charge occupancy in the quantum dot conditional on the spin state. This in turn changes the current signal in an adjacent capacitively coupled single-electron-transistor (SET) [13]. Single-shot readout of the qubit state can be done by thresholding the current signal through the SET [13]. At the end of the measurement, either an electron with state $|1\rangle$ will tunnel out and another electron from the reservoir will tunnel into the quantum dot acquiring $|0\rangle$ or an electron with state $|0\rangle$ will stay in the dot. Hence, this measurement protocol automatically serves the purpose of qubit initialization to $|0\rangle$ for the following experiment. Q_1 is tuned to be only weakly coupled to the SET, which serves as the electron reservoir for Q_1. This is to minimize the back-action from the SET, but also makes it less efficient to read out Q_1 by spin-selective tunnelling to the SET. Therefore, with Q_2 reinitialized, a $CROT$ gate is applied by the cryo-controller to map the state of Q_1 onto Q_2. Then Q_1 is readout by measuring Q_2 again [140] as depicted in Fig. 6.6.

Since the energy levels of the qubit device are aligned with the reservoir and the tunnelling of the electron depends on the state of the qubit, any excessive voltage noise on the gate can affect the readout visibility/fidelity (difference between the max

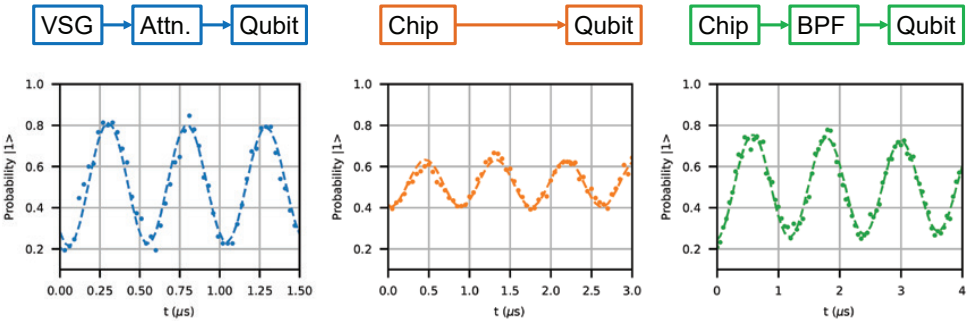


Figure 6.8: Readout visibility improved using a bandpass filter, similar to what is measured with RT control electronics.

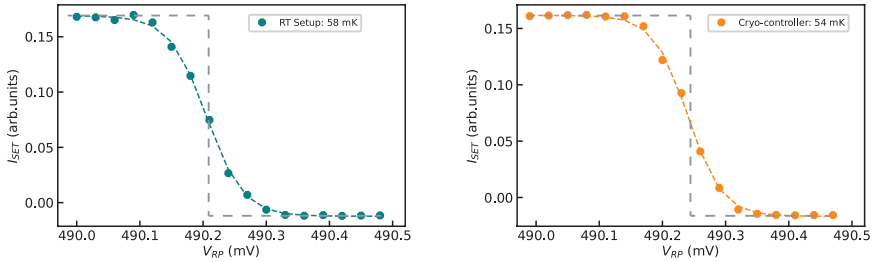


Figure 6.9: Electron temperature measured with (a) VSG at RT with 6 dB attenuation before connecting to qubits and (b) Cryo-controller at 3 K directly connected to qubits.

and min value of current when reading out $|0\rangle$ or $|1\rangle$) as shown in Fig. 6.7.

This can be improved by adding a bandpass filter (BPF) to remove the out-of-band noise from the controller which is generated due to the ultra-wide frequency range (e.g. 2-15 GHz) of the output matching networks. The improvement in readout visibility can be compared between three Rabi oscillation experiments i.e. room temperature control electronics and with/without the band-pass filter (BPF) at the output of the cryo-controller, as shown in Fig. 6.7. Finally, the readout fidelity of Q_2 is mainly limited by the thermal broadening of the electron reservoir [13], common to the readout protocol used for this work [13]. This has been quantified by measuring the electron temperature in the following subsection. The readout fidelity of Q_1 is limited by both the error in the $CROT$ gate and in the readout of Q_2. Thus the readout visibility of Q_1 is lower than Q_2.

6.4.4. Electron temperature

The effect of the controller's output noise on the qubits can be quantified by measuring the electron temperature (T_e) in a quantum dot. At 0 K, the Fermi-Dirac distribution of the SET is a vertical line. However, as the temperature increases in the quantum dot, it causes thermal broadening as shown in Fig. 6.9. This can be used to extract the electron temperature. The SET current signal (I_{SET}) as a function of RP voltage

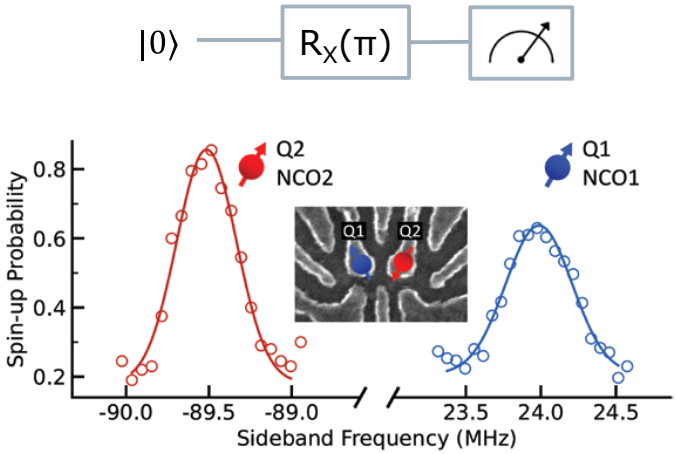


Figure 6.10: Coarse frequency sweep.

(V_{RP}) measured at the charge transition between (1,0) and (1,1) can be expressed as:

$$I_{SET} = \frac{1}{e^{\alpha V_{RP}/KT_e} + 1}, \tag{6.1}$$

where K is the Boltzmann constant, T_e is the electron temperature, α is the gate lever arm to convert a voltage fluctuation on V_{RP} to an energy fluctuation (for extraction of the lever arm, see supplementary of [141]).

Fig. 6.9 shows the SET current signal (I_{SET}) as a function of RP voltage (V_{RP}) measured at the charge transition between (1,0) and (1,1) when the quantum device is connected to the RT vector signal generator (VSG) or to the cryo-controller (at zero magnetic field) using a microwave switch (Fig. 6.1). The electron temperatures are derived by fitting the curves with the Fermi-Dirac distribution, with a lever arm of $0.172\,\mathrm{eV/V}$. The measurements indicate that the output noise of the cryo-controller does not affect the electron temperature more than the noise from the RT setup reduced by $6\,\mathrm{dB}$ at the $3\,\mathrm{K}$ plate.

6.5. Calibration of pulses

Before the execution of qubit experiments, the microwave pulses need to be calibrated to account for the drift in qubit frequency. This is done by directly applying the pulses to the qubits and tuning their amplitude and frequency based on the results of the following experiments.

6.5.1. Finding the qubit resonance frequency

The first step towards qubit control is to find the resonance frequency of the qubit. This frequency can be initially estimated from the external magnetic field. However, the high quality factor of the system and the additional magnetic field gradient created by the micromagnet makes it difficult to estimate the accurate resonance frequency

with a few Hz resolution, necessary for high-fidelity qubit control. To obtain the qubit resonance frequency, an experiment can be carried out by applying a pulse of a certain amplitude and sweeping the frequency over a certain range, also known as *pulsed spectroscopy*. When the driving field is on resonance with the transition frequency of the electron, the measured probability is maximum. This experiment can be readily implemented by sweeping the frequency tuning word of the NCO as shown in Fig. 6.10. In this example, the frequency is swept over a span of $3\,\mathrm{MHz}$ in 40 steps, as this experiment only provides a rough estimate of the frequency.

6.5.2. Rabi oscillation

To demonstrate qubit control, the oscillatory behavior of a two-level quantum system can be produced in a Rabi oscillation. In this experiment, the qubit is rotated around the x-axis by a certain angle determined by the amplitude and duration of a resonance microwave pulse. The amplitude of the pulse determines the speed of rotation, i.e. the Rabi frequency.

There are two versions of this experiment, i.e. *"time Rabi"* and *"power Rabi"*. In *time Rabi*, a constant power pulse is applied for an increasing period to rotate the qubit by an increasing angle around the x-axis. When the qubit state is measured by projecting the state on the z-axis, an oscillatory behavior is observed. Contrary to time Rabi, in *power Rabi*, the duration of the pulse is fixed and the amplitude is varied over time. Since the amplitude defines the speed of rotation, an increasing amplitude causes the qubit to rotate faster. In combination with a fixed pulse duration, a faster rotation causes an increased rotation angle around the x-axis, leading to an oscillatory response.

In this work, *time Rabi* is chosen, wherein the qubit is first initialized to state $|0\rangle$, then excited by a rectangular microwave pulse with a given duration and finally the quantum state is readout. By varying the pulse duration and averaging the results over multiple runs, a Rabi frequency of $1\,\mathrm{MHz}$ and $400\,\mathrm{kHz}$ at $13.4\,\mathrm{GHz}$ (RF-low output) has been measured (Fig. 6.11). The maximum Rabi frequency is limited by the peak power generated by the controller at the respective frequencies (measurement results shown in Chapter 5). To perform the experiment, the pulse duration was adjusted at the maximum output power at the qubit resonance frequency to obtain a π-rotation. All other pulse duration for various rotation angles were interpolated from this value.

A Rabi experiment serves as a general check of the qubit and control electronics operating properly. Imperfect pulse parameters such as high level of spurious tones resulting from non-linearity or mixer IQ leakage would cause a distorted curve[142]. Similar performance obtained with the room-temperature control validates the effectiveness of the cryo-CMOS controller.

6.5.3. Ramsey experiment

As explained in the beginning of Section 6.6, the rough frequency of the qubit is first determined by sweeping the frequency of a pulse while observing the qubit rotation. However, the accuracy of such an experiment is limited to a few $100\,\mathrm{kHz}$ due to the broad peak of the measured probability. A precise qubit frequency can be measured

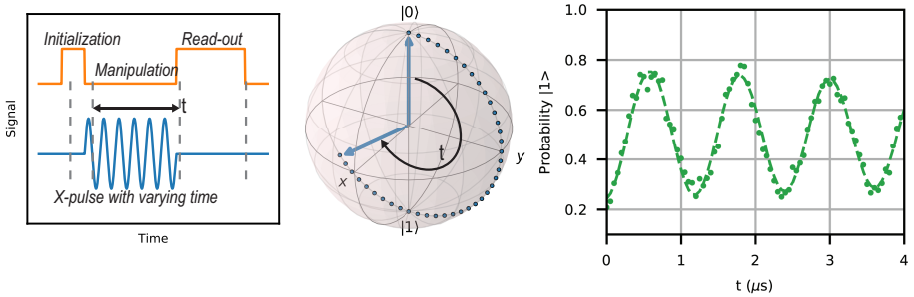


Figure 6.11: Rabi oscillation experiment showing the pulses (left), the qubit rotation on the bloch sphere and the measured results (right) by projecting the qubit state onto z-axis.

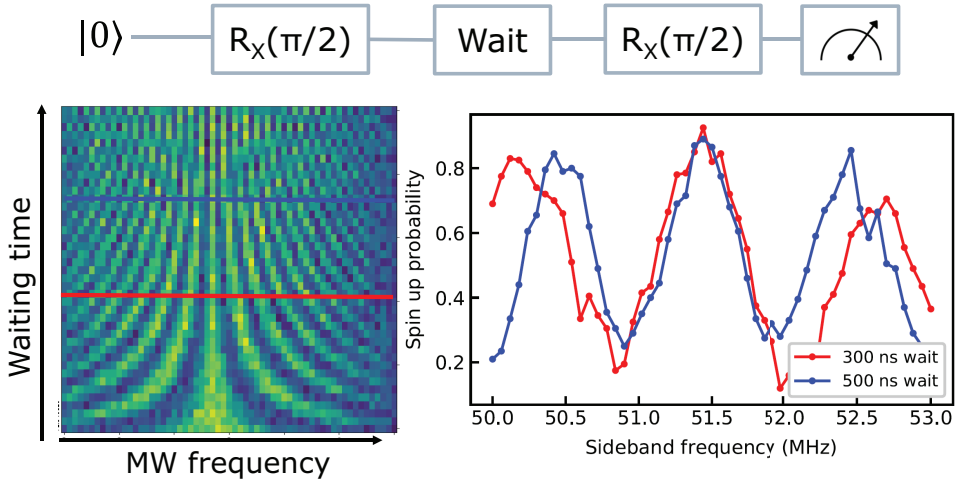


Figure 6.12: Ramsey experiment to obtain accurate qubit resonance frequency.

using the Ramsey experiment, which is also used for the calibration of instruments like atomic clocks[143].

The core idea behind this experiment is the fact that a difference between the qubit frequency (ω_0) and the controller output frequency (ω) (also known as detuning $\Delta = \omega - \omega_0$) is equivalent to the continuous application of a z-gate at a rate Δ. Hence, tiny detunings can be measured by integrating this detuning as a function of time, limited by the dephasing rate (T_2^*).

In this experiment, the qubit is initialized to $|0\rangle$ and then brought to a superposition state at the equator of the Bloch sphere by applying a $\pi/2$ pulse. The qubit is then allowed to evolve for a certain period around the z-axis. Finally, another $\pi/2$ pulse is applied and the qubit is measured. An on-resonance pulse would result in a final state of $|1\rangle$, wheres if there is a detuning, the qubit will oscillate between the ground and the excited state as a function of the waiting time. By measuring

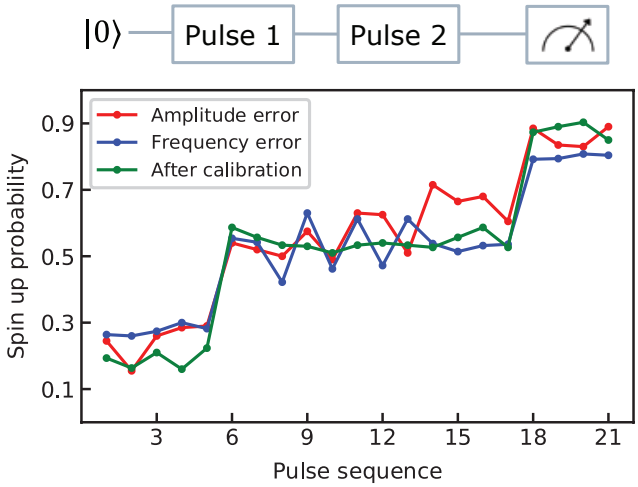


Figure 6.13: AllXY experiment to calibrate the amplitude and frequency of the microwave pulses.

the spin up probability while sweeping the microwave frequency around the qubit resonance and waiting time between the pulses, a 3D plot is generated as shown in Fig. 6.12 (left). Note that, this experiment has been implemented using RT control electronics due to insufficient memory of the cryo-controller required to implement a 2D sweep. However, two Ramsey experiments are implemented at specific waiting times (corresponding to red and blue lines) using the cryo-controller, generating a 2D plot shown in Fig. 6.12 (right). The frequency corresponding to the center peak indicates the qubit resonance frequency. A longer waiting time (blue line with respect to red line) produces a narrow linewidth providing a more accurate estimation of the resonance frequency.

6.5.4. AllXY

The pulses for single-qubit rotations are precisely calibrated using the AllXY experiment [142]. In the AllXY experiment, 21 different pairs of single-qubit gates from the set $\{I, X, Y, X^2, Y^2\}$ are applied to a qubit initialized to $|0\rangle$, as shown in Eq. (6.2).

$$\begin{aligned}&['I','I'],['Xpi','Xpi'],['Ypi','Ypi'],['Xpi','Ypi'],['Ypi','Xpi'],['X','I'],['Y','I'],\\&['X','Y'],['Y','X'],['X','Ypi'],['Y','Xpi'],['Xpi','Y'],['Ypi','X'],['X','Xpi'],\\&['Xpi','X'],['Y','Ypi'],['Ypi','Y'],['Xpi','I'],['Ypi','I'],['X','X'],['Y','Y']\end{aligned} \quad (6.2)$$

Here, I is the identity operation, X and Y are $\pi/2$ rotations around the $\hat{x}$ and $\hat{y}$ axis respectively, and X^2 and Y^2 are π rotations. The final state $\hat{z}$-projection $\langle\sigma_z\rangle$ takes values from $\{0, 0.5, 1\}$ under perfect operations. Any miscalibration in the amplitude, frequency or phase of the pulse results in deviations from the ideal outcome (green curve), as shown in Fig. 6.13. An amplitude error would result in a positive or negative

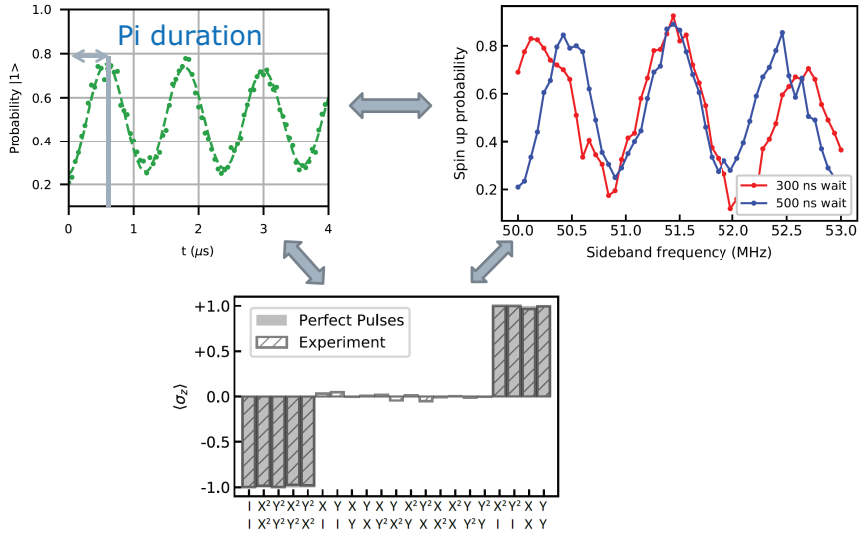


Figure 6.14: Calibration cycle.

6

slope of the flat region at the center (red curve) due to over or under rotation. In Fig. 6.13, for example, the over-rotation caused by the amplitude error in the red curve can be fixed by reducing the pulse duration from 295 ns to 270 ns to obtain the green curve. However, a frequency error would show up as a zig-zag behavior (blue curve) and can be corrected by a Ramsey experiment with a longer waiting time and thus, higher accuracy.

6.5.5. Calibration Routine

For all the following experiments, a calibration routine is followed to ensure the amplitude and phase accuracy of the pulses as shown in Fig. 6.14. First, a Ramsey sweep is performed to obtain the resonance frequency. Second, the period of the Rabi oscillation at the maximum output power provides the duration of a π rotation and the other gates are calculated from this accordingly. Finally, an AllXY experiment is carried out to measure the accuracy of the frequency and duration.

The result of this AllXY experiment is used to calibrate the amplitude and phase of the pulses. This calibration cycle is repeated until enough accuracy is achieved, as confirmed by the AllXY experiment.

6.6. Single qubit experiments

Once the calibration is completed, the controller can be used to execute a Ramsey-style experiment to demonstrate coherent control over two axes[94].

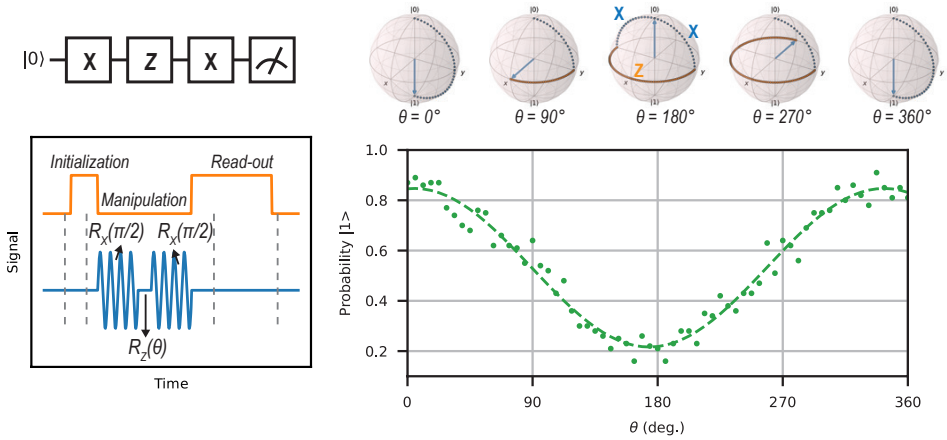


Figure 6.15: Explanation and measurement results of the Ramsey-style experiment.

6.6.1. Ramsey-style experiment

In this experiment, the qubit is initialized to state $|0\rangle$ and two rotations around the X-axis are then applied $\left(R_X(\frac{\pi}{2})\right)$ sandwiched by a Z-gate of varying angle from $0°$ to $360°$ $(R_Z(\theta))$. This resulted in a cosinusoidal variation in the measured $|1\rangle$ probability (Fig. 6.15), as expected. The X rotation is implemented by a rectangular microwave pulse with a duration directly proportional to the rotation angle as shown in the Rabi oscillation experiment. Since the electron rotates around the Z-axis under the influence of an external magnetic field, a Z-rotation can be achieved by waiting for a certain time proportional to the rotating angle, without generating any signal. However, in this experiment, the Z-rotation is implemented by updating the reference phase of the NCO (applying a digital phase offset), which continuously keeps track of this phase evolution. The experimental data closely tracking the theoretical expectation proves the coherent qubit control and the capability of correctly executing any type of single-qubit gate.

6.6.2. Crosstalk in FDMA

As discussed in Chapter 4, an off-resonance pulse can cause unintended rotation on the qubit based on its frequency separation from the qubit. The unintended X/Y rotation as well as Z-rotation can be quantified as shown in Fig. 6.16. The image shows the infidelity due to an off-resonance pulse versus the normalized (with respect to Rabi frequency) frequency separation from the qubit. Comparing the two plots with rectangular and Gaussian pulses, it can be observed that shaped pulses can be used to mitigate the X/Y crosstalk error. However, Z-error due to crosstalk cannot be mitigated by pulse shaping and its compensation will be discussed in Section 6.6.4.

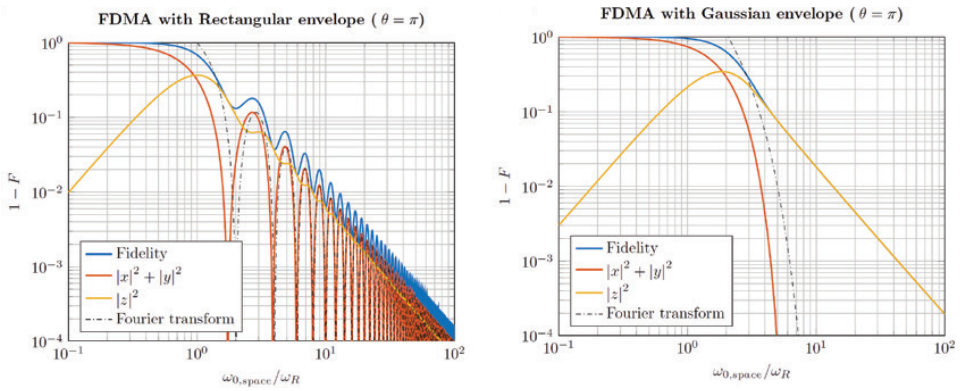


Figure 6.16: Infidelity of unaddressed qubit versus frequency separation (normalized to Rabi frequency) from the addressed qubit due to X/Y and Z error when applying rectangular (left) or Gaussian (right) pulses. Image is taken from [102].

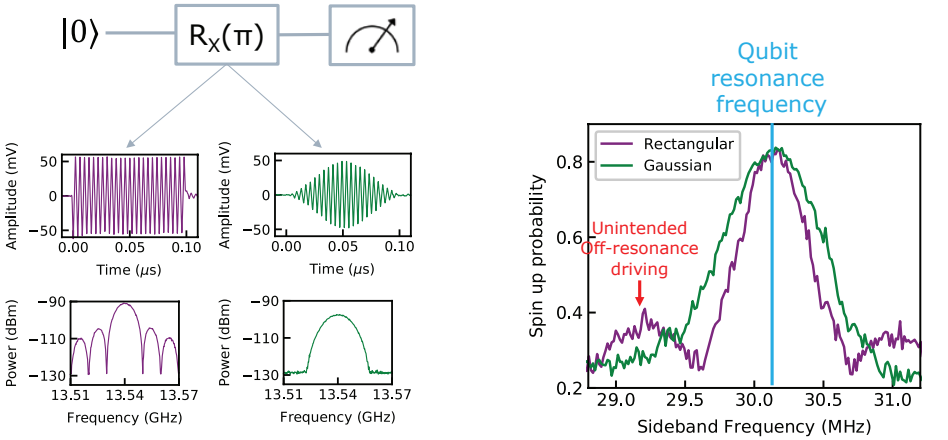


Figure 6.17: Left: Rectangular (purple) and Gaussian (green) shaped bursts before up-conversion (base-band signal) and the corresponding spectra after up-conversion. Right: Qubit response for different burst envelopes, obtained when sweeping the NCO frequency around the qubit resonance.

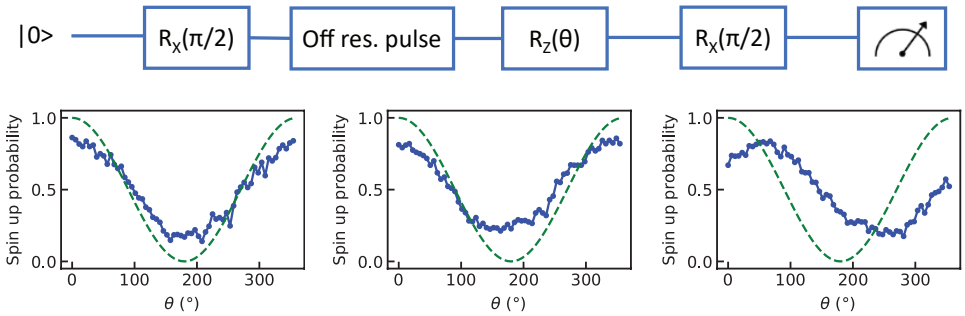


Figure 6.18: Quantifying the Z error due to off-resonance pulse at various offset frequencies i.e. 3 MHz (left), 2 MHz (middle), 1 MHz (right). Dashed green lines show the ideal result without the effect of crosstalk and blue dotted lines show the measurement results.

6.6.3. Pulse shaping

The purity of the generated signal can be quantified using the output signal spectrum shown in Chapter 5. The SNR is 48 dB when integrating over 25 MHz bandwidth. Along with the low quantization noise and frequency noise, the output signal quality is predicted to achieve a single-qubit gate fidelity of 99.99%, assuming ideal qubits [93]. However, all these specifications correspond to the addressed qubits. To prevent the unaddressed qubits from being affected, the SFDR should be higher than 44 dB [93].

For a continuous wave tone, the generated signal has an SFDR of 46 dB at 13.54 GHz in a 1 GHz bandwidth, excluding the residual LO leakage. However, a microwave pulse applied to an addressed qubit would have leakage onto the adjacent unaddressed qubit frequency band depending on the pulse shape. As shown in Fig. 6.17, a Gaussian pulse has lower leakage compared to a rectangular pulse[1]. This can help in a tighter packing of qubits in an FDMA scheme allowing for higher power efficiency.

The amplitude and phase modulation capabilities of the controller allow the chip to generate arbitrary waveforms to precisely shape the spectral content of the pulse used to manipulate the qubits. The advantage of pulse shaping can be illustrated by applying a π pulse of two different shapes and sweeping its frequency around the qubit resonance frequency. Fig. 6.17 shows the response of Q_2 to a microwave burst with rectangular versus Gaussian envelope, both calibrated to invert the qubit state when the drive is on-resonance with the qubit. Frequency of a π-pulse swept over a span of 3 MHz with a step size of 15 kHz. It can be observed that only off-resonance rectangular pulse causes unintended qubit rotation.

6.6.4. Characterizing the unintended Z-rotation

As shown in Fig. 6.16, pulse shaping can only correct for X/Y errors. The Z-error due to AC stark shift should be compensated by applying a phase offset to the NCO, which keeps track of the phase evolution of the qubit. This Z-error can be quantified by

[1]Note that, in this measurement, the noise floor of the Gaussian pulse is limited by the instrument noise floor as mentioned in Chapter 5.

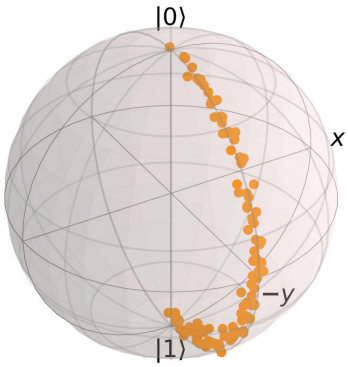


Figure 6.19: Quantum state tomography of an X^2 gate.

applying an off-resonance pulse (a frequency offset with respect to the actual qubit resonance frequency) and observing the unintended Z-rotation on the qubit. Since the qubit is most sensitive to Z-rotation at the equator of a Bloch sphere, a $\pi/2$ pulse is applied after initializing the qubit to $|0\rangle$. Next, an off-resonance rectangular pulse is applied, followed by the Z-phase shift swept from $0°$ to $360°$. Finally, a $\pi/2$ pulse is applied before measurement or projecting the qubit state to Z-axis. This is similar to the Ramsey style experiment with the addition of an off-resonance pulse. This additional pulse creates a Z-error thereby shifting the center of the expected cosine curve outcome of a Ramsey-style experiment. As it can be observed from the figure Fig. 6.18, the closer the off-resonance pulse frequency, the larger the amount of phase shift at the center. This can be used to compensate for the unintended rotation of adjacent qubit when using FDMA for multi-qubit control.

6.6.5. Quantum-State Tomography

The trajectory of an X^2 gate can be reconstructed by performing quantum-state tomography (QST) [144] at incremental burst times of a rectangular microwave signal, as shown in Fig. 6.19. In the QST experiment, the qubit state is measured by projecting it onto the $(-\hat{z}, +\hat{x}, -\hat{y}, +\hat{z})$ axes. The projection on the $-\hat{z}$ axis is measured by direct readout of the spin state, while the projections on other axes are measured by applying a X, Y, or X^2 gate, which are calibrated by the AllXY experiment, before the readout with each measurement repeated 1,000 times. To visualize the qubit state in the Bloch sphere, the readout errors were removed from the data. Since error removal can lead to unphysical states such as data points outside the Bloch sphere, a maximum likelihood estimation is implemented to find the closest physical state of the qubit [144].

The ideal quantum state for each burst time can be predicted using the Rabi frequency fitted from experimental data. The quantum state fidelities at each burst time can be calculated and an average state fidelity of 97.92% is obtained. Here the infidelity comes from the error during the operation as well as the residual state preparation and measurement (SPAM) error after imperfect readout error removal.

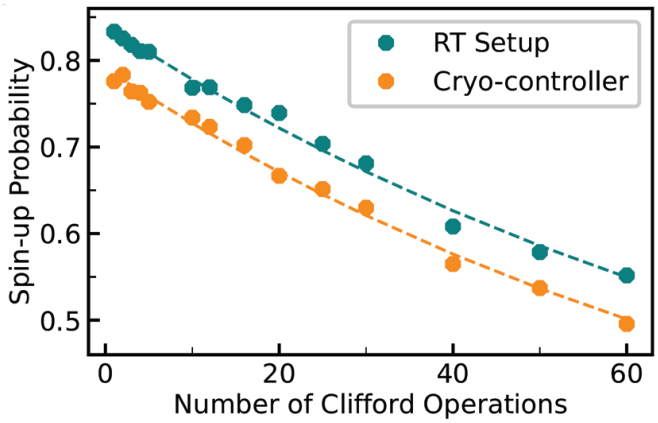


Figure 6.20: Randomized Benchmarking.

6.6.6. Randomized Benchmarking

Although QST allows us to characterize an experimental implementation of a unitary operation, due to the substantial number of experiments involved and the residual SPAM error, a better experiment for characterizing the gate fidelity is needed i.e. Randomized Benchmarking (RB). RB can estimate the single-qubit gate fidelity influenced by all error sources during the course of a quantum operation, i.e. decoherence, imperfect pulse shapes and other unknown error sources [145, 146]. In the RB experiment, sequences of increasing numbers of randomly selected Clifford operations (N) are applied to the qubit (Q_2), followed by a final Clifford operation that returns the qubit to its initial state in the ideal case. For each sequence length N, an average is done over M different randomized sequences. The resulting probability (P) is fitted with an exponential decay:

$$P = A\alpha^N + B \tag{6.3}$$

where A and B capture the state preparation and measurement error which are assumed to be constant in each experiment, while α captures the control fidelity.

A single-qubit RB is executed to compare the performance of the cryo-controller with the conventional room temperature (RT) setup, which consists of an arbitrary waveform generator (Tektronix 5014C) and a vector signal generator (Keysight E8267D). A programmable microwave switch placed at the $3\,\mathrm{K}$ plate allows to conveniently alternate between the cryo-controller and the RT setup. For each data point in Fig. 6.20, 32 different sequences are randomly sampled and each is repeated 200 times. Each Clifford operation is decomposed into gates from the set I, X, Y, X^2, Y^2. Envelopes of all gates to be used are uploaded to the envelope memory, and saved as instructions. The random sequences are constructed by updating the instruction list. The instructions in the list are executed sequentially after an external trigger via the SPI is received. The same random sequences are used in an RB experiment using the RT setup. We find an average single-qubit gate fidelity of $99.71 \pm 0.03\%$ with the RT setup and $99.69 \pm 0.02\%$ with the cryo-controller. The fidelities are consistently

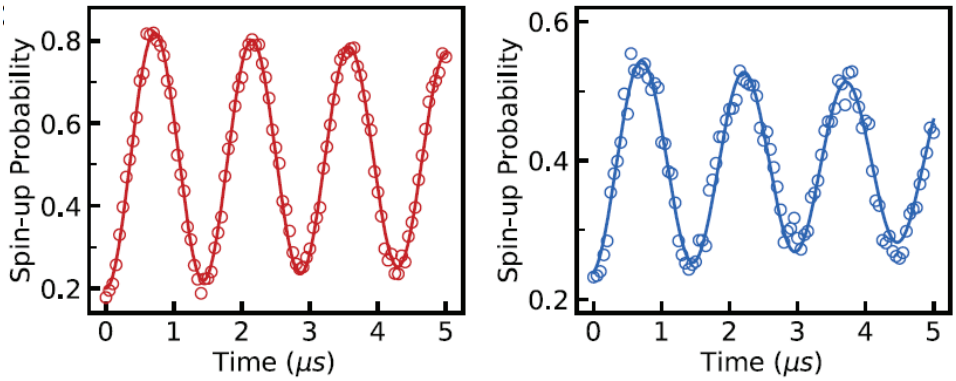


Figure 6.21: Simultaneous Rabi of Q2 (left) and Q1 (right).

identical within the error bars[2] and well above the threshold for fault-tolerance [76], with the infidelity limited by the qubit. These experiments demonstrate the high signal quality from the cryo-controller as well as its capability to generate complex sequences.

6.6.7. Simultaneous Rabi

Figure 6.21 shows the simultaneous execution of Rabi oscillation on two qubits using a single FDMA output generated by the combination of two NCO outputs, one from each bank of the cryo-controller. In this experiment, we attribute the visible decays in both curves to the residual exchange coupling between the two qubits. Although it seems like a decay, it represents the initial part of a beating pattern observed during simultaneous Rabi oscillations recorded (in this case using the RT setup) over larger numbers of oscillations [147]. These patterns are well reproduced by numerical models of the spin evolution in the presence of a finite residual exchange coupling (similar to transmons in [147]). Such an effect is absent in the individually driven Rabi oscillation.

6.7. Two-qubit experiments

Two-qubit gates in spin qubits can be implemented either using Controlled Phase (CZ) [71] or Controlled Rotation (CROT) [16] as a basis. For CZ, a two-qubit gate is realized using electrical pulses that control the exchange coupling between the qubits. In a Controlled Rotation (CROT) gate, the resonance frequency of the target qubit depends on the state of the control qubit, mediated by the exchange interaction between the quantum dots, which is controlled by the barrier gate. In this work, we have used controlled rotation (CROT) gate as the native two-qubit gate.

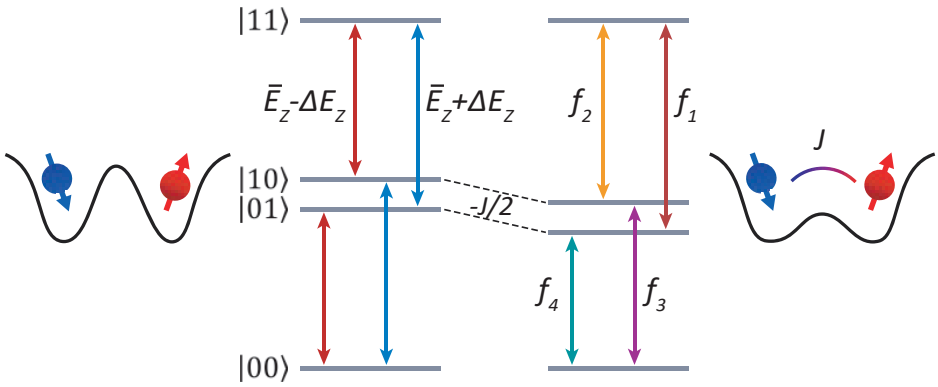


Figure 6.22: Splitting of two individual resonance frequencies into four resonance frequencies by enabling exchange interaction between two qubits.

6.7.1. Gate definition in coupled regime

The two-qubit interaction is mediated by the exchange coupling (J) between the two spins [148], controlled by T-gate. When J = 0, the resonant frequencies of the two qubits are defined as $f_{Q1,Q2} = \bar{E_Z} \pm \Delta E_Z$ shown as the red and blue lines of energy splitting in Fig. 6.22, where $\bar{E_Z}$ represents the mean Zeeman energy of the two dots and ΔE_Z represents the difference in Zeeman energy between the dots. When exchange interaction is enabled, its effect here is to shift the anti-parallel spin states ($|01\rangle$ and $|10\rangle$) down in energy [149], thus splitting each resonant frequency into two defined as [150]:

$$f_1 = \bar{E_Z} + \sqrt{J^2 + \Delta E_Z^2}/2 + J/2 \quad (6.4)$$

$$f_2 = \bar{E_Z} - \sqrt{J^2 + \Delta E_Z^2}/2 + J/2 \quad (6.5)$$

$$f_3 = \bar{E_Z} + \sqrt{J^2 + \Delta E_Z^2}/2 - J/2 \quad (6.6)$$

$$f_4 = \bar{E_Z} - \sqrt{J^2 + \Delta E_Z^2}/2 - J/2 \quad (6.7)$$

As a result, the resonance frequency of each qubit now depends on the state of the other qubit, allowing conditional operations on each qubit via narrow-band microwave bursts [151, 152]. The corresponding four different frequencies can be individually addressed using frequency multiplexing. Both qubits are read out in single-shot mode, as elaborated in Section 6.4.3. Compared to a CPHASE gate, CROT does not require pulsing the exchange coupling (J), reducing the requirements on

[2]determined by the accuracy of microwave pulse calibration

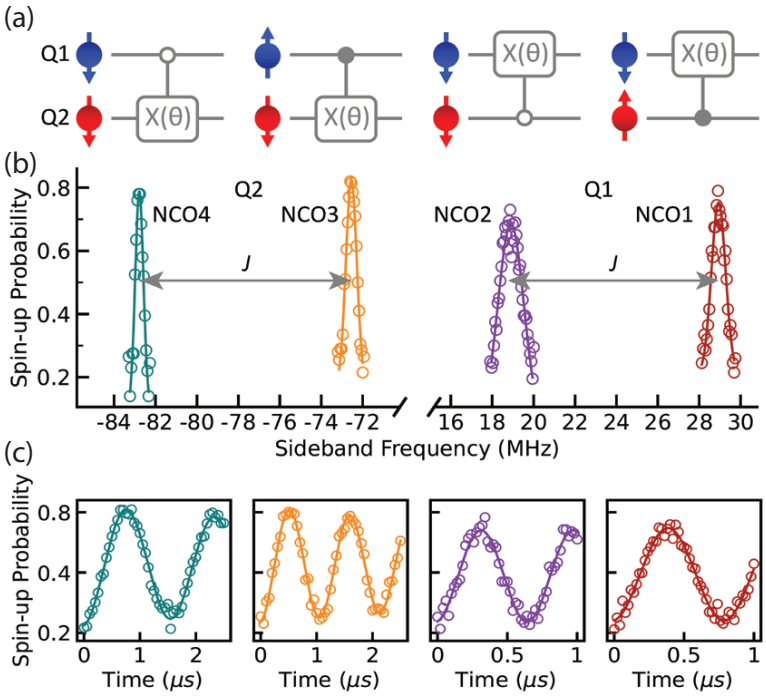


Figure 6.23: (a) Two-qubit gates based on controlled-rotation. From left to right: Z-CROT on Q2, CROT on Q2, Z-CROT on Q1, CROT on Q1. (b) The spectra of two qubits obtained using the cryo-controller with the exchange coupling (J) between the qubits turned on. Selective excitation of each of the four resonances can be used for implementing various two-qubit controlled-rotation gates shown in (a). (c) Rabi oscillations (shared Y-axis labels) at each frequency.

quantum dot control at the cost of lower gate speed due to the execution of two-qubit gates with microwave pulses.

Taking advantage of the frequency shift of each qubit conditional on the state of the other qubit, we use controlled-rotation ($CROT$) gates as the native two-qubit gates. These are achieved by frequency selective addressing [151, 152], thus demanding 2 phase-synchronized NCOs per qubit. Phase-synchronization between the NCOs is achieved by simultaneously enabling the start-up of NCOs, using a digitally-controlled programmable register. Fig. 6.23 shows the two-qubit gate definitions where the Z-CROT is equivalent to CROT gate with the additional flip on the control qubit. To execute, for example, a Z-CROT with Q2 as the control qubit and Q1 as the data qubit, a microwave pulse corresponding to its resonance frequency (purple) and gate duration (obtained from its Rabi oscillation) corresponding to rotation angle (θ) is applied. A π-rotation at the higher or lower frequency implements the canonical controlled-NOT ($CNOT$) gate or the zero-controlled-NOT ($Z\text{-}CNOT$) gate respectively. However, along with CNOT gate on data qubit, CROT based gates cause single-qubit rotation on the control qubit by $\pi/2$ around $\hat{z}$-axis. Moreover, due to cross-talk coming from off-resonance driving, an additional phase correction in the form of a $\hat{z}$-rotation

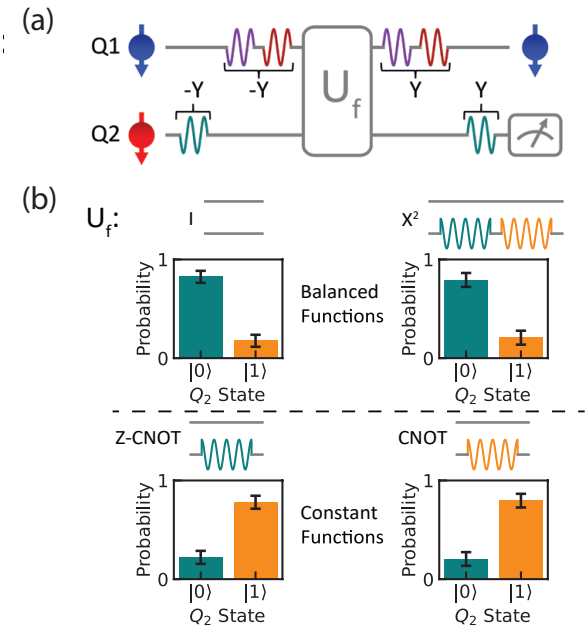


Figure 6.24: (a) Pulse sequences of the Deutsch–Josza algorithm programmed into the cryo-controller. (b) Measured probabilities of the output qubit state (Q2) after running the algorithm.

is needed to cancel out such effects. All $\hat{z}$ rotations are implemented by updating the reference phase of the NCO.

In the two-qubit coupled regime, single-qubit gates are implemented by addressing both frequencies of the same qubit sequentially i.e. the application of microwave pulses corresponding to the green and yellow resonance frequencies and Rabi oscillations in order to apply a single qubit gate on Q2. This would ensure that a single-qubit gate is executed on Q2 independent of the state of Q1. Note that, the decay in the controlled-rotation Rabi oscillations is largely attributed to charge noise. With the exchange coupling turned on, as needed for two-qubit gates, the energy levels are much more sensitive to charge noise.

6.7.2. Deutsch-Jozsa Algorithm

We program the cryo-controller to run the two-qubit Deutsch–Josza algorithm, which determines whether a function (U_f) is constant or balanced in a single evaluation [153]. In this experiment, we use four NCOs to selectively excite the four resonances corresponding to various two-qubit controlled-rotation gates shown in Fig. 6.23. Fig. 6.24 (a) shows the pulse sequences of the Deutsch–Josza algorithm programmed into the cryo-controller. Here, we choose Q_1 to be the output qubit and Q_2 to be the input qubit. Before the function (U_f) is applied, the qubits are brought to superposition states by applying $-Y$ gate on Q_1 and Q_2. Note that, a single pulse (corresponding to the lower frequency green branch of Q_2 i.e. $Z\text{-}CROT$) is used for the $-Y$ and Y gate on Q_2, whereas two pulses are used for Q_1. As explained in the previous section,

this is because Q_1 has a known state at these instances i.e. Q1 ideally starts from and ends up in $|0\rangle$. The two constant (balanced) functions that map one input bit on one output bit are implemented by the $CNOT$ and Z-$CNOT$ (I and X^2) operations as shown in Fig. 6.24 (b). Note that, all functions execute gates around the $\hat{x}$-axis.

A constant function is composed of either a $CNOT$ or a Z-$CNOT$ gate, which consists of a $CROT$ gate on Q_2 and a phase correction on Q_1 (not plotted). Fig. 6.24 (b) shows measured probabilities of the output qubit state (Q_2) after running the algorithm. The constant (balanced) functions lead to a high probability of 78% - 80% (79% - 82%) for measuring the data qubit as $|1\rangle$ ($|0\rangle$), as expected. Error bars indicate standard deviations of the measured probability data. The visibility of Q_2 is normalized by removing the readout error. Empirically, we attribute the remaining errors mostly to charge noise in the presence of a finite J. This experiment highlights the ability to program the cryo-controller with arbitrary sequences of operations.

6.8. Conclusion

The cryo-controller introduces the concept of integrated instruction set non-existent in the prior art and allows for much more complex sequences, containing up to 2048 instructions for each of the four transmitters. Each instruction defines a microwave burst at one of 32 independent frequencies with an amplitude and phase profile that can be arbitrarily shaped. The cryo-controller can be conveniently embedded in existing micro-architectures and programmed via standard QASM variants [154]. This quantum-classical architecture can thus be directly applied to multi-qubit algorithms and noisy intermediate-scale quantum devices [155].

The versatile programmability combined with the signal quality allowing up to 99.99% gate fidelities, the footprint of just $4\,\mathrm{mm}^2$, the power consumption of $384\,\mathrm{mW}$, the ability to integrate multiple transmitters on one die, and operation at $3\,\mathrm{K}$, highlight the promise of cryo-controllers to address key challenges in building a large-scale quantum computer. As discussed in Chapter 5, the power consumption of the controller can be drastically reduced down to $\sim 50\,\mathrm{mW}$ as proved in the future generation of the controller [131].

7

Conclusion

Current implementations of solid-state quantum computers employ rack-mount electronics to generate the qubit control signals at room temperature, which are routed via RF lines to individual qubits operating at dilution refrigerator temperatures. Even if a large-scale quantum processor would be available today, a practical quantum computer could not be built, because the currently adopted room-temperature control approach would be unfeasible. In our vision, this bottleneck can be overcome when the qubits and control are integrated on the same die or package.

This thesis addresses one of the biggest practical obstacles to scaling up solid-state quantum computers. Prior art showed universal quantum logic on two spin qubits operating above $1\,\mathrm{K}$ using room temperature instrumentation[16]. Here we show high-fidelity universal spin qubit control driven by a cryogenic microwave control chip implemented using Intel 22-nm FinFET technology and operating at a few Kelvin. Together, these results pave the way to an integrated scalable quantum computer on a single cryo-CMOS chip.

7.1. Thesis outcome

The objective of achieving a fully integrated quantum computer by integrating the control electronics with the qubit devices led to the definition of five research questions(RQ). These were outlined in Chapter 1 and addressed in the various chapters of this thesis. In the following paragraphs, answers to these research questions are formulated based on the reported findings.

RQ1: Modeling device behavior at cryogenic temperatures

How does existing devices in CMOS technology designed to operate in the military temperature range i.e. $-55\,^{\circ}\mathrm{C}$ *to* $100\,^{\circ}\mathrm{C}$ *behave at cryogenic temperatures i.e. at* $4.2\,\mathrm{K}$*?*

To address this question, microwave passive components in TSMC40 process were characterized at $4.2\,\mathrm{K}$. The changes in device behavior compared to room temper-

ature data were modeled by modifying frequency-independent lumped model parameters accordingly. Furthermore, the parameters of the back-end-of-line metal stack provided by the foundry were modified to capture the cryogenic effects during electromagnetic simulation. These models were validated using a composite structure containing the modeled components. Furthermore, circuit design parameters were derived from prior-art active device characterization results to complement the passive device models in analyzing the benefits and challenges of operating radio frequency integrated circuits at cryogenic temperatures.

RQ2: Predicting cryogenic circuit performance

How do circuits behave based on the cryogenic device characteristics? How essential is a cryogenic model to predict performance?

In the third chapter, the cryogenic models developed in Chapter 2 were used to predict the behavior of an oscillator operating at 4.2 K. It was observed that cryogenic device models can modestly predict the circuit performance. However, due to the lack of compact models for active devices that could be used for Cadence® simulations, the prediction accuracy is limited. It was concluded that cryogenic models are essential for low-power integrated circuit design which is a necessary condition to operate circuit inside dilution refrigeration with limited cooling power.

RQ3: Qubit controller specifications

What are the signal specifications necessary to achieve high-fidelity qubit control? What would be a scalable architecture to design a cryogenic multi-qubit controller?

The operation of spin qubits was thoroughly analyzed and modeled using qubit Hamiltonian in Chapter 3. A Matlab® based model of the controller was developed to be co-simulated with qubit Hamiltonian. Based on the required qubit control signals, several architectures were compared to develop the final controller architecture. Detailed system-level specifications were derived for a power-efficient controller to achieve a 99.99 % control fidelity.

RQ4: Controller implementation

What are the challenges in the practical realization of a scalable cryogenic multi-qubit controller?

The proposed system specifications in Chapter 3 were used to develop a scalable qubit control circuit and implemented in Intel 22-nm FinFET technology. Preliminary device models were used for the realization of a digitally intensive cryogenic microwave signal generator. Custom-made PCBs, low drop-out voltage regulators, power splitter and cryogenic compatible instrumentation enabled the characterization of this device inside a dilution refrigerator. The circuits were thoroughly characterized at 3 K to verify that it complies with the required system specifications and ready to be used for controlling qubits.

RQ5: Final validation with qubits

How does the controller performance compare to the existing experimental setups?

In Chapter 6 it was demonstrated that the single-qubit gate fidelities using the control chip match the high-fidelities obtained using bulky and expensive room temperature microwave vector sources and arbitrary waveform generators. Furthermore, a variety of demanding qubit calibration experiments were implemented to showcase the use of shaped envelopes of the microwave bursts, and achieve the landmark feat of a quantum algorithm fully controlled by cryogenic electronics. With this, the thesis addressed the complete cycle of a design idea to validation following the path: Device characterization and modeling **–>** Validation of models using cryogenic circuit **–>** System architecture and specifications of a qubit controller **–>** Design and cryogenic characterization of a qubit controller **–>** Extensive experimentation with qubits to prove the effectiveness of the controller.

7.2. Outlook

The research on cryogenic CMOS-based qubit controllers is being pursued by several research groups and various large-scale qubit architectures with integrated control electronics have been proposed [24, 22]. Here we present some challenges and suggestions for improvement to realize the vision of co-integration of the cryogenic controller and large-scale qubit arrays on the same chip or package.

O1: Cryogenic characterization and modeling

As demonstrated in Chapter 5, the internal chip temperature of the controller can be significantly higher than the plate temperature of the dilution refrigerator. Hence, accurate modeling of devices integrated in circuit simulators would enable building power-efficient cryogenic circuits which is critical for co-integration of qubits and controller on a single platform. Integration of new materials optimized for cryogenic temperatures such as NbTiN in the back-end-of-line stack can open several opportunities such as integration of superconducting matching networks and building oscillator tanks with high quality factor in CMOS technology. To address the mismatch in form factor between the qubits and controller, multiplexing chips operating at milliKelvin temperatures have been explored [133]. Hence, modeling efforts of the devices should be extended further down to such temperatures to leverage the opportunities or tackle the challenges presented due to operation close to absolute zero.

O2: Oscillator

To further reduce the wiring bottleneck from room temperature to cryogenic electronics, the frequency synthesizer should be integrated on the controller chip. To control a multiqubit array with a wide range of operating frequencies, it is essential to have a low-power wide tuning range oscillator. Moreover, off-chip I/Q hybrids used in Chapter 5 limits the co-integration of the oscillator with the cryogenic controller and hence, quadrature modulation should be implemented in the oscillator. As mentioned in Chapter 5, the contribution of out-of-band noise is more critical towards the frequency noise and hence oscillator topologies with low flicker noise upconversion should be explored.

O3: System-level modelling

The coupling from the electrode to the qubit in EDSR can drastically vary between samples as observed during the experiment and it is difficult to model these inconsistencies in fabrication. Since the qubit fabrication is at the research stage sufficient margin should be accommodated in signal specifications due to inconsistency in quantum dot fabrication in an academic setting until highly reproducible industrial devices are developed. Crosstalk effects between the gate electrodes and quantum dots in the qubit device that manifests while addressing multiple qubits simultaneously can be included in larger qubit array models.

O4: Cryogenic controller improvements

The integration of tunable band pass filters and digital filters on the controller can enable flexibility in frequency planning during the research stage of the qubits where the resonance frequency can vary dramatically. The currently used discrete fixed-frequency BPF could be replaced by a SAW filter on the PCB or by an on-chip higher-order reconstruction filter and/or by a passive filter at the mixer output, when the frequency of qubits is fixed to a certain range. Optimized design of cryogenic CMOS circuits, e.g. the use of a narrower frequency band, can substantially reduce the power consumption and make it possible to work at $1\,\mathrm{K}$ or even lower temperatures. Integration of other functionalities into the cryogenic chip such as readout, biasing, fast pulsing, etc. can further reduce the wiring bottleneck from the room temperature into the refrigerator.

O5: Qubit interface improvements

Since any continuous large-signal tone can affect the electron temperature, high signal isolation is necessary from the controller to the qubit chip, during the off state of the controller. Although LO feedthrough can be avoided from hitting the qubit by proper frequency planning in FDMA, it is important to have in-built LO modulation to completely switch of the LO signal from feeding to the output during other operating modes such as initialization and readout. Spectral purity is of the essence and hence it is important to track and mitigate the origin of all the tones in the spectra. Since the fabrication technology used for spin qubits and commercial CMOS devices differ significantly, advanced cryogenic packaging techniques can enable high-density heterogeneous integration.

Epilogue

Several experimental demonstrations using the cryogenic controller highlight the feasibility of our ultimate vision for a large-scale qubit architecture. The proposed cryogenic controller chip (Horse Ridge) already supports the control of up to 128 qubits, while providing control fidelities limited by the qubits and not the control electronics. Simple replication of this chip allows for the control of thousands of qubits, without excessive heating of the refrigerator. Furthermore, FinFET quantum dots have been developed that are fully compatible with CMOS processing [156, 157] and increased operating temperatures ($\sim 1\,\mathrm{K}$) of spin qubits show only a modest reduction in coherence times [17, 16]. These advances further materialize the possibility to fully

integrate the quantum processor with the classical controller on-chip or by flip-chip technology, lifting a major roadblock in scaling.

Bibliography

[1] D. Deutsch. "Quantum theory, the Church–Turing principle and the universal quantum computer". In: *Proceedings of the Royal Society of London. A. Mathematical and Physical Sciences* 400.1818 (1985), pp. 97–117.

[2] M. A. Nielsen and I. L. Chuang. "Quantum computation and quantum information: 10th". In: *New York, NY, USA: Cambridge University Press* 1107002176 (2011), p. 9781107002173.

[3] A. Kandala, A. Mezzacapo, K. Temme, M. Takita, M. Brink, J. M. Chow, and J. M. Gambetta. "Hardware-efficient variational quantum eigensolver for small molecules and quantum magnets". In: *Nature* 549.7671 (2017), p. 242.

[4] M. Reiher, N. Wiebe, K. M. Svore, D. Wecker, and M. Troyer. "Elucidating reaction mechanisms on quantum computers". In: *Proceedings of the National Academy of Sciences* 114.29 (2017), pp. 7555–7560.

[5] F. Arute, K. Arya, R. Babbush, D. Bacon, J. C. Bardin, R. Barends, R. Biswas, S. Boixo, F. G. Brandao, D. A. Buell, et al. "Quantum supremacy using a programmable superconducting processor". In: *Nature* 574.7779 (2019), pp. 505–510.

[6] C. Monroe, D. Meekhof, B. King, W. M. Itano, and D. J. Wineland. "Demonstration of a fundamental quantum logic gate". In: *Physical review letters* 75.25 (1995), p. 4714.

[7] I. L. Chuang, N. Gershenfeld, M. G. Kubinec, and D. W. Leung. "Bulk quantum computation with nuclear magnetic resonance: theory and experiment". In: *Proceedings of the Royal Society of London. Series A: Mathematical, Physical and Engineering Sciences* 454.1969 (1998), pp. 447–467.

[8] Y. Nakamura, Y. A. Pashkin, and J. S. Tsai. "Coherent control of macroscopic quantum states in a single-Cooper-pair box". In: *nature* 398.6730 (1999), pp. 786–788.

[9] D. Loss and D. P. DiVincenzo. "Quantum computation with quantum dots". In: *Physical Review A* 57.1 (1998), p. 120.

[10] N. Hendrickx, D. Franke, A. Sammak, G. Scappucci, and M. Veldhorst. "Fast two-qubit logic with holes in germanium". In: *Nature* 577.7791 (2020), pp. 487–491.

[11] C. Simmons, M. Thalakulam, N. Shaji, L. J. Klein, H. Qin, R. Blick, D. Savage, M. Lagally, S. Coppersmith, and M. Eriksson. "Single-electron quantum dot in Si/ Si Ge with integrated charge sensing". In: *Applied Physics Letters* 91.21 (2007), p. 213103.

[12] M. Veldhorst, J. C. C. Hwang, C. H. Yang, A. W. Leenstra, B. de Ronde, J. P. Dehollain, J. T. Muhonen, F. E. Hudson, K. M. Itoh, A. Morello, and A. S. Dzurak. "An addressable quantum dot qubit with fault-tolerant control-fidelity". In: *Nature Nanotechnology* 9 (Oct. 2014), p. 981.

[13] J. Elzerman, R. Hanson, L. W. Van Beveren, B. Witkamp, L. Vandersypen, and L. P. Kouwenhoven. "Single-shot read-out of an individual electron spin in a quantum dot". In: *nature* 430.6998 (2004), pp. 431–435.

[14] F. H. Koppens, C. Buizert, K.-J. Tielrooij, I. T. Vink, K. C. Nowack, T. Meunier, L. Kouwenhoven, and L. Vandersypen. "Driven coherent oscillations of a single electron spin in a quantum dot". In: *Nature* 442.7104 (2006), pp. 766–771.

[15] L. C. Camenzind, S. Geyer, A. Fuhrer, R. J. Warburton, D. M. Zumbühl, and A. V. Kuhlmann. "A spin qubit in a fin field-effect transistor". In: *arXiv preprint arXiv:2103.07369* (2021).

[16] L. Petit, H. Eenink, M. Russ, W. Lawrie, N. Hendrickx, S. Philips, J. Clarke, L. Vandersypen, and M. Veldhorst. "Universal quantum logic in hot silicon qubits". In: *Nature* 580.7803 (2020), pp. 355–359.

[17] C. H. Yang, R. Leon, J. Hwang, A. Saraiva, T. Tanttu, W. Huang, J. C. Lemyre, K. W. Chan, K. Tan, F. E. Hudson, et al. "Operation of a silicon quantum processor unit cell above one kelvin". In: *Nature* 580.7803 (2020), pp. 350–354.

[18] H. H. Goldstine and A. Goldstine. "The Electronic Numerical Integrator and Computer (ENIAC)". In: *Mathematical Tables and Other Aids to Computation* 2.15 (1946), pp. 97–110.

[19] W. Shockley, M. Sparks, and G. K. Teal. "p- n Junction Transistors". In: *Physical Review* 83.1 (1951), p. 151.

[20] J. S. Kilby. "Invention of the Integrated Circuit". In: *IEEE Transactions on electron devices* 23.7 (1976), pp. 648–654.

[21] C. A. Ryan, B. R. Johnson, D. Ristè, B. Donovan, and T. A. Ohki. "Hardware for dynamic quantum computing". In: *Review of Scientific Instruments* 88.10 (2017), p. 104703.

[22] L. Vandersypen, H. Bluhm, J. Clarke, A. Dzurak, R. Ishihara, A. Morello, D. Reilly, L. Schreiber, and M. Veldhorst. "Interfacing spin qubits in quantum dots and donors —- hot, dense, and coherent". In: *npj Quantum Information* 3.1 (2017), p. 34.

[23] H. Homulle, S. Visser, B. Patra, G. Ferrari, E. Prati, F. Sebastiano, and E. Charbon. "A reconfigurable cryogenic platform for the classical control of quantum processors". In: *Review of Scientific Instruments* 88.4 (2017), p. 045103.

[24] D. J. Reilly. "Engineering the quantum-classical interface of solid-state qubits". In: *npj Quantum Information* 1 (2015), p. 15011.

[25] E. Charbon, F. Sebastiano, A. Vladimirescu, H. Homulle, S. Visser, L. Song, and R. M. Incandela. "Cryo-CMOS for quantum computing". In: *2016 IEEE International Electron Devices Meeting (IEDM)*. IEEE. 2016, pp. 13–5.

[26] E. Charbon, F. Sebastiano, M. Babaie, A. Vladimirescu, M. Shahmohammadi, R. B. Staszewski, H. A. Homulle, B. Patra, J. P. Van Dijk, R. M. Incandela, et al. "15.5 Cryo-CMOS circuits and systems for scalable quantum computing". In: *2017 IEEE International Solid-State Circuits Conference (ISSCC)*. Ieee. 2017, pp. 264–265.

[27] B. Patra, R. M. Incandela, J. P. Van Dijk, H. A. Homulle, L. Song, M. Shahmohammadi, R. B. Staszewski, A. Vladimirescu, M. Babaie, F. Sebastiano, et al. "Cryo-CMOS circuits and systems for quantum computing applications". In: *IEEE Journal of Solid-State Circuits* 53.1 (2018), pp. 309–321.

[28] B. Patra, M. Mehrpoo, A. Ruffino, F. Sebastiano, E. Charbon, and M. Babaie. "Characterization and analysis of on-chip microwave passive components at cryogenic temperatures". In: *IEEE Journal of the Electron Devices Society* 8 (2020), pp. 448–456.

[29] J. C. Bardin, E. Jeffrey, E. Lucero, T. Huang, O. Naaman, R. Barends, T. White, M. Giustina, D. Sank, P. Roushan, K. Arya, B. Chiaro, J. Kelly, J. Chen, B. Burkett, Y. Chen, A. Dunsworth, A. Fowler, B. Foxen, C. Gidney, R. Graff, P. Klimov, J. Mutus, M. McEwen, A. Megrant, M. Neeley, C. Neill, C. Quintana, A. Vainsencher, H. Neven, and J. Martinis. "A 28nm Bulk-CMOS 4-to-8GHz <2mW Cryogenic Pulse Modulator for Scalable Quantum Computing". In: *2019 IEEE International Solid- State Circuits Conference - (ISSCC)*. Feb. 2019, pp. 456–458.

[30] M. Mehrpoo, B. Patra, J. Gong, J. van Dijk, H. Homulle, G. Kiene, A. Vladimirescu, F. Sebastiano, E. Charbon, M. Babaie, et al. "Benefits and Challenges of Designing Cryogenic CMOS RF Circuits for Quantum Computers". In: *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE. 2019, pp. 1–5.

[31] R. M. Incandela, L. Song, H. Homulle, E. Charbon, A. Vladimirescu, and F. Sebastiano. "Characterization and Compact Modeling of Nanometer CMOS Transistors at Deep-Cryogenic Temperatures". In: *IEEE Journal of the Electron Devices Society* 6 (Apr. 2018), pp. 996–1006.

[32] A. Beckers, F. Jazaeri, A. Ruffino, C. Bruschini, A. Baschirotto, and C. Enz. "Cryogenic characterization of 28 nm bulk CMOS technology for quantum computing". In: *2017 47th European Solid-State Device Research Conference (ESSDERC)*. Sept. 2017, pp. 62–65.

[33] A. Siligaris, G. Pailloncy, S. Delcourt, R. Valentin, S. Lepilliet, F. Danneville, D. Gloria, and G. Dambrine. "High-Frequency and Noise Performances of 65-nm MOSFET at Liquid Nitrogen Temperature". In: *IEEE Transactions on Electron Devices* 53.8 (Aug. 2006), pp. 1902–1908.

[34] N. C. Dao, A. E. Kass, C. T. Jin, and P. H. W. Leong. "Impact of Series Resistance on Bulk CMOS Current Matching Over the 5-300 K Temperature Range". In: *IEEE Electron Device Letters* 38.7 (July 2017), pp. 847–850.

[35] P. A. 't Hart, J. P. G. van Dijk, M. Babaie, E. Charbon, A. Vladimircscu, and F. Sebastiano. "Characterization and Model Validation of Mismatch in Nanometer CMOS at Cryogenic Temperatures". In: *2018 48th European Solid-State Device Research Conference (ESSDERC)*. Sept. 2018, pp. 246–249.

[36] P. Galy, J. C. Lemyre, P. Lemieux, F. Arnaud, D. Drouin, and M. Pioro-Ladrière. "Cryogenic temperature characterization of a 28-nm FD-SOI dedicated structure for advanced CMOS and quantum technologies co-integration". In: *IEEE Journal of the Electron Devices Society* 6 (2018), pp. 594–600.

[37] A. Beckers, F. Jazaeri, H. Bohuslavskyi, L. Hutin, S. De Franceschi, and C. Enz. "Characterization and modeling of 28-nm FDSOI CMOS technology down to cryogenic temperatures". In: *Solid-State Electronics* 159 (2019), pp. 106–115.

[38] A. H. Coskun and J. C. Bardin. "Cryogenic small-signal and noise performance of 32nm SOI CMOS". In: *2014 IEEE MTT-S International Microwave Symposium (IMS2014)*. June 2014, pp. 1–4.

[39] F. Balestra and G. Ghibaudo. "Brief review of the MOS device physics for low temperature electronics". In: *Solid-state electronics* 37.12 (1994), pp. 1967–1975.

[40] R. M. Incandela, L. Song, H. Homulle, E. Charbon, A. Vladimirescu, and F. Sebastiano. "Characterization and compact modeling of nanometer CMOS transistors at deep-cryogenic temperatures". In: *IEEE Journal of the Electron Devices Society* 6 (2018), pp. 996–1006.

[41] J. Craninckx, A. Potočnik, B. Parvais, A. Grill, S. Narasimhamoorthy, S. Van Winckel, S. Brebels, M. Mongillo, R. Li, B. Govoreanu, et al. "CMOS Cryo-Electronics for Quantum Computing". In: *2020 IEEE International Electron Devices Meeting (IEDM)*. IEEE. 2020, pp. 25–1.

[42] H. Homulle, S. Visser, B. Patra, and E. Charbon. "Design techniques for a stable operation of cryogenic field-programmable gate arrays". In: *Review of Scientific Instruments* 89.1 (2018), p. 014703.

[43] F. Teyssandier and D. Prêle. "Commercially Available Capacitors at Cryogenic Temperatures". In: *Ninth International Workshop on Low Temperature Electronics - WOLTE9*. Guaruja, Brazil, June 2010.

[44] M. Gong, U. Alakusu, S. Bonen, M. Dadash, L. Lucci, H. Jia, L. Gutierrez, W. Chen, D. Daughton, G. Adam, et al. "Design considerations for spin readout amplifiers in monolithically integrated semiconductor quantum processors". In: *2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*. 2019, pp. 111–114.

[45] D. S. Russell. "Technology Advances for Radio Astronomy". PhD thesis. California Institute of Technology, 2013.

[46] M. Asheghi, K. Kurabayashi, R. Kasnavi, and K. E. Goodson. "Thermal conduction in doped single-crystal silicon films". In: *Journal of Applied Physics* 91.8 (2002), pp. 5079–5088.

[47] P. Duthil. “Material Properties at Low Temperature”. In: (Jan. 2015), 77–95. 18 p.

[48] E. P. Vandamme, D. M. M. .-. Schreurs, and G. V. Dinther. “Improved three-step de-embedding method to accurately account for the influence of pad parasitics in silicon on-wafer RF test-structures”. In: *IEEE Transactions on Electron Devices* 48.4 (Apr. 2001), pp. 737–742.

[49] D. F. Williams, F.-J. Schmückle, R. Doerner, G. N. Phung, U. Arz, and W. Heinrich. “Crosstalk corrections for coplanar-waveguide scattering-parameter calibrations”. In: *IEEE transactions on microwave theory and techniques* 62.8 (2014), pp. 1748–1761.

[50] K. Lee, S. Mohammadi, P. K. Bhattacharya, and L. P. B. Katehi. “Compact Models Based on Transmission-Line Concept for Integrated Capacitors and Inductors”. In: *IEEE Transactions on Microwave Theory and Techniques* 54.12 (Dec. 2006), pp. 4141–4148.

[51] F.-W. Tsai, K.-C. Wang, K.-C. Lin, C.-L. Lin, and S.-M. Jeng. “Extreme low-K dielectric film scheme for advanced interconnects”. 7626245 (Hsin-Chu, TW). Dec. 2009.

[52] P. Riess and P. Baumgartner. “Temperature Dependent Dielectric Absorption of MIM Capacitors: RF Characterization and Modeling”. In: *2006 European Solid-State Device Research Conference*. Sept. 2006, pp. 459–462.

[53] V. F. Tseng and H. Xie. “Increased Multilayer Fabrication and RF Characterization of a High-Density Stacked MIM Capacitor Based on Selective Etching”. In: *IEEE Transactions on Electron Devices* 61.7 (July 2014), pp. 2302–2308.

[54] H. Samavati, A. Hajimiri, A. R. Shahani, G. N. Nasserbakht, and T. H. Lee. “Fractal capacitors”. In: *IEEE Journal of Solid-State Circuits* 33.12 (Dec. 1998), pp. 2035–2041.

[55] R. Romano, F. Mubarak, M. Spirito, and L. Galatro. “The HΓ-VNA, an Interferometric Approach for the Accurate Measurement of Extreme Impedances”. In: *2019 93rd ARFTG Microwave Measurement Conference (ARFTG)*. IEEE. 2019, pp. 1–6.

[56] Y. Cao, R. A. Groves, X. Huang, N. D. Zamdmer, J. .-. Plouchart, R. A. Wachnik, T.-J. King, and C. Hu. “Frequency-independent equivalent-circuit model for on-chip spiral inductors”. In: *IEEE Journal of Solid-State Circuits* 38.3 (Mar. 2003), pp. 419–426.

[57] C. P. Yue and S. S. Wong. “Physical modeling of spiral inductors on silicon”. In: *IEEE Transactions on Electron Devices* 47.3 (Mar. 2000), pp. 560–568.

[58] S. H. Hall and H. L. Heck. *Advanced signal integrity for high-speed digital designs*. John Wiley & Sons, 2011.

[59] H. Homulle. “Cryogenic electronics for the read-out of quantum processors”. PhD thesis. Delft University of Technology, 2019.

[60] D. Eggert, P. Huebler, A. Huerrich, H. Kueck, W. Budde, and M. Vorwerk. "A SOI-RF-CMOS technology on high resistivity SIMOX substrates for microwave applications to 5 GHz". In: *IEEE Transactions on Electron Devices* 44.11 (Nov. 1997), pp. 1981–1989.

[61] R. A. Johnson, C. E. Chang, P. M. Asbeck, M. E. Wood, G. A. Garcia, and I. Lagnado. "Comparison of microwave inductors fabricated on silicon-on-sapphire and bulk silicon". In: *IEEE Microwave and Guided Wave Letters* 6.9 (Sept. 1996), pp. 323–325.

[62] C. Detcheverry, W. van Noort, R. Hoofman, L. Tiemeijer, V. H. Nguyen, G. Verheyden, P. Bancken, R. Daamen, and R. Havens. "The effect of copper design rules on inductor performance". In: *ESSDERC '03. 33rd Conference on European Solid-State Device Research, 2003.* Sept. 2003, pp. 107–110.

[63] P. A. T Hart, M. Babaie, E. Charbon, A. Vladimirescu, and F. Sebastiano. "Subthreshold Mismatch in Nanometer CMOS at Cryogenic Temperatures". In: *IEEE Journal of the Electron Devices Society* 8 (2020), pp. 797–806.

[64] M. Babaie and R. B. Staszewski. "A class-f cmos oscillator". In: *IEEE Journal of Solid-State Circuits* 48.12 (2013), pp. 3120–3133.

[65] M. Vigilante and P. Reynaert. "A Wideband Class-AB Power Amplifier With 29–57-GHz AM–PM Compensation in 0.9-V 28-nm Bulk CMOS". In: *IEEE Journal of Solid-State Circuits* 53.5 (May 2018), pp. 1288–1301.

[66] M. Vigilante and P. Reynaert. "On the Design of Wideband Transformer-Based Fourth Order Matching Networks for E-Band Receivers in 28-nm CMOS". In: *IEEE Journal of Solid-State Circuits* 52.8 (Aug. 2017), pp. 2071–2082.

[67] A. Ruffino, Y. Peng, F. Sebastiano, M. Babaie, and E. Charbon. "A 6.5-GHz Cryogenic All-Pass Filter Circulator in 40-nm CMOS for Quantum Computing Applications". In: *2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*. June 2019, pp. 107–110.

[68] M. Mehrpoo, F. Sebastiano, E. Charbon, and M. Babaie. "A Cryogenic CMOS Parametric Amplifier". In: *IEEE Solid-State Circuits Letters* 3.1 (2019), pp. 5–8.

[69] S. Asaad, C. Dickel, N. K. Langford, S. Poletto, A. Bruno, M. A. Rol, D. Deurloo, and L. DiCarlo. "Independent, extensible control of same-frequency superconducting qubits by selective broadcasting". In: *Npj Quantum Information* 2 (Aug. 2016). Article, 16029 EP.

[70] J. M. Chow, J. M. Gambetta, E. Magesan, D. W. Abraham, A. W. Cross, B. R. Johnson, N. A. Masluk, C. A. Ryan, J. A. Smolin, S. J. Srinivasan, and M. Steffen. "Implementing a strand of a scalable fault-tolerant quantum computing fabric". In: *Nature communications* 5 (2014).

[71] M. Veldhorst, C. Yang, J. Hwang, W. Huang, J. Dehollain, J. Muhonen, S. Simmons, A. Laucht, F. Hudson, K. M. Itoh, et al. "A two-qubit logic gate in silicon". In: *Nature* 526.7573 (2015), pp. 410–414.

[72] A. Takamizawa, S. Yanagimachi, T. Tanabe, K. Hagimoto, I. Hirano, K.-i. Watabe, T. Ikegami, and J. G. Hartnett. "Atomic fountain clock with very high frequency stability employing a pulse-tube-cryocooled sapphire oscillator". In: *IEEE transactions on ultrasonics, ferroelectrics, and frequency control* 61.9 (2014), pp. 1463–1469.

[73] G. Gualco, J. Anders, A. Sienkiewicz, S. Alberti, L. Forró, and G. Boero. "Cryogenic single-chip electron spin resonance detector". In: *Journal of Magnetic Resonance* 247 (2014), pp. 96–103.

[74] R. Hanson, L. P. Kouwenhoven, J. R. Petta, S. Tarucha, and L. M. Vandersypen. "Spins in few-electron quantum dots". In: *Reviews of Modern Physics* 79.4 (2007), p. 1217.

[75] E. Kawakami, T. Jullien, P. Scarlino, D. R. Ward, D. E. Savage, M. G. Lagally, V. V. Dobrovitski, M. Friesen, S. N. Coppersmith, M. A. Eriksson, et al. "Gate fidelity and coherence time of an electron spin in a Si/SiGe quantum dot". In: *APS Meeting Abstracts*. 2016.

[76] A. G. Fowler, M. Mariantoni, J. M. Martinis, and A. N. Cleland. "Surface codes: Towards practical large-scale quantum computation". In: *Physical Review A* 86.3 (2012), p. 032324.

[77] M. Veldhorst, J. C. C. Hwang, C. H. Yang, A. W. Leenstra, B. De Ronde, J. P. Dehollain, J. T. Muhonen, F. E. Hudson, K. M. Itoh, A. Morello, and A. S. Dzurak. "An addressable quantum dot qubit with fault-tolerant control-fidelity". In: *Nature nanotechnology* 9.12 (2014), pp. 981–985.

[78] T. J. Green, J. Sastrawan, H. Uys, and M. J. Biercuk. "Arbitrary quantum control of qubits in the presence of universal noise". In: *New Journal of Physics* 15.9 (2013), p. 095004.

[79] W. D. Oliver, H. Ball, and M. J. Biercuk. *Upper-bounds on qubit coherence set by master clock instabilities*. Tech. rep. MIT Lincoln Laboratory Lexington United States, 2016.

[80] F. W. Kuo, S. B. Ferreira, H. N. R. Chen, L. C. Cho, C. P. Jou, F. L. Hsueh, I. Madadi, M. Tohidian, M. Shahmohammadi, M. Babaie, and R. B. Staszewski. "A Bluetooth Low-Energy Transceiver With 3.7-mW All-Digital Transmitter, 2.75-mW High-IF Discrete-Time Receiver, and TX/RX Switchable On-Chip Matching Network". In: *IEEE Journal of Solid-State Circuits* 52.4 (Apr. 2017), pp. 1144–1162.

[81] X. Gao, E. A. M. Klumperink, M. Bohsali, and B. Nauta. "A Low Noise Sub-Sampling PLL in Which Divider Noise is Eliminated and PD/CP Noise is Not Multiplied by N^2". In: *IEEE Journal of Solid-State Circuits* 44.12 (Dic. 2009), pp. 3253–3263.

[82] M. Shahmohammadi, M. Babaie, and R. B. Staszewski. "A 1/f noise upconversion reduction technique applied to Class-D and Class-F oscillators". In: *2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*. Feb. 2015, pp. 1–3.

[83] D. Murphy, H. Darabi, and H. Wu. "A VCO with implicit common-mode resonance". In: *2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*. Feb. 2015, pp. 1–3.

[84] M. Shahmohammadi, M. Babaie, and R. B. Staszewski. "A 1/f Noise Upconversion Reduction Technique for Voltage-Biased RF CMOS Oscillators". In: *IEEE Journal of Solid-State Circuits* 51.11 (Nov. 2016), pp. 2610–2624.

[85] H. Homulle, S. Visser, B. Patra, and E. Charbon. "Design techniques for a stable operation of cryogenic field-programmable gate arrays". In: *Review of Scientific Instruments* 89.1 (2018), p. 014703.

[86] H. Homulle, S. Visser, B. Patra, G. Ferrari, E. Prati, F. Sebastiano, and E. Charbon. "A reconfigurable cryogenic platform for the classical control of quantum processors". In: *Review of Scientific Instruments* 88.4 (2017), p. 045103.

[87] M. Babaie and R. B. Staszewski. "An Ultra-Low Phase Noise Class-F_2 CMOS Oscillator With 191 dBc/Hz FoM and Long-Term Reliability". In: *IEEE Journal of Solid-State Circuits* 50.3 (Mar. 2015), pp. 679–692.

[88] M. Mehrpoo, B. Patra, J. Gong, J. van Dijk, H. Homulle, G. Kiene, A. Vladimirescu, F. Sebastiano, E. Charbon, and M. Babaie. "Benefits and challenges of designing cryogenic CMOS RF circuits for quantum computers". In: *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE. 2019, pp. 1–5.

[89] T. H. Lee and A. Hajimiri. "Oscillator phase noise: a tutorial". In: *IEEE Journal of Solid-State Circuits* 35.3 (Mar. 2000), pp. 326–336.

[90] L. Le Guevel, G. Billiot, X. Jehl, S. De Franceschi, M. Zurita, Y. Thonnart, M. Vinet, M. Sanquer, R. Maurand, A. G. Jansen, et al. "19.2 A 110mK 295μW 28nm FDSOI CMOS Quantum Integrated Circuit with a 2.8 GHz Excitation and nA Current Sensing of an On-Chip Double Quantum Dot". In: *2020 IEEE International Solid-State Circuits Conference-(ISSCC)*. IEEE. 2020, pp. 306–308.

[91] J. Gong, Y. Chen, F. Sebastiano, E. Charbon, and M. Babaie. "19.3 a 200dB FoM 4-to-5GHz cryogenic oscillator with an automatic common-mode resonance calibration for quantum computing applications". In: *2020 IEEE International Solid-State Circuits Conference-(ISSCC)*. IEEE. 2020, pp. 308–310.

[92] J. Gong, E. Charbon, F. Sebastiano, and M. Babaie. "A 2.7mW 45fsrms-Jitter Cryogenic Dynamic-Amplifier-Based PLL for Quantum Computing Applications". In: *2021 IEEE Custom Integrated Circuits Conference (CICC)*. 2021, pp. 1–2.

[93] J. P. van Dijk, B. Patra, S. Pellerano, E. Charbon, F. Sebastiano, and M. Babaie. "Designing a DDS-based SoC for high-fidelity multi-qubit control". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 67.12 (2020), pp. 5380–5393.

[94] T. F. Watson, S. G. J. Philips, E. Kawakami, D. R. Ward, P. Scarlino, M. Veldhorst, D. E. Savage, M. G. Lagally, M. Friesen, S. N. Coppersmith, M. A. Eriksson, and L. M. K. Vandersypen. "A programmable two-qubit quantum processor in silicon". In: *Nature* 555 (Feb. 2018), p. 633.

[95] A. Morello, J. J. Pla, F. A. Zwanenburg, K. W. Chan, K. Y. Tan, H. Huebl, M. Möttönen, C. D. Nugroho, C. Yang, J. A. van Donkelaar, et al. "Single-shot readout of an electron spin in silicon". In: *Nature* 467.7316 (2010), pp. 687–691.

[96] E. Kawakami. "Characterization of an electron spin qubit in a Si/SiGe quantum dot". PhD thesis. TU Delft, 2016.

[97] M. Steffen, L. M. K. Vandersypen, and I. L. Chuang. "Simultaneous Soft Pulses Applied at Nearby Frequencies". In: *Journal of Magnetic Resonance* 146.2 (2000), pp. 369–374.

[98] T. F. Watson, S. G. J. Philips, E. Kawakami, D. R. Ward, P. Scarlino, M. Veldhorst, D. E. Savage, M. G. Lagally, M. Friesen, S. N. Coppersmith, M. A. Eriksson, and L. M. K. Vandersypen. "A programmable two-qubit quantum processor in silicon". In: *Nature* (Feb. 2018), EP–.

[99] J. Yoneda, K. Takeda, T. Otsuka, T. Nakajima, M. R. Delbecq, G. Allison, T. Honda, T. Kodera, S. Oda, Y. Hoshi, et al. "A quantum-dot spin qubit with coherence limited by charge noise and fidelity higher than 99.9%". In: *Nature nanotechnology* 13.2 (2018), p. 102.

[100] E. Kawakami, P. Scarlino, D. R. Ward, F. R. Braakman, D. E. Savage, M. G. Lagally, M. Friesen, S. N. Coppersmith, M. A. Eriksson, and L. M. K. Vandersypen. "Electrical control of a long-lived spin qubit in a Si/SiGe quantum dot". In: *Nature Nanotechnology* 9 (Aug. 2014), 666 EP -.

[101] R. Barends, J. Kelly, A. Megrant, A. Veitia, D. Sank, E. Jeffrey, T. C. White, J. Mutus, A. G. Fowler, B. Campbell, et al. "Superconducting quantum circuits at the surface code threshold for fault tolerance". In: *Nature* 508.7497 (2014), pp. 500–503.

[102] J. P. van Dijk, E. Kawakami, R. N. Schouten, M. Veldhorst, L. M. Vandersypen, M. Babaie, E. Charbon, and F. Sebastiano. "Impact of Classical Control Electronics on Qubit Fidelity". In: *Physical Review Applied* 12.4 (2019), p. 044054.

[103] Y. M. Greshishchev, D. Pollex, S. Wang, M. Besson, P. Flemeke, S. Szilagyi, J. Aguirre, C. Falt, N. Ben-Hamida, R. Gibbins, and P. Schvan. "A 56GS/s 6b DAC in 65nm CMOS with 256×6b memory". In: *2011 IEEE International Solid-State Circuits Conference*. Feb. 2011, pp. 194–196.

[104] L. Duncan, B. Dupaix, J. J. McCue, B. Mathieu, M. LaRue, V. J. Patel, M. Teshome, M. Choe, and W. Khalil. "A 10-bit DC-20-GHz Multiple-Return-to-Zero DAC With $>$ 48-dB SFDR". In: *IEEE Journal of Solid-State Circuits* 52.12 (Dec. 2017), pp. 3262–3275.

[105] E. Bechthum, G. I. Radulov, J. Briaire, G. J. G. M. Geelen, and A. H. M. van Roermund. "A Wideband RF Mixing-DAC Achieving IMD $<$ -82 dBc Up to 1.9 GHz". In: *IEEE Journal of Solid-State Circuits* 51.6 (June 2016), pp. 1374–1384.

[106] A. Devices. "A technical tutorial on digital signal synthesis". In: *Application Note* (1999), pp. 1–122.

[107] C. A. Ryan, B. R. Johnson, D. Ristè, B. Donovan, and T. A. Ohki. "Hardware for dynamic quantum computing". In: *Review of Scientific Instruments* 88.10 (2017), p. 104703.

[108] Z. Chen, J. Kelly, C. Quintana, R. Barends, B. Campbell, Y. Chen, B. Chiaro, A. Dunsworth, A. G. Fowler, E. Lucero, E. Jeffrey, A. Megrant, J. Mutus, M. Neeley, C. Neill, P. J. J. O'Malley, P. Roushan, D. Sank, A. Vainsencher, J. Wenner, T. C. White, A. N. Korotkov, and J. M. Martinis. "Measuring and Suppressing Quantum State Leakage in a Superconducting Qubit". In: *Phys. Rev. Lett.* 116 (2 Jan. 2016), p. 020501.

[109] D. C. McKay, C. J. Wood, S. Sheldon, J. M. Chow, and J. M. Gambetta. "Efficient Z gates for quantum computing". In: *Phys. Rev. A* 96 (2 Aug. 2017), p. 022330.

[110] E. A. Vittoz. "Low-power design: ways to approach the limits". In: *Proceedings of IEEE International Solid-State Circuits Conference - ISSCC '94*. Feb. 1994, pp. 14–18.

[111] L. M. K. Vandersypen. "Experimental quantum computation with nuclear spins in liquid helium". PhD thesis. stanford university, 2001.

[112] T. Yoo, H. C. Yeoh, Y. Jung, S. Cho, Y. S. Kim, S. Kang, and K. Baek. "A 2 GHz 130 mW Direct-Digital Frequency Synthesizer With a Nonlinear DAC in 55 nm CMOS". In: *IEEE Journal of Solid-State Circuits* 49.12 (Dec. 2014), pp. 2976–2989.

[113] A. Martinez Alonso, M. Miyahara, and A. Matsuzawa. "A 12.8-ns-Latency DDFS MMIC With Frequency, Phase, and Amplitude Modulations in 65-nm CMOS". In: *IEEE Journal of Solid-State Circuits* 53.10 (Oct. 2018), pp. 2840–2849.

[114] G. G. Shahidi. "Chip Power Scaling in Recent CMOS Technology Nodes". In: *IEEE Access* 7 (2018), pp. 851–856.

[115] B. Patra, J. P. van Dijk, S. Subramanian, A. Corna, X. Xue, C. Jeon, F. Sheikh, E. Juarez-Hernandez, B. P. Esparza, H. Rampurawala, et al. "19.1 A Scalable Cryo-CMOS 2-to-20GHz Digitally Intensive Controller for 4× 32 Frequency Multiplexed Spin Qubits / Transmons in 22nm FinFET Technology for Quantum Computers". In: *2020 IEEE International Solid-State Circuits Conference-(ISSCC)*. IEEE. 2020, pp. 304–306.

[116] J. P. G. Van Dijk, B. Patra, S. Subramanian, X. Xue, N. Samkharadze, A. Corna, C. Jeon, F. Sheikh, E. Juarez-Hernandez, B. P. Esparza, et al. "A Scalable Cryo-CMOS Controller for the Wideband Frequency-Multiplexed Control of Spin Qubits and Transmons". In: *IEEE Journal of Solid-State Circuits* 55.11 (2020), pp. 2930–2946.

[117] C. H. Yang, R. C. C. Leon, J. C. C. Hwang, A. Saraiva, T. Tanttu, W. Huang, J. C. Lemyre, K. W. Chan, K. Y. Tan, F. E. Hudson, K. M. Itoh, A. Morello, M. Pioro-Ladrière, A. Laucht, and A. S. Dzurak. "Operation of a silicon quantum processor unit cell above one kelvin". In: *Nature* 580.7803 (Apr. 2020), pp. 350–354.

[118] R. M. Incandela, L. Song, H. Homulle, E. Charbon, A. Vladimirescu, and F. Sebastiano. "Characterization and Compact Modeling of Nanometer CMOS Transistors at Deep-Cryogenic Temperatures". In: *IEEE Journal of the Electron Devices Society* 6 (2018), pp. 996–1006.

[119] A. Coskun and J. Bardin. "Cryogenic small-signal and noise performance of 32nm SOI CMOS". In: *2014 IEEE MTT-S International Microwave Symposium (IMS2014)*. IEEE. 2014, pp. 1–4.

[120] M. H. Roshan, S. Zaliasl, K. Joo, K. Souri, R. Palwai, W. Chen, S. Pamarti, J. C. Doll, N. Miller, C. Arft, S. Tabatabaei, C. Sechen, A. Partridge, and V. Menon. "Dual-MEMS-resonator temperature-to-digital converter with 40 K resolution and FOM of 0.12pJK2". In: *2016 IEEE International Solid-State Circuits Conference (ISSCC)*. Jan. 2016, pp. 200–201.

[121] B. Razavi. *RF Microelectronics (2Nd Edition) (Prentice Hall Communications Engineering and Emerging Technologies Series)*. 2nd. Upper Saddle River, NJ, USA: Prentice Hall Press, 2011.

[122] B. Razavi. *Design of analog CMOS integrated circuits*. Tata McGraw-Hill Education, 2002.

[123] S.-G. Lee and J.-K. Choi. "Current-reuse bleeding mixer". In: *Electronics letters* 36.8 (2000), pp. 696–697.

[124] M. Vigilante and P. Reynaert. "On the Design of Wideband Transformer-Based Fourth Order Matching Networks for E-Band Receivers in 28-nm CMOS". In: *IEEE Journal of Solid-State Circuits* 52.8 (2017), pp. 2071–2082.

[125] M. Babaie, F.-W. Kuo, H.-N. R. Chen, L.-C. Cho, C.-P. Jou, F.-L. Hsueh, M. Shahmohammadi, and R. B. Staszewski. "A fully integrated Bluetooth low-energy transmitter in 28 nm CMOS with 36% system efficiency at 3 dBm". In: *IEEE Journal of Solid-State Circuits* 51.7 (2016), pp. 1547–1565.

[126] S. C. Blaakmeer, E. A. Klumperink, D. M. Leenaerts, and B. Nauta. "Wideband balun-LNA with simultaneous output balancing, noise-canceling and distortion-canceling". In: *IEEE journal of solid-state circuits* 43.6 (2008), pp. 1341–1350.

[127] B. Sell, B. Bigwood, S. Cha, Z. Chen, P. Dhage, P. Fan, M. Giraud-Carrier, A. Kar, E. Karl, C.-J. Ku, et al. "22FFL: A high performance and ultra low power FinFET technology for mobile and RF applications". In: *2017 IEEE International Electron Devices Meeting (IEDM)*. IEEE. 2017, pp. 29–4.

[128] L. Tavian. *Latest developments in cryogenics at CERN*. Tech. rep. 2005.

[129] H. Darabi. *Radio frequency integrated circuits and systems*. Cambridge University Press, 2015.

[130] J. C. Bardin, E. Jeffrey, E. Lucero, T. Huang, S. Das, D. T. Sank, O. Naaman, A. E. Megrant, R. Barends, T. White, et al. "Design and Characterization of a 28-nm Bulk-CMOS Cryogenic Quantum Controller Dissipating Less Than 2 mW at 3 K". In: *IEEE Journal of Solid-State Circuits* 54.11 (2019), pp. 3043–3060.

[131] J.-S. Park, S. Subramanian, L. Lampert, T. Mladenov, I. Klotchkov, D. J. Kurian, E. Juarez-Hernandez, B. Perez-Esparza, S. R. Kale, K. A. Beevi, et al. "A Fully Integrated Cryo-CMOS SoC for Qubit Control in Quantum Computers Capable of State Manipulation, Readout and High-Speed Gate Pulsing of Spin Qubits in Intel 22nm FFL FinFET Technology". In: *2021 IEEE International Solid-State Circuits Conference (ISSCC)*. Vol. 64. IEEE. 2021, pp. 208–210.

[132] X. Xue, B. Patra, J. P. van Dijk, N. Samkharadze, S. Subramanian, A. Corna, B. P. Wuetz, C. Jeon, F. Sheikh, E. Juarez-Hernandez, et al. "CMOS-based cryogenic control of silicon quantum circuits". In: *Nature* 593.7858 (2021), pp. 205–210.

[133] S. Pauka, K. Das, R. Kalra, A. Moini, Y. Yang, M. Trainer, A. Bousquet, C. Cantaloube, N. Dick, G. Gardner, et al. "A cryogenic CMOS chip for generating control signals for multiple qubits". In: *Nature Electronics* 4.1 (2021), pp. 64–70.

[134] Y. Xu, F. Unseld, A. Corna, A. Zwerver, A. Sammak, D. Brousse, N. Samkharadze, S. Amitonov, M. Veldhorst, G. Scappucci, et al. "On-chip integration of Si/SiGe-based quantum dots and switched-capacitor circuits". In: *Applied Physics Letters* 117.14 (2020), p. 144002.

[135] G. Scappucci. "Semiconductor materials stacks for quantum dot spin qubits". In: *arXiv preprint arXiv:2102.10897* (2021).

[136] V. Srinivasa, K. C. Nowack, M. Shafiei, L. Vandersypen, and J. M. Taylor. "Simultaneous spin-charge relaxation in double quantum dots". In: *Physical review letters* 110.19 (2013), p. 196803.

[137] M. Pioro-Ladrière, T. Obata, Y. Tokura, Y.-S. Shin, T. Kubo, K. Yoshida, T. Taniyama, and S. Tarucha. "Electrically driven single-electron spin resonance in a slanting Zeeman field". In: *Nat. Phys.* 4 (Aug. 2008), p. 776.

[138] E. Kawakami, P. Scarlino, D. R. Ward, F. R. Braakman, D. E. Savage, M. G. Lagally, M. Friesen, S. N. Coppersmith, M. A. Eriksson, and L. M. K. Vandersypen. "Electrical control of a long-lived spin qubit in a Si/SiGe quantum dot". In: *Nature nanotechnology* 9.9 (2014), pp. 666–670.

[139] L. M. K. Vandersypen and I. L. Chuang. "NMR techniques for quantum control and computation". In: *Rev. Mod. Phys.* 76 (4 Jan. 2005), pp. 1037–1069.

[140] X. Xue, B. D'Anjou, T. F. Watson, D. R. Ward, D. E. Savage, M. G. Lagally, M. Friesen, S. N. Coppersmith, M. A. Eriksson, W. A. Coish, et al. "Repetitive quantum nondemolition measurement and soft decoding of a silicon spin qubit". In: *Physical Review X* 10.2 (2020), p. 021006.

[141] T. F. Watson, B. Weber, Y.-L. Hsueh, L. C. Hollenberg, R. Rahman, and M. Y. Simmons. "Atomically engineered electron spin lifetimes of 30 s in silicon". In: *Science advances* 3.3 (2017), e1602811.

[142] M. Reed. *Entanglement and quantum error correction with superconducting qubits*. Lulu. com, 2013.

[143] L. Essen and J. V. Parry. "An atomic standard of frequency and time interval: a caesium resonator". In: *Nature* 176.4476 (1955), pp. 280–282.

[144] J. B. Altepeter, E. R. Jeffrey, and P. G. Kwiat. "Photonic state tomography". In: *Advances in Atomic, Molecular, and Optical Physics* 52 (2005), pp. 105–159.

[145] E. Knill, D. Leibfried, R. Reichle, J. Britton, R. B. Blakestad, J. D. Jost, C. Langer, R. Ozeri, S. Seidelin, and D. J. Wineland. "Randomized benchmarking of quantum gates". In: *Physical Review A* 77.1 (2008), p. 012307.

[146] E. Magesan, J. M. Gambetta, and J. Emerson. "Characterizing quantum gates via randomized benchmarking". In: *Physical Review A* 85.4 (2012), p. 042311.

[147] A. M. Forney, S. R. Jackson, and F. W. Strauch. "Multifrequency control pulses for multilevel superconducting quantum circuits". In: *Physical Review A* 81.1 (2010), p. 012306.

[148] J. R. Petta, A. C. Johnson, J. M. Taylor, E. A. Laird, A. Yacoby, M. D. Lukin, C. M. Marcus, M. P. Hanson, and A. C. Gossard. "Coherent manipulation of coupled electron spins in semiconductor quantum dots". In: *Science* 309.5744 (2005), pp. 2180–2184.

[149] T. Meunier, V. Calado, and L. Vandersypen. "Efficient controlled-phase gate for single-spin qubits in quantum dots". In: *Physical Review B* 83.12 (2011), p. 121403.

[150] M. Russ, D. M. Zajac, A. J. Sigillito, F. Borjans, J. M. Taylor, J. R. Petta, and G. Burkard. "High-fidelity quantum gates in Si/SiGe double quantum dots". In: *Physical Review B* 97.8 (2018), p. 085421.

[151] D. M. Zajac, A. J. Sigillito, M. Russ, F. Borjans, J. M. Taylor, G. Burkard, and J. R. Petta. "Resonantly driven CNOT gate for electron spins". In: *Science* 359.6374 (2017), pp. 439–442.

[152] W. Huang, C. Yang, K. Chan, T. Tanttu, B. Hensen, R. Leon, M. Fogarty, J. Hwang, F. Hudson, K. M. Itoh, A. Morello, A. Laucht, and A. S. Dzurak. "Fidelity benchmarks for two-qubit gates in silicon". In: *Nature* 569.7757 (2019), p. 532.

[153] D. Deutsch and R. Jozsa. "Rapid solution of problems by quantum computation". In: *Proceedings of the Royal Society of London. Series A: Mathematical and Physical Sciences* 439.1907 (1992), pp. 553–558.

[154] K. M. Svore, A. V. Aho, A. W. Cross, I. Chuang, and I. L. Markov. "A layered software architecture for quantum computing design tools". In: *Computer* 39.1 (2006), pp. 74–83.

[155] J. Preskill. "Quantum Computing in the NISQ era and beyond". In: *Quantum* 2 (2018), p. 79.

[156] R. Pillarisetty, N. Thomas, H. George, K. Singh, J. Roberts, L. Lampert, P. Amin, T. Watson, G. Zheng, J. Torres, et al. "Qubit device integration using advanced semiconductor manufacturing process technology". In: *2018 IEEE International Electron Devices Meeting (IEDM)*. IEEE. 2018, pp. 6–3.

[157] A. Zwerver, T. Krähenmann, T. Watson, L. Lampert, H. George, R. Pillarisetty, et al. "Qubits made by advanced semiconductor manufacturing". In: *arXiv preprint arXiv:2101.12650* (2021).

Acknowledgements

During my sophomore year internship at IIT Jodhpur, I got a glimpse into microwave engineering, which introduced me to CMOS devices, smith charts and matching networks. This fueled me with the passion to pursue microelectronics and brought me to TU Delft for my graduate studies. Little did I know of the whole new world waiting for me.

The graduate school course by Prof. Leo Di Carlo and Prof. Edoardo Charbon ignited my interest in quantum computing. Fortunately, microwave engineering is also vital for quantum computers. So this is where I could experience the best of both worlds. I was very impressed by the digital RF course by Dr. Masoud Babaie, which tackled several practical aspects of circuit design for wireless communications. Meanwhile, Prof. Charbon started his research group in cryogenic CMOS electronics. Coincidentally, Dr. Babaie joined the cryo-CMOS endeavor and was the daily supervisor for my MSc thesis. This marked the beginning of a memorable journey and opportunities to work with some of the best professors and scientists during my Ph.D.

Edoardo, thank you for walking me into this new yet fascinating field of cryogenic electronics. Being a part of a group that evolved from just two people to twenty has been a great learning experience. You have been a great promotor and have always given me the best opportunities to present my work around the world. I will cherish our trips to all the conferences and Hillsboro.

Masoud, your remarkable attention to detail has brought the best out of me, time and again. You have pushed me to be better by the day. I have learned amply about radio-frequency circuit design techniques from you.

Fabio, although you are not my official supervisor, I consider you my shadow supervisor. You have been very inspirational during all my conference presentations. You have always prioritized my necessities, enabling me to have a smooth journey in pursuing my research.

Lieven, you have always motivated me to pursue quantum computing since I was a graduate student. It meant a lot. I thank you for successfully facilitating a colossal collaboration project like Horse Ridge.

Stefano, you always bring along a lot of energy and positivity. Your system-level perspective on wireless communications as well as racing cars continues to amaze me. Your appreciation for my achievements has been really uplifting.

I have met some excellent colleagues during my PhD who have influenced me and helped me sail through this journey. Most importantly, Jeroen who was in the same boat as me for three years. We have shouldered each other's responsibilities like brothers in arms. I appreciate our unique collaboration and complementary skills. I fondly remember writing our JSSC paper last year when we had become such experts in divide and conquer.

Xiao, I had the opportunity to spend quite some time with you in the lab during the last year of qubit experiments and writing the paper for Nature. This has been a stimulating experience and I learned a lot from you and Nodar. I wish you all the best for your PhD. Andrea Corna, you have been a great help with the initial cryogenic measurements and dilution refrigerator setup.

Since its inception, I have been fortunate to be a part of a great team, the Coolgroup with Rosario, Harald, Bahador and Jeroen. Rosario you have been a dear friend and confidant. Our laid-back chit-chats back in the good old times are nostalgic. You will certainly nail your Ph.D. Harald, I had great time with you in the lab building our group's first cryogenic experimental setups. Pascal, thanks for organizing all the Coolgroup events. Your office at EEMCS with antique electronics was the perfect example for a grad student. I had fun with you and Job during the graduate school courses. The post-work beers took our minds off the lonely pandemic. Gerd, you have been a good friend and office mate. We bonded during the last year of my Ph.D. and I have enjoyed your German lessons. The campus run with Gerd, Pascal, Augusto and Jeroen will stick with me forever. Milad, it was nice knowing you while measuring with the cryogenic probe station. I appreciated your circuit design insights during the group meetings. Andrea Ruffino, thanks for the collaboration and fun times during your tenure at Delft. Jiang, it was nice working with you during our tape-out together. Bagas, it was a pleasure working with you too. Our intense cryogenic experiments with Guoji, Patrick, Jurgen during the last week before ISSCC deadline was quite eventful. Niels, it was a pleasure supervising you and wish you the best for all your future endeavors. I would also like to thank the past members of the coolgroup Lin Song, Bahador, Lizzy, Pinakin. I hope the best for the next generation coolgroup members Job, Ramon, Bagas, Luc, Rikadur, Niels, Lennart, Aishwariya.

I would like to thank the members of the imaging group Esteban, Augusto, Preethi, Ting, Chao, Chockalingam. Augusto, I appreciate your help in planning my PhD completion. Our trip to China couldn't be more adventurous. Esteban, you goading us to soccer table matches has been dearly missed. Thanks to several friends Priyanka, Satoshi, Gerasimos, Augusto Ximenes, Ernesto, Michel, who saw me through the cultural shock transition in the Netherlands.

I must thank several members at Intel Corporation, including Sushil Subraramanian who helped me to steer through my internship journey at Intel and carry out several responsibilities for a successful tape-out. Thanks to Jim Clarke and Jim Held for supporting our project and appreciating our Horse Ridge work. I also express my heartfelt thanks to the colleagues at Intel Amsterdam, who made us very comfortable during our internship.

Zu Yao and Lukasz, I admire your professionalism during crunch times for wirebonding and PCB assembly. Thanks to Antoon, we always had a flawless server supporting our Cadence designs. I want to thank Atef for teaching me practical aspects of RF wafer probing and Olaf for helping out in handling the Big Whoop dilution refrigerator. I am thankful to our go-to electronics point at TNW, Raymond Schouten and Raymond Vermeulen.

Special thanks to Matt, Nico, Tim, Remco and Siebe for their contributions in building our cryogenic measurement setups. I acknowledge all the secretaries at

EEMCS and TNW, Joyce, Marja, Chantal and Joanna, for attending to our administrative needs with utmost urgency.

Prof. Akhilesh Mohan (IIT Kharagpur), you have been a father figure in introducing me to the world of scientific research. The spark that you ignited in a boy's mind years ago continues to grow ceaselessly.

Last but not least, I would also like to thank my family, who have always supported me behind the curtains. I express the deepest affection for my wife Ankita. You have been an earnest troubleshooter, bringing me back to reality in those overwhelming days. Your groundedness keeps me rooted in our culture, believing that no accomplishment is worth trading my values. Thanks to my sisters (Swarna, Riti and Prabhati) and parents (Niranjan and Sukanti) for believing in my abilities. My parents-in-law (Manoranjan and Sabita) have also been very kind in relating to my struggles and celebrating my achievements.

List of Publications

Journal papers

7. X. Xue*, **B. Patra***, J. Van Dijk*, et al., "CMOS-based cryogenic control of silicon quantum circuits," in *Nature* 593, 205-210 (2021), doi: 10.1038/s41586-021-03469-4.

6. J. Van Dijk*, **B. Patra***, et al., "A Scalable Cryo-CMOS Controller for the Wideband Frequency-Multiplexed Control of Spin Qubits and Transmons," in *IEEE Journal of Solid-State Circuits*, vol. 55, no. 11, pp. 2930-2946, Nov. 2020, doi: 10.1109/JSSC.2020.3024678.

5. J. van Dijk*, **B. Patra***, S. Pellerano, E. Charbon, F. Sebastiano and M. Babaie, "Designing a DDS-Based SoC for High-Fidelity Multi-Qubit Control," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 12, pp. 5380-5393, Dec. 2020, doi: 10.1109/TCSI.2020.3019413.

4. **B. Patra**, M. Mehrpoo, A. Ruffino, F. Sebastiano, E. Charbon and M. Babaie, "Characterization and Analysis of On-Chip Microwave Passive Components at Cryogenic Temperatures," in *IEEE Journal of the Electron Devices Society*, vol. 8, pp. 448-456, 2020, doi: 10.1109/JEDS.2020.2986722.

3. H. Homulle, S. Visser, **B. Patra**, and E. Charbon, "Design techniques for a stable operation of cryogenic field-programmable gate arrays," *Review of Scientific Instruments*, vol. 89, no. 1, 2018, Art. no. 014703, doi: 10.1063/1.5004484.

2. **B. Patra***, R. M. Incandela*, et al., "Cryo-CMOS Circuits and Systems for Quantum Computing Applications," in *IEEE Journal of Solid-State Circuits*, vol. 53, no. 1, pp. 309-321, Jan. 2018, doi: 10.1109/JSSC.2017.2737549.

1. H. Homulle, S. Visser, **B. Patra**, G. Ferrari, E. Prati, F. Sebastiano, E. Charbon, "A reconfigurable cryogenic platform for the classical control of quantum processors," *Review of Scientific Instruments*, vol. 88, no. 4, Apr. 2017, Art. no. 045103, doi: 10.1063/1.4979611.

***equal contribution**

Conference papers

8. J. Gong, **B. Patra**, L. Enthoven, J. Staveren, F. Sebastiano, M. Babaie, "A 0.049 mm2 7.1-to-16.8 GHz Dual-Core Triple-Mode VCO Achieving 200 dB FoMA in 22nm FinFET," accepted for publication in *IEEE International Solid- State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, 2022.

7. B. Prabowo, G. Zheng, M. Mehrpoo, **B. Patra**, P. Collard, J. Dijkema, A. Sammak, G. Scappucci, E. Charbon, F. Sebastiano, L. M. K. Vandersypen, M. Babaie, "A 6 to 8 GHz 0.17 mW/Qubit Cryo-CMOS Receiver for Multiple Spin Qubit Readout in 40 nm CMOS Technology," *IEEE International Solid- State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, 2021, doi: 10.1109/ISSCC42613.2021.9365848

6. F. Sebastiano, J. Van Dijk, P. A. Hart, **B. Patra**, J. V. Staveren, X. Xue, C. Almudever, G. Scappucci, m. Veldhorst, L. Vandersypen, A. Vladimirescu, S. Pellerano, M. Babaie, E. Charbon "Cryo-CMOS Interfaces for Large-Scale Quantum Computers," *IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, 2020, doi: 10.1109/IEDM13553.2020.9372075

5. **B. Patra***, J. P. G. Van Dijk*, et al., "A Scalable Cryo-CMOS 2-to-20GHz Digitally Intensive Controller for 4×32 Frequency Multiplexed Spin Qubits / Transmons in 22nm FinFET Technology for Quantum Computers," *IEEE International Solid-State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, 2020, pp. 304-306, doi: 10.1109/ISSCC19947.2020.9063109.

4. M. Mehrpoo, **B. Patra**, J. Gong, P. A. Hart, J.P.G. van Dijk, H. Homulle, G. Kiene, A. Vladimirescu, F. Sebastiano, E. Charbon, M. Babaie, "Benefits and Challenges of Designing Cryogenic CMOS RF Circuits for Quantum Computers," *IEEE International Symposium on Circuits and Systems (ISCAS)*, Sapporo, Japan, 2019, pp. 1-5, doi: 10.1109/ISCAS.2019.8702452.

3. F Sebastiano, H. Homulle, J. PG van Dijk, R. M. Incandela, **B. Patra**, M. Mehrpoo, M. Babaie, A. Vladimirescu, E. Charbon, "Cryogenic CMOS interfaces for quantum devices," *7th IEEE International Workshop on Advances in Sensors and Interfaces (IWASI)*, Vieste, 2017, pp. 59-62, doi: 10.1109/IWASI.2017.7974215.

2. F. Sebastiano, H. Homulle, **B. Patra**, R. Incandela, J. Dijk, L. Song, M. Babaie, A. Vladimirescu, and E. Charbon. "Cryo-CMOS Electronic Control for Scalable Quantum Computing: Invited". In Proceedings of the *54th Annual Design Automation Conference 2017*(DAC '17). Association for Computing Machinery, New York, NY, USA, Article 13, 1–6. doi: 10.1145/3061639.3072948.

1. E. Charbon, F. Sebastiano, M. Babaie, A. Vladimirescu, M. Shahmohammadi, R. B. Staszewski, H. Homulle, **B. Patra**, J. P. G. Van Dijk, R. M. Incandela, L. Song, B. Valizadehpasha, "Cryo-CMOS circuits and systems for scalable quantum computing," *IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, 2017, pp. 264-265, doi: 10.1109/ISSCC.2017.7870362.

Conference talks (without paper)

3. **B. Patra**, et. al., "CMOS-based cryogenic control of silicon quantum circuits", Bulletin of the American Physical Society, *APS March Meeting 2021*.

2. **B. Patra**, et. al., "A Scalable Multi-Channel Cryogenic Controller for Spin Qubits / Transmons with Frequency Multiplexing Capability Implemented in Intel 22nm

FinFET Technology", Bulletin of the American Physical Society, *APS March Meeting 2020*.

1. **B. Patra**, "Cryogenic Frequency Synthesis for Qubit Control", *International Workshop on Silicon Quantum Electronics*, Hillsboro, USA in August 2017.

Invited forum

1. **B. Patra**, "A Cryogenic CMOS Multiqubit Controller", Forum: Electronics for a Quantum World, *2021 IEEE International Solid-State Circuits Conference (ISSCC)*.

About the author

Bishnu Patra received the MSc degree in Electrical Engineering (Microelectronics) from Delft University of Technology, Delft, The Netherlands, in 2016, where he is currently pursuing the PhD degree, focusing on cryogenic RF Integrated circuits for quantum computing applications. From 2013 to 2014, he was a B.Sc. Researcher with the ELCA Department, Delft University of Technology. During his PhD, he worked as an RF & Mixed Signal IC Design Intern at Intel labs, Hillsboro, OR, USA from 2017 to 2018. His current research interests include RF transmitters for qubit control, CMOS frequency synthesizers, design and modelling of microwave passive components at cryogenic temperatures.

Mr. Patra serves as a reviewer of IEEE Journal of Solid-State Circuits, Transactions on Electron Devices, Transactions on Circuits and Systems and Transactions on Very Large Scale Integration systems. He was a recipient of the IEEE Solid-State Circuits Society Predoctoral Achievement Award (2019-2020) and ISSCC 2020 Jan Van Vessem Award for Outstanding European Paper.

Casimir PhD series 2021-36
ISBN 978-90-8593-501-8