Device Realization, Characterization and Modeling for Linear RF Applications

Koen Buisman

Device Realization, Characterization and Modeling for Linear RF Applications

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*Aan mijn moeder, R. K. Buisman-Zilver (*1948-†2003)*

'Tantae molis erat...'
Publius Vergilius Maro, Aeneis (29-19 BCE)

Contents

Chapter 1

Introduction

Since the early days of electronics, there has been high interest in developing wireless communication systems. This is best illustrated by the experiments of Tesla (1894) [1] and Marconi (1895) [2,3], based on Maxwells theory (1864) [4] and the groundbreaking work of Hertz (1887) [5]. In these early days, communication systems were primitive and implemented through the use of coherers (electro-mechanical detectors) and spark transmitters. It was only with the invention of the vacuum tube [6–8] that more complex transmitters and receivers with a significantly better performance could be developed. Already at that time, the future use of advanced semiconductor devices was predicted (e.g. MOS [9] in 1925 by Lillienfeld), to enable more advanced and compact wireless systems. However, it was not until the invention of the bipolar transistor in 1947 [10,11] and the introduction of silicon planar integration techniques [12, 13] in the early 60's, that these theoretical ideas could be realized.

Enabled by these developments that facilitate increased integration and miniaturization, in the last decade, a tremendous growth in individual communication has taken place. This is driven by the basic desire of people, to communicate anywhere, anytime. It is this desire that resulted in the enormous consumer market for handheld mobile phones of today.

The fact, that the development of the telecommunication standards with their related functionality / performance has been a gradual process, has resulted in many different communication standards. These standards range from the basic voice oriented 'global system for mobile communications' (GSM) established by the 'Conférence européenne des administrations des postes et des télécommunications' (CEPT) in 1982 [14] to the much more complex 'universal mobile telecommunications system' (UMTS) phones, which can also offer high data rate and video services. It is this plurality of communication standards, which need to co-exist with the already present services, like radio and TV broadcast services, that resulted in a very complex distribution of the available frequency spectrum. This situation is even worse because of the varying frequency-band allocation from continent to continent, resulting in a densely populated, complicated spectral distribution of wireless services (Fig. 1.1) that complicates the business of phone manufacturers.

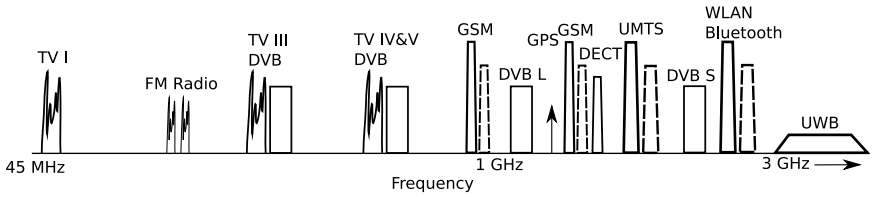


Figure 1.1: Frequency spectrum population relevant to a modern handset.

1.1 Modern wireless communication nodes

Currently various communication standards and other wireless services are offered that are of interest to the mobile phone user. The most important are:

- GSM - voice communication,
- WLAN - short range broadband internet access,
- EDGE, HSDPA, UMTS, LTE - medium range (high speed) data transfer,
- WiMAX - long range broadband internet access,
- Bluetooth - ultra short range personal network,
- FM radio (receive only),
- TV/DVB (receive only),
- GPS - position.

While the original voice oriented modulation schemes, such as GSM, are characterized by low-data rates and a constant envelop signal, modern communication protocols can offer higher data rates while being spectrally efficient, this results in relative high peak-to-average power ratios for their modulated signals. This later property severely taxes the linearity and efficiency requirements of the transmit path as well as the receive path, yielding complications in the development of modern mobile phones. The other, equally important complication is the very high hardware complexity (Fig. 1.2) of a high-end mobile phone that can offer most of the services listed above [15].

As can be noted from Fig. 1.2 the current approach to implement the various communication services is based on a multi-path approach in which each receive / transmit path has been entirely optimized for the communication standard to be handled. As one can note from this approach, many circuit functions (circuit blocks) are repeated multiple times, increasing the total footprint and costs of the mobile phone. With the continuous increase in wireless services the exploding complexity with related drawbacks is currently considered to be the major bottleneck in the development of a new generation low-cost multi-purpose smart phones.

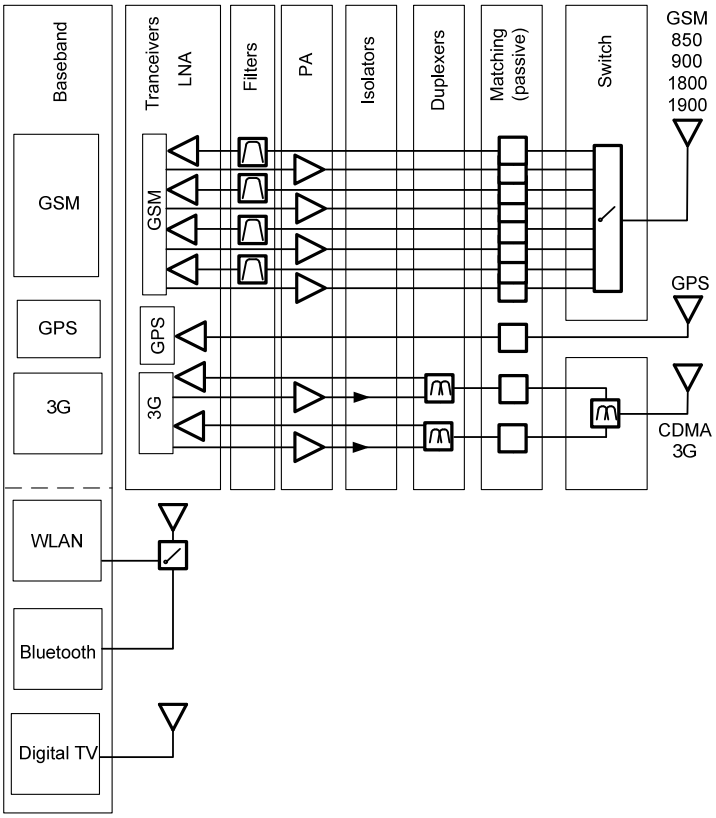


Figure 1.2: Schematic of a modern mobile phone offering many different communication services. The current implementation approach is characterized by using multiple hardware signal paths in parallel to handle the different standards, yielding significant duplications in the hardware configuration. After [16].

1.1.1 The need for radio-frequency adaptivity

From the forgoing discussion it is clear that the availability of adaptive RF (Radio Frequency) frontends would greatly reduce the hardware complexity, yielding the situation of Fig. 1.3(b). To facilitate this, the RF frontend must be able to change operating frequency as well as modulation standard. This requires the realization of tunable filters and matching networks that allow for flexible frequency-band selection and adaptive matching to optimize low noise operation in the receive chain, as well as a transmit chain that is highly efficient at all times (Fig. 1.3). For the implementation of adaptive filters and matching networks, tunable passive components are required, which can change in component value, without degrading the signal quality. This proves to be a complicated task in practice, since varying component values almost automatically results in distortion of the received or transmitted signal. It is

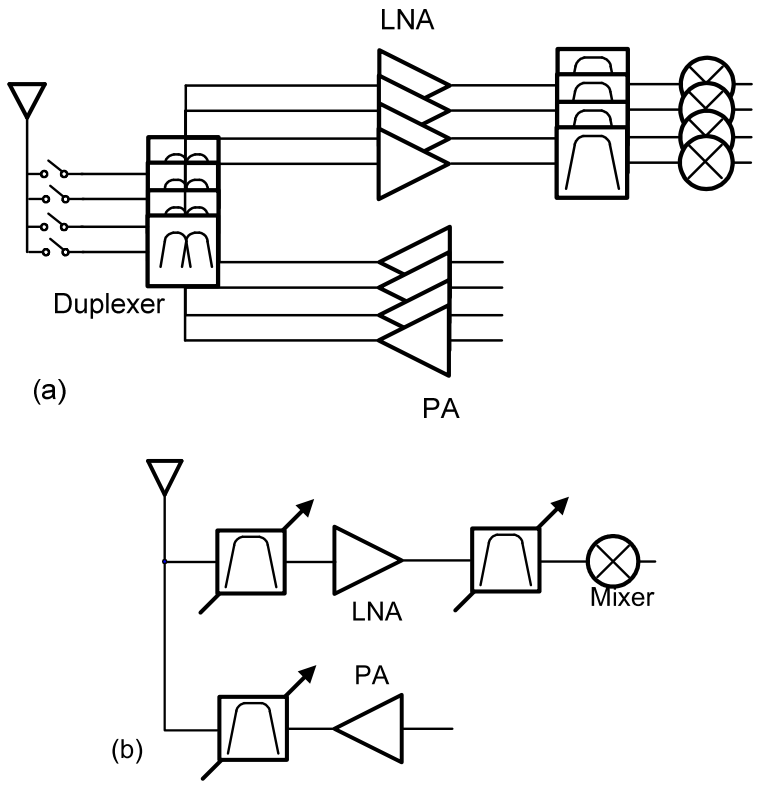


Figure 1.3: (a) Traditional parallel path RF architecture, (b) transceiver concept based on adaptive RF function blocks.

therefore not surprising that currently in industry significant attention is paid to the development of new components that can offer this functionality without introducing significant losses or degradation of the signal quality.

1.2 Linearity requirements in wireless transceivers

To operate correctly, wireless transceivers should be configured in such a way that they are able to receive the desired signals without being troubled by other broadcasted signals. Also transmission should take place without causing any interference to other channels. To fulfill these requirements, historically the super heterodyne concept was used for its high selectivity and relaxed requirements on its functional blocks [17]. However, in view of the desire to integrate as much as possible, currently the direct conversion (homodyne) transceiver tends to be favored since it requires fewer (external) filters for its implementation. A principle schematic of a (single channel) direct conversion wireless transceiver is given in Fig. 1.4. Also note that filters play an important role in achieving the desired frequency selectivity for direct conversion

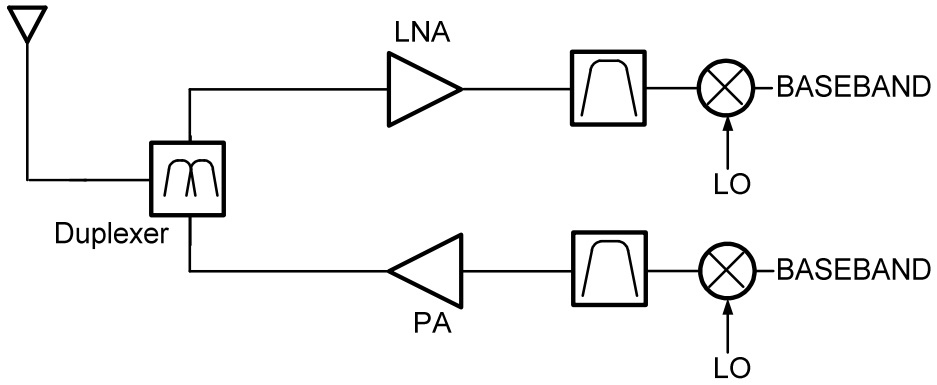


Figure 1.4: Schematic of typical homodyne transceiver front-end.

transceivers. If one aims at handling multiple frequency bands and communication standards with one transceiver line-up, these filters should be made adaptive while not causing any degradation in signal quality. To avoid this degradation the system needs to be linear, which basically means that the signals present in the system cannot mix with each other nor with itself, thus avoiding the creation of interfering distortion products. To support understanding for the reader, the linearity considerations of the RF frontend for the receive path and transmit path are briefly discussed below.

1.2.1 Signal conditions receive path

When considering the receive path of the handset, not only the desired signal will be present at the antenna interface, but also other unwanted signals that can have magnitudes several orders higher than the desired signal to be received. The handset receiver must be able to handle all these signals without causing any interference between them. This requires a high dynamic range of the system. To achieve this, not only the noise figure of the RF frontend needs to be low, guaranteeing good reception of the weak incoming signals, but it must also be linear to handle the signals with higher power levels. This high linearity is required to avoid undesired mixing of the signals present in the receive path, which yields distortion products that can interfere with the desired signals.

1.2.2 Signal conditions transmit path

When transmitting, the handset should only broadcast the desired signal causing neither signal interference to other wireless services nor block its own receiver. To achieve this situation, the transmitted signal must be confined within the bandwidth of the intended transmit channel. This requires a linear behavior of the transmitting chain, since non-linear distortion will give rise to undesired harmonics and intermodulation sidebands that broadens the bandwidth of the transmit signal. While harmonics can be filtered out, the intermodulation products can only be avoided by making the transmit path sufficiently linear. In practical situations, some ‘spectral leakage’ into

the next communication channel cannot be avoided; however this leakage should not exceed the levels given by the so called spectral mask of the communication standard. (See Fig. 1.5 for an 802.11g WiFi communication signal). These spectral masks are defined by governmental regulations and have to be fulfilled by RF equipment manufacturers. The amount of spectral leakage into he next channel is normally expressed as the adjacent channel power ratio (ACPR or ACLR), which is the ratio of the transmitted power in the 'wanted' channel to the spectral leakage into the adjacent channel. Also for the undesired harmonics spectral requirements are defined, which in practice can be satisfied by harmonic terminations in the output stage or filtering.

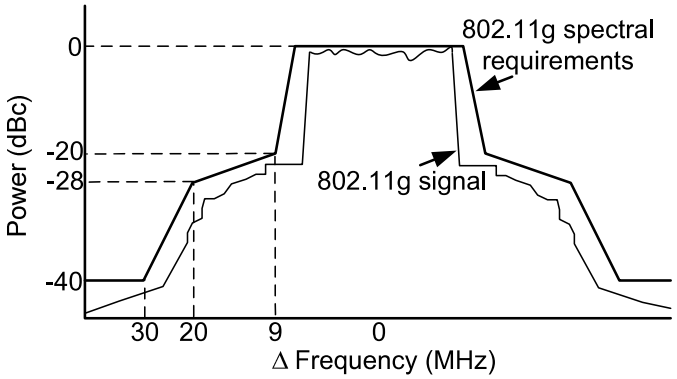


Figure 1.5: Example of a spectral mask of an 802.11g WiFi communication signal. The transmitted signal should not exceed the levels given in the mask.

1.2.3 Needs for future wireless nodes

From the forgoing discussions it has become clear that RF adaptivity and high linearity are currently the key topics in the development of future mobile communication systems, since they can in principle offer:

- Band/mode switching,
- Multi standard operation,
- High efficiency operation,
- Antenna mismatch correction.

It is therefore not surprising that within industry significant attention is given to the development of new (more linear) devices and circuit techniques that address these needs. Not only these new devices and circuit techniques are needed, but also deep understanding of their operation and accurate models for predicting their (non-linear) imperfections. To support this, advanced measurement and modeling techniques are mandatory. Historically however, measurements and models are mainly focused on the small-signal (linear) behavior of electronics devices, while large-signal characterization was mostly focused on single-tone performance to optimize for gain, output power

and efficiency. It is only with the recent high interest in linear (distortion free) circuit operation, that new technologies, circuits, measurement and models are especially developed to also handle these aspects correctly. Although significant progress has been made over the last few years, the close interaction between the device physics of the component(s) under consideration and their peripheral circuitry has complicated understanding and slowed down progress in this area. To support the development of the next generation of wireless applications, this thesis work addresses technology, characterization and modeling solutions that ease and shorten the development of the future generation of mobile phones, those are low cost, compact, battery efficient, and support all thinkable wireless services in a flexible manner.

1.3 Research goals of this thesis

The content of this thesis can be basically divided in two parts. The first part deals with the development of tunable passive low-distortion adaptive components that can facilitate a future generation of adaptive wireless transceivers, while the second part is focused on bipolar devices technologies and models to evaluate their suitability for the implementation of linear transmitters. Since both topics involve linearity considerations, first an introduction of some basic theory, needed to understand and describe non-linear distortion, is given. After this introduction the details of tunable passive devices and bipolar devices are discussed, taking in consideration their related technology, characterization and modeling issues.

1.3.1 Tunable passive devices

To place this work in the proper context first an overview is given of current adaptive devices as present in literature, e.g. Barium Strontium Titanate (BST), Micro-Electro-Mechanical Systems (MEMS) and Silicon-on-Insulator (SOI) switches based adaptive elements, for which their properties are discussed in terms of figure of merit and their implementation advantages and disadvantages. Following this overview the focus is on a within the Delft Institute of Microsystems and Nanoelectronics (DIMES) developed novel varactor technology that, in combination with specific varactor circuit topologies, can offer low loss devices with no, or extremely low distortion properties. These new varactor elements are characterized, modeled and applied in adaptive RF circuit demonstrators, which include tunable filters, phase shifters and matching networks.

1.3.2 Bipolar devices for linear RF applications

The second half of this thesis is focused on suitable techniques to characterize, model and enhance devices for application in power amplifiers for wireless applications. Note, that these transmitting amplifier stages not only have to be efficient, but should also be linear to handle correctly the complex modulated signals as present in modern handsets. Currently, bipolar devices are favored for this task since it is claimed that they can offer better efficiency, linearity and ruggedness than their CMOS counterparts. Also, performance differences are reported between SiGe and III-V devices.

This work is aimed at providing characterization techniques for a clear and objective technology comparison and the modeling tools to cover the essential differences found for the various technology systems. In this work the combination of optimum bias conditions and optimum harmonic loading at the input and output of the active device are investigated. For this purpose a custom active harmonic load-pull measurement system is used. By experimentally investigating the linearity of bipolar devices and pinpointing at the important parts of models that describe the critical phenomena, not only the (dis)advantages of some technologies are highlighted but also the tools and techniques are provided to support the development of future linear transmitters for future 3G/4G/LTE communication applications.

1.3.3 Outline

The flow of the thesis is given in Fig. 1.6.

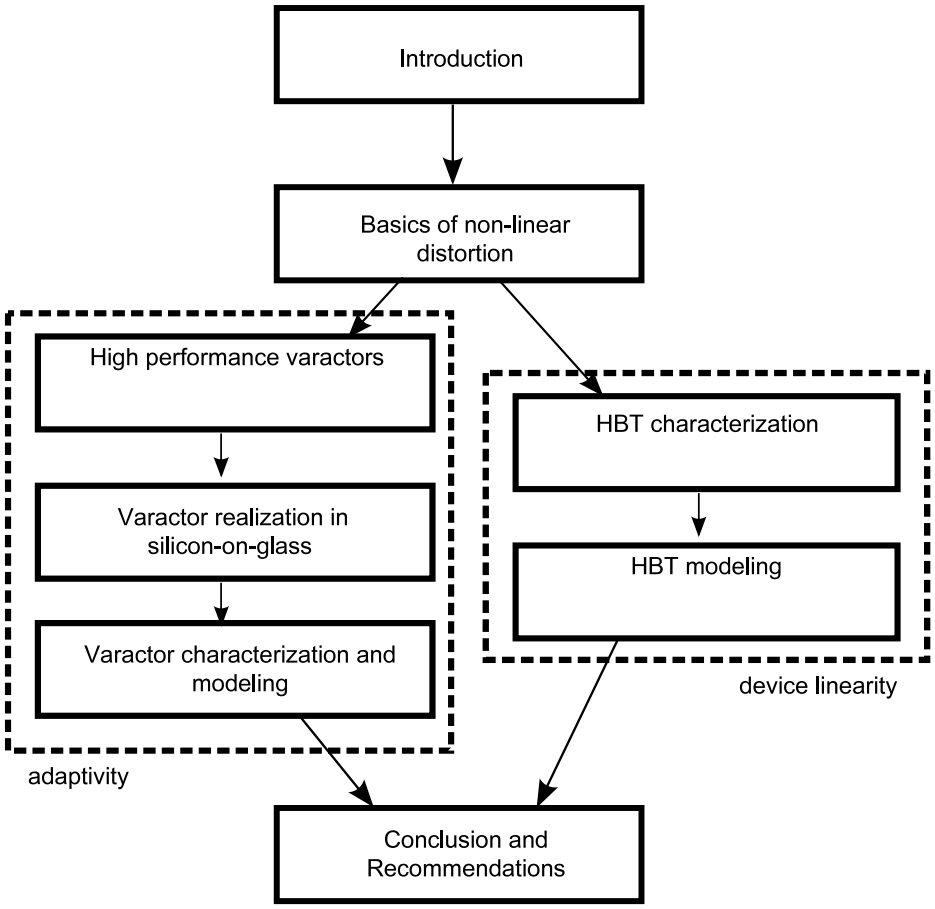


Figure 1.6: Outline of thesis.

Chapter 2

Basics of non-linear distortion

2.1 Introduction

In an ideal linear system the output signal will be a perfectly scaled replica of the input signal, where only its original amplitude and phase might be adjusted. In contrast, when non-linear phenomena are present, signals tend to mix with each other or itself, giving rise to new signal components (distortion products), which can cause channel-to-channel interference or errors in the bit detection of the original signal. Consequently, since distortion can strongly affect the operation of communication systems, its nature and impact on circuit performance must be qualified. For this purpose in literature some basic situations are considered for (multi-tone) sinusoidal signals, which are later used in this thesis to characterize, understand and improve the linearity of semiconductor devices. To support the understanding of the reader, this chapter will briefly discuss the distortion characteristics of single tone excitation, two-tone excitation, three-tone excitation and, finally, wide-band modulated signals. Also, attention will be given to the conventions and notations used in the following chapters.

2.1.1 Single-tone excitation

When a signal $x(t)$ at a frequency f_1 with amplitude A is present at the input of a non-linear analog block, e.g. an amplifier, its output $y(t)$ can be described using a Taylor series expansion,

$$y(t) = a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) + ..., \tag{2.1}$$

where a_n are the Taylor coefficients of the function relation of the transfer function at a given bias point X_0.

$$a_n = \frac{1}{n!} \frac{d^n y(X_0)}{dx^n}. \tag{2.2}$$

If the input signal is sinusoidal ($x(t) = Acos(\omega t)$), the resulting output signal of the non-linear system described by (2.1) can be written as:

$$y(t) = \frac{1}{2}a_2A^2 + \left(a_1A + \frac{3}{4}a_3A^3\right)cos(\omega t) + \frac{1}{2}a_2A^2cos(2\omega t) + \frac{1}{4}a_3A^3cos(3\omega t) + ... \quad (2.3)$$

From this approximation, the following signal components can be identified: a DC shift represented by $\frac{1}{2}a_2A^2$, the desired gain a_1, a factor representing gain compression/expansion $\frac{3}{4}a_3A^3$, the amplitude of the second harmonic $\frac{1}{2}a_2A^2$ and a term representing the magnitude of the third harmonic $\frac{1}{4}a_3A^3$. The harmonic distortion can be expressed as the amplitude of a specific harmonic component divided by the amplitude of the fundamental, so that the second harmonic distortion can be expressed as ($HD2$) is $\frac{1}{2}|\frac{a_2}{a_1}|A$ and the third harmonic distortion ($HD3$) is $\frac{1}{4}|\frac{a_3}{a_1}|A^2$. For the single tone excitation the non-linearity of the circuit function can be characterized by the total harmonic distortion which is expressed as a ratio:

$$THD = \frac{\text{all harmonic power}}{\text{fundamental power}} = \sqrt{HD2^2 + HD3^2 + HD4^2 + ...} \quad (2.4)$$

This figure of merit is mostly in use for systems with a low pass character like audio amplifiers.

2.1.2 Two-tone excitation

When considering band-pass oriented systems, like wireless communication links, linearity determination using single-tone characterization is less applicable. In these situations the use of a two-tone test signal is preferred. In this test the input signal of (2.1) is set to: $x(t) = Acos(\omega_1 t) + Acos(\omega_2 t)$, which represents two sinusoidal signals at frequency ω_1 and ω_2 with equal amplitude. When applying this to a non-linear system characterized up to the third order as described by (2.1), the resulting output signal is:

$$\begin{aligned} y(t) =& a_2A^2 + \left(a_1A + \frac{9}{4}a_3A^3\right)cos(\omega_{1,2}t) + \\ & \frac{1}{2}a_2A^2cos(2\omega_{1,2}t) + \frac{1}{4}a_3A^3cos(3\omega_{1,2}t) + \\ & a_2A^2cos(\omega_2 \pm \omega_1) + \frac{3}{4}a_3A^3cos(2\omega_{1,2} \pm \omega_{2,1}) + ... \end{aligned} \quad (2.5)$$

When considering the resulting output (see also Fig. 2.1) now besides the already previously discussed DC shift and harmonics, also the second order intermodulation products $a_2A^2cos(\omega_2 \pm \omega_1)$ ($IM2$) and third order intermodulation products $\frac{3}{4}a_3A^3cos(2\omega_{1,2} \pm \omega_{2,1})$ ($IM3$) can be identified. These frequency products result from the mixing of the signals at ω_1 and ω_2.

As can be noted from Fig. 2.1, for a bandpass system the $IM3$ distortion products are causing signal interference, since they appear very close to the desired signal components ω_1 and ω_2 and therefore cannot be filtered. The second order frequency products appear in baseband and near the double frequency and are for this reason

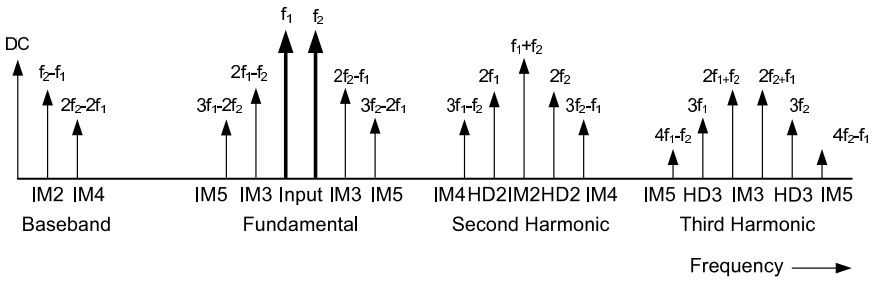


Figure 2.1: Resulting frequency spectrum of a two-tone signal applied to a (higher order) non-linear system. In this figure IMx represent the x-th order intermodulation products, HDx relates to the x-th order harmonics and f_1 and f_2 are the frequencies of the original two-tone test signal.

relatively easy to filter. It will work out, however, that these latter frequency components can be of great importance to the in-band linearity when secondary interaction between the second and fundamental components is taken into account. This will be an important issue in the discussion of the low-distortion varactor configurations in Chapter 4, as well as the linearity of bipolar devices in Chapter 8.

Power dependence of the distortion components and higher order intercept points

When considering equation (2.5) it can be noted, that the resulting amplitudes of the various frequency components have different relations with the amplitude of the input signal. This relation depends on the order of the signal component under consideration, yielding different slopes versus input power. These relations are plotted in Fig. 2.2 for the fundamental, $IM3$ and $IM5$ components. Note, that the fundamental component rises with a slope of one, while the third order and fifth order dominated terms have a slope of three and five, respectively. The different slopes yield virtual intersects when performing an extrapolation of these components with input power, which are referred to as third and fifth-order intercept points ($IP3$, $IP5$). The intercept points at various orders (IPx) are often used as a measure of the linearity of the system under consideration; the higher these intercepts are, the higher the linearity of the system. Also in this thesis work these quantities are used to characterize the linearity of circuit components. The third or fifth-order (for $IM3$ compensated systems) intercept points are used, depending on the nature of the device under consideration. These intercept points are related to the signal conditions present at the input and output of a system. Therefore, e.g. for an amplifier both input ($IIP3$) and output intercept points ($OIP3$) are in use, which can be related as: $OIP3 = IIP3 + Gain$ in dB, as indicated in Fig. 2.2.

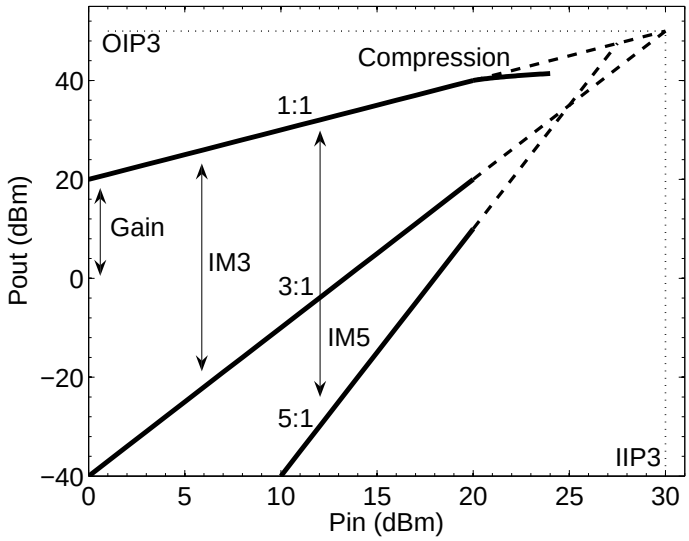


Figure 2.2: Fundamental and third- and fifth-order intermodulation products as function of input power. The powerlevels are given for indication purposes only.

2.1.3 Three-tone excitation for cross-modulation

Both, single-tone and two-tone excitation tests can be used to quantify linearity performance. However, both these tests are in-band, which means the input signals fall into the frequency band of interest of the circuit. However, also outside this band of interest signals can be present. These signals are the out-of-band signals. Typically a circuit rejects these so called out-of-band signals. However, if a very strong out-of band signal is present it can still influence the in-band signals, through undesired mixing with other signals, creating in-band distortion products. Such an out-of-band signal is often called a jammer. A typical test to qualify the system's susceptibility to such a signal is a three-tone test. While a two-tone excitation is often employed to quantify the linearity of band limited systems, a three-tone excitation is better suited for wide-band systems, e.g. CATV (Community Antenna TeleVison) or receiver systems. Consequently, the three-tone test is used to quantify the cross-modulation, which arise as the distortion products around a single jammer, in this particular case the jammer is in-band, as shown in Fig. 2.3. When a triple sinusoidal signal is present at the input, the resulting frequency components can be found in the same way as for single (2.3) or two-tone excitation (2.5). The $IP3$ can be calculated by a three tone test as well and is given by [18]:

$$IP3 \approx 10log(2) + P_{txl} - \frac{\Delta P_{xmod}}{2} \tag{2.6}$$

Where P_{txl} is the power per signal of the two out-of-band signals f_1 and f_2 in dBm and ΔP_{xmod} is the difference in dBc between the in-band jammer signal f_{jam} and the

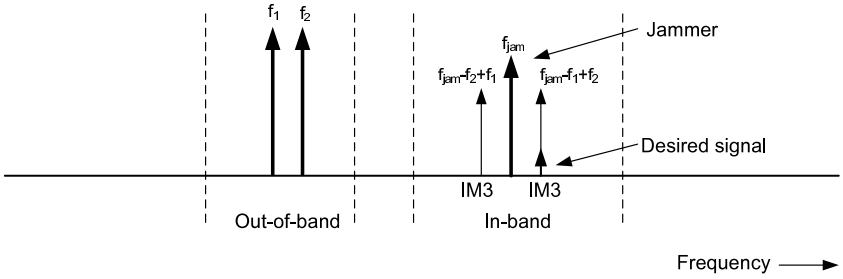


Figure 2.3: Three-tone excitation to measure cross-modulation, only the most important distortion products are indicated. f_{jam} is the in-band jammer signal, the upper $IM3$ product obscures the 'desired signal'.

nearby distortion products.

2.1.4 Wideband modulated signals

To demonstrate the effect of non-linear distortion on a realistic wideband signal, the spectrum of a W-CDMA (Wideband Code Division Multiple Access) signal is presented with and without distortion. Distortion leads to so-called spectral re-growth around the desired signal in the communication system, as demonstrated in Fig. 2.4. The leakage due to spectral re-growth into the side-by-side channels is given by the ACLR (Adjacent Channel Leakage Ratio). Since this phenomenon appears as in-band distortion, a two-tone test can be useful to get insight in this type of non-linear distortion. In Fig. 2.4 the neighboring channels are indicated where this spectral re-growth results in channel-to-channel interference. Spectral re-growth can be seen to some extend as the accumulation of many-tone signals, yielding numerous frequency components outside the desired operating channel.

2.2 Non-linear behavior of bipolar devices

In this section the non-linear distortion behavior of bipolar transistors is discussed. Linear distortion, e.g. amplitude and/or phase variation in the transfer-characteristics versus frequency, is assumed to be without any influence in these specific cases. In general, distortion can be divided into weak and strong non-linearities. In this work the focus will be on weak non-linearities. Strong non-linearities, like clipping of a voltage or current waveform, are considered to be outside the scope of this thesis. For the distortion behavior of the bipolar transistor several phenomena play a role. Here they will be identified and the most important ones will be discussed.

Typically, advanced models in simulators are used to describe all relevant effects in these devices; examples of such models are Mextram [19] and Hicum [20]. However, these models are too complex to be useful for analytical linearity consideration. Instead a more limited representation will be used, which includes the most important contributions. From literature the following effects are known to be of importance.

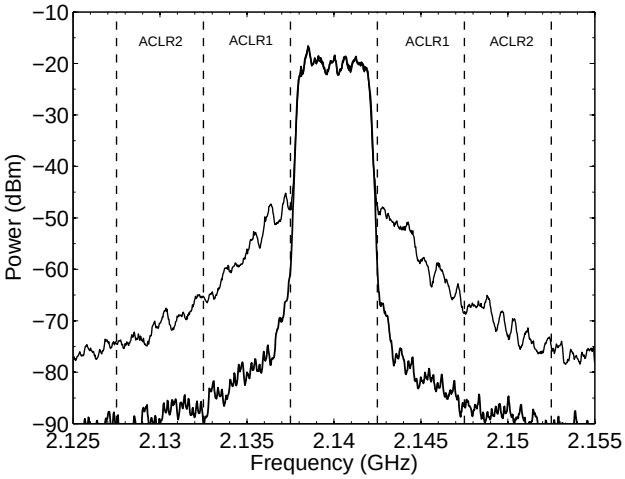


Figure 2.4: W-CDMA signal with low spectral re-growth and increased spectral re-growth due to non-linear behavior of the transmitter chain.

Firstly, the exponential behavior of a bipolar device:

$$I_c = I_s \left(\exp \frac{V_{be}}{v_t} - 1 \right) \approx I_s \exp \frac{V_{be}}{v_t} \tag{2.7}$$

where I_c is the collector current, I_s the saturation current, V_{be} the applied base emitter voltage and the thermal voltage $v_t = \frac{kT}{q}$, with k the Boltzmann constant, q the electron charge and T for the temperature. The base current I_b is assumed to be linearly related to the collector current by the current gain β. The dependence of collector current $i_c(t)$ on base emitter voltage $v_{be}(t)$ can be expressed by the transconductance g_m, which for a time-dependent input signal results in

$$i_c(t) = g_m v_{be}(t) + g_{m,2} v_{be}^2(t) + g_{m,3} v_{be}^3(t). \tag{2.8}$$

Furthermore, the base emitter diffusion capacitance C_{JE}, resulting from the charge formed by the current flowing from emitter to base is important. Finally, the non-linear feedback through the base-collector capacitance plays an important role.

Since the common emitter (CE) configuration is often applied in power amplifiers, a typical CE amplifier scheme is given in Fig. 2.6. The distortion analysis will be done according to this scheme. Furthermore, the actual testing, as done later in this thesis, will also be performed in CE configuration. The $Z_{s,x}$ and $Z_{l,x}$ represent the source and load impedances that the bipolar device 'sees' at the different frequency bands of interest. Therefore, they represent the source/load impedances provided by the 'real' matching networks.

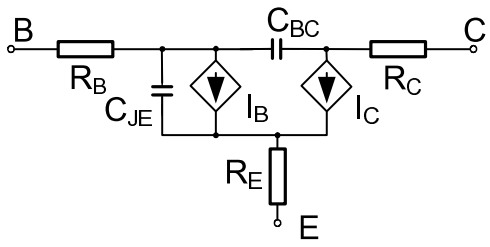


Figure 2.5: Simplified lumped element representation of a generic bipolar device, with the most dominant contributors to non-linear distortion.

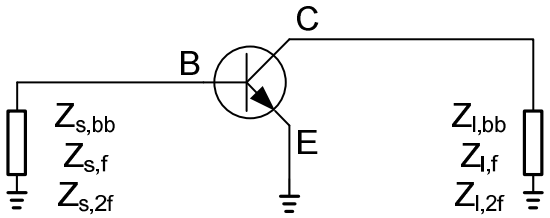
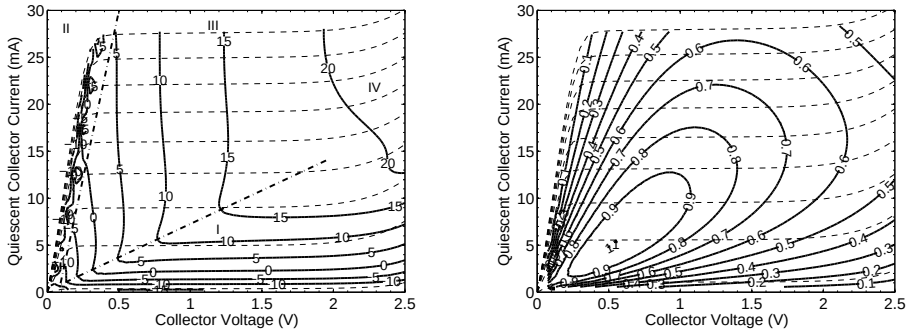


Figure 2.6: Common emitter (CE) stage of generic bipolar device. Biasing has been omitted.

2.2.1 Linearization of non-linear elements within the bipolar transistor

When using a circuit simulator to evaluate the distortion properties of a bipolar device in CE configuration, the regions where certain non-linearities tend to dominate can be identified (Fig. 2.7(a)). This is done by switching the individual non-linear contributions on and off in a modified verilog-A model [21]. Doing so the bias operating conditions where the exponential, C_{bc}, τ_f and avalanche dominate could be determined. Following this excercise only the contributions as shown in Fig. 2.5 were included with the analytical considerations.

To analyze distortion analytically several techniques exist. For weak non-linear behavior the distortion can be analyzed analytically using Volterra series [22]. Many examples of this technique can be found in literature e.g. [23]. Using Volterra series, one can describe a non-linear system in a similar way as done with a Taylor series expansion around a bias point. However, in contrast to Taylor series based considerations, Volterra series calculations can include the impact of reactive components (e.g. capacitors, inductors). This allows the inclusion of the frequency response, as well as memory effects. Using Volterra techniques, the small excursions around a bias point can be described using a limited amount of terms (e.g. up to third or fifth-order) in order to keep the equations manageable. The result is basically a summation of different non-linear contributions, which makes it possible to identify dominant linearities and their point of origin. This technique will be shortly discussed in Section



(a) (b)

Figure 2.7: (a) Contours of constant OIP3 (dBm) and (b) normalized efficiency $\frac{\eta}{\max(\eta)}$ plotted in the $I_c(V_{ce})$ plane for a Qubic bipolar device in CE configuration with 50 Ohm input and output at 2 GHz. The $I_c(V_{ce})$ plane can be divided in the following regions: I) dominated by exponential non-linearity, II) hard saturation, III) dominated by C_{bc} non-linearity and IV) avalanche influenced non-linearity.

2.3 to present the current state of the art in literature.

2.2.2 Linearity efficiency trade-off

The two most important requirements on the transmitting front-end are its linearity and efficiency. Typically, a class AB amplifier can only provide maximum efficiency at maximum output power, therefore, in practice, to comply with the spectral requirements and avoid distortion between channels/services a trade-off between efficiency and linearity needs to be made (Fig. 2.7). By operating in power back-off, that is to reduce the operation power below the maximal possible peak power, one can increase the linearity at the cost of a decay in efficiency. This can be illustrated by using Fig. 2.2. When reducing the input power, the third-order distortion products, which are often the most important ones, reduce by a factor three compared to the fundamental power. Furthermore, linearity can be improved by increasing the device size and the DC bias conditions proportionally. Namely, doubling the device size, or assuming two devices in parallel, such that each of the devices receives half the input power, will improve the overall IIP3 by 3 dB, at the expense of requiring twice the dc power. Therefore, methods which can improve linearity without sacrificing efficiency are very attractive.

2.3 Out-of-band termination of bipolar devices

In the previous discussion the dominant sources of non-linear distortion in bipolar devices were identified. Here, the out-of band linearization method will be discussed,

which can reduce the non-linear distortion without any increase in DC power consumption.

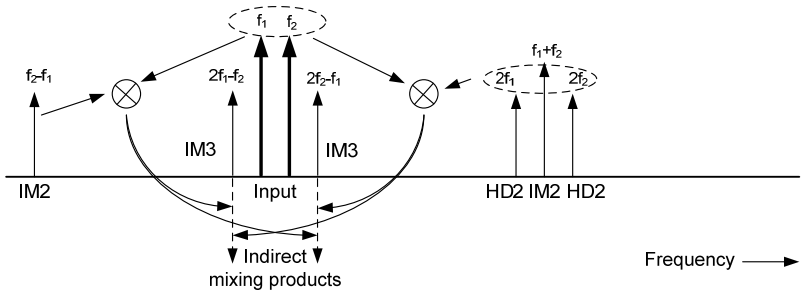


Figure 2.8: The out-of-band linearization technique, in this approach the out-of-band terminations in baseband and at the double frequency are used to cancel the in-band 'direct' $IM3$ products by the 'indirect' $IM3$ products, after [24].

The principle of out-of-band linearization is shown in Fig. 2.8, which gives the typical output spectrum of a non-linear device under two-tone excitation (see also Fig. 2.1). When an active device is driven with a two-tone signal, its non-linearities will yield intermodulation distortion. The third-order device non-linearities will give rise to the so-called 'direct' $IM3$ products. Whereas, the mixing of the $IM2$ products (baseband and second harmonic frequencies), over the non-linear junction of the device with the desired fundamental signal, will give rise to the so-called 'in-direct' $IM3$ components (Fig. 2.8). By controlling the base-band ($Z_{s,bb}$ and $Z_{l,bb}$) and 2nd harmonic impedances ($Z_{s,2f}$ and $Z_{l,2f}$) at the in- and output of the device (Fig. 2.6), the magnitude and phase of these indirect $IM3$ components can be adjusted. Therefore, the indirect $IM3$ products can be used to cancel the direct ones. This method can provide excellent linearity over a large power range up to the compression point [25] (Fig. 2.2). For a given bipolar technology there is an optimum combination of base-band and second harmonic source impedance that result in perfect $IM3$ cancellation over an unrestricted bandwidth. Under the constraint of short-circuited out-of-band impedances at the output of the active device, while neglecting the parasitic base and emitter resistance, the source out-of-band conditions for a CE-stage for frequency independent $IM3$ cancellation are given by [26]:

$$\begin{aligned} Z_{s,bb} = Z_{s,2f} &= \frac{\beta}{2g_m}, \\ \text{while } I_{cq,opt} &= v_t \frac{C_{je}}{2\tau_f}. \end{aligned} \tag{2.9}$$

As mentioned previously, normally there is a direct trade-off between linearity and efficiency. Consequently, improving the linearity without sacrificing efficiency is very advantageous. Therefore, in this work the method of out of band terminations is experimentally investigated in Chapter 9 to improve the linearity of bipolar devices.

2.4 Conclusion

Some standard test signals for linearity verification have been discussed. These will be applied to devices to quantify their linearity, for example to tunable devices for RF adaptivity or bipolar devices. For the later one, the tests are driven by the demand to increase their linearity performance without sacrificing efficiency. For this purpose a suitable method namely out-of-band linearization has been introduced.

Chapter 3

Review of Varactors for RF adaptivity

3.1 Introduction

At this moment PIN Diodes [27], GaAs 'pseudomorphic high electron mobility transistors' (pHEMT) [28, 29] and CMOS on sapphire switches (SOS) [30] are used in industry to implement RF adaptivity through switching. However, besides performance constraints in view of losses, these solutions are considered to be too expensive, area consuming, technologically incompatible, or consume too much dc power, to be an acceptable long term solution for cost and performance sensitive applications.

An ideal tuning element for RF applications will exhibit extremely low-loss, low dc power consumption, high linearity, excellent ruggedness, wide tuning range, high reliability, low area usage and is preferably continuously tunable with a high tuning speed. This all is required in combination with a very low cost level in mass production. This rather extensive list of requirements has initiated intensive research world wide to come up with new technology solutions that can meet these requirements. In most of these approaches the attention is directed to tunable reactive elements that can offer a tunable/variable capacitance. In this chapter a short overview of these technology developments is given and their pros and cons will be discussed.

3.2 Tunable varactor elements

One of the most active research activities related to RF adaptivity is devoted to the MEMS capacitor, which in its most popular implementation is able to switch between two fixed capacitance values. MEMS capacitors can provide a very high Quality Factor (Q) for small capacitance values and an extraordinarily high linearity [31, 32]. However they require non-standard processing and packaging techniques, high control voltages, and their reliability and switching speed are still poor compared to semiconductor-based solutions. Other proposed tuning techniques, based on voltage-variable dielectrics, exhibit similar drawbacks of manufacturability and

Table 3.1: Comparison of tunable elements - continuously tunable varactors and switches - with respect to power consumption, control voltage, loss and distortion. The solutions introduced in this thesis are not included here.

Technology	power consumption	control voltage	voltage handling	typical loss	distortion
pn	++	+/–	+/–	+/–	–
BST	++	+/–	+/–	+/–	–[a]
MOS (SOS)	++	+	–	+/–	–[a]
MEMS varactor	++	–	+	+[b]	+
MEMS switch	++	–	++	++	++
PIN	–	+	+	+[c]	+/–
PHEMT	+	+	+/–	+	–[a]

[a] Good results have been reported for multiple stacked devices. [b] For small devices. [c] For high bias currents.

performance [33]. In view of this, more simple tunable elements like varactor diodes would seem to be a logical choice for implementing RF adaptivity [34]. However, their inherently nonlinear behavior disqualifies them for use with modern communication standards characterized by high peak-to-average power ratios, and their related Q factors are usually too low at the microwave frequencies of interest for the most demanding applications. A summary comparative between various tunable varactor elements is given in Table 3.1. These tunable elements depend on voltage dependent dielectric (BST), change in area (MEMS, capacitive switch bank), change in distance of the conductive plates (pn, MOS, MEMS) or a current/voltage dependency of the conductivity (pHEMT, PIN). The results in the table depend on the following considerations:

Power consumption - Most devices draw only a small current during operation, since they are either reverse biased (e.g. pn) or are low conductive (e.g. BST, MOS, MEMS). The exception is the PIN diode which requires a relatively large current for low loss operation.

Control voltage - Both pn and BST varactors require relatively moderate control voltages (10-20 V) in contrast to MEMS devices (50-100 V). For MEMS switches the pull-in voltage has to be sufficiently large to avoid self-actuation under large signal RF voltage swings, while the pull-out voltage has to be large to avoid non-release during hot-switching. In aggressively downscaled MOS, the control voltages are small, however MOS varactors can be realized with control voltages similar to pn varactors.

Voltage handling - The voltage handling is complementary to the control voltage, since typically high control voltages imply good large voltage handling.

Typical loss - The pn, BST and MOS varactor have similar loss performance, although the loss mechanisms are only partly identical. They all have losses in their metal connections, however in BST the dielectric losses will dominate. The losses in pn varactors will be discussed in Section 3.3. In contrast MEMS varactors only have

metal losses, therefore their low loss performance is expected to exceed that of the other devices, as will be shown in Section 3.4, where losses in different technologies are compared.

Distortion - Due to their inherent nonlinear behavior all these devices exhibit (some) distortion. In this respect MEMS devices typically perform well due to their high voltage capability and low mechanical cutoff frequency, above which the envelope of the RF voltage does not modulate the (off-state) capacitance.

3.3 Conventional semiconductor varactors

Semiconductor varactors are based on a reversed biased junction that can provide a variable capacitance with changing voltage (Fig. 3.1(a)). In these devices the actual capacitance is controlled by the voltage defined thickness of the depletion layer around the junction. Basically there are two major types of semiconductor varactor diodes, namely based on the pn junction diode and the Schottky diode. Only devices where the p-layer is doped much higher than the n-layer are considered here, since the higher mobility of electrons can provide higher Q-factors.

The main difference between the two varactor diodes is the carrier transport over the junction. In a Schottky diode the current mainly consists of majority carriers, whereas in a pn junction diode the relevant carriers are minority carriers. This has as a consequence that Schottky diodes have no minority carrier charge storage, which makes them faster when operated as switches. However, this feature does not influence their performance too much when operated as varactor. For their function as varactor more important is the reverse bias leakage, which for a proper dimensioned pn junction, below breakdown is mostly dominated by the generation/recombination current in the depletion region. In view of this the reverse bias current for a Schottky diode is a thermionic emission current over the Schottky barrier. This barrier gets lowered for an increased reverse bias voltage. Therefore the resulting leakage current is typically orders of magnitude higher than the generation/recombination current of the pn junction diode. Another difference between these two types of diodes can be found in the series resistance of the p-layer, since this layer is not present in the Schottky diode (Fig. 3.1(b)). One would expect that a Schottky diode could potentially reach a higher Q. However, the series resistance of the p-layer is only important in the contact resistance dominated regime (vertical current flow), it offers not necessarily an advantage compared to a pn junction due to difference in size for a given capacitance value. This is due to the fact that the zero bias capacitance density of a Schottky diode is higher than that of a pn diode, due to its lower build-in voltage (ϕ).

The breakdown mechanisms of these two types are typically the same. However, due to the higher leakage in Schottky devices often the leakage current influences the ideal varactor function before breakdown is reached.

From literature it is known that loss, linearity and power handling are the most important limitations for these components, which will be discussed in the following sections.

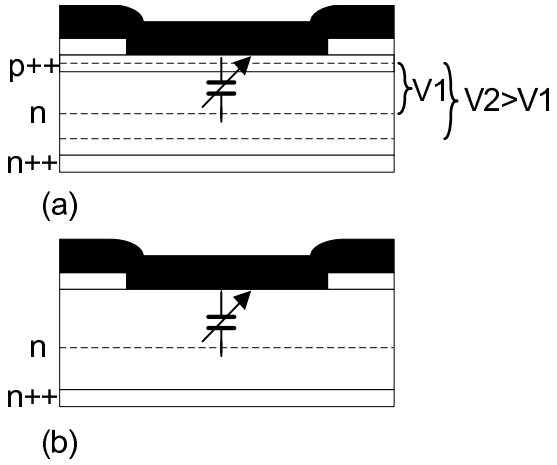


Figure 3.1: (a) pn junction varactor diode, the depletion region increases with increased reverse bias voltage (b) Schottky junction varactor formed by the metal to semiconductor.

3.3.1 Loss of varactors

The loss performance is expressed by the quality factor (Q), where

$$Q \approx \frac{\Im(Z_{var})}{\Re(Z_{var})}, \tag{3.1}$$

where Z_{var} is the impedance of the varactor diode. Note, that this equation is not valid near the resonance frequency of the device. This can be derived from the average energy stored over the energy loss [35, 36].

Loss of the intrinsic one dimensional varactor

For reason of simplicity an uniform doping in the n-region is assumed. Now, consider the simplified varactor diode structure of Fig. 3.1(a), with an ideal junction between an uniform lightly doped n-layer and a much more heavily doped p^+ region. The resistance due to the highly doped p^{++} and n^{++} connecting region is here assumed to be negligible.

Starting with the conventional textbook equation [37], the following can be derived. The varactor diode capacitance C is given by

$$C = \frac{\epsilon A}{x_n}, \tag{3.2}$$

where ϵ is the material permittivity, A is the diode area, and x_n is the depletion width given by

$$x_n = \sqrt{\frac{2\epsilon N_a(\phi - V_j)}{qN_d(N_a + N_d)}}, \tag{3.3}$$

where

$$\phi = v_t ln\left(\frac{N_a N_d}{n_i^2}\right) \tag{3.4}$$

and N_a, N_d and n_i are, the acceptor, donor and intrinsic carrier concentrations respectively.

Using the expression for x_n we can solve for the breakdown voltage by setting the maximum value of the electric field E_{max} ($qN_d x_n/\epsilon$) equal to the critical electric field for the material at a given doping level, yielding

$$V_{break} = -\frac{\epsilon}{2}\left(\frac{N_a + N_d}{qN_d N_a}\right) E_{crit}^2(N_d) + \phi. \tag{3.5}$$

The resulting breakdown voltage for a uniformly doped silicon pn varactor device, as function of doping concentration, is given in Fig. 3.2. As the doping level is decreased, the resulting breakdown voltage increases. However, the series resistance of the undepleted region also increases, lowering the Q. The resistance for the completely undepleted situation for silicon can be written as:

$$R_{var} = \frac{\psi_{si} l}{A} \approx \frac{x_n(V_{break})}{qN_d \mu_n A}, \tag{3.6}$$

in which the length l is set to the thickness of the lightly-doped n-region $x_n(V_{break})$, which is bounded by the breakdown constrained maximum depletion width for a given doping concentration. Furthermore, ψ_{si} represents the doping dependent resistivity of silicon, which at room temperature for the doping range of $10^{15} \sim 10^{18}$ cm^{-3} is approximately [37]:

$$\psi_{si} = \frac{4 \times 10^{12}}{N_d^{0.8}}. \tag{3.7}$$

Using (3.2)-(3.7) the Q of the varactor diode is calculated and shown in Fig. 3.2 versus doping concentration for the zero-bias condition. Note, that this situation represents the worst-case condition, since the Q tends to improve for higher reverse bias of the diode, due to the decrease in capacitance as well as series resistance, caused both by the increased size of the depletion region. The conclusion of this analysis is that, in order to maintain a Q of greater than 100 at 1 GHz for a silicon device, the doping level must exceed 3.10^{16} cm^{-3}, which limits the breakdown voltage to less than 25 V. Although this already represents an excellent level of performance, further Q enhancement can be achieved in a material system with a better mobility/breakdown voltage trade-off, such as GaAs, SiC or GaN, provided, that in these technologies a low contact resistance can be realized.

Loss of the extrinsic varactor

In the previous section the breakdown/intrinsic Q tradeoff was discussed. However, the Q is not only limited by the intrinsic resistance; the device still needs to be contacted with its metal connection tracks, therefore, the contact resistance between the metal and semiconductor material, as well as the resistance of the metal tracks become important. In Fig. 3.3 the left metal-track connects to the Schottky junction

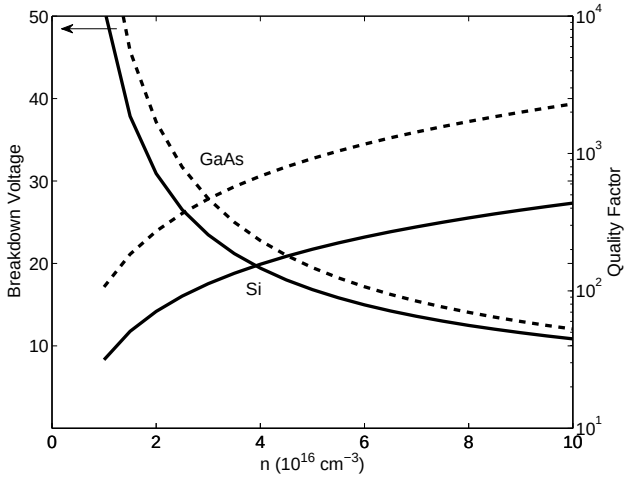


Figure 3.2: Intrinsic quality factor at 1 GHz and breakdown voltage for silicon (solid lines) and GaAs (dashed lines) varactor diodes as a function of doping.

on the n region material, while the right metal-track connects to a highly doped n region (DN), which ensures the connection to the buried n-region at the bottom of the device. The equivalent lumped loss components are indicated in the figure. Typical sheet resistance values for aluminum are in the order of 40 mΩ, whereas a buried layer typically has a sheet resistance of 30 Ω. The contact resistances are typically much lower for reasonably sized contacts; in the case of laser annealed contacts they provide values in the order of 10^{-7} Ω cm^2 [38]. From the above results we can directly

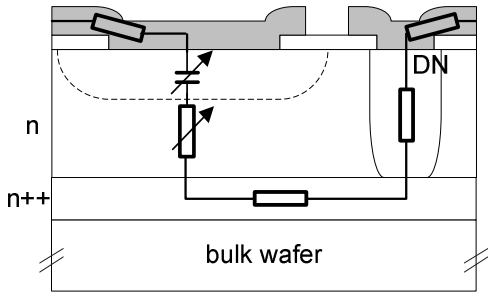


Figure 3.3: Schottky junction varactor with indicated losses, both intrinsic and extrinsic.

conclude that the buried n^{++} layer will usually dominate the losses. To improve for this situation typically finger structures are introduced at the expense of higher area usage and additional parasitics, e.g. the direct capacitance between these fingers. However, also other layouts could be considered [39]. In the context of this thesis a more aggressive strategy to improve the Q will be introduced in Chapter 5.

3.4 Comparison varactor technology achievements

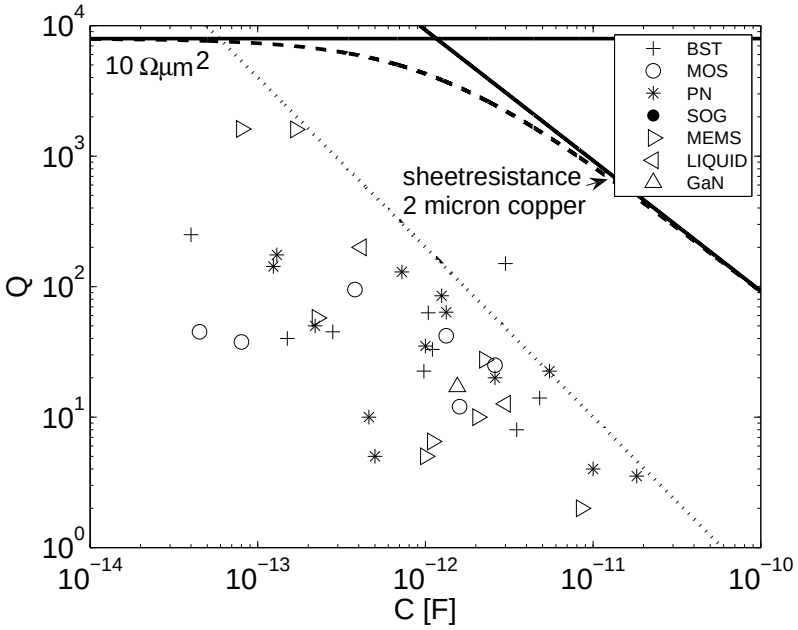


Figure 3.4: Normalized Quality factor (Q) at 2 GHz versus capacitance for different technologies, the dashed line indicates the potential Q (based on a capacitance-density of 1 fF/μm^2) when only the metal resistance and contact resistance are limiting. The dotted line indicates the apparent trend in Q versus capacitance value.

Specific data are visualized in Fig. 3.4, which gives an overview of the different varactor technology achievements, as published in IEEE publications over the period 1997-2007 [79]. In this figure the normalized quality factor (Q) at 2 GHz for different technologies is given with the related references in Table 3.2. For all cases the Q-factor at the highest reported capacitance value is taken.

When studying Fig. 3.4 the following can be observed. Firstly the dashed line indicates the limitation of a semiconductor device, due to the resistance of the metal (here shown as 2 μm of copper) and the contact resistance to the semiconductor (10 Ω μm^2). For the implementations using pn, BST, MOS, GaN and Liquid technologies, the measured data mostly deviate from this indicated line, which suggests that other losses such as buried layer resistance or dielectric losses, constrain the total quality factor of these devices. Secondly, the dotted line indicates the apparent trend in quality factor versus capacitance value.

For the pn junction varactors the scaling depends on contact resistance, intrinsic resistance and metal resistance. Note, that the contact resistance and intrinsic resistance will limit the maximum Q for small devices, whereas the metal resistance will

Table 3.2: References for tunable varactor technologies from Fig. 3.4

Abreviation	Varactor technology	References
pn	PN junction	[40–49]
BST	Barium Strontium Titanate	[50–59]
MOS	Metal Oxide Semiconductor	[42, 60–66]
GaN	Gallium Nitride	[67, 68]
Liquid	Liquid dielectric	[69]
MEMS	Micro Electro Mechanical System	[70–78]

limit the Q for large devices. This is due to the fact, that in first order approximation, the contact/intrinsic resistance scales inversely with the area, whereas the metal resistance in the ideal case remains constant.

For MEMS devices, there is no contact resistance, since the metal plate forms the capacitance directly. Therefore, it only scales with the metal resistance. This clearly gives advantages for the application of small MEMS devices, making MEMS an excellent candidate for high performance mm-wave applications. For the RF applications in the low GHz range, however, there is no real advantage related to Q over semiconductor based varactors. In fact, the higher capacitance density of semiconductor devices, due to the high dielectric constant of semiconductors, seems to be an advantage when implementing the practical capacitance values needed for these RF applications.

The lower capacitance density of MEMS is also related to an effect called 'snap-down', which may occur when the two plates are close together with a significant voltage applied to them, that forces the plates together. To avoid this snap-down effect a certain minimum separation between the plates should be maintained. This minimum separation reduces the achievable capacitance density for continuously tunable MEMS devices. This is a reason why the MEMS (capacitive) switch is often preferred over the MEMS varactor. Capacitive switching MEMS devices typically use a thin dielectric layer on one of the plates, allowing for small separations of the plates, which increases their maximum achievable capacitance density.

Secondly, in a MEMS device a trade-off exists between tuning range and Q, which for MEMS devices is often limited by the connections to the plates. These connections should be small enough to be flexible, yet large enough to ensure low series resistance to avoid degradation of the Q-factor. The fact that most of the measured data of the MEMS devices deviates from the ideal metal resistance scaling reveals that the connection losses play a more important role in determining the total quality factor of MEMS devices. Furthermore the connections should be stiff enough to support the plates to prevent mechanical failure, this may reduce the achievable tuning range. This is more favorable for small (mm-wave) MEMS devices, since the mass of the moving part is lower.

3.5 Conclusion

Several tunable components exist. They have been examined with respect to their power consumption, control voltage, voltage handling, losses and distortion properties. In particular the origin of losses in various varactor technologies has been discussed. Furthermore, the fundamental trade-off of breakdown voltage and loss for semiconductor varactors has been illuminated. When comparing the relation between a specific capacitance value and its associated losses, semiconductor devices perform best for large capacitance values, whereas MEMS devices seem to be better suited for small capacitance values. However, if the contact resistance and intrinsic resistance of semiconductor devices are both low, their performance may approach the performance of MEMS devices at mm-wave frequencies.

Chapter 4

Linear varactors for RF adaptivity[1]

4.1 Introduction

Varactor diodes are typically unsuitable as components in linear systems, due to their inherent non-linearity. In order to overcome this drawback a new, semiconductor based varactor solution, as has been developed within the context of this thesis, will be introduced. The proposed solutions consist of varactor diode-based circuit topologies, which for a given grading coefficient ($n > 0.5$), can act as variable capacitors with extremely low or, in the special case of $n = 0.5$, theoretically without any distortion. These low distortion varactor stack components are, through their ease of implementation and inherently high performance, suitable for use in a variety of high-Q tunable circuits, including filters, switches, phase shifters and matching networks.

4.2 Distortion free varactors

4.2.1 General theory of non-linear varactor diode topologies

When considering a reverse-biased varactor diode, or any nonlinear capacitance, we can write the current through the capacitor using a Taylor series as,

$$i_c = C_0 \frac{dv}{dt} + \frac{C_1}{2} \frac{dv^2}{dt} + \frac{C_2}{3} \frac{dv^3}{dt} + ... \tag{4.1}$$

[1]Parts of this chapter were published by: K. Buisman, L. C. N. de Vreede, L. E. Larson, M. Spirito, A. Akhnoukh, T. L. M. Scholtes and L. K. Nanver, "Distortion-free varactor diode topologies for RF adaptivity," in Microwave Symposium Digest, 2005 IEEE MTT-S. And by: K. Buisman, C. Huang, A. Akhnoukh, M. Marchetti, L. C. N. de Vreede, L. E. Larson and L. K. Nanver, "Varactor Topologies for RF adaptivity with improved power handling and linearity," in Microwave Symposium Digest, 2007 IEEE MTT-S.

where, v is the small-signal incremental voltage applied to the varactor terminals, and the coefficients C_0, C_1, ...C_n are the Taylor coefficients that depend on the dc operating point of the varactor, i.e.

$$C(v) = \frac{dQ}{dv} = C_0 + C_1 v + C_2 v^2 + ... \tag{4.2}$$

The coefficients C_1, ...C_n are responsible for the generation of distortion products in the circuit. In particular, the second-order distortion created by C_1 and the third-order distortion created by C_2 should both be made as small as possible.

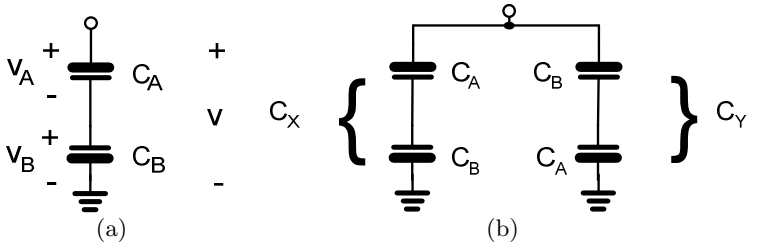


Figure 4.1: (a) Anti-series connection of arbitrary nonlinear capacitors to minimize third-order distortion and (b) anti-series/anti-parallel connection of nonlinear capacitors to minimize second and third-order distortion.

If two capacitors C_A and C_B are connected in the "anti-series" configuration, as shown in Fig. 4.1, then we can write,

$$C_A(v_A) = C_{A0} + C_{A1} v_A + C_{A2} v_A^2 + ... \tag{4.3}$$

$$C_B(v_B) = C_{B0} - C_{B1} v_B + C_{B2} v_B^2 + ... \tag{4.4}$$

where the minus sign in (4.4) comes from the reversed connection of C_B. When current flows through the capacitors the incremental charge is given by

$$Q(v_x) = \int_0^{v_x} C(v) dv. \tag{4.5}$$

In this case, the incremental charge on the two capacitors C_A and C_B is the same, and is given by

$$Q(v_A) = C_{A0} v_A + \frac{C_{A1}}{2} v_A^2 + \frac{C_{A2}}{3} v_A^3, \tag{4.6}$$

$$Q(v_B) = C_{B0} v_B - \frac{C_{B1}}{2} v_B^2 + \frac{C_{B2}}{3} v_B^3. \tag{4.7}$$

Since these two charges are equal, we can set $Q(v_A) = Q(v_B) = Q$ and solve for v_A and v_B through a series reversion. The total voltage across the series capacitor v is the sum of the two individual voltages v_A and v_B, so

$$v = S_0 Q + S_1 Q^2 + S_2 Q^3 + ... \tag{4.8}$$

where

$$S_0 = \frac{1}{C_{A0}} + \frac{1}{C_{B0}}, \tag{4.9}$$

$$S_1 = \frac{C_{B1}}{2C_{B0}^3} - \frac{C_{A1}}{2C_{A0}^3} \tag{4.10}$$

and

$$S_2 = \frac{C_{A1}^2/2 - C_{A0}C_{A2}/3}{C_{A0}^5} + \frac{C_{B1}^2/2 - C_{B0}C_{B2}/3}{C_{B0}^5} \tag{4.11}$$

Taking the results from (4.8)-(4.11) and performing one last reversion and a differentiation yields:

$$C_{as}(v) = C_0 + C_1 v + C_2 v^2 = \frac{1}{S_0} - \frac{2S_1}{S_0^3} v + \frac{6S_1^2 - 3S_0S_2}{S_0^5} v^2, \tag{4.12}$$

where the linear and quadratic terms in v need to be minimized - ideally to zero - in order to reduce the distortion in the circuit. This result is essentially identical to what was obtained in [80] and will now be utilized as starting point for the introduction of more generalized low-distortion varactor topologies.

There are several possibilities for minimizing the C_2 term in (4.12), which is primarily responsible for the third-order distortion in the current. If the nonlinear capacitors are fabricated in the same semiconductor process and operated at the same dc bias, but their sizes differ by some constant s, then their non-linear coefficients will each differ by s, i.e. $C_{B0} = sC_{B0}$, $C_{B1} = sC_{A1}$ and $C_{B2} = sC_{A2}$. In this case the quadratic term in (4.12) can be set to zero when

$$s = \frac{3C_{A1}^2 + 2C_{A0}C_{A2} \pm \sqrt{9C_{A1}^2 + 12(C_{A1}^2C_{A0}C_{A2} - C_{A0}^2C_{A2}^2)}}{4C_{A0}C_{A2}}. \tag{4.13}$$

Although this is a relatively complicated result, there are some straightforward limiting cases that will be examined in the next section.

Unfortunately, setting only C_2 to zero will not completely eliminate third-order distortion in a circuit application, due to the second-order interaction between the C_1 and C_0 terms through the finite source impedance. Complete elimination of third-order distortion would also require that C_1 in (4.12) be eliminated. From (4.10), C_1 can only be set be zero for the case of two equal sized capacitors ($s = 1$) with an identical capacitance voltage behavior, something that is for most cases in contradiction to the requirements for s that follow from (4.13), for the elimination of C_2. Fortunately, the effect of a finite C_1 term can be independently eliminated, by the use of the anti-parallel connection of an identical network, as shown in Fig. 4.1(b). In this anti-parallel connection of two nonlinear capacitors,

$$C_x(v) = C_{x0} + C_{x1}v + C_{x2}v^2 + ... \tag{4.14}$$

$$C_y(v) = C_{y0} - C_{y1}v + C_{y2}v^2 + ... \tag{4.15}$$

the resulting total capacitance is then the sum of all the individual capacitance, i.e.

$$C(v) = (C_{x0} + C_{y0}) + (C_{x1} - C_{y1})v + (C_{x2} + C_{y2})v^2 + ... \tag{4.16}$$

When considering the case of size-matched diodes in the anti-parallel connection of Fig. 4.1(b),

$$C_{asap}(v) = 2C_{x0} + 2C_{x2}v^2 + ... \tag{4.17}$$

The result is perfect canceling of all second-order components, which arise from the C_1 terms. Combining the results of (4.13) - canceling the third-order distortion (so $C_{x2} = 0$ - with (4.17) - canceling second-order (and all even) distortion products - results in a capacitor with no residual distortion of order less than five, a substantial improvement.

4.2.2 Low distortion varactor diode circuits

In order to derive a mathematical description for the low distortion varactor configuration, the starting point is the classical capacitance relation of a single varactor diode, which can be expressed as

$$C(V) = \frac{K}{(\phi + V)^n}, \tag{4.18}$$

where ϕ is the built-in potential of the diode, V is the applied voltage, n is the power law exponent of the diode capacitance, and $K = C_{j0}\phi^n$ is the capacitance constant, where C_{j0} is the zero bias capacitance. The power law exponent can exhibit a wide variation in different situations, from a value of $n = 0.3$ for an implanted junction to $n = 0.5$ for a uniformly doped junction to $n = 2$ for a hyper-abrupt junction.

In order to develop the low distortion varactor diode circuits the Taylor coefficients of (4.18) are derived, yielding

$$C_0 = \frac{K}{(\phi + V_c)^n}, \tag{4.19}$$

$$C_1 = -C_0 \frac{n}{\phi + V_c} \tag{4.20}$$

and

$$C_2 = C_0 \frac{n(n+1)}{2(\phi + V_c)^2}, \tag{4.21}$$

where V_c is the dc bias voltage on the point between the diodes as from Fig. 4.2.

The diode configuration in Fig. 4.2(a) can now be employed to realize a voltage variable capacitor with low third-order distortion. In this case, we set the ratio of the diode areas D_B/D_A to s as in (4.13) and - following the same procedure as in (4.8)-4.13) - this yields expressions for the linear and nonlinear terms of the capacitance of the circuit of Fig. 4.2(a) of

$$C_0 = \frac{sK_A}{(1+s)(\phi + V_c)^n}, \tag{4.22}$$

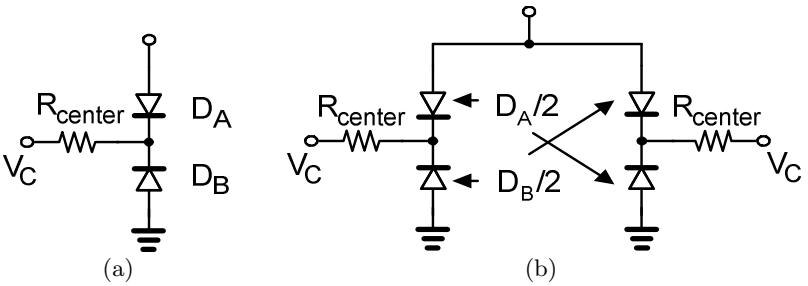


Figure 4.2: (a) Anti-series connection of varactor diodes to minimize third-order distortion. The ratio of the areas of D_A and D_B follows from setting C_2 to zero, for $n \geq 0.5$. (b) Anti-series/anti-parallel connection of varactor diodes to minimize second and third-order distoriton for grading coefficients > 0.5. In this case, both C_1 and C_2 can be set to zero.

$$C_1 = \frac{(1-s)nC_0}{(1+s)(\phi + V_c)} \tag{4.23}$$

and

$$C_2 = \frac{C_0 n[(s^2+1)(n+1) - s(4n+1)]}{2(\phi + V_c)^2(s+1)^2}. \tag{4.24}$$

Note, that - as in (4.13) - C_2 (4.24) can be made equal to zero by setting

$$s = \frac{4n + 1 + \sqrt{12n^2 - 3}}{2(n+1)}, \tag{4.25}$$

resulting in zero third-order distortion caused by the capacitance term C_2. The result of (4.25) demonstrates that cancellation can only occur for cases where the diode power law exponent is equal or greater than 0.5. The second root of (4.24) and (4.13) can be neglected because the two roots are inverses of each other; diode area ratios of value s and $1/s$ both result in $C_2 = 0$.

Also, as was pointed out originally in [80], a constant doping profile in the diode (the so-called "abrupt junction" case, where $n = 0.5$) results in a value of s of unity. This case is particularly attractive because - from (4.17) - this set of conditions ($n = 0.5$ and $s = 1$), sets both C_2 and C_1 equal to zero. A more elaborate analysis shows that all higher order distortion terms vanish, yielding (in theory) a 'distortion-free' operation for this unique case.

The explanation for this desirable 'distortion free' behavior can be intuitively seen from rewriting (4.18) for the diode stored charge as function of the applied voltage for the $n = 0.5$ case, i.e.

$$V = \phi \left(\frac{Q_0^2 - Q^2}{Q_0^2} \right), \tag{4.26}$$

where $Q_0 = 2K/\phi^{n-1}$.

When an incremental voltage v is applied to the diode pair, an incremental charge q is stored in the diodes, and the incremental voltage - in terms of the stored charge - is (from Fig. 4.1(a))

$$\begin{aligned} v &= V_A + V_B \\ &= \phi\left(\frac{Q_0^2-(Q+q)^2}{Q_0^2}\right) - \phi\left(\frac{Q_0^2-(Q-q)^2}{Q_0^2}\right) \\ &= \frac{4\phi Q}{Q_0^2}q \\ &= \frac{2}{C_0}q \end{aligned} \tag{4.27}$$

So, the incremental charge has a linear relationship with the applied incremental voltage in the special case of $n = 0.5$, and the diode pair acts like an ideal voltage-controlled linear capacitor. This principle of producing a linear controlled source from the difference between two square-law controlled sources has also been used extensively in the design of linear MOS transconductors that exploit the square law behavior of long channel MOSFETS [81].

This result can also be used to calculate the ideal center-tap voltage ΔV_{CT}, under RF voltage excitation ΔV, for the special case of $n = 0.5$

$$\Delta V_{CT} = \frac{\Delta V}{2} + \frac{(\Delta V)^2}{16(\phi + V_c)} \tag{4.28}$$

which exhibits only the fundamental frequency and second-order distortion.

When dealing with process technologies that allow a higher capacitance tuning range ($n > 0.5$) the solution of (4.25) provides a direct means to calculate the required diode area ratio to minimize C_2. For example, in the case of $n = 1$, the required area ratio is exactly two. In the case of $n = 2$, which corresponds to the ideal hyper-abrupt junction, the required area ratio is 2.6. These area ratios are straightforward to realize with high accuracy in any standard integrated circuit process that includes (varactor) diodes.

Although this approach can minimize C_2, it is clear from our previous analysis that a value of $s \neq 1$ will result in a finite value of C_1. Fortunately, by placing the identical varactor stack in anti-parallel configuration, as shown in Fig. 4.2(b) this distortion contribution can be eliminated. The resulting linear capacitance of the circuits of Fig. 4.2(a) and Fig. 4.2(b) are identical, but the circuit of Fig. 4.2(b) now has $C_1 = C_2 = 0$ when the proper area ratio is set. It should be noted that all the even-order distortion coefficients are zero (C_1, C_3, C_5, ...= 0) in this topology, but the higher coefficients that create odd-order distortion (C_4, C_6, C_8, ...) are finite, although the IM3 contribution at $(2\omega_2 - \omega_1)$ due to the fifth and higher order nonlinearities are very small.

There are two implications of this analysis. The first is that the configuration of Fig. 4.2(a) provides a "distortion-free" varactor stack (DFVS) when $s = 1$ and $n = 0.5$, corresponding to an uniform doping profile of the varactors. The second is that the more generalized configuration of Fig. 4.2(b) provides an ultra-low distortion varactor stack for any value of $n > 0.5$, by setting the proper ratio of the diode areas,

which sets C_1 and C_2 to zero. This topology provides more freedom for use in different process technologies and facilitates linear operation with a higher C_{max}/C_{min} ratio than the $n = 0.5$ case. Therefore this topology is named the high tuning range varactor stack (HTRVS).

The intercept points of the varactor configurations are a function of the control voltage and can be expressed analytically as shown in Table 4.1. Since varactors are non-dissipative elements, their linearity will be quantified by considering the third-order intermodulation and fundamental current through the varactor. The extrapolated intercept of these currents as a function of the applied two-tone RF voltage yields the third order-intercept voltage IIP3V. Note, that this quantity is independent of the operating frequency as well as capacitance value and is therefore a very suitable linearity measure for a given varactor technology.

Table 4.1: Theoretical voltage intercept points for different varactor diode configurations. The calculated IP2V, IP3V and IP4V for the high tuning-range varactor stack correspond to the $n = 1$, $s = 2$ condition. Since there is no third-order distortion for this configuration, the IP3V value is the extrapolated intercept point of the residual fifth-order distortion at $2\omega_2 - \omega_1$.

	IP2V	IP3V	IP4V
Single diode	$-\frac{\phi+V_c}{n}$	$2\sqrt{\frac{2(\phi+V_c)^2}{n(n+1)}}$	$2\left(\frac{-(\phi+V_c)^3}{n(n^2+3n+2)}\right)^{\frac{1}{3}}$
DFVS	∞	∞	∞
HTRVS ($n = 1$, $s = 2$)	∞	$\approx 3.4\,(\phi + V_c)$	∞

4.2.3 Optimized biasing networks of anti-series varactor diodes

As was pointed out in the previous subsection, a constant doping profile in the varactor diode results in essentially no distortion in the capacitance of an anti-series pair, which is highly desirable. In these derivations it was assumed that there is no RF current component flowing through the center tap connections. Consequently, to avoid linearity degradation by the center-tap impedance of the dc biasing network, the impedance provided by this network should be significantly higher than the reactance of the varactors itself at all frequency components. In practical situations this is difficult to achieve, e.g. in a two-tone intermodulation test, the center-tap voltage has a component at the difference frequency Δf. When Δf approaches zero, the reactance of the varactors for this difference frequency component increases without any bound. Consequently, the connecting center-tap impedance should become infinite to avoid linearity degradation.

Referring to Fig. 4.3(a), the requirement for linear operation of the varactor stack is given by

$$R_{center} \gg \frac{1}{2\pi C_A \Delta f}. \tag{4.29}$$

For large tone spacings this condition can be satisfied by an integrated resistor, but the resistance value - and hence the required die area - can become prohibitively large

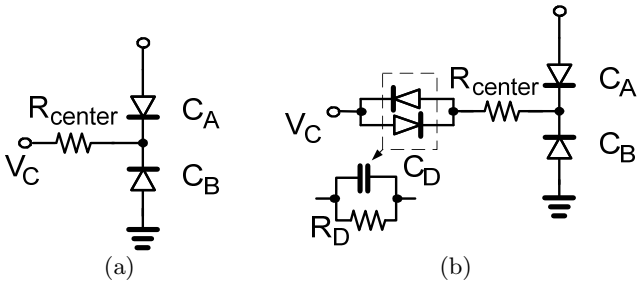


Figure 4.3: (a) Low-distortion anti-series diode configuration with resistor bias. (b) Low-distortion anti-series diode configuration with resistor and antiparallel diode bias for improved performance at low tone spacing.

even for moderate tone spacings. A simple way to implement the high impedance at the center-tap, while keeping the area required for the bias circuit small, is the use of a small anti-parallel diode pair, depicted in Fig. 4.3(b). The zero-bias impedance of the diodes is very high, but now the shunt capacitance of the diodes limits the linearity. Consequently, the centertap diodes should be chosen much smaller in value than the intended varactors in the RF path.

The effect of center-tap impedance on linearity is shown with a specific simulation example of $IIP3$ in Fig. 4.4. The figure shows three distinct regions of operation: the shunt dc leakage impedance of the diodes R_D limits the linearity at very low tone spacings with an IIP3V given by $IIP3V = 8\,(\phi + V_c)$. At moderate tone spacings the zero-bias capacitance C_D of the anti-parallel-diode pair limits the $IIP3$ to a rather constant value, given by:

$$IIP3V = \sqrt{\frac{2C_{j0}^2\left(2C_{j0}+C_D\right)^4}{2C_1^2C_D\left(C_D^3+4C_{j0}C_D^2+6C_{j0}^2C_D+2C_{j0}^3\right)}}, \tag{4.30}$$

which can be approximated, for the uniformly doped case ($n = 0.5$) and for small values of C_D as:

$$IIP3V \approx 8\,(\phi + V_c)\sqrt{\frac{C_{eq}}{3C_D}} \tag{4.31}$$

where C_{eq} is the series equivalent capacitance of the two diodes. This illustrates the importance of low parasitic capacitances for the anti-parallel diode pair and the physical layout of the anti-series configuration. Finally, for a resistive center-tap configuration, the 3dB corner frequency for the high tone spacing regime, where the linearity starts to approach the ideal distortion free operation (infinite IIP3V) can be expressed as

$$\Delta f_{corner} = \frac{3/4}{2\pi C_{eq}R_{center}}\sqrt{\frac{\phi + V_c}{\phi}} \tag{4.32}$$

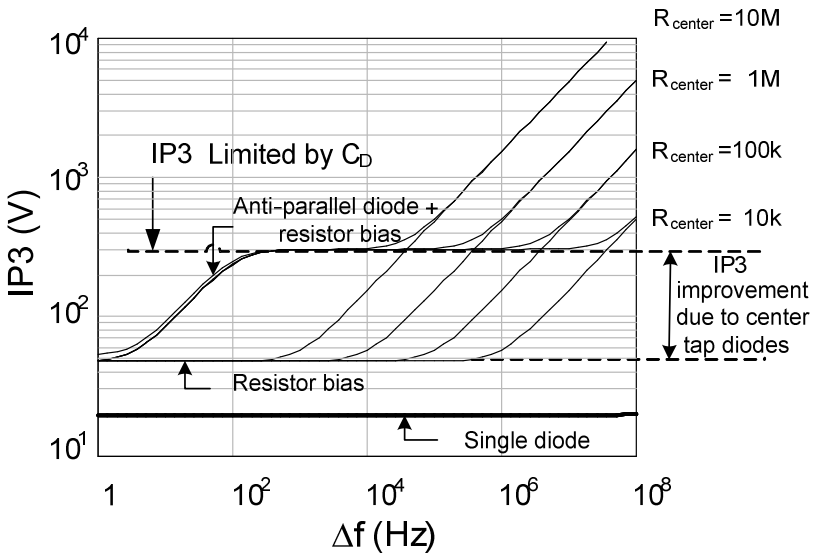


Figure 4.4: Simulated $IIP3(V)$ for a single varactor and an anti-series varactor pair as a function of tone spacing and center tap impedance (f_c=1 GHz, C_{eq}=10 pF, V_C =5 V, n=0.5, C_D=0.1 pF).

In the regime of ultra-low tone spacing, where (4.29) cannot be satisfied, the modest $IIP3$ improvement over a single diode can be almost entirely explained by the twofold reduction in the RF voltage across each diode.

In Fig. 4.4 we observe that the DFVS performs much better than the single varactor in terms of linearity; however, the best results are obtained when the cut-off frequency of the dc bias network is much lower than the difference frequency. In addition, to maintain good linearity, the varactor diodes should neither become forward biased (much), nor exceed the diode voltage-breakdown conditions during the RF signal cycle.

4.2.4 Varactor technology considerations

By improving the linearity of varactors, they now qualify for 'linear' applications in wireless communication systems. However, varactors for integrated impedance matching tuners, for example, are subject to many design constraints. This is due to the harsh signal conditions that occur with high impedance transformation ratios. These high ratios often translate into high Q conditions (not to be confused with high Q-factor), which are accompanied by high RF voltages and currents. These conditions require ultra-low loss, as well as high breakdown voltage of the network elements.

Therefore in practical RF applications of the varactor stack, high RF voltage swings can arise over the reverse biased diodes, which will affect their useful operation. E.g., if the RF voltage swing becomes so high that forward biasing of one of the diodes

occurs, the IM3 cancellation in the varactor stack will be violated, yielding high distortion. Consequently, the varactor diodes should never become forward biased nor exceed the diode voltage breakdown (V_{break}) conditions, which can trigger device failure, during the RF signal cycle. Since the RF voltage amplitude limits the 'safe' linear operation region of the varactors, also the effective tuning ratio of the varactor capacitance (c_{ratio}) will be reduced when tuning 'high power' RF applications. This restriction of the tuning range can be denoted as

$$c_{ratio} = \frac{C(V_{cont\_min})}{C(V_{cont\_max})}. \tag{4.33}$$

With $C(V)$ given by (4.2) and the control voltages limited by the RF signal, namely $V_{cont\_min} = V_{RF}/2$ and $V_{cont\_max} = V_{break} - V_{RF}/2$, where V_{RF} is the voltage amplitude of the applied RF signal over the varactor stack. In these considerations, for reasons of simplicity, it is assumed that the RF voltage is divided equally between the two diodes. These considerations demonstrate that the effective tuning range can be improved by increasing the breakdown voltage of the diodes, by lowering the doping concentration of the epilayer and increasing its thickness. However, this approach will result in a higher series resistance - and lower Q - and the need for higher control voltages. Since both effects are undesired, it is important to limit the RF voltage swing per device. To assess the influence of the RF voltage amplitude, Fig. 3.2 and 4.5. show the calculated breakdown voltage, zero bias Q-factor and the effective capacitance ratio for different RF voltage amplitudes as function of doping. From this graph it can be seen that a doping level of 3.10^{16}cm^{-3} gives a good compromise between tuning range, varactor quality factor (Q>100 at 2 GHz) and breakdown voltage ($\sim$25 V). These same considerations are also valid for the HTRVS, with the added constraint, that, due to the size difference between the varactors, the larger part of the RF voltage will be over the smaller device, leading to a reduced control voltage headroom compared to the DFVS.

Improving the power handling by (multi) stacking

When considering the anti-series connection of two identical (uniformly doped) varactor diodes under low RF power and reverse biased operation, the applied RF voltage will split almost equally over the individual diodes. However, at high power levels, the diode capacitances will be modulated by the RF signal, and the voltage distribution between the two will not be exactly equal. In practice, this is not a problem, since the largest RF voltage will be across the smallest capacitance, which is offered by the most strongly reverse biased diode. With the above consideration in mind, it is clear that the voltage handling capabilities of the varactor stack can be improved by stacking multiple anti-series varactor diode pairs, Fig. 4.6. The major penalty for this approach is a larger device area for a given capacitance (roughly four times the area for each doubling of the number of varactor diodes). The use of multi-DFVS configurations affects the effective capacitance tuning ratio, i.e. the difference between the minimum and maximum capacitance for a given RF level without forward biasing or exceeding breakdown. The improvement in tuning range of these multiple varactor stacks for higher applied RF voltages is illustrated in Fig. 4.7.

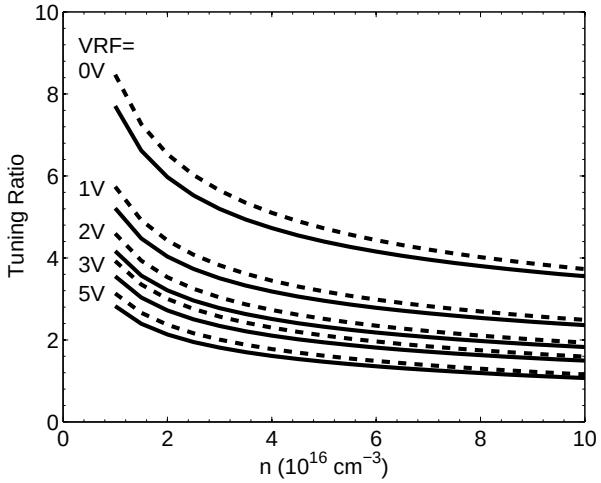


Figure 4.5: Effective single varactor diode capacitance tuning ratio (c_{ratio} for silicon (solid lines) and GaAs (dashed lines) based varactor diodes at different RF voltage amplitudes as function of doping.

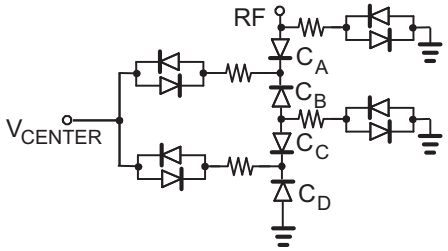


Figure 4.6: Multi-varactor stacks in series to lower the RF voltage per diode and consequently improve the voltage handling and tuning range capabilities.

In this figure the RF voltage represents the applied voltage to the whole varactor stack. Note, that GaAs varactors have an advantage over silicon in terms of Q due to the higher mobility, and provide limited improvement in tuning range over silicon for a given uniform doping concentration. The control voltage of these multi-varactor stacks is constrained by the breakdown voltage of a single varactor and in these cases limited for silicon to ∼20V (GaAs: ∼25V) and ∼30V (GaAs: ∼40V) for $N_d = 4.10^{16}$ and $N_d = 2.10^{16}$, respectively.

The reduced voltage swing per diode in this multi-stacked configuration is directly beneficial to the linearity. This is illustrated in Fig. 4.8. where the $IIP3V$ is given for a single diode, a DFVS, a multi-DFVS configuration with four anti-series diodes and a multi-DFVS configuration, featuring eight anti-series diodes. Fig. 4.8 shows the exact doubling of the IIP3V, at very low tone spacing, for each halving of the RF voltage per diode, when utilizing multi-DFVS configurations. Also the requirement on the

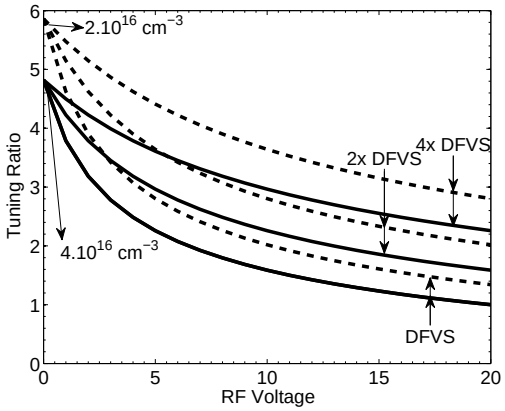


Figure 4.7: Calculated maximum effective capacitance tuning ratio for the uniformly doped multi-stacked DFVS configuration, featuring two, four and eight anti-series diodes, ($N_d = 2.10^{16}$ and $N_d = 4.10^{16}$) as function of applied RF voltage.

high center-tap impedance for a lower tone-spacing is somewhat relaxed, since this impedance is kept constant, while the capacitance doubles to keep the same effective capacitance.

In this section no forward biasing of the varactors diodes was allowed due to linearity considerations. In practice, however, small excursions into the forward bias region might be permitted, as long as the related dc current and its associated diffusion capacitance are small and their effective impedances (V_t/I and $2V_t/j\omega I\tau$ where τ is the carrier lifetime) remain significantly larger than the impedance offered by the depletion capacitance.

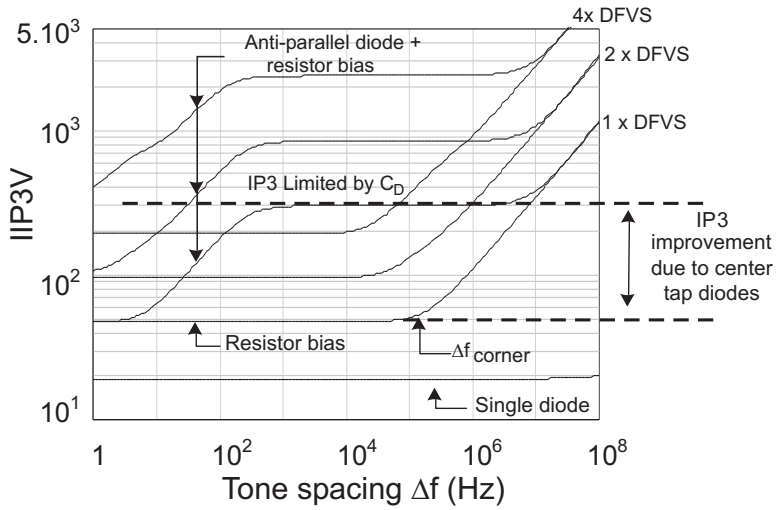


Figure 4.8: Simulated IIP3V single varactor and (multi)-DFVS configurations, featuring two, four and eight anti-series diodes, using a two-tone test as function of the tone spacing ($f_c = 1$ GHz, $C_{eq} = 10$ pF, $V_{center} = 5$ V, $n = 0.5$, $C_D = 0.1$ pF, $\phi = 1V$, $R_{center} = 100$ kΩ).

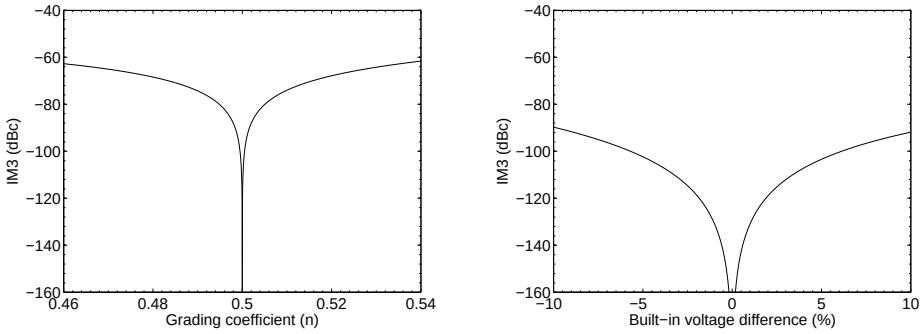
4.3 The impact of process variations on device linearity

When implementing the theoretical concepts of the previous sections as linearized practical devices, some deviations from the ideal assumptions due to process variations may exist. To quantify these effects, small excursions from the ideal situation are considered and simulated.

4.3.1 Device matching

Small differences between devices may influence the distortion cancellation in these varactor topologies. For example the junctions may not be exactly identical, which influences ϕ. Furthermore differences in the doping profile will show up in C_{j0} and n. Differences in size will result in non ideal canceling of the distortion products and related harmonic components. Therefore the impact of each of these deviations on the distortion components is considered. For these simulation based experiments the varactor stack is assumed to be a shunt element in a 50 Ω environment.

In Fig. 4.9(a) the simulated linearity as function of grading coefficient n is given. Clearly a grading coefficient of $n = 0.5$ results in ideal distortion cancellation. However, small deviations from this ideal point still result in reasonable linearity performance. In similar fashion from Fig. 4.9(b) can be concluded that a 10% deviation in ϕ would translate in a $IM3$ performance of -90 dBc, which, at this power level, is equivalent to an $IP3$ of 72 dBm. The accuracy of the size difference between the



(a) (b)

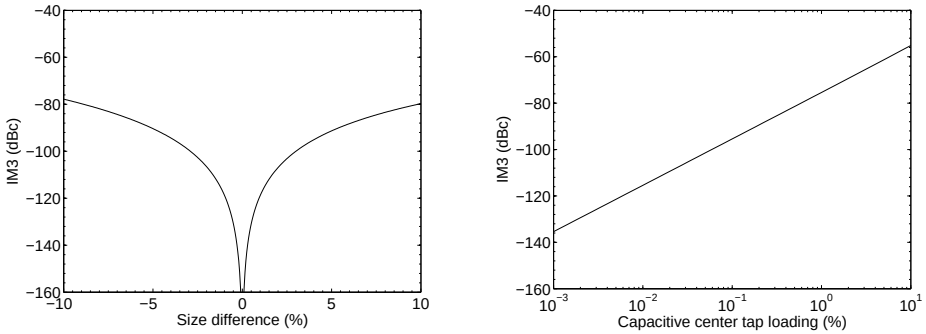
Figure 4.9: (a) Simulated $IM3$ of a DFVS as function of grading coefficient n. (b) Simulated $IM3$ of a DFVS as function of built-in voltage difference between the diodes ($f_c = 1$ GHz, $\Delta f = 1$ MHz, $C_{eq} = 10$ pF, P_{avs}=30 dBm, $V_{center} = 5$ V, $n = 0.5$, $\phi = 1V$, R_{center} = ideal (∞ for RF, zero for DC)).

two devices is given in Fig. 4.10(a) from which can be concluded that a 5% difference is allowed for the same $IP3$ of 72 dBm, which is easy to realize using modern lithography.

4.3.2 The influence of parasitic loading of the center tap node

Furthermore, as discussed in Section 4.2.3, the impedance of the center-tap for the DFVS and HTRVS should be high; however, in practical realizations this node will be to some extend capacitively loaded by the substrate.

Fig. 4.10(b) shows the importance of keeping the loading of the centertap minimized. Already a 0.2% center tap loading results in the same $IP3$ of 72 dBm. An issue that will be addressed with a suitable technology solution in the following chapter.



(a) (b)

Figure 4.10: (a) Simulated $IM3$ of a DFVS as function of size difference, (b) Simulated $IM3$ of a DFVS as function of capacitive loading of center-tap, where the percentage is the parasitic capacitance as fraction of the single diode zero bias capacitance value. ($f_c = 1$ GHz, $\Delta f = 1$ MHz, $C_{eq} = 10$ pF, $V_{center} = 5$ V, P_{avs}=30 dBm, $n = 0.5$, $\phi = 1V$, R_{center} = ideal (∞ for RF, zero for DC)).

4.4 Conclusion

In this chapter it has been theoretically demonstrated that it is possible to make perfectly linear capacitive tunable elements that do not introduce any signal distortion. The use of specific doping profiles in certain circuit topologies, anti-series or anti-series and anti-parallel, provide these remarkable properties. For optimal linear operation it is necessary to take proper care of the center-tap biasing. If even better linearity performance is required multiple devices can be stacked, which also improves the power handling capabilities. Furthermore, these solutions are not too sensitive to process variation, therefore practical implementations are truly feasible as will be demonstrated in the following chapters.

Chapter 5

High performance varactor realization in silicon-on-glass technology[1]

5.1 Introduction

From the previous chapters it can be concluded that the critical points for the devices used in the low distortion varactor configurations are loss, linearity and electrical isolation. To reduce the losses, the buried layer (Section 3.3) should be avoided. To reach the linearity potential of the DFVS, the doping profile needs to be exactly controlled. To avoid the need for complicated doping profiles, the ideal one-dimensional behavior of the device should be approached as good as possible. And, finally, an electrically isolating substrate keeps the loading of the center-tap within limits (Section 4.2). To demonstrate the feasibility of these low distortion varactor topologies, a technology that addresses all these concerns will be introduced in this chapter.

The starting point for this technology is substrate transfer, which is gaining interest as enabling technology for the realization of high-performance RF integrated circuits which feature on-chip high quality passive RF components [82–84]. These technologies, such as the in-house DIMES-TUDelft Silicon-on-Glass process with front and backside wafer patterning [85], are particularly attractive since they can offer enhanced performance for the semiconductor devices. In the DIMES process strategy, the semiconductor device regions below the surface can be contacted directly from the backwafer, thus eliminating the need for buried layers with their associated RC parasitics, which are normally reduced through the use of finger structures for the active devices. Using backwafer contacting, eliminating the use of finger structures, not only

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the resistance can be reduced, but also the devices can be made more area efficient, while their C-V relation can be more accurately controlled. These measures provide close to ideal 'intrinsic' device performance, which opens the door to circuit design concepts that are simple, low-loss and fully benefit from the previously introduced distortion cancellation strategies. Although the basic device design concept [86], i.e. an epitaxial varactor in combination with bulk etching of the wafer, is not new, the essential technology needed for realizing high quality integration has only recently become available.

To support the reader with detailed information on the developed novel varactor technology, this chapter provides a description of the technology steps, which yields the low-loss high-linearity devices. For this purpose, the Silicon-on-Glass substrate transfer process is given, together with the additional measures that yield the ultra-low-loss operation, e.g. the use of thick metals with high conductivity (copper plating). Excimer laser annealing is used to establish the low-contact resistance, and special Boron layers are added to reduce the leakage of the diodes. The high linearity operation of the varactor diodes is based on the use of the varactor circuit topologies of Chapter 4 in combination with specific implanted/epitaxially grown doping profiles that may only minimally be affected during the subsequent (low temperature) processing.

5.2 Silicon-on-Glass substrate transfer technology

The varactor implementations are based on a modified version of the Silicon-on-Glass substrate-transfer technology, which has been originally developed for improved RF performance for silicon integrated circuits [87]. It has been further enhanced by introducing backwafer contacting [85, 88]. While metal transmission lines can be placed on the low-loss glass substrate, the resistive and capacitive parasitics of the silicon devices can also be minimized by direct contacting of the device omitting the need of buried layers.

5.2.1 Silicon-on-Glass varactor process flow

The basic varactor process flow is shown schematically in Fig. 5.1. The starting material is 100 mm silicon-on-insulator (SOI) SOITEC wafers with 0.34 μm intrinsic silicon on 0.4 μm buried oxide (BOX), on which any additional layers needed for the specific device fabrication are grown epitaxially of As-doped silicon. For thin layers, below 0.5 μm a thin silicon layer is grown epitaxially on the intrinsic silicon, followed by multiple implants to obtain the desired doping profile. After this step various (guard-ring) implants can be applied. Then, to dimension and isolate the various diodes and resistors, islands are defined by two or three shallow trench plasma etch steps, depending on the total top silicon-layer thickness. The steps in height are no larger than 0.5 μm so that a relatively thin metallization layer can be used on the front-wafer, such that sufficient step coverage can be achieved, but now without the high stress associated with thick deposited layers. Note, that such stress can lead to damage of the silicon due to stress relief at the trench edges, which can result in

significant diode leakage. Since high valued resistors are needed to implement the biasing network of the diodes (Section 4.2), the trench etching is also used to remove most of the doped silicon where the resistors are patterned.

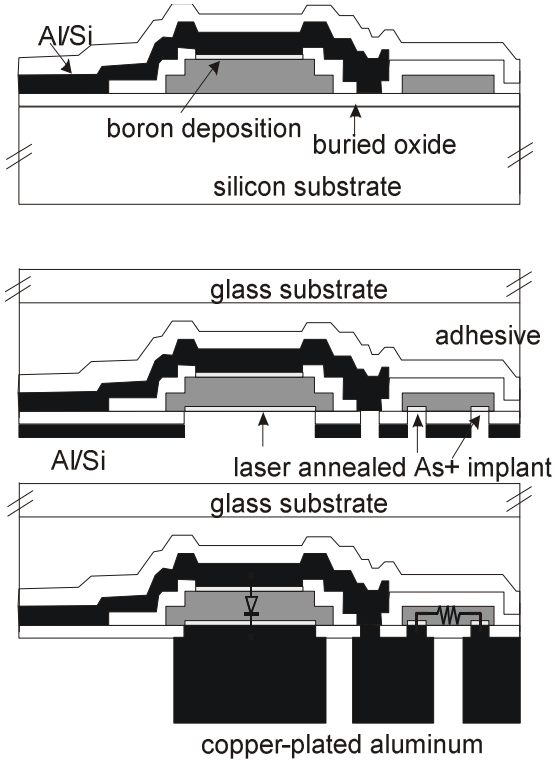


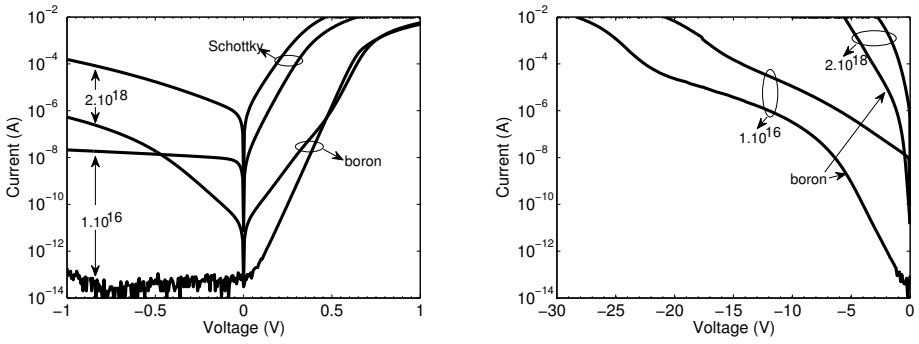
Figure 5.1: Schematic of the process flow for the integration of Silicon-on-Glass varactor diodes and high-ohmic resistors.

After defining the device islands a 30 nm 850 °C thermal oxide is grown. Then a 600 nm LPCVD TEOS at 700 °C is deposited, followed by an anisotropic plasma etch of 0.2 μm to planarize the structure. After this step the contact windows that define the actual diodes are plasma etched. The windows are placed so that the lateral extension of the depletion region will not reach the trenches. Then a 2.5 minute 700 °C boron layer is epitaxially deposited [89] after an 800 °C 3 minute backoff to remove the native oxide. This deposition is directly followed by metallization with 0.675 μm Al/Si(1%). A second set of contact windows is opened by plasma etching, directly followed by a dip-etch in HF, followed by metallization with 1.075 μm Al/Si(1%) to form Schottky diodes. The metal is anodized to form Aluminum oxide to implement MIM capacitors. The capacitors are defined by plasma etching, followed by patterning the Al/Si(1%) first metal layer. A 1.4 μm plasma oxide is deposited followed by 0.2 μm anisotropic plasma etch to planarize. Contact openings are defined to contact the first to the second metal layer. Followed by metallization of the second front metal,

3 μm thick Al/Si(1%). The second metal is patterned, covered with 1 μm PECVD oxide and substrate transfer to glass is performed by gluing, after which only thermal processing temperatures below 300 °C are permitted. The silicon substrate is removed by TMAH etching selectively to the BOX. An Al/Si(1%) layer is sputtered on the back-wafer to serve as a reflective mask for laser annealing that is used for dopant activation instead of thermal processing. The back-wafer contact windows are then etched through the Al/Si(1%) and BOX. To contact directly to the desired doping profile without any of the starting intrinsic silicon between the contact and doped region, extra silicon up to 500 nm is also removed. The contacts are implanted with 5 keV, 2×10^{15} cm^{-2} As^{+} and laser annealed with an energy of 900 mJ/cm^2. Next, the contact windows to the front-wafer are etched and a 1.4 μm Al/Si(1%) is sputtered and patterned on the back-wafer. Electro-plating of 4 μm copper on the Al/Si(1%) and 10 nm gold as top-contact layer to facilitate bonding, completes the process.

5.3 Realization of Silicon-on-Glass varactor diodes

Electrical qualification results of the realized silicon devices, processed according to the flowchart in the previous section, are presented here. These results include the basic varactor diode functionality, i.e. current-voltage, capacitance-voltage and losses (Q-factor).



(a) (b)

Figure 5.2: (a) Measured I-V characteristics and (b) reverse I-V characteristics of diodes with and without B-deposition for a uniform n-doping of 10^{16} or 2.10^{18} cm^{-3}. The diode area is 17240 μm^2.

5.3.1 Varactor diode current-voltage characteristics

Several devices with different characteristics were fabricated. The I-V characteristics of diodes with and without boron deposition (B-deposition) are compared in Fig. 5.2 for a very high (2.10^{18} cm^{-3}) and very low (10^{16} cm^{-3}) uniform doping. The boron layer acts as a combination of a highly boron-doped silicon at the boron silicon interface [89] and as metallic boron on top of this layer that reduces the current by 3-6

decades [2]. In addition, this increases the series resistance that attenuates the current at high forward biasing due to the resistance of the metallic boron. In the present circuit applications this will reduce the Q-factor to some extend. However, the reduction of the reverse current leakage as shown in Fig. 5.2(b) is of great importance. It increases the breakdown voltage and thus the potential dynamic range of the adaptive circuits. The results presented in Fig. 5.2(a) and (b) suffer from an increased current

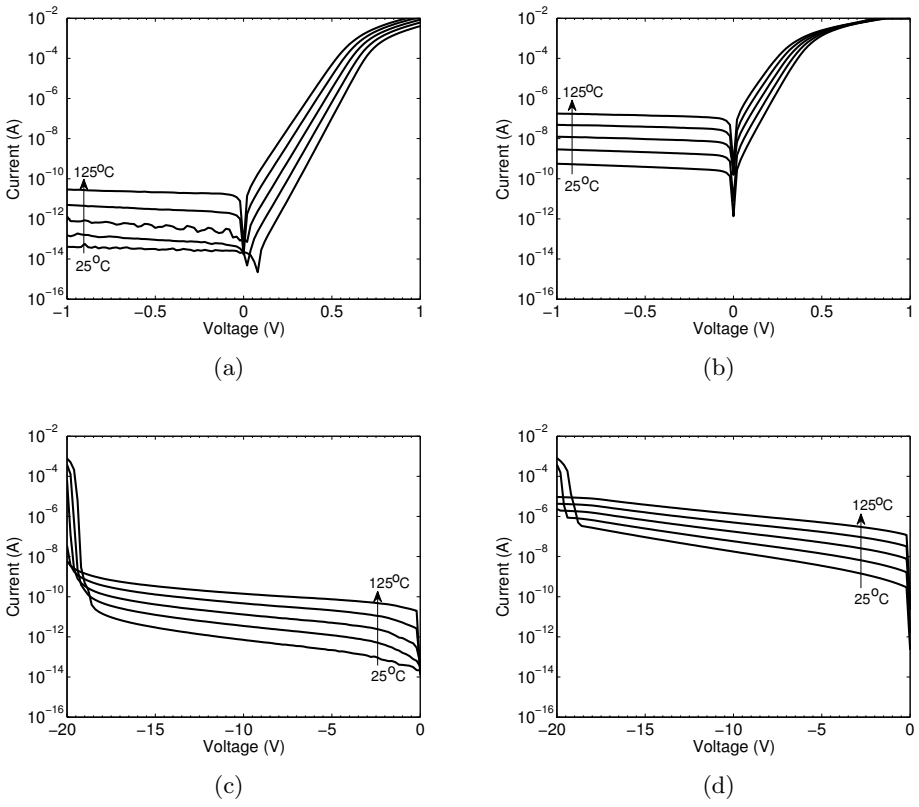


Figure 5.3: Measured I-V characteristics and reverse I-V characteristics at temperatures from 25^{o}C to 125^{o}C of diodes with B-deposition (a, c) and Schottky diodes without B-deposition (b, d) for a uniform n-doping of 4.10^{16} cm^{-3} with guard ring. The area is 4304 μm^2.

at reverse voltage before reaching breakdown. This is mainly due to the fact that the electric field over the depletion layer at the periphery of the contact opening can be significantly higher than in the rest of the device. This arises if the depletion layer in lateral direction is smaller than in the perpendicular direction. However, over them

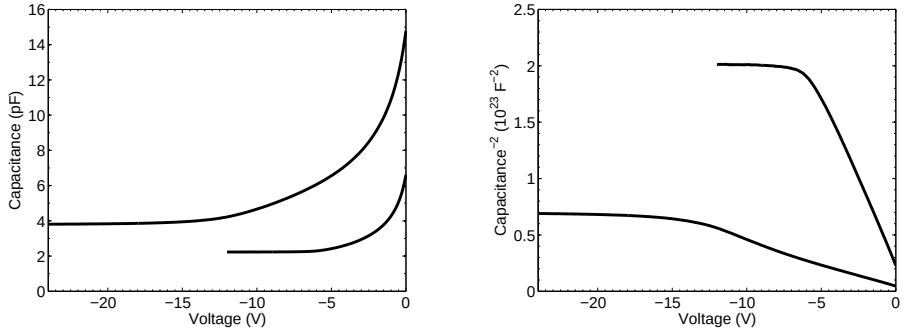
[2]Basically the boron deposition forms a very highly doped, shallow pn junction (a few nm) with extra suppression of the minority carrier injection from the n-layer. For more information the reader is referred to the work of Sarubbi [89].

the same voltage is present. To reduce this increase in electric field, implants along the periphery of the contact opening can be applied, namely the so-called 'guard ring' implants. Fig. 5.3 shows I-V characteristics at various temperatures of devices with a doping of 4.10^{16} cm^{-3} where a 1 μm wide guard ring (5 keV 10^{15} cm^{-2}, BF_2^+ implant) has been implemented. The measurement results clearly demonstrate the reduction of reverse leakage current, compared to Fig. 5.2(b), in this case almost up to the theoretical breakdown voltage of 19 V.

5.3.2 Varactor diode RF characteristics

Varactor diode capacitance-voltage characteristics

Since the Silicon-on-Glass varactor diodes are very large and laterally uniform, their C-V characteristics are in first approximation mostly determined by the one-dimensional vertical doping profile. The C-V characteristics were extracted from S-parameter measurements at 2 GHz, which, compared to the conventional low frequency (1 MHz) C-V measurements, increases the applicable biasing. The series inductance was calculated from the 50 MHz zero bias capacitance and the resonance frequency and deembedded. The plot of C^{-2} versus biasing voltage gives an indication of the 'abruptness' of the corresponding doping profile; a linear relationship corresponds to an ideal abrupt junction. As can be seen in Fig. 5.4, there is a strong deviation from this ideal situation at high reverse biasing for both types of diodes. The strong deviation corresponds to a significant increase in diode leakage, which leads to a significant voltage drop over the integrated bias resistor. This voltage drop tends to dominate the C-V measurement rather than the voltage dependency of the actual depletion capacitance. However, at low voltages the higher doped device (10^{17} cm^{-3}) is nearly ideal abrupt $n = 0.5$, whereas the lower doped device (4.10^{16} cm^{-3}) has a doping profile corresponding to $n \approx 0.55$.

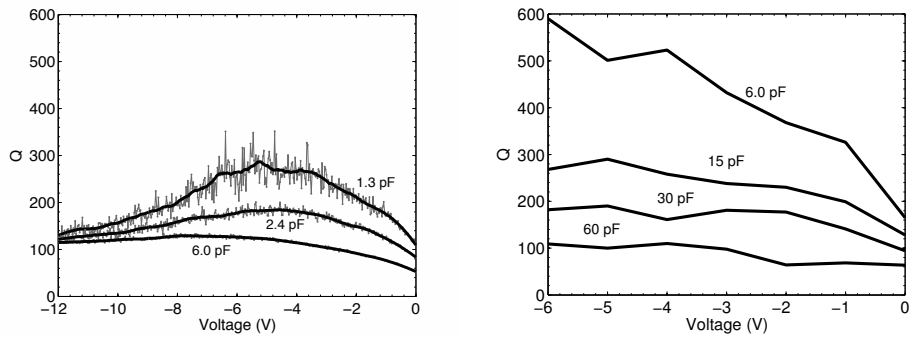


(a) (b)

Figure 5.4: (a) Measured C-V characteristics and (b) corresponding C^{-2} characteristics of diodes with B-deposition for a uniform n-doping of 4.10^{16} cm^{-3} and 10^{17} cm^{-3}.

Varactor diode Q-factors

The Q factor is calculated from S-parameter measurements. The resistances determining the Q factor can be divided in several parts: the metal resistance, the n^+ contact resistance and the non-depleted, low-doped n-region resistance. The resistivity of the metal layers is kept low by the copper-plating of the back-wafer aluminum while the laser annealing provides low contact resistance. The intrinsic resistance of the n-region can, however, be high and lowering it gives a trade-off with the breakdown voltage as discussed in Section 3.3. The resulting Q factors at 2 GHz for the lightly-doped diodes in DFVS configuration range from 40 (0 V) till 250(- 15 V) for a 17.5 pF device (Fig. 5.5(c) and for the more heavily-doped diodes from 150 (0 V) till 600(-6 V) for a 6.0 pF device as shown in Fig. 5.5(b). For a higher capacitance device of 60 pF a Q >60 was obtained. When comparing the 6.0 pF device with and without copper plating, one can conclude the copper plating keeps the resistivity of the metal layers low.



(a) 10^{17} cm^{-3}

(b) 10^{17} cm^{-3} with copper plating

(c) 4.10^{16} cm^{-3} with copper plating

Figure 5.5: Measured Q at 2 GHz versus bias voltage for various device sizes of Silicon-on-Glass varactor diodes in DFVS configuration, without (a) and with (b, c) copper plating (10^{17} cm^{-3} (a, b) and 4.10^{16} cm^{-3} (c)). Note the voltage scales are different, e.g. the region where the diode reverse current is reducing the Q has been omitted for the 10^{17} cm^{-3} copper plated varactors.

Process characterization

In the Q measurements a clear dependence of the laser anneal energy was detected as shown in Fig. 5.6. The Q increases with laser energy, a behavior that can have two origins. Firstly, below an energy of 700 mJ/cm^2 the melt is not complete and the contact resistance can be a few factors higher. Secondly, the presence of interstitials from the contact implantation will increase the resistivity of the n-doped region near the contact. These interstitials can be found at a large distance from the end-of-range damage region that for 5 keV As^+ implants is no more than a few tens of nanometers deep and is almost entirely annealed during the laser melting of the silicon surface [90]. As a result of the laser anneal a micro-second short heat pulse is sent into the silicon. The higher the laser energy, the longer the heat pulse and the more probable that interstitials will be annealed. These interstitials were also identified in other Silicon-on-Glass processes using similar implanted laser annealed contacts [91,92]. To reduce the effect of these interstitials the implant can be performed under a larger angle, this has been investigated in [93]. As a result an angle of 60 degrees is currently used, whereas the implantation angle in the experiment as presented in Fig. 5.6 was seven degrees.

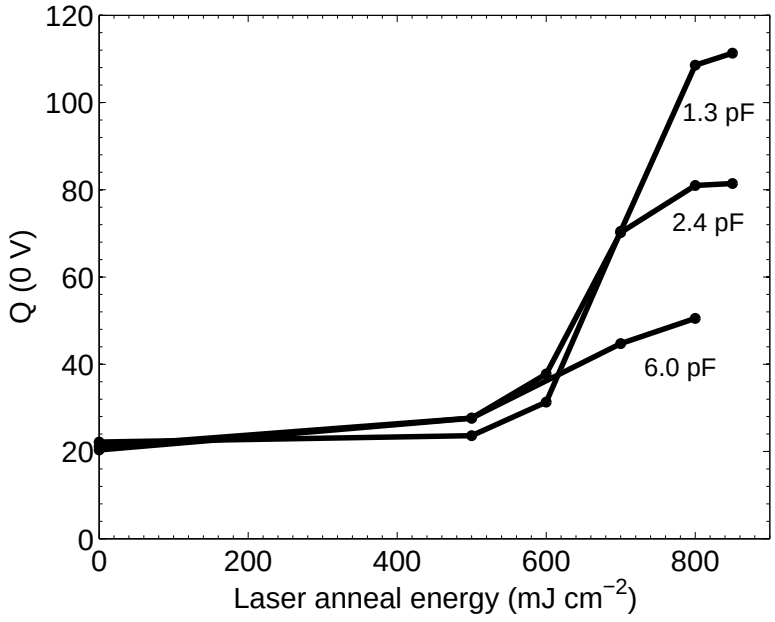


Figure 5.6: Zero bias quality factor at 2 GHz versus laser anneal energy.

5.4 Conclusion

A high performance varactor technology has been developed, which benefits from the advantages of substrate transfer technologies. This Silicon-on-Glass process has been demonstrated to be very suitable for implementing low-loss varactors in low distortion configurations. In particular, Fig. 5.7 shows that the series resistance has been strongly reduced for the Silicon-on-Glass varactors compared to other published results. However, the contact resistance and/or intrinsic resistance remains to be the limiting factor for further improvement of the Q-factor for small mm-wave devices. Something that suggests the investigation of the use of high mobility (III-V) or wide bandgap materials in combination with two-sided processing in order to create even higher performance devices. The electrical isolation properties will be demonstrated by the large signal results as presented in the next chapter.

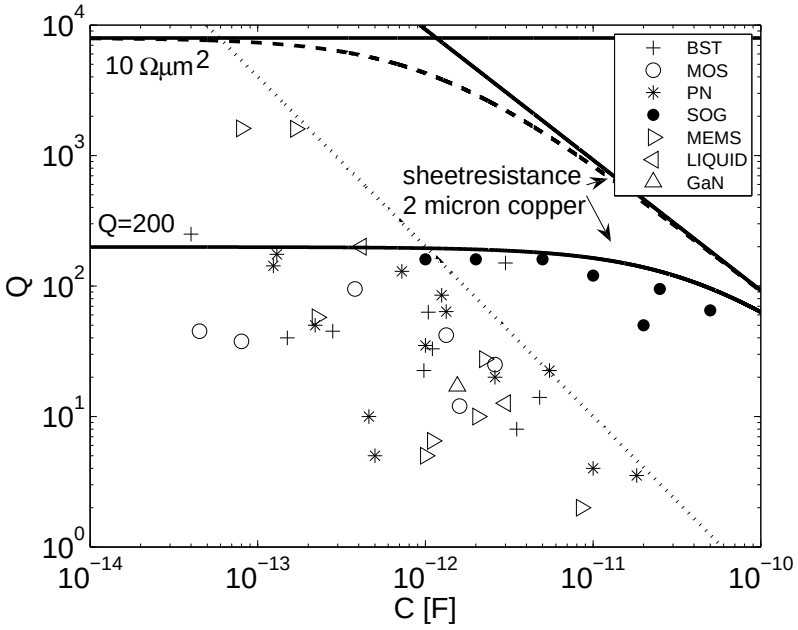


Figure 5.7: Reproduction of Fig. 3.4 including the Silicon-on-Glass measurement results. Normalized Quality factor (Q) at 2 GHz versus capacitance for different technologies, the solid line marked $Q = 200$ indicates the trend for Silicon-on-Glass pn junction varactors [83, 84] with an intrinsic Q of 200 and a sheetresistance of 2 μm copper.

Chapter 6

High performance varactors characterization and modeling[1]

6.1 Introduction

The Silicon-on-Glass varactor technology, as developed in the preceding chapter, is now applied to the low-distortion varactor topologies. To verify the low distortion properties large-signal characterization results will be presented and compared to simulations. In view of the thermal isolation properties of the chosen substrate, a thermal characterization will be described and presented to study the RF power constraints of the varactors in large-signal operation. Finally, a direct model calculation method will be shown.

6.2 Large signal characterization

6.2.1 Distortion-free varactor stack characterization

In order to test the distortion-free operation, a two-tone test (f_c=2.14 GHz) was performed on a single varactor and a DFVS (Fig. 6.1) using a 50 Ω terminated two-port configuration. For the calibrated power measurement of all frequency components of interest, the system of [25] is used. Fig. 6.2 plots the measured and simulated $IM3$ and $IM5$ components as function of power for different tone-spacing (Δf=100

[1]Parts of this chapter were published by: K. Buisman, L. C. N. de Vreede, L. E. Larson, M. Spirito, A. Akhnoukh, T. L. M. Scholtes and L. K. Nanver, "Distortion-free varactor diode topologies for RF adaptivity," in Microwave Symposium Digest, 2005 IEEE MTT-S. And by: K. Buisman, C. Huang, A. Akhnoukh, M. Marchetti, L. C. N. de Vreede, L. E. Larson and L. K. Nanver, "Varactor Topologies for RF adaptivity with improved power handling and linearity," in Microwave Symposium Digest, 2007 IEEE MTT-S.

kHz and Δf=10 MHz) using a center-tap impedance of 47 kΩ and a center-tap bias of 2 V. These results match the theory presented earlier in Section 4.2.2 very well. There is a substantial improvement in linearity using the DFVS configuration over a single-varactor diode. Note, that due to the fact that the RF voltage is split over the diodes of the DFVS, the forward drive conditions occur at a 6 dB higher power level for this configuration. The better suppression of the $IM3$ and $IM5$ products at the higher tone spacing is also clearly visible, supporting the theory introduced previously.

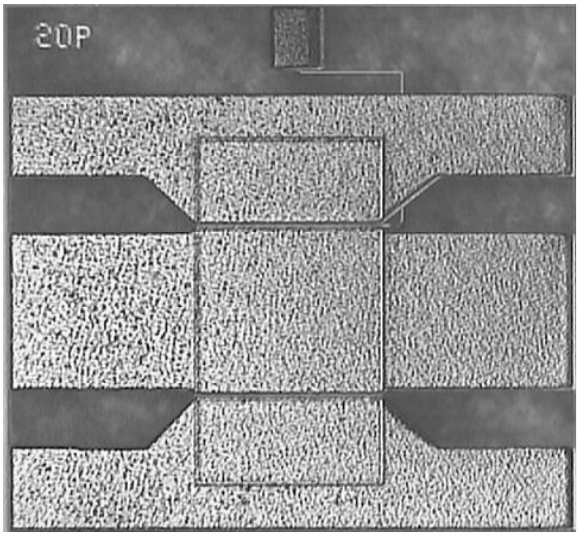


Figure 6.1: Microphotograph of a 20 pF DFVS as used in the two-tone characterization.

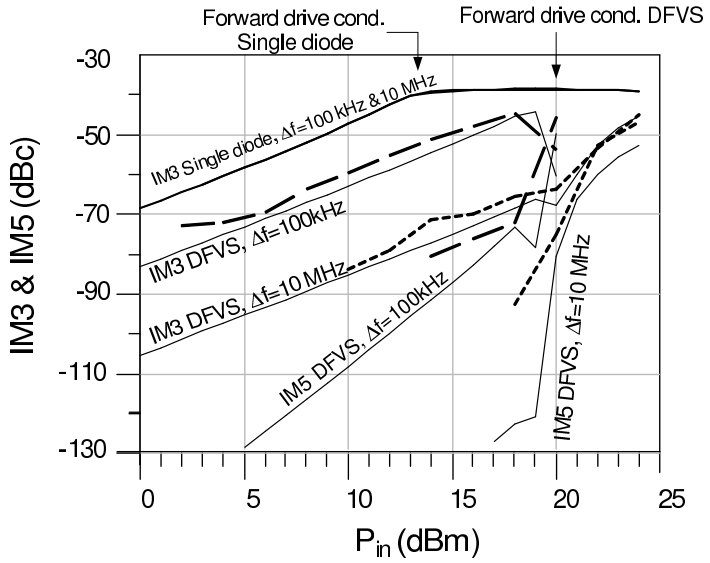


Figure 6.2: Measured (dashed lines) and simulated (solid lines) $IM3$ and $IM5$ for a single varactor and a 20 pF DFVS as function of power using; $V_{cont} = 2$ V, $f_c = 2.14$ GHz, for tone-spacings of Δf=100 kHz and 10 MHz.

6.2.2 Single vs multi-stack linearity characterization

As shown in Section 4.2, stacking multiple varactors in series can improve the power handling and the linearity of the varactor stack. To test this theory, both DFVS as well as double-stacked DFVS structures with integrated biasing networks and optional MIM decoupling capacitor have been realized in the Silicon-on-Glass technology using an uniform doping of 4.10^{16} cm^{-3}. The devices are flip-chip compatible with their footprints given in Fig. 6.3. The related Q factors at 2 GHz of a ∼20 pF DFVS and 2xDFVS (effective capacitance also ∼20 pF) configuration with and without MIM capacitor are presented in Fig. 6.4. Note, that these are scaled versions of the ones given in Fig. 6.3. The footprints of these experimental structures can be reduced by simplifying the layout of the integrated bias network.

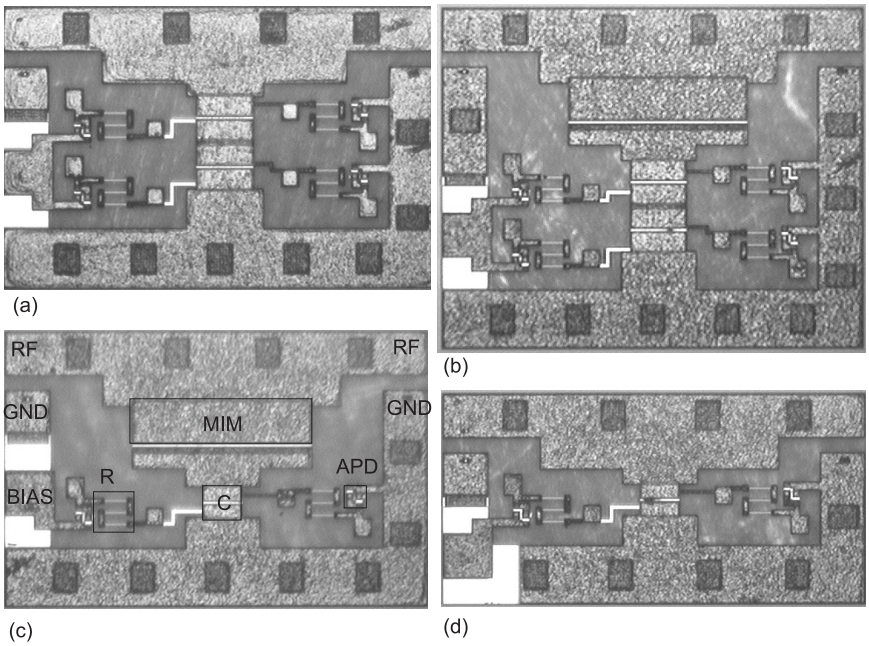


Figure 6.3: Microphotographs of the 2.3 pF varactor stacks used in the linearity measurements (a) 2xDFVS - 1424 μm x 952 μm - (b) 2xDFVS with MIM capacitor - 1424 μm x 1176 μm - (c) DFVS with MIM capacitor - 1424 μm x 952 μm - and (d) DFVS - 1424 μm x 728 μm. (Dimensions are outer edge of photographs.)

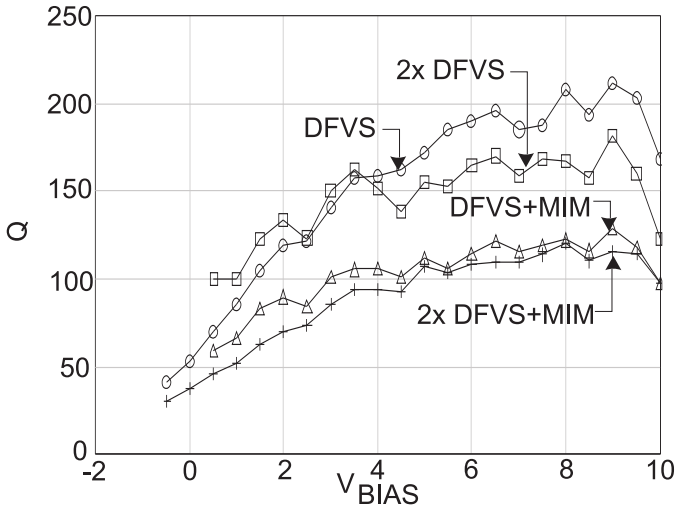


Figure 6.4: Measured deembedded quality factor at 2 GHz of ∼20 pF flip-chip compatible DFVS and 2xDFVS devices with and without MIM capacitor versus bias voltage.

In order to test the narrow tone spacing linearity, a two-tone test (f_c = 2.14 GHz) was performed on a DFVS and a multi-varactor stack (2xDFVS) using 50 Ω two-port test conditions. Fig. 6.5 shows the measured $IM3$ components for a DFVS with 80 kΩ center tap impedance, a DFVS with anti-parallel diodes in the center tap and a double stacked DFVS configuration with anti-parallel diodes for biasing. The devices have been measured as a function of power for a tone spacing of 100 kHz. Note the dramatic linearity improvements when introducing the anti-parallel diode configuration as well the double stacking of the DFVS. In Fig. 6.5(b) the power level required to reach an $IM3$ level of -60 dBc is indicated as a function of bias. Clearly, for low tone spacings an improvement can also be seen for increased reverse bias, as implied by the theory. Furthermore the multi-DFVS can withstand higher power levels (∼6dB more) for a given distortion level and biasing.

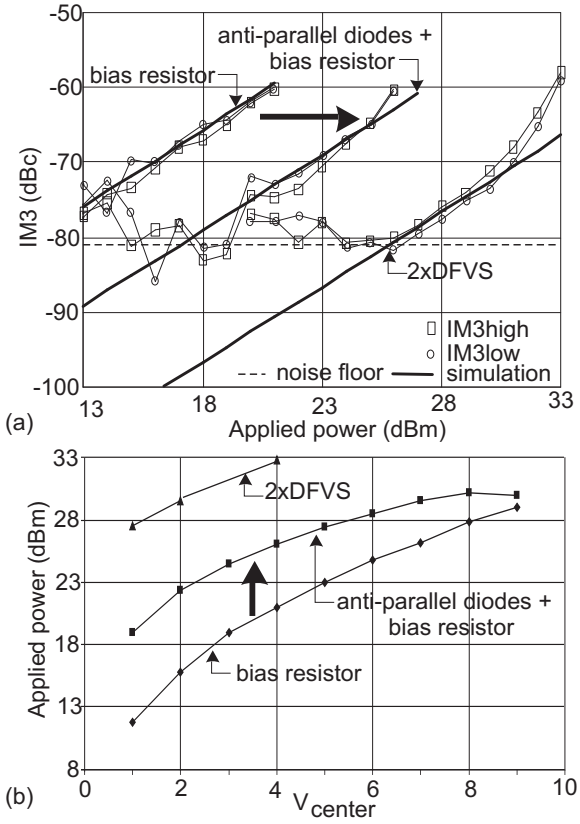


Figure 6.5: Narrow tone spacing linearity testing (f_c=2.14 GHz, Δf=100 kHz) of DFVS configurations with a purely resistive centertap (R_{center}=80 kΩ), a center tap connection with resistor and antiparallel diodes, and 2xDFVS with resistor and anti-parallel diodes. (a) Measured and simulated $IM3$ as function of power (V_{center} = 4 V). (b) Measured contours of applied power, resulting in -60 dBc $IM3$ as function of V_{center}.

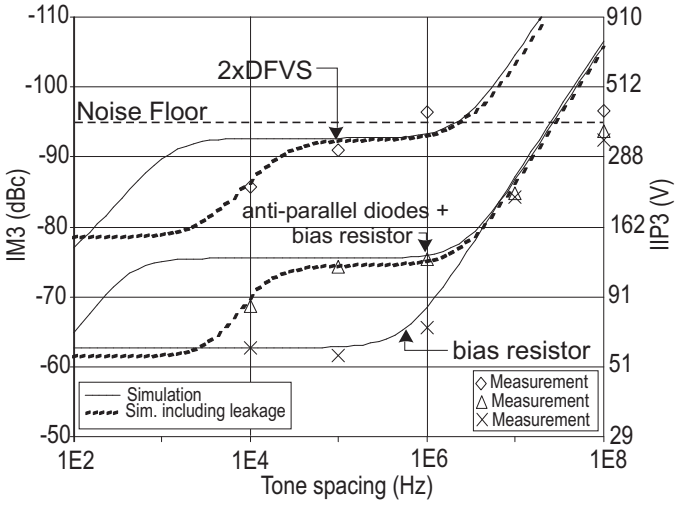


Figure 6.6: Simulated (lines) and measured (markers) $IM3$ and $IIP3$ for a DFVS with and without anti-parallel diodes and a double 2.3 pF DFVS with resistor and anti-parallel diodes as function of tone-spacing Δf; V_{center}=5 V, f_c=2.14 GHz, applied power: 21 dBm.

Fig. 6.6 plots the measured and simulated $IM3$ components as function of tone-spacing at a power level of 21 dBm. The multi-stack clearly offers a superior performance over the DFVS and the results match the theory quite well. Note, that the presence of leakage currents will determine the lower boundary of the linearity improvement for narrow tone-spacing by the anti-parallel diode configuration. As predicted by theory, for larger tone-spacings, the linearity further improves and cannot be measured anymore by the available equipment.

6.3 Thermal characterization

6.3.1 Introduction

The introduction of varactor diodes with low loss and very low distortion leads to the application of these diodes under high RF power conditions. At the same time the used technology, Silicon-on-Glass, which is mainly responsible for the low loss, has a very high thermal resistance. In other technologies with a lower thermal resistance, typically the reachable quality factor is lower, and therefore the related losses higher. For many technologies, however, the quality factor tends to decrease with temperature; the combination of these effects may lead to thermal instability under high RF power. To investigate these effects first the relation between the thermal resistance and the increase in temperature has to be calculated, which gives an upper limit for the thermal resistance and a lower limit for the quality factor, for a given RF power and temperature increase. To quantify these effects, pulsed measurements are performed on a Silicon-on-Glass varactor diode. From these measurements the thermal

resistance, as well as the thermal behavior of the quality factor versus temperature has been extracted.

6.3.2 Self heating

Under normal operation the varactor diodes will not reach forward bias, nor reverse breakdown. Therefore, in this analysis it is assumed that the thermal dissipation only depends on the RF losses in the device. Heating due to high reverse leakage current which can flow at high reverse bias, before reaching actual breakdown is assumed to be negligible, which, for a correctly constructed varactor, is generally true.

Heating due to RF losses

For typical varactors the losses related to the RF signal arise from the series resistances, which are mainly the metal resistance, the metal to semiconductor contact resistance and the semiconductor resistance of the undepleted region of the active semiconductor (see Section 3.3). The losses in the device are quantified by the quality factor, which can be expressed as

$$Q(\Delta T) = \frac{1}{2\pi f R(\Delta T) C}, \tag{6.1}$$

where f is the frequency, C is the capacitance assumed independent of temperature $T = T_0 + \Delta T$ and $R(\Delta T)$ is the temperature dependent resistance, where a linear temperature dependency can be assumed for simplicity as

$$R(\Delta T) = R_0(1 + \alpha \Delta T), \tag{6.2}$$

in which R_0 is the resistance at the reference temperature, α is the thermal coefficient of the resistance and ΔT is the temperature increase due to dissipation. The device temperature T_{dev} is $T_{amb} + \Delta T$.

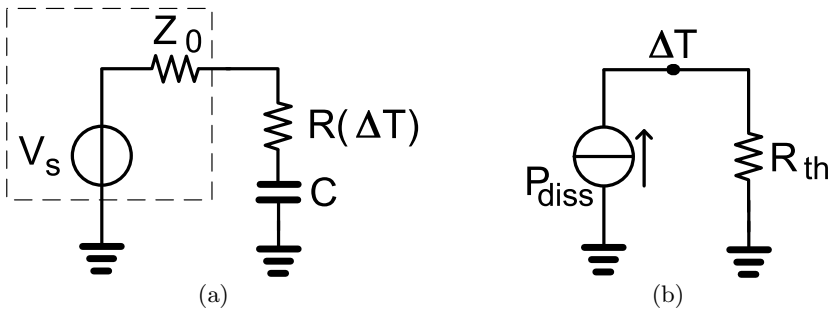


Figure 6.7: (a) Power source V_s with internal impedance Z_0 applied to the varactor C with temperature dependent series resistance $R(\Delta T)$. (b) Associated thermal network.

The schematic in Fig. 6.7(a) shows a varactor with its associated losses connected to a power source with impedance Z_0. Fig. 6.7(b) shows the thermal network used to calculate the rise in temperature ΔT as function of thermal resistance R_{th} and dissipation P_{diss}. The RF current I_{rf} can be calculated as:

$$I_{rf} = \frac{V_s}{Z_{in}} = \frac{V_s}{\left| Z_0 + R(\Delta T) + \frac{1}{j\omega C} \right|}. \tag{6.3}$$

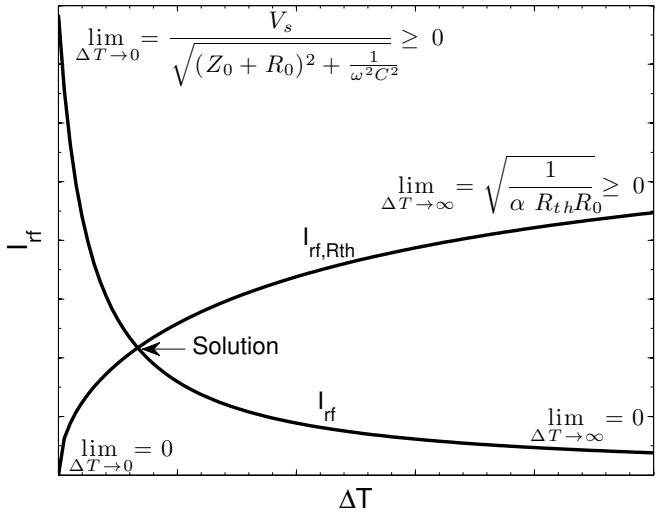
Since $\Delta T = P_{diss} R_{th}$ and $P_{diss} = I_{rf}^2 R(\Delta T)$ the RF current can also be written as

$$I_{rf,Rth} = \sqrt{\frac{\Delta T}{R_{th} R(\Delta T)}}, \tag{6.4}$$

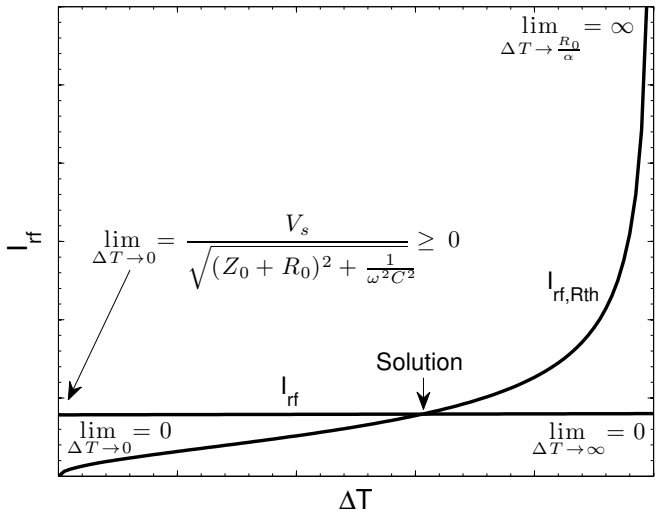
where the subscript '$_{Rth}$' indicates that the current is calculated using the thermal network. Solving the equations (6.3) and (6.4) simultaneously determines the solution of currents and voltages in these two networks, taking into account the dissipation and resulting heating of the device. If this set of equations is unsolvable, a point of thermal instability is found [94]. Therefore, solving $I_{rf} = I_{rf,Rth}$ for R_{th}, where all variables are ≥ 0, except α, followed by substituting (6.1) leads to

$$R_{th} = \frac{Q \Delta T \left(\omega^2 C^2 {Z_0}^2 + \frac{2\omega C Z_0}{Q} + \frac{2\omega C Z_0 \alpha \Delta T}{Q} + \frac{1}{Q^2} + \frac{2\alpha \Delta T}{Q^2} + \frac{\alpha^2 \Delta T^2}{Q^2} + 1 \right)}{\omega C {Vs}^2 (1 + \alpha \Delta T)} \tag{6.5}$$

which directly determines the relation between the R_{th} and resulting ΔT. This indicates for these networks no thermal instability will occur under the assumptions given at the start, e.g. linear temperature dependence of the resistance. This solution can also be graphically determined by plotting both I_{rf} and $I_{rf,Rth}$ as shown in Fig. 6.8(a) for $\alpha \geq 0$. For $\alpha < 0$ the maximum ΔT is limited to R_0/α, as shown in Fig. 6.8(b), since $R(\Delta T)$ reaches zero at that point.



(a) $\alpha \geq 0$



(b) $\alpha < 0$

Figure 6.8: (a) Graphical solution of equations (6.3) and (6.4) for $\alpha \geq 0$ and (b) for $\alpha < 0$. The limits to zero and ∞ are indicated.

By now limiting the allowed ΔT to a fixed value, the minimum required Q for a given V_s and R_{th} is given in Fig. 6.9 for a 10 pF device with $\alpha = 0.004$ (typical for metals [95]). Using results from literature (R_{th} = 10,500 K/W, $A = 20\ \mu m^2$) [96] and assuming an inverse quadratic dependency on scaling of the active device area [97], the expected thermal resistance for the Silicon-on-Glass varactors on 525 μm glass substrate is 400 K/W (10 pF) - 1250 K/W (1 pF). E.g. from Fig. 6.9 can be concluded that for V_s = 20 V (this corresponds to P_{avs} = 1 W) and an R_{th} = 400 K/W a minimal Q of 100 is required to keep the temperature increase below 10 degrees. In the next section the R_{th} will be determined for the Silicon-on-Glass technology, using pulsed/continuous measurements, so the conclusions on the thermal behavior of Silicon-on-Glass varactors can be refined.

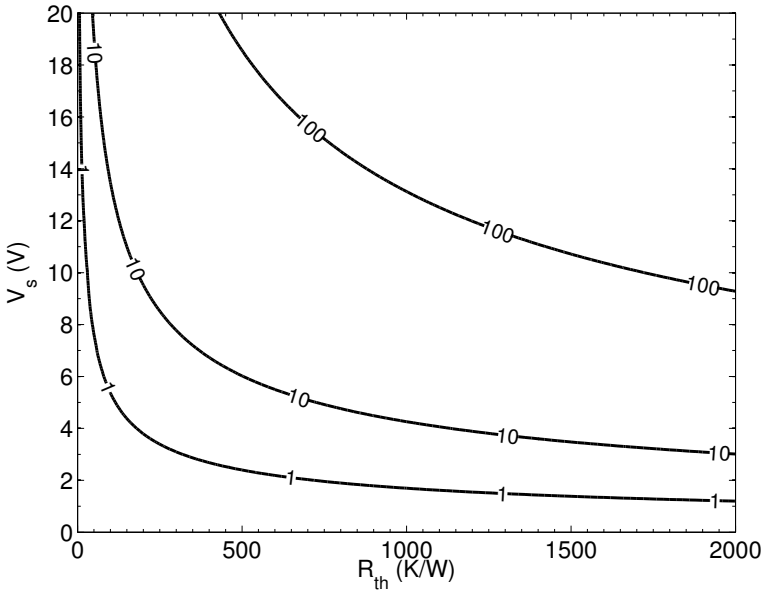


Figure 6.9: Contours of constant Q for a maximum allowed temperature increase ΔT of 10 K as function of V_s and R_{th}, for a 10 pF device with $\alpha = 0.004$ at 1 GHz in a 50 Ω environment.

6.3.3 Experimental results

To investigate the thermal behavior, pulsed dc and S-parameter measurements [98] are performed at different temperatures ranging from 25 ^{0}C to 125 ^{0}C. Due to the fact that in most bias regimes the dc dissipation is not high enough to create any difference between the pulsed and continuous measurements, the thermal resistance of the device has to be extracted from measurements in forward bias or in reverse bias close to breakdown. In addition there is a limitation on the minimum current the pulsed setup can measure accurately. The measured dc thermal resistance may differ from the RF thermal resistance, e.g. due to the skin effect of the metal connecting resistances.

To avoid differences due to heat transfer through the probes, both dc measurements and S-parameter measurements made use of RF probes. Furthermore, care has been taken not to change the contact resistance when changing from continuous to pulsed measurements.

Pulsed DC results

From the comparison (Fig. 6.10) between a continuous measurement and pulsed dc measurements at different temperatures, the internal device temperature under continuous dissipation can be extracted. During the pulsed measurements the heating of the device is negligible, whereas during the continuous measurements the device will heat up due to dissipation to an equilibrium. The intersection of the pulsed measurement curve with the continuous measurement curve indicates the temperature of the device during the continuous measurement. From the power dissipation and device temperature as shown in the inset of Fig. 6.10 the thermal resistance and the ambient temperature can be determined. The ambient temperature is the intersection with the x-axis, i.e. zero power dissipation, while the thermal resistance is equivalent to the slope of the curve. From this experiment $T_{amb} = 23.9\ ^0$C and R_{th}=1706 K/W are found. Compared to Silicon-on-Glass results from literature, this device has been fabricated on a thicker substrate, notably 700 μm, which explains the higher thermal resistance.

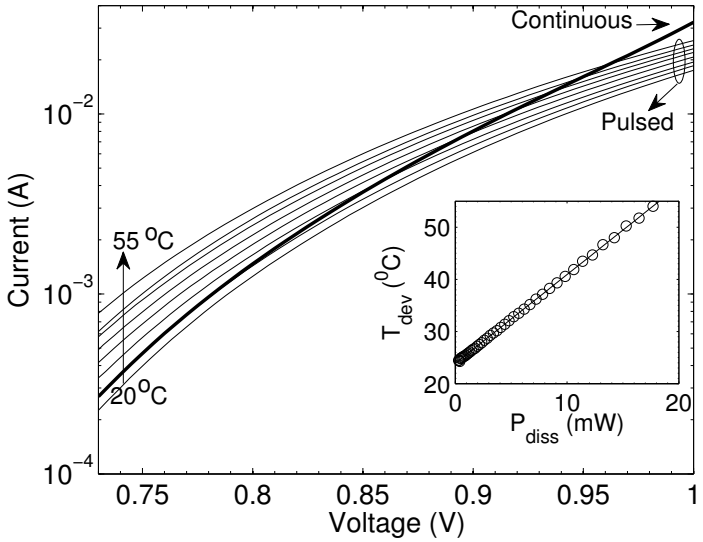


Figure 6.10: Measured I-V characteristics of a 1296 μm^2 varactor ($\sim$ 1 pF), both in continuous mode (thick line) at one temperature and pulsed mode (1 μs pulse, 1 ms pulse period) at various temperatures from 20 to 55 ^{0}C. The inset shows the extracted device temperature as function of power dissipation during the continuous measurement.

Small signal results

Using small signal measurements the capacitance and its associated series resistance can be determined as function of both temperature and voltage. This data can then be used to calculate the thermal coefficient of resistance as function of voltage and to calculate the thermal dependency of the capacitance value as function of voltage.

From S-parameter measurements of a varactor, the raw and deembedded series resistance $R(V,T) = \Re(Z_{11})$ at 2 GHz are extracted and are given in Fig. 6.11(a) for zero bias voltage. From the $R(V,T)$ data over the frequency range 2 - 26.5 GHz the thermal dependence α is extracted using [6.2] for every frequency and bias point. From this data the mean and standard deviation of the extracted thermal dependence are calculated using all frequency points and are given in Fig. 6.11(b) as function of voltage. Also the capacitance temperature dependency of the raw and deembedded varactor at 2 GHz is given in Fig. 6.11(c) for zero bias. The mean and standard deviation of the associated capacitance thermal dependency in ppm/degree are given in Fig. 6.11(d) as function of bias voltage. Where the mean and standard deviation were calculated over the range from 2 GHz - 13 GHz. The upper frequency is limited to remain below the self-resonance of the varactor. From the deembedded data it is concluded that α is possibly voltage dependent. However, due to the large standard deviation of this extracted value, a fixed value of 0.005 $^0C^{-1}$ is taken. The thermal dependence of the capacitance is voltage dependent and ranges from 114 ppm $^0C^{-1}$ to 750 ppm $^0C^{-1}$. This thermal dependence of the capacitance is important for designers who require exact capacitance values, but due to the small dependency compared to α, the capacitance thermal dependency is ignored in the calculations of maximum allowed R_{th}, as was also done in the earlier presented theory.

By now using this theory, the maximum R_{th} that can be allowed for this device (using α=0.005 $^0C^{-1}$), for a 10 degrees increase in ΔT is 176 K/W for an input power of 1 W in a 50 Ω system, which is much less than the extracted value for this device. Instead under the same conditions, the maximum power this particular device could handle, while warming up by a maximum of ten degrees, is 100 mW. However this is the thermal resistance of a single varactor, for the implementation of a DFVS with the same capacitance 4x more area is required, reducing the thermal resistance. Furthermore, the thermal resistance can be reduced by thinning down the glass wafer. However, care has to be taken not to increase parasitics too much, since parasitics can both reduce the linearity (Section 4.3) and the tuning range of the varactors. Another possibility would be the use of AlN layers around the active device region as a heat-spreader to reduce the thermal resistance, as has been demonstrated on Silicon-on-Glass bipolar transistors [99].

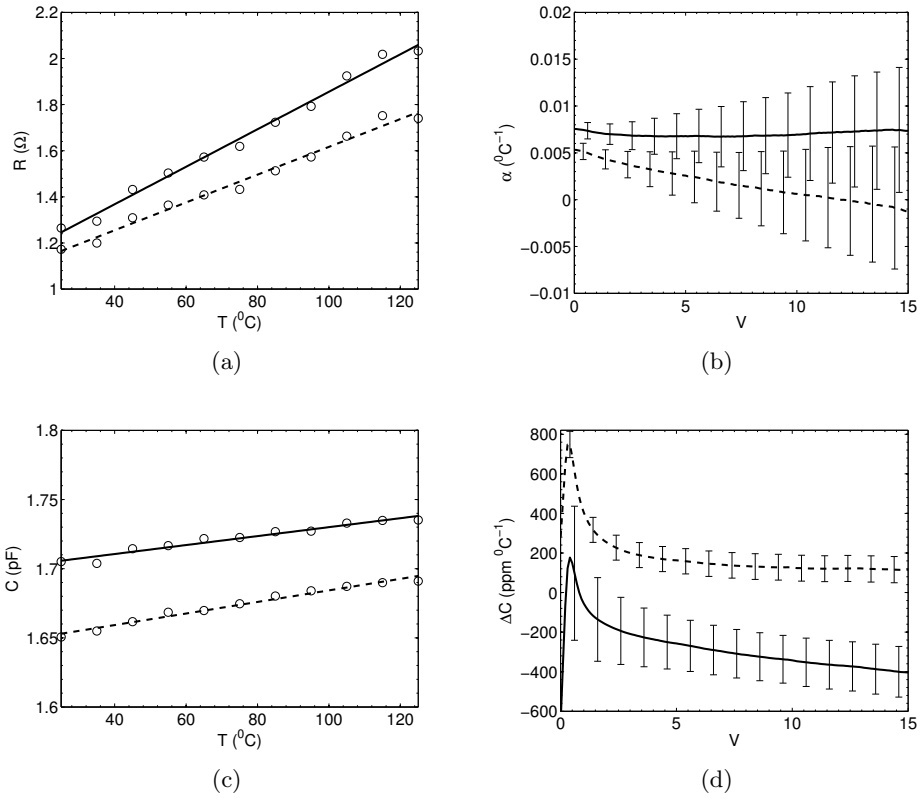


Figure 6.11: Extracted from measured s-parameters at 2 - 26.5 GHz of a 1296 μm^2 varactor (a) resistance versus temperature at zero bias at 2 GHz. (b) Mean thermal dependence of resistance versus voltage, input data ranged from 2 GHz - 26.5 GHz, the error-bars indicate the standard deviation. (c) Capacitance versus temperature at zero bias at 2 GHz and (d) capacitance thermal dependency versus bias in ppm/degree, input data ranged from 2 GHz - 13 GHz, the error-bars indicate the standard deviation. (Solid lines are based on raw measurement data, dashed lines on open-short deembedded measurement data, lines in (a,c) are fitted to (o) marked measured data.)

6.4 Direct model extraction

6.4.1 Introduction

The capacitive and resistive behavior of devices is mostly studied by looking at the real and imaginary part of a measured impedance Z. However, these components are not strictly independent when parasitics are considered. In this section a method will be discussed that takes into account these parasitics and extracts a small signal model. The method is then applied to measured data. The correct extraction of small signal parameters of devices, i.e. varactor diodes, is necessary for creating an accurate model. Current extraction techniques can correctly determine the imaginary part, assuming the Q factor is high enough. However, for model extraction also the real part is important. Therefore, a technique is proposed to simultaneous extract all parameters. Furthermore, the technique is only limited by the accuracy of the measurement technique and the assumptions placed on the small signal network. The proposed technique is based on a certain network assumption to represent the device. By measuring the impedance of the device at two different frequencies, a set of equations can we written and solved uniquely. This technique can also be used to determine the doping profile of devices, similar to conventional CV methods. However, this technique also performs well on leaky diodes, fets and can be extended further towards breakdown than conventional methods. The proposed technique is applied to high performance varactor diodes.

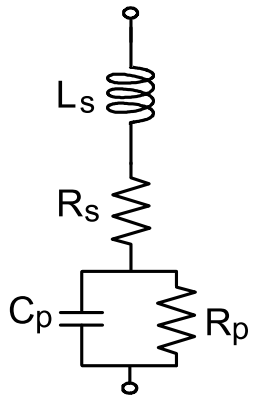


Figure 6.12: Schematic of varactor model used in direct model calculation.

6.4.2 Extraction procedure

First, a small signal network to represent the device is constructed, (Fig. 6.12). In which R_s represent the series resistance, L_s the series inductance, R_p the parallel resistance and C_p the parallel capacitance. The impedance Z of the network is given by

$$Z = R_s + j\omega L_s + \frac{1}{j\omega C_p + \frac{1}{R_p}}. \tag{6.6}$$

The difficulty in present techniques arises because the resistance and capacitance are not strictly dependent on the real and imaginary parts only:

$$\Re(Z) = R_s + \frac{1}{R_p\left(\frac{1}{R_p^2} + \omega^2 C_p^2\right)}, \tag{6.7}$$

$$\Im(Z) = \omega L_s + \frac{\omega C_p}{\frac{1}{R_p^2} + \omega^2 C_p^2}. \tag{6.8}$$

From equations (6.7) it is clear that $\Re(Z)$ is only equal to R_s when R_p is very large. In a similar fashion from equation (6.8) it can be seen that $\Im(Z)$ is only equivalent to ωC_p when both L_s and R_p are small. Of course the influence of L_s is well known, since it will result in resonance. The components R_s, L_s, R_p and C_p are assumed to be frequency independent, which will be correct for small variations in frequency. These components can be solved from the following equations, for which measurements at two different frequencies are required:

$$R_s = f_1(\omega_1, \omega_2, Z_1, Z_2), \tag{6.9}$$

$$L_s = f_2(\omega_1, \omega_2, Z_1, Z_2), \tag{6.10}$$

$$R_p = f_3(\omega_1, \omega_2, Z_1, Z_2), \tag{6.11}$$

$$C_p = f_4(\omega_1, \omega_2, Z_1, Z_2), \tag{6.12}$$

where ω_1 and ω_2 are the angular frequencies at which the impedances Z_1 and Z_2 are measured. The equations are straightforward for the case where $L_s = 0$:

$$R_s = -AX_2^2\omega_1\omega_2 + AX_1X_2\omega_1^2 + R_2, \tag{6.13}$$

$$R_p = A(\omega_1 + \omega_2)(-\omega_1 + \omega_2)X_1X_2, \tag{6.14}$$

$$C_p = -\frac{-X_2\omega_1 + X_1\omega_2}{X_2X_1(-\omega_1^2 + \omega_2^2)}, \tag{6.15}$$

with

$$A = \sqrt{\frac{1}{\omega_1^3X_1X_2\omega_2 + \omega_2^3X_1X_2\omega_1 - \omega_1^2X_2^2\omega_2^2 - \omega_1^2X_1^2\omega_2^2}}. \tag{6.16}$$

Where R_1, X_1 and R_2, X_2 are the real and imaginary components of Z_1 and Z_2, respectively. In the rest of the thesis we use the full four components, where L_s is included as well. The resulting equation are more complicated (see Appendix A), however, easy to handle in a software package like MATLAB® [100].

6.4.3 Extraction results

The above theory has now been applied to a 36 μm x 36 μm varactor device. The current voltage characteristics are given in Fig. 6.13. In this figure three different regions can be be identified: forward biased region, low reverse bias region with very low leakage and increased leakage at increased reverse bias voltage. This last region needs the proposed direct model calculation the most, since the parallel resistance will be low and will influence both the series resistance as well as the capacitance when using more traditional methods.

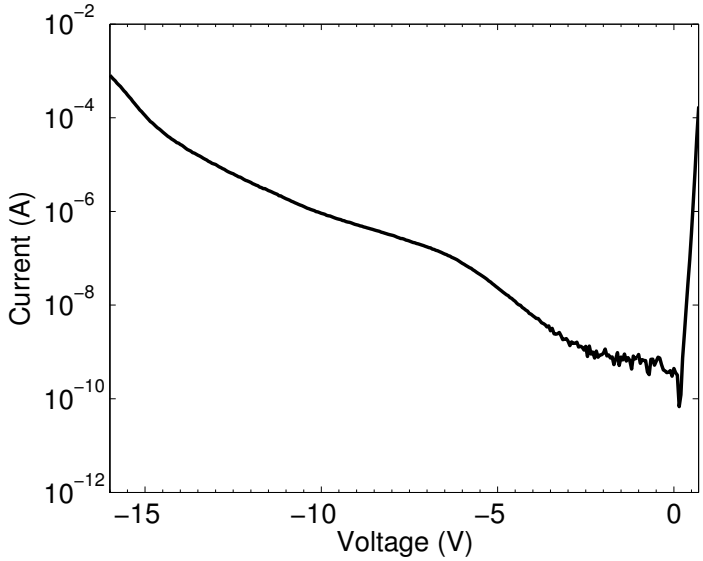


Figure 6.13: Measured current as function of applied voltage of a 1296 μm^2 varactor.

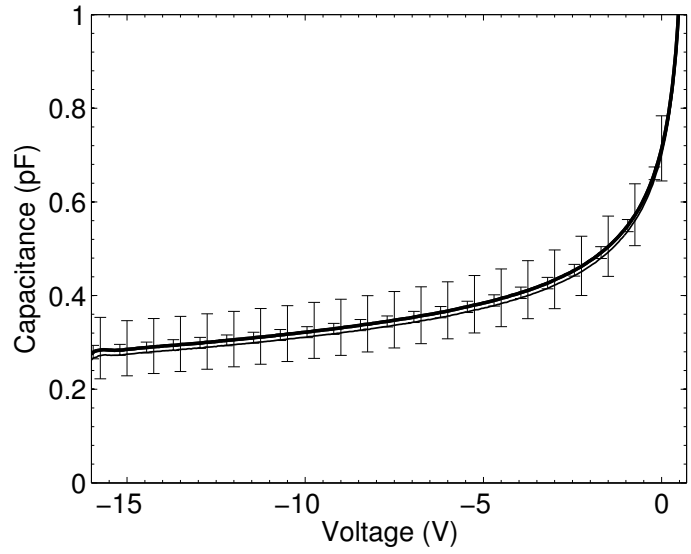
The S-parameters as a function of frequency and voltage have been measured of a varactor in shunt configuration. The device has been de-embedded using the open/short method. The resulting de-embedded S-parameters have been converted to Z-parameters. Note that Z_{11} represents directly the impedance of the varactor. Now Z_{11} at 2 and 2.25 GHz is the starting point for the direct model calculation. The measurement of Z_{11} suffers from small errors, both random and systematic errors. Note, that the frequency separation should be chosen large enough to have two clearly separate impedances, since otherwise the random errors have too large influence.

The systematic error can be seen as a small error vector on top of the impedance vector. These errors result from imperfect calibration and/or small phase deviations, which appear over time after calibration. This systematic error can be estimated directly after calibration, by comparing a model of a standard (open or short) with the actual measurement of this standard. Typical amplitude deviations after calibration, for a open or short standard, are in the order of 0.05 dB to 0.01 dB. However, the phase of this error vector is unknown. To estimate the influence of this error vector

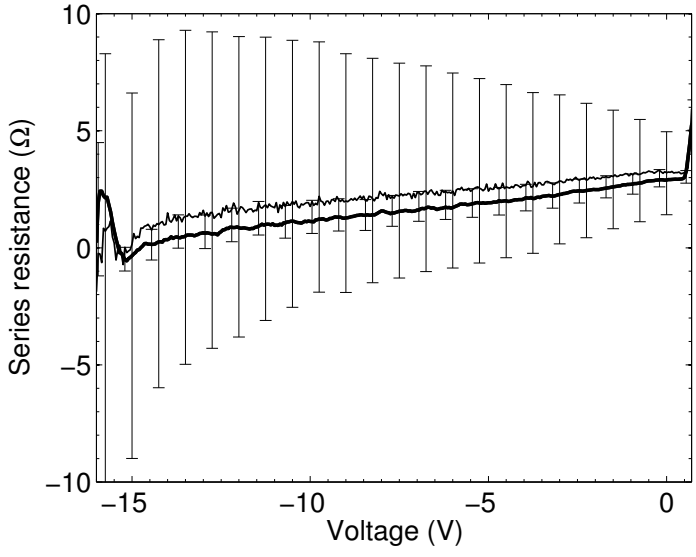
the worst case scenarios have been calculated for the extracted component values and have been plotted as error-bars for both an amplitude of 0.05 dB and 0.01 dB.

The extracted C_p is given in Fig. 6.14(a) with its associated error bars. The error bars do not indicate the standard deviation, but indicate the range within the 'real' value of C_p is expected for a specific estimated error vector. In similar way R_s is given in Fig. 6.14(b), and R_p and L_s are given in Fig. 6.15. The extracted R_p value is a direct indication for the amplitude of this error-vector, the smaller the error, the larger R_p. Furthermore, the 'real' R_p is known from dV/dI (see Fig. 6.15(a)) and can be compared to the extracted value of R_p. Note, that in Fig. 6.15(a) the range for R_p moves towards larger R_p values, when the estimated error is smaller.

Now, the extracted values using the direct model calculation can be optimized by estimating the error vector. By using the extra information provided by $R_{pIV} = dV/dI$, the difference between R_p and R_{pIV} can be minimized. The resulting optimized C_p, R_s, R_p and L_s are also given in Fig. 6.14 and Fig. 6.15.

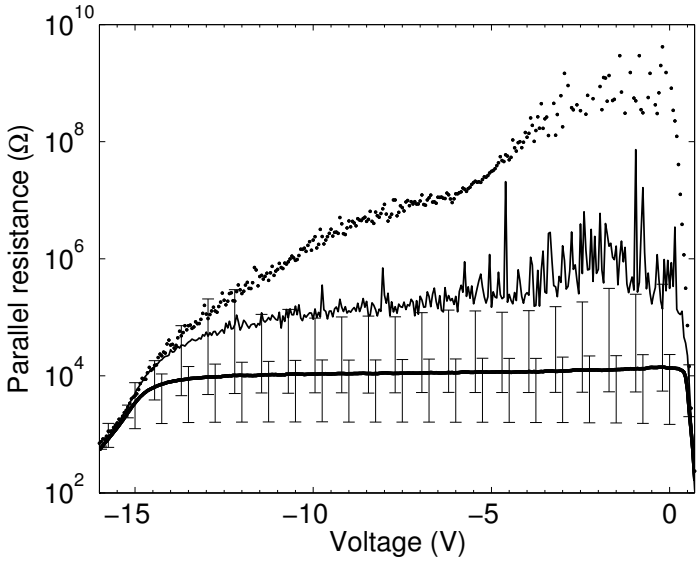


(a)

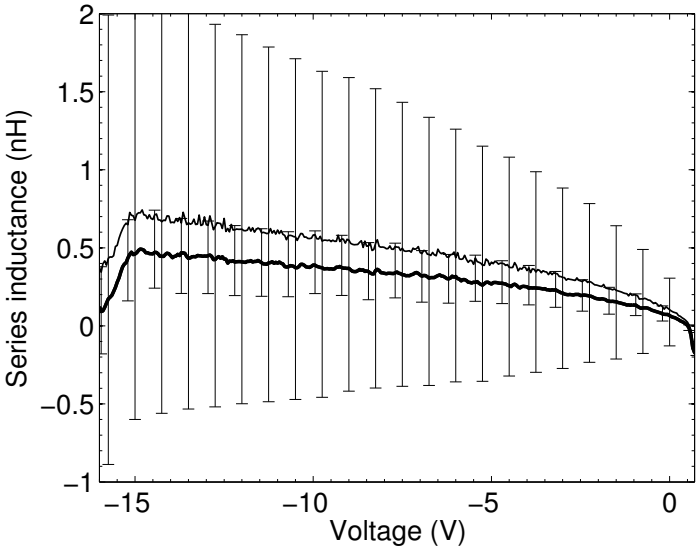


(b)

Figure 6.14: (a) Extracted C_p using the direct model calculation (thick line) with associated error-bars indicating worst case error-vector corresponding to 0.05 dB and 0.01 dB. Extracted optimized C_p based on R_{pIV} (thin line). (b) Extracted R_s using the direct model calculation (thick line) with associated error-bars indicating worst case error-vector corresponding to 0.05 dB to 0.01 dB. Extracted optimized R_s based on R_{pIV} (thin line).



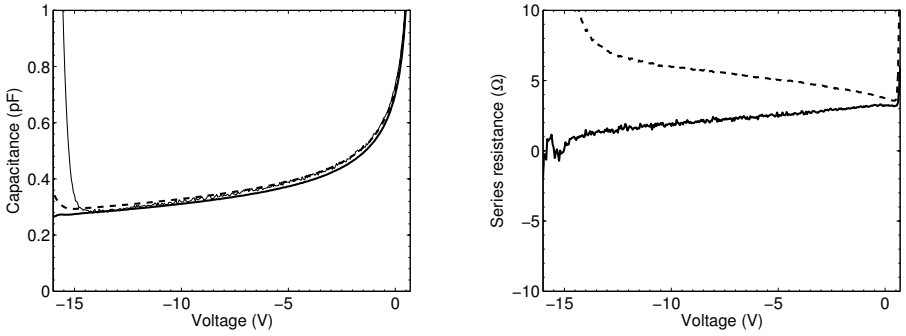
(a)



(b)

Figure 6.15: Extracted R_p using the direct model calculation (thick line) with associated error-bars indicating worst case error-vector corresponding to 0.05 dB and 0.01 dB. Extracted optimized R_p based on R_{pIV} (thin line). R_{pIV} is given by the dots. (b) Extracted L_s using the direct model calculation (thick line) with associated error-bars indicating worst case error-vector corresponding to 0.05 dB to 0.01 dB. Extracted optimized L_s based on R_{pIV} (thin line).

When comparing $(j\omega\Im(Z_{11}))^{-1}$ at 250 MHz and 2 GHz to the extracted optimized C_p, the advantage of the direct model calculation is demonstrated (Fig. 6.16(a)). Whereas the imaginary part of Z_{11} is strongly influenced by the reverse leakage, the direct model calculation gives a smooth result up to close to the breakdown voltage. Note, that C_p has slightly lower values because the series inductance L_s has been extracted. Furthermore, the advantage of increasing the measurement frequency to perform doping profile extraction is demonstrated. However, even better results can be obtained using the direct model calculation. The extracted and optimized R_s compared to $\Re(Z_{11})$ shows a similar result, the real part of Z_{11} is influenced by the capacitance, and by the leakage. The extracted R_s as given in Fig. 6.16(b) shows the resistance behavior as expected from a varactor where the depletion region grows and the non-depleted region shrinks.



(a) (b)

Figure 6.16: (a) Extracted optimized C_p (thick line) compared to $(j\omega\Im(Z_{11}))^{-1}$ at 250 MHz (thin line) and 2 GHz (dashed line). (b) Extracted optimized R_s (thick line) compared to $\Re(Z_{11})$ at 2 GHz (dashed line).

Fig. 6.17 shows the extracted Q, calculated from the optimized C_p and R_s only. This show that the error vector of the measurement may reduce the obtainable Q. For the high Q measurements of Chapter 5, special care has been taken to keep the error vector low, i.e. make sure the residual deviation on a measured standard is as small as possible after calibration, below 0.01 dB.

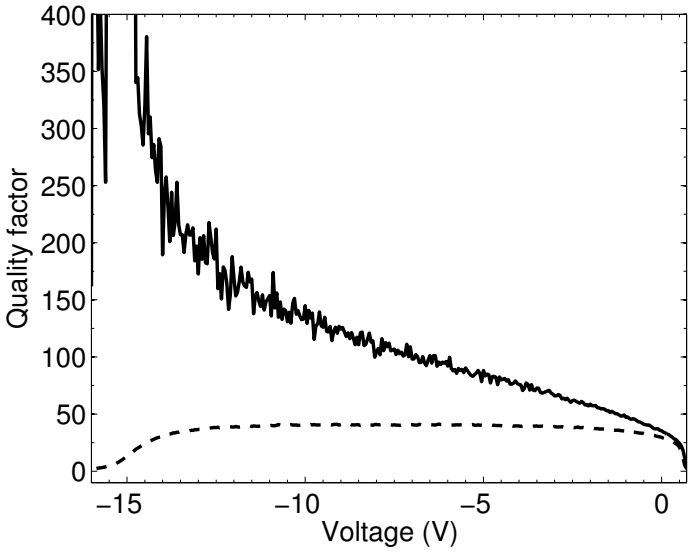


Figure 6.17: Extracted Q from optimized C_p and R_s (thick line) and measured $Q = \Im(Z_{11})/\Re(Z_{11})$ (dashed line).

6.5 Conclusion

Large signal two-tone measurements confirm the linearity performance of the DFVS topologies. This very high linearity also demonstrated the suitability of Silicon-on-Glass technology for low device parasitics, especially with respect to the center tap connection. Furthermore, stacking multiple devices improves the power handling capabilities and simultaneously improves the linearity. However, the low thermal conductive properties of glass may be an issue. There are two potential solutions, either thinning down the glass substrate, or the inclusion of thermally good conductive layers around the active device region, e.g. AlN. Finally, a direct model calculation method has been introduced and demonstrated to be a helpful tool to obtain insight in the exact behavior of the varactor diodes. In connection to that the importance for measurement error has been demonstrated for high Q devices.

Chapter 7

Silicon-on-glass varactor circuit realizations[1]

7.1 Introduction

Earlier this thesis discussed the need for adaptive RF systems in order to handle the continuously increasing number of communication bands and standards. To address this need, the focus was on electronic and technology concepts to realize low-loss, low-distortion tunable RF components. While until now the emphasis was on the performance of individual components, in this chapter these devices are applied in various subcircuits that can act as technology demonstrators for the Silicon-on-Glass technology. The demonstrators include adaptive matching networks, which facilitate the implementation of multi-band power amplifiers, varactor based low-distortion tunable bandpass filters, continuously tunable phase shifters, as well as an example of a tunable reflect array antenna.

7.2 Adaptive matching networks

Low-loss adaptive matching networks promise to solve a number of outstanding problems in the design of microwave and RF circuits. For example, they have the ability to tune the matching conditions for power amplifiers in order to optimize the load impedance such that the best performance at varying output powers and antenna conditions is achieved.

In this section varactor based tuning elements are used for the implementation of two adaptive matching networks. For these networks the technology constrains, their

[1]Parts of this chapter were published by: K. Buisman, L. C. N. de Vreede, L. E. Larson, M. Spirito, A. Akhnoukh, Y. Lin, X.-d. Liu and L. K. Nanver, "Low distortion, low-loss varactor-based adaptive matching networks, implemented in a silicon-on-glass technology," in Digest of IEEE Radio Frequency integrated Circuits, 2005, RFIC 2005. And by the same authors in: "A monolithic low-distortion low-loss silicon-on-glass varactor-tuned filter with optimized biasing," in IEEE Microwave and Wireless Components Letters, 2007.

design and measured performance are discussed in terms of impedance tuning range, losses and linearity. The resulting networks are compact (< 3.5 mm^2), continuously tunable, and meet the power and linearity requirements for a typical handset output stage.

7.2.1 Adaptive matching network design

The impedance tuner of Fig. 7.1 consists of low-loss coplanar transmission lines and varactor diode tuning to continuously vary the impedance transformation. This topology has been selected for its ease of implementation and the low Q condition it offers for the high input power/low input impedance condition (see Fig. 7.2(a)). Furthermore, due to the shunt configuration of the varactor stack, it is less sensitive to varactor parasitics since these are also shunted to ground. There are only two control voltages, and the total structure is very compact (< 3.5 mm^2).

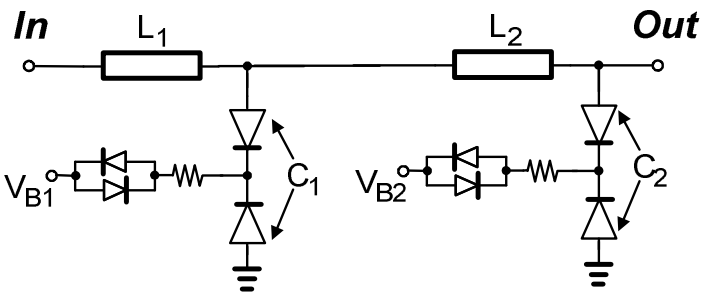


Figure 7.1: Schematic diagram of varactor diode-based tuners. The two versions of the tuner are designed for a load impedance of either 50 Ω or 25 Ω. The element values for the tuner are given in Table 7.1.

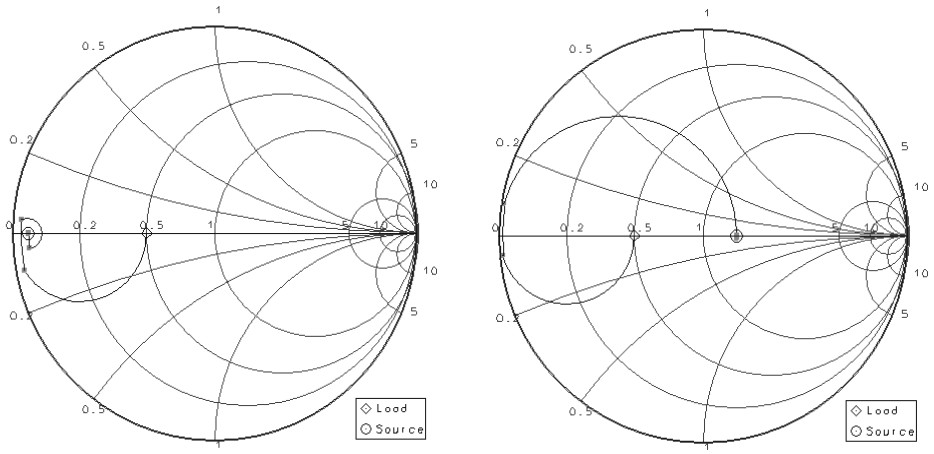
Table 7.1: Component values of the integrated tuners, the other coplanar transmission line parameters are; width=265 μm, gap=143 μm. The capacitance values are zero-bias values.

Element	25 Ω structure	50 Ω structure
L_1	612 μm	450 μm
C_1	43.5 pF	72.9 pF
L_2	2491 μm	2018 μm
C_2	32.5 pF	32.5 pF

One of the features of this structure is, that it provides an ohmic loading condition at its input port ranging from below one ohm to tens of ohms. Since the tuning speed can be very high, this also makes the network a potential candidate for use in dynamic load-line amplifier concepts [101]. Two circuits based on the topology of Fig. 7.1,

have been implemented with approximately the same power handling capabilities. One tuner is designed for a 50 Ω output loading, and the other is designed for a 25 Ω output loading (for more relaxed element values (see Table 7.1)). Both tuners fulfill the following constraints:

- tuning range varactors (c_{ratio}): < 2.5,
- design frequency: 2 GHz,
- control voltages: < 18 V,
- impedance transformation ratio: > 10,
- no-forward biasing of one of the diodes by RF input powers up to 1 Watt.



(a) (b)

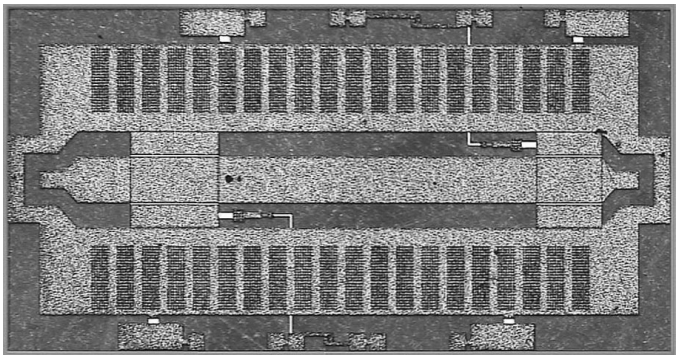
Figure 7.2: Simulated Smith Chart trajectory with variation in varactor diode capacitance for the 25 Ω structure; (a) low input impedance (2 Ω) mode, (b) high input impedance (50 Ω) mode. Note the high-Q (trajectory very close to the edge) in the 50 Ω mode.

7.2.2 Experimental results

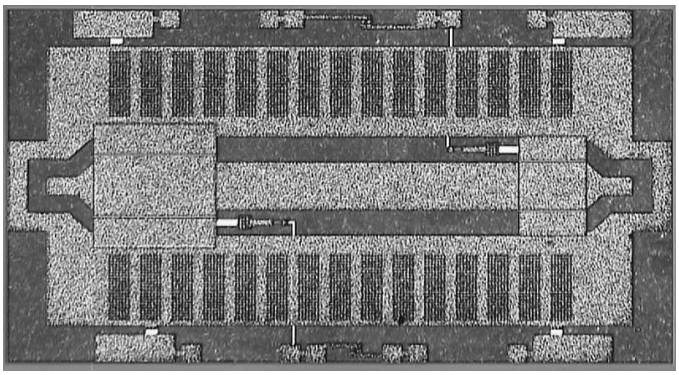
The tuner circuits of Fig. 7.1 were fabricated in the high performance Silicon-on-Glass technology described in Chapter 5. The diodes were designed for a uniform doping profile, to realize a value of $n = 0.5$, but due to the limited availability of wafers at the time of processing, a grading coefficient of $n \approx 0.55$ was used. The realized tuner circuits are given in Fig. 7.3. The measured Q and C^{-2} versus voltage of a 15 pF test DFVS are given in Section 5.3.2. The measured C^{-2} plot shows a deviation from the ideal straight line of the uniformly doped case. This is also reflected by the somewhat reduced zero bias quality factor of the varactors. This is expected to slightly degrade

the linearity of the tuner, but, fortunately, the linearity of the anti-series configuration is quite insensitive to these deviations (Section 4.3), as will be shown later.

Fig. 7.4 shows the measured values of S_{11} at 2 GHz for the two tuners. Note the close-to-ideal distribution of impedance points which cover the ohmic control range of 0.2 to 82 Ω and 0.2 to 49 Ω for the 25 Ω tuner and the 50 Ω tuner respectively. From this data we observe for both tuners a VSWR > 250:1.



(a)



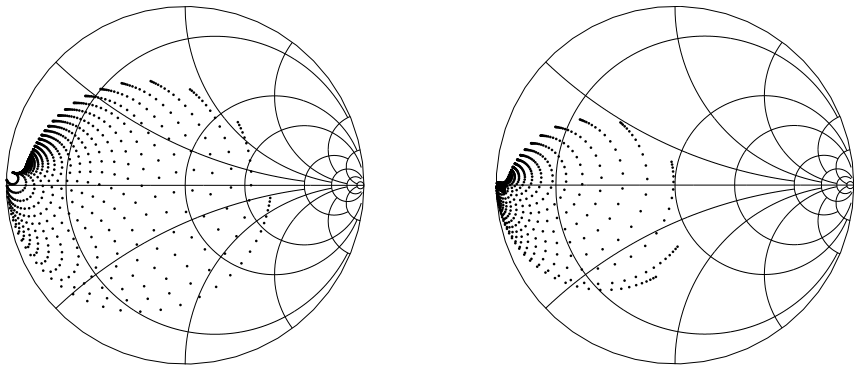
(b)

Figure 7.3: (a) Microphotograph of the 25 Ω varactor based impedance tuner. The outer dimensions of the photograph are 4182 μm by 1963 μm. (b) Microphotograph of the 50 Ω varactor based impedance tuner. The outer dimensions of the photograph are 3372 μm by 1963 μm.

One of the most important aspects of tuner design is to maximize the power gain (Pout/Pin) or to minimize the losses of the structure. The definition of this gain is:

$$G_p = \frac{|S_{21}|^2}{1 - |\Gamma_{in}|^2} \tag{7.1}$$

Note, that G_p is a more appropriate measure for this network than G_{max}, which



(a) (b)

Figure 7.4: Measured S_{11} at 2 GHz for the integrated Silicon-on-Glass tuners; (a) tuner designed for 25 Ω loading, (b) tuner designed for 50 Ω output loading.

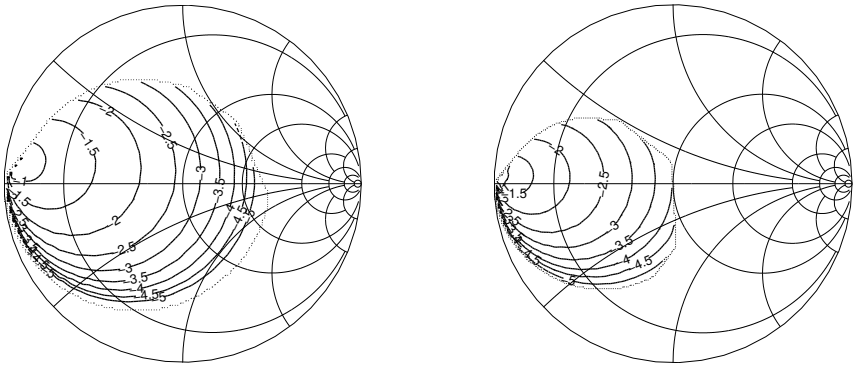
assumes conjugate matching conditions at both input and output. (G_{max} for both structures was approximately 0.2 dB for all tuning values). Maximizing the Q of the varactor diodes and minimizing ohmic losses in the transmission lines results in the lowest losses. Fig. 7.5(a) plots the measured loss contours at all the different tuning points, for the 25 Ω structure, the losses vary from 0.4 dB at 3 Ω to 2 dB for Z_{in}=50 Ω. The losses for the 50 Ω tuner are plotted in Fig. 7.5(b) and range from 0.6 dB at 1 Ω to 3.5 dB for Z_{in}=40 Ω.

At first glance, it is somewhat surprising that the highest losses are found for the lowest impedance transformation ratios. This is a consequence of the applied optimization of these matching networks, which was focused on achieving low Q conditions for high input power levels (low input impedances). As result high Q conditions arise for the low input power condition (high input impedances Fig. 7.2(b)). Other possible configurations can solve this limitation by using a low Q matching solution for all power levels.

The large-signal performance of the tuners has also been measured. Fig. 7.6 plots the $IM3$ versus output power for the 50 Ω structure as function of output power at low (2 Ω) and high (37 Ω) input impedance conditions. The IM3 components are below 50 dBc for both 27 dBm (2 Ω input) as well as 17 dBm (37 Ω input) output power, which represents the 10 dB power back-off condition. This performance is compatible with the linearity constraints of most communication standards for handsets.

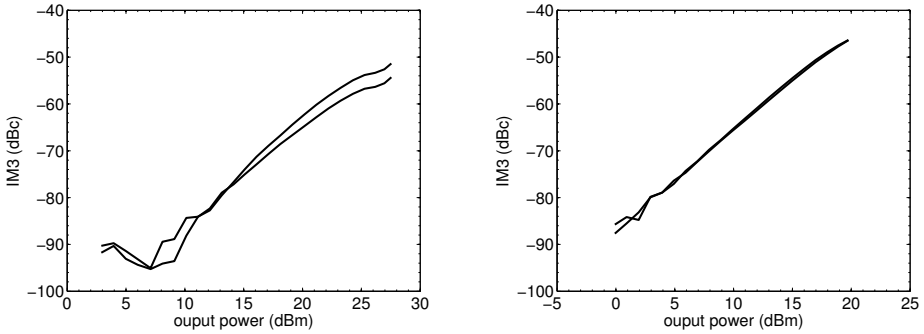
Conclusions on adaptive matching networks

An ultra low distortion varactor configuration has been applied in combination with a very low-loss, Silicon-on-Glass technology for the implementation of integrated tuners for adaptive matching. The measured close-to-ideal continuous tuning capabilities



(a) (b)

Figure 7.5: Measured loss contours (G_p in dB) at 2 GHz for the integrated Silicon-on-Glass tuners; (a) tuner designed for 25 Ω loading, (b) tuner designed for 50 Ω output loading.



(a) (b)

Figure 7.6: Measured upper and lower $IM3$ in dBc for the 50 Ω tuner structure f_c=2 GHz Δf=20 MHz; (a) Z_{in}=2 Ω, (b) Z_{in}=37 Ω.

make these networks very suitable for providing optimum loading conditions to the output stage, under varying output power or antenna matching conditions. The achieved performance of these networks in terms of loss, size, cost, tuning range, power handling and linearity, makes them attractive candidates for a variety of future adaptive tuning applications.

7.3 Multi-mode multi-band power amplifier using varactor based adaptive matching networks

Neo et al. realized a multi-mode, multi-band power amplifier [102] using Silicon-on-Glass adaptive matching networks comparable to the ones described in Section 7.2. The realized adaptive amplifier provided 13 dB gain, 27-28 dBm output power at the 900, 1800, 1900 and 2100 MHz bands. For the communication bands above 1 GHz these networks facilitate optimum load adaptation, resulting in efficiencies between 30%-55% over a 10 dB output power control range.

7.4 High linearity tunable varactor-based bandpass filter

A simple tunable single-pole/single-zero filter (Fig. 7.7) was implemented in order to demonstrate the capabilities of the Silicon-on-Glass DFVS technology. A filter like this might eventually be part of a SAW filter replacement in a mobile handset, minimizing the transmit leakage to the receiver/mixer in frequency-duplex cellular systems. The requirements for such a filter are extremely low loss in the receive band, high rejection in the transmit band, and high linearity to avoid cross-modulation distortion. A combination of low-loss on-chip micro-strip transmission lines and bondwires was utilized to create the required high-Q on-chip inductance as shown in Fig. 7.8. The measured tunable filter insertion loss and stop-band suppression is shown in Fig. 7.9, and the loss in the passband is 2-3 dB over the 1 GHz center frequency variation. The dc bias was varied from 1 to 13.5 V to tune the filter from 2.4 to 3.5 GHz. Although the dc tuning voltage is quite high, very little dc current is required for the tuning, because the diodes are reverse biased.

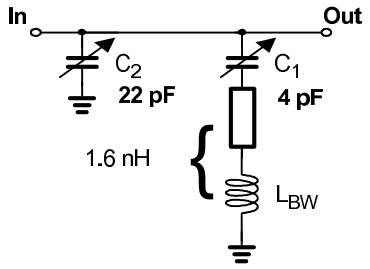
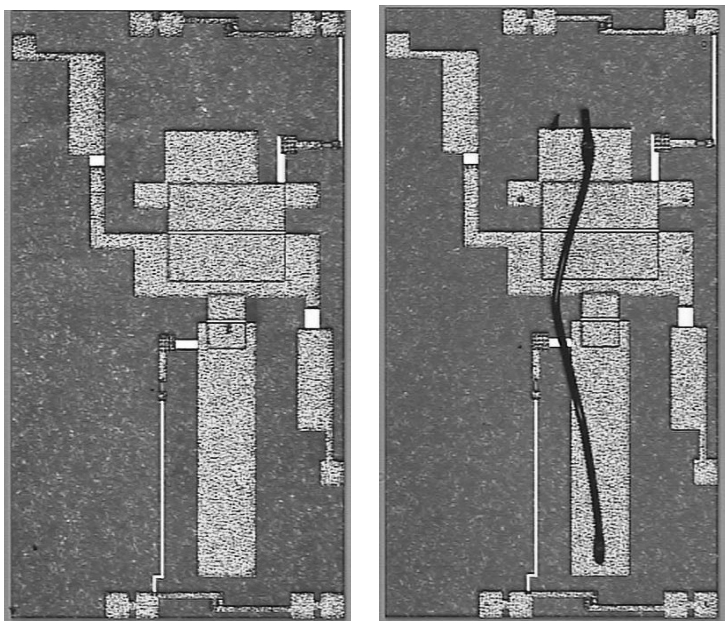


Figure 7.7: Schematic of the tunable bandpass filter.

The pole-zero spacing for this filter was set to 400 MHz and a triple-beat/XMOD distortion test (Section 2.1.3) was performed in order to characterize the large-signal behavior. For this purpose, two signals are presented at the stopband at 1.999 and 2.001 GHz with an output power level of -5.6 dBm (the input power is ∼25 dB higher). A jammer signal (f_{jam}=2.5 GHz, P_{out}=0 dBm) signal is presented in the passband. The resulting cross-modulation distortion components at f_{dist}=2.498 and 2.502 GHz,



(a) (b)

Figure 7.8: (a) Microphotograph of the bandpass filter, (b) with single bondwire. The outer dimensions of the photographs are 2394 μm by 1438 μm.

are -98.5 dBc with respect to the jammer signal. The resulting $IIP3$ for this test condition is calculated to be

$$IIP3 = 10\log(2) + P_{txl} - \frac{\Delta P_{xmod}}{2} = 46 \text{ dBm}, \tag{7.2}$$

where P_{txl} is the transmitted power level and ΔP_{xmod} is the cross modulation distortion product related to P_{txl} in dBc. In addition, a traditional two-tone test (Δf=2 MHz) was performed in the passband of the filter, also yielding an $IIP3$ of +46 dBm, confirming the cross-modulation derived $IIP3$ value. The performance of the filter, in terms of loss, size, cost, tuning range, power handling and linearity, are compatible with current requirements in modern communication systems.

7.5 Phase-shifters using high performance varactors

S. Kim et al., G. Gentile et al. and J. H. Qureshi et al. used the described varactor technology to realize tunable phase-shifters. Some of their results are briefly presented here:

Qureshi et al. presented a compact, low-loss (0.6 dB/90° @ 1.0 GHz), wideband 0 - 2 GHz and extremely linear, ($IP3$=47 dBm), varactor-based phase shifter [103].

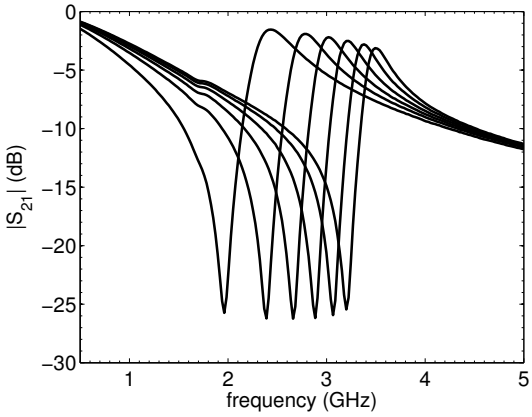


Figure 7.9: Measured $|S_{21}|$ versus frequency for tunable bandpass filter.

Kim et al. presented a varactor tuned continuously variable phase shifter [104] based on an all-pass network. The phase-shifter achieved an IIP3 of 52 dBm with 10 MHz tone-spacing at 2 GHz with a loss of 2.3 - 3.7 dB while providing continuous 180° phase control at 2 GHz. The total chip size including connection pads was 2900 μm $\times$ 2200 μm.

Gentile et al. presented experimental results for an integrated coplanar phase shifter based on varactor diodes [105]. A differential phase shift of 180 degrees has been obtained at 50 GHz with a control voltage varied between 2.1 and 15 volt. The return loss of the phase shifter was below 15 dB. The measured insertion loss in this structure strongly depends on the dc bias voltage applied, and ranged from 6.5 to 14 dB in the bias range of interest.

7.6 Active scan-beam reflect array antenna using high performance varactors

Hajian et al. built and tested a reflect array antenna at 6 GHz using the described Silicon-on-Glass varactors (see Fig. 7.10) as tunable element. The tunable elements are single DFVS connected in series in each antenna element. The bias is done thru high ohmic resistors, integrated directly with the varactors. The metal connections around the device are relatively large to facilitate bonding. The devices are mounted on a printed circuit board with the antenna elements, which, trough vias, applies the biasing and provides extra de-coupling on the back of the printed circuit board.

By biasing these varactor devices, the phase of each antenna element in the array can be adapted dynamically, and consequently its radiation beam (see Fig. 7.11) can be reconfigured [106, 107].

In the future, these devices could be flip-chipped onto these antenna elements to further reduce the losses and self-inductance, which will lead to the possibility of increasing the operating frequency.

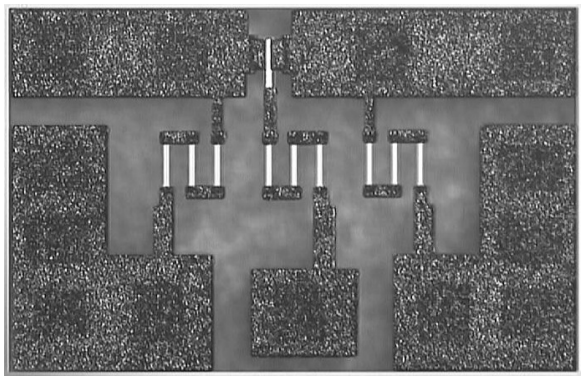


Figure 7.10: Single 1.3 pF varactor device with bias network and metal connections to facilitate bonding, as applied in the reflect array.

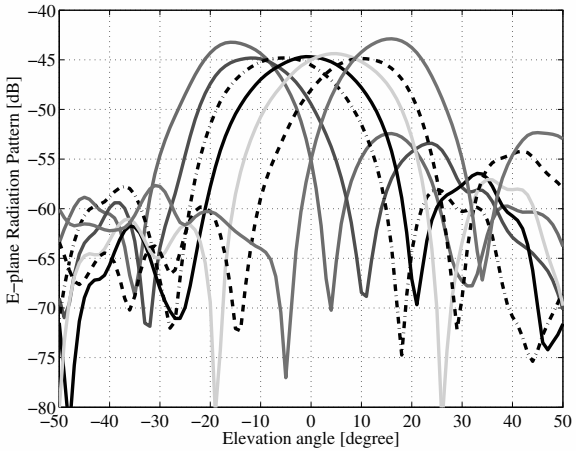


Figure 7.11: Measured radiation pattern at 6.15 GHz, the bias conditions have been varied to construct the different radiation patterns. From [106].

7.7 Conclusion

Several demonstrators have been shown to illustrate the performance and feasibility of these high performance, low loss, low distortion Silicon-on-Glass varactor devices in actual circuit applications. Typical linearities of the developed demonstrators were of the order of OIP3 $>$ 45 dBm. For these circuit applications the linearity performance could be further improved by implementing multi-stacking. This concludes the discussion on linear tunable elements and their applications. Final remarks will be made in the conclusion and recommendation section of Chapter 10.

Chapter 8

Modeling of linearity related quantities in BJTs

8.1 Introduction

In this chapter the effect of the base-collector capacitance on the linearity performance of bipolar devices will be investigated. As was shown in Section 2.2, different distortion contributions tend to dominate at different bias conditions. In the experiments described next the impact of the exponential distortion that dominates the linearity behavior of bipolar devices at lower current levels will be reduced by the use of the out-of-band cancellation method. When the exponential distortion has been cancelled, it will be shown that the next dominating distortion contribution for bipolar devices, is due to the non-linear base-collector capacitance. Since it is known that the behavior of the base-collector capacitance of bipolar transistors in III-V technologies is different from a device made in silicon technologies [108], this opens the question whether different material systems will have different linearity performance. In order to answer this question in this chapter the linearity behavior of SiGe and GaAs HBTs will be investigated. The choice for these technologies is made based on their dominant position in the handset RF PA market.

The differences in linearity performance between these technologies will be discussed in relation to their behavior of the base-collector capacitance. Physical device simulations (TCAD) are utilized to provide insight and additional support in order to relate the behavior of the base-collector capacitance to the large-signal linearity behavior of the bipolar device.

8.2 Overview of differences between Si/SiGe and GaAs technologies

From literature various differences between Si/SiGe and GaAs technologies are known. The most well known difference is found in the f_t characteristics, where the f_t of

the GaAs devices shows a peak, which does not occur in Si/SiGe devices. This f_t-peak is associated with a sudden reduction in base-collector capacitance. This reduction can be attributed to the electron velocity modulation [109, 110]. In GaAs materials the electron velocity, which is a function of the electric field, has the highest value for relative low electric fields and has a negative slope for high electric fields (Fig. 8.1). It is this phenomena that causes the velocity of electrons to strongly depend on the electric field distribution in the epilayer, which, in turn, modulates the electron concentration. As a result, in GaAs devices the electron concentration becomes reduced, just before the bipolar device enters quasi saturation, yielding a reduction of the base collector capacitance. It will be shown experimentally that this behavior tends to yield a more constant behavior of the base-collector capacitance in the output plane. Since the base-collector capacitance acts like a feedback element, and in that sense defines the transfer function, its dependency on the output voltage and current direcly impacts the linearity of the bipolar device.

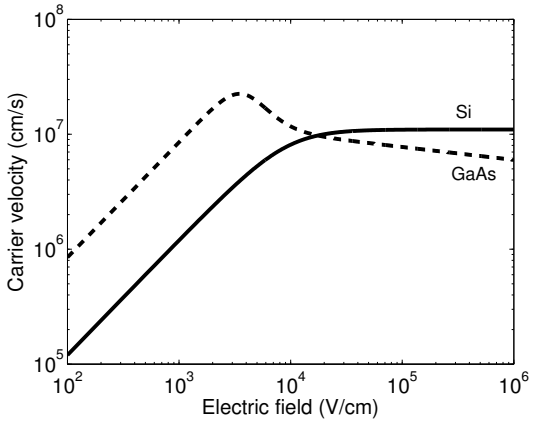


Figure 8.1: Typical carrier velocity dependency on the electric field for silicon or GaAs materials [111–113].

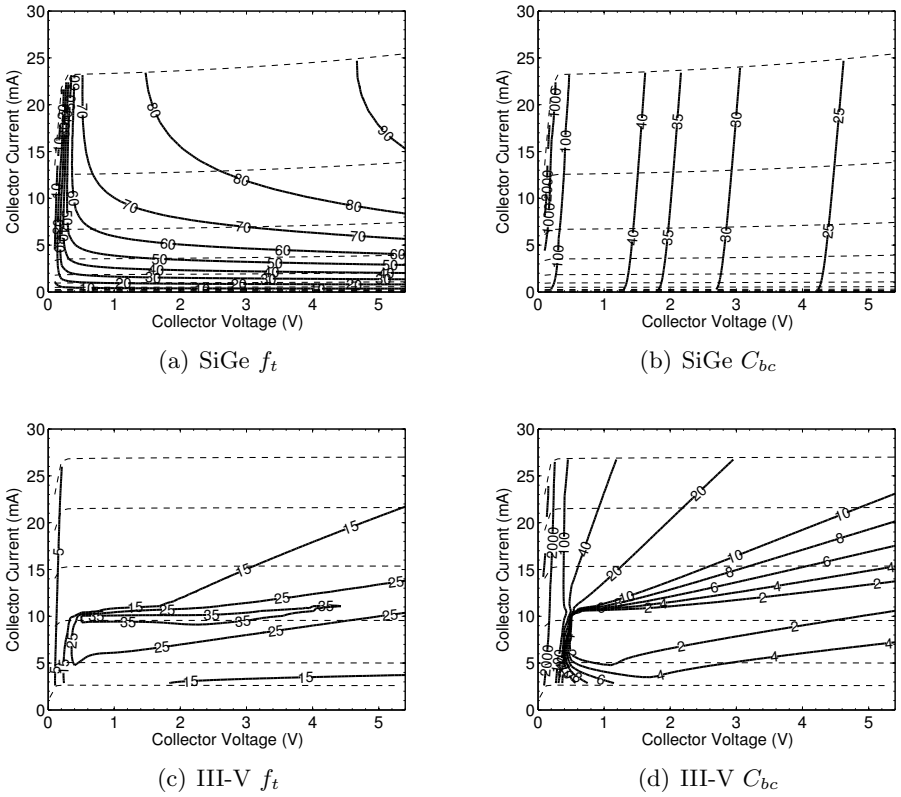
8.3 Physical device simulations of HBT devices

For the investigation of the small-signal behavior, specifically the related f_t and base-collector capacitance behavior of SiGe and III-V devices, first the intrinsic one-dimensional devices are simulated using Medici [114]. The applied models and model-parameters are given in Appendix C. The typical C_{bc} behavior of III-V devices depends on the exact realization of the collector; e.g. specifically graded [115] or step dopings can be applied to influence, or suppress III-V like effects on the C_{bc}. Therefore, devices were chosen with relatively simple collector profiles, i.e. with uniform and not too high doping ($\sim 1.10^{16}$–3.10^{16}), which exhibit a reduction in C_{bc} for bias conditions relevant for power amplifier applications.

The simulated III-V device structure is based on reference [116]. The SiGe device is a fictional, typical high speed device with similar dimensions as the III-V device.

The resulting $f_t(I_c, V_{ce})$ dependence is given in Fig. 8.2(a). The related C_{bc} behavior is given in Fig. 8.2(b) on the $I_c(V_{ce})$ plane for the SiGe bipolar device. It can be noted, that the f_t increases with voltage and current, whereas the C_{bc} is mostly a function of the applied collector-base voltage. In Fig. 8.2(c, d) the f_t and C_{bc} of a typical III-V device are given. In the III-V case and SiGe case an uniform collector doping of 2.10^{16} cm^{-3} and 1.10^{17} cm^{-3}, respectively, in combination with a highly doped (10^{19} cm^{-3}) buried layer were applied. The higher doping level in the collector of the SiGe device was chosen to follow the trend in SiGe devices, where breakdown is sacrificed to gain speed.

Note, that for the III-V device a sharp minimum is visible in the $C_{bc}(I_c, V_{ce})$ as was discussed in Section 8.2. Furthermore, an area with very low capacitance variation can be identified, as was already shown in [117]. These results illustrate the pronounced differences between SiGe and III-V devices.



(a) SiGe f_t (b) SiGe C_{bc}

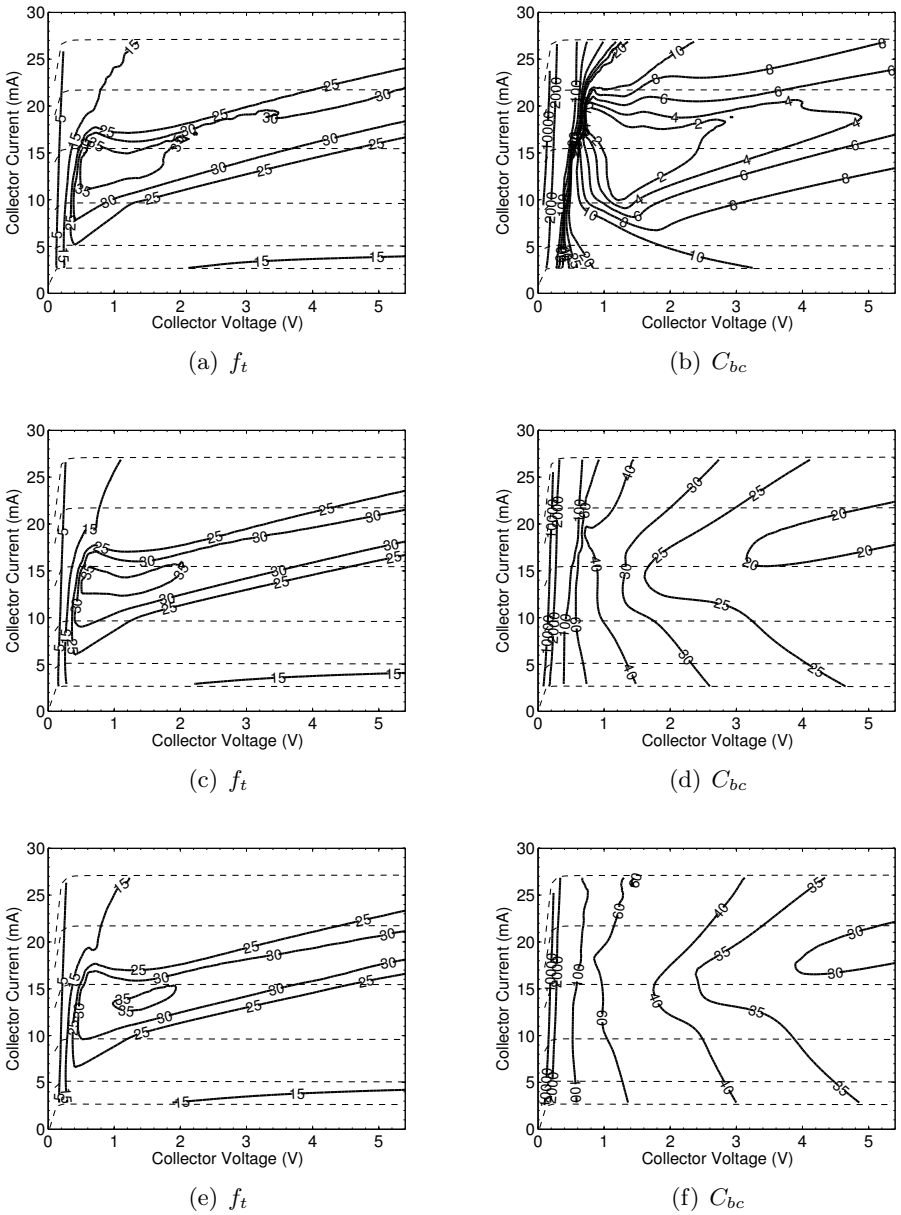
(c) III-V f_t (d) III-V C_{bc}

Figure 8.2: Extracted (a, c) f_t (GHz) and (b, d) C_{bc} (fF) contours at 1 GHz from simulated y-parameters in Medici of an 1-D SiGe (a, b) and III-V (c, d) device as function of collector current and collector voltage. Both devices have an emitter area of 1 μm^2.

Since the SiGe C_{bc} is only weakly current dependent, two-dimensional simulations are only performed for the GaAs devices. Because the intrinsic and extrinsic region have a different capacitance behavior, i.e. only the intrinsic region is strongly current dependent, the behavior of the total base-collector capacitance will differ from the 1-D approximation. If the intrinsic region is defined as the part of the device where the main vertical current flows below the emitter, then current spreading changes the ratio between the intrinsic and extrinsic region. As a result, the sharp minimum as shown in Fig. 8.2(c, d) will be smoothened. Simulation results including the influence of the extrinsic region, are given in Fig. 8.3. In GaAs devices, however, due to their mesa-structure, the extrinsic region is relatively large. In fact the ratio between extrinsic and intrinsic region $C_{bc,ext}/C_{bc,int}$, can be as high as four–six. Therefore, simulations with these high ratios are also presented in Fig. 8.3. Consequently, from the figures (8.2) and (8.3) three conclusions can be drawn. Firstly, the C_{bc} minimum lies along a straight line, slightly inclined with voltage. Secondly, below the current level associated with peak f_t, the f_t decreases with increased collector voltage. Thirdly, the extrinsic region will mask the sharp C_{bc} minimum as predicted by the one-dimensional simulations.

When comparing these III-V simulation results with device measurements, it can be concluded that the trend seems to be correct. In Fig. 8.4(b) the total measured C_{bc}, and in Fig. 8.4(a) the transit frequency (f_t) behavior of a 9.68 μm^2 Skyworks III-V device are shown over the output bias plane. Note, that the peak f_t and the minimum in C_{bc} follow indeed a slightly inclined line with collector voltage and the f_t for a given current level drops with increased collector voltage, as was predicted by the physical device simulations.

To complete the comparison between Si/SiGe and GaAs HBTs also measured data of a QUBiC device is shown. In Fig. 8.5 the f_t and C_{bc} are presented. As one can observe from this data the SiGe device behavior is fundamentally different from that of the GaAs HBT (Fig. 8.4). In the case of the SiGe device the C_{bc} is mainly voltage dependent, while its f_t keeps increasing with both higher voltage and current, as was also expected from the physical device simulations. Models that describe these differences between Si/SiGe and GaAs exist and are able to capture the current dependency of the f_t and C_{bc} of GaAs HBTs. Examples can be found in [108, 118, 119].

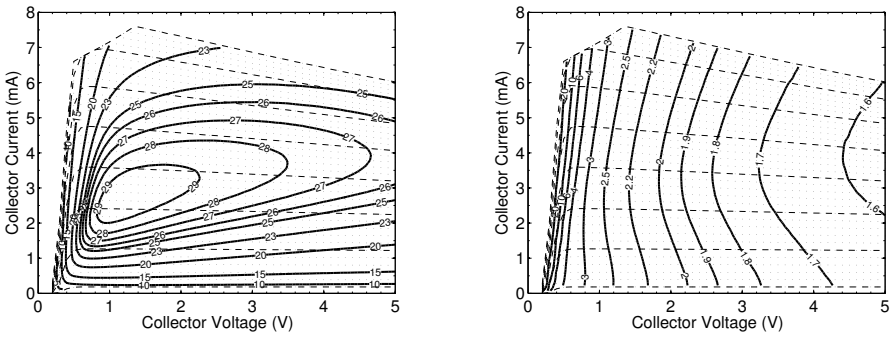


(a) f_t (b) C_{bc}

(c) f_t (d) C_{bc}

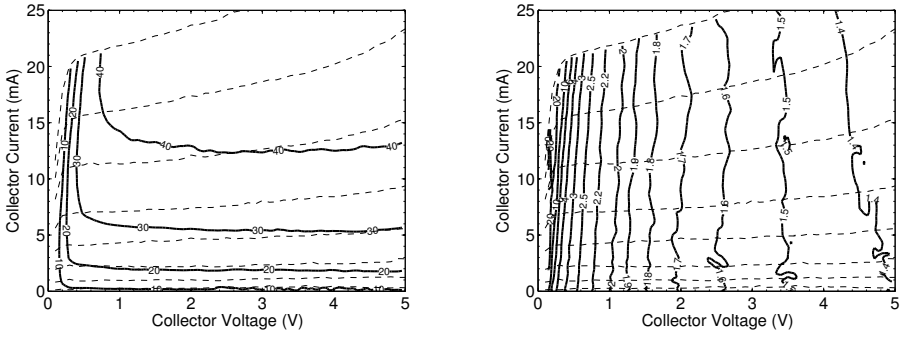
(e) f_t (f) C_{bc}

Figure 8.3: Extracted (a, c, e) f_t (GHz) and (b, d, f) C_{bc} (fF) contours for the III-V device 2-D simulations, where the area of the extrinsic region is (a, b) equal to the intrinsic region, (c, d) four times the intrinsic region and (e, f) six times the intrinsic region. The emitter area is kept constant and is 1 μm^2 for all simulations.



(a) (b)

Figure 8.4: (a) Extracted f_t (GHz) contours and (b) C_{bc} (fF/μm^2) contours at 2 GHz from deembedded measured s-parameters of a 2.2 by 4.4 μm, base current driven III-V device as function of collector current (dots) and collector voltage.



(a) (b)

Figure 8.5: (a) Extracted f_t (GHz) contours and (b) C_{bc} (fF/μm^2) contours at 2 GHz from measured s-parameters of a 44.5 μm^2 voltage driven SiGe device as function of collector current and collector voltage.

8.4 Investigation of the various HBT non-linearities using model linearization

In Section 2.2.1 the influence of various non-linear phenomena of the bipolar device were discussed and the bias conditions for which they dominate where indicated in the $I_c(V_{ce})$ plane. Here, the impact of these non-linearities will be investigated in more detail. For this purpose a compact model of a single transistor will be modified, such that it allows to linearize certain non-linear contributions by selection. The applied voltages consist of both DC and AC contributions. In this case the model will be linearized around the applied DC bias point. Since verilog-A [21] gives the possibility to easily modify models, certain non-linear contributions can be omitted by linearizing the function of interest around its quiescent point. The starting point is a branch current I_{br}, given by:

$$I_{br} = I_x(V_1, V_2, ..., V_n) + \frac{dQ_x(V_1, V_2, ..., V_n)}{dt}, \tag{8.1}$$

from which the small signal conductances $\delta I_n/\delta V_n$ and capacitances $\delta Q_n/\delta V_n$ can be derived. Or, if they (also) depend on voltages other then their own branch-voltage, transconductances and transcapacitances can be derived.These (trans)capacitances and conductances will be exploited to linearize the model.

8.4.1 Linearized dynamic currents - (trans)capacitances

In these models capacitances are described by their charge behavior. The dynamic current can be expressed as:

$$I_Q = \frac{\delta Q}{\delta t} = \frac{\delta Q}{\delta V}\frac{\delta V}{\delta t}, \tag{8.2}$$

which for a charge, dependent on two variables, V_1 and V_2, can be written as:

$$I_Q = \frac{\delta Q(V_1, V_2)}{\delta t} = \frac{\delta Q(V_1, V_2)}{\delta V_1}\frac{\delta V_1}{\delta t} + \frac{\delta Q(V_1, V_2)}{\delta V_2}\frac{\delta V_2}{\delta t}. \tag{8.3}$$

This gives the opportunity to linearize the charge by substituting the original functions through linearization around the DC bias point (V_{1DC}, V_{2DC}):

$$I_Q = \frac{\delta Q(V_1, V_2)}{\delta t} = \frac{\delta Q(V_{1DC}, V_{2DC})}{\delta V_{1DC}}\frac{\delta V_1}{\delta t} + \frac{\delta Q(V_{1DC}, V_{2DC})}{\delta V_{2DC}}\frac{\delta V_2}{\delta t}. \tag{8.4}$$

This can be done for all charges present in the model. Consequently, the base-collector and base-emitter capacitance in Mextram can be linearized this way; details on the resulting Verilog-A code are given in Appendix B, which exploits the automatic differentiation of Verilog-A to calculate the linearization.

8.4.2 Linearized currents - (trans)conductances

In a similar fashion the currents can also be linearized. If the DC solution is known, a current can be expressed as:

$$I = I_{DC} + \frac{\delta I}{\delta V}V. \tag{8.5}$$

In which $\delta I/\delta V$ represents the linearization, resulting in a small signal conductance. This linearization can be done around a defined bias point:

$$I = I_{DC} + \frac{\delta I_{DC}}{\delta V_{DC}} V. \tag{8.6}$$

The resulting Mextram Verilog-A implementation to linearize the transfer current I_n is given in Appendix B.

8.4.3 Simulations using a linearized Mextram model

In Fig. 8.6(a) the simulated OIP3 of the original unlinearized full Mextram model of a SiGe Qubic [120] device is presented. Then the linearized simulation results are given in Fig. 8.6(b) for the linearized exponential behavior of I_c, in Fig. 8.6(c), for the linearized C_{bc} and in Fig. 8.6(d), for the linearization of both C_{bc} and for the exponential behavior of I_c. The regions where the resulting $OIP3$ is significantly different from the original simulation, i.e. $\Delta OIP3 > 3$ dB, are indicated. The input signal used for this simulation is small (here -50 dBm in a 50 Ω environment). Note, that this exercise only gives an indication of those regions, since due to second-order mixing the various non-linearities can interact, yielding changes in the resulting $IM3$ level, as presented in Section 2.3. To remove this secondary interaction, the simulation is repeated using frequency dependent terminations, where at both input and output the baseband and higher harmonic impedances are shorted. The fundamental terminations were kept at 50 Ω. The results are presented in Fig. 8.7. Clearly, from Fig. 8.7(b-d) the regions where different linearities dominate can be identified.

The different dependencies of the non-linearities can be seen from the slope of the $OIP3$ contours. Horizontal contours indicate current dependencies, whereas vertical contours indicate voltage dependencies. When the C_{bc} is linearized the voltage dependency nearly disappears; when the transfer current gets linearized the current dependency reduces. Linearizing both, results in a far more linear device operation, over a large bias plane. Note, that linearizing the transfer current I_n is quite similar to applying $IM3$ canceling for the exponential behavior, as can be implemented for specific bias points using the out-of-band cancellation technique (Section 2.3). Note, that out-of-band cancellation linearizes the non-linear contribution of C_{be}. So far, this has not been considered. Therefore, Fig. 8.8 presents the results for the linearized C_{be} case. Consequently, out-of-band cancellation can provide better linearity compared to removing a single contribution like I_n, since even though I_n has been removed, other contributions to distortion are still present, e.g. I_b, C_{be}. Nevertheless, all simulations (Fig. 8.7 and 8.8) indicated that, when using out-of-band cancellation, even better linearity can be achieved if the base collector capacitance behaves linear. Note, that this basically represents the case for GaAs HBTs as demonstrated in Section 8.3.

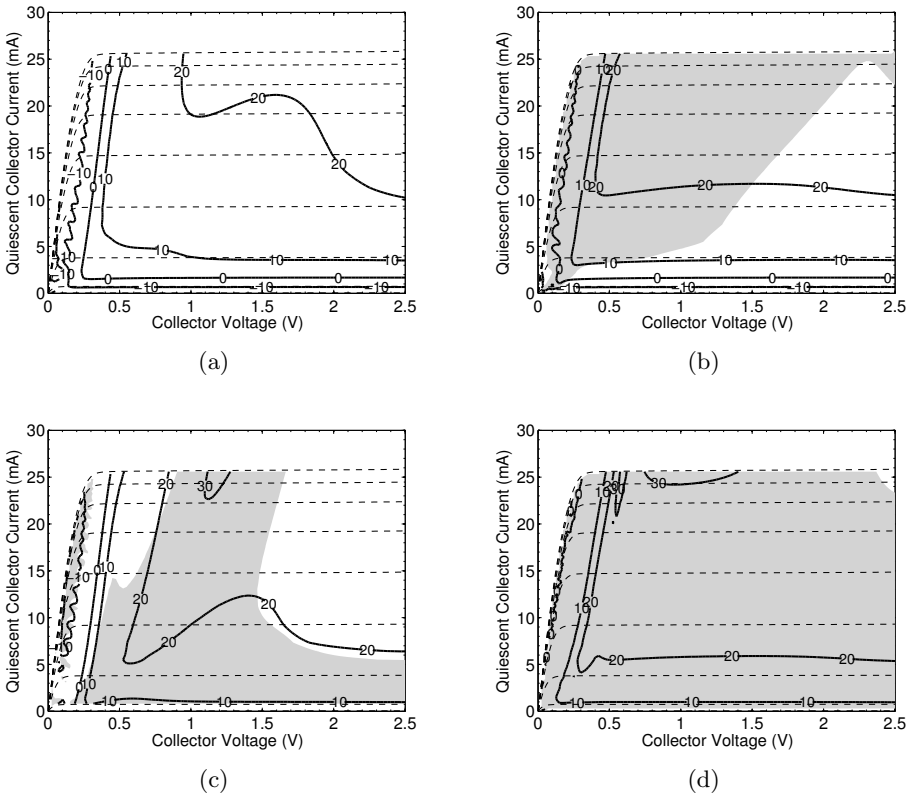


Figure 8.6: Simulated contours of constant $OIP3$ (dBm) plotted in the $I_c(V_{ce})$ plane for a Qubic bipolar device in CE configuration with 50 Ohm input and output impedance at 2 GHz using an input power level of -50 dBm. (a) Full Mextram model of the QUBiC device, (b) Mextram model with linearized C_{bc}, (c) Mextram model with linearized transfer current I_n and (d) Mextram model with both linearized C_{bc} and I_n. The gray area indicates where the linearity improvement ($\Delta OIP3$) is larger than 3 dB.

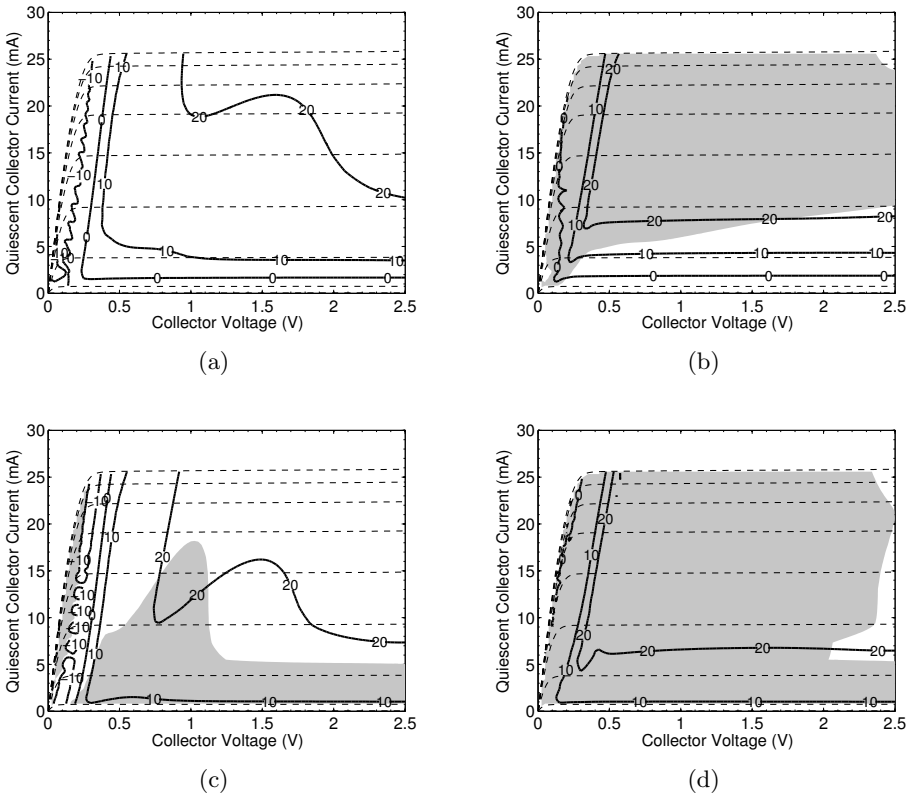


Figure 8.7: Simulated contours of constant $OIP3$ (dBm) plotted in the $I_c(V_{ce})$ plane for a Qubic bipolar device in CE configuration with 50 Ohm input and output impedances at 2 GHz, where the baseband and harmonic impedances are shorted at both input and output. Using a (a) Mextram model of the QUBiC device, (b) Mextram model with linearized C_{bc}, (c) Mextram model with linearized transfer current I_n and (d) Mextram model with both linearized C_{bc} and I_n. The gray area indicates where the linearity improvement ($\Delta OIP3$) is larger than 3 dB.

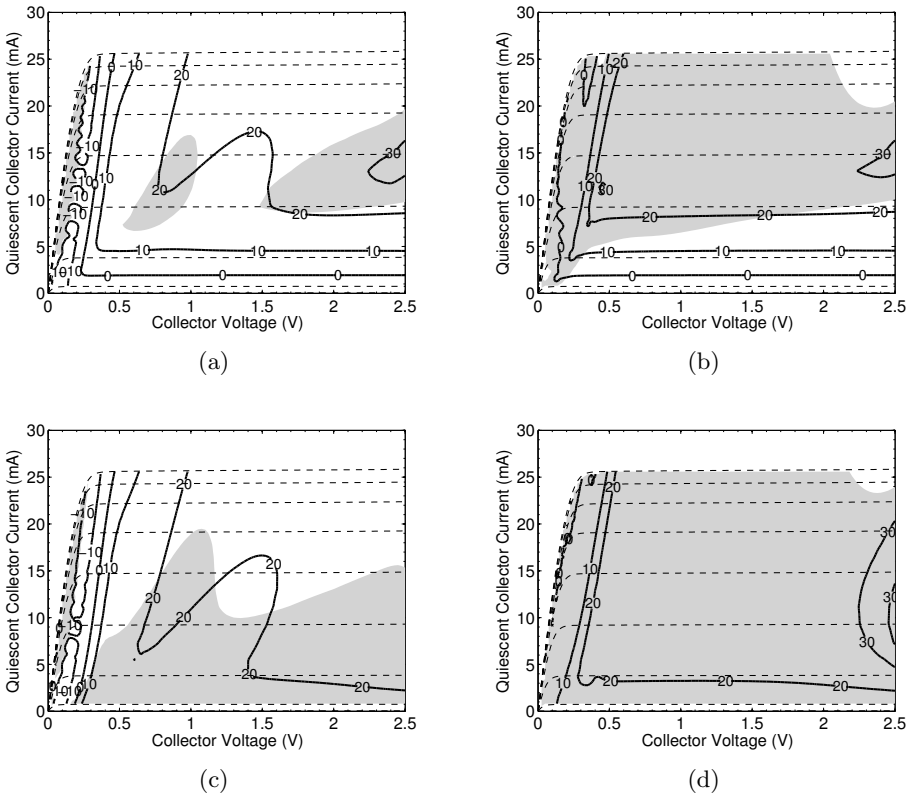


Figure 8.8: Simulated contours of constant $OIP3$ (dBm) plotted in the $I_c(V_{ce})$ plane for a Qubic bipolar device in CE configuration with 50 Ohm input and output impedances at 2 GHz, where the baseband and harmonic impedances are shorted at both input and output. Using a (a) Mextram model of the QUBiC device with linearized C_{be}, (b) Mextram model with linearized C_{bc} and C_{be}, (c) Mextram model with both linearized transfer current I_n and C_{be} and (d) Mextram model with linearized C_{be}, C_{bc} and I_n. The gray area indicates where the linearity improvement ($\Delta OIP3$) is larger than 3 dB, compared to Fig. 8.7(a).

8.5 Conclusion

In this chapter some basic differences between SiGe and GaAs bipolar technologies, due to the base-collector capacitance, have been identified using both simulations and measurements. It was shown that the behavior of the base-collector capacitance is fundamentally different for GaAs devices when compared to Si/SiGe devices. This phenomena finds its origin in the different behavior of the electron velocity for GaAs, which yields a more constant base-collector capacitance versus collector current and collector emitter voltage than for comparable SiGe devices. The importance of the base-collector capacitance for the overall linearity performance of the active device was shown using a linearized Mextram model. In the following chapter the influence of these effects on bipolar device linearity will be experimentally investigated.

Chapter 9

Experimental high power out-of-band linearity optimization of BJTs

9.1 Introduction

This chapter discusses the use of out-of-band linearization techniques at higher power levels, i.e. power levels up to the compression of the device. The general theory for out-of-band linearization was discussed in Section 2.3. This theory will now be extended to a fifth-order Volterra series valid up to the compression point of the device. This approach is based on the theory introduced by Van der Heijden [24]. The theory will be supported in Section 9.3 by simulations using the Mextram model and experimentally verified in Section 9.4. The main focus of this study is on determining the influence of the base-collector capacitance from the resulting linearity when operating the device up to its compression point.

9.2 Theory of high power out of band linearity optimization

The third-order Volterra series optimization, as presented in Section 2.3, provides the optimum combination of bias, base-band and second-harmonic impedance for linearity. When extended to higher power levels, however, this basic theory does not hold, since harmonics with an order larger than three start to become important.

By increasing the order of the Volterra series, the validity range can be extended up to higher power levels, at the expense of increased complexity of the equations. This analysis was originally performed in [24] and these results will be utilized here.

For low-power conditions the linearity of a bipolar transistor can be investigated using a number of simplifications to ease the Volterra calculations, this is possible since the exponential behavior of the device will dominate the distortion contribution.

For low power levels it was found that the optimal out-of-band impedance occurs for $Z_{s,bb} = Z_{s,2f} = \beta/2g_m$. At the same time, at a specific current level the influence of the non-linear base-emitter diffusion capacitance C_d is cancelled if $I_c = C_d V_t/2\tau_f$ [121]. Therefore, for a specific BJT, the frequency independent $IM3$ cancellation condition [26] fixes bias current, baseband impedance and harmonic impedance at the source, while at the same time shorted harmonics and baseband are preferred at the load.

Without out-of-band $IM3$ cancellation the $IM3$ is limited by the third order contribution, which is equal to zero for the out-of-band canceling condition $Z_s = Z_{s,bb}, Z_{s,2f} = \beta/2gm$ at a specific current. At higher power levels it is necessary to expand the Volterra series to include contributions up to fifth order. Now, multiple distortion components contribute to the $IM3$ products at $2f_2 - f_1$ and $2f_1 - f_2$. At these higher power levels, after applying out-of-band $IM3$ cancellation, the remaining $IM3$ will be limited by the 5^{th} order contribution, which is given by [24]:

$$H5 = \frac{g_m}{270V_T^4} \frac{1 + j\omega Z_s(\omega_0)2\tau_f g_m}{[1 + Z_s(\omega_0)(g_\pi + j\omega C_\pi]^6} \tag{9.1}$$

The third order transfer function $H3$ is zero for the optimal $Z_{s,bb}, Z_{s,2f}$ and changes sign as function of $Z_{s,bb}, Z_{s,2f}$, therefore, a region is expected to exist where $H3$ and $H5$ have opposite signs. From [24] it is concluded that $H3$ and $H5$ are 180 degrees out of phase for $Z_{s,bb} > \beta/2g_m$. Therefore, in this region for a specific input power $IM3$ cancellation can occur, yielding so-called $IM3$ sweet-spots.

This phenomenon will be studied in the following section, using a simulator with a representative bipolar model. The following procedure will be applied in both the simulator (Section 9.3), and in the experimental verification (Section 9.4):

- Optimize the device for the highest PAE using single-tone excitation to find Γ_{source} and Γ_{load} at the fundamental frequency;

- Sweep the real part of $Z_{s,bb}$ and $Z_{s,2f}$ over a wide range, while at the same time sweeping V_{be} at low RF input power to find the optimal I_{cq} and $Z_{s,bb}$ and $Z_{s,2f}$ for linearity. At the same time $Z_{l,bb}$, $Z_{l,2f}$ and higher harmonics at the load are shorted. $Z_{s,f}$ and $Z_{l,f}$ were already found in the previous step. This measurement is performed under two-tone excitation and the $IM3$ components are evaluated to find the optimal point for best linearity performance;

- Apply a two-tone excitation with swept input power and V_{be} to find the optimum linearity locus up to the 1 dB compression point, using the impedances found in the previous steps.

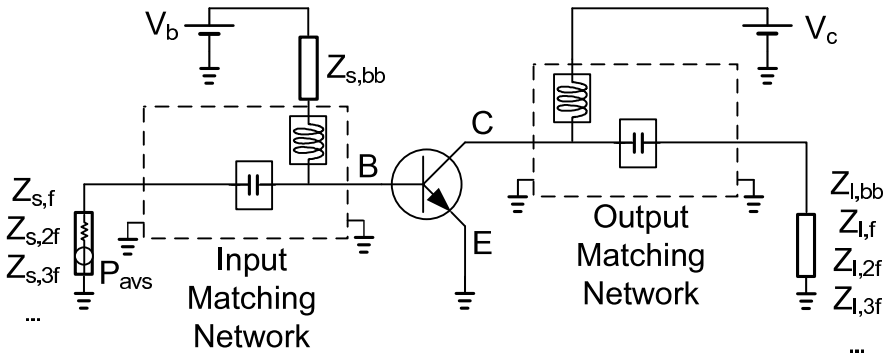


Figure 9.1: Common emitter (CE) stage of generic bipolar device as applied in the simulator, the biasing is done using ideal dc-blocks and dc-feeds. In practical realizations these will be included in the matching networks.

9.3 Simulations of high power out-of-band linearity optimized HBT devices

The configuration as given in Fig. 9.1 is simulated. In a practical realization of this circuit, the matching network at in and output provides the impedances for fundamental and second harmonics, whereas a resistor in the base-bias connection sets the baseband impedance. It should be noted that any inductance in the base-bias connection should be low, to avoid providing a complex base-band impedance that may lead to asymmetry in the $IM3$ products. At the output, special care has to be taken to properly set the baseband impedance (mostly close to a short), which will also depend on the realization of the bias circuitry. The quiescent collector current is set by the value of the base voltage V_b and flows through the baseband resistor. The quiescent current is chosen such that the device operates in class-AB mode. The collector voltage is chosen such that the RF voltage and current swing does not reach too far into the strong saturation region. This is specifically done to avoid the strong increase of the base-collector capacitance in this region, such that the linearity can maximally profit from the relatively flat C_{bc}-area of the III-V HBTs, as presented in Section 8.3.

Several cases are simulated according to the procedure given in Section 9.2; a short overview is given here:

- Simulations with full compact model using optimized impedances:
  - optimized at P_{in}= -60 dBm;
  - optimized at P_{in} ∼-26 dBm, as will be necessary in the measurement system, due to noisefloor limitations (Section 9.4);
  - mismatched source impedance at higher input power ∼-26 dBm, as will be discussed in Section 9.4.

- Simulations with full compact model with linearized C_{bc}, using optimized impedances:
  - optimized at P_{in}= -60 dBm.

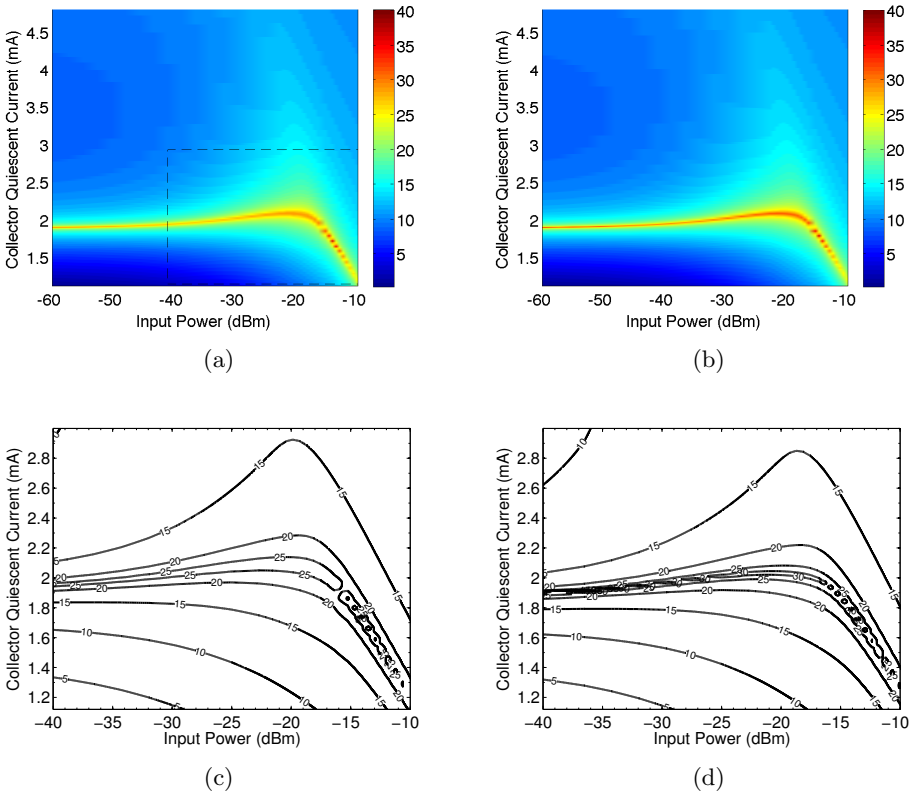


Figure 9.2: Simulated $OIP3_{hi}$ (dBm) contours from a harmonic balance simulated Qubic bipolar device at 2 GHz versus input power and collector quiescent current for (a) optimized at P_{in}= -60 dBm with $Z_{s,f}$=12 Ω, $Z_{s,bb,opt}$=$Z_{s,2f,opt}$ =1245.7 Ω, (b) $OIP3_{lo}$ using same conditions as (a), (c) zoomed in on the interesting region of Fig. 9.2 (a), (d) optimized at P_{in}= -26 dBm with $Z_{s,f}$=12 Ω, $Z_{s,bb,opt}$=$Z_{s,2f,opt}$ =1540.1 Ω.

In Fig. 9.2 the simulations results are presented. The bias current for which canceling occurs is clearly visible. This optimum combination of bias current and power level will be referred to as the ideal locus for $IM3$. Fig 9.2(a) shows the $OIP3_{hi}$. The $OIP3_{hi}$ in this figure first increases somewhat with quiescent current, but when approaching the 1dB compression point of the device, the locus of ideal $IM3$ drops with quiescent current. To demonstrate that the proper canceling point has been chosen in 9.2(b) the $OIP3_{lo}$ is presented, which has the same behavior and nearly the same magnitude as the $OIP3_{hi}$. To further investigate the ideal locus Fig. 9.2(c)

zooms into the region up to the compression point. During the real measurements (Section 9.4) it is not possible to optimize at such low power levels as we use in the simulator, therefore the optimization will actually be performed in the region where the locus already deviates from the low power result. To illustrate this influence on the locus, the resulting $OIP3$ is presented in Fig. 9.2(d). Clearly the locus still follows the same behavior, however the found ideal impedance $Z_{s,bb,opt}$=$Z_{s,2f,opt}$ =1245.7 Ω differs from the value found in this case: 1540.1 Ω. Also the $OIP3$ differs somewhat.

Due to measurement constrains on an active harmonic loadpull system, with respect to the noisefloor (Section 9.4), the input of the device may be unmatched. The resulting $OIP3$ contours for $Z_{s,f}$=50 Ω, optimized at P_{avs}=-18 dBm, are given in Fig. 9.3.

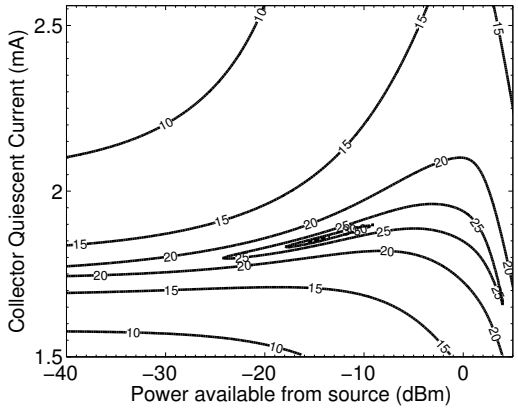


Figure 9.3: Simulated $OIP3$ (dBm) contours from harmonic balance simulations at 2 GHz with $Z_{s,f}$=50 Ω of a Qubic bipolar device versus input power and collector quiescent current.

9.4 Characterization of high power out of band linearity optimization

In this section experimental results measured on an Active Harmonic Load Pull[1] (AHLP) measurement setup will be presented. The system used is described in [25, 123] and is capable of actively controlling the impedances offered to the device under test at the fundamental and second harmonic frequencies at both input and output of the device over a wide bandwidth (up to 160 MHz). At the same time it is also capable of passively controlling the baseband impedance using real impedances ranging from 0.5 to 2048 Ω. A simplified schematic of the measurement system is given in Fig. 9.4. The system capabilities to control the various impedances make it the ideal tool to verify the results presented in the previous section.

The study will be completed by comparing the measured linearity results with specific small signal measurements. As shown in Section 8.4, after canceling exponential distortion, the base-collector capacitance becomes dominant for the linearity. Therefore, the variation of C_{bc} over the loadline gives an indication for the expected level of distortion. Consequently, by comparing the C_{bc} variation over the loadline to the measured non-linearity, while applying the proper out-of-band terminations, conclusions can be drawn with respect to the suitability of different devices and technologies for linear power amplifier applications. In support of the above, four different bipolar devices of different technologies are analyzed, a description of these devices is given in the next section.

9.4.1 Description of investigated devices

The investigated devices are heterojunction bipolar transistors (HBT), namely one SiGe HBT and three GaAs HBTs, some basic parameters of the measured devices are given in Table 9.1. Note, that due to the higher maximum current density capabilities of GaAs devices, the size of the GaAs devices is chosen to be about half the size of the SiGe device.

Table 9.1: Overview of the studied device used in the linearity characterization

	Technology	Size (μm^2)	Measured Peak f_t (GHz)	Remarks
A	SiGe (C) [120]	99	∼45	
B	GaAs (AlGaAs*) [116]	48.4	∼43	0.7 μm epi
C	GaAs (AlGaAs*) [116, 124]	48.4	∼35	1 μm epi
D	GaAs (InGaP) [125]	44	∼100	very high R_{th}

* Devices are identical, except for the realization of their collector.

For a description of the SiGe device A, the reader is referred to [120]. The GaAs

[1] For more information the reader is referred to work of Marchetti [122].

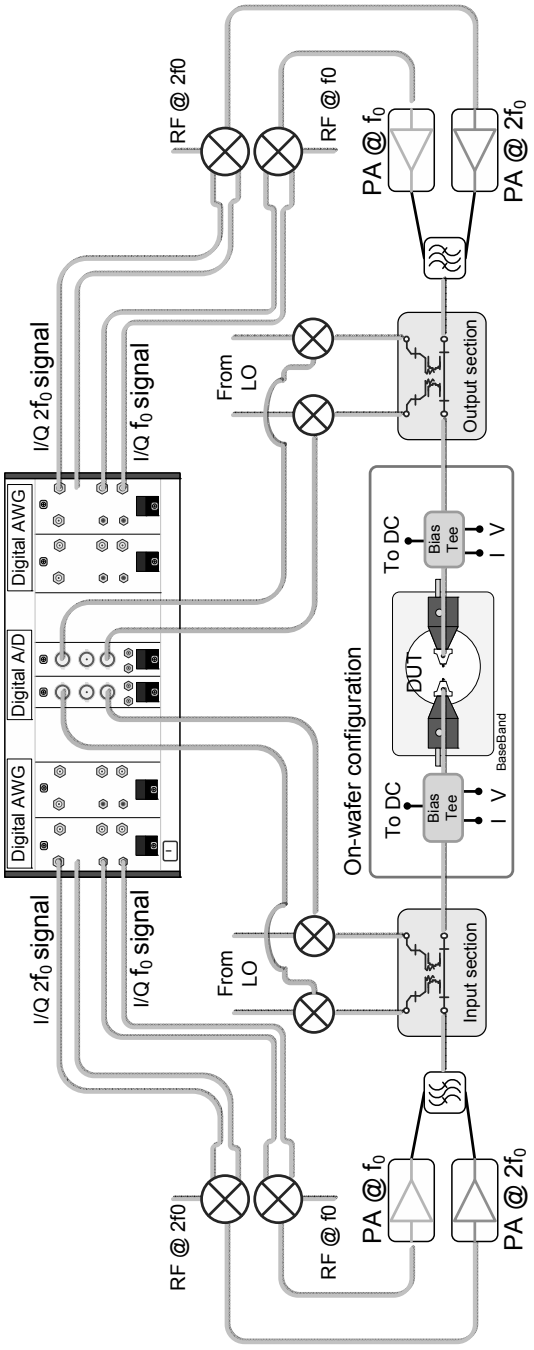


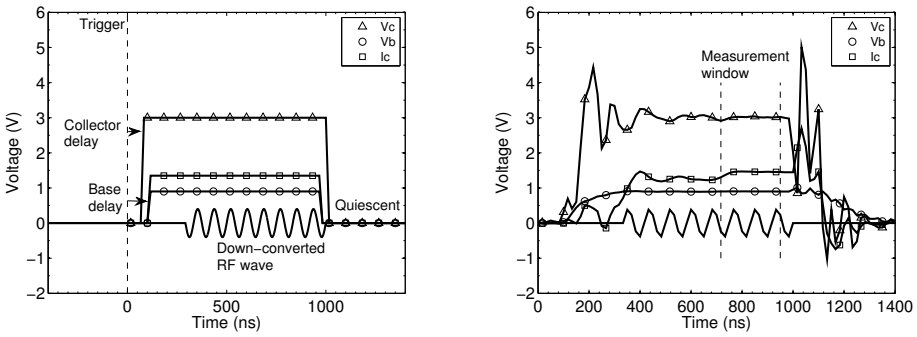
Figure 9.4: Simplified schematic of the active harmonic load pull measurement system. Courtesy of M. Marchetti.

devices have either an AlGaAs or InGaP emitter. A short description of the layer structure of device B and C is given here, starting at the bottom. Both devices are epitaxial grown by MOCVD and consist of a highly doped GaAs sub-collector, followed by a 7000-10000 Å uniformly doped collector (1×10^{16} cm^{-3}), 1370 Å base (4×10^{19} cm^{-3}), 525 Å $Al_{0.25}Ga_{0.75}As$ emitter (4×10^{17} cm^{-3}), followed by a 200 Å $Al_{0.25}Ga_{0.75}As$ ramp to GaAs (4×10^{17} cm^{-3}), covered with a 1500 Å, 8×10^{18} cm^{-3} layer of GaAs and a highly doped InGaAs cap layer. Device C has the same structure as device B. The drift-collector of device B is 7000 Å with an extra non-uniform doping from 1×10^{16} to 5×10^{18} cm^{-3} towards the sub-collector, whereas the drift-collector of device C is 10000 Å .

Device D has an InGaP emitter, and is grown by MOCVD as well. The device consists of a highly doped sub-collector, a two-step collector from high at the sub-collector to low near the base. The 500 Å base is doped 4×10^{19} cm^{-3}, followed by a 400 Å, 3×10^{17} InGaP emitter, covered with a 1200 Å, 4×10^{18} cm^{-3} layer of GaAs and a highly doped InGaAs cap layer.

For the GaAs devices, the wafer has been thinned down to reduce the thermal resistance, with exception of device D. Since the thermal resistance of GaAs is high compared to silicon [37], it is necessary to characterize the devices under pulsed conditions. This is much less an issue during the linearity measurements, since the total power dissipation will be lower in these situations. The reason for this is the following; during the single-tone device characterization, the device must be characterized up to its maximum RF voltage/current swing, which by far exceeds the DC voltage/current conditions during the linearity measurement. The devices were measured under pulsed conditions using the pulsed RF/IV measurement system, as presented in [98]. The devices were measured at a frequency of 2 GHz, the input power provided to the device was -24 dBm at the device plane, and the collector pulse width was 1 μs. The base pulse was slightly shorter than the collector pulse and started just after the collector pulse to avoid biasing of the device in the saturation condition. The RF pulse width was 0.7 μs, starting 0.3 μs after the collector and a pulse period of 1 ms was used for all measurements. All quantities, the base and collector voltage and current as well as the down-converted RF waves, were measured from 717 ns to 950 ns after the start of the pulse and averaged over this interval (Fig. 9.5). The voltage level during the quiescent of the pulse, i.e. the non-pulsed part of the period, was 0 V at both base and collector. The measured pulse characteristics are presented in Fig. 9.5(b). To suppress overshoot on the base pulse, which can potentially be destructive to a device, a low-pass RC filter was included in the bias line close to the device.

From the measured S-parameters the f_t was extracted. These measured f_t's are presented in Fig. 9.6. As was discussed in Section 8.2 and 8.3, the difference in f_t between SiGe and GaAs technologies can be seen by comparing Fig. 9.6(a) to Fig. 9.6(b–d). It can be clearly seen that the f_t of the SiGe device keeps increasing with increased voltage and current, while the f_t of the GaAs device shows a pronounced maximum.



(a) (b)

Figure 9.5: (a) Pulse timing diagram and (b) resulting measured pulses [98] as applied during the pulsed device characterization. The current has been scaled 100 times and its sensitivity therefore is 0.1A/V in this figure.

9.4.2 Linearity characterization

Following the strategy outlined in Section 9.2 the devices are first optimized for single-tone PAE, then those fundamental impedances are applied in the two-tone characterization. For the single-tone PAE actually Γ_{in}^* was applied as fundamental source impedance.

Table 9.2: Source and load impedances applied during the linearity characterization.

Device	Γ_{source}	Γ_{load}
A	Γ_{in}^* or 0.011-j*0.138	0.343+j*0.192
B	Γ_{in}^* or 0.137-j*0.182	0.228+j*0.022
C	Γ_{in}^* or 0.026-j*0.295	0.350+j*0.149
D	Γ_{in}^* or 0.011-j*0.277	0.350+j*0.149

Next, a two-tone sweep is performed at low input power levels. However, the experimental setup is limited by the system noise floor, which consists of two components, namely the lowest signal level that can be measured due to noise and the purity of the input signal. Especially the purity of the input signal is of interest, to get an accurate measurement the spectral purity of the input signal should be 20 dB better than the $IM3$ product produced by the DUT. The dynamic range of the system is 80 dB [123], which gives a useful 60 dB dynamic range for the input signal and the actively controlled impedances.

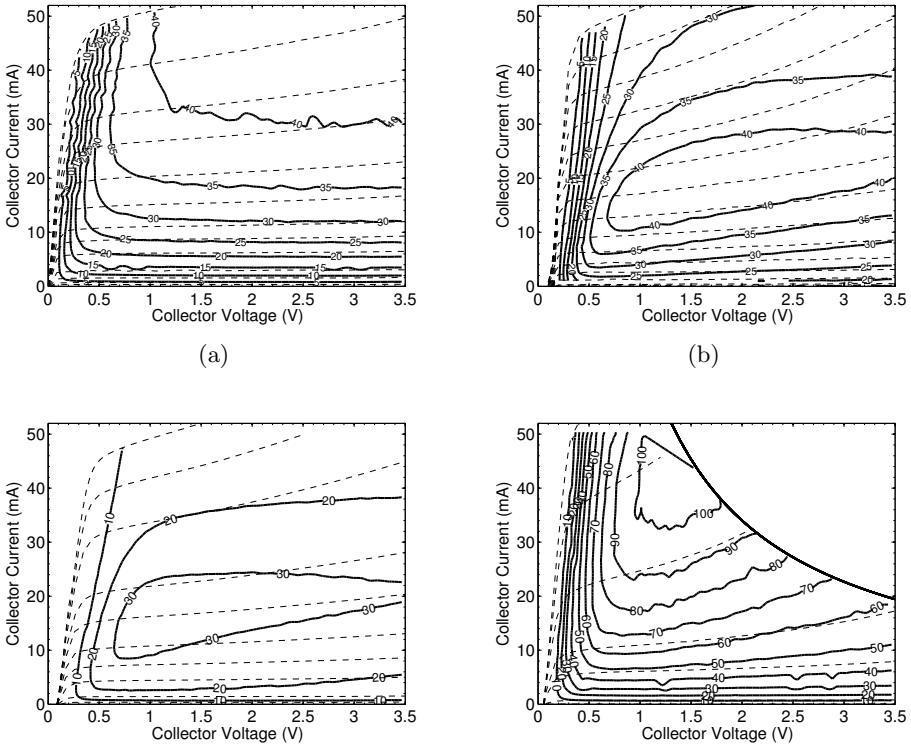


Figure 9.6: Extracted f_t (GHz) contours from measured pulsed s-parameters at 2 GHz (298 K) on the output plane for (a) device A, (b) device B (c) device C and (d) device D. The curves for device D are power limited to 68 mW*duty cycle due to the high R_{th}.

The power of the $IM3$ and $IM5$ components emanating from these small devices at the base is very low. In fact, these levels are so low that it is not possible to correctly set the impedance at input using an active loop. Therefore, during the two tone measurement, the fundamental input impedance was controlled passively. The impedances used are given in Table 9.2.

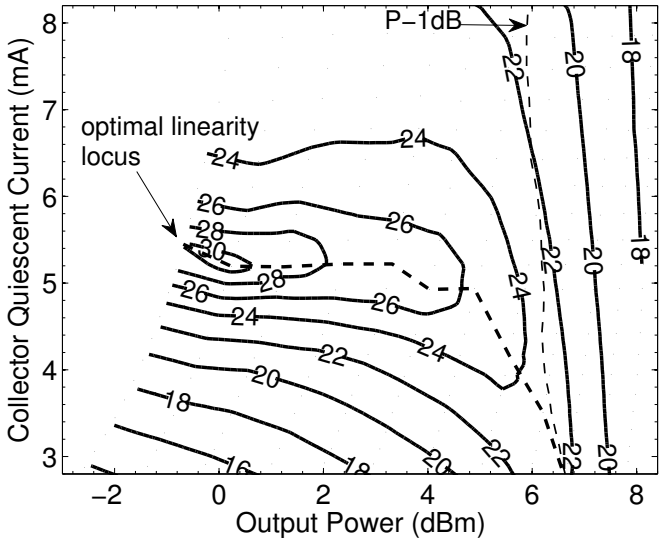
From two-tone measurements, while the baseband impedance, second harmonic impedance and base-emitter voltage were swept, the optimal combination of the external $Z_{s,bb}$, $Z_{s,2f}$ and collector current were found. The applied input power was -20 dBm. The resulting impedances and quiescent collector current are given in Table 9.3. Due to the fact, that the internal series resistances vary between the different devices, the external resistance to be added can vary considerably for achieving optimum $IM3$ cancellation. Furthermore, the differences in $Z_{s,bb}$, $Z_{s,2f}$ between the different devices can be in part also related to the different β's of the measured devices, which

are therefore also listed in Table 9.3.

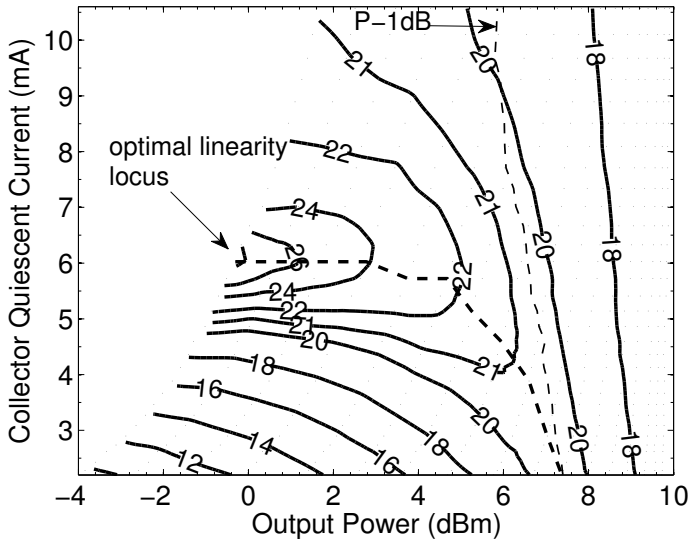
Table 9.3: Overview of optimal base-band and second-harmonic impedance and collector quiescent current.

Device	optimal $Z_{s,bb}$ and $Z_{s,2f}$	Optimal I_{cq} (mA)	β
A	432	5.4	> 300
B	7	6	~ 50
C	10	8.5	~ 50
D	256	7	> 250

Since the actual measurements are restricted by the noise limits of the measurement system, the determination of the optimal impedance and current for the bipolar devices are performed at a higher input power level, than used in the simulations of Section 9.3. Therefore the established optimum impedance and quiescent current work out to be slightly higher than the optimal values for lower input power levels (Section 9.3). Since these optimal impedances and collector quiescent currents are now known, the device can be investigated at higher power levels up to the compression point. For this the $Z_{s,bb}$, $Z_{s,2f}$ are fixed to their optimal value and the input power and and V_{be} are swept. The resulting measurements are given in Fig. 9.7 and 9.8.

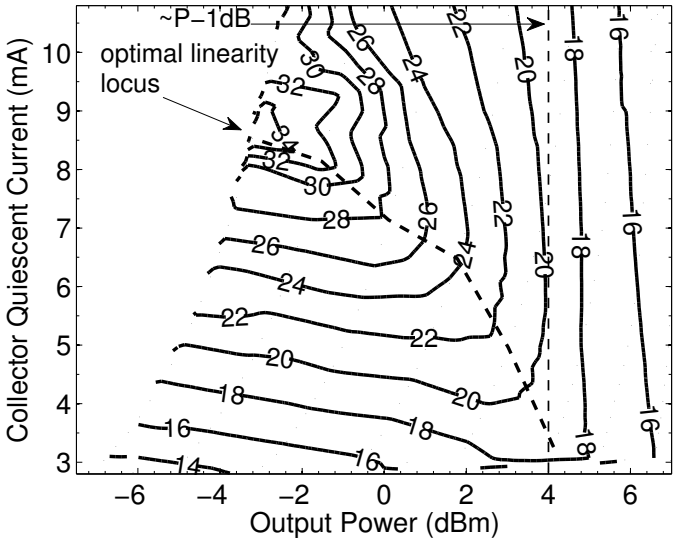


(a)

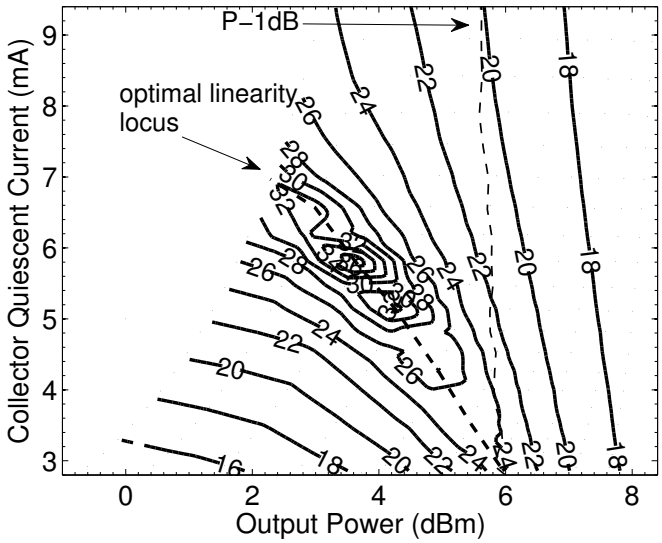


(b)

Figure 9.7: Measured OIP3hi contours on the output power and quiescent current plane for (a) device A and (b) device B. The 1-dB compression point and optimal linearity locus are indicated. The dots indicate the measurement points.



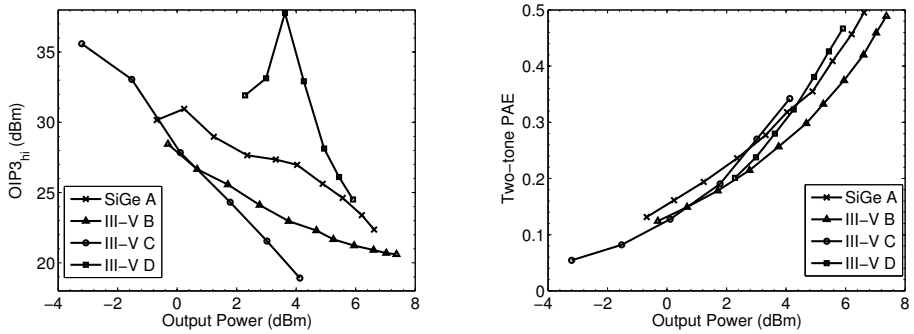
(a)



(b)

Figure 9.8: Measured OIP3hi contours on the output power and quiescent current plane for (a) device C and (b) device D. The 1-dB compression point and optimal linearity locus are indicated. The dots indicate the measurement points.

By tracing the optimum linearity curves the four devices can be compared for their maximum linearity versus output power. Therefore, in Fig. 9.9(a) the optimal linearity is given. Furthermore, in Fig. 9.9(b) the two-tone power added efficiency for this optimal linearity is presented.

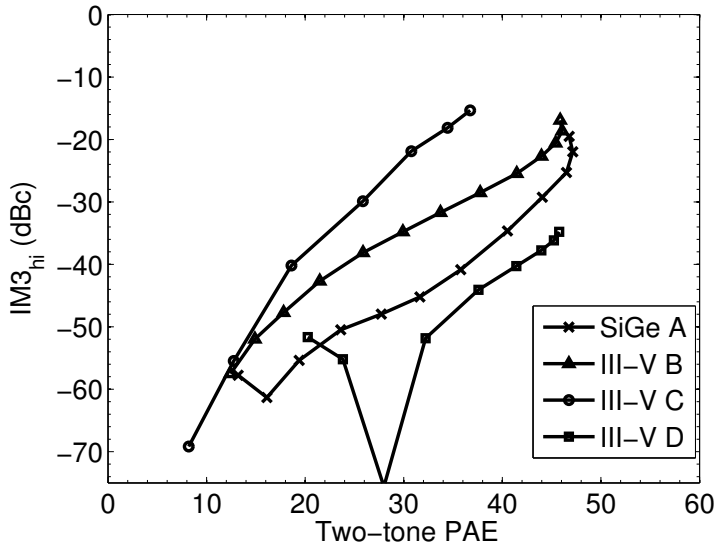


(a) (b)

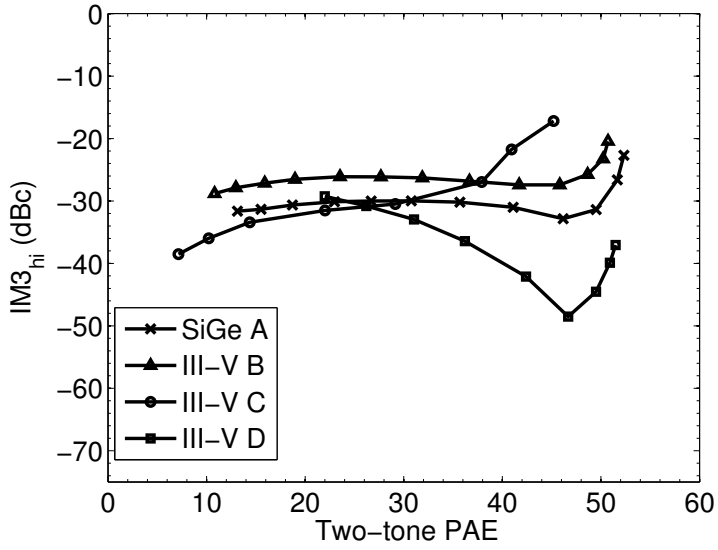
Figure 9.9: (a) Optimal OIP3hi versus output power and (b) Two tone PAE at optimal OIP3hi versus output power for the four studied devices.

However, such a locus versus output power is difficult to realize in practice. Therefore, the linearity performance will also be evaluated at a fixed bias current resulting from a set base voltage and base-band resistance. Two specific bias points are chosen. Firstly, the device is biased at the current for which the highest linearity was measured (Table 9.3). Secondly, the device is biased at the current for which the highest two-tone PAE near the 1 dB compression point was measured, for these devices around 3 mA. The measurement results are presented in Fig. 9.10. These bias currents are also indicated in Fig. 9.7 and Fig. 9.8.

From Fig. 9.9 and Fig. 9.10 some conclusions can be drawn. Device C has a lower two-tone power added efficiency compared to the others. This may be related to the fact that device C has a thicker collector, resulting in lower efficiency. The three other devices reach comparable efficiencies, while their peak power levels are within 1 dB of each other. Device D has the best linearity performance, followed by the SiGe device A.



(a)



(b)

Figure 9.10: $IM3$ versus two-tone PAE for (a) the bias current for which the highest $OIP3$ was measured (given in Table 9.3) and (b) the bias current for which the highest two-tone PAE was measured near the 1-dB compression point, which was around 3 mA for all four devices.

A compact model for the SiGe device was available. Therefore, by using simulated two-tone loadline data, the variation of C_{bc} over the loadline can be reconstructed (Note, that for all devices the same loadline data is applied). From the same measurements as used for the extraction of f_t's also the C_{bc} was extracted. The resulting C_{bc} data over the output plane are given in Fig. 9.11, on which the simulated two-tone loadline is projected.

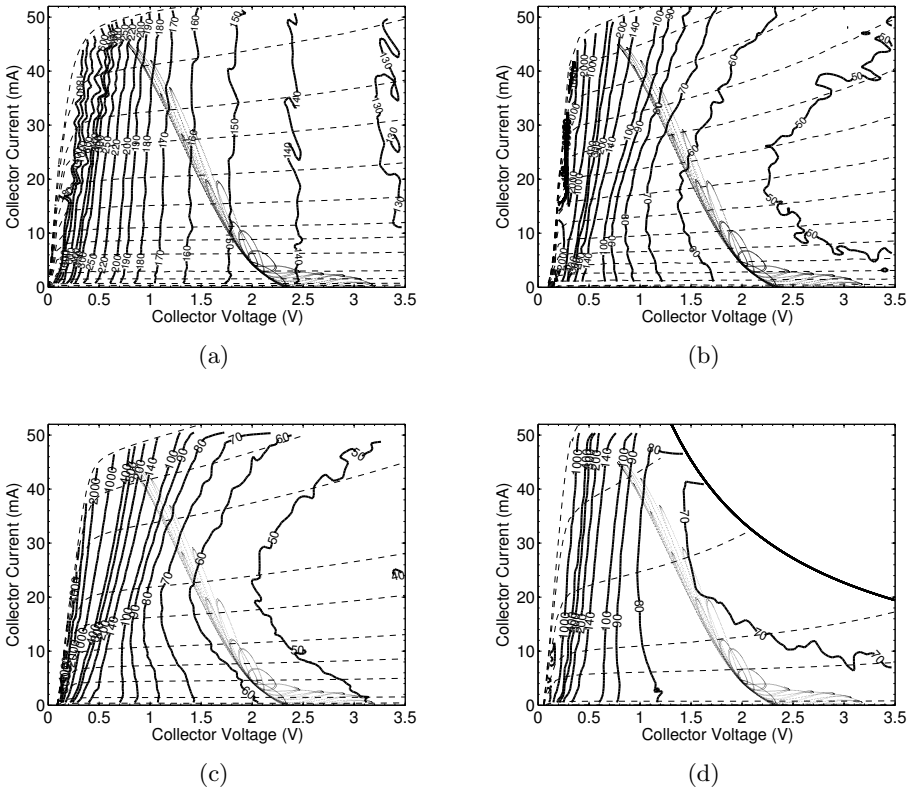
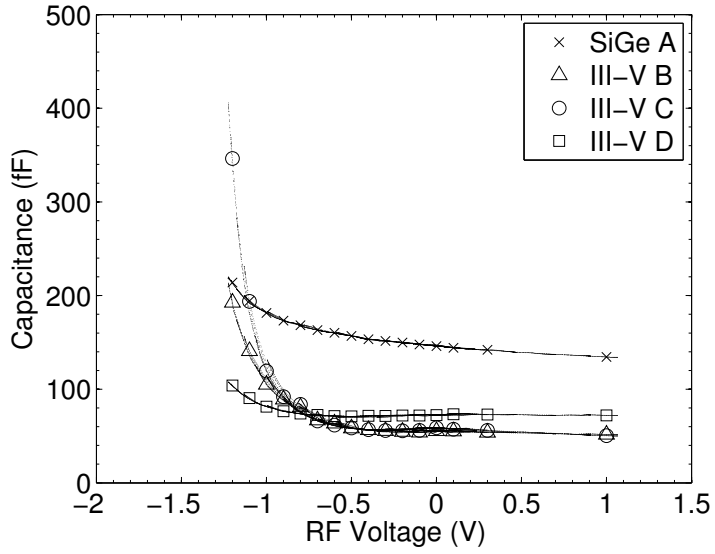
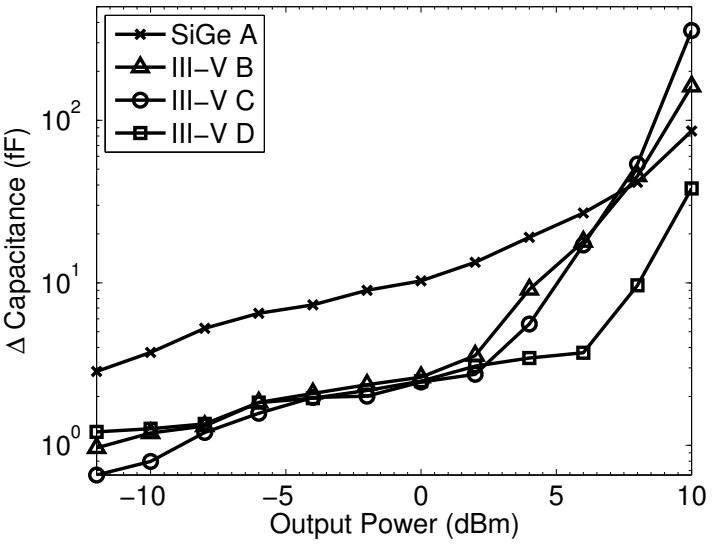


Figure 9.11: Extracted C_{bc} (fF) from measured pulsed s-parameters at 2 GHz (298 K) of (a) device A (SiGe), (b) device B, (c) device C and (d) device D (power limited, see Table 9.1 and Fig. 9.6). On all figures the simulated two-tone loadline is projected.

The resulting C_{bc} over the two-tone loadline can be extracted from the measurements and is given in Fig. 9.12.



(a)



(b)

Figure 9.12: Extracted measured C_{bc} over the two-tone loadline of the four characterized devices. (a) As function of RF voltage swing for a power level close to the compression point and (b) the change in capcitance ΔC for a given output power.

The final conclusion with respect to the impact of the base-collector can be made by combining the figures for the $OIP3$ with the variation of C_{bc} over the loadline. The device with the lowest variation over the loadline has the highest linearity over the optimum linearity locus, when the exponential distortion has been cancelled. Furthermore, a recommendation for choosing the device-size can be made. For GaAs devices it should be chosen such that the current level for the peak f_t (Fig. 9.6(d)) appears near the maximum RF current swing, since this will align the loadline with the constant C_{bc} contour, as can be seen in Fig. 9.11(d). For Si/SiGe devices the only option to realize a more linear C_{bc} is by increasing the collector voltage. Note that in these experiments a collector voltage of 2 V was chosen to benefit most from the GaAs C_{bc} behavior.

9.5 Conclusion

In this chapter the out-of-band cancellation method is experimentally demonstrated up to high power levels, i.e. up to the 1 dB compression point of the device. This has been applied to four devices, one SiGe device, two AlGaAs devices and one InGaP device. It has been demonstrated by both simulations and measurements that when the exponential distortion has been cancelled, even better linearity can be reached when the C_{bc} behaves linear. As a result, some recommendations for bipolar device design and their optimum scaling are given.

Chapter 10

Conclusions and recommendations

10.1 Conclusions

This thesis addresses technology, characterization and modeling solutions that ease and/or shorten the development of the future generations of mobile phones aiming at: low cost, compact form factor, battery efficient operation, and support of all possible wireless services in a flexible manner. This latter requirement follows from the tremendous growth in individual communication over the last decade. As a result a plurality of communication standards need to co-exist, which severely taxes the linearity and efficiency of the transceiver. Currently, in handsets a multi-path approach is followed to integrate these multiple communication services. However, to handle this exploding complexity with an increasing number of bands, an adaptive front-end able to change the operating frequency, as well as the modulation standard, would be very advantageous. For this reason, it is the general expectation that adaptive circuitry will be an essential part of future RF communication systems.

To address the needs of these new features, this thesis examines the requirements for tunable devices, i. e. varactors, that can support adaptive operation in future RF communication systems. The most important quantifiers prove to be efficiency (low losses) and low distortion. Consequently, for a varactor device, both a technology to drastically reduce the losses, as well as circuit topologies to improve the linearity, have been introduced in this thesis, to create a high performance tunable linear capacitor that can act as enabler for future adaptive wireless systems. Also, new characterization methods and modeling strategies were introduced in this thesis in support of these device innovations.

With respect to the bipolar devices currently used in the transmitter output stage, the trade-off between efficiency and linearity has been investigated. In view of this, the importance of the base-collector capacitance has been illuminated. To study the linearity of bipolar transistors implemented in different technologies, out-of-band cancellation techniques have been used. The related experiments that provide

the connection between the non-linear base-collector capacitance and the resulting linearity have been supported by simulations using a verilog-A based linearizable Mextram model.

The most important conclusions of these investigations will now be discussed in more detail.

10.1.1 Adaptivity - losses

Losses in RF system components lead to a performance degradation of the entire system, or when compensating for these losses to an increased power consumption. Therefore, RF components and especially adaptive RF components need to be low loss. The adaptive components in this thesis are based on semiconductor varactor diodes. Typically, the losses in these devices are dominated by the series resistance of the buried-layer. In this thesis an aggressive strategy has been introduced to completely remove the bulk wafer, and then contact the varactor device with metal from both sides. This approach enables to reach the near ideal intrinsic 1-D varactor performance. The actual achieved performance in device experiments has been compared to published results in literature and outperforms existing solutions, especially in the low GHz region.

10.1.2 Adaptivity - distortion

Similar to the requirement for low losses, the RF components need to have low distortion properties to avoid performance degradation of the wireless system. This means that the applied RF devices need to be very linear in order to avoid undesired mixing of the signals present in the system. As such, the creation of interfering distortion products that may obscure the desired signal can be avoided.

To overcome the poor linearity properties of traditional varactors some distortion-cancellation schemes for these devices have been demonstrated. The proposed varactor configurations make use of anti-series connections or alternatively anti-series / anti-parallel connections, in combination with specific doping profiles and specific device areas. Further improvement of linearity of these structures can be reached by stacking multiple varactor diodes in anti-series configuration. An approach that is advantageous for both effective tuning range and power handling. Furthermore, the importance of a proper varactor bias-network is discussed, since it influences the distortion cancellation. For this purpose a dedicated anti-parallel diode pair was introduced in the varactor bias network to increase the impedance that the bias network offers to the varactor devices.

In order to conclude if the proposed devices with their $IM3$ cancelation scheme can be reliable manufactured, the influence of process-spreading is investigated. It was found that process parameter variation has only limited influence on the actual $IM3$ cancelation. In view of this, also the use of two-sided contacting proves to be beneficial, since it strongly reduced the layout parasitics of the varactor devices that can degrade the effectiveness of the $IM3$ cancellation.

10.1.3 Adaptivity - device characterization

An essential part in device development is the characterization of the realized devices. In this thesis several characterization methods have been employed and introduced. Both off-the-shelve as well as custom built state-of-the art measurement systems have been applied to obtain the measurement results shown in this thesis. A custom load-pull system[1] was employed to measure the linearity of the devices. Also a custom pulsed measurement system[2] is employed to study thermal effects in varactor diodes. From this later analysis it had been shown that thermal runaway, due the temperature dependency of the losses, will not occur in the studied varactor diodes.

Typically, device characterization is the starting point of device modeling. For better understanding of the behavior of (varactor) diodes with large reverse leakage current a direct modeling approach is introduced. This method has the advantage of being able to extract doping profiles that reach deeper into a device when large reverse leakage currents are present. This direct modeling approach was also applied to study the effect of measurement-errors on the characterization of high-Q devices. These characterization methods are directly applicable to other tunable device technologies as well.

10.1.4 Adaptivity - demonstrators

Several technology demonstrators have been developed in the context of this thesis to illustrate the low loss and high linearity properties of the implemented adaptive elements. Adaptive matching networks and a tunable band-pass filter have been realized with excellent linearity performance and low-loss performance. Furthermore, in collaborations with other DIMES/TUDelft and UCSD circuit-designers highly linear phase-shifters, an adaptive multi-band multi-mode power amplifier and a tunable antenna haven been realized. This demonstrates that the introduced distortion canceling topologies are directly applicable in many relevant applications.

10.1.5 Trends in tunable elements

Since the first publication of the distortion-free varactor stack, using uniform doping profiles, also other publications that aim for distortion cancelation using similar strategies have appeared, for example in BST varactors [127] or MEMS varactors [128]. Further research collaboration activities within DIMES have resulted in other remarkable solutions, notably varactors in anti-series using an exponential capacitance voltage relation[3], these later solutions are closely connected to the work described in this thesis and are for this reason briefly adressed here.

It was demonstrated that when using varactors with an exponential capacitance-voltage relation [130, 131], similar as for uniformly doped varactors, anti-series and

[1] For more information the reader is referred to the work of Spirito [126] and Marchetti et al. [123] on active harmonic load-pull.

[2] For more information the reader is referred to the work of Marchetti et al. [98] on pulsed measurement systems.

[3] For more information the reader is referred to the work of Huang. [129]

anti-series, anti-parallel solutions can be found that behave very linear. The anti-series configuration differs in its baseband impedance requirements for biasing. Namely, the center-tap contact of the varactor stack for uniform doped varactors needs to be as high as possible, while a varactor stack based on exponential varactors, it needs to be as low as possible, however, without compromising its RF performance. When comparing the various low-distortion varactor configurations it becomes clear that the varactor stack with uniform varactors (DFVS – Distortion Free Varactor Stack) is a special case where ideally all distortion components disappear. Whereas in the exponential varactors (NTSVS – Narrow Tone-Spacing Varactor Stack) only the $IM3$ is cancelled, while the remaining $IM5$ distortion dominates the linearity performance.

The anti-series, anti-parallel solution (HTRVS – High Tuning Range Varactor Stack) has the advantage that other doping profiles can be used, of which the exponential ($\frac{N}{x^2}$-doping) solution (WTSVS – Wide Tone-Spacing Varactor Stack) is a special case. The exponential anti-series, anti-parallel solution proves to be complementary to the NTSVS in its linearity performance for a given tone-spacing. As a consequence, the NTSVS works best for low tone-spacings, whereas the WTSVS performs best for wider tone-spacing. Since they both make use of the $\frac{N}{x^2}$-doping profile the NTSVS and WTSVS can be fabricated on the same wafer providing complementary linearity properties within one technology.

The use of stacking to increase the power handling, effective tuning range and linearity without compromising the quality factor too much, has been also demonstrated in this thesis. Furthermore, both Fu et al. [132] and Huang et al. [131] have shown results for BST and GaAs pn junction varactors, respectively. From the analysis of Huang it becomes clear that stacking is more effective in $IM3$-cancelled devices. This is caused by the fact that their remaining distortion is dominated by $IM5$ components, which have a steeper power dependency and therefore, offer a superior linearity performance when increasing the power back-off conditions through (multiple) device stacking.

In the context of this thesis a high performance varactor technology has been developed that outmost profits from the advantages of substrate transfer technologies. This Silicon-on-Glass process has been demonstrated to be very suitable for implementing low-loss varactors in low distortion configurations. In special, Fig. 5.7 clearly shows that the series resistance has been strongly reduced for the in this thesis realized Silicon-on-Glass varactors compared to other published results. Therefore, record breaking quality factors have been realized, even for relatively large capacitance values.

10.1.6 Handset power amplifiers - device simulation and modeling

When discussing passive tunable elements the losses and linearity are considered to be the most important criteria in their device development. Similarly when developing bipolar technologies for handset power amplifiers, again efficiency and linearity are considered to be the key development parameters. In support of this, in this work the most dominant non-linearities are studied that cause non-linear distortion, namely, the exponential nature of the bipolar device and distortion contributions due to the

non-linear base-collector capacitance.

In this work, using physical device simulations and measurements, a study has been done to evaluate the base-collector capacitance behavior of both silicon as well as GaAs heterojunction bipolar devices. It was shown that compared to silicon devices, a well dimensioned GaAs device can provide a lower variation of the base-collector capacitance over a class-AB loadline trajectory, suggesting a low-distortion optimum when optimum bias and out-of-band loading conditions are applied. To verify this assumption, a compact modeling tool has been developed, which allows the user to linearize certain non-linear contributions including the base-collector capacitance. Using this tool the impact of the base-collector capacitance on the device linearity, when optimum out-of-band linearization is applied, has been studied. This study confirmed the general statement that, the lower the variation of C_{bc} over the loadline, the better the linearity performance of the bipolar device will be.

These simulation results have been experimentally confirmed using pulsed small-signal measurements to extract the C_{bc}-behavior over the loadline, as well as active harmonic load pull measurements to provide out-of-band matching conditions to the device under test. The measurement results support the earlier conclusions found by the simulations, namely the device with lowest variation in C_{bc} can provide the best linearity performance. This gives an advantage to well dimensioned GaAs devices, which, due to their inherently different mobility dependence on the electric field compared to silicon, allow optimization of their C_{bc} behavior for low distortion.

10.2 Recommendations

10.2.1 Adaptivity

Some non-ideal aspects of capacitive tunable devices have been noticed during these investigations, it was observed that the effective capacitance value of a continuous tunable capacitive device can be weakly dependent on the applied RF power. This implies its effective capacitance value changes as function of the amplitude of the RF signal. This phenomenon can complicate the use of these components in high precision applications, e. g. in tunable RF phase shifters, high power signal fluctuations can give rise to small phase deviations. When applied in very selective tunable filters such a power dependence can yield de-tuning of the the passband/stopband of the filter. Initial work shows that $IM3$ compensated tunable devices are less sensitive to these phenomena, but depending on the $IM3$ compensation applied, also here differences can be found in this power dependence between various implementations. It is therefore strongly recommended to continue investigations in this direction.

The application of CVD boron in the fabrication of highly linear, low loss devices has many advantages. At first boron was introduced to reduce the reverse bias leakage current, however at a later stage this leakage current was further suppressed using implants at the edge of the device. Unfortunately metallic boron is not a very good conductor. This leads to the possibility of increasing the varactor quality factor (Q) by reducing the deposit times of the boron layer, at the expense of increased reverse leakage current. However, from the measurements as presented in Chapter 5, can be concluded that an increase of a few decades of leakage current will not

influence their performance as tunable element. Therefore, a potential lower RF power loss is possible by applying thinner boron layers. When skipping the boron layer altogether a Schottky diode would be formed, with its associated high leakage current. Depending on the specific application and the operating frequency this may still result in acceptable performance. However, this increases the capacitance density, which may result in a lower Q.

When aiming for mm-wave varactor diodes or varactors for even higher frequencies, the Q-factor of the device might become an issue. The Q-factor of a varactor diode can be increased at the expense of tuning range and/or breakdown voltage. In the case of a varactor with uniform doping, increasing the doping level will improve the quality factor at the expense of the power handling (breakdown voltage reduces). In case of a hyperabrupt varactor a trade-off is possible between tuning range and breakdown with respect to quality factor of the device. Another method of exchanging tuning range for Q-factor would be the use of a lowly doped top layer, this will reduce the capacitance density and therefore increases the Q-factor, at the expense of tuning range, however the breakdown voltage remains similar. This approach would also be advantageous when the devices become so small that the contact resistance becomes dominant. Special care has to be taken when considering this method, since this will influence the capacitance-voltage characteristics. In the case of the NTSVS and WTSVS this will violate the distortion cancelation requirements. In other cases, e. g. DFVS or HTRVS, distortion cancellation is still possible.

The material of choice in this thesis was silicon, however wide-bandgap materials offer significant potential for improving both Q-factor and tuning range. Therefore, the use of GaAs, SiC and GaN should be investigated. Some results in this respect have already been reported [67, 133, 134], however, since the current results are still far away from what is theoretical possible, significant improvements can still be expected [135]. Especially when considering these wide-bandgap materials for varactor implementations in combination with two-sided contacting.

10.2.2 Handset power amplifiers

The investigation of the impact of the base-collector capacitance on the linearity of an amplifier using the out-of-band cancellation method has provided the link between small-signal parameters (C_{bc}) and the large signal linearity performance. This opens the way to optimize the collector epilayer for specific RF applications or communication standards, based on small-signal measurements or device simulations. However, the availability of a harmonic load-pull system, which can control baseband, fundamental and second harmonic impedance, is essential for the verification of this epilayer optimization.

The linearity optimization as presented in this thesis has been verified using passive base-band impedances. This restricts the useful measurement bandwidths to values below 1 MHz. However, active injection of baseband signals can provide baseband impedance control in a similar way as recently is applied to the fundamental and higher harmonics in the mixed-signal based harmonic load pull setup. These new tools facilitate device technology optimization for the future generations of wideband wireless communication standards, a topic of major importance to the developers of

3G/4G communication systems.

Appendix A

Direct model extraction

The equations of the direct model calculation method from Section 6.4 for four components, R_s, L_s, R_p and C_p are as follows:

$$R_s = \frac{\omega_2^4 R_2 X_1^2 - 2\omega_2^3\omega_1 R_2 X_2 X_1 + \omega_2^2\omega_1^2 R_2 X_2^2 - \omega_2^2\omega_1^2 R_1 X_1^2 + \omega_2^2\omega_1^2 R_2^3 - \omega_2^2\omega_1^2 R_1^3}{\omega_1^2 X_2^2\omega_2^2 + 2\omega_1^3 X_2 X_1\omega_2 + X_1^2\omega_2^4 - \omega_1^2 X_1^2\omega_2^2 - 2\omega_1 X_2 X_1\omega_2^3 - \omega_1^4 X_2^2} + \frac{3\omega_2^2\omega_1^2 R_2 R_1^2 - 3\omega_2^2\omega_1^2 R_2^2 R_1 + 2\omega_2\omega_1^3 R_1 X_2 X_1 - \omega_1^4 R_1 X_2^2}{\omega_1^2 X_2^2\omega_2^2 + 2\omega_1^3 X_2 X_1\omega_2 + X_1^2\omega_2^4 - \omega_1^2 X_1^2\omega_2^2 - 2\omega_1 X_2 X_1\omega_2^3 - \omega_1^4 X_2^2}. \tag{A.1}$$

$$L_s = \frac{X_1 X_2\omega_2^2 - \omega_2\omega_1 X_2^2 - \omega_2\omega_1 R_1^2 - \omega_2\omega_1 R_2^2 - \omega_2\omega_1 X_1^2 + 2\omega_2\omega_1 R_2 R_1 + \omega_1^2 X_2 X_1}{-\omega_1 X_2\omega_2^2 + \omega_1^3 X_2 + X_1\omega_2^3 - \omega_1^2 X_1\omega_2}. \tag{A.2}$$

$$\begin{aligned} R_p = {} & \frac{-2\omega_2\omega_1^3 R_2^2 X_2 X_1 - 2\omega_2\omega_1^3 R_1^2 X_2 X_1 - 2\omega_2^3\omega_1 R_2^2 X_2 X_1 + 4\omega_2^3\omega_1 R_2 R_1 X_2 X_1}{A_1} \\ & + \frac{\omega_2^2\omega_1^2 R_2^2 X_1^2 + 6\omega_2^2\omega_1^2 R_2^2 R_1^2 - 4\omega_2^2\omega_1^2 R_2^3 R_1 + \omega_2^2\omega_1^2 R_1^2 X_2^2 + \omega_1^4 X_2^4 + \omega_2^4 X_1^4}{A_1} \\ & + \frac{-2\omega_2^2\omega_1^2 R_2 R_1 X_1^2 - 2\omega_2^3\omega_1 R_1^2 X_2 X_1 + 4\omega_2\omega_1^3 R_2 R_1 X_2 X_1 - 2\omega_2^2\omega_1^2 R_2 R_1 X_2^2}{A_1} \\ & + \frac{-4\omega_2\omega_1^3 X_2^3 X_1 - 2\omega_1^4 R_2 R_1 X_2^2 - 2\omega_2^4 R_2 R_1 X_1^2 - 4\omega_2^3\omega_1 X_2 X_1^3 + \omega_2^2\omega_1^2 R_1^2 X_1^2}{A_1} \\ & + \frac{\omega_2^2\omega_1^2 R_2^4 + \omega_2^2\omega_1^2 R_1^4 + \omega_1^4 R_1^2 X_2^2 + \omega_1^4 R_2^2 X_2^2 + \omega_2^4 R_2^2 X_1^2}{A_1} \\ & + \frac{\omega_2^4 R_1^2 X_1^2 + 6\omega_2^2\omega_1^2 X_2^2 X_1^2 + \omega_2^2\omega_1^2 R_2^2 X_2^2 - 4\omega_2^2\omega_1^2 R_2 R_1^3}{A_1}. \end{aligned} \tag{A.3}$$

Where A_1 is given by

$$\begin{aligned} A_1 = {} & \omega_2^4 R_1 X_1^2 + 2\omega_2\omega_1^3 R_1 X_2 X_1 + \omega_2^2\omega_1^2 R_1 X_2^2 - \omega_2^2\omega_1^2 R_2 X_2^2 \\ & -2\omega_2\omega_1^3 R_2 X_2 X_1 - 2\omega_2^3\omega_1 R_1 X_2 X_1 - \omega_2^4 R_2 X_1^2 - \omega_2^2\omega_1^2 R_1 X_1^2 \\ & +\omega_2^2\omega_1^2 R_2 X_1^2 + 2\omega_2^3\omega_1 R_2 X_2 X_1 + \omega_1^4 R_2 X_2^2 - \omega_1^4 R_1 X_2^2. \end{aligned} \tag{A.4}$$

$$\begin{aligned} C_p = {} & \frac{-\omega_1^3 X_2^3\omega_2^2 - X_1^3\omega_2^3\omega_1^2 + X_1^3\omega_2^5 - 3\omega_1^4 X_2^2\omega_2 X_1 - 3\omega_1 X_2\omega_2^4 X_1^2}{A_2} \\ & + \frac{3\omega_1^2 X_2^2\omega_2^3 X_1 + \omega_1^5 X_2^3 + 3\omega_1^3 X_2\omega_2^2 X_1^2}{A_2}. \end{aligned} \tag{A.5}$$

Where A_2 is given by

$$\begin{aligned} A_2 = {} & (-2\omega_2\omega_1^3 R_2^2 X_2 X_1 - 2\omega_2\omega_1^3 R_1^2 X_2 X_1 - 2\omega_2^3\omega_1 R_2^2 X_2 X_1 + 4\omega_2^3\omega_1 R_2 R_1 X_2 X_1 \\ & +\omega_2^2\omega_1^2 R_2^2 X_1^2 + 6\omega_2^2\omega_1^2 R_2^2 R_1^2 - 4\omega_2^2\omega_1^2 R_2^3 R_1 + \omega_2^2\omega_1^2 R_1^2 X_2^2 + \omega_1^4 X_2^4 + \omega_2^4 X_1^4 \\ & -2\omega_2^2\omega_1^2 R_2 R_1 X_1^2 - 2\omega_2^3\omega_1 R_1^2 X_2 X_1 + 4\omega_2\omega_1^3 R_2 R_1 X_2 X_1 - 2\omega_2^2\omega_1^2 R_2 R_1 X_2^2 \\ & -4\omega_2\omega_1^3 X_2^3 X_1 - 2\omega_1^4 R_2 R_1 X_2^2 - 2\omega_2^4 R_2 R_1 X_1^2 - 4\omega_2^3\omega_1 X_2 X_1^3 + \omega_2^2\omega_1^2 R_1^2 X_1^2 \\ & +\omega_2^2\omega_1^2 R_2^4 + \omega_2^2\omega_1^2 R_1^4 + \omega_1^4 R_1^2 X_2^2 + \omega_1^4 R_2^2 X_2^2 + \omega_2^4 R_2^2 X_1^2 + \omega_2^4 R_1^2 X_1^2 \\ & +6\omega_2^2\omega_1^2 X_2^2 X_1^2 + \omega_2^2\omega_1^2 R_2^2 X_2^2 - 4\omega_2^2\omega_1^2 R_2 R_1^3)\omega_1\omega_2. \end{aligned} \tag{A.6}$$

Where ω_1 and ω_2 are the angular frequencies at which the impedances $R_1 + jX_1$ and $R_2 + jX_2$ are measured.

Appendix B

Verilog-A code for a linearized Mextram model

In this appendix the terminology is based on the official Mextram release 504.6 [136]. To linearize the Verilog-A model it is necessary to have the DC solution available. To be able to set this DC point independently of the full model simulation, the model will be extended. To do so an extra set of internal nodes, namely: 'c_DC', 'b_DC', 'e_DC', 's_DC', 'e1_DC', 'b1_DC', 'b2_DC', 'c1_DC', 'c2_DC' will be used to calculate the DC solution. For these nodes all the equations from the main evaluation routine ('evaluate.inc') are copied with an added '_DC' to the variables. This equations are a function of 3-5 extra parameters (V_C, V_B, V_E, V_S and V_T) which define the DC operating point. The following code indicates the most important changes and is based on 'bjt504.va' and therefore ignores the thermal node. Since the model has been split in a DC solution and a DC+AC solution, the DC solution is available twice. To avoid issues resulting from this, performing a differentiation followed by an integration without adding the integration constant ('`idt(ddt(...))`') removes the DC component. Note that this is only an issue for the currents arising from the (trans)conductances, since the DC current is zero through a capacitor.

B.1 bjt504.va

```
// Linearization nodes
electrical c_DC, b_DC, e_DC, s_DC, e1_DC, b1_DC, b2_DC, c1_DC, c2_DC;
```

B.2 parameters.inc

```
parameter real    VC=0            from (-inf:inf);
parameter real    VB=0            from (-inf:inf);
parameter real    VE=0            from (-inf:inf);
parameter real    VS=0            from (-inf:inf);
```

B.3 evaluate.inc

```
//Linearization In
In_help=In_DC-idt(ddt(In_DC))+idt(ddt(-ddx(In_DC, V(e1_DC))*V(c2, e1)
         -ddx(In_DC, V(c2_DC))*Vb2c2star
         -ddx(In_DC, V(c1_DC))*(Vb2c2star+V(c2, c1))));

  I(c2, e1) <+ TYPE * In_help;

//Linearization base emitter charges
dVb2e1=ddt(V(b2, e1));
dVb1e1=ddt(V(b1, e1));
I(b2, e1) <+ TYPE * ddx(QteL + QbeL + QeL, V(e1_DC)) * dVb2e1;
I(b1, e1) <+ TYPE * ddx(QteL_s, V(e_DC)) * dVb1e1;

//Linearization base collector charges
dVb2c2=ddt(V(b2, c2));
dVb1c1=ddt(V(b1, c1));
dVb2c1=ddt(V(b2, c1));
dVbc1=ddt(V(b, c1));
dVb2c2star=ddt(Vb2c2star);
dVb2c1star=ddt(Vb2c2star+V(c2, c1));
I(b2, c2) <+ TYPE * (-ddx(Qtc_DC, V(c2_DC))*dVb2c2
                     -ddx(Qtc_DC, V(c1_DC))*dVb2c1);
I(b2, c2) <+ TYPE * (-ddx(Qbc_DC, V(c2_DC))*dVb2c2
                     -ddx(Qbc_DC, V(c1_DC))*dVb2c1);
I(b2, c2) <+ TYPE * (-ddx(Qepi_DC, V(c2_DC))*dVb2c2star
                     -ddx(Qepi_DC, V(c1_DC))*dVb2c1star);
I(b1, c1) <+ TYPE * (ddx(Qtex_DC, V(b_DC))
                     +ddx(Qtex_DC, V(b1_DC)))*dVb1c1;
I(b1, c1) <+ TYPE * (ddx(Qex_DC, V(b_DC))
                     +ddx(Qex_DC, V(b1_DC)))*dVb1c1;
I(b,  c1) <+ TYPE * (ddx(XQtex_DC, V(b_DC))*dVbc1);
I(b,  c1) <+ TYPE * (ddx(XQex_DC, V(b_DC))*dVbc1);
```

Appendix C

Models and model parameters TCAD Medici simulations

Mostly Medici [114] default models and parameters where applied in these simulation, however sometimes specific models were applied and sometimes parameters were modified to include specific physical effects. The models and parameters used are given in this appendix.

C.1 SiGe

Applied models

```
MODELS SRH FLDMOB BGN COMP.ET
```

Applied solver options

```
METHOD CONT.STK AUTONR DAMP.CON ITLIMIT=40 N.DAMP
```

C.2 III-V

Material changes

```
MATERIAL INGAAS V0.BGN=0 CON.BGN=0 NSRHN=1
         BN=0 EN=0 NSRHP=1 BP=0 EP=0 AUGN=0 AUGP=0
MATERIAL INGAAS AFFINITY=4.72 EG.MODEL=4
MATERIAL GAAS EG.MODEL=4 EG300=1.34
MATERIAL INGAP EG.MODEL=4
```

Relaxation times

```
MATERIAL GAAS ELE.TAUW=10e-12 HOL.TAUW=10e-12
MATERIAL INGAAS ELE.TAUW=10e-12 HOL.TAUW=10e-12
MATERIAL INGAP ELE.TAUW=10e-12 HOL.TAUW=10e-12
```

Mobility parameters

```
MOBILITY INGAAS MUN0=2.7252E04 MUP0=480
MOBILITY INGAP MUN0=1000 MUP0=50
MOBILITY FLDMOB=2 E0N=3.9e3 VSATN=1.1148E7
         EXN1.GAA=3.8911 EXN2.GAA=4.0032
```

Applied models

```
MODELS SRH FLDMOB BGN COMP.ET ND.MOB
```

Applied solver options

```
METHOD CONT.STK AUTONR DAMP.CON ITLIMIT=40 N.DAMP
```

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Summary

Title: Device Realization, Characterization and Modeling for Linear RF Applications
By: Koen Buisman

This thesis work addresses technology, characterization and modeling solutions that ease and shorten the development of the future generations of mobile phones that are: low cost, compact, battery efficient, and support all possible wireless services in a flexible manner. This is required due to the tremendous growth in individual communication over the last decade. As discussed in **Chapter 1** a plurality of communication standards need to co-exist, while at the same time higher data-rates require spectrally efficient modulation standards with high peak-to-average power ratios tax the linearity and efficiency of transceivers. Currently a multi-path approach is applied to integrate multiple communication services together. To handle this exploding complexity an adaptive front-end able to change operating frequency as well as modulation standard would be very advantageous. To reach this goal tunable passive components without introducing significant losses or degradation of the signal quality are required.

For this purpose **Chapter 2** introduces the conventions and notations of this thesis and at the same time introduces non-linear distortion. Furthermore typical measurement methods to quantify non-linear distortion are discussed, comprising of single-tone excitation up to full wide-band modulated communication signals. Shortly non-linear distortion in bipolar devices is discussed, followed by introducing a method that can reduce distortion in bipolar devices, using out-of-band terminations.

Several quantifiers exist to compare tunable device technologies. Notably power consumption, required control voltage, voltage handling, losses and distortion properties. **Chapter 3** examines these quantifiers for pn, BST, MOS, MEMS varactors and MEMS, PIN and PHEMT switches. Furthermore the origin of losses, especially in semiconductor varactors are illuminated. Special attention has been paid to the trade-off between breakdown voltage and losses in semiconductor varactors.

Varactor diodes are typically disqualified for linear RF applications, due to their inherent non-linearity. In order to overcome this drawback **Chapter 4** introduces varactor topologies in combination with specific doping profiles that can overcome these limitations. Furthermore the influence of the biasing connection on the linearity of these varactor stacks is discussed and the required high impedance is improved by introducing the use of anti-parallel bias diodes. Then the use of multiple stacks in se-

ries to improve the power handling, effective tuning range and linearity is introduced. Finally the chapter discusses the influence of spreading, due to process parameter spread during fabrication, on the reachable linearity and comes to the conclusion that device realization with the predicted linearity properties should be possible.

Based on the analysis in the previous chapter, devices have been fabricated and the realized devices are introduced in **Chapter 5**. This chapter discusses the fabrication methods and focusses on the relation between loss performance and fabrication. Special fabrication methods like substrate transfer, boron deposition to realize the pn junction and laser annealing to make low-ohmic contacts without influencing the doping profile are discussed. Furthermore suppressed leakage due to implants around the periphery of the device are demonstrated. Finally the realized devices are compared to tunable devices from literature and are shown to outperform existing solution with respect to loss especially in the low GHz region.

The fabricated devices are then characterized for their linearity performance in **Chapter 6**, measured results of two-tone tests on single varactor stacks and multiple stacks in series are presented. The influence of the impedance of the biasing point is demonstrated by measuring with different tone-spacings. The excellent linearity performance as predicted by Chapter 4 are measured and are in good agreement with simulated results. The introduction of these tunable elements with very low distortion leads to the application of these diodes under high RF power conditions. Therefore, the devices are analyzed for their thermal behavior and measurement results supporting this are presented. Finally a direct model extraction method for varactor diodes is presented and demonstrated.

In **Chapter 7** realized circuit demonstrators using these low-loss, low distortion tunable devices are presented. These demonstrators include adaptive matching networks, a multi-mode multi-band adaptive power amplifier, adaptive filters, tunable phase-shifters and an adaptive scan-beam reflectarray antenna. Measurement results on circuit performance and linearity are presented.

The first part of the thesis addresses loss and linearity in tunable devices, now the thesis switches to linearization of bipolar devices using the out-of-band cancellation technique. **Chapter 8** introduces the background and analyses the difference between SiGe and GaAs devices with respect to their linearity performance. The focus of this analysis was on the behavior of the base-collector capacitance. To support this analysis an linearizable Mextram model is introduced.

Followed by experimentally investigating the linearity of bipolar devices in **Chapter 9** and pinpointing the important parts of models that describe the critical phenomena, not only the (dis)advantages of some technologies are highlighted but also the tools and techniques are provided to support the development of future linear transmitters for future 3G/4G/lte communication applications.

Chapter 10 finishes the thesis and gives the conclusions of the thesis and the recommendations for future work.

Samenvatting

Titel: Component Realisatie, Karakterisatie and Modellering voor Lineare RF Toepassingen
Door: Koen Buisman

Dit proefschrift bestudeert halfgeleider technologie, karakterisatie en modelleer methodes, die de ontwikkeling van toekomstige generaties mobiele telefoons eenvoudiger en sneller maken. Deze telefoons zijn: goedkoop, compact, efficiënt en zijn in staat om verschillende draadloze diensten op een flexibele manier te gebruiken. Dit is noodzakelijk geworden door de grote groei in individuele communicatie over het laatste decennium. Zoals besproken in **hoofdstuk 1** bestaan een veelvoud van communicatie standaarden naast elkaar, terwijl tegelijkertijd snellere data-verbindingen spectraal efficiënte modulatie methodes nodig hebben, met hoge top/gemiddelde vermogensverhouding, die hoge lineariteit eisen en die hoge efficiëntie van zendontvangers lastig maken. Op dit moment wordt een parallelle aanpak gebruikt om meerdere communicatie diensten te integreren. Om de toename in complexiteit door de toename in verschillende communicatie standaarden bij te houden, zou een adaptief RF frontend, welke kan schakelen tussen de verschillende frequenties, bandbreedtes, alsmede uitgangsvermogens, voordelen bieden. Om dit doel te bereiken zijn nieuwe afstembare passieve componenten noodzakelijke, welke geen extra verliezen of degradatie van de signaal kwaliteit introduceren.

Voor dit doel, introduceert **hoofdstuk 2** de conventies en notaties zoals gebruikt in dit proefschrift. Ook wordt tegelijkertijd niet-lineaire distorsie geïntroduceerd. Verder worden typerende karakterisatiemethodes voor niet-lineaire distorsie behandelt. Deze methodes gaan van een-toon excitatie tot volledige breedband gemoduleerde communicatiesignalen. Niet-lineaire distorsie in bipolaire transistoren wordt kort behandeld, gevolgd door een methode welke distorsie in bipolaire transistoren kan verminderen met gebruik van 'out-of-band' afsluitingen.

Er bestaan diverse eisen welke gebruikt kunnen worden om technologieën van afstembare componenten te vergelijken. Dit zijn met name: verbruik, benodigde stuurspanning, doorslagspanning, verliezen en distorsie eigenschappen. **Hoofdstuk 3** kijkt naar deze eisen voor pn, BST, MOS, MEMS varactors en MEMS, PIN en PHEMT schakelaars. Verder wordt de oorzaak van verliezen belicht, met name voor halfgeleider varactor diodes. Speciale aandacht wordt gegeven aan het compromis tussen doorslagspanning en verliezen voor halfgeleider varactor diodes.

Conventionele varactor diodes zijn inherent niet-lineair, wat problemen oplev-

ert voor lineaire RF toepassingen. Om dit nadeel op te heffen worden in **hoofdstuk 4** nieuwe varactor topologieën in combinatie met specifieke doteringsprofielen voorgesteld. Verder wordt de invloed van de aansluiting van de stuurspanning op de lineariteit besproken en wordt de benodigde hoge impedantie met anti-parallelle diodes verhoogd. Vervolgens worden meervoudig gestapelde varactors in serie gebruikt om het maximale vermogen, het effectieve afstembereik en de lineariteit te verhogen. Uiteindelijk wordt de invloed van productie parameter variatie op de uiteindelijke lineariteit van de varactors bekeken en wordt geconcludeerd dat realisatie met de voorspelde resultaten mogelijk is.

Gebaseerd op de analyze in de voorgaande hoofdstukken worden componenten gemaakt en geïntroduceerd in **hoofdstuk 5**. De manier van fabriceren en de invloed van de fabricage op de verliezen worden geanalyseerd. Speciale fabricage methodes zoals dubbelzijdige metalen contacten, borium depositie en 'laser annealing' worden gebruikt om de pn junctie te maken zonder het doteringsprofiel te beïnvloeden. Verder worden doteringsatomen geïmplanteerd rond de periferie van de componenten om de lekstroom onder negatieve spanning te onderdrukken. Uiteindelijk worden de gefabriceerde componenten vergeleken met componenten uit de literatuur. Duidelijk wordt dat de voorgestelde componenten lagere verliezen hebben, met name in het lage GHz gebied.

De lineariteitskarakterisatie van de gefabriceerde componenten is gedaan in **hoofdstuk 6**. Gemeten resultaten van twee-toon tests op individuele varactor topologien en meervoudige gestapelde varactors in serie zijn gepresenteerd. De invloed van de impedantie van de aansluiting van de stuurspanning is aangetoond door metingen bij verschillende verschilfrequenties. De uitstekende lineariteitsresultaten zoals voorspeld in hoofdstuk vier zijn gemeten en komen goed overeen met de simulaties. De introductie van deze componenten met hele lage distorsie leidt ertoe dat deze gebruikt gaan worden onder hoge RF vermogens condities. Daarom is het thermische gedrag geanalyseerd en ondersteund met metingen. Uiteindelijk is een directe model extractie methode voor varactor diodes geïntroduceerd en gedemonstreerd.

Om de bruikbaarheid van de voorgestelde aanpak aan te tonen zijn verschillende circuits gerealiseerd in **hoofdstuk 7** met deze componenten met lage verliezen en lage distorsie. Bijvoorbeeld afstembare aanpassingsnetwerken, een afstembare vermogensversterker, een afstembaar filter, afstembare fase-verschuivers en een adaptieve reflecterende antenne. Meetresultaten van de circuits inclusief het lineariteitsgedrag zijn gegeven.

Het eerste deel van dit proefschift heeft gekeken naar de verliezen en distorsie in afstembare componenten. Nu gaat dit proefschrift verder met linearisatie van bipolaire transistoren met gebruik van 'out-of-band' afsluitingen. **Hoofdstuk 8** behandelt de achtergrond en analyseert de verschillen in lineariteit tussen SiGe en GaAs bipolaire transistoren. De focus van deze analyse is op het gedrag van de basis-collector capaciteit. Om deze analyse te ondersteunen is een linearizeerbaar mextram model ontwikkeld.

Dit wordt gevolgd door experimenteel de lineariteit van bipolaire transistoren te onderzoeken in **hoofdstuk 9**. Hiermee zijn niet alleen de kritieke verschijnselen en de voor en nadelen van verschillende technologieën aangegeven, maar ook het gereedschap en de technieken voor de ontwikkeling van toekomstige lineaire zendontvangers

voor toekomstige 3G/4G/LTE communicatie toepassingen.

Hoofdstuk 10 sluit het proefschrift af met conclusies en aanbevelingen voor toekomstig onderzoek.

List of Publications

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B. Yang, A. G. Yarovoy, A. S. E. Valavan, **K. Buisman**, and O. Shoykhetbrod, "A Novel LTCC Differentially-Fed UWB Antenna for the 60 GHz band," *International Journal of Microwave and Wireless Technologies*, vol. 3, special issue no. 2, pp. 171–177, April 2011.

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