A CMOS Dual-RC frequency reference with ±250ppm inaccuracy from -45°C to 85°C

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3.3 A Fully Integrated Dual-RC Frequency Reference with ±250ppm Inaccuracy from -45°C to 85°C

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To comply with wired communication standards such as USB, SATA and PCI/PCI-E, systems-on-chip require frequency references with better than 300ppm accuracy. LC-based references achieve 100ppm accuracy [1], but suffer from high power consumption (~20mW). Thermal diffusivity (TD) references require less power (~2mW), at the expense of less accuracy (1000ppm) [2]. RC-based references offer the lowest power consumption, but their accuracy is typically limited to ~0.1% [3]. In RC relaxation oscillators, comparator offset and delay are the major sources of inaccuracy [4-5]. References based on frequency-locked loops (FLLs) circumvent these by locking an oscillator's frequency to the time-constant of an RC filter, but their accuracy is then limited by the nonlinear temperature dependency of on-chip resistors [3, 6].

This paper describes a 7MHz RC-based frequency reference that solves this problem by accurately combining the complementary temperature dependencies of two integrated resistors in the digital domain. Measurements on 12 samples show that it achieves an inaccuracy of ±250ppm from -45°C to 85°C and an Allan Deviation floor of 250ppb. These results represent the lowest inaccuracy (by 3.5x) and long-term drift (by 16x) ever reported for a CMOS RC-based frequency reference.

The proposed frequency reference (Fig.1) consists of a frequency-locked loop (FLL), in which the frequency of a digitally-controlled oscillator (DCO) is locked to a composite phase-shift derived from two Wien Bridge (WB) filters. Due to the finite temperature coefficients (TCs) of their resistors, the phase-shift of each WB will be a function of temperature. Phase-shifts with complementary TCs can then be generated by realizing WBs from different resistor types, e.g. silicided p-poly (TC=0.36%/°C) and unsilicided n-poly (TC=-0.17%/°C). By digitizing and appropriately combining the complementary phase shifts of the two such WBs, Φ_{sp} and Φ_n, a temperature *independent* phase-shift, Φ_e, can be realized.

As shown in Fig. 1, the phase shift of each WB is digitized by a Phase Domain ΔΣ-Modulator (PDΔΣM). The resulting bitstream output is then decimated by a CIC (cascaded integrator-comb) filter. The non-linear temperature dependence of the resulting Φ_{sp} and Φ_n is first corrected by fixed polynomials [$p_{sp}(.)$ and $p_n(.)$], and then combined to generate Φ_e. The gain provided by the FLL's digital integrator drives Φ_e to zero, thus making the DCO's output frequency f_{DCO} (=7MHz) temperature independent as well.

Fig. 2 shows the block diagram of a WB and its 2nd-order PDΔΣM [8]. Both are driven at $f_{DRV} = f_{DCO}/16$, which is also used to generate the modulator's sampling clock f_s and its phase references, Φ_0 and Φ_1. A chopper demodulator detects the difference between the WB's phase shift, Φ_{WB}, and the phase reference selected by the bitstream, BS. The resulting DC signal is driven to zero by the loop filter's gain, ensuring that the average value of the selected phase references is in quadrature with Φ_{WB}, and therefore, that BS is a digital representation of Φ_{WB}. As in [8], the 1st integrator is based on a 2-stage opamp, while the 2nd integrator employs a g_m-C OTA, which uses R_{ff} to realize the modulator's feed-forward coefficient. Fig. 2 also shows the measured output spectrum of the PDΔΣM that digitizes WB_{sp} when it is driven by a fixed 7MHz clock and the CIC filter output. The decimation factor of the CIC filter involves a trade-off between modulator resolution (smaller bandwidth) and suppression of DCO drift and noise (wider bandwidth). A decimation factor of 1024 places the filter's first notch at ~425Hz, which ensures sufficient suppression of quantization noise (highlighted area in Fig. 2). After decimation, the PDΔΣM+CIC combination achieves a phase resolution of ~0.025m° (rms), which translates into negligible DCO jitter: <0.5ps (rms). A digital gain following the integrator sets the dominant pole of the entire FLL at ~50Hz.

Fig. 3 shows the circuit diagram of the DCO. It consists of a 9-stage current-starved ring oscillator, which is driven by a 5-bit coarse current-steering DAC, and a 13-bit fine current-output R-2R DAC. The coarse DAC covers a ±50% range around the 7MHz nominal output frequency, while the fine DAC covers a ±7.5% range with a 120Hz LSB. The FLL loop primarily controls the fine DAC using linear feedback, but the coarse DAC can be updated when the digital integrator is close to saturation. To ensure feedback stability, the fine DAC must be monotonic, and so a segmented architecture based on a 5-bit unary DAC and an 8-bit R-2R ladder was used. Its reference is generated from the supply voltage via a resistive divider, and then applied to the DAC via a buffer and a gain-boosted current mirror (g_m and M_1). An RC low-pass filter (R_{lpf}-C_{lpf}), with a cut-off much higher than the FLL pole, suppresses the DAC's wide-band noise, this reducing the DCO's jitter. This coarse-fine architecture results in a fine LSB small enough (18ppm) to keep the DCO's quantization noise well below the expected accuracy, while achieving a large enough range to handle process variations.

The prototype (Fig. 7) was fabricated in TSMC 180nm CMOS process. 12 samples in ceramic DIL packages were characterized. The two WB and PDΔΣM channels occupy 1.24mm² and draw 180µA from a 1.8V supply. The DCO occupies 0.35mm² and draws 250µA from a separate 1.8V supply. Digital circuitry is implemented in an external FPGA for flexibility.

The phase vs. temperature characteristic of the two WBs was initially determined with the help of a fixed 7MHz reference frequency. As in [8], after correcting for the inherent nonlinearity of the PDΔΣM (same for all samples & resistor types), each sample was trimmed at two temperatures (-35°C, 75°C), and then, for each resistor type, the remaining systematic error is corrected by a fixed 4th order polynomial (the same for all samples). The resulting polynomials and calibration coefficients were then loaded in the FPGA, the FLL closed and a second temperature sweep done to characterize its output frequency over temperature. Fig. 4 shows the frequency output of the 12 samples and the residual frequency error over temperature and supply voltage. The frequency error is less than ±250ppm over the temperature range from -45°C to 85°C, corresponding to a TC of 3.85ppm/°C (box method). Over a 1.7-2V supply range, the worst-case peak-to-peak frequency error is 548ppm, corresponding to a worst-case supply sensitivity of 0.18%/V. Fig. 5 shows the period jitter of the DCO in open-loop and closed-loop modes. The open-loop and closed-loop period jitter is $22ps_{rms}$ and $23ps_{rms}$, respectively, showing that short-term jitter is mainly dominated by the DCO. The Allan Deviation (Fig.5) is greatly improved by closed-loop operation, reaching a 250ppb floor beyond 3s measurement time.

Fig. 6 summarizes the performance of the frequency reference and compares it to state-of-the-art RC oscillators with low TC and long-term stability. The proposed frequency reference achieves the lowest inaccuracy over multiple samples and the lowest long-term drift. This demonstrates that fully-integrated CMOS RC frequency references can achieve enough accuracy at a low power consumption to enable wired communication standards on systems-on-chip.

Acknowledgements:
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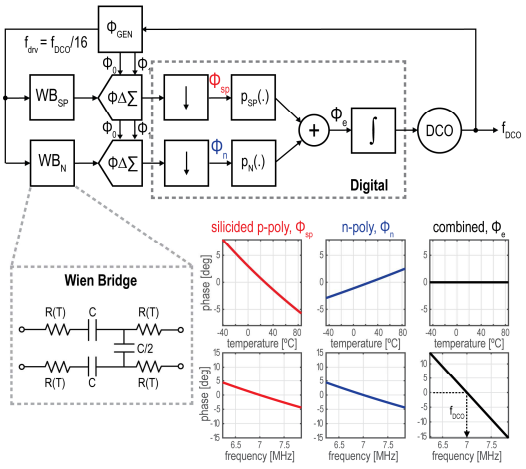

Figure 3.3.1: Block diagram of the proposed dual-RC reference (top), showing also the Wien Bridge (WB) filter (bottom left) and the simulated phase response of the two WBs and their combination (bottom right)

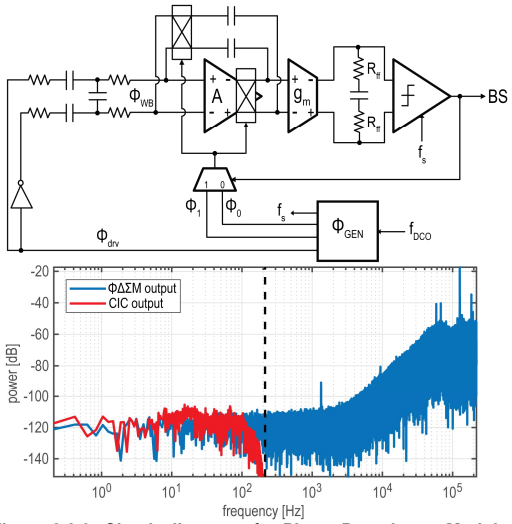

Figure 3.3.2: Circuit diagram of a Phase Domain ΔΣ-Modulator (PDSDM) (top) and PSD of the measured bitstream of the silicided p-poly bridge, using an external 7MHz clock (bottom)

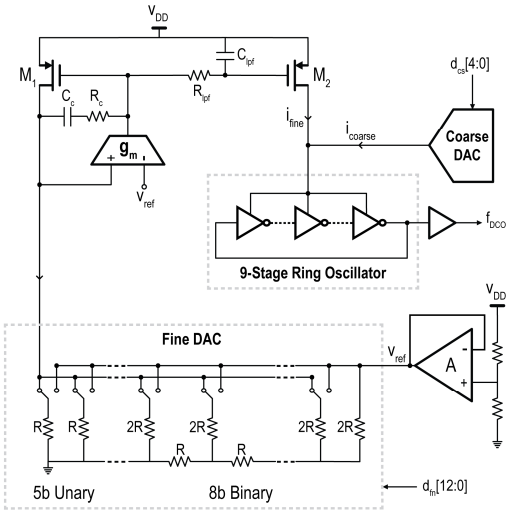

Figure 3.3.3: Circuit diagram of the Digitally Controlled Oscillator (DCO)

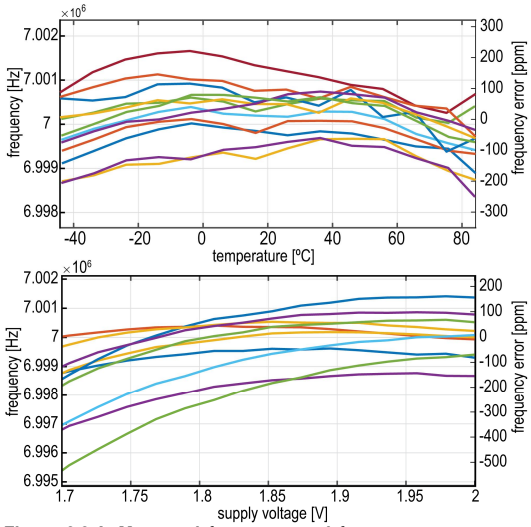

Figure 3.3.4: Measured frequency and frequency error over temperature (top) and supply voltage (bottom)

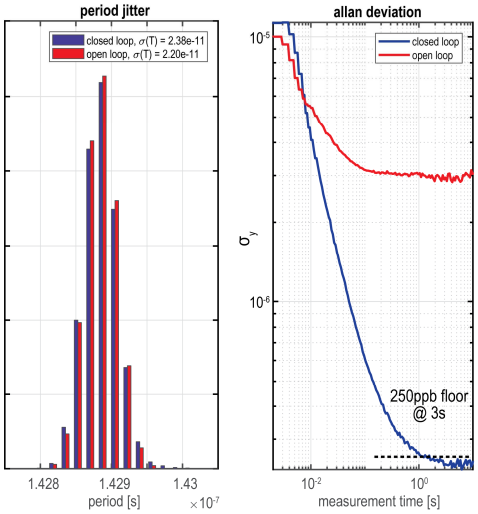

Figure 3.3.5: Measured period jitter (left) and Allan Deviation (right)

	This Work	Zhang VLSI2017	Jang [5] ISSCC2016	Hsiao VLSI2012	Choi [6] VLSI2016	Griffith [7] ISSCC2014	Savanth ISSCC2017
Process [nm]	180	180	180	60	180	65	65
Frequency [Hz]	8e6	24e6	3e3	3.2768e4	7.04e4	3.2768e4	1.3e6
TC [ppm/°C]	3.85	3.2[1]	13.8	16.67	27.4	38.18	96
T Range [°C]	-45 to 85	-40 to 150	-25 to 85	-20 to 100	-40 to 80	-20 to 90	0 to 150
Voltage [%/V]	0.18	0.03	0.49	0.125	0.5	0.09	0.49
V Range [V]	1.7 to 2.0	1.8 to 5.0	0.85 to 1.4	3.2 to 1.6	1.2 to 3.0	1.15 to 1.45	0.9 to 1.9
# of Samples	**12**	1	1	4	1	5	2
Allan Deviation Floor [ppm]	**0.25**	-	63	-	7	4	-
Power	750uW	200uW	4nW	4.48uW	99.4nW	0.19uW	0.92uW

[1] Utilizes a thin-film resistor

Figure 3.3.6: Performance summary and comparison table with previous work

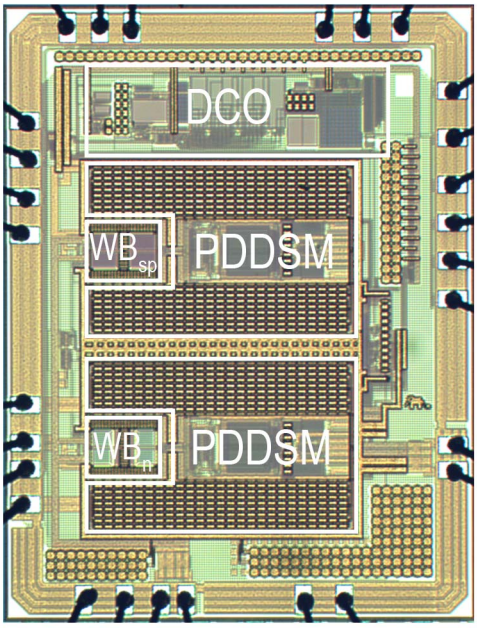

Figure 3.3.7: Chip Micrograph