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M.Sc. Thesis

Semi-custom VLSI Design and Realization of DC-DC Converters in UMC90

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Abstract

As CMOS technology is scaling down, the effect of voltage drop in power distribution network is becoming more prominent. Such voltage drops on power lines in a clock network introduces significant amount of skew, thereby degrading the signal integrity. With rising power consumption and decreasing supply voltages, the supply current will increase in future devices. The IR drops can be reduced by using large wires which negatively impacts the global routing. Thus to provide proper supply voltages, on chip DC-DC converters are designed.

The purpose of this project is to design an on-chip DC-DC converter targeted for System on Chip (SOC). In this thesis switched capacitor up converter and differential based voltage down converter is designed in UMC90. A new design for differential based voltage down converter is described to increase the efficiency of the converter. The specifications of the converters are defined by the system requirements. After meting the system requirements, layout of both converters is designed. The converters designed have high efficiency and small layout area.

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Semi-custom VLSI Design and Realization of DC-DC Converters in UMC90

Thesis

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1 Introduction

1.1 Motivation

From past few years there is increasing demand for portable devices leading to tremendous improvement in process technologies thereby shrinking devices to level which were earlier thought as impossible. With CMOS process technology scaling down to 90nm and even below, IR-drop is becoming an extremely important phenomenon in determining the performance and reliability of VLSI designs. Significant IR drops (e.g. >5% of V_{dd}) lead to reduced noise margins. As the supply voltage is reduced with technology scaling, the IR drop becomes even more problematic since the ratio of voltage drop to the ideal supply voltage level increases, thereby degrading the switching speed of the CMOS gates [2].

IR drop also introduces significant amount of skew due to voltage drops on power lines of switching devices in clock network further degrading the signal integrity [2]. Thus in order to achieve high clock frequencies, the power supply networks must be designed to supply current with minimal IR drops. The IR drop effect can be reduced by using large wires which in turn negatively impacts the global routing. To resolve the issues occurring due to IR drop in System-on-Chip (SoC), on-chip dc converters are proposed to provide local supply voltages to different parts of the chip.

1.2 Related work

The idea of on-chip DC–DC converters came to existence few years back. The passive components (i.e. inductor and capacitor) form an integral part of most of the architectures of dc converters. As inductor occupies around 30% area of the chip, technology of micro-fabricating the inductor on chip was developed [6]. Later inductor-less dc converters i.e. switched capacitor dc converters were designed for low power applications [3]. A new architecture of down converter consisting of reference voltage generator, voltage follower and pass device was designed for low power digital circuits [17, 20]. Most of the converters were designed with length of 0.18 um. However, with technology scaling, there was a tremendous impetus on reducing the converter size. In recent development, the challenges faced while designing converters with length of 90 nm were described.

1.3 Thesis goals

The goal of the thesis is to design on-chip DC-DC converters. A step up DC-DC converter is needed for supplying higher voltages to off chip drivers while step-down DC-DC converters is needed for supplying lower voltages to other parts of the chip. For designing on-chip dc converters following steps need to be taken.

- First the specifications of the converters have to be determined. The typical voltage range for digital circuits is 0V~5V. The efficiency and area of the converters are important parameters to consider while designing the converter.
- The next step is to choose a proper architecture for designing the converters considering the system requirements and trade offs.

After selecting proper architecture, implementation of the converters is to be done. The converter has to be designed such that the efficiency is as high as possible with the low ripple. Also the response time of the output voltage with respect to input should be low. Finally after meeting the required specifications, the layout of the converters have to be designed.

1.4 Thesis contributions

In this thesis, a switched capacitor up converter and differential based voltage down converter are designed in UMC090 for low power applications. The design of switched capacitor up converter is taken from [3]. A non overlapping phase clock generator is designed to provide drive signals to dc converter. A load model i.e. Random generator is designed in order to study the behavior of dc converters for switching circuits. The random generator is designed with low power of 6.68uW. The switched capacitor dc up converter can operates for input range of 0.6V ~3V and generates output of 1.2V~5.8V. The efficiency of the up converter is 70% and layout area of up converter is 110x135um^2. The design of differential based voltage down converter is done with input voltage range of 2V~5Vand provides output range of 1.2V~2.5V. The efficiency of down converter is 76 % and layout area of the down converter is 85x 45 um$^{2.}$

1.5 Thesis outline

The thesis is organized as follows:

Firstly Chapter 2 gives an overview of different types of basic converters being used for several years. The converters are classified as Isolating and Non-Isolating converters and further working mechanism of the converters is given. In the last section, the different applications of the dc converters are explained.

Chapter 3 introduces on-chip dc converters and the detail manufacturing process of micro-machined inductors. Later the basic principle behind charge pumps i.e. switched capacitors is explained. In the last section design choices are discussed.

Chapter 4 presents switched capacitor DC-DC up converter from [3] designed to operate input of range of 0.6V ~3V. The clock generator is designed using NOR and Inverter blocks to generate non-overlapping phase clock signals for the converter. In the last section load

model i.e. random generator is designed in UMC90 using D flip-flops and XOR gates to study the behavior of converter to switching load.

Chapter 5 introduces the working of differential based voltage down converter. The down converter is designed in UMC90 and operates for input range of 2V~5V. The circuit of down converter is modified to increase the efficiency of the converter. In the last section of the chapter comparison is made between the designed converter and Qianneng Zhou's converter.

Chapter 6, the simulations results for up and down converter are presented

Chapter 7 gives detail of layout process. The layout is made for both switched capacitor up converter and differential based voltage down converter in UMC90 technology. The LVS and DRC check are performed for both layouts.

Chapter 8 presents results and future work prospects.

2 DC-DC converter topologies

For different applications, different voltages are required. The output voltages of DC-DC converters range from one volt for special VLSI circuits to ten volt to tens of kilovolts in X-ray lamps. For System-on-Chip (SoC) the voltage ranges from 0V~3.3V. The microprocessors in SOC operate at 1V while voltages of about 2.5V/3.3V are needed for off-chip drivers. For devices requiring AC voltages voltage can be stepped up or down using transformer. For devices requiring dc voltages, DC-DC converters play the role of transformer for efficiently transforming the desired voltage.

In this chapter different kinds of DC-DC converters used for several years for different applications are explained. Some of the applications require high voltages while some require low voltages, thus depending on the application step up and down converters are used. Converters can be grouped on different criteria such as step up, step down, isolated and non-isolated converters. The DC-DC converters here are grouped as Non-isolating and Isolating DC-DC converters.

The chapter is organized as follows:
Section 2.1 describes the different Non-isolating converters;
Section 2.2 explains the Isolating converters;
Section 2.3 Applications of DC-DC converters and
Section 2.4 gives short Summary.

2.1 Non-isolating converters

In the Non-isolating converters, as the name explains that there is no dielectric isolation between the input and output. The need of isolation is eliminated as the voltage has to be stepped up or down by small ratio. The non-isolated converters are buck, boost, buck-boost converter, cuk and charge pump converters. The buck converters are used for stepping down the voltage where as the boost converters are used for stepping up. Then we have buck-boost converter and cuk converter used for both step up and down conversion. Lastly the charge-pump converter is used for either voltage step-up or voltage inversion in low power applications. The detail description of these converters is explained in the following section.

2.1.1 Buck converter

Buck converter is made of voltage source, voltage controlled switch, flywheel diode, inductor, capacitor and load R. A control circuit is connected between the base of MOSFET M_1 and one of the plates of capacitor. It is called the buck converter because the voltage across the inductor L bucks or opposes supply voltage. The circuit diagram of buck converter is shown in Figure 2.1. The output voltage of the buck converter is less than the

input voltage. Therefore it is also called as Step-down converter.

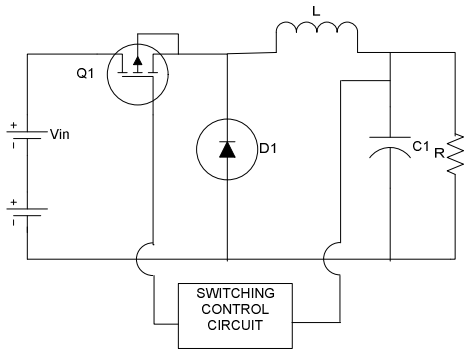


Figure 2.1 Circuit diagram of buck converter [15]

The switching of MOSFET M_1 depends on the output voltage at the fixed operating frequency with varying duty cycle. When M_1 turns on current from the source flows through M_1 to L, then C and finally to the load R. As current flows through L magnetic field is build up, causing energy to be stored in inductor. When M1 turns off, energy stored in the inductor supplies current to the load through diode D1. The voltage across the load is fraction of input voltage; this fraction is called duty cycle (D). Duty cycle in terms of voltage and time is defined by equation 2.1.

$$D = \frac{V_{out}}{V_{in}} = \frac{T_{ON}}{T} \tag{2.1}$$

Where Ton is the time for which transistor is on and T is reciprocal of operating frequency (1/f).Thus the buck converters output voltage can be varied as fraction of input voltage by varying switching duty cycle.

Power losses due to the control circuitry are usually insignificant when compared with the losses in the power devices like switches, diodes, inductors, etc. The non-idealities of the power devices are responsible for most of the power losses in the converter. Thus the efficiency of buck converter reduces due to the non-idealities of circuit components. The output waveforms of buck converter are shown in Figure 2.2.

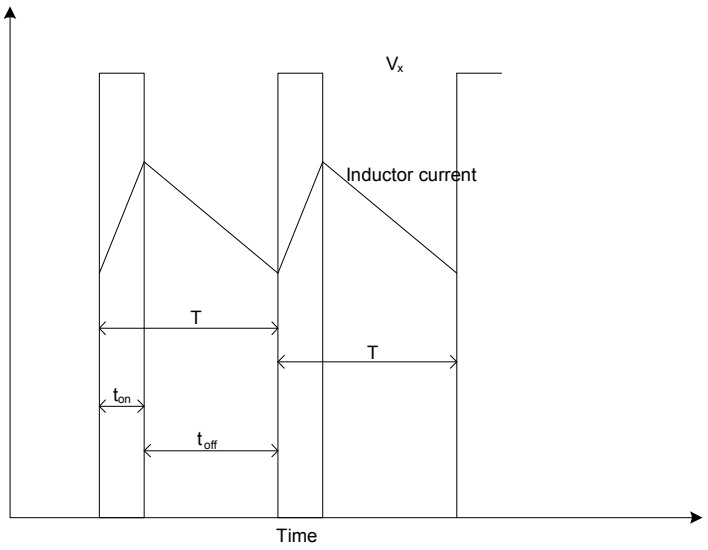


Figure 2.2 Output waveforms of buck converter

2.1.2 Boost converter

The boost converter has similar structure as the buck converter, but has components arranged in different manner. It is called boost converter because the voltage across inductor L adds to the input supply voltage to boost the voltage above input voltage. The output of boost is always greater than input voltage therefore the circuit is used when higher output voltage than input is required. Figure 2.3 shows the circuit diagram of boost converter.

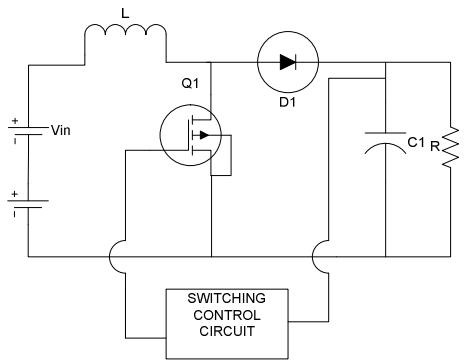


Figure 2.3 Boost converter [15]

When MOSFET M_1 is turned on current flows through L and Q_1, thereby storing energy in the inductors magnetic field. Thus no current flows through D_1 and the load current is supplied through the charge in capacitor C. When M_1 is turned OFF, the inductor L opposes any drop in current by immediately reversing its EMF (Electro Magnetic Field). Thus the inductor voltage adds to the source voltage, thus boosting the output voltage. The current

now flows from the source through L, D_1 and load, and then charging the capacitor again.

The voltage step up ratio is equal to

$$\frac{V_{out}}{V_{in}} = \frac{1}{(1-D)} \tag{2.2}$$

Where (1-D) is the proportion of switching cycle when M_1 is off

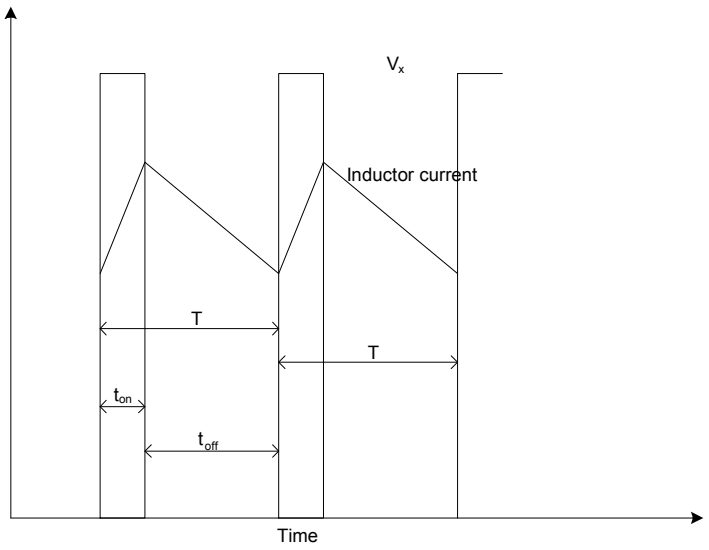


Figure 2.4 Output waveforms of boost converter

Figure 2.4 shows output waveforms of boost converter. Boost converter requires much more capacitor than buck converter because the capacitor supplies the entire load current when the switch is closed. Thus the boost converter has higher efficiency than the buck converter. Only for duty cycles approaching 100% the buck converter approaches the energy efficiency of boost converter.

2.1.3 Buck-boost converter

The components in buck-boost converter are MOSFET, diode, inductor and capacitor similar to buck and boost converter. The components are arranged in different way to provide step up as well as step down with polarity reversal or inversion as well. In Fig 2.5, the circuit diagram of buck-boost converter is shown.

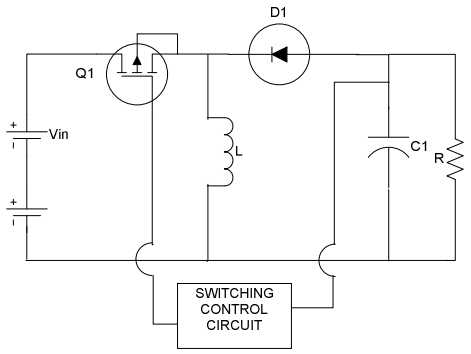


Figure 2.5 Buck-Boost Converter [15]

When MOSFET M_1 turns ON, there is path between inductor L and source voltage. As current flows through inductor L energy is stored due to magnetic field. As the diode D_1 is reversed biased no current flows through the diode D_1 to the load .The capacitor C_1 supplies the load current in this 'T_{on}' phase.

When MOSFET M_1 turns OFF, the path between inductor L and source is broken. The stored energy in the inductor L generates a voltage which forward biases the diode D_1 and current flows into load and capacitor, thus recharging the capacitor. The ratio between the output and input voltage is given by equation 2.3.

$$\frac{V_{out}}{V_{in}} = \frac{-D}{(1-D)} = \frac{T_{ON}}{T_{OFF}} \tag{2.3}$$

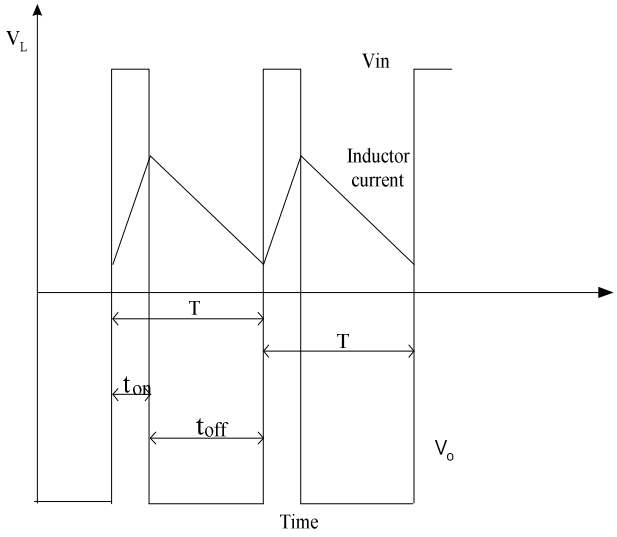


Figure 2.6 Output waveforms of buck-boost converter

The buck-boost converter acts like a voltage inverter as the output polarity is reversed with

reference to the input. The buck-boost converter has duty ratio between 0 and 1 therefore the output voltage can vary between lower or higher than the input voltage in magnitude. When the duty cycle is exactly 50%, V_{out} is essentially the same as V_{IN} with opposite polarity. Thus buck-boost converter may be used to generate negative voltage in equipment operating from a single battery.

2.1.4 Cuk converter

The buck, boost and buck-boost converters all transfer energy between input and output using the inductor, thus building the voltage across the inductor. The cuk converter transfers energy through the capacitor thus the analysis is based on current through the capacitor. The output is inverted as in the buck-boost converter whereas the circuit configuration is a combination of buck and boost converters.

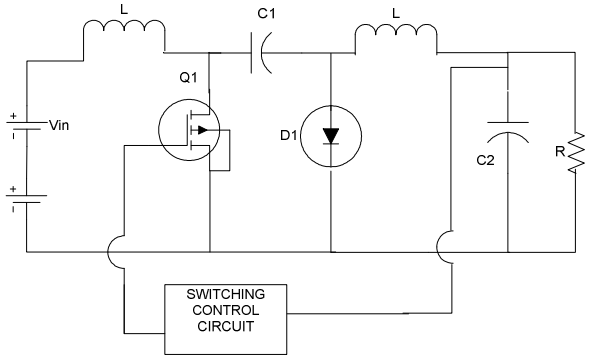


Figure 2.6 Cuk converter [15]

Figure 2.6 shows the block diagram of cuk converter. Assuming that the current through the inductors is essentially ripple free we can examine the charge balance for the capacitor C_1. When MOSFET M_1 turns on, the path of M_1 gets shorted whereas the path of the diode D_1 is open circuited .The current through C_1 is $\mathbf{I_{L1}}$ **a**nd energy is stored due to magnetic field in L_1. When M_1 turns off, thus the path across it becomes open circuit. The diode conducts and the current in C_1 becomes $\mathbf{I_{L2}}$.Thus the current flows from input source, through L_1, D_1 charging C_1 to voltage higher than V_{IN} and transferring to it some of the energy that was stored in L_1 in previous cycle.

When M_1 turns on again, C_1 discharges through L_2 into the load, with L_2 and C_2 acting as smoothing filter, whereas at the same time energy is being stored in L_1.

The ratio between the input and output is

$$\frac{V_{out}}{V_{in}} = \frac{-D}{(1-D)} \tag{2.4}$$

$$\frac{V_{out}}{V_{in}} = \frac{-T_{ON}}{T_{OFF}} \tag{2.5}$$

Thus in the cuk converter voltage can be stepped up or down depending on switching duty cycle. The advantage of the cuk converter is that the input and output inductors create a smooth current at both sides of the converter due to lower current ripple while the buck, boost and buck-boost have one side with pulse current.

2.1.5 Charge-pump converter

A charge-pump converter has quite different working mechanism than cuk converters. These converters operate by storing energy as electric charge in capacitor which is quite different from the above mentioned converters in which operation is dependent on storing energy in the magnetic field of inductor. The charge-pump converters are developed from traditional voltage doubling and voltage multiplying rectifier circuits. Figure 2.7 shows the circuit of charge pump converter.

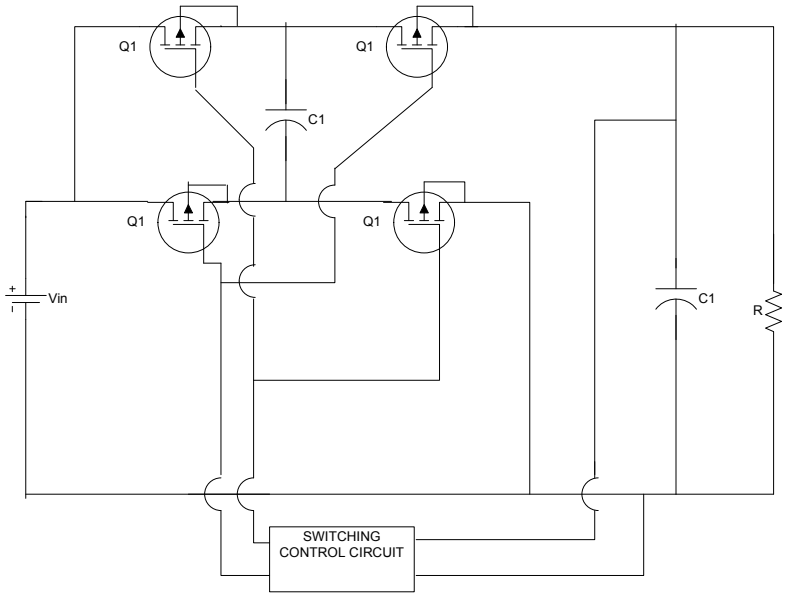


Figure 2.7 Charge-pump converter [15]

The charge-pump converter consists of four MOSFET switches and a capacitor C_1 called as the 'charge bucket' capacitor. When the voltage source is connected to circuit, first MOSFET M_1 and M_4 are turned on, thus capacitor C_1 is connected to input source, allowing it to charge to V_{IN}. Then these switches are turned off and M_2 and M_3 are turned on. Then the capacitor C_1 is connected in series with the input voltage source, across output capacitor C_2. As result now energy is transferred from C_1 to C_2 which charges twice as the input voltage. Thus C_2 provides load current during part of cycle when M_2 and M_3 are turned off.

The energy supplied to load in this type of converter flows through C_1 and as ripple current. Therefore this capacitor needs to have relatively high value and have low ESR (Equivalent Series Resistance) to minimize losses and be able to cope with heavy ripple current [15]. The charge–pump converters are used for relatively low current application as the converters rely for their operation on charge stored in capacitor. These converters are often considered to be cheaper and compact than inductor- type converters.

2.2 Isolating converters

For the above explained converters, there is no electrical isolation between input and output circuits, in other words they share a common connection. For many applications isolation is not required but for some applications complete isolation between the input and output is required.

The two main types of isolating converters are forward converter and fly back converter. The working principle behind these converters is that the converters depend for their operation on storing energy in the magnetic field of the inductor.

2.2.1 Fly back converter

The Figure 2.8 presents a fly back converter [15] which is similar to the buck-boost converter. The inductor in the buck-boost converter is replaced by a transformer. As seen before, the buck-boost converter works by storing energy in the inductor during the on state and releasing it to the output during the off state. Now with the transformer the energy storage is in the transformer core.

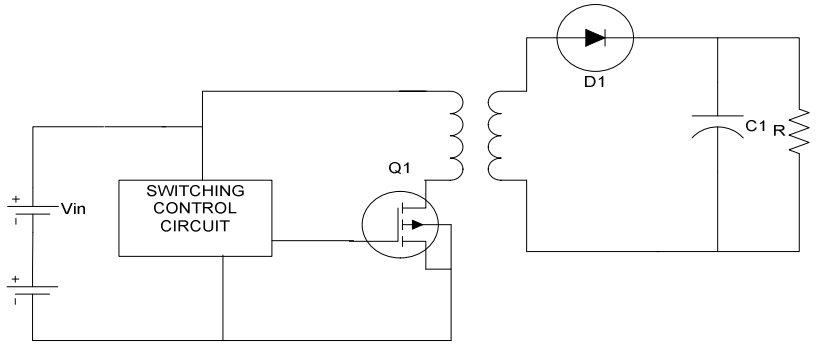


Figure 2.8 Fly back converter [15]

When the MOSFET M_1 turns on, current starts to flow from the source through primary winding L. Thus energy is stored in the transformers magnetic field. Later M_1 turns off, and then the transformer tries to maintain current flow through L1 by suddenly reversing the voltage across it. Due to transformer action higher Fly back pulse is induced in secondary winding L2. Thus current is being supplied to load and to recharge capacitor C1 through diode D1.

The Fly back converter has two distinct phases in its switching cycle. During the first phase M_1 conducts and energy is stored in transformer core through the primary winding L1. During second phase M_1 turns off, the energy stored in the transformer is transferred to the output of the converter through secondary winding L2. The ratio between input and output depends not only on the turn's ratio but also magnetic field, winding inductance, and the length of time that Q1 is turned on. The fly back converters have high turn's ratio to allow a high voltage step-up ratio. Also the core in these converters needs to be large to avoid saturation, as the magnetic flux in its transformer core never reverses in polarity. For automatic regulation of the output voltage, a small winding is added to fly back transformer to allow sensing of fly back pulse amplitude close to the output voltage and then feedback MOSFET switching control circuit.

2.2.2 Forward converter

The forward converter consists of ideal transformer that converts the input AC voltage to an isolated secondary output voltage. Thus energy transfer is directly between input and output in one step than the fly back converter which requires two phases for energy storage and delivering to the output. Figure 2.9 shows the circuit diagram of forward converter.

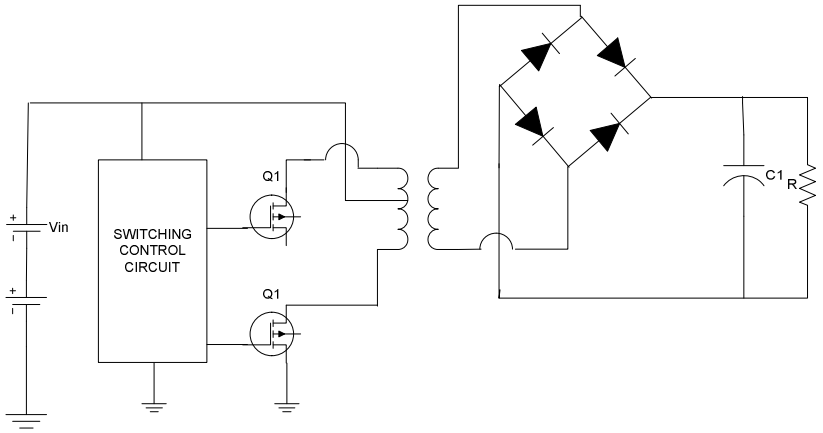


Figure 2.9 Forward converter [15]

The forward converter is shown in Figure 2.9 is push pull type. As we see it has two switching MOSFETs M_1 and M_2 connected to either end of a center tapped primary winding on transformer. The switching control circuit never turns M_1 and M_2 ON at the same time. The positive terminal of input voltage source is connected to the center tape and the negative terminal is connected to the sources of MOSFETs. Thus the input voltage is first connected to one half of primary winding then across the other, thus current flows through L1 then L2.

The MOSFETS Q1 and Q2 convert the dc input voltage into high frequency ac square wave.

The secondary of the transformer, during each half cycle delivers the same ac square wave with a peak voltage equal to

$$V_{ac(pk)} = V_{in} \frac{L_3}{L_1} \tag{2.6}$$

L1 and L3 are the number of turns on each winding. The diodes D1-D4 are connected as bridge rectifier which is then connected directly to the secondary winding. Thus the ac square wave that appears across L3 is rectified back into high voltage dc, thus feeding the load and maintaining the charge on the filter capacitor C1. Thus the dc output voltage Vout will be equal to the peak ac output from the transformer, while ignoring the diode voltage drops. Thus the output voltage can be given as

$$V_{out} = V_{in} \frac{L_3}{L_1} \tag{2.7}$$

The forward converter is used like a transformer for dc, for converting the dc energy into ac. After the transformation the ac voltage is rectified back into dc. The chances of saturation are less in forward converter as compared to fly back converter, as the polarity of magnetic flux in the transformer core reverses for each alternate half cycle. Also the forward converters have more tighter and predictable relation between input and output making them suitable for high power applications.

2.3 Applications of dc-dc converters

The step-down choppers find most of their applications in high performance dc drive systems like electric traction, electric vehicles and machine tools. The dc motors with their winding inductances and mechanical inertia act as filters resulting in high quality armature currents. The step up choppers are primarily used in radar and ignition systems. The dc choppers can be modified for two quadrant and four quadrant operation. Two quadrant choppers may be part of autonomous power supply systems that contain battery and such renewable dc sources as photo voltaic arrays, fuel cells or wind turbines. Four quadrant choppers are used in drivers where the breaking of dc motor is desired like transportation system with frequent stops.

In isolated dc-dc converters, multiple outputs are possible with additional secondary windings of transformers. Only one output is regulated with feedback loop, but other outputs depend on the duty ratio of regulated one and on their loads. The forward converter is mostly used in low- medium (up to several hundreds of watts) power applications whereas the fly back converter is popular in low power applications (up to 200W).

DC-DC converters also have major applications related to the utility ac grid. For critical

loads, if the utility grid fails, there must be backup source of energy like battery pack. The need for continuous power delivery gave rise to various types of uninterrupted power supplies (UPSs). The dc-dc converters are used in UPSs to adjust the level of a rectified grid voltage to that of back up source. Bidirectional dc-dc converters are used as in two modes, during normal operation the energy flows from the grid to the back up source and during emergency conditions, the backup source must supply the load.

2.4 Summary

The dc-dc converters can be viewed as dc transformers that can deliver different values of voltages or current to the load than the input source. The selection of topology of dc-dc converter is determined by required input and output voltages, which can be additionally adjusted with the turn's ratio in isolated converters. The other important aspect to consider while deciding the topology are the power levels, voltage and current stresses of semiconductor switches and utilization of magnetic components.

The Table 2.1 shows ratio V_o/V_{in} of converters for continuous current mode operation.

Table 2.1 Various converters with their V_o/V_{in} ratio

Type of converter	**V_o/V_{in}**
Buck	D
Boost	1/1-D
Buck-Boost	-(1/1-D)
Cuk	-(1/1-D)

3 System on-Chip DC-DC converters & design choice

In the previous chapter various DC-DC converters used from years were explained in detail. Now this chapter focuses on system on-chip DC-DC converters. Miniaturization and integration of dc-dc converter is becoming an area of great interest due to the tremendous requirement for voltage conversion in portable electronics equipment. The main challenge of these converters is to minimize and integrate passive components. Also as the processor core voltage drops below 1V, the demand of power supply from the load increases, thus making lower voltages difficult to achieve at faster frequencies due to lower duty cycle. In this chapter two most commonly used on chip converters, charge pumps (switched capacitor) and inductor based converter are discussed.

The chapter is organized as follows:
Section 3.1 gives an overview of system on- chip converters;
Section 3.2 explains inductor based converters;
Section 3.3 explains switched capacitor converters;
Section 3.3 gives short summary.

3.1 Overview of system on-chip dc-dc converters

The demand for portable devices has been increasing tremendously in past few years. The dc-dc converters are required to supply different voltages to various circuits. The overall converter miniaturization is obstructed by the passive components in these converters. The size of these passive components i.e. inductor and capacitor can be reduced by using higher switching frequency of the converter. At higher frequencies the value of inductances and capacitances reduces. There are different ways in which inductor can be fabricated on the chip. An overview of inductor based converters and switched capacitor converters are given.

3.2 Inductor based dc-dc converters

As we have already seen passive components like inductor play an important role in the designing of dc converters as they occupy significant fraction of the volume (around 30%) of the power converters. Thus the selection of inductor is an important deciding factor for the overall performance and size of the converter itself. The most common inductor based DC-DC converters is the buck, boost and Single Ended Primary Inductive Converter (SEPIC). The buck and boost provide unregulated output voltage whereas the SEPIC provides regulated output voltage which can be higher or lower than the input voltage as required. Integrating inductors on the chip was considered a difficult task before but nowadays with the increasing demand of on chip dc converters, new technique of fabricating inductors i.e. micromachining is explained in later section.

3.2.1 Introduction to micro fabricated inductors

From many years significant research has be done for fabrication of micro inductors onto the chip using IC or MEMS type fabrication techniques. Thus the realization of on chip DC-DC converters was considered a difficult task before due to the absence of appropriate planar chip inductors. Nowadays using micro-fabrication techniques, inductor can be integrated into the IC or package.

Micro fabrication techniques produce thin films and fine patterning which help to reduce the eddy current losses. A micro-fabrication technique uses low temperature processes which are compatible with direct fabrication of the inductor on the active components. The micro-inductor technology must be implemented in cost effective manner and size of the inductor is an important factor for cost-effectiveness. The cost of the final micro fabricated devices is related to the number of steps used in fabrication and substrate area occupied by the device

3.2.2 Fabrication steps

During the fabrication of micro machined inductors number of steps has to be carried out. To begin with, the fabricated inductors need to have good magnetic coupling, as low as possible magnetic losses at high frequencies and low resistance in the windings. Thus to achieve good coupling between the windings, a magnetic material with relative permeability of 300 is used as core. Ni 45Fe55 is chosen because it has high resistivity of 50u*ohm*cm to reduce the eddy current losses, also has low coercivity to reduce the hysteresis losses and high saturation flux density of 1.5T for high power density [23]

The fabricated micro-inductor consists of racetrack shaped copper coil and is surrounded all over by magnetic material. There are different ways to deposit the magnetic core layers like screen printing, sputtering and electroplating [21-23]. Electro deposition is used to form thicker core and is considered a better choice as its economical than screen printing and sputtering. The Q factor of micro machined inductor is lower than sputtering and electroplating, due to the conductivity of electroplated magnetic material. Thus as the operating frequency increases, the eddy current loss in the magnetic core becomes large. Normally these planar inductive components are operated at high frequencies as they have better thermal management and high power density as compared to conventional component magnetic core.

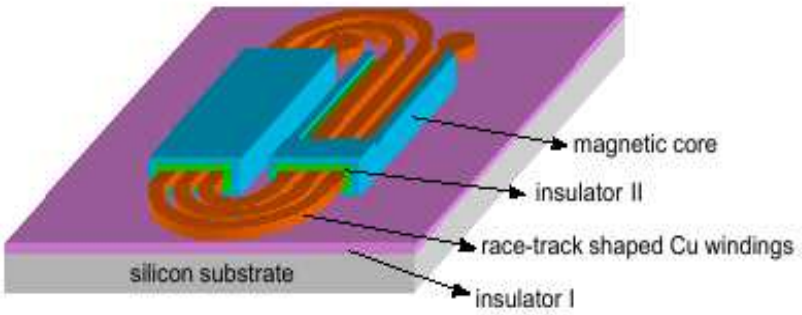


Figure 3.1 Schematic of micro-machined inductor [22]

Figure 3.1 presents the schematic of micro-machined inductor. The steps for fabrication of the device are taken from the references [21-23]. The micro fabricated inductor consists of four rectangular NiFe cores and four single turn copper windings. The copper windings are placed between the layers of magnetic material. First of all the silicon substrate is coated with 3-um- thick layer of insulation (BCB-benzocyclobutane). Then a seed layer of titanium and copper (Ti/Cu) is deposited by sputtering onto the insulation. Later the seed layer is masked using a photo resist (AZ9260). Then layer of magnetic material like alloy of Ni 45Fe 55 (i.e. Nickel 45% and Iron 55%) is then electroplated and patterned using a pulse reverse plating technique [25]. Later the photo resist mask and seed layer are removed. Now the second layer of magnetic material is electroplated by following the same steps as during the first layer of magnetic material.

The insulator BCB is placed between the magnetic layers to block the eddy current thereby reducing the eddy current losses. Later the Cu windings are deposited. To provide insulation between magnetic material and copper windings a layer of SU8 epoxy type photo resist is deposited on the magnetic material. Then seed layer Ti/Cu is deposited on SU8.

After depositing the seed layer it is again masked by photo resist AZ9260 for electro depositing the copper windings at a height of 60um. Then again these windings are covered with a layer of epoxy type. Photo resists SU8 for isolating them from top magnetic material. At last to achieve a closed magnetic path, a final magnetic layer is deposited. Thus the fabrication of micro inductors is completed.

The advantages of micro fabricated inductors is that its uses less substrate area. These inductors also allow more cross sectional and surface area for low dc and ac resistance respectively.

3.3 Switched capacitor converters

The switched-capacitor dc converters are also called as "charge pumps". A charge pump is a circuit which uses a capacitor to either increase or invert the input voltage. The charge pump capacitor is called a flying capacitor as the switches resemble flapping wings as the change state. They are also known as inductor less dc converters. As these converters do not use inductor as storage element they offer better characteristics than inductor based dc converters. The efficiency of these charge pump circuits is around 80-85%.

3.3.1 Working principle

The working principle of charge pump circuit is quite simple. During charging, the flying capacitor is charged through switches. Later the capacitor is connected to the load in series with the input supply to provide a voltage above the input. The switching action behaves like an equivalent resistance that depends on the switching frequency and relative values of the capacitors. A capacitor is connected at the output stage to provide smooth output voltage.

The mostly commonly used architecture of charge pump is the doubling charge pump. The figure 3.2 shows an unregulated doubling charge pump.

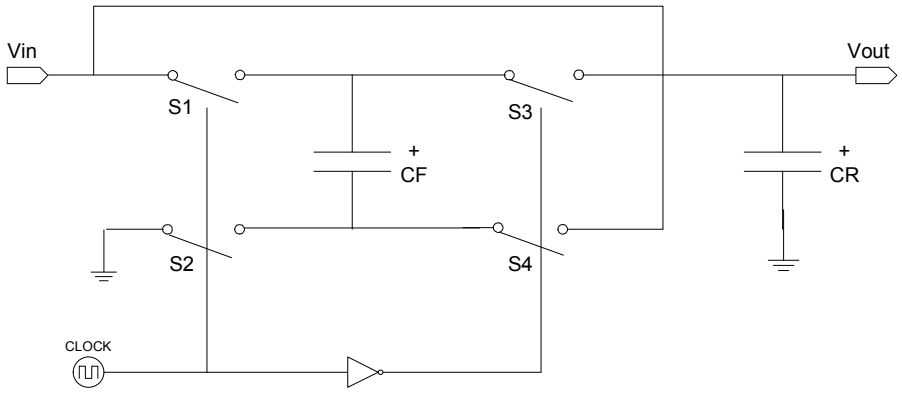


Figure 3.2 Unregulated doubling charge pump.

The circuit consists of four switched S1, S2, S3, S4, CF and CR. C_F is known as the flying capacitor which transfers the energy stored in it and C_R is external output capacitor known as reservoir capacitor.

During the first phase switches S1 and S3 are closed while S2 and S4 are open. The capacitor CF charges to input voltage through S1 and S3. From the previous cycle voltage V_{IN} is transferred to the reservoir capacitor CR. The capacitor CR now charges to $2V_{IN}$. In the next phase switches S1 and S3 are open and switches S2 and S4 are closed. The voltage across CF is V_{IN} from the previous charging cycle, this voltage V_{IN} is transferred to the output capacitor CR in the present phase. The voltage across CR now is 2Vin. Thus we can see the output voltage is twice of the input voltage, therefore it is called as doubling charge

pump. As the output changes according to the input voltage and load, it is called as unregulated doubling charge pump. For regulated output voltage the circuit is modified by adding a simple feedback loop to the existing circuit.

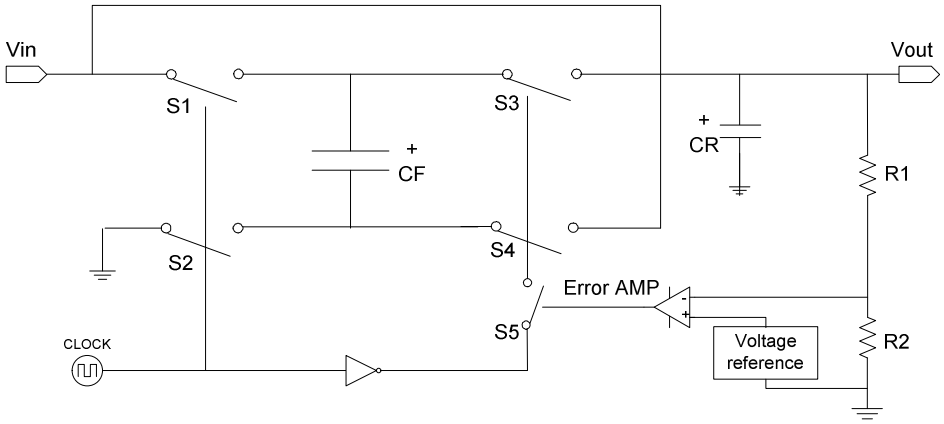


Figure 3.3 Regulated charge pump

Figure 3.3 shows a regulated charge pump. The feedback loop consists of a switch S5, comparator, and voltage reference control and resistor divider. The switch S5 is used for controlling the switches S2 and S4. The switch S5 is then controlled by the comparator and the voltage reference. At one of the input of the comparator is resistor divider and the other input is voltage reference. This comparator has built in hysteresis to prevent oscillation.

The output voltage of this charge pump is regulated by the feedback loop by controlling the switching on and off of the switches S2, S4 and S5. When the output voltage V_{OUT} is below the preset regulated output voltage in the discharge phase, the comparator closes switch S5, which in turn closes the switches S2 and S4. When switches S2 and S4 close, stored energy is transferred from the capacitor CF to capacitor CR and then to the load to bring V_{OUT} up to the preset regulated output voltage. When V_{OUT} reaches above the preset regulated voltage, the comparator opens switch S5, which in turn opens switches S2 and S4 thereby terminating the energy transfer from CF to CR.

In the later case when the output V_{OUT} is above the preset regulated output voltage, the comparator opens switch S5 which in turn opens the switch S2 and S4, thereby terminating the energy transfer from C_F to C_R and the load, thus bringing the output V_{OUT} below the preset regulated output voltage. In case during the discharging phase if output V_{OUT} cannot be brought down the preset regulated output voltage, the switches S2, S4 and S5 stay open.

The regulated output voltage in the charge pump can be made higher or lower than the input voltage by manipulating the value of resistors R1 and R2 in the resistor divider. The charge pump thus gives regulated output voltage. These charge pumps operate at high frequencies, as at higher frequencies the size of capacitance reduces. Charge pumps are used in many portable applications like notebook computers and mobile phones. They are typically used in

applications where a low current is necessary such as in bias supply for an IC or FET amplifier. Charge pumps are not able to supply large amounts of current without using large value capacitors. Usually the practical limit to the output current is approximately 250mA.

3.3.2 Design choices

While comparing the inductor based dc converters with the switched capacitors converters following points can be concluded

1. The complexity of inductor based converters is high as compared to the switched capacitor converter. The switched capacitor converters are overall simpler in design as compared to inductor based converters as they have lower area and cost.
2. The output current of the switched capacitor is low while the output current of inductor based converters is relatively high due to stored magnetic filed in the inductor.
3. The efficiency of switched capacitor converter lies in the medium range whereas the efficiency of inductor based converters lies between the medium and high range.
4. The inductor based converters are expensive as compared to switched capacitor converter. The inductor based converters are bulky. As the area of the converter increases, the overall fabrication cost increases.

Both these converters have their advantages and disadvantages. Depending on the system requirements and tradeoff, choice is made between the inductor based and switched capacitor converters.

In this thesis the application of DC- DC converters is for on-chip ASIC implementation. The efficiency and size of the converter are the most important parameters of the design. Thus considering the system requirements and trade offs of the converters; Switched capacitor dc converters have been selected. Switched capacitor dc converters are simple, efficient and less expensive as compared to inductor based converters.

3.4 Summary

Switched capacitor DC-DC converters in comparison with dc converters using micro machined inductors are used in applications where high conversion efficiency is important and where power levels are in mill watt range. A switched capacitor DC-DC converter is not limited by the number of components or circuit complexity. They show high circuit flexibility in sizing switches and capacitors as compared to other discrete circuit designs. However switched capacitors are limited by their output current capacity. They also exhibit large parasitic bottom plate capacitance that increases switching losses in the converter which then limit the achievable power efficiency.

4 Designing of switched capacitor up converters

In the previous chapter an overview of system on chip dc-dc converters was given. According to the requirements a choice is made between the inductor based converters and switched capacitor converters. As we already saw switched capacitor converters are simple, efficient and less expensive than inductor based converters. Thus switched-capacitor DC-DC converters are preferred as compared to inductor based converters in many low-power and medium-power applications. Thus depending on the requirements of the application, choice can be made between the converters, as both the converters have the trade offs. In this chapter switched capacitor up converter for low power applications is implemented in UMC90 technology.

This chapter is organized as follows:
Section 4.1 gives introduction to switched capacitor DC-DC converters;
Section 4.2 explains the key components in DC-DC converters along with designing of the converter;
Section 4.3 explains the design of switched capacitor dc converters with designed clock generator;
Section 4.4 describes the design of random generator as load model.

4.1 Introduction

The switched capacitor (SC) DC-DC converter replaces the magnetic coils in the inductive DC-DC Converter with few capacitors and array of switches thus making it possible to fabricate the entire converter on a single chip. In the SC DC-DC converter, the switching array is responsible for charging and discharging the capacitors so that a desired output supply voltage is provided to power the electronic device. The advantages of SC DC-DC converter include high integration, low fabrication cost, high switching frequency, and medium-to-high conversion efficiency and reduced voltage mode electronic interference (EMI)

The drawback of SC DC-DC converter is that it suffers from signal dependent current spikes mainly due to the nonzero switch on-resistance (R_{on}). While considering the ideal case, a perfect switch with zero on resistance is used to charge a capacitor in an SC DC-DC converter, the electric charges flows into the capacitor instantaneously, while the voltage across the capacitor changes slowly and the resulting current waveform consist of a sequence of impulse functions. However for a real switch with nonzero on-resistance, the charge cannot be transferred instantaneously. Thus the output current waveform contains high pulse width current spikes instead of zero pulse width impulses. The value of R_{on} depends on the input signal, thereby introducing signal dependent distortions to the converter. Thus SC DC-DC converters suffer from current mode Electromagnetic Interference (EMI) in the form of tones or harmonics.

The achievable conversion efficiency reduces as R_{on} dissipates energy. Thus to minimize the power losses due to R_{on} , the MOS transistors that are implemented as switches in an SC DC-DC converter must have large (W/L) ratios, where W is the effective gate width and L is effective gate length.

Further we see as the capacitors of the converter are implemented on chip, the parasitic capacitances will also introduce power loss, thereby further reducing the conversion efficiency. To achieve high conversion efficiency advanced process technologies are needed which are able to fabricate on chip capacitors with low parasitic capacitances.

4.2 Designing of switched capacitor dc up converters

In this section the implementation of on-chip switched capacitor DC-DC up converter is described. There are numerous literatures available on on-chip DC-DC converters. As we saw in the previous chapter a choice is made among the inductor based and switched capacitor based converters. The switched capacitor converters are preferred as its matches the requirements of our application. Figure 4.1 shows architecture of SC converter. A non-overlapping phase clock generator is designed to provide drive signals to the converter. The switched capacitor converter is designed in UMC90 and is taken from [3] .Later in this section random generator is designed which is acts as load model.

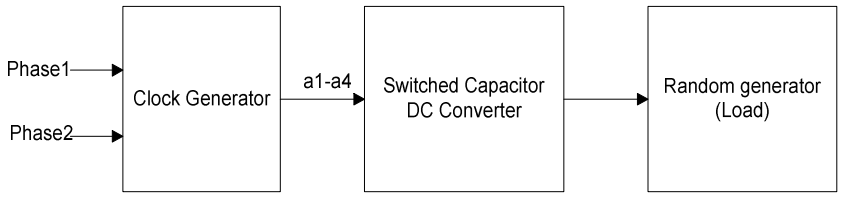


Figure 4.1 Architecture of switched capacitor converter

The switched capacitor DC-DC converters consist of switches and energy transfer capacitors in the power stage. The converter cycles through a number of switched networks as the switches are periodically turned on and off .While designing the on-chip converter low power, efficiency of the converter and area occupied by the converter are considered as important parameters. This on-chip SC converter is capable of generating various dc voltages from the external dc supply voltage. Before moving to the actual implementation of on-chip SC converters in UMC90 technology, the basic voltage doubler is described.

Figure 4.2 shows ideal switched capacitor voltage doubler. The switched capacitor voltage doubler consists of four switches, two capacitors C_1 and C_{out} and load R. The basic voltage doubler is required for step up voltage conversion. It consists of two switching networks. During the first phase all switches '1' are closed. The capacitor C_1 is charged to supply voltage through switches '1'. Then in the second phase all switches '2' are closed. In the

second phase, voltage V_{dd} across C_1 in the previous phase is transferred to the output. Thus 2Vdd voltage appears across the output capacitor $C_{out.}$ The circuit is therefore called as voltage doubler, as the output voltage of the circuit is twice the input voltage. Thus the conversion ratio for the voltage doubler is $M = (V_O/V_{DD}) = 2$ whereas for ideal SC converter when unloaded has dc voltage conversion ratio $M = (V_O/V_{DD})$.

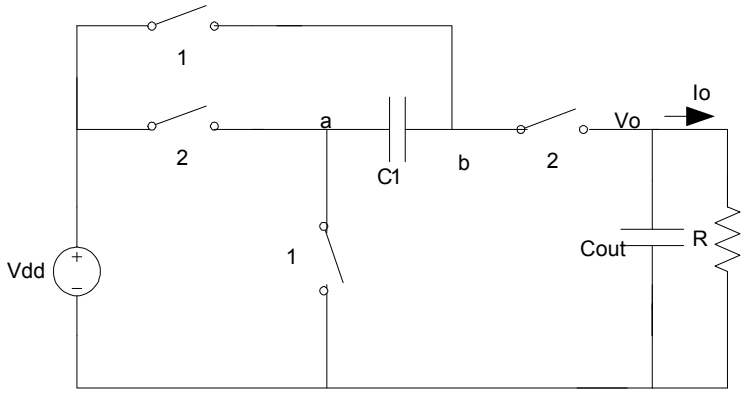


Figure 4.2 Switched capacitor voltage doubler

The gate drive signals for the switches in SC converters must be higher than the supply voltage V_{DD}. While designing the switched capacitor converter area and efficiency of the converter is of prime importance. In the traditional power converters circuit complexity and the number of power stages were the main cost constraints

4.3 Designing of switched capacitor Converter

In this section first a block diagram implementing the opposite phase SC converters is shown, and then a non overlapping phase clock generator is implemented to generate the gate drive signals a_1 to a_4 for the converter.

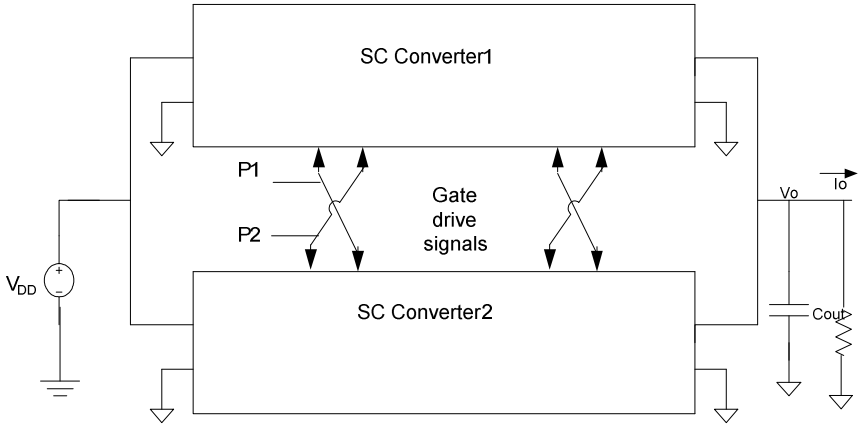


Figure 4.3 Block diagram of switched capacitor converter

Figure 4.3 above shows the block diagram of opposite phase SC converter connected in parallel. The two SC converters are connected to the input supply voltage and opposite phase clock signal p1; p2 at constant switching frequency f is applied to the converter. The circuit configuration requires no positive feedback due to the parallel, opposite phase, cross coupled converters. A non-overlapping phase clock generator is implemented to generate the appropriate gate drive signals for the SC converter. The non-overlapping phase clock generator generates four gate signals a1, a2, a3, a4 which are then applied to the gates of the MOSFET. The two SC converters have the same but opposite phase pulsating voltages at their nodes .The pulsating voltages from one converter are used as gate drive signals in other converters.

4.3.1 Implementation of non-overlapping phase clock generator

In analog as well as digital circuits clock play an important role in the designing of the circuit. Ideally clock signals should have zero rise time, fall time and skew and also constant duty cycles. In practical cases however clock signals have nonzero rise and fall times and non zero skew along with varying duty cycles. While designing switched capacitor DC-DC converters, the clock signals control the switching activities thereby play an important role in determining the entire operation of the circuit.

The switched capacitor dc converter implemented in this thesis requires non-overlapping phase clock signals to be applied to the gates of the MOSFETS. Non-overlapping signals are signals operating at the same frequency. The non overlapping signals while making transition from high to low or vice-versa, during this period none of the signals are high. The signals a1and a2 are non overlapping signals generated for the SC dc converter.

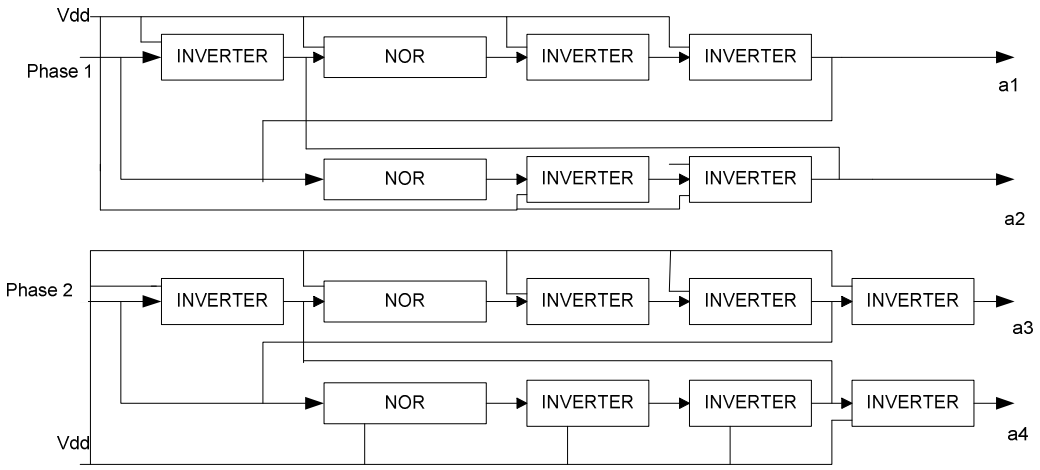


Figure 4.4 Circuit of two phase non overlapping clock generator**.**

Figure 4.4 shows circuit of two phase non overlapping clock generator. The non-overlapping two phase clock generator circuit is based on cross coupled RS flip-flop. The circuit is

divided into two parts where first part contains two NOR gates and five inverters and the second part contains two NOR gates and seven inverters. Phase1 and Phase2 signals are applied to the circuit and at the output signals a1, a2, a3 and a4 are generated. The signals a1, a2 are non-overlapping signals while a3, a4 are overlapping signals. The inverters and NOR are build with basic gates like NMOS and PMOS. The inverter consists of a PMOS and NMOS gate. The NOR consists of two PMOS and NMOS.

The inverters are used to generate delay in the circuit. With the inverters the required gate delays for the circuit can be chosen. The delay in the inverters decides the non-overlap period. The size of the gates are modified to met the overlap requirements and drive considerations. The circuit can be implemented also with NAND gates but with a buffer inverter on the output.

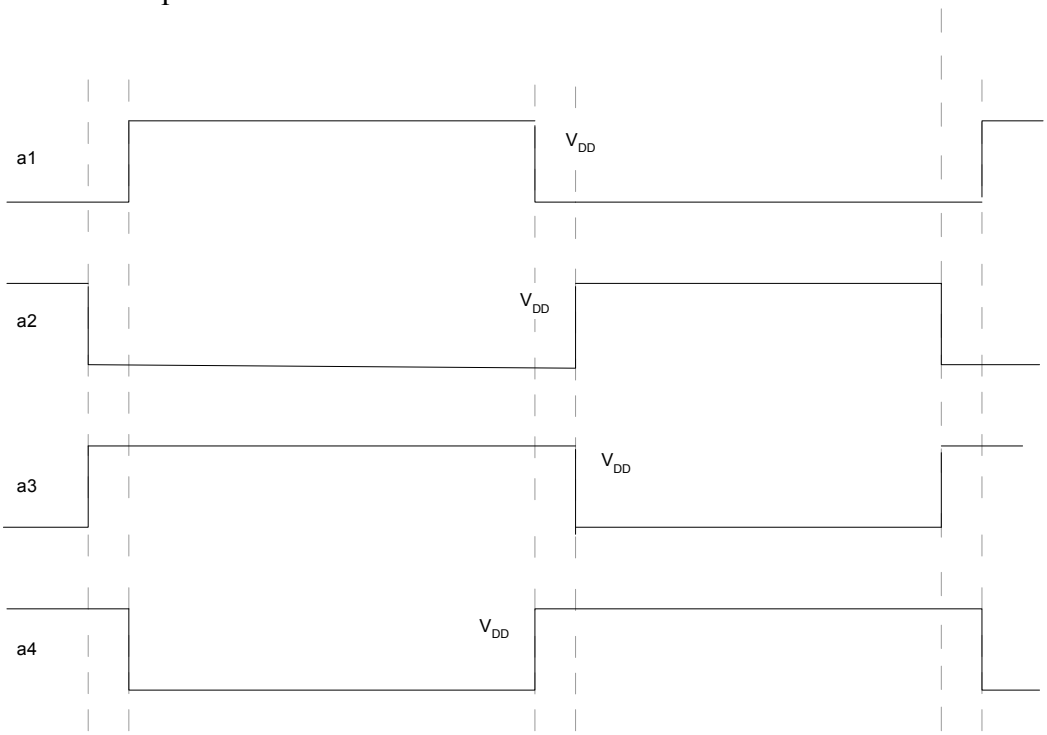


Figure 4.5 Output waveforms of clock generator

The output waveforms of clock generator are shown in Figure 4.5. The signals a1, a2, a3 and a4 act as drive signals for the voltage doubler. For portable applications, mixed signal VLSI applications and auxiliary supplies for analog portions of low voltage, high power conversion efficiency and area taken are important. Thus conduction and switching losses should be considered for optimizing the design for switching frequency and component sizes.

4.3.2 Designing of voltage doubler

In this section the basic voltage doubler is implemented. As in the previous section we already saw the block diagram of two opposite phase SC converters connected in parallel.

Now we implement the switched capacitor DC-DC converters. The switches in the converter are realized using NMOS or PMOS device or by series or parallel combination.

4.3.2.1 Introduction doubler and tripler circuit

The supply voltage Vdd along with opposite phase clock signals p1 and p2 is applied to the converter. These two phase clock signals p1, p2 at a constant switching frequency are applied to the two phase non-overlapping clock generator. In the previous section non-overlapping phase clock generator is implemented to generate the gate drive signals a1, a2, a3 and a4 which are then applied to the gates of the MOSFET.

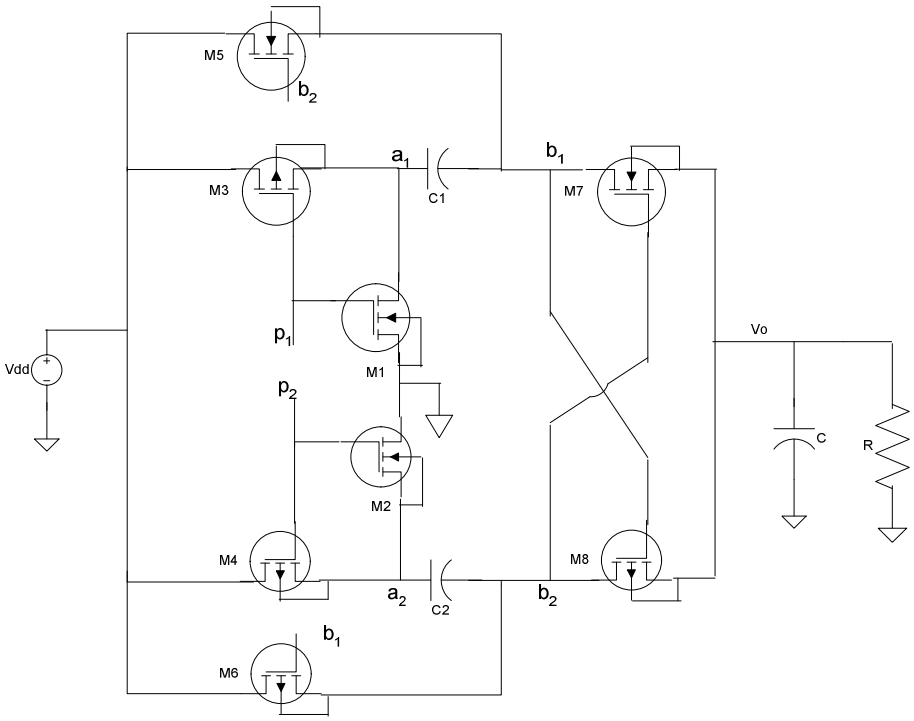


Figure 4.6 Voltage doubler based on block diagram of Fig 4.3 [3]

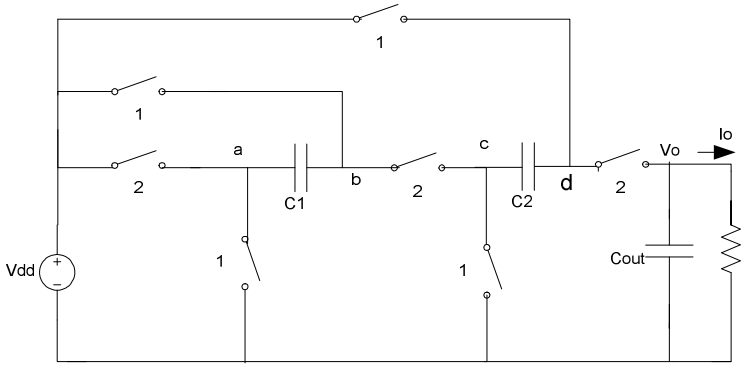
The implementation of the voltage doubler is shown in Figure 4.6. The clock signal p_1 is applied to MOSFET M_1 and M_3 while clock p_2 is applied to MOSFET M_2 and M_4. The above circuit has two converters, one contains MOSFET M_1, M_3, M_5, M_7 and C_1 and other converter contains M_2, M_4, M_6, M_8 and C_2. The input Voltage V_{DD} and the output capacitor are common to both the SC converters. The MOSFETs M_5, M_6, M_7 and M_8 are cross coupled. The working of the SC converter is explained in following paragraph.

During the first phase p_1 is high i.e. $V_{dd,}$ thus M_1 turns on. Thus voltage across node a_1 reaches V_{dd}. At the same time p_2 is low i.e. 0, thus M_4 turns on and voltage across node a_2 is V_{dd}. Now the voltage across C_2 reaches $2V_{dd}$ as there is charge V_{dd} across the capacitor from the previous cycle. Thus now the voltage at node b_2 is $2V_{dd}$. The node b_2 is connected to the

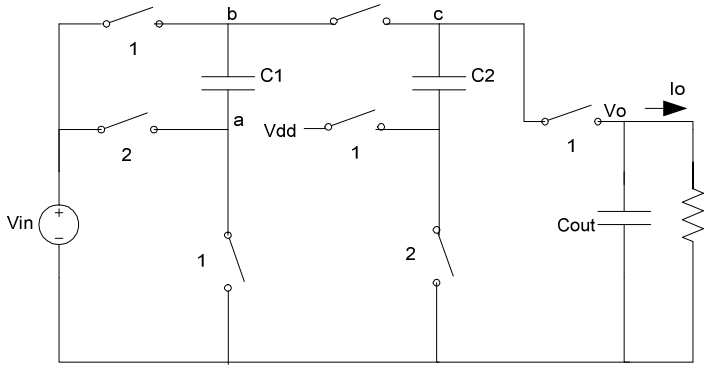
gate of M_5 .Thus the at the source of NMOS M_5 voltage is V_{dd} whereas the voltage at the gate of M_5 is $2V_{dd}$.Then at the output of M_5 is V_{dd} which is connected to node b_1. The capacitor C_1 is connected between node b_1 and a_1. The node a_1 is then connected to ground through MOSFET M_1. The capacitor C_1 thus charges to voltage V_{dd} through M_5 and M_1. The node b_1 is then connected to the gate of PMOS, M_8. Thus the voltage at the gate of M_8 is V_{dd} while the voltage across source i.e. node b_2 is $2V_{dd}$. The PMOS M_8 turns on and voltage $2V_{dd}$ is transferred to the output. The voltage across the output is transferred through MOSFETs M_4 and M_8 while MOSFET M_7 is off.

In the next phase the capacitor C_2 is recharged to V_{dd} through MOSFETs M_2 and M_6. Then the voltage at node b_2 is V_{dd} which is connected to gate of MOSFET M_7 and voltage at the source of M_7 is $2V_{dd}$. Thus at the output, voltage $2V_{dd}$ is transferred through M3, M_7 and C_1 while M_8 is switched off. The effective switching frequency for output filter capacitor is 2f where f is the clock frequency.

Thus voltage doubler is build using MOSFETs which act as switches. The cross coupled converter configuration can be also used to construct other SC converter configurations. Figure 3.5 shows two SC converters voltage tripler build using switches and capacitors. The voltage tripler shown has ideal unloaded step up conversion ratio $V_O/V_{DD}=3$



(a)



(b)

Figure 4.7 Switched capacitor voltage tripler

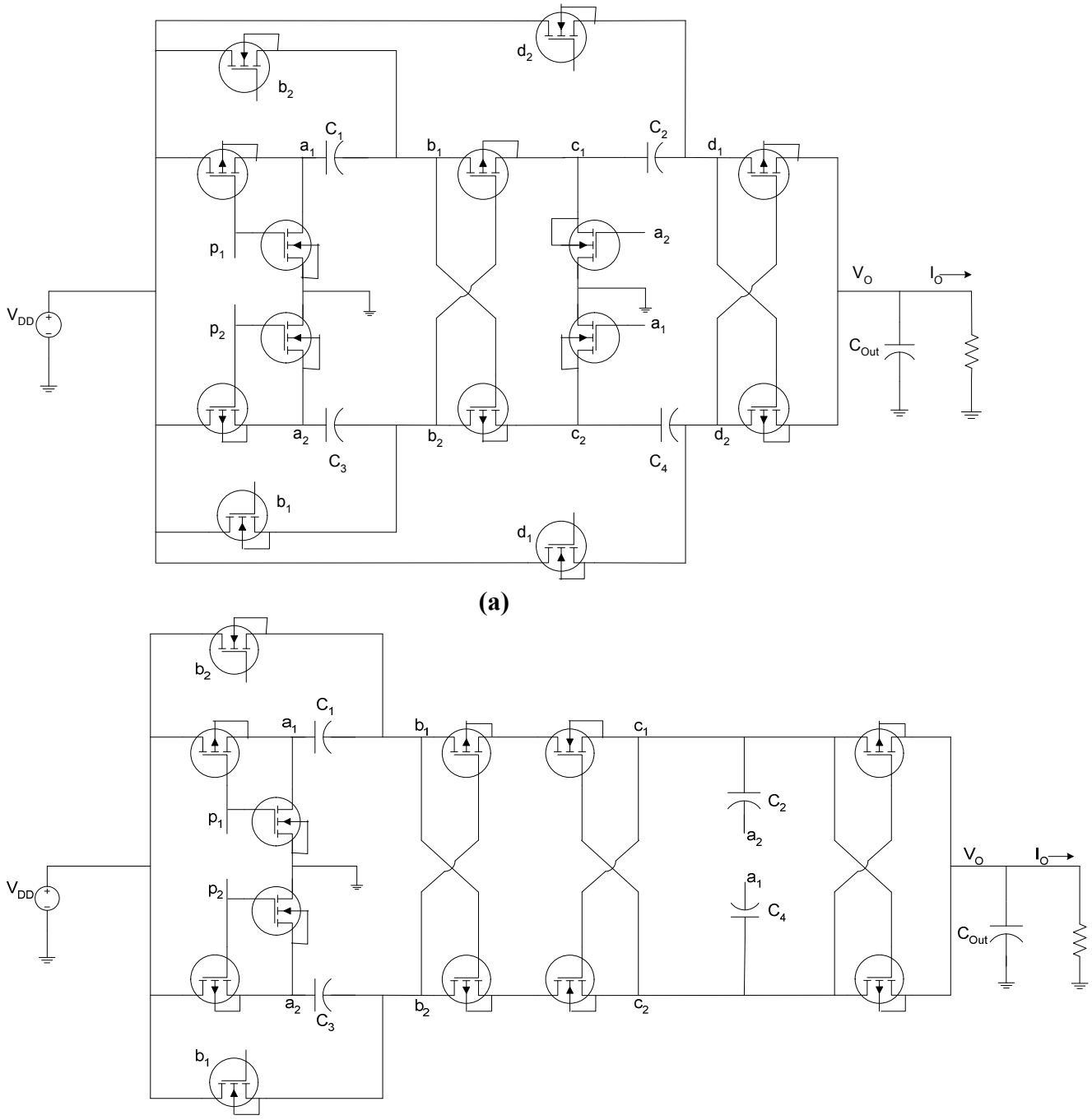


Figure 4.8 Implementation of the converter examples from Figure 4.7 [3]

The two switched capacitor voltage triplers mentioned in Figure 4.7 are implemented in Figure 4.8 taking into consideration the block diagram (Figure 4.3). In on-chip capacitors the bottom plate parasitic capacitor dominates the nodal capacitances. The converter shown in

Figure 4.8b has lower switching losses as the internal voltage swings are smaller as compared to Figure 4.8a.

4.3.2.2 Losses in converter

There are conduction losses due to charging and discharging of capacitors. The power is dissipated in the switch on resistances. The switch capacitor has dc conversion ratio M = V_O/V_{DD}. In the low frequency limit, the output resistance is inversely proportional to the energy transfer capacitance values and the clock frequency [9].

$$R_o(f) = \frac{K}{C_f} \tag{4.1}$$

The output resistance reaches a minimum value R_{omin} which depends on the switch on resistances at switching frequencies. The analytical approximation for R_o (f) for wide range of frequencies is expressed by equation 4.2 [6].

$$R_o(f) = R_{omin}\sqrt{\left(1+\frac{f_c}{f_s}\right)^2} \tag{4.2}$$

Where $f_c = \frac{K}{C \cdot R_{omin}}$, is the corner frequency.

At fc, the lower frequency and higher frequency have the same value.

The conduction loss P_c can be found as [3];

$$P_c = R_o(f) \cdot I_o^2 \tag{4.3}$$

The total parasitic at various nodes and voltage swing across the capacitances are used to estimate the switching losses in an on chip implementation. The total switching loss is found by summation of switching losses over all nodes in the SC converter as;

$$P_{sw} = \sum_{nodes} P_{nodes} \tag{4.4}$$

Thus the conduction and switching losses are described in equation 4.3 and 4.4. These losses are used to determine the efficiency of the converter. During the designing of the converter care should be taken to keep the losses as minimum as possible, since it directly affects the efficiency of the converter.

4.3.2.3 Designing of voltage doubler

In section 4.3.2.1 the general circuit of voltage doubler is shown. As in the previous section we see there are conduction and switching losses in the converter. To reduce the losses in the converter (as we cannot completely eliminate the losses) modifications are done to the existing circuit. Figure 4.9 gives modified circuit diagram of voltage doubler of Figure 4.5

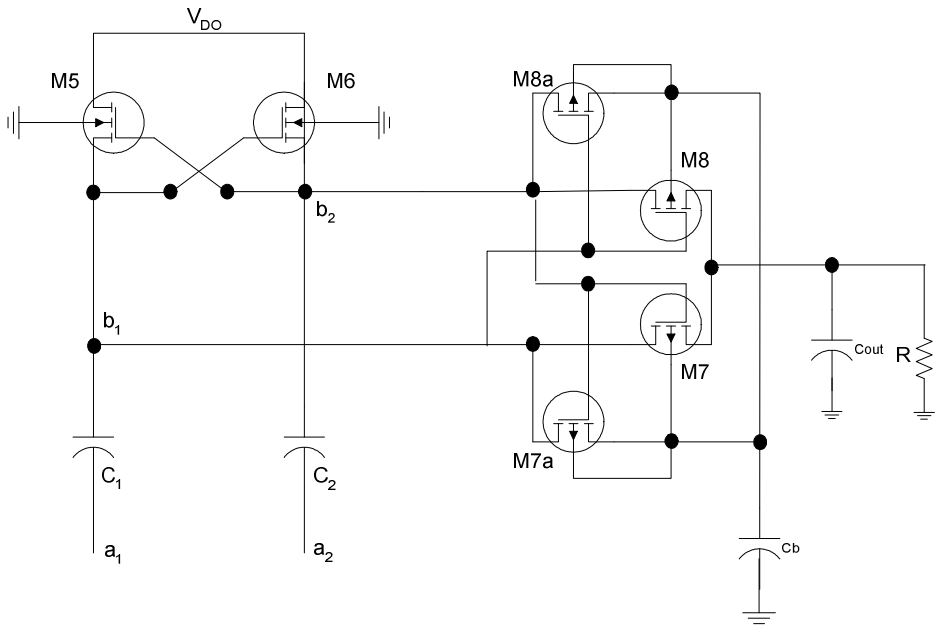


Figure 4.9 Detailed circuit diagram of the voltage doubler of Figure 4.6 [3]

In the above circuit $M_{7a,}$ M_{8a} and capacitor C_b are additionally added with reference to the Fig 3.4 which are used to bias the nwell of PMOS devices at voltage The circuit consists of NMOS devices as well as PMOS devices. PMOS devices are constructed in a common n-well biased at voltage V_B. NMOS device share common substrate which is connected to the ground. There are two opposite phase clock phase signals p1 and p2 used to drive the CMOS inverters $M_{1,}$ M_2, $M_{3,}$ M_4 which produce the drive signals at node a_1 and a_2. Drive transistors $M_{1,}$ M_2, $M_{3,}$ M4 are not shown. The signals at node a_1 and a_2 are non-overlapping opposite phase signals, which are zero at a short interval times. M_5, $M_{6,}$ M_7, M_8 all devices have cross coupled gates. NMOS devices M_5 and M_6 can never turn on at the same time due to non-overlapping signals. The energy transfer capacitors C_1, C_2 are charged through M_5, M_6 to V_{DD} in opposite phase of clock signals. The series PMOS switches M_7, M_8 pass $2V_{DD}$ to the output filter capacitance C_{out}. To avoid forward bias of PMOS devices V_B must be always greater than or equal to V_{out}. PMOS devices are always reversing biased because forward bias of these junctions may cause lossy discharge of the output or latch up condition through the p substrate of the chip.

The drawback of this circuit is that during intervals when nodes a_1 and a_2 are close to ground, both b_1 and b_2 are close to V_{DD} causing both PMOS switches M_7, M_8 to turn on at the same time. This leads to lossy discharge of the output filter capacitor $C_{out.}$ To avoid this from happening, the time intervals are reduced when a_1 and a_2 are simultaneously low or are overlapping signals. Now due to his NMOS devices M_5 and M_6 are turned on at the same time which would result again in lossy discharge of C_1, C_2 to V_{DD}. The exact timing of the driving signals a_1, a_2 is important at high frequencies as the losses incurred due to the undesirable conduction of the cross coupled device causes increase in the switching losses in

the converter.

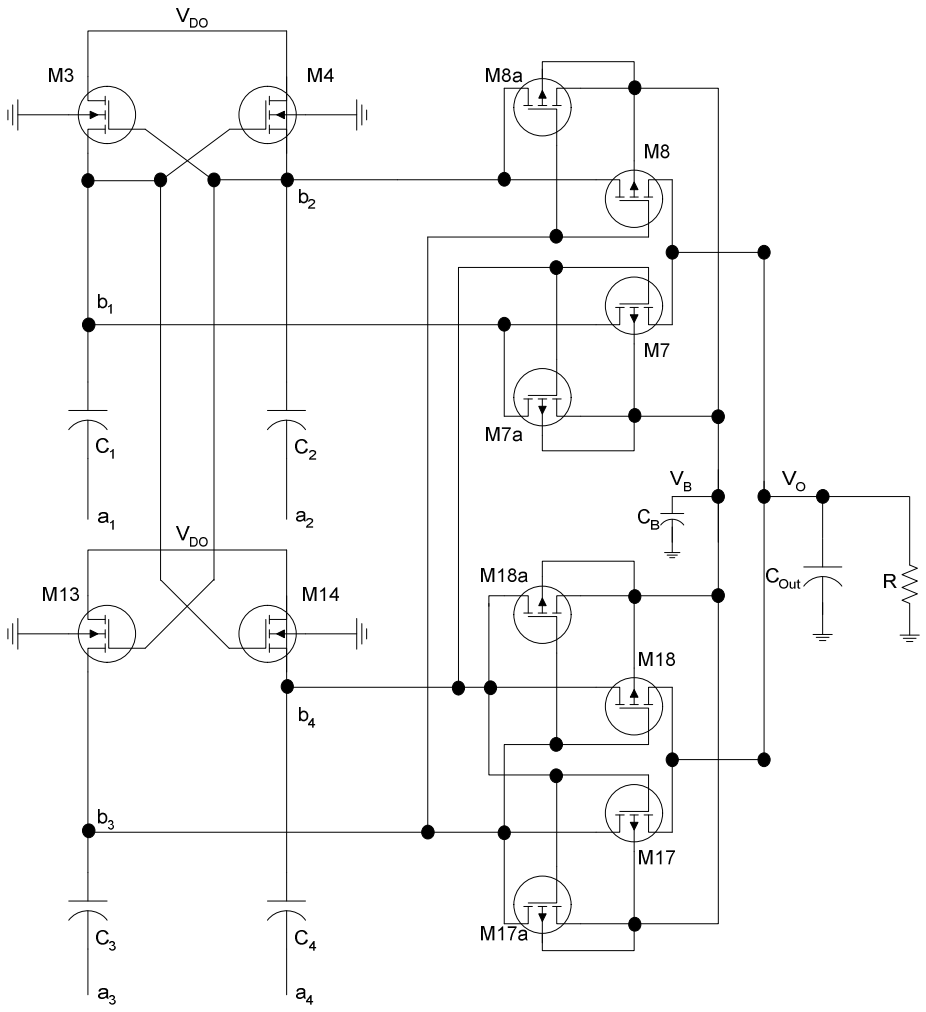


Figure 4.10 Modified circuit diagram of the voltage doubler of Figure 4.9 [6]

Thus to remove the problem occurring in the previous circuit another cross coupled pumps is added which is driven by the overlapping drive signals at nodes a_3 and a_4. The two pumps are coupled such that PMOS devices in both pumps are driven by overlapping signals and NMOS devices in both pumps are driven by non-overlapping signals.

The Figure 4.10 is implemented as voltage doubler in UMC90, the values of the capacitor are C_1= C_2 =C_3= C_4= 229.5fF and the output capacitor C_B =306fF. The sizes of the MOSFETs depend on the current required at the output terminal. The width and length of NMOS and PMOS are kept same i.e. W=10u and L=90n for all the MOSFETs in the circuit.

In order to avoid parasitic discharge of the output filter capacitor C_{out}, it is important that the

transitions of a_1 and a_3 as well as a_2 and a_4 occur at the same time and these transitions have short rise and fall times.

4.4 Designing of random generator

In this section designing of load model for dc converters is presented. A random generator is designed as load model for the converter to see the behavior of dc converters for switching circuits. The random generator is designed with low power consumption. The random generator has power consumption of 7.092uW.

Random generator is a circuit which generates a sequence of random numbers. The random generator is build using a Linear Feedback Shift Register (LFSR). An LFSR is a shift register whose input bit is linear function of its previous state. In this design an 8 bit LFSR is designed. The architecture used in this design is fibonacci which includes D-flip flops and XORs. The topology fibonacci was chosen as it's more structural as galois topology. In 8-bit fibonacci LFSR tap positions are on position 8, 6, 5, 4. The LFSR is designed in UMC090 technology with minimum power consumption.

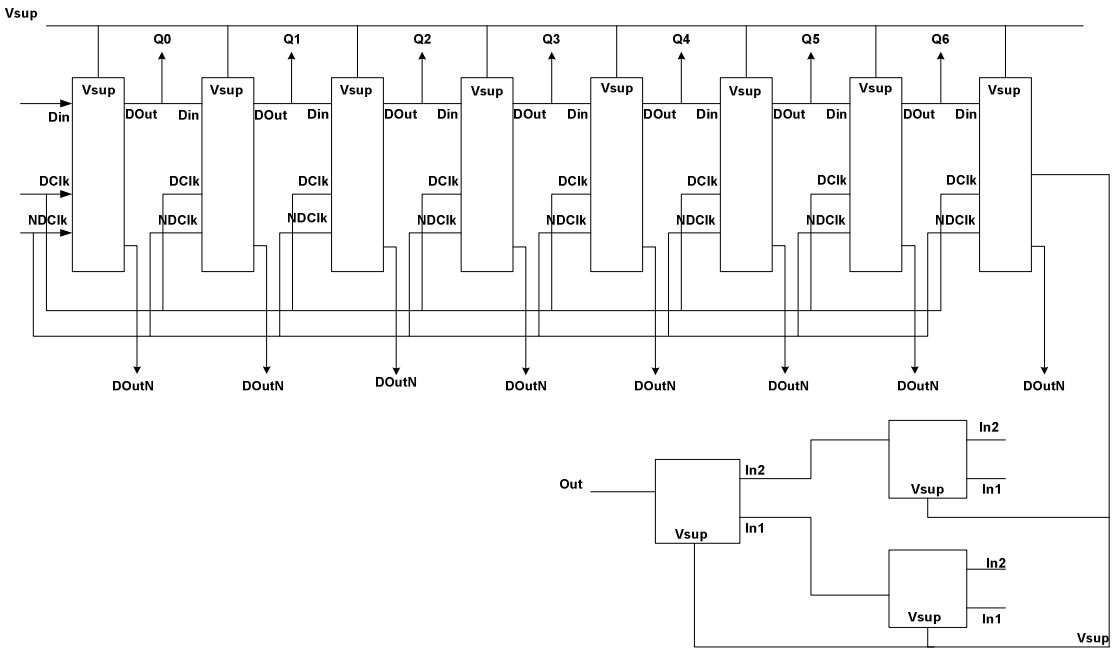


Figure 4.11 Block diagram of random generator

Figure 4.11 gives block diagram of random generator which consists of D flip-flops and XOR gates. For designing LFSR, we first begin with designing XOR and inverter gates. Then with the gates we start building the D-flip flops. Then after designing the D-flip flops the LSFR circuit is designed. While designing the LFSR at each step different structures can be used. The difference between them is the number of transistor, speed, driving strength and size of the transistor for the same functionality. In this design, structures are implemented

with minimum size and minimum number of transistors. For reducing the power consumption in the design, the number of transistors and the size of transistors are kept as small as possible. In the next section design of XOR gate is shown

4.4.1 Implementation of X0R gate

The XOR means exclusive OR gate. The description of XOR gate is given as one of the input should be high (1) for the output to be high (1).The truth table of XOR gate is shown in Table 4.1.

Table 4.1 Truth table of XOR gate

INPUT A	INPUT B	OUTPUT (A XOR B)
0	0	0
0	1	1
1	0	1
1	1	0

Figure 4.12 and 4.13 shows the block diagram and schematic of XOR gate respectively.

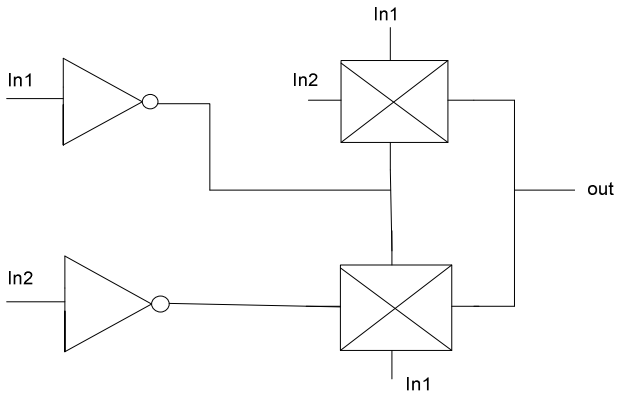


Figure 4.12 Block diagram of XOR gate

Figure 4.13 shows the schematic of XOR gate shows the circuit for inverter and transmission gate. The most common way of implementing XOR is using inverters and OR gates. But in Figure 4.13, XOR gate is implemented using inverters and transmission gates. The transmission gate is an electronic relay which switches on depending on the input at the gate. The transmission gate is made of PMOS and NMOS devices. The gates and drains of PMOS and NMOS are connected to each other. The transmission gates are used instead of OR gates to save the power consumption and avoid glitches.

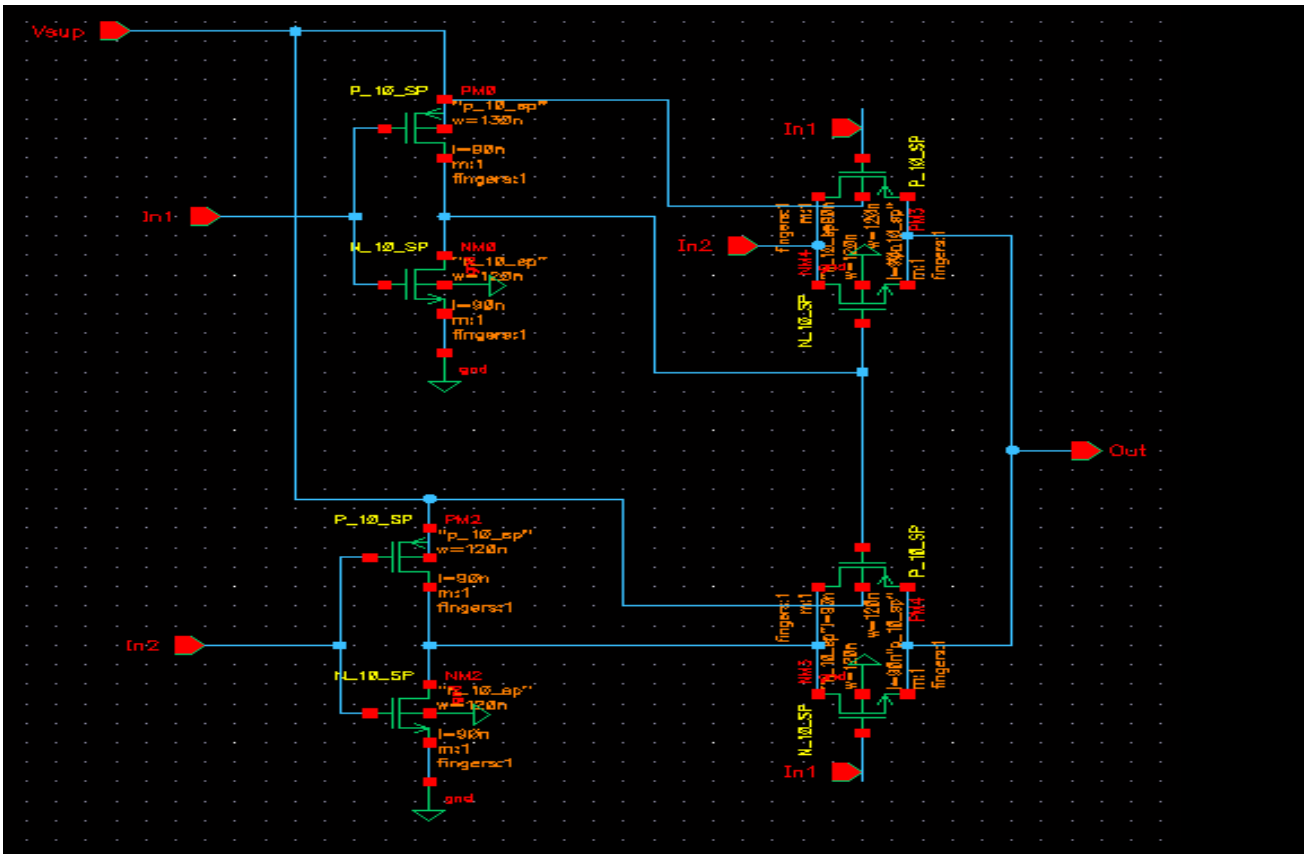


Figure 4.13 Schematic of XOR gate

4.4.2 Implementation of D Flip flop

The D flip-flop is circuit in which the input appears at the output delayed by one clock cycle. The D Flip-flop is implemented using two transmission gates and two inverters. The transmission gates work alternately i.e. when one is on, the other is off. Figure 4.14 shows block diagram of D flip flop.

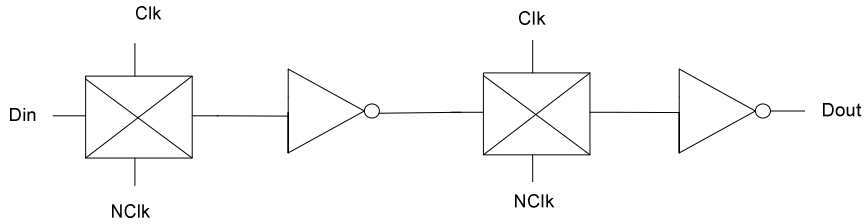


Figure 4.14 Block diagram of D-flip flop

The input Din is connected to the transmission gate. In the first transmission gate, the gate of PMOS is connected to DClk and gate of NMOS is connected to NDClk (NDClk is opposite of DClk) and is exactly opposite case for second transmission gate. When Din is 0, DClk=0, and NDClk =1, the transmission conducts, delivering Din voltage to the inverter. At the output of inverter is **Din.** The second transmission gate does not conduct, thus the value is

stored and transferred to the output during the next cycle. The D in D-flip flop stands for data; as the flip-flop is used to store the value that is on the data line.

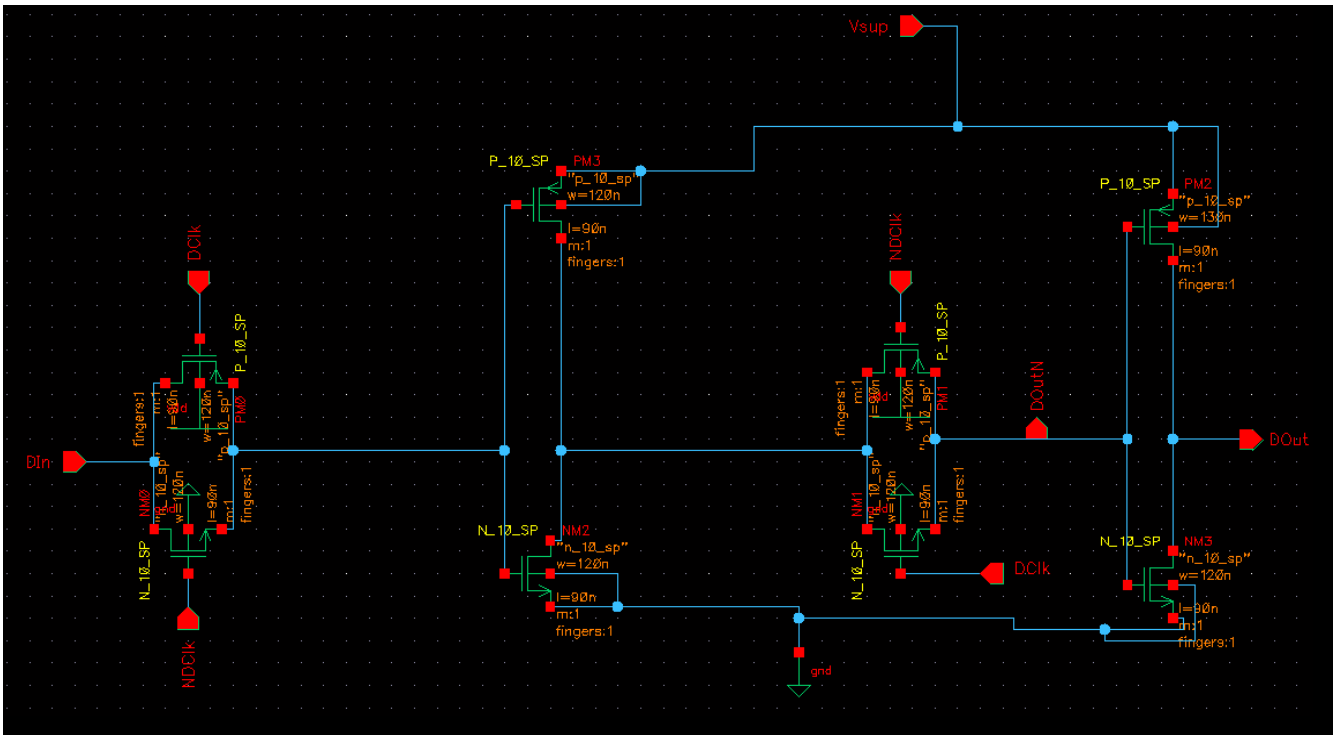


Figure 4.15 Schematic of D flip-flop

Figure 4.15 shows the schematic of D-flipflop. The two different types of flip flops are ordinary and driving flops. Ordinary flip flops are used for intermediate flops while driving flops are used for driving XOR gates. The two types of D flip flops have same the circuit with different values of the transistors.

For driving flip-flop

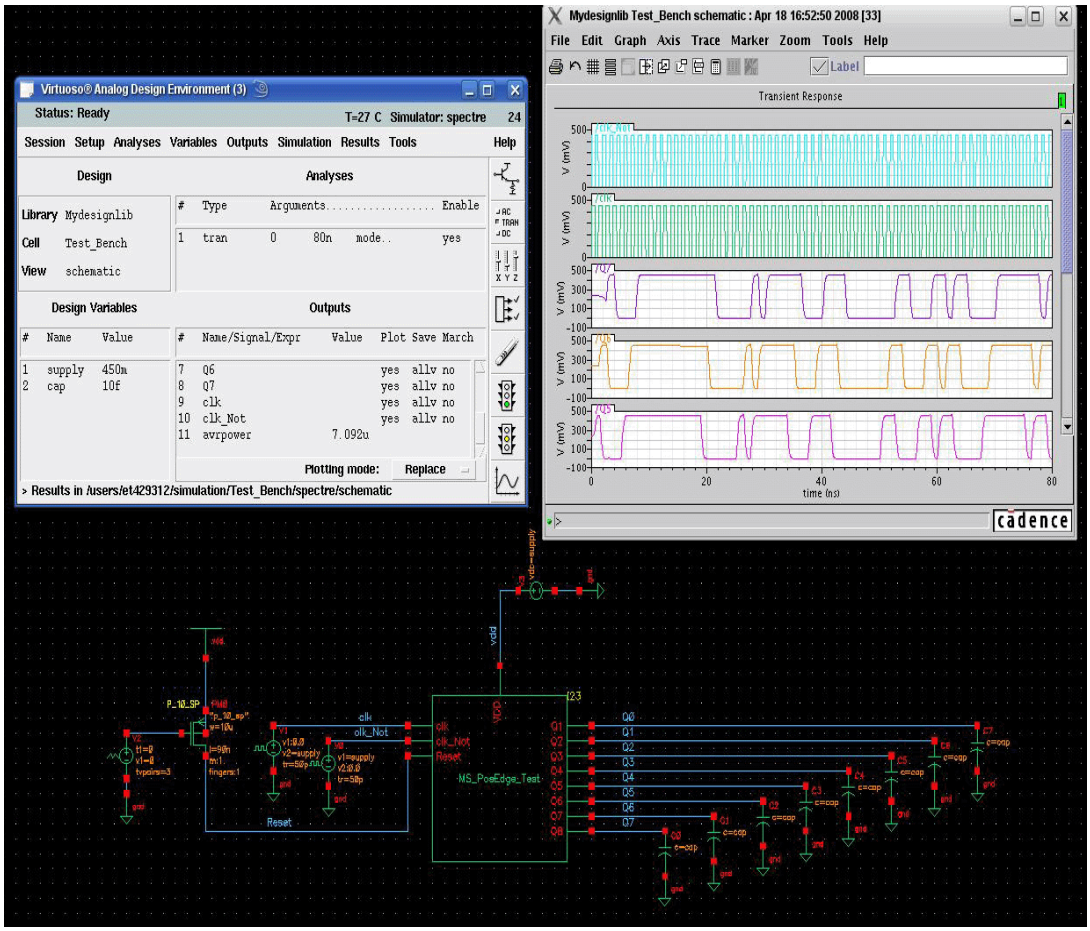
These flips flops have larger transistor in first latch as well as in the second latch
For the first latch the ratio (W/L) is
(W/L) n = 120
(W/L) p = 140

For the second latch the ratio (W/L) is
(W/L) n = 200
(W/L) p = 290
For ordinary flip-flop
These flips flops have smaller transistors in first latch and larger transistors in the second latch. For the first latch the ratio (W/L) is

(W/L) n = 120
(W/L) p = 120

For the second latch the ratio (W/L) is
(W/L) n = 120
(W/L) p = 130

By using different types of flip flops for different places in the structure, area and power is saved. While designing the XOR gates instead of using 8 transistor ordinary gates, another structure is used. To avoid glitches the new structure is used, otherwise it has the same number of transistors as previous one.



. **Figure 4.16** The output waveforms of the random generator

After designing the D-flip flops and XOR gates, the random generator circuit is built. The supply voltage is 450mV and the load capacitor C_L= 10fF. Figure 4.16 shows the power consumption of random generator of 7.09uW.

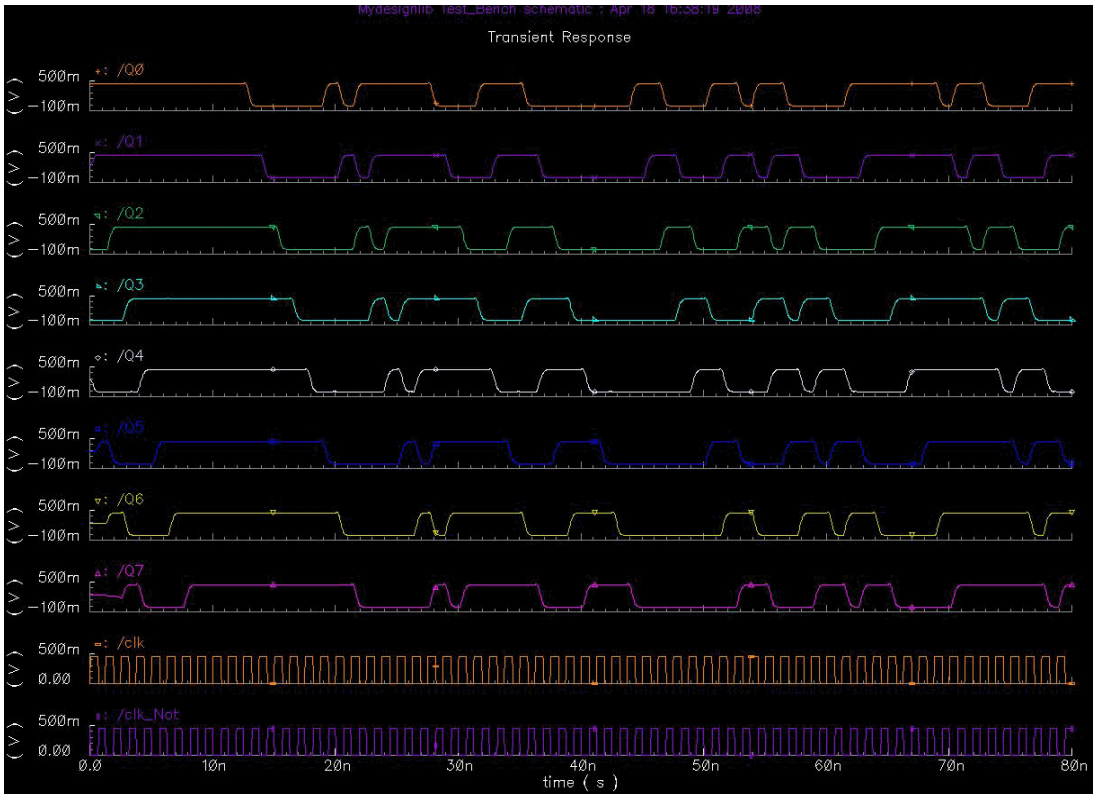


Figure 4.17 Output waveforms of random generator

The outputs of D-flip flops, D_0 to D_7 are Q_0 toQ_7. From the output waveforms it can be clearly seen that the output Q_0 is shifted to the right at Q_1, and then it shifts at Q_2 and so on. At every 255cycles we get the same value and it goes on.

4.5 Summary

The design of switched capacitor up converter is described in this chapter. Also non-overlapping phase clock generator is designed to generate non-overlapping phase clock signals for converter. In the last section Random generator is designed which is used as load model for the converters. The load model is designed to analyze the behavior of dc converters to switching circuits. The up converter doubles the input voltage approximately. The up converter generates output voltage of 1.2V~5.8V for input range 0.6V~3.0V. The converter operates at 10 MHz operating frequency with efficiency of 70%.

5 Designing of DC- DC down converter for System on-Chip

After analyzing the architecture of DC-DC up converter in the previous chapter, this chapter now focuses on designing of down converter for supplying lower voltages to different parts of the chip. There are number of papers available on on-chip down converters. In this chapter an on-chip differential-amplifier based dc-to-dc voltage down converter is proposed which has similar architecture as reference [20]. This architecture is composed of reference voltage generator, a differential based voltage follower and pass device. In this architecture the reference voltage generator operates in moderate inversion. The on chip differential based Voltage Down Converter (VDC) requires a temperature independent current source to provide stable reference voltage. Thus differential amplifier based VDC is designed in UMC090, with input voltage of 2V~5V generates output voltage 1.2V~2.5V and has efficiency of 76%.

The section is organized as:
Section 5.1 presents an overview of the architecture of VDC;
Section 5.2 describes designing of VDC;
Section 5.3 compares the designed architecture with reference VDC.

5.1 Overview of the architecture of VDC

From past few years research has been done on on-chip down converters. There has been a continuous effort to incorporate an on chip dc to dc voltage down converter into high density VLSI. There are number of problems existing such as thermal cooling, power dissipation, and device reliability of short channel MOS transistor. The above problems could be solved by reducing the supply voltage to acceptable limit such that the performance of chip is not degraded. The traditional type of VDC that has been used in power systems is the switching mode circuit [12], [13]. Switching mode VDC has high power efficiency but the main drawback is that it requires an external LC filter. The other option is to integrate L and C components into the chip which results in large layout area and overall accuracy of the converter is also poor. To overcome these drawbacks an on-chip differential based VDCs has been proposed from few years [14]-[17].

While designing an on-chip differential based voltage down converter in digital circuits, parameters like standby current; layout area and stable voltage range are considered as important parameters. The designed down converter should have

1) low standby current so that VDC consumes little power when its on standby
2) a small layout area and
3) A stable reduced internal supply voltage for wide range of operating conditions.

In this section an overview of the architecture of VDC is given below. The architecture of

VDC consists of reference voltage generator, differential amplifier based voltage follower and pass device. In order to get stable reference voltage, a temperature independent current source is required which reduces the temperature dependency but in turn increases the complexity of circuit.

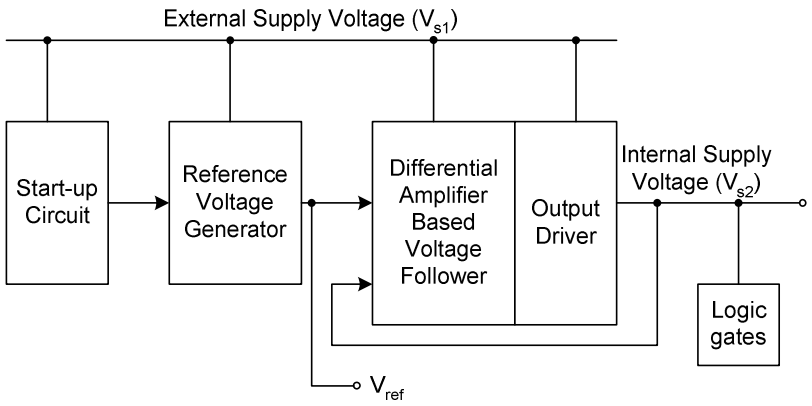


Figure 5.1 Architecture of VDC [20]

Figure 5.1 shows the architecture of VDC, the external supply voltage V_{dd} is simultaneously applied to the reference voltage generator, differential amplifier based voltage follower and pass device. The function of the reference voltage generator is to produce a stable voltage V_{ref} that is free from fluctuations of V_{dd} and temperature. The voltage V_{ref} is then applied to the voltage follower. The voltage follower is made of differential amplifier which acts as gain stage in VDC. The output of voltage follower is applied to the pass device. The pass device is nothing but an NMOS device. The NMOS device is considerably large for high drivability requirement of VDC. The output of the pass device is then connected to the input of differential based voltage follower to form a negative feedback system. In random logic circuits this kind of structure is considered to be suitable in terms of drivability and layout area.

5.2 Circuit description

In the previous section description of the architecture of the on-chip VDC is explained. As seen the input is external supply voltage (Vdd) and output is the internal power supply (Vout). To begin with the implementing of the voltage down converter, the simplified circuit schematic of a VDC is shown in Figure 5.2.

First at the input reference voltage generator is present, which produces two voltages i.e. Vcon and Vref. Vcon closely keeps pace with external supply voltage Vdd and the reference voltage Vref is free from fluctuations of Vdd and temperature. The next stage is a differential amplifier which works as gain as stage in the VDC. In the last stage a NMOS device is used to implement a pass device.

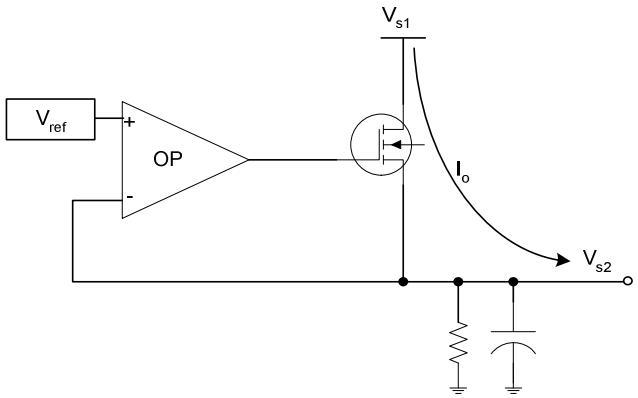


Figure 5.2 Simplified circuit schematic of VDC

5.2.1 Reference voltage generator

The reference voltage generator forms an integral part of on-chip VDC. The constant current source is considered to be an important component in the design of internal reference voltage.

Thus while designing the reference voltage generator some of the points to be considered are

1. it should have low standby current
2. it should be temperature and power-supply-independent

Figure 5.3 shows the circuit of Reference voltage generator. The reference voltage generator consists of NMOS and PMOS devices. NMOS and PMOS with long channel are used in the reference voltage to reduce the channel-length modulation effect. For an MOSFET named M_i, the width and length are described as Wi and L_i whereas I_i is the current flowing through M_i. The PMOS devices M_1, M_2, M_3, M_6, M_7, M_{10}, M_{11} and M_{12} are all long channel MOSFETS. The current flowing through M1, M_2 and M_3 is same with small drain current flowing through it. The MOSFETs M_4 and M_5 operate in saturation. The MOSFETs connected in series have the same current flowing through it. Thus M_4 and M_5 also have the same current flowing through them. The voltage across drain of M_6 i.e. V_{con} is given by equation 5.1 [19]

$$V_{con} = V_{dd} + V_{TP} \qquad (5.1)$$

Where V_{dd} is the external supply voltage and
V_{TP} is the threshold voltage for PMOS device.

When the source to bulk voltage i.e. $V_{SB} = 0$, any variation in the temperature T has also variations in the threshold voltage of the devices. When the supply voltage V_{dd} fluctuates and the temperature T is constant, the voltage V_{con} tires to remain close to $V_{dd.}$ Thus the source-gate voltage of M_8 and M_{13} is equal to $V_{TP.}$

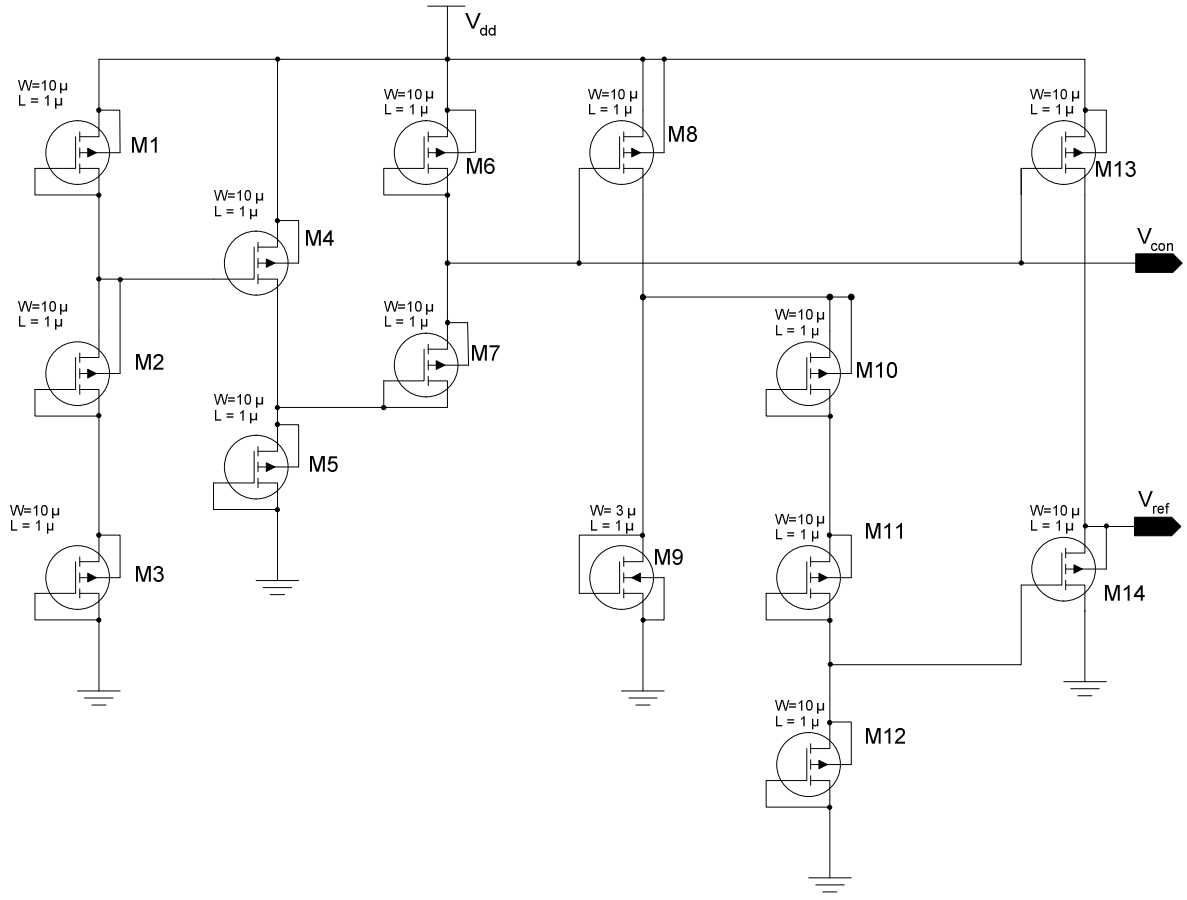


Figure 5.3 Reference Voltage generator [20]

For minimum power consumption, the MOSFETs should be operated in weak inversion however the speed of the device also reduces. Thus to achieve an optimum between the speed and power consumption, the MOSFETS M_8 and M_{13} operate in moderate inversion. The reference voltage generator thus conducts in moderate inversion [26-27]. The drain current flowing through the MOSFETs is given as

$$I_d = 2\mu C_{ox}\left(\frac{W}{L}\right)_n U_t I_n \tag{5.2}$$

The reference voltage is given as

$$V_{ref} = U_t\sqrt{\frac{1.92nW_n}{L_n}}\left(\sqrt{\frac{L_{14}}{W_{14}}} + \frac{1}{3}\sqrt{\frac{\mu_p L_n}{\mu_n W_n}}\right) + \frac{V_{TN}}{3} - V_{TP} \tag{5.3}$$

The complete derivations of the drain current I_d and reference voltage V_{ref} can be found in

reference [20]. After understanding the working of reference voltage generator, overview of voltage follower is given in following section.

5.2.2 Voltage follower

The voltage follower should be designed in such a way that it can supply enough current with low output impedance so that the output voltage is not very much affected by the large loading current fluctuation.

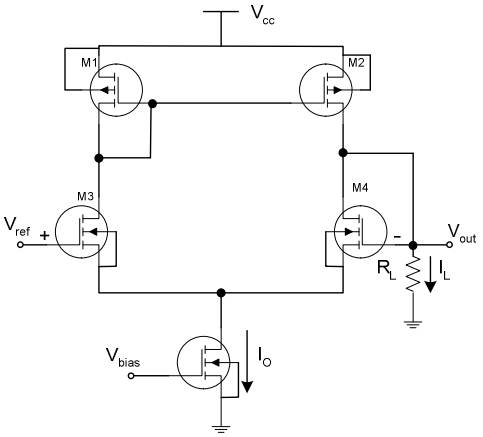


Figure 5.4 Single stage Follower [15]

A single stage voltage follower is show in Figure 5.4. In some literatures a differential input single output CMOS amplifier operated as comparator cascaded by an additional PMOS device works as driver. However this voltage follower with PMOS device has lower loop stability [20].

This voltage follower is implemented for the VDC for memory chip application. This voltage follower has excellent phase margin for wide range of load impedance. For smaller voltage error between the reference voltage and output voltage, the device dimensions of the transistors in the voltage follower have to be made large.

5.3 Comparison of designed down converter with Zhou's converter [20]

In this section the designed down converter (called as converter2 for explanation) is compared with the converter in [20] (converter1). As described before the architecture of the down converter1 consists of reference voltage generator; differential based voltage follower and pass device which is almost similar to converter2. The reference voltage generator for converter2 is same as for the converter1 except for the sizes of the transistor. Thus the MOSFETs M_1~M_{14} are connected in similar way to the reference circuit in the paper.

The MOSFETs M_1, M_2, M_3, M_5, M_6, M_7, M_9, M_{10}, M_{11} and M_{12} are all diode connected MOSFETs. The MOSFETs M_4, M_8 and M_{13} are all voltage controlled current sources, which are used to perform biasing. The diode connected MOSFETs are used as voltage dividers.

The MOSFET M_{14} is a source follower which buffers its gate voltage to its source, providing a low impedance output voltage. The remaining MOSFETs from M_{15} to M_{21} form a two stage voltage-buffer .The MOSFETs M_{15} to M_{19} form the first stage while M_{21} and M_{22} form the second stage of the voltage buffer.

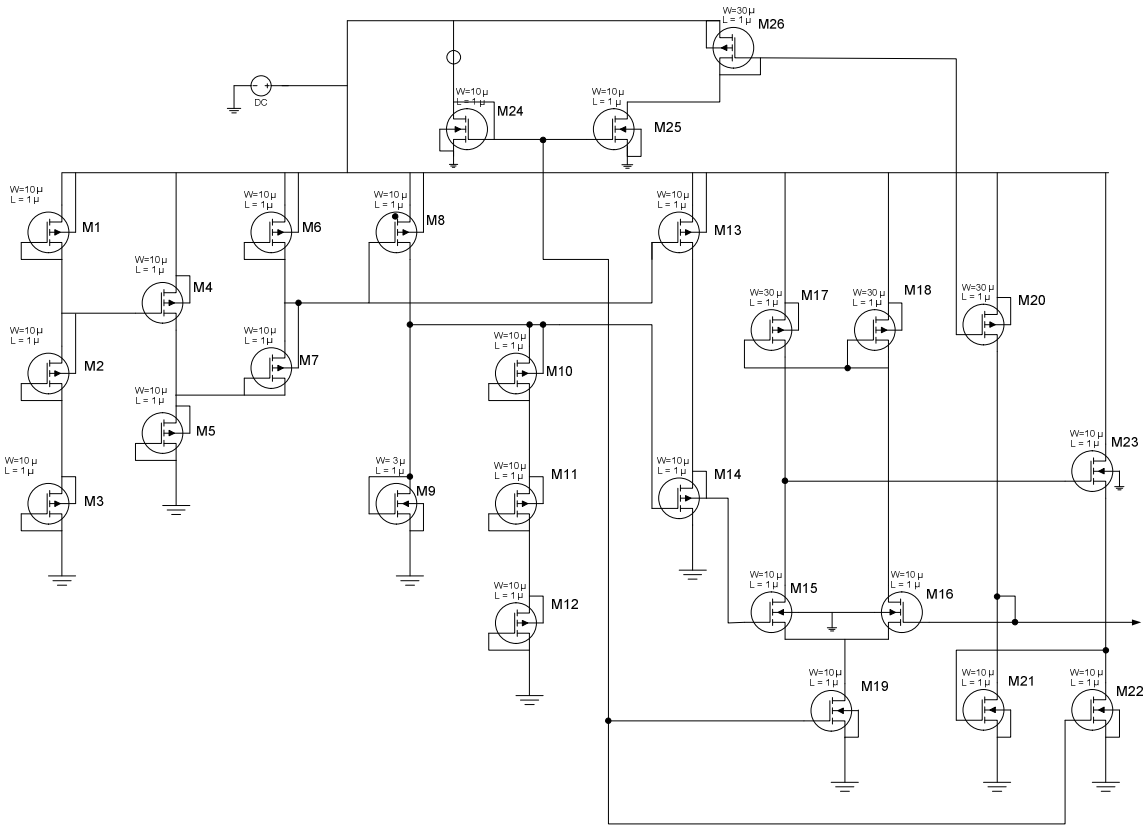


Figure 5.5 Designed differential based voltage down converter

MOSFETs M_{15} and M_{16} form a differential pair, driving the active load M_{17} and M_{18} and provide a forward gain. MOSFET M_{23} is a source follower shifting the DC voltage of the first-stage output down to a lower level in order to bias M_{21}. The second stage is implemented by the common source connected M_{21}. The in-phase output voltage (at the drain of M_{21}) is feed back to the anti-phase input (the gate of M_{16}). The remaining MOSFETs, namely M_{19}, M_{20}, M_{22}, M_{24}, M_{25} and M_{26} are used as biasing sources.

Basically, the first part of the circuit (MOSFETS M_1 to M_{14}) generates a reference voltage. And the second part (the rest) implements a buffer to accurately output this reference voltage, accommodating a large variation of the load. If you want to derive mathematically the reference voltage generated in the first part, redraw the MOSFETs as diodes and Voltage Controlled Current Sources (VCCSs). For example, M_1 to M_3 are 3 diodes in series forming

a voltage divider, so the voltage output at the gate of M_4 is 2/3 Vdd. The similar case applies to M_6 to M_7 and M_{10} to M_{12}. However, in converter2 we don't use M_{10} to M_{12}, the original design does. This means our output voltage at this stage is 3/2 times larger than the original one. At this point the output voltage required should be low. Due to this high voltage at the output, M_{10} to M_{12} are not used in converter2.

In converter2 the circuit is designed in UMC 90nm while in converter1 it is designed in HJTC 0.18um. The designing of the circuit in different topologies results in changing the sizes of the MOSFETs, which eliminates the use of M_{10} to M_{12}.

The MOSFETs M4 and M_8 are implemented as VCCSs while MOSFETs M_5 and M_9 as diodes.

For VCCSs, the drain current is given as

$$I_d = 0.5\mu C_{ox}\left(\frac{W}{L}\right)_n \left(V_{gs} - V_{th}\right)^2 \tag{5.4}$$

For diodes, the ratio of current is

$$\frac{I}{I_s} = \exp\left(\frac{V_{gs}}{a \cdot V_t}\right) \tag{5.5}$$

Where a (alpha or gamma in the literature) is called the slope factor and it has value of ~1.5. Vt is the thermal voltage (26mV in room temperature). So far, given the device characteristics, we should be able to derive the reference voltage at the source of M10 without using the spice. M14 is a source follower; we can derive the Vgs using equation 5.4.

For the explanation of second part, see the figure below. The in-phase, anti-phase input and the output are the gate of M_{15}, M_{16} and the drain of M_{21}, respectively. All the transistors simply form up a 2-stage op-amp.

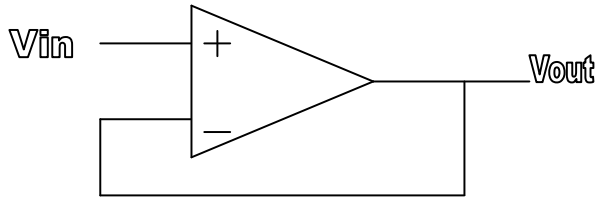


Figure 5.6 Basic voltage follower

The figure 5.6 shows basic voltage follower which is being implemented in down converter. The output of this voltage follower is then feedback to the input as in VDC.

In the down converter2 additional MOSFET M_{23} is placed which acts as the source follower. The DC biasing at the gate of M21 should be conditioned. This implies that the voltage at the drain of M15 might be too high for it. So we down shift the voltage using this source follower.

5.3.1 Sizing of the MOSFETs

MOSFETs have a voltage-current relationship of

$$I_d = 0.5 \cdot m\mu \cdot C_{ox} \cdot \left(\frac{W}{L}\right) \cdot \left(V_{gs} - V_{th}\right)^2 \tag{5.6}$$

Where Id, mu, Cox, W, L, Vgs and V_{th} are the drain current, carrier mobility, oxide capacitance per area, width, length, gate-source voltage and threshold voltage of a transistor.

By increasing the number of electrons or hole increases the materials conductivity. The hole is more tightly coupled to the atoms nucleus; therefore its mobility is lower than the electrons mobility in the conduction band. Thus the mobility of holes is only around one third of the mobility of electrons; we normally increase the width of a PMOS to be 3 times as large as its NMOS counter-part in order for them to have same voltage-current relationships. While designing circuits PMOS devices have larger size than NMOS devices so that both devices have the same drive strength.

5.4 Summary

The design of differential based voltage down converter is explained. The architecture of the designed converter is similar to the Qianneng Zhou's Converter. The down converter is also designed in UMC090. The down converter produces 1.2V~2.5Voutput voltage for input voltage of 2V~5V with load current of 0-0.5mA. In the last section of the chapter comparison is made between the designed converter and Qianneng Zhou's Converter.

6 Simulation results

In the previous chapter the design of differential amplifier based voltage down converter is shown along with the comparison with the reference converter. In this chapter simulations results of Switched capacitor up converter and differential amplifier based voltage down converter is shown. The up and down Converters are designed according to specifications required for the application. The dc converters are used as power supplies so they should provide accurate and very stable output voltages, excellent load regulation, fast transient response and high efficiency.

The chapter is divided as follows;
Section 6.1 presents results and graphs for switched capacitor up converter and
Section 6.2 presents results and graphs for voltage down converter.

6.1 Results for switched capacitor up converter

The specifications of the up converter are given in Table 6.1

Table 6.1 Specifications of SC DC-DC up converter

Parameters	**Value**
Operating input voltage	0.6V-3V
Output voltage	1.2V- 5.8V
Output current	0 mA-1mA
Frequency	10MHz
Operating temperature range	26°C
Efficiency	~70%
Layout area	110x135µm^2

Figure 6.1 presents the input signals given to up converter. The input signal V_{IN} and two opposite phase clock signals are given to clock generator. The clock generator produces 4 drives signals for the converter. As seen from the figure 6.1, a_1, a_2 are non-overlapping while a_3, a_4 overlapping phase clock signals.

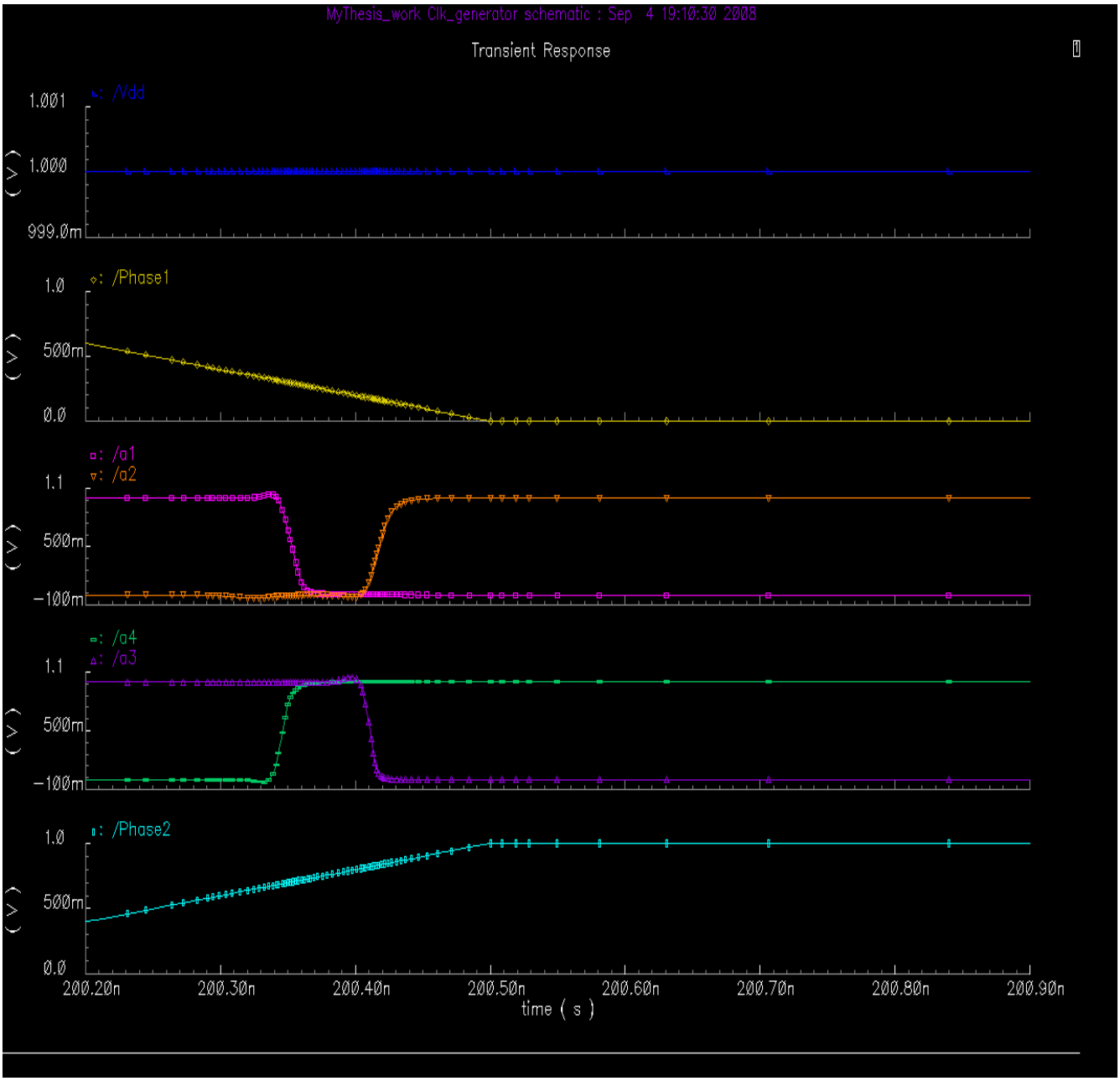


Figure 6.1 Input signals to the switched capacitor up converter

Figure 6.2 shows the output waveforms of the converter. The up converter generates an output voltage 1.2V for input voltage of 0.6V. The graph shows that the switched capacitor converter works like a voltage doubler.

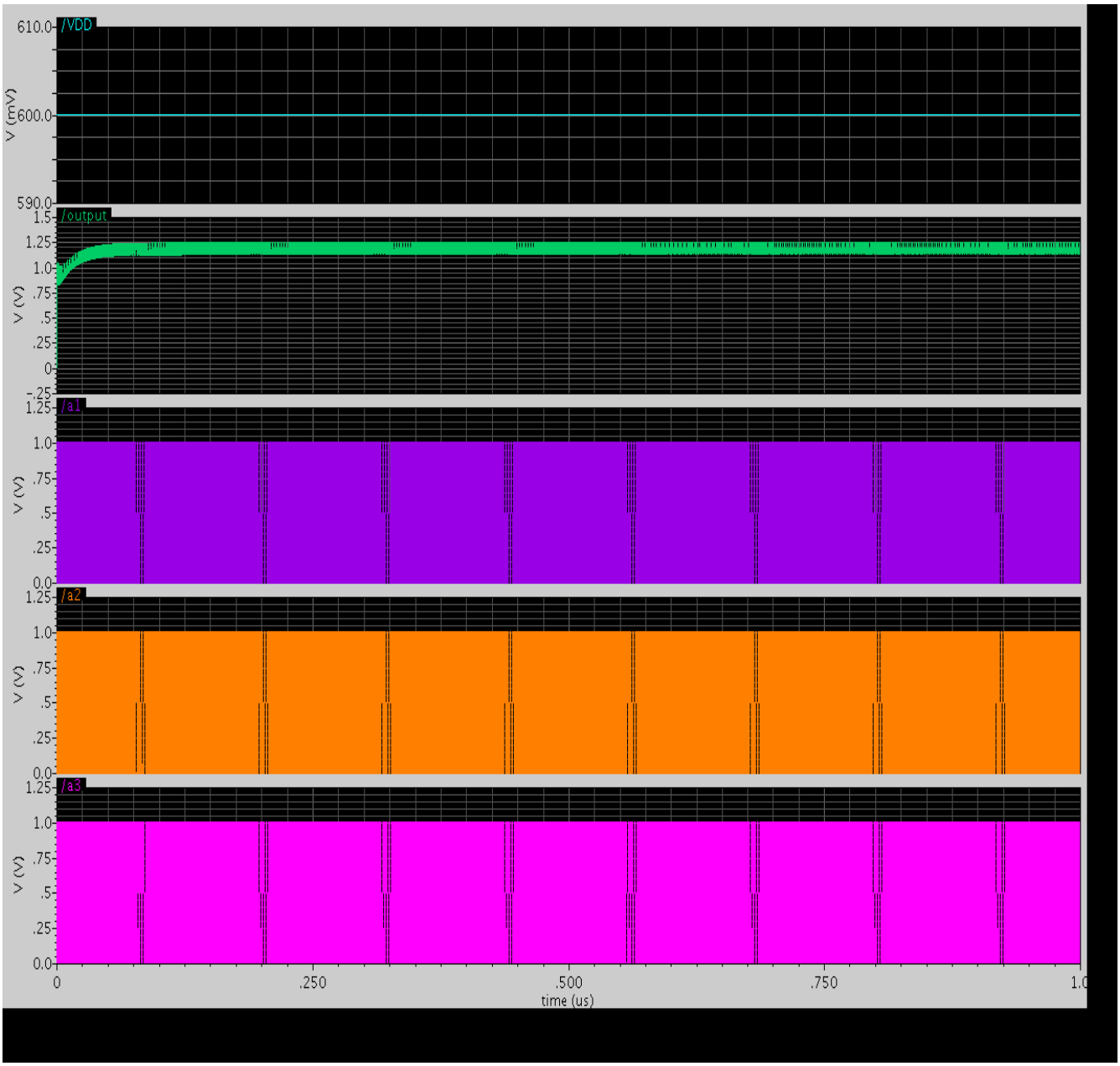


Figure 6.2 Output waveform of switched capacitor up converter

From graph of 6.3 we can see the variation in output voltage as the temperature changes. The temperature is varied from -55° to125°. The output voltage variation is maximum at -55° C (red graph), the output variation reduces at temperature 10° and 35° (blue and purple respectively). As the temperature increase to 80°C (green), the output variation increases little and further increase as temperature is increased to 125° C (orange graph).

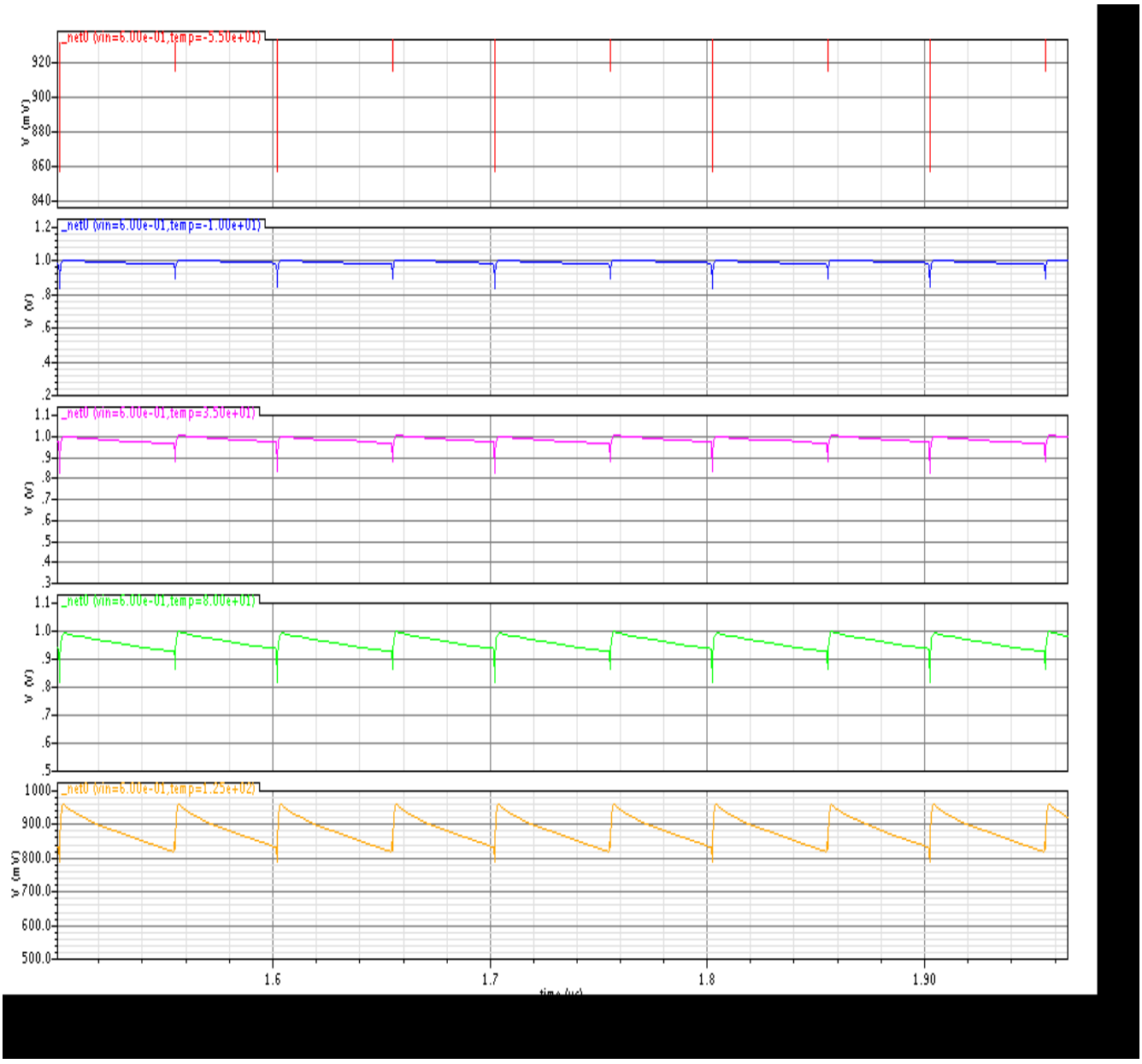


Figure 6.3 Output voltage of up converter as function of temperature

In Figure 6.4 the output waveforms of the SC up converter are shown for period of 10µs.

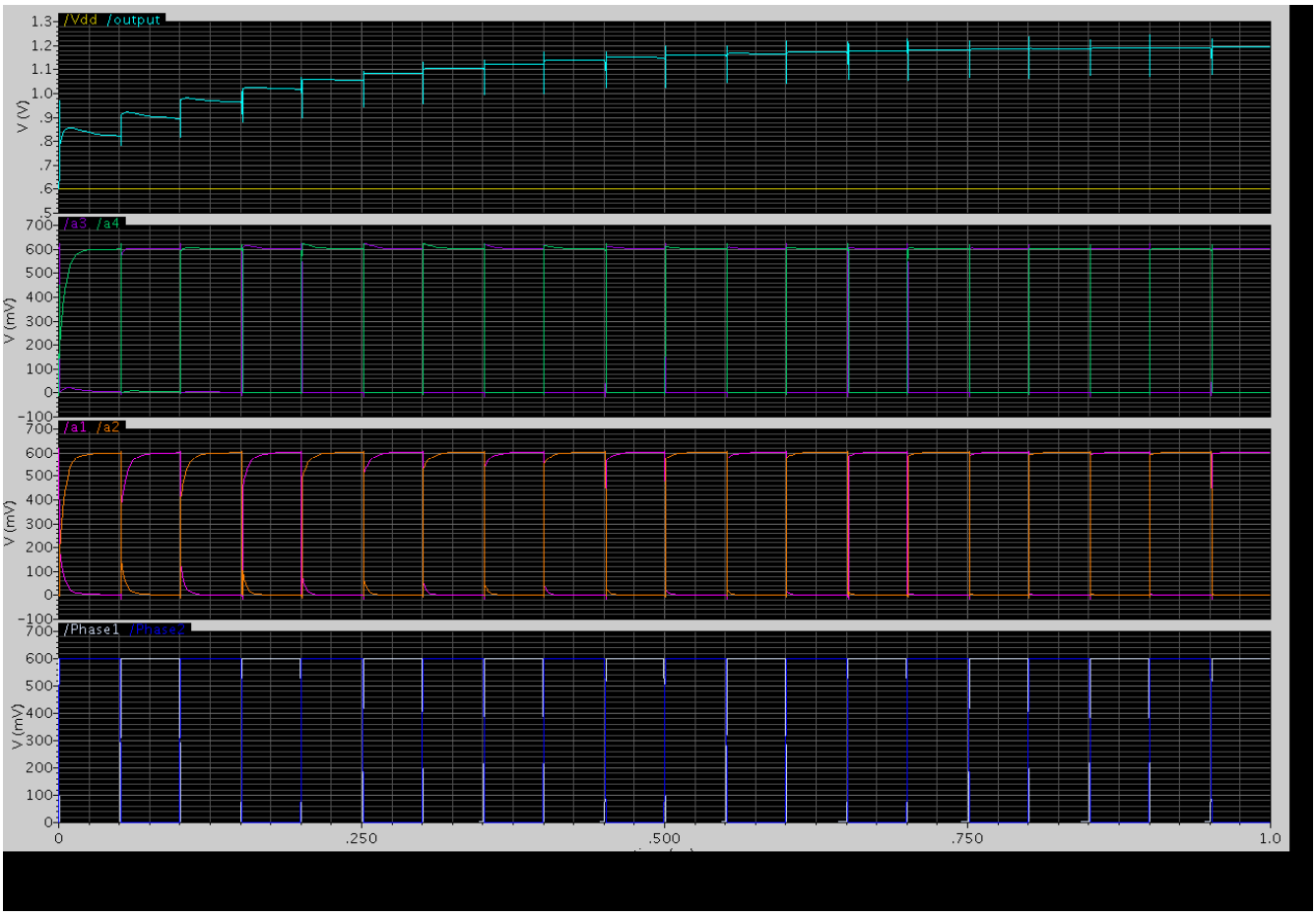


Figure 6.4 Output waveforms of the up converter

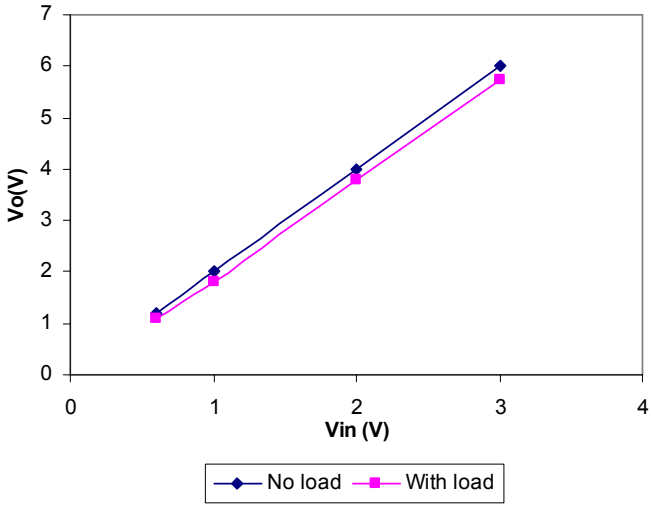


Figure 6.5 Output voltage variation with the no load and with load connected.

Figure 6.5 shows the output voltage of SC dc converter for no load (blue graph) and for

variation in output voltage when load of R=10k is connected (pink graph). From the graph it is clear that output voltage variation is less with output when no load.

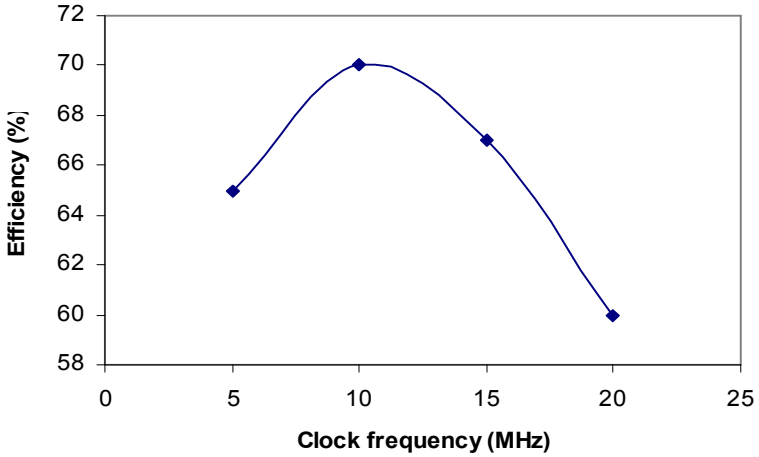


Figure 6.6 Efficiency v/s clock frequency (MHz)

From Figure 6.6 we can see that as clock frequency is increased the efficiency of the converter decrease. The converter provides maximum efficiency of 70% at 10MHz clock frequency.

6.2 Results for differential based voltage down converter

The specifications of the Differential based voltage down converter are given in Table 6.2.

Table 6.2 Specifications of differential based VDC

Parameters	Value
Operating Input voltage	2V-5V
Output voltage	1.2V- 2.5V
Output current	0 mA-0.5mA
Operating temperature range	0-80°C
Efficiency	~76%
Layout area	85 x 45μm^2

Figure 6.7 shows schematic of down converter with node voltages. In the schematic an input voltage of 3.3V is given and at the output node 1.799V is observed.

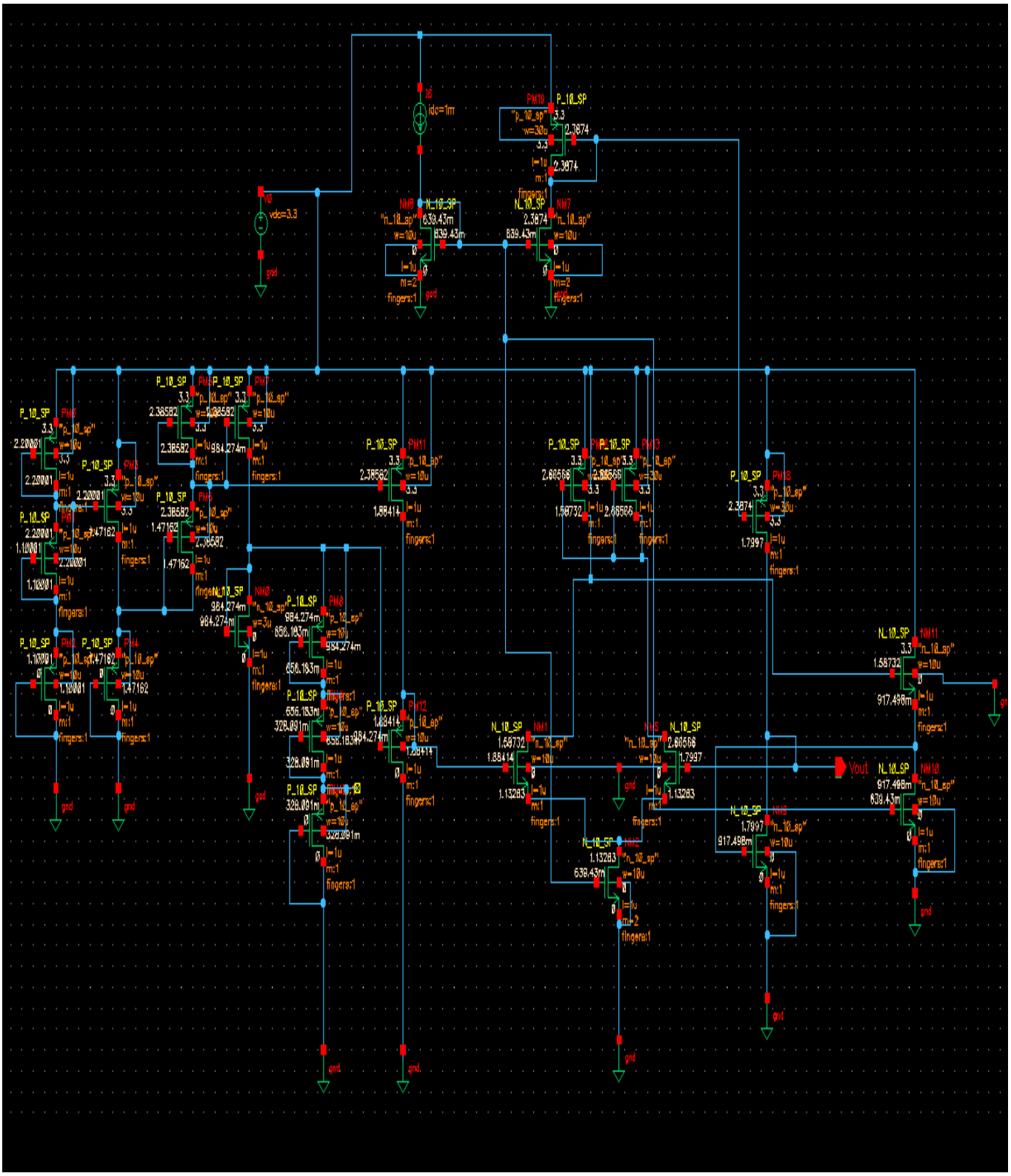


Figure 6.7 Schematic of down converter with node voltages displayed.

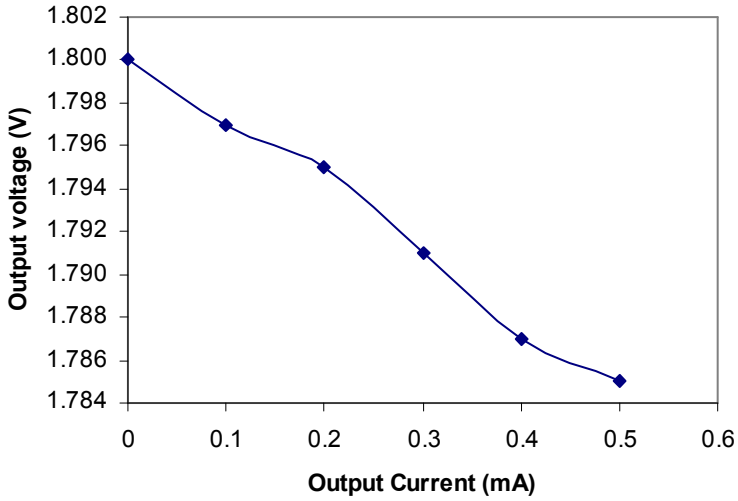


Figure 6.8 Output Voltage v/s Output Current (mA)

Figure 6.8 shows the variation in output voltage with output current. The converter should provide constant supply voltage with varying load current. The graph shows that the output voltage variation is very small (almost negligible) with varying load current.

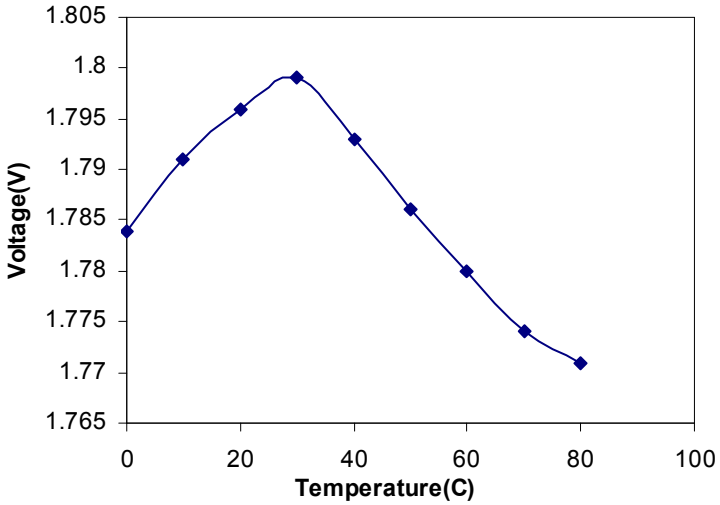


Figure 6.9 Output Voltage v/s Temperature(C)

In graph 6.9 the output voltage with varying temperature is shown. The output voltage is maximum between 30°C to 40°C.

6.3 Summary

In this chapter the simulations results of up and down converter are given. The SC DC-DC up converter operates with an input range of 0.6V~3V and generates output of 1.2V~5.8V

with 70% efficiency and low settling time. The change in output voltage of the converter with load is quite less. The differential based voltage down converter operates for input voltage range of 2V~5V and produces output voltage of 1.2V~2.5V. The down converter has 76% efficiency and output is temperature independent.

7 Layout of circuits

In the previous chapter the simulations results of up and down converters are discussed. After meting the specifications of up and down converters, layout of these converters are designed in UMC090 technology. In this chapter the steps followed while making layout are discussed.

While designing layouts some of the parameters to be considered are, the number of metal layers used for making the layout design. The increase in the number of metal layers increases the complexity of the fabrication process. While making layouts care should be taken to keep the circuit area as low as possible. As the designed circuit area reduces, the number of yields for the same die size increases. Yield is the number of good die/ total number of dies on the wafer. Also increasing the number of die on wafer decreases the cost per die.

In this chapter,
Section 7.1 gives an overview of layout process
Section 7.2 presents the designed layout of up and down converters.

7.1 Overview of layout process

To make layout of the circuit, number of layers are required. Firstly we begin with the fabrication of the well. The well is the first layer fabricated while making a CMOS IC. The substrate or well is sometimes refereed as to as the bulk or body of the MOSFET. The CMOS circuits are fabricated on a silicon wafer. The most common substrate used in IC processing is the P type wafer. The wafer is doped with acceptor atoms such as boron for a p type wafer and donor atoms such as Phosphorous for an n type wafer. While designing CMOS integrated circuits with a p type wafer, n channel MOSFETs (NMOS) are fabricated directly in the p type wafer, while p-channel transistors, PMOS are fabricated in an n well. A process that uses a p type substrate with n well is called n well process and the p well process uses n type substrate with p well. Some of the processes use a p well or both n well and p well and are called as twin well processes.

After fabricating the well, we move to the next layer, i.e. metal layer. The metal layers in a CMOS integrated circuit connect circuit elements like MOSFETs, capacitors and resistors. In UMC 90nm technology the devices being used while designing the circuit provides 9 layers of Metal. In the design of switched capacitor up converter 3 metal layers are used while for the design of voltage converter 2 metal layers are used. The metal in a CMOS process is either aluminum or copper. The unnecessary increase in the number of metal layer increases the complexity of the fabrication process.

7.1.1 Layout using metal layers

In this section short description of connecting the devices through metal layers is described. As mentioned before the metal layers connect the resistors, capacitors and MOSFETs in a CMOS integrated circuit. Metal1 is a layer of metal found directly below metal2 and metal2 is layer found below metal3 and it goes on. The contact M1_M2 is used to connect the metal1 and metal2. When a third layer of metal is used, M2_M3 contact is used to connect metal2 and metal3, M3_M4 would connect metal3 to metal4, etc.

7.1.2 Active and poly Layers

The active, n-select, p-select and poly layers are used to form n-channel and p-channel MOSFETs (i.e. NMOS and PMOS respectively) and so that metal1 can make an ohmic contact to the substrate or well. The active and select layers are always used together. The active defines an opening in the oxide and the select then dopes the semiconductor in the opening either n-type or p-type.

The polysilicon (poly) layer forms the gate of the MOSFET. Polycrystalline is made up of crystalline regions of silicon. Poly is not amorphous silicon i.e. randomly organized atoms and it is not crystalline silicon i.e. an orderly arrangement of atoms in the material such as the wafer.

The contact M1_Poly is used to connect metal1 to either active (n+/p+) or poly. The metal is preferably not connected directly to the substrate or the well as a rectifying contact (Schottky diode) is formed.

7.2 Designed layout

Figure 7.1 and 7.2 shows the layout of SC DC-DC up converter. The size of the layout is 110 x 135μm^2.

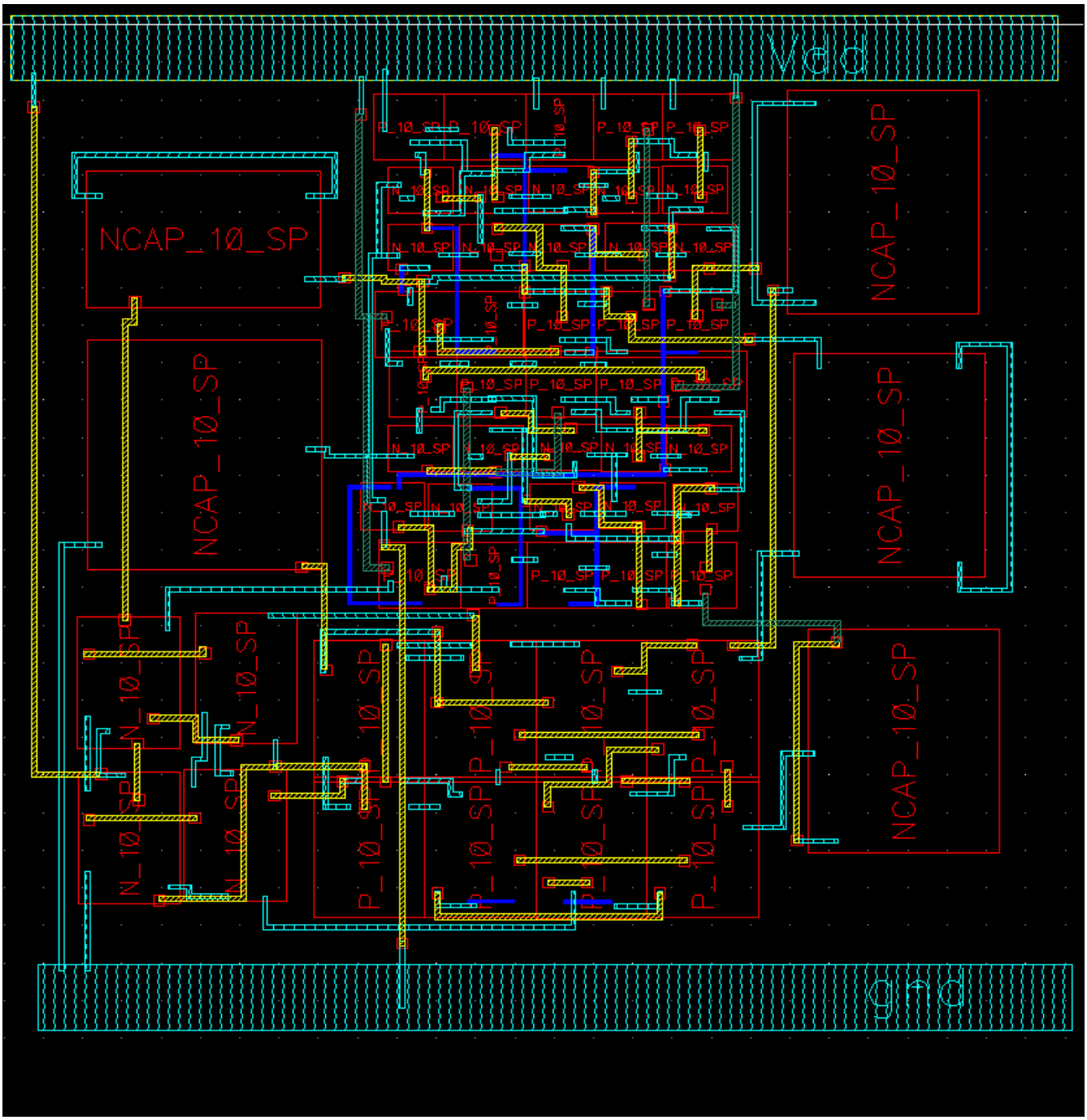


Figure 7.1 Layout of switched capacitor up converter

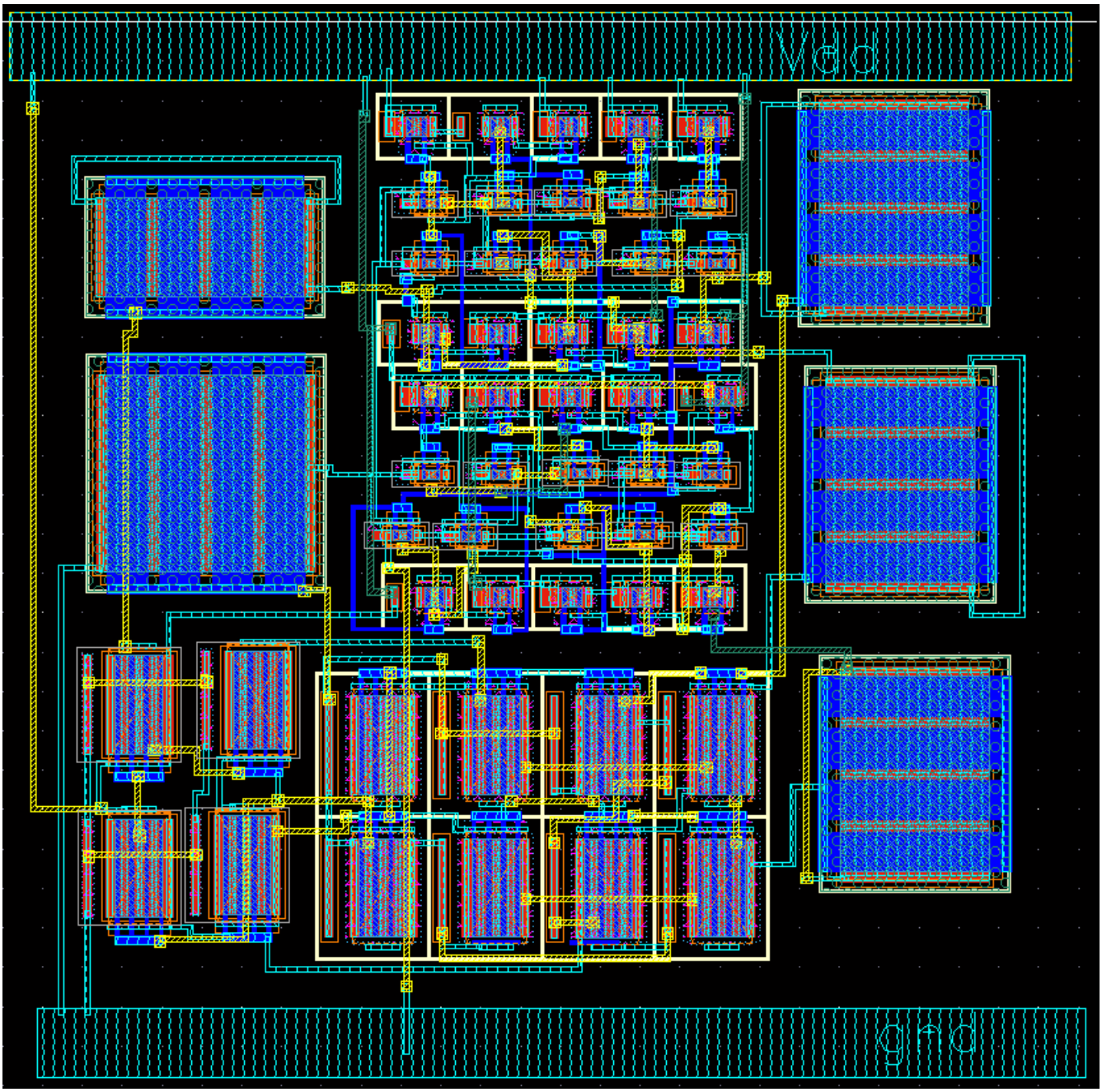


Figure 7.2 Layout of switched capacitor up converter with layers of the components

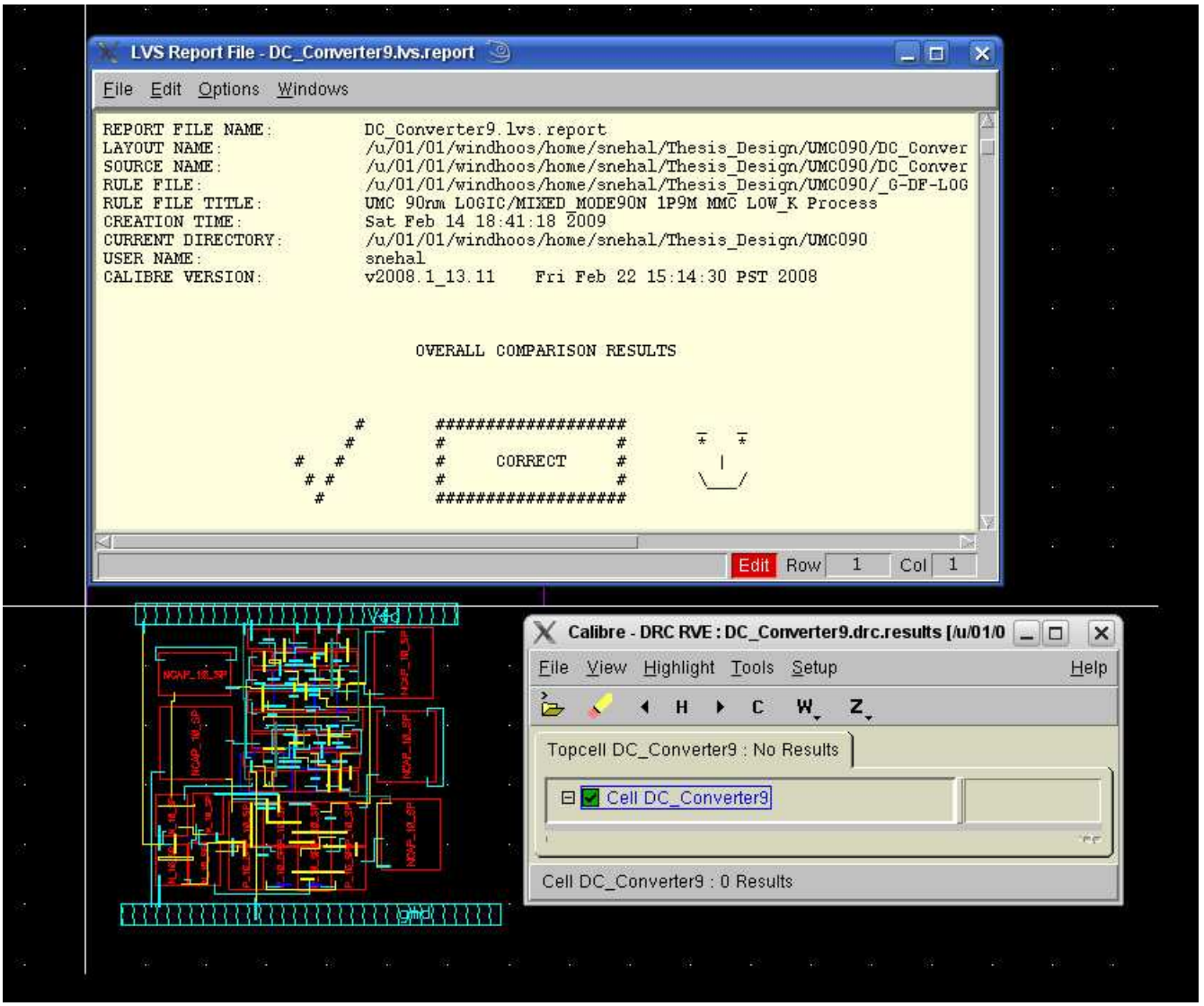


Figure 7.3 Layout of switched capacitor up converter with LVS and DRC

Figure 7.3 shows the layout of down converter with Layout v/s Schematic (LVS) and Design Rule Check (DRC) performed on the converters.

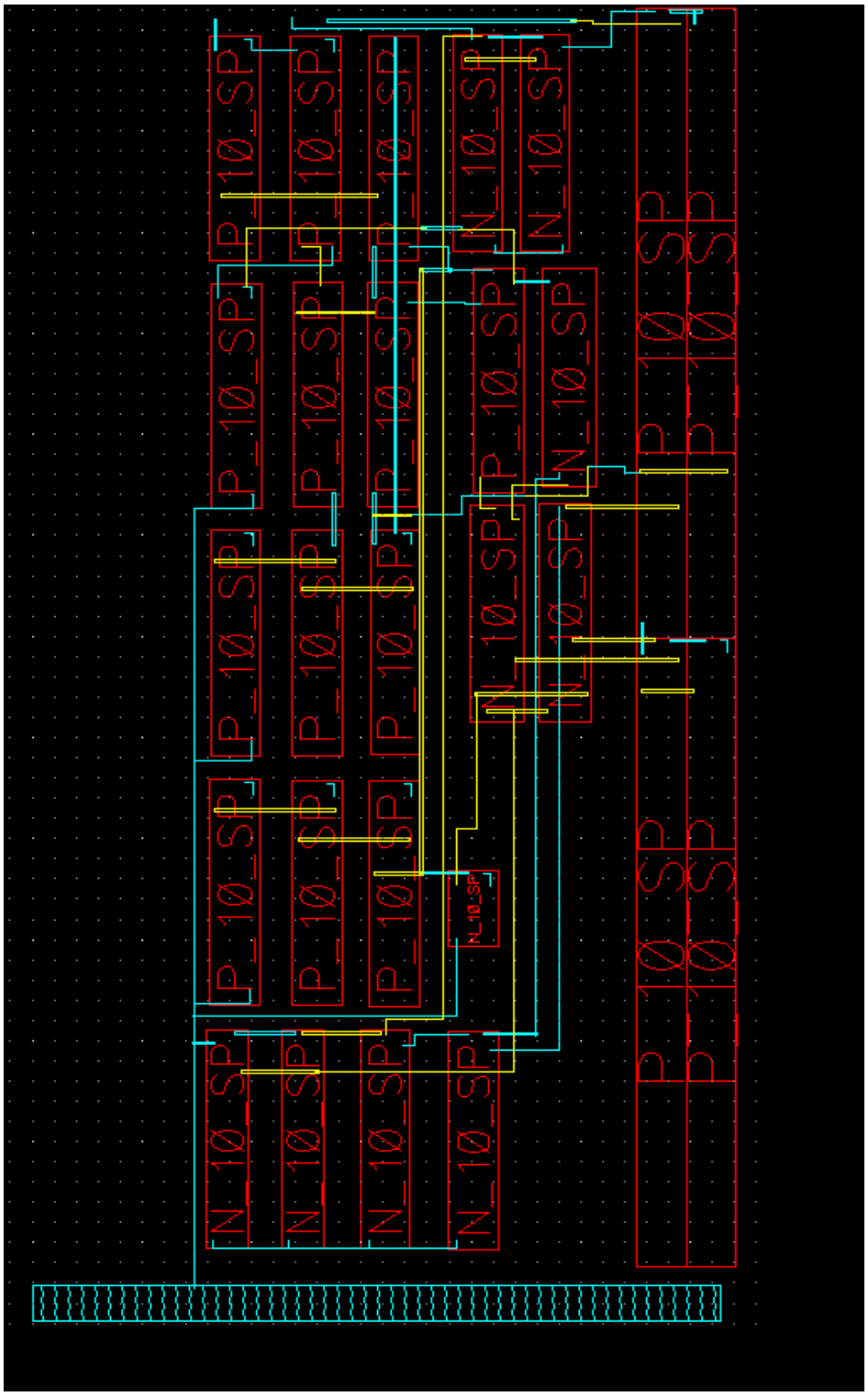


Figure 7.4 Layout of differential based voltage down converter

Figure 7.4 and 7.5 shows the layout of down converters. The size of the layout is 85x 45µm^2.

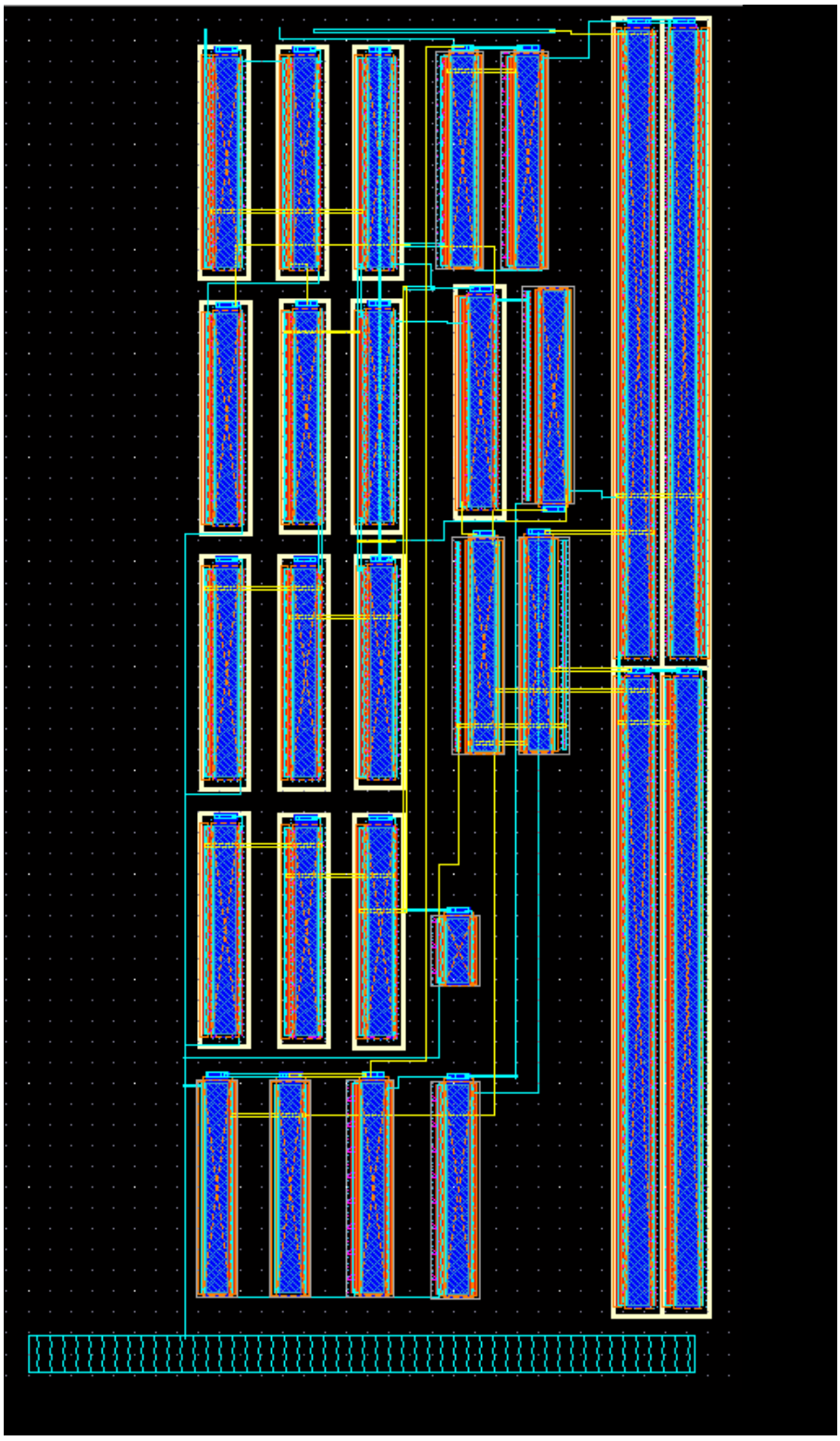


Figure 7.4 Layout of differential based voltage down converter with components layout

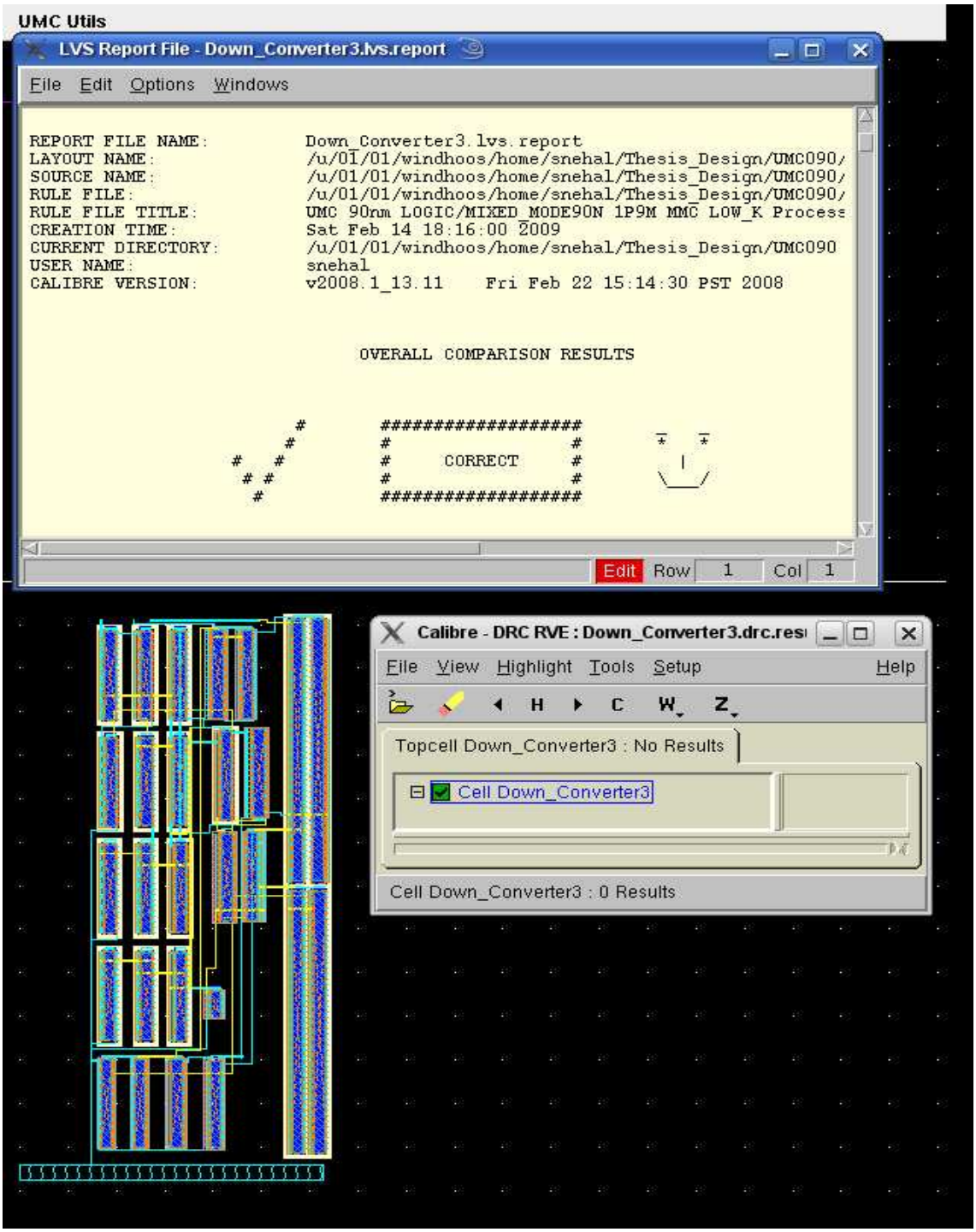


Figure 7.5 Layout of differential based voltage down converter with LVS and DRC

Figure 7.5 shows the layout of down converter with Layout v/s Schematic (LVS) and Design Rule Check (DRC) performed on the converters.

7.3 Summary

In this chapter layout of SC DC-DC up converter and differential based voltage down converter is designed in UMC90. The layout of up converter is designed using 3 metal layers while design of down converter is designed using 2 metal layers. The layout of up converter is 110 x 135μm^2 and down converter is 85 x 45μm^2.

8 Conclusion

8.1 Summary

In this thesis, a switched capacitor up converter and differential based voltage down converter are designed. The key contributions to the thesis are as follows:

- First of all, literature survey of on chip dc converter is done. Then the specifications of the dc converters are defined according to the system requirements.

- According to the specifications, choice is made between switched capacitor and inductor based converter. Switched capacitor converters are preferred due to accuracy; reduce size and complexity of the circuit. The dc converters are designed with desirable input range, high efficiency and small layout area.

- A load model is designed to see the behavior of converters to switching circuits. Lastly layouts of up and down converters are designed. The LVS and DRC check is performed for both layouts.

8.2 Future work

In this section some ideas for future work are stated:

1. Future exploration of the design space would involve comparing the SoC with an integrated DC-DC Converter, to a SoC without one. This would lead to the identification of the various effects that may potentially arise due to the IR drops in the supply lines in the absence of a DC-DC converter.

2. After comparison, the chip can be fabricated and tested to check the overall performance of the Converter after fabrication

3. Models can be developed in Matlab to implement the designed up and down converte

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