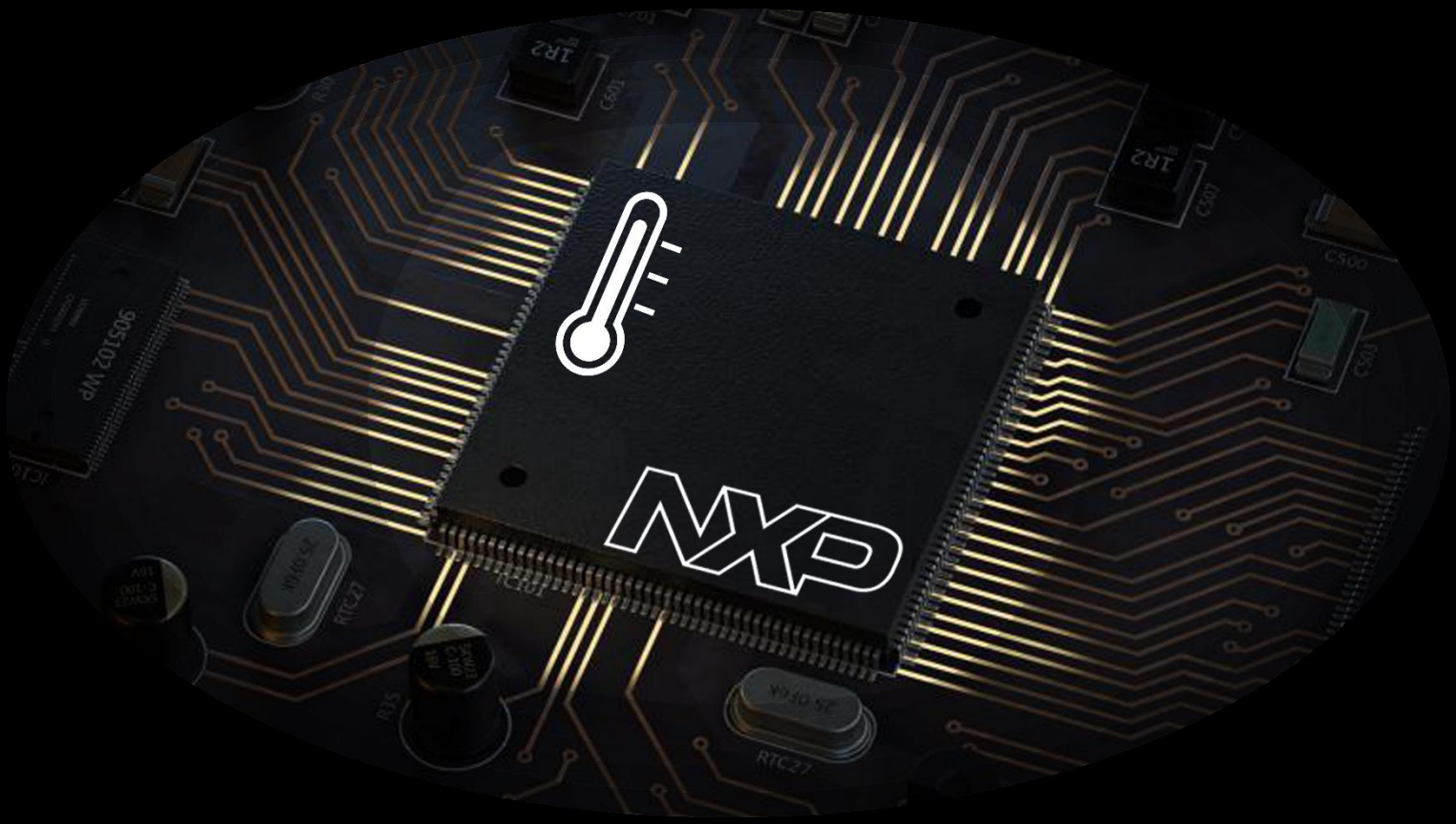
A Programmable Temperature Switch

S.S. Rautmare



TU Delft

NXP

A Programmable Temperature Switch

By

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Abstract

Temperature threshold sensors facilitate temperature protection in microprocessors by indicating when the processor gets overheated or too cold. This thesis presents a BJT based temperature sensor with a programmable temperature threshold from -40°C to 150°C. Comparison of a CTAT voltage with a PTAT voltage gives a one-bit digital output when the temperature of the die exceeds the set threshold. This work achieves a temperature detection accuracy of ±0.75°C, leading to the lowest reported relative inaccuracy among temperature switches by using a room temperature digital trim and without the use of any dynamic techniques. The design has a current consumption of 7uA, and the estimated area of the system is less than 0.05mm^2 in 0.16um CMOS technology.

Acknowledgement

Graduate school has been an eventful journey with its ups and downs and through it all, I had the support of numerous people who helped me accomplish this thesis.

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My parents have been very patient, supportive and understanding throughout my studies. Thank you for understanding me through all the technical gibberish that I spoke and always being there for me.

-S.S. Rautmare

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Chapter 1 Introduction

1.1. Motivation

In today's data-driven world, microprocessors comprising millions of transistors need to process data at GHz rates, leading to high current consumption. This, in turn, leads to increased temperatures, either at local hot-spots or of the entire die. To avoid the accelerated device ageing associated with higher temperatures [1], die temperature should be kept below a certain maximum temperature threshold (typically 125°C). Thus, thermal sensors, which can sense die temperature, and thermal management units, that can lower the temperature by taking corrective action, are required.

The output of a thermal sensor can either be a digital word with temperature information or a one-bit signal that indicates that a temperature threshold has been exceeded. These two architectures are shown in Fig. 1-1.

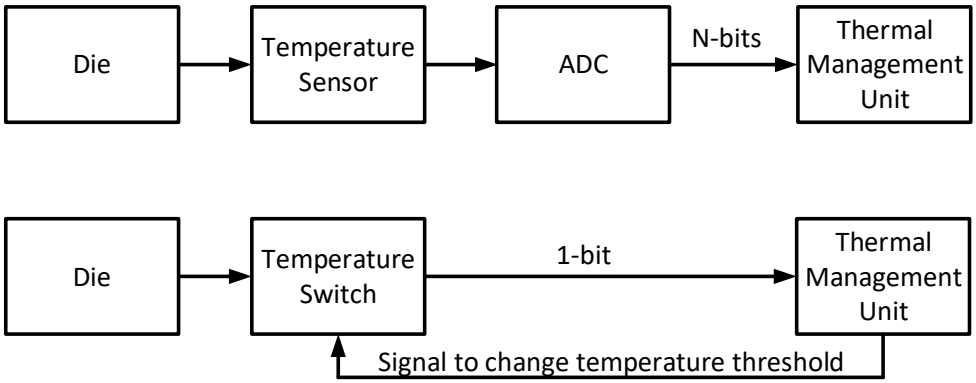


Fig. 1-1:Signal flow in ADC based design and in a programmable temperature switch

Sensors that output a digital word, are more complex because they typically incorporate an analog-to-digital converter (ADC). The thermal management unit then uses the digital word to determine if a pre-programmed temperature threshold is exceeded. Although quite flexible, the need to process the digital word leads to a slower system response time. Temperature switches that provide a one-bit signal have faster response times and also a simpler implementation. Since the temperature switch only provides a signal to the thermal management unit when the temperature threshold is exceeded, the programmability of the temperature threshold has to be done within the sensor itself. On receiving the 1-bit signal, the thermal management unit either reduces the frequency of operation or powers down the device until the operating temperature drops to safe levels.

The algorithm that the thermal management unit uses to control the temperature of the processor must include a safety margin to account for sensing errors. For typical processor heatsinks with thermal resistance, a 5°C error in temperature threshold detection corresponds to a 10W safety margin. Since processors generally typically dissipate less than 100W of power, an error of 10W implies a significant loss in the processor's performance. Hence, more accurate temperature threshold detection is required[2].

Apart from detecting overheating conditions, thermal sensors should also be able to sense cold temperatures, because chip performance can deteriorate due to the inverse temperature dependence of the threshold voltage and mobility. To reduce the impact on the processor performance due to the increased threshold voltages at cold temperatures, the thermal management unit has to increase the supply voltage to the processor. Hence localized measurement of cold-spots is also required.

In practice, multiple hot-spots/cold-spots may be present on the die of a large processor. As a result, multiple programmable thermal switches (PTS) are required to detect the temperature, as shown in Fig. 1-2.

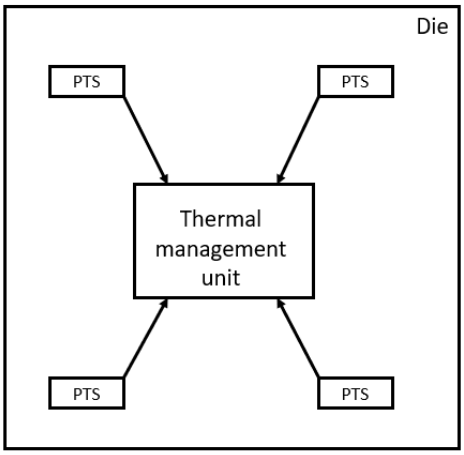


Fig. 1-2: multiple programmable temperature switches on a single die

Each switch must then be as small as possible to minimize their total area and reduce manufacturing cost. According to [3], thermal switches in older technology nodes (greater than 65nm) occupy areas between $2mm^2$ to $0.02mm^2$, becoming even lower in advanced nodes (below 65nm), with state-of-the-art designs occupying less than $0.0025mm^2$[4].

During the initial stages of the design, the positioning of these PTS is difficult as accurately predicting the location of potential hot-spots/cold-spots is difficult. Hence it should be possible to move the position of the PTS flexibly in the layout, even at later stages of the design. This requirement places a serious constraint on the clock routing. To simplify clock routing, the PTS has to be independent of a clock signal. Furthermore, dynamic techniques, such as chopping, require a large filter capacitor resulting in an increased area requirement. Hence a non-dynamic PTS design is preferred.

Another concern while developing thermal sensors is their need for calibration at stable, well-known temperatures. This is quite costly to do in mass production, and so sensors that require minimum calibration temperature points are preferred.

1.2. Target Specifications

These considerations provide a starting point for the design of a temperature switch with multiple temperature thresholds, no dynamic techniques, only 1-point temperature calibration and a large temperature detection range as target specifications.

There are four main temperature sensing elements compatible with CMOS technology.

1. MOS-based temperature sensors [5], [6] are susceptible to process, channel doping and gate oxide thickness variations.
2. Resistor-based sensors [7]–[9] are area and power-efficient but require expensive multi-point trimming to get the desired temperature accuracy.
3. Thermal diffusivity based temperature sensors [2], [10] uses electro-thermal filters (ETF) which typically require high power.
4. BJT based temperature sensors [11], [12], require low power and provide good accuracy for a 1-point trim.

Hence, in this work, only the use of BJTs as sensing elements are considered. However, NPN transistors require a deep N-well for their realization which is not available in the CMOS 160-flv process. Hence PNP transistors are used to create a BJT based PTS.

The performance of previous BJT-based temperature switches is summarized below, together with the target specifications of this thesis.

	Schinkel et al. [13]	Duarte et al. [14]	Bass et.al. [15]	Lu et al. [16]	Canio et al. [17]	Target
Technology (nm)	180	65	65	22	28	160
Output type	1-bit	1-bit	8-bit	8-bit	1-bit	1-bit
Temperature range (ºC)	125	30 to 105	-10 to 110	-30 to 120	-40 to 125	-40 to 150
Trimming Type	NA	2-point	2-points	1-point		1-point
3-sigma inaccuracy (ºC)	±4.6	±1.1	±1.35	±1.07	±4.0	±1.0
Relative inaccuracy (%)	3.68	1.33	1.12	0.71	2.42	0.52
Power Consumption (uA)	13	1200	86	50	72	-
Dynamic techniques	NA	chopping	NA	NA	NA	NA
Area estimate(mm^2)	0.03	0.027	0.003	0.0043	0.075	0.03

1.3. Thesis Organization

The thesis has been organized into the following chapters

Chapter 2: This chapter explains the operating principle of the temperature sensor. It is followed by a discussion about the impact of various error sources on its accuracy.

Chapter 3: In this chapter, the proposed system design is outlined. System-level propositions are made, and the trade-offs regarding those choices are explained.

Chapter 4: The circuit-level implementation of the temperature sensor is explained.

Chapter 5: Simulation results for the designed sensor are shown. These include the performance of the trimming circuits and the entire system assuming the presence of various error sources.

Chapter 6: Conclusions are drawn, along with possible suggestions for future work.

Chapter 2 System Analysis

This chapter reviews the literature and explains the operating principles of BJT based temperature switches. It also discusses the impact of various error sources on the accuracy of their temperature thresholds.

2.1 Introduction

Temperature detection can be done by comparing a temperature-dependent quantity with a reference, which may or may not be temperature-dependent. Our options, regarding these two quantities, are limited to those that can be created with BJTs, as discussed in section 1.2. These quantities are generated using the circuit shown in Fig. 2.1

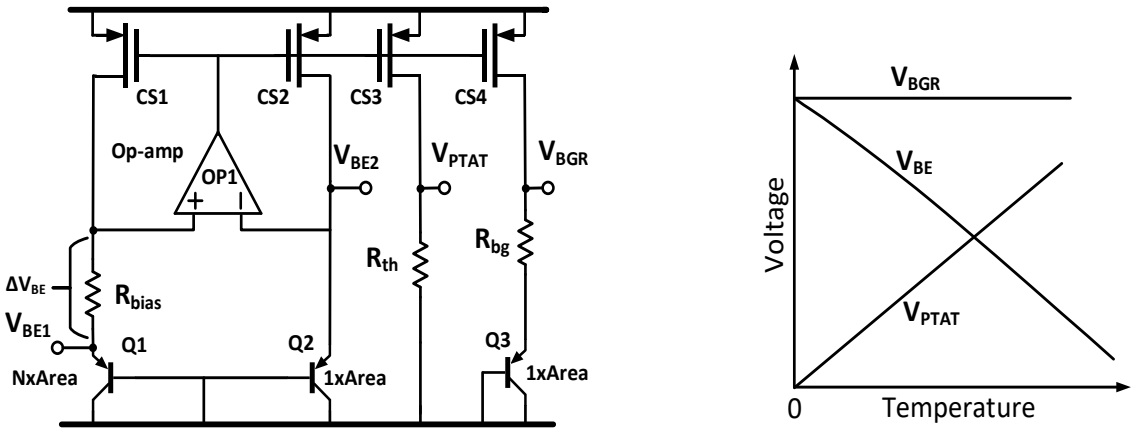


Fig. 2-1: Bandgap, V_{BE} and V_{PTAT} (a) generator circuit and (b) behaviour over temperature

The circuit comprises of substrate PNP transistors, Q1-3, which are biased via their emitters using the current, I_{PTAT}, from identical PMOS current sources, CS1-4. Due to the virtual ground established by the op-amp (OP1), a potential difference, ΔV_{BE} is developed over a resistor R_{bias}, which is proportional to the absolute temperature (PTAT). Due to the current, an amplified PTAT voltage (V_{PTAT}) is also developed over resistor R_{th}, while a voltage complementary to the absolute temperature (CTAT) is developed across the PNP transistors, V_{BE}. A combination of CTAT and PTAT voltages using Q3 and R_{BGR} results in a constant voltage with respect to temperature, which is known as a bandgap reference voltage (V_{BGR}). The behaviour of V_{BE}, V_{PTAT}, and V_{BGR} with respect to temperature is shown in Fig. 2-12.1(b).

Transistors Q1 and Q2 have a current density ratio of 1: N, due to their different emitter areas. Thus, the same current flowing through Q1 and Q2 results in two different base-emitter voltages, namely, V_{BE1} and V_{BE2}. The base-emitter voltages (V_{BE1} and V_{BE2}) and ΔV_{BE} are derived as follows:

$$V_{BE1} = \frac{kT}{q} ln \frac{I_{PTAT}}{NI_s} \qquad 2.1(a)$$

$$V_{BE2} = \frac{kT}{q} ln \frac{I_{PTAT}}{I_s} \qquad 2.1(b)$$

$$\Delta V_{BE} = V_{BE2} - V_{BE1} = \frac{kT}{q} ln\ N \qquad 2.2$$

Where 'kT/q' is the thermal voltage and 'I_s' is the saturation current of the PNP transistors The current I_{PTAT} is defined using ΔV_{BE} and R_{bias}

$$I_{PTAT} = \frac{\Delta V_{BE}}{R_{bias}} \quad 2.3$$

Based on the definition of I_{PTAT}, V_{PTAT} and V_{BGR} can be defined as

$$V_{PTAT} = \frac{R_{th} \times \Delta V_{BE}}{R_{bias}} \quad 2.4$$

$$V_{BGR} = \frac{R_{bg} \times \Delta V_{BE}}{R_{bias}} + V_{BE3} \quad 2.5$$

Using V_{BE}, V_{PTAT} and V_{BGR}, possible combinations for temperature threshold detection are V_{BE} vs V_{PTAT}, V_{BE} vs V_{BGR} and V_{PTAT} vs V_{BGR}.

2.1.1 Sensitivity

To identify the optimum combination for temperature detection the sensitivity of the various possibilities must be investigated. Sensitivity is defined as the change in voltage required to change the temperature threshold. Here the temperature threshold is the temperature at which the voltages of the above-described pairs of quantities are equal. To derive the sensitivity of the resulting temperature switch, consider the diagram shown in Fig. 2-2.

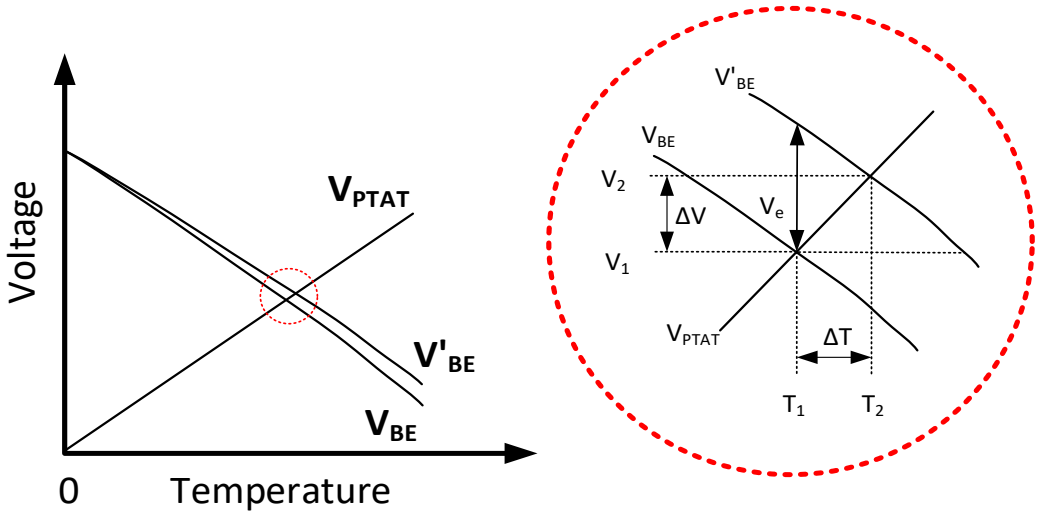


Fig. 2-2: Behaviour of the circuit in presence of error in V_{BE}

It is assumed that V_{PTAT} and V_{BE} are straight lines that intersect at temperature T_1, and a corresponding voltage V_1. An error introduced in V_{BE}, denoted by 'V_e', changes the base-emitter voltage to V'_{BE}, while V_{PTAT} remains unchanged. Because of this, the new temperature threshold for the system is T_2 at voltage V_2. This change in temperature threshold from T_1 to T_2 is denoted by 'ΔT', while the change in threshold voltage from V_1 to V_2 is denoted by 'ΔV'. The slope of V_{PTAT} and V_{BE} is given by

$$Slope\ of\ V_{PTAT} = \frac{V_2 - V_1}{T_2 - T_1} = \frac{\Delta V}{\Delta T} \quad 2.4$$

$$Slope\ of\ V_{BE} = \frac{V_2 - (V_1 + V_e)}{T_2 - T_1} = \frac{\Delta V - V_e}{\Delta T} \qquad 2.5$$

Substituting Eq. 2.4 in Eq. 2.5, the error voltage can be expressed as

$$\frac{V_e}{(|Slope\ of\ V_{PTAT}| + |Slope\ of\ V_{BE}|)} = \Delta T \qquad 2.6$$

Thus, sensitivity is a function of the slopes of the compared quantities. A higher relative slope of the compared input voltages implies a higher resilience of the temperature threshold to error voltages, e.g. due to offset in the op-amp or spread in the saturation current of the BJTs. Eq. 2.6 implies that the use of a scaled bandgap voltage as one of the quantities for comparison will not be ideal as this will reduce the sensitivity of the switch. Based on this inference, only architectures that compare V_{PTAT} to V_{BE} will be considered for use in the temperature switch.

2.2 Literature Review

In [13], a temperature switch with a fixed temperature threshold is proposed. As can be seen in Fig. 2-3, it is based on the circuit shown in Fig. 2-1. A comparator compares V_{BE2} and V_{PTAT} and provides a digital output when the threshold is exceeded. The temperature threshold is the temperature where the value of V_{BE2} is equal to V_{PTAT} as shown in Fig. 2-3(b). This architecture entirely relies on transistors sizing to mitigate the impact of offset and mismatch. Since there is no feature to reduce the impact of the saturation current spread, the resultant temperature detection error is high (±4.6°C).

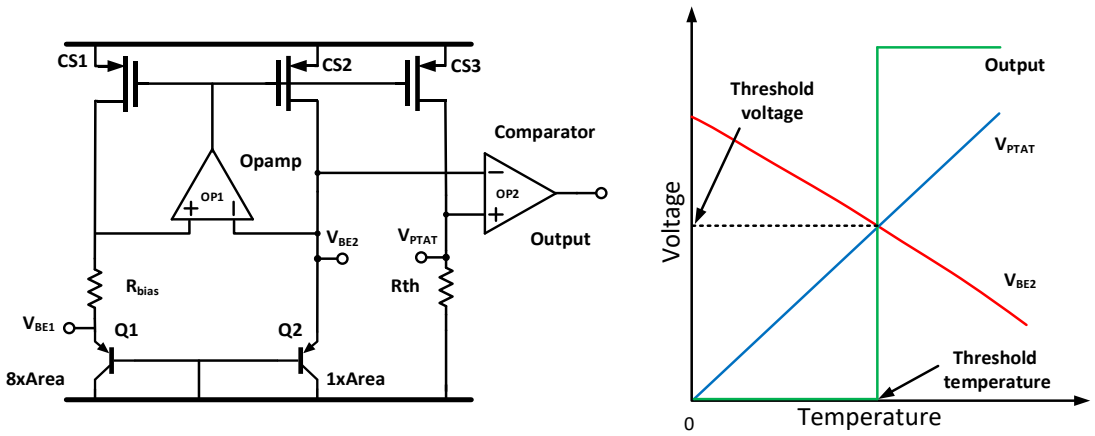


Fig. 2-3: (a) Architecture proposed in [13] (b)Waveforms showing its operating principle

Since [13] is affected by offset and saturation current spread, the design proposed in [14] uses chopping to reduce the offset, and a two-point temperature trim to reduce the impact of the saturation current spread. The overall design proposed in [14] is shown in Fig. 2-4. Here the current going into the resistor, R_c, and the emitter of Q3 is varied using a current-DAC (I-DAC), resulting in a programmable V_{DAC}. This V_{DAC} consists of a PTAT voltage developed over R_c and a CTAT voltage, V_{BE3}, developed over Q3. The comparator compares V_{DAC} and V_{PTAT} to detect the temperature threshold.

A drawback of the design is a limited temperature detection range, due to the logarithmic nature of V_{BE3}, and the limited current generation range of the I-DAC. Apart from the temperature range, since the V_{DAC} is a combination of a PTAT and a CTAT voltage its slope is less

compared to a purely CTAT V_{BE}, over temperature. This implies that this architecture is more susceptible to errors due to reduced sensitivity based on Eq. 2.6.

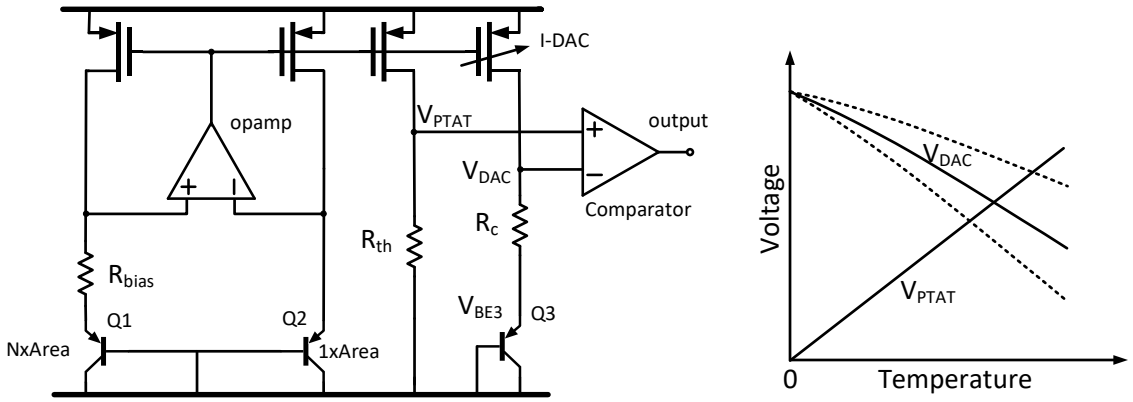


Fig. 2-4:Architecture proposed in [14]

Based on the requirement of a large temperature range and high sensitivity, the architecture proposed in [13] is used to develop our programmable temperature switch.

2.3 Error Analysis

The impact of various error sources on V_{BE} and V_{PTAT} is discussed in this section. The various error sources affecting this architecture are shown in Fig. 2-5 and listed in Table 2-1.

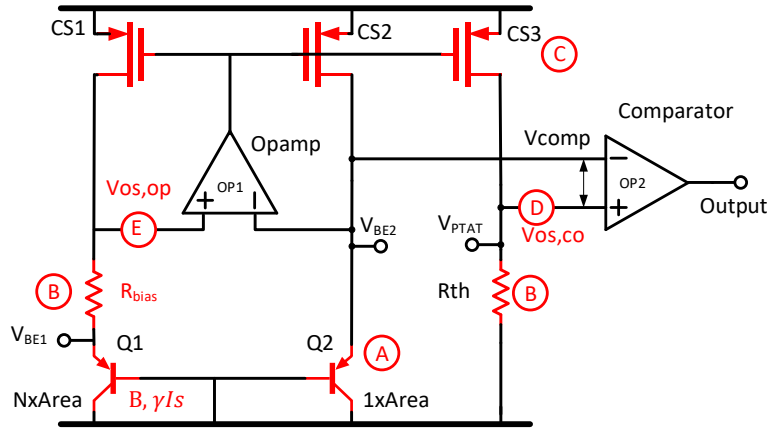


Fig. 2-5: Error sources

Table 2-1: List of error sources

A	Saturation current spread, Current gain spread, Series BJT resistance
B	Resistor mismatch
C	Current source mismatch
D	Op-amp offset
E	Comparator offset

Here it can be seen that Q1 and Q2 suffer from the spread in saturation current, parasitic series resistance as well as spread in their current gains. The resistors, R_{th} and R_{bias}, are affected by mismatch and a spread in their resistance values due to the thermal expansion. The current

sources, CS1-3, are also affected by the mismatch. The op-amp and the comparator are affected by an offset which is a result of a mismatch in their building transistors.

2.3.1 Saturation current spread

The saturation current (Is) is an intrinsic quantity of the substrate PNP transistors. The relation of the saturation current and the base-emitter voltage is given by Eq. 2.1(a). The impact of spread in the saturation current (ΔIs) to the V_{BE} is given by Eq. 2.7[18]

$$V'_{BE} = V_{BE} - \frac{kT}{q}\left(\frac{\Delta Is}{Is}\right), assuming\ (\Delta Is \ll Is) \qquad 2.7$$

Here V'_{BE} is the base-emitter voltage with the error due to the saturation current spread (ΔI_s), while V_{BE} is the ideal base-emitter voltage. It can be seen that the spread in the saturation current results in a PTAT error in V_{BE}, which can be corrected by a PTAT trim.

2.3.2 BJT current gain spread

The circuit shown in Fig. 2-5, biases the substrate PNP transistors via their emitters. This implies that the collector current and thus the V_{BE} is dependent on the transistor's current gain. Let α be the current gain from emitter to collector and β_f be the current gain from base to the collector. The relation between α and β_f is given by

$$\alpha = \frac{\beta_f}{1 + \beta_f} \qquad 2.8(a)$$

Based on the Eq. 2.8(a) the spread in α can be expressed as

$$\frac{\Delta\alpha}{\alpha} = \frac{1}{1 + \beta_f (T/T_r)^X}\frac{\Delta\beta_f}{\beta_f} \qquad 2.8(b)$$

Where '*Tr*' stands for the reference temperature used and '*X*' is the non-ideality coefficient (≈2). From which we can see that $'\Delta\alpha/\alpha'$ will also be temperature-dependent. The impact of spread in the current gain on the base-emitter voltage is given by

$$V'_{BE} = V_{BE} + \frac{kT}{q}\frac{\Delta\alpha}{\alpha} \qquad 2.9$$

where V_{BE} is ideal base-emitter voltage while the second term denotes the error introduced by the spread in the emitter-collector current gain. This expression looks similar to the saturation current spread, however, the error introduced by the current gain spread is not purely PTAT as seen in Eq. 2.8(b), and therefore cannot be completely corrected by a PTAT trim, resulting in a residual error. This residual spread in V_{BE} can be reduced either by increasing the value of β_f or by decreasing $\Delta\beta_f$.

2.3.3 Series Resistance

The V_{BE} that we measure at the emitter of the PNP transistor is comprised of the actual V_{BE} and the potential drop across the emitter resistance, Re, as well as the base resistance Rb as shown in Fig. 2-6(a). The combined series resistance, Rs, is given by Eq. 2.10[18]

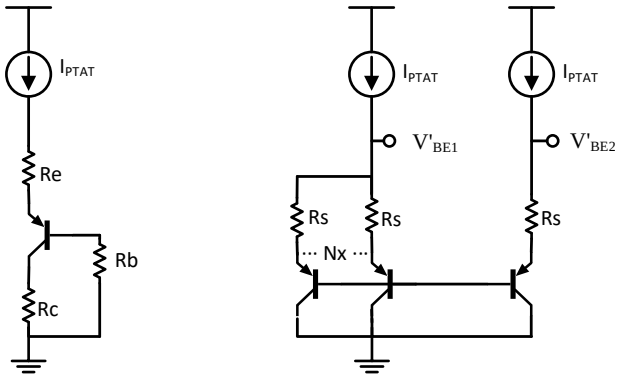


Fig. 2-6: (a)Parasitic resistance structure in the BJT (b) Series resistances modelled as a single resistance Rs

$$Rs = Re + \frac{Rb}{1+\beta} \tag{2.10}$$

The impact of series resistance on ΔV_{BE} and V_{BE}, for a given current density ratio of N, where N is the emitter area ratio between the two branches, is given by Eq. 2.13

$$V'_{BE} = V_{BE} + R_s I_{PTAT} \tag{2.11}$$

$$\Delta V'_{BE} = V'_{BE1} - V'_{BE2} \tag{2.12}$$

$$\Delta V'_{BE} = \Delta V_{BE} + I_{PTAT}\left(1 - \frac{1}{N}\right) Rs \tag{2.13}$$

Based on Eq. 2.11 and 2.13, the error due to series resistance is found to be PTAT in nature and can be corrected by a PTAT trim.

2.3.4 Current source (CS) mismatch

Current source mismatch will affect the current density ratio between Q1 and Q2. This affects the generation of both V_{BE} and V_{PTAT}. Assuming that the CS mismatch leads to a change in current by 'ΔI' which results in a change in the current density ratio by 'ΔN', then the change in V_{BE} and ΔV_{BE} is given by

$$V'_{BE} = \frac{kT}{q} ln\left(\frac{I_{PTAT} + \Delta I}{I_s}\right) \tag{2.14(a)}$$

$$V'_{BE} = V_{BE} + \frac{kT}{q} \cdot \frac{\Delta I}{I} \tag{2.14(b)}$$

$$\Delta V'_{BE} = \Delta V_{BE} + \frac{kT}{q}\left(\frac{\Delta N}{N}\right) \tag{2.15}$$

Based on Eq. 2.14 and 2.15, it appears that the impact of CS mismatch is also PTAT in nature. However, the derivation is based on the assumption that the mismatch is constant and not temperature-dependent. In reality, a temperature-dependent part of the current source mismatch will result in residual error after a PTAT trim is performed.

2.3.5 Resistor mismatch and spread

The impact of mismatch in the resistors (ΔR_{bias} and ΔR_{th}) is shown in Eq. 2.16 and Eq. 2.17.

$$V'_{BE} = V_{BE} - \frac{kT}{q}\frac{\Delta R_{bias}}{R_{bias}} \tag{2.16}$$

$$V'_{PTAT} = V_{PTAT} + I_{PTAT} \cdot \Delta R_{th} \quad 2.17$$

Both the equations show that the resistor mismatch can be resolved using a PTAT trim. But, the spread in the resistance due to the temperature coefficient of the resistors Npoly material will result in a finite error. However, the impact of this resistive spread will be less on V_{PTAT} as it is proportional to the ratio of two resistors. Hence the resistive spread is not considered in the error analysis.

2.3.6 Op-amp and comparator offset.

The op-amp offset, $V_{os,\,op}$, affects the current generation as it gets added to the ΔV_{BE}. As a consequence of this, the three current sources, CS1, CS2 and CS3 output additional currents Ios1, Ios2 and Ios3, respectively, apart from I_{PTAT}. However, as the current sources have the same dimensions, the error current due to offset for all three CS is also the same. The offset at the comparator, $V_{os,co}$, simply adds to the final temperature detection error. These error sources and error currents due to offset are shown in Fig. 2-7. The impact of the op-amp offset on I_{PTAT} is assessed and presented in Eq. 2.23

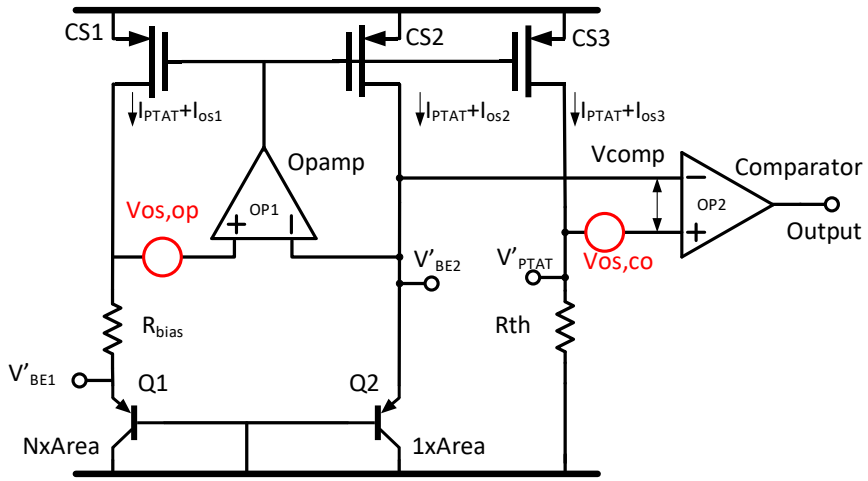


Fig. 2-7:Circuit diagram showing the op-amp and comparator offset and the current error sources

$$I_{PTAT} = A \times (Input_+ - Input_-) \quad 2.18$$

Here A is the gain of the op-amp, while the $Input_+, Input_-$ are its inputs.

$$I'_{PTAT} = A \times \{\{Vos,op + R_{bias}(I'_{PTAT}) + V'_{BE1}\} - V'_{BE2}\} \quad 2.19$$

$$I'_{PTAT} = \frac{A}{(1 - AR_{bias})} \times (Vos,op + V'_{BE1} - V'_{BE2}) \quad 2.20$$

$$I'_{PTAT} = \left(\frac{Vos,op}{R_{bias}} + \frac{V_t}{R_{bias}} ln(N) - \frac{V_t}{R_{bias}} ln\left(\frac{I_{PTAT} + Ios1}{I_{PTAT} + Ios2}\right)\right) \quad 2.21$$

Since Ios1 = Ios2, the 3rd term in Eq. 2.20 can be simplified as

$$V_t \, ln\left(\frac{I_{PTAT} + Ios1}{I_{PTAT} + Ios2}\right) \approx \; 0 \qquad 2.22$$

Thus Eq. 21 can be simplified as

$$I'_{PTAT} = \left(\frac{Vos,op}{R_{bias}} + \frac{V_t}{R_{bias}} ln(N)\right) \qquad 2.23$$

From Eq. 23. V_{PTAT} can be derived as

$$V'_{PTAT} = \frac{R_{th}}{R_{bias}} \cdot Vos,op + \frac{R_{th}}{R_{bias}} \cdot V_t \, ln(N) \qquad 2.24$$

This shows the impact of the op-amp offset on the voltage developed over R_{th}. The first term is the result of the op-amp offset. V_{PTAT} and V'_{BE2} are compared along with the comparator offset at the comparator.

$$V'_{comp} = V'_{PTAT} + Vos,co - V'_{BE2} \qquad 2.25$$

Where V'_{BE2} is the error in V_{BE2} due to op-amp offset and is given by

$$V'_{BE2} = \; V_{BE2} + V_t \left(\frac{Ios2}{I_{PTAT}}\right) \qquad 2.26$$

Substituting the value of V_{PTAT} from Eq. 2.24

$$V'_{comp} = \left\{\frac{R_{th}}{R_{bias}} \cdot Vos,op + \frac{R_{th}}{R_{bias}} \cdot V_t \, ln(N)\right\} + \; Vos,co - V'_{BE2} \qquad 2.27$$

In ideal circumstances; without any offset, the voltage at the comparator is given by

$$V_{comp} = \left(\frac{R_{th}}{R_{bias}} \cdot V_t \, ln(N)\right) - V_{BE2} \qquad 2.28$$

Subtracting Eq. 2.28 from Eq. 2.27, the error at the comparator due to op-amp and comparator offset is given by

$$\Delta V_{comp} = \; Vos,co + \left(\frac{R_{th}}{R_{bias}}\right) Vos,op + V_t \left(\frac{Ios2}{I_{PTAT}}\right) \qquad 2.29$$

Since (I_{os2}/I_{PTAT}) is a very small quantity, it can be ignored, simplifying Eq. 2.29 to

$$\Delta V_{comp} = Vos,co + \left(\frac{R_{th}}{R_{bias}}\right) Vos,op \qquad 2.30$$

Assuming that the structures for the op-amp and the comparator are similar and they see a similar statistical offset, based on Eq. 2.30, it can be inferred that the error in temperature threshold detection is primarily due to the amplification of the op-amp offset by a factor of (R_{th}/R_{bias}). The comparator offset does not see this amplification and thus contributes less to the overall temperature error. The offset can be reduced by increasing the dimensions of the op-amp or by resorting to an offset trimming technique.

2.4 Conclusion

Based on the impact of various sources to V_{BE} and ΔV_{BE}, it can be seen that all the PTAT error sources can be corrected by a single PTAT trim, while a separate trimming/mitigation technique will be required for non-PTAT error sources.

Error sources like the saturation current spread, CS mismatch and op-amp offset have the potential to severely impact the temperature threshold detection, hence their impact should be mitigated by proper system design. This can be done by increasing the current density ratio to ensure that the impact of the error source is less and by including specific error mitigation circuits for the saturation current spread, CS mismatch and op-amp offset.

2.5 Summary

The system analysis and the impact of various error sources on V_{PTAT} and V_{BE} are summarized below

1. An analysis of the sensitivity of the temperature switch shows that the greater the relative slope of the inputs to the comparator, the lower the impact of various error sources on the detected temperature.
2. Based on the need for high sensitivity, the need to operate over a large temperature range, as well as the use of a minimum of external components, the architecture proposed in [13], which compares V_{PTAT} and V_{BE}, is chosen as the starting point of this design.
3. The various error sources have been categorised based on their behaviour with temperature. This clarifies the choice of error compensation techniques, as all PTAT error sources can be tackled by a PTAT trim, while separate error mitigation circuits will be required to remove non-PTAT errors.

Error	Nature	Error Voltage
Saturation current spread	PTAT	$\frac{kT}{q}\left(\frac{\Delta Is}{Is}\right)$
Current gain spread	Non-PTAT*	$\frac{kT}{q}\frac{1}{1+\beta_f(T/T_r)^X}\frac{\Delta\beta_f}{\beta_f}$
BJT Series resistance	PTAT	$I_{PTAT}\left(1-\frac{1}{N}\right)Rs$
Current source mismatch	Non-PTAT*	$\frac{kT}{q}\cdot\frac{\Delta I}{I}$
Resistor mismatch	PTAT	$I_{PTAT}\cdot\Delta R_{th}$
Op-amp offset	Non-PTAT	$\left(\frac{R_{th}}{R_{bias}}\right)(Vos,op)$
Comparator offset	Non-PTAT	Vos,co

*The temperature dependence of the spread in current gain and the CS mismatch is not taken into account while deriving the formula for these error sources.

Chapter 3 System Design

This chapter discusses the detailed system-level design of the programmable temperature switch. It includes the choice of the current density ratio, op-amp topology and the programmable threshold parameter. This chapter also explains the ways in which PTAT and non-PTAT errors are mitigated.

3.1 BJT current density ratio (CDR)

Consider the basic design of the temperature switch shown in Fig. 3-1.

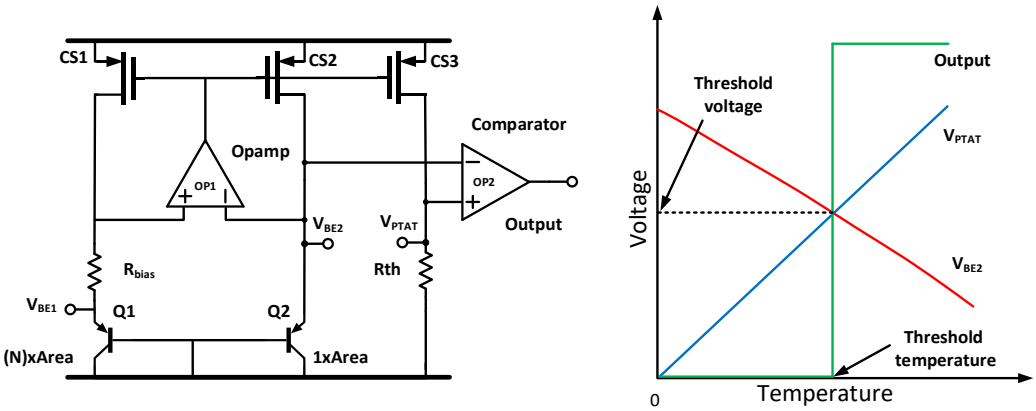


Fig. 3-1: Basic circuit design of a temperature switch

The temperature threshold is set by equating V_{PTAT} to V_{BE2}, where V_{PTAT} is ΔV_{BE} amplified by (R_{th}/R_{bias}). This amplification of ΔV_{BE} also results in the amplification of the op-amp offset as seen in Eq. 2.24 in section 2.4.6. Thus, to reduce the impact of the op-amp offset on the measured temperature threshold, the amplification factor has to be reduced either by decreasing V_{BE2} or by increasing the current density ratio (CDR).

Consider the case where V_{BE2} is reduced. V_{BE2} can be reduced by reducing the current through the transistor. However, to significantly reduce V_{BE}, the current has to be made very small (up to few pico-amperes) due to the logarithmic relation between them, which is not feasible. Another possible solution could be to use a current bleeding technique, in which, some of the current is diverted away from the PNP transistors (Q1 and Q2) into the current sinks (M4 and M5) [19] as shown in Fig. 3-2.

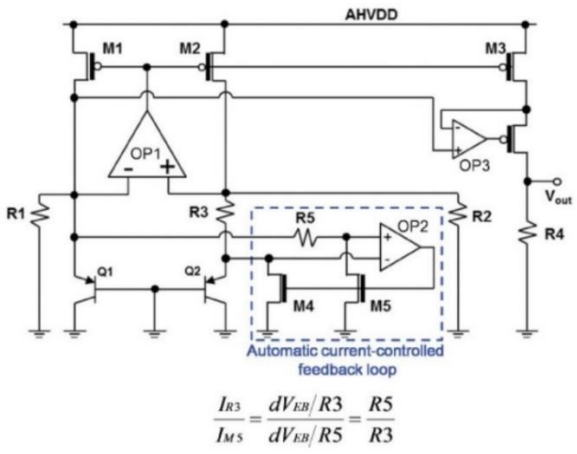


Fig. 3-2: Current bleeding technique used in [19]

However, this current bleeding technique requires a huge resistor(R5) and an additional op-amp (OP2) to set the ratio between the sourced and the sunk current, which isn't desirable. Hence, due to area concerns, reducing V_{BE} by decreasing I_{PTAT} is not a feasible approach.

The second case is when ΔV_{BE} is increased to reduce the required amplification. This can be done by increasing either the BJT emitter area of Q1 or the current flowing through Q2. Both these alternatives ensure that the amplification requirement of ΔV_{BE} is reduced. However, as the CDR increases, the errors due to the BJT series resistor and from the spread in the BJT current gain also increases. Thus, the combined impact of op-amp offset, current gain spread and the series BJT resistance as a function of the CDR has to be observed. The following subsections will show the impact of the series BJT resistance and the spread in current gain on V_{BE} and ΔV_{BE}.

3.1.1 Series BJT resistance.

The error introduced by the series resistance (Rs) in V_{BE} and ΔV_{BE}, as explained in section 2.4, and its impact on V_{BE} and ΔV_{BE} is summarized by the Eq. 2.10 and Eq. 2.12 [18]. It can be seen that as the CDR increases, the error introduced by the series resistance increases. In the target 160nm CMOS technology, the value of Rs is approximately 70Ω for a BJT emitter area of 5µm×5µm. To minimize the impact of the series resistance, the BJTs should be biased at micro-ampere levels of current. The choice of current also depends on the spread in the current gain, which is discussed in the next subsection.

3.1.2 Spread in the BJT current gain.

In section 2.4.2, the susceptibility of V_{BE} to the spread of the current gain is explained and is shown via Eq.2.7 [18]. Based on these equations, the spread in V_{BE} can be reduced either by increasing the value of β_f or by decreasing $\Delta\beta_f$. The value of β_f is fixed for a substrate PNP and is approximately 4.5. Thus, $\Delta\beta_f$ must be minimized to reduce the spread in V_{BE}. Fig. 3-3 shows the collector-base current gain of a PNP transistor with a fixed emitter area of 5µm×5µm for different emitter currents.

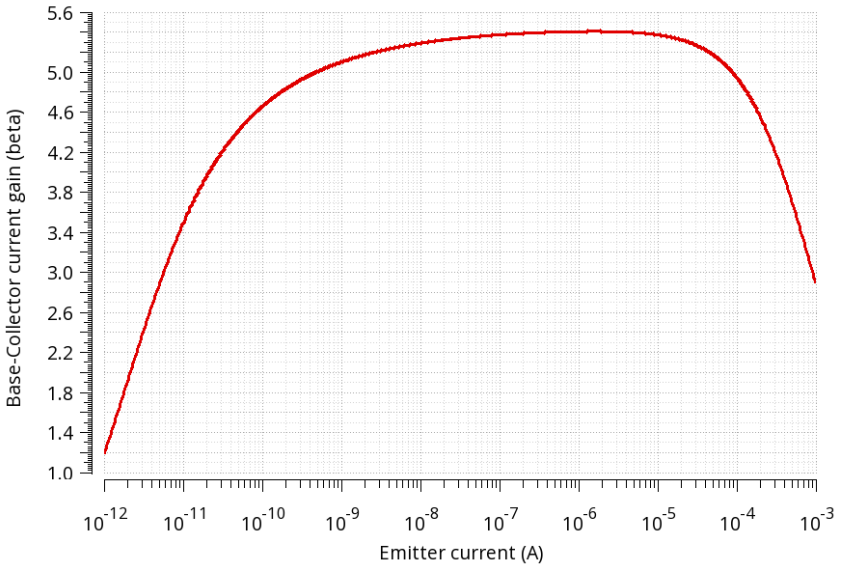


Fig. 3-3: Base-collector current gain vs emitter current:

It can be seen that β_f is almost constant for the emitter current range of 100 nA to 4 µA. Therefore, a current in the above-mentioned range must be chosen to minimize $\Delta\beta_f$.

Considering the impact of series resistance and the current gain spread, a current density of 100nA/unit emitter area is chosen.

3.1.3 Op-amp offset

To understand the effect of the op-amp offset on the temperature threshold, the amplified offset at V_{PTAT} has to be observed as a function of CDR. The CDR is varied by increasing the PNP emitter area and at the same time, R_{th} and R_{bias} are adjusted to get a fixed temperature threshold detection at 125 °C. 125°C is chosen as it is one of the required temperature thresholds for the application. A 1mV offset is applied at the input of the op-amp as shown in Fig. 3-4. The amplified op-amp offset is measured over R_{th}, as the difference between V_{PTAT} with and without offset. During this analysis, the BJT's are ideal to ensure that errors due to series resistance and spread in current gain is neglected.

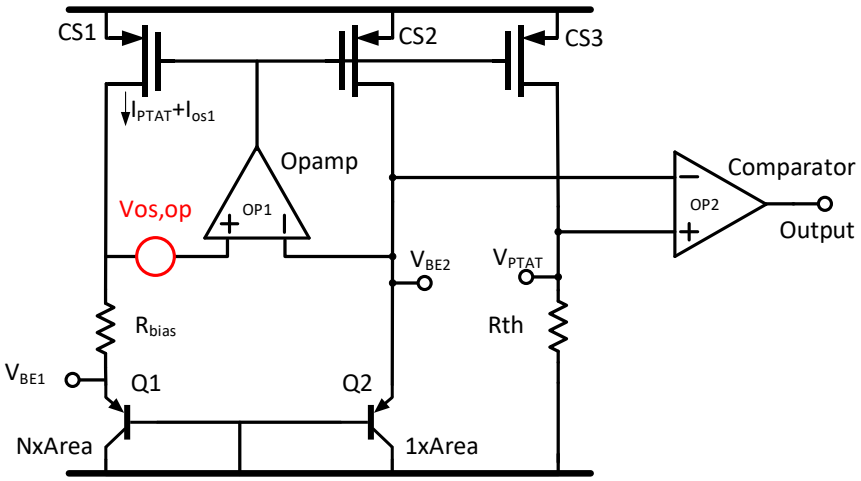


Fig. 3-4: Temperature switch with 1mV op-amp offset

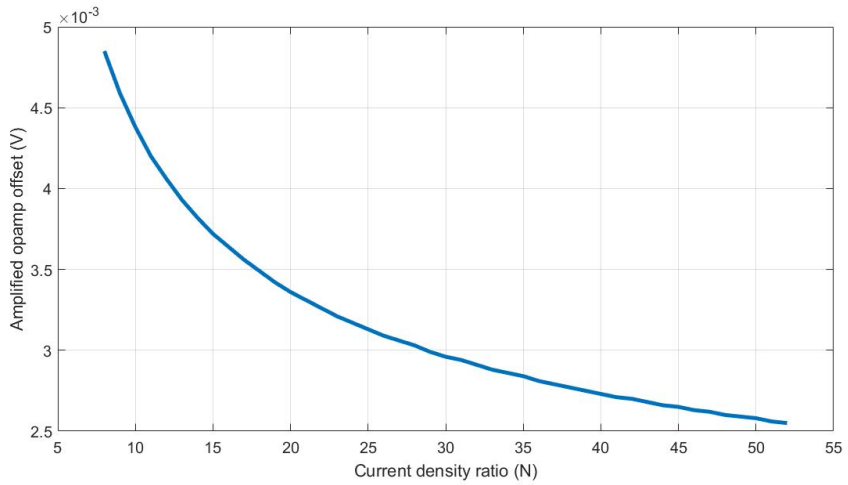


Fig. 3-5: Amplified op-amp offset as a function of the current density ratio

As can be seen in Fig. 3-5, as the CDR increases, the amplification of the op-amp offset decreases logarithmically. However, to get a holistic view of the effect of increasing the CDR, the combined error voltage due to series resistance, spread in current gain and op-amp offset has to be observed which is done in the next subsection.

3.1.4 Combined V_{error}

The root-mean-squared addition of combined error sources (op-amp offset, series resistance and spread in the current gain) on V_{PTAT} is denoted by V_{error}. V_{error} as a function of the CDR is presented in Fig. 3-6

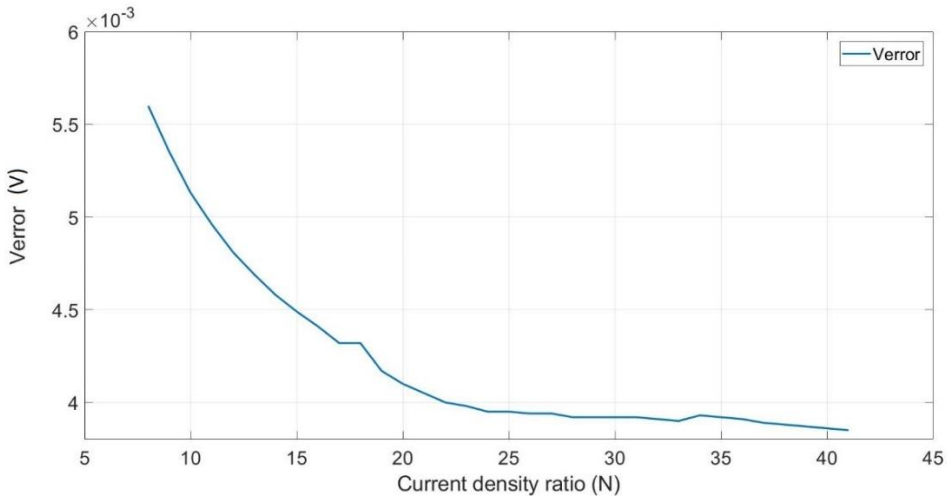


Fig. 3-6: Combined error, Verror, as a function of the current density ratio

Beyond a CDR of 1:20, any further increment in the CDR only has a small impact on V_{error}. This is because, beyond 1:20, the reduction in the impact of op-amp offset is compensated by the increase in errors due to current gain spread and series resistance. Hence a current density ratio of 1:20 is chosen for the system implementation.

3.1.5 Sensitivity

As explained in Section 2.1.1, the sensitivity of the temperature switch is a function of the slopes of the compared quantities: namely V_{BE} and V_{PTAT} as shown in Eq. 2.6. While V_{BE} has a slope of 2.18mV/K, the slope of V_{PTAT} depends on the programmed temperature threshold and the V_{BE} at that temperature. Thus, the sensitivity of the device changes as the slope of V_{PTAT} changes based on the choice of different temperature thresholds. The choice of current density as 100nA/unit emitter area and a CDR of 1:20 defines a current of 2µA in Q2 at room temperature (27°C). Thus, using the slope of V_{PTAT} at the extreme operating temperature of -40°C and 150° C, the sensitivity is calculated to be 5.18mV/K and 2.89mV/K respectively. These sensitivities are used in further sections to convert error voltages into corresponding temperature error.

3.2 Op-amp and its offset cancellation

In this section, the op-amp specifications are discussed. These specifications facilitate the decision on the choice of the op-amp's topology. This section also presents an offset cancellation scheme for the op-amp.

3.2.1 Op-amp requirements

The following section details the essential specification of the op-amp and the same have been shown in Fig. 3-7:

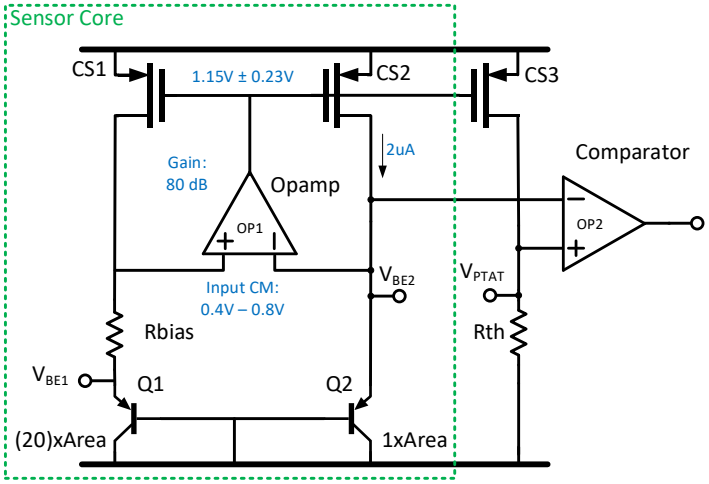


Fig. 3-7: op-amp specifications

1 **Input common-mode range:** As mentioned in the earlier section, BJT Q2 is biased with 2µA of current. With this bias current, the common-mode level of V_{BE} changes from 0.4V to 0.8V over the entire operating temperature range. This voltage range defines the input common-mode range of the op-amp.

2 **Output swing:** The op-amp's output is used to bias the PMOS current sources of the sensor core. The biasing voltage for the current sources determines the output common-mode voltage of the op-amp. As the bias voltage of the PMOS current sources varies from 1.4V to 0.9V over the entire temperature range, the required output swing is ±0.23V over a common-mode output voltage of 1.15V.

3 **Low offset:** The goal of the design is to achieve an accuracy of ±1°C in temperature measurement. Since the amplification of op-amp offset leads to a major error in temperature threshold detection, 50% or ±0.5°C of the total error budget is budgeted for the op-amp offset. Using the sensitivity at -40°C and 150°C as derived in section 3.1.4, this 0.5°C error budget translates to a maximum offset of 260µV at 150°C and 460µV at -40°C. Due to area constraints, it is not feasible to attain such low levels of offset by increasing the area alone. Also, the lack of a clock signal in the design implies that dynamic offset cancellation techniques cannot be used. Thus, a trimming-based offset cancellation technique has to be considered.

4 **DC gain:** Lower open-loop gain of the op-amp results in a weaker virtual ground at its inputs. As a result, the virtual ground can have an error of '$\pm V_{BE}$/Gain'. This error then adds to the ΔV_{BE} and gets amplified, like the op-amp offset. To minimize the error contributed by this limited op-amp gain, a high gain has to be realized. Since the targeted offset is around 260µV, the contribution of the error due to limited op-amp gain has to be at least 4x less than the offset. Based on this, a gain of 80dB is chosen.

3.2.2 Choice of op-amp topology

To ensure that all the op-amp transistors are in saturation for the given common-mode input voltage, a PMOS input pair is chosen. In the intended 160nm process, an advantage of a PMOS

input pair is its low noise and offset contribution compared to an NMOS input pair, for the same g_m and I.

While the common-mode input voltage determines the input stage, the common-mode output voltage sets the available headroom for the op-amp topology. Based on the common-mode output voltage (1.15V) and its swings (±0.23V), the available headroom for the PMOS transistors above the output node is only 0.42V.

Fig. 3-8 shows the two op-amp topologies; telescopic amplifier topology and the folded cascode topology.

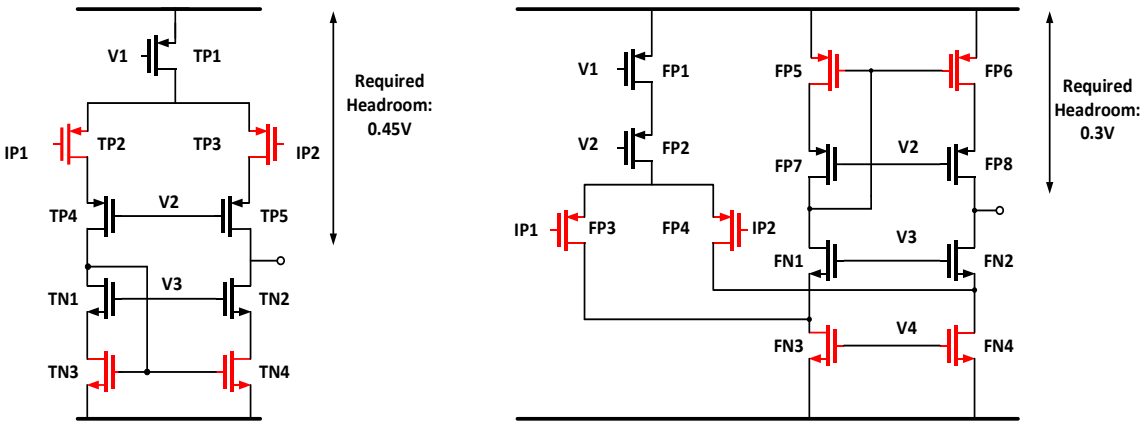


Fig. 3-8: Headroom constraints in (a) telescopic and (b) folded cascode amplifier

In both the amplifier topologies the PMOS current sources(TP1, FP1, FP5 and FP6) and PMOS cascodes (TP4-5 and FP2, FP7-8) are each allocated a headroom of 0.2V and 0.1V respectively, making the overall headroom requirement of the upper half of the amplifier as 0.45V and 0.3V respectively. Based on the headroom requirements and the available headroom, it can be seen that a telescopic topology doesn't fit into the given supply range, hence the folded cascode topology has been chosen. However, a drawback of the folded cascode topology is larger area requirements and a higher number of offset sources (transistors marked in red) as compared to the telescopic amplifier topology.

3.2.3 Offset cancellation circuit

Op-amp offset is one of the main sources of errors in temperature detection for this design. This offset arises from current-factor mismatch ($\Delta\beta/\beta$) and the threshold voltage mismatch (ΔV_{th}) of the transistors. The current-factor mismatch can be due to manufacturing defect, whereas, the threshold mismatch is caused by the change in doping concentrations. The current-factor mismatch can be represented by Eq. 3.1 [20]

$$\frac{\Delta\beta}{\beta} = \frac{\Delta\mu}{\mu} + \frac{\Delta C_{ox}}{C_{ox}} + \frac{\Delta W}{W} - \frac{\Delta L}{L} \qquad 3.1$$

where '$\Delta\mu$' is the mobility mismatch, 'ΔC_{ox}' is the oxide capacitance mismatch, 'ΔW' is the channel width mismatch and 'ΔL' is the channel length mismatch respectively.

The op-amp offset voltage is a function of threshold voltage and current-factor mismatch is defined by Eq. 3.2 [21]

$$V_{os} = \Delta V_{th} + \frac{I}{g_m}\left(\frac{\Delta\beta}{\beta}\right) \qquad 3.2$$

The threshold mismatch (ΔV_{th}) and the current-factor mismatch ($\Delta\beta/\beta$) are temperature-independent but I/g_m is temperature-dependent [21]–[23]. From Eq. 3.2, it can be deduced that the offset can be reduced, if the g_m is high, implying that the device should be biased in weak inversion region. If the input pair is biased in weak inversion, the trans-conductance of the transistor is given as

$$g_m = \frac{I}{nV_t} \qquad 3.3(a)$$

Where '*n*' is the non-ideality factor. Rearranging the terms in Eq. 3.3(a) we get Eq. 3.3(b) [21]

$$\frac{I}{g_m} \propto \frac{kT}{q} \qquad 3.3(b)$$

Which shows that I/g_m is PTAT in nature. Hence, the product of I/g_m and the current-factor mismatch results in a PTAT offset spread.

Offset cancellation can be done by eliminating the temperature-dependent and independent components separately or in a combined manner. This suggests three possible scenarios regarding offset cancellation techniques:

1. Both temperature-dependent and independent techniques are used[21].
2. Only a temperature-independent technique is used [24], [25].
3. Only a temperature-dependent technique is used. [26]–[29]

Of the above-mentioned architectures, the temperature-independent offset cancellation [21] and the reconfigurable differential pair from [26], [27] are considered for implementation. Because of the area restrictions, a combined offset cancellation technique is not preferred. The bandgap trim [21] is shown in Fig. 3-9

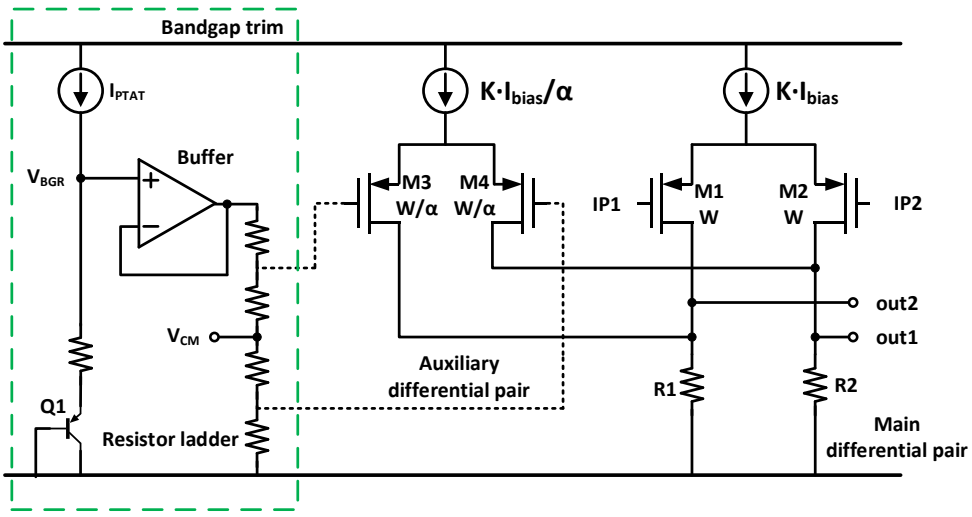


Fig. 3-9: Bandgap trim

It consists of a bandgap reference voltage connected to a resistive ladder through a buffer. The inputs of the auxiliary differential pair (ADP) are 'α' times smaller than the main differential pair and are biased using the differential voltages developed over the resistive ladder to perform a temperature-independent offset cancellation in the main differential pair (MDP).

An offset in the MDP will result in a differential current to flow through the resistors R1 and R2. To negate the effect of the offset in MDP, the ADP is biased such that it produces a differential current in with the opposite polarity as that of the offset. The current through the ADP and width of the ADP is 'α' times smaller compared to the MDP. Thus, the ratio of g_m of the two differential pairs is 1: α. Thus, a voltage α times the offset has to be applied to the inputs of the ADP. The resolution achieved using this technique is 30uV. However, for low current levels, the unit element of the resistive ladder becomes quite large and thus overall offset cancellation technique becomes area intensive.

In contrast, the reconfigurable differential pair (RDP) proposed in [26], [27], requires smaller size input pairs (as compared to the main differential pair) which can be switched on or off to trim the offset. The circuit implementation of the concept is shown in Fig. 3-10

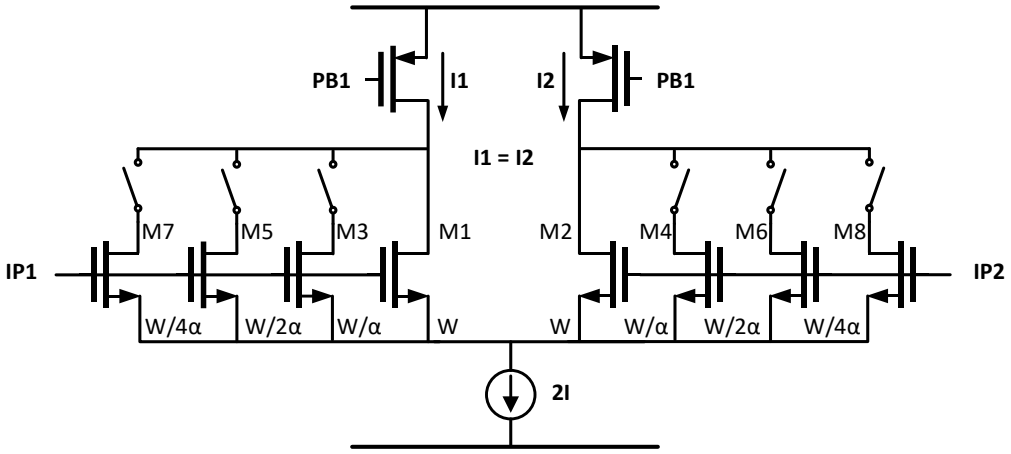


Fig. 3-10: Reconfigurable differential pair (RDP)

The RDP consists of two equal PMOS current sources, while the NMOS differential pair has multiple fingers attached in parallel with the main differential pair via switches. While the main differential pair has a width of W, the next element in the differential pair is 'α' times smaller. As the number of fingers increases, so does the resolution of the trim. Based on the polarity and amount of offset, the switches in the RDP are activated. Since this technique compensates the offset by modifying the width of the differential pair, its offset cancellation is temperature-dependent. Hence, it is critical to ensure that the resultant spread of residual offset over temperature is within the error budget.

Considering the area requirements and the error budget specifications, reconfigurable differential pair (RDP) is preferred over the bandgap trimming technique.

However, in the present op-amp configuration, it is difficult to assess the impact of the offset cancellation circuit. Thus, a modification to the op-amp structure is required to observe the op-amp offset and the efficacy of the offset cancellation circuit, which is introduced in the next section.

3.2.4 Alternating op-amp operation

In a reconfigurable differential pair, the width of one side of the input pair is changed to compensate for the threshold voltage and current-factor mismatch based on the polarity of the offset. However, the polarity of the offset, as well as the extent of trimming required, cannot be assessed if the op-amp is in the closed-loop configuration. Hence a modified sensor core structure is proposed in Fig. 3-11.

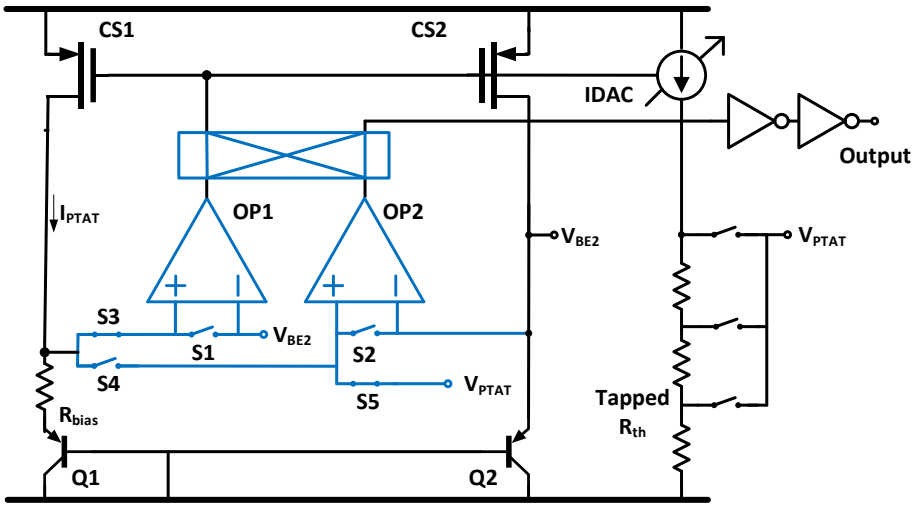


Fig. 3-11:Alternating op-amp operation

In the new sensor core design, op-amp1(OP1) functions as a bias voltage generator for the current sources, CS1-2, while the op-amp2 (OP2) functions as a comparator, with its inputs connected to V_{PTAT} and V_{BE2}, and its output is connected to the digital buffer. Switches S1-5 are used to change the configuration of the op-amps. S1-5 in conjunction with the switches connected at the output of the op-amps enable the swapping of functionalities of the op-amps.

The normal operation is the one described above. However, when the op-amp is connected in the open-loop configuration, the op-amp acts as a comparator and gives a digital high or low based on the polarity of the offset. To ensure that the offset becomes the input signal, the inputs of the op-amp are shorted, using switches, S1 and S2. At the same time, the common-mode input of the op-amp is maintained by connecting its inputs to V_{BE2}. However, when op-amp-1 is in the open-loop configuration, it can't be used to bias the CS. Hence, in that configuration, OP2 is used to bias the CS. While in the open-loop configuration, the offset of OP1 is trimmed using the RDP until the output of OP1 flips from digital one to digital zero or vice versa. In this fashion, the polarity of the offset and efficacy of the trimming circuit can be observed. Once the offset of OP1 is trimmed, OP1 goes back in closed-loop configuration and OP2 is switched into the open-loop configuration for offset cancellation.

The offset of the op-amps is trimmed in two phases. The offset of OP1 is trimmed in phase-1, while the offset of OP2 is trimmed in phase-2. The configuration of the switches S1-5 in both phases of operation is shown in Fig. 3-12

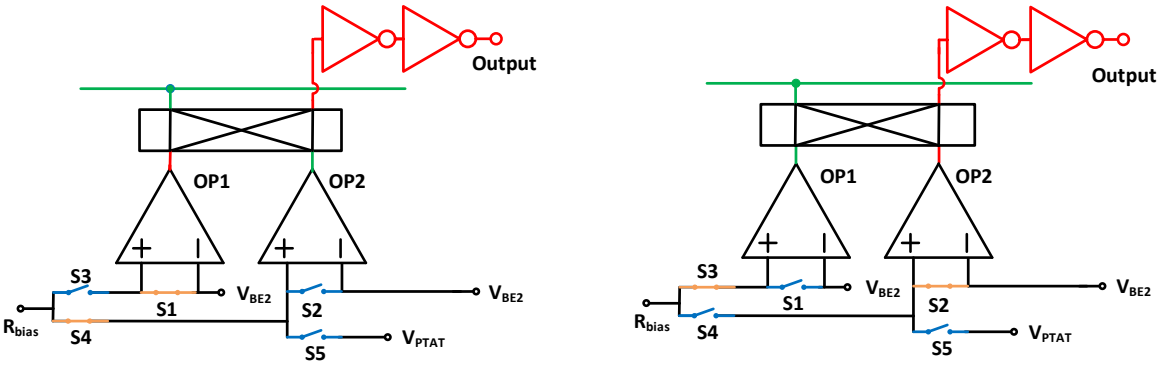


Fig. 3-12: Phase-1 and Phase-2 of op-amp offset trimming

Now that the system-level design of the sensor core is explained, the next section will shed light on the realisation of the programmable temperature threshold.

3.3 Programmable temperature threshold

In this design, the threshold is set using V_{BE} and V_{PTAT}. However, both V_{BE} and V_{PTAT} can be made programmable. In this section, the choice of a programmable threshold generation block is discussed followed by some points regarding its implementation.

3.3.1 Choice of the threshold parameter

Based on the system specifications, the programmable temperature threshold range is from -40°C to 150°C. Over this range, the V_{BE} changes from 800 mV to 400mV, which defines the voltage range over which the comparison has to be made.

As discussed in section 2.2, if V_{BE} is used as the basis of the programmable threshold, the adjustability of its slope is a concern, given the wide temperature range. Since the relation between V_{BE} and emitter current is logarithmic, exponential current changes are then required to get significant changes in V_{BE}. For the given temperature range, this implies that the current must change from femto-amperes to microamperes (10^{-15} – 10^{-6} A) which is a huge current range to realize. However, in the case of V_{PTAT}, adjustability of its slope is simpler as compared to V_{BE}. V_{PTAT} can change by several hundred millivolts by adjusting either the current (I_{PTAT}) or the resistance (R_{th}).

Based on the ease of adjustability, V_{PTAT} is chosen as the programmable threshold. The architectures to implement the V_{PTAT} programmability are discussed in the following sub-section.

3.3.2 Programmability of V_{PTAT}

V_{PTAT} can be programmed by either varying the current (I_{PTAT}) passing through R_{th} or by changing the resistor R_{th} itself. The possible alternatives to change the current and the resistance are shown in Fig. 3-13

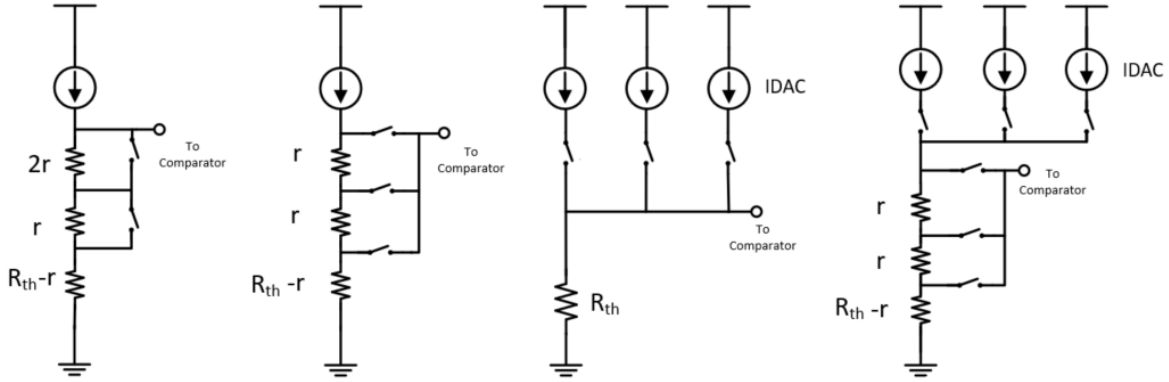


Figure 3-13: Architectures for programming V_{PTAT}

The Fig. 3-13(a) shows as binary resistive-DAC with a fixed current source and switches connecting the resistor nodes to the comparator. The tapped resistor is shown in Fig. 3-13(b) has a fixed current source and a unary resistor ladder where the taps are connected to the comparator using switches. The current DAC showed in Fig. 3-13(c) has a fixed resistor and the current through it is varied to get the desired voltage, which is then connected to the comparator. The last image in Fig. 3-13(d) is that of the segmented DAC, which is a combination of the I-DAC and the tapped resistor. The I-DAC varies the current through a unary tapped structure, where the taps are connected to the comparator.

Assuming that the current through the resistor is a few µA, the R-DAC will require resistors of hundreds of kΩ to cover the voltage range of V_{BE}. This will require a large area. Furthermore, the switches in the R-DAC will appear in parallel with the resistors when they are closed and result in a voltage error.

The error due to finite on-resistance is eradicated in the tapped resistor ladder. Since the switches connect the resistor to the input of the comparator, no current is drawn through them. However, because of the unary nature of the resistor structure, a large number of taps are required to cover the entire voltage range of V_{BE} resulting in a large area as well as high complexity.

While the required voltage range is easily achieved, the I-DAC has to trade-off resolution for the area. This is because high resolution requires small currents which in turn requires long length PMOS transistors, assuming minimum width and fixed overdrive voltage is used. Furthermore, the leakage current from the switches in their off condition is another point of concern in the I-DAC. To minimize the impact of leakage current, long length switches are required, which cost area. Hence, because of the area requirements for a high-resolution configuration, the I-DAC is not preferred.

The problem of area requirement vs resolution in an I-DAC can be tackled by using a segmented DAC. It uses a combination of the I-DAC and the tapped resistor ladder and thus can achieve a large voltage range without high area while achieving a high resolution using the tapped resistor structure. Though, like the I-DAC, the leakage current is an issue here as well.

Based on the available options, the segmented DAC is the best choice to achieve the desired goal of high voltage range, high resolution and limited area consumption.

3.3.3 PTAT trim

As mentioned in section 2.4, the PTAT error sources result in a substantial error in the temperature threshold detection. The saturation current spread of the substrate BJTs results into a variation of 32mV in the V_{BE} over corners and mismatch which translates into a temperature error of up to 10°C around 150°C. To eliminate these errors, a PTAT trim is required. The PTAT trim is performed at room temperature (27 °C) and its efficacy has to be assessed at the extreme operating temperature (-40°C and 150°C). An error budget of 0.4ºC is allocated for the residual PTAT trim error. This implies an error voltage of 2.07mV at -40°C and 1.15mV at 150°C. Based on these values, the circuit level implementation of the segmented DAC is proposed in the next section.

As suggested in [30], trimming should be done such that all the PTAT error sources can be corrected simultaneously. The three available choices for implementing a PTAT trim are R_{bias}, the tapped-R_{th} and the I-DAC. However, it can be seen that trimming R_{bias} changes the current flowing into PNP and R_{th} simultaneously resulting in a different temperature threshold while correcting for the saturation current spread. Therefore, modifying R_{bias} is not an effective solution. Another alternative is to trim V_{PTAT}. This can be done by changing the resistance of R_{th} and/or the current from the I-DAC. Since the segmented DAC is already being utilised to change V_{PTAT} for setting different temperature thresholds, its use for performing a PTAT trim simplifies the design. However, care has to be taken while integrating the PTAT trim setting with the setting for different temperature thresholds.

3.4 System-level design

The design proposition is shown in Fig.3-14, and is summarized below

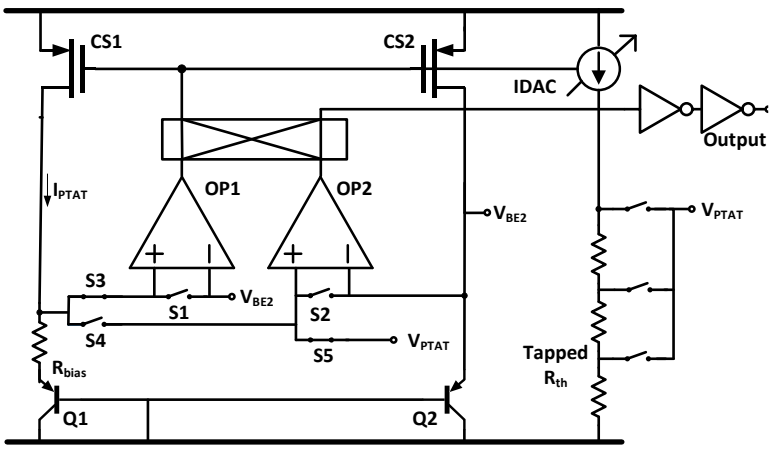


Fig. 3-14: System-level design

1. The BJT current density ratio of 1:20 is chosen for ΔV_{BE} generation. The intention is to maximise ΔV_{BE} so that less amplification is required. This will reduce the impact of the op-amp offset on the V_{PTAT}. The trade-off between current density ratio and error sources like op-amp offset, spread in current gain and the series BJT resistance are considered while making the choice.

2. A folded cascode op-amp with PMOS input stage is chosen. The op-amp has an input common-mode voltage of 0.4V-0.8V, a common-mode output voltage of 1.15V with a ±0.23V swing and a gain of 80dB.
3. A temperature-dependent offset cancellation scheme of the reconfigurable differential amplifier is chosen to reduce the offset. This scheme is advantageous because of its simplicity and low area requirement. However, the PTAT spread of the residual offset over temperature is a concern and must be kept within the error budget.
4. Since the output of the op-amp biases the PNP which is used to generate the common-mode input voltage, another identical op-amp is required to bias the network when the first op-amp is undergoing offset trimming. While the offset of the second op-amp is being trimmed, the first op-amp is used to bias the network. This alternating operation of the op-amp is required only during the offset trimming phase.
5. After the trimming phase, the second op-amp is used as a comparator to detect the threshold using V_{PTAT} and V_{BE} as its inputs.
6. The programmability of the threshold is implemented by using a segmented DAC which consists of an I-DAC and a tapped resistor. The I-DAC provides the ability to generate the required voltage range and the tapped resistor provides the resolution without the error associated with the on-resistances of the switches.
7. The same I-DAC and tapped resistance will be used to trim out PTAT errors. The trimming configuration is then integrated with the temperature setting configuration to provide a PTAT spread compensated temperature setting code.
8. The various error sources and their mitigation techniques have been listed

Error	Nature	Cancellation technique	Error budget
Saturation current spread	PTAT	PTAT trim using the segmented DAC	0.4°C
Resistor mismatch	PTAT		
BJT Series resistance	PTAT		
Current source mismatch	Non-PTAT		
Current gain spread	Non-PTAT		
Op-amp offset	Non-PTAT	Sizing and RDP	0.5°C
Comparator offset	Non-PTAT		0.1°C

Chapter 4 Circuit Implementation

This chapter discusses the circuit implementation of the various blocks of the proposed temperature switch. It is implemented in a 160nm CMOS process. First, the realization of the intended 1:20 current density ratio (CDR) is discussed, followed by the design of the op-amp, offset cancellation circuit, biasing circuit and start-up circuit. Furthermore, the implementation of the segmented DAC comprising of the IDAC and the tapped resistor ladder is also discussed.

4.1 Implementation of the CDR

As mentioned in section 3.1, a CDR of 1:20 is chosen between the two BJTs, Q1 and Q2. However, this can be implemented in a number of different ways by varying the current ratio (1:M) or the BJT emitter area ratio (N:1) used in the two branches. The 6 possible configurations are listed in Table 4-1, while the circuit is shown in Fig. 4-1

Table 4-1: Configurations to realize CDR of 1:20

Sr.No.	CDR	BJT emitter area ratio (N)	Current ratio (M)
1.	1:20	1:1	20:1
2.		1:2	10:1
3.		1:4	5:1
4.		1:5	4:1
5.		1:10	2:1
6.		1:20	1:1

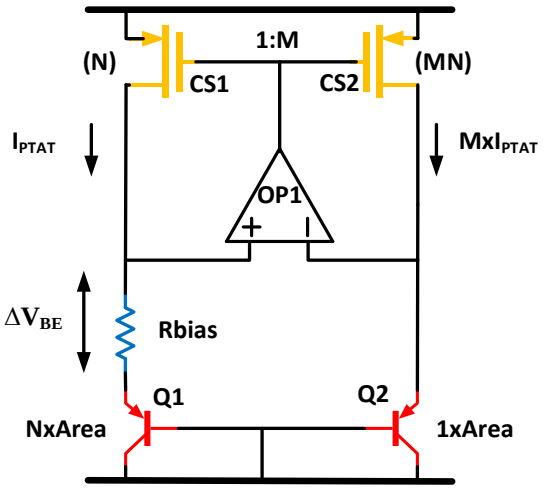


Fig. 4-1:Sensor core with a CDR of 1:20

To realize the various configurations listed in Table 4-1, the emitter area ratio is varied by changing the emitter area of Q1, while the current ratio is varied by increasing the current through CS2. If the emitter area of Q1 has increased to 'N' times the unit emitter area, then CS1 has to be increased 'N' times as well, to maintain the target current density of 100nA/unit emitter area. This implies that the current through CS2 has to be increased 'MN' times to realize a current ratio of 1:M between Q1 and Q2. In this process, the overall area of the circuit increases. Fig. 4-2 shows the estimated area occupied by the PNP transistors, R_{bias} and the current sources in various configurations.

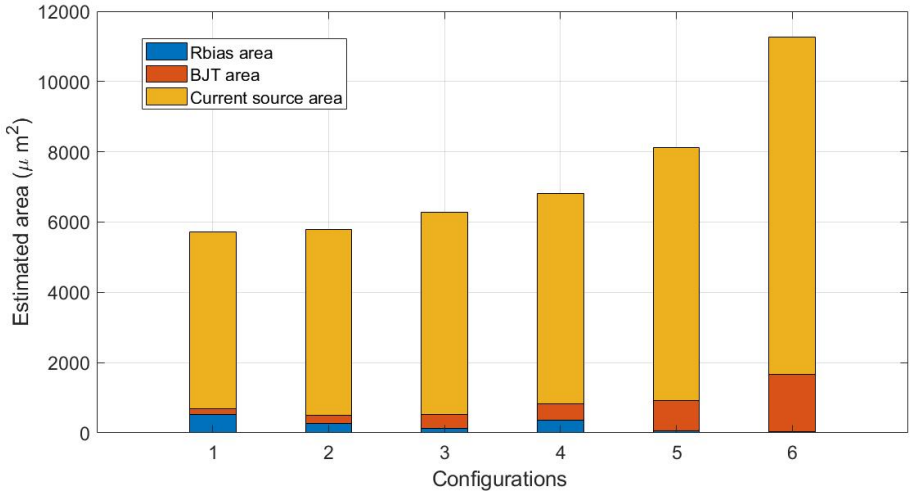


Fig. 4-2:Estimated area of each configuration to realize 1:20 CDR

It can be seen that as the BJT emitter area ratio increases, the total area also increases. As the area increases, the mismatch between the current sources and emitter areas in the two branches decreases [31], resulting in less error in ΔV_{BE}, as shown in Fig. 4-3.

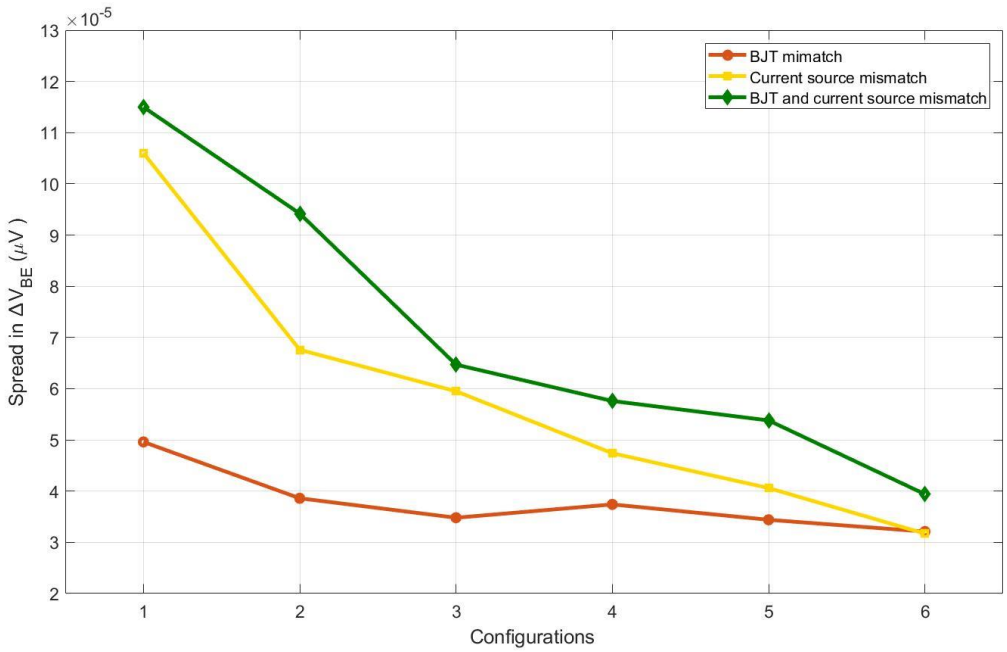


Fig. 4-3: Spread in ΔV_{BE} due to mismatch in various configurations

Each line represents the spread in ΔV_{BE} due to various sources of mismatch while the rest of the circuit is assumed to be ideal.

Since the primary intended application of the temperature switch is to detect the overheating of microprocessors, the impact of mismatch is investigated at high temperatures ($T \approx 150°C$). Using the amplification factor and sensitivity at 150°C (see section 3.1.5), errors due to mismatch can be converted to temperature errors. Fig. 4-4 compares the temperature error due to mismatch and the estimated area for each configuration.

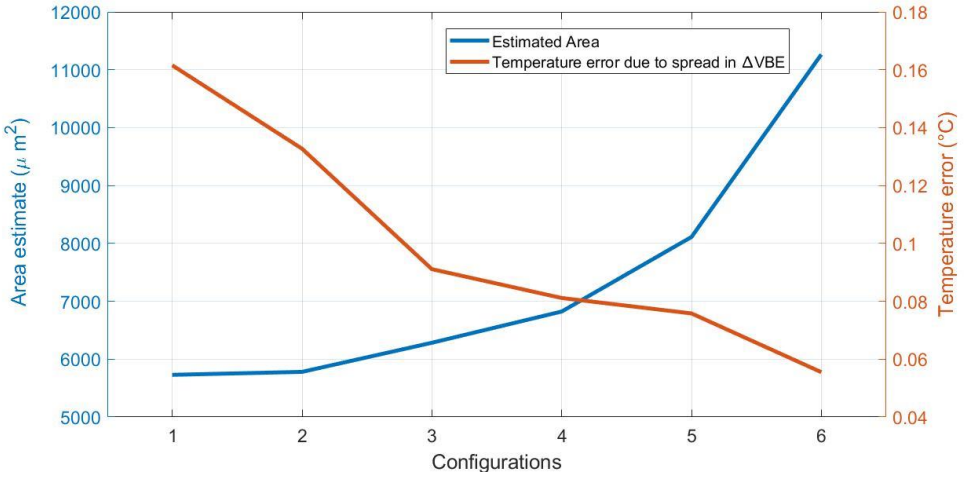


Fig. 4-4: Temperature error due to mismatch vs Area estimate of each configuration

The two lines indicate the temperature error and area for the different configurations shown in Fig. 4-2 and Fig. 4-3. The error due to the mismatch has to be kept below 0.1°C, while area should be minimized. Based on these requirements, configuration 3 was chosen for implementation, i.e. a 1:4 BJT emitter area ratio and a 5:1 current ratio. The circuit is shown in Fig. 4-5 while the device sizes are presented in Table 4-2.

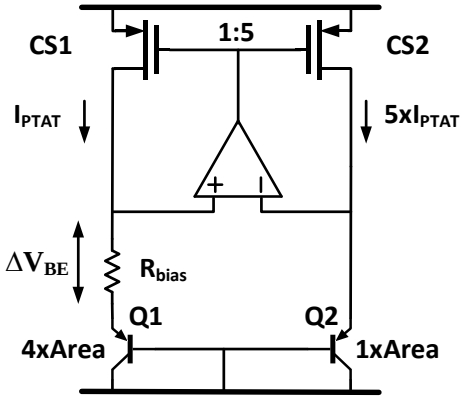


Fig. 4-5: Sensor core

Table 4-2: Details about the sensor core

Name	M	W(µm)	L(µm)	Name	M	W(µm)	L(µm)
CS1	12	0.768	30	Q1	4	5	5
CS2	60	0.768	30	Q2	1	5	5
Current	**I (µA)**		**Current**	**I (µA)**		**Resistor**	**R (kΩ)**
I_{PTAT}	0.4		5x I_{PTAT}	2		R_{bias}	193.97

4.2 Op-amp design

In section 3.2, the specifications of the op-amp were discussed. The two primary specifications are its DC gain and offset.

4.2.1 DC gain

Op-amp gain mainly depends on the trans-conductance of the input differential pair and the output impedance of the transistors in the folded cascode branch. As temperature increases the

output impedance decreases, resulting in a lower gain of the amplifier. To ensure that the DC gain remains above 80dB for all temperatures and corners, a DC gain of 93dB at 27 °C was found to be sufficient.

4.2.2 Op-amp offset

The choice of reconfigurable differential pair (RDP) to cancel the offset, results in a residual offset drift over temperature, as discussed in section 3.2.3 After trimming, this should be less than 260uV at -40°C and 460uV at 150°C to meet the error budget. This puts certain requirements on the *untrimmed* offset, which must also be examined. To establish these requirements an understanding of the nature of offset and the temperature-associated-spread is required.

Based on simulations, ~70% of the op-amp offset was due to the threshold voltage mismatch while the remaining 30% was from the current-factor mismatch. While these statistics help in understanding the nature of offset, Eq.3.3 helps in calculating the temperature-dependent spread of the residual offset. The temperature-dependent spread in the offset is due to the (I/g_m) term, which is a PTAT quantity. By setting the non-ideality factor 'n' equal to 1.5, (I/g_m) can be calculated.

The residual offset (V_{res}) generated after the offset is trimmed by the RDP is given by

$$V_{res} = \Delta V_{th} + \left(\frac{I}{gm}\right)\frac{\Delta\beta}{\beta} - \left(\frac{I}{gm}\right)\frac{\Delta W_{RDP}}{W} \qquad 4.1$$

Where '$\Delta W_{RDP}/W$' is the modified width due to trimming, 'I' is the current through the transistor and 'g_m' is the trans-conductance of the differential pair. The residual offset at -40°C and 150°C after an offset cancelling trim is done at 27°C, is shown in Fig. 4-6

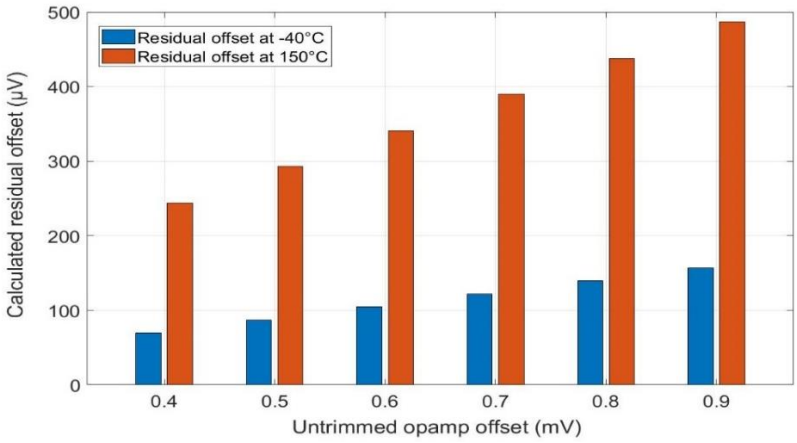


Fig. 4-6: Calculated residual offset drift for different untrimmed offsets

Based on Fig. 4-6, it can be seen that offsets less than 800uV are enough to satisfy the conditions related to the drift of the residual offset, however, to maintain a safety margin, an untrimmed offset of 700uV is chosen for realization.

To attain such a low offset, the offset from all the three sources in the folded cascode topology namely, the input pair (FP3, FP4), the current sources (FP5, FP6) and the current sink (FN3, FN4), has to be addressed. The offset voltage from the afore-mentioned sources is shown in Fig. 4-7.

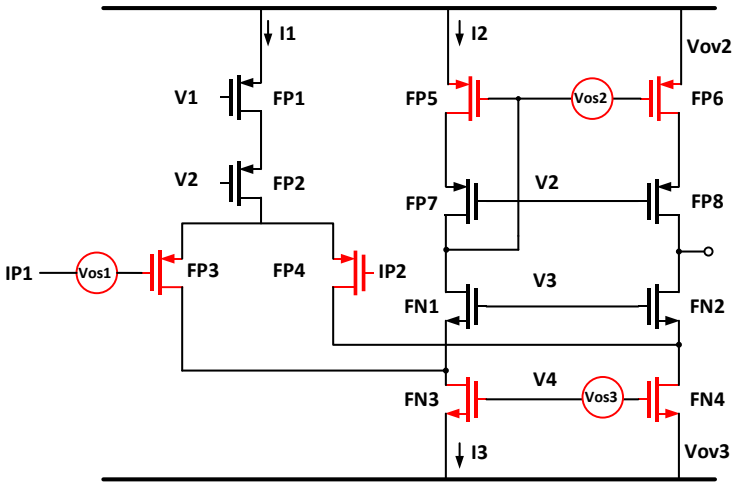


Fig. 4-7: Design details of the op-amp and sources of offset

The offset contributed by the input pair is V_{os1}, from the current sources is V_{os2} and from the current sink is V_{os3}. The expression for the input-referred offset voltage[26] is given by Eq. 4.2

$$\sigma^2(V_{os}) \approx \sum_{i=1}^{3}\left(\frac{g_{m\,i}}{g_{m\,1}}\right)^2 \sigma^2(V_{osi}) \qquad 4.2$$

Where g_{m1} is the trans-conductance of the input pair and 'i' indicates the three locations of offset generation.

Based on the expression, an increase in the input pair's trans-conductance reduces the offset. Another inference is that the trans-conductance of the other two offset sources, FP5-6 and FN3-4, should be as low as possible. Hence, they are biased in strong inversion. Since the current from the input pair and the current sources flow into the current sink (FN3-4), the trans-conductance of the current sink has to be even lower compared to the current source to reduce the offset. Thus, an overdrive (V_{ov2}) of 300mV is used to bias the current source, while the current sink is biased using an overdrive (V_{ov3}) of 400mV.

Thus, using transistor sizing and overdrive voltage management, an offset of 700uV is realized. The dimensions of the devices used in the op-amp are shown in Fig. 4-8 and Table 4-3

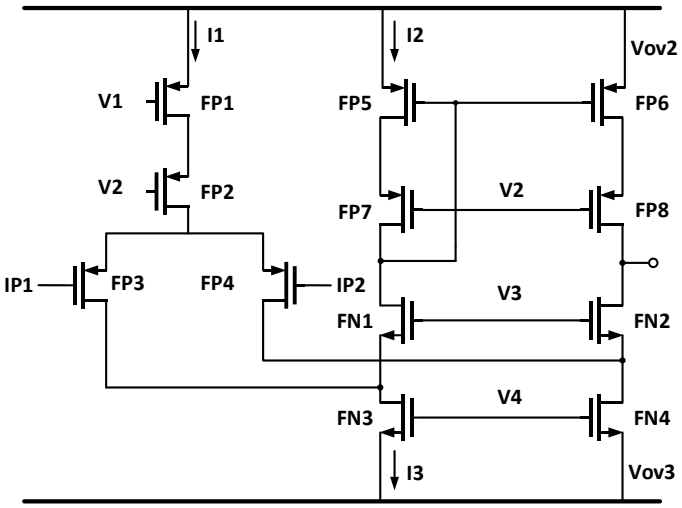


Fig. 4-8: Folded cascode amplifier

Table 4-3: Design details of the op-amp

Name	M	W (µm)	L (µm)	Name	M	W (µm)	L (µm)
FP1	1	0.768	30	FP7, FP8	4	4	4
FP2	1	4	4	FN1, FN2	4	4	4
FP3, FP4	12	12	6	FN3, FN4	1	0.768	120
FP5, FP6	2	0.768	60				
Current	**I (nA)**		**Current**	**I (nA)**		**Current**	**I (nA)**
I1	99		I2	33		I3	82.5
Voltage	**V**	**Voltage**	**V**	**Voltage**	**V**	**Voltage**	**V**
V1	1.05	V2	0.95	V3	0.83	V4	0.73

4.3 Op-amp offset cancellation circuit

The RDP uses multiple fingers of different widths to trim the op-amp offset. However, the minimum width of the fingers is limited by the design-for-manufacturability rules (DFM), thus, for higher resolution, the length of the fingers is increased. However, this also increases the area. Based on these concerns, a resolution of 30uV was chosen to trim the 700µV offset. This results in a 6-bit trimming network for the offset.

In [26], [27], the RDP had trimming fingers on both sides of the differential pair. To save area in the implemented design, only one set of fingers (RDP0-5) are implemented. Depending on the offset polarity, these can then be connected to either side of the input differential pair by means of switches (S6-7). The offset cancellation circuit is shown in Fig. 4-9 while its details are presented in Table 4-4. The efficacy of the offset cancellation circuit is presented in the next chapter.

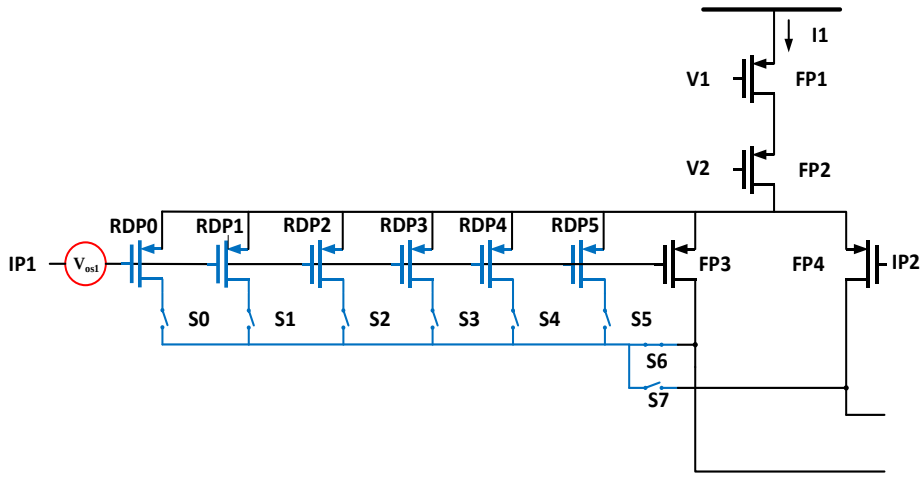


Fig. 4-9: Reconfigurable differential pair connected to the folded cascode

Table 4-4: Details of the RDP implementation

Name	M	W(µm)	L(µm)	Name	M	W(µm)	L(µm)
RDP0	1	0.768	48	RDP4	2	0.768	6
RDP1	1	0.768	24	RDP5	4	0.768	6
RDP2	1	0.768	12	S1-7	1	0.768	2
RDP3	1	0.768	6				

The RDP fingers, RDP0-6, are connected to one end of the differential inputs of the op-amp. However, based on the polarity of offset, the current through the fingers can be channeled to the drain terminal of either FP3 or FP4, based on the position of switch S6-7.

4.4 Biasing Circuit for the op-amp

This design uses a constant-g_m biasing circuit. In literature [1], [32], [33], such circuits require a resistor (which generates I_{PTAT}) and MOSFET-based feedback loops (to regulate I_{PTAT}). However, they suffer from a trade-off between area and power. Low biasing currents require large resistors, which increases circuit area. Since this design requires biasing current in the range of tens of nano-amperes, the resulting resistor will be in the order of hundred's of kilo ohm. Hence, instead of going for a separate biasing circuit, the current I_{PTAT} generated by the sensor core is also used to bias the op-amp. A disadvantage of this biasing scheme is that the amplifier's output is now dependent on the biasing circuit, while the biasing circuit is driven by the amplifier's output, thus creating a loop. To ensure that the circuit reaches the desired operating region, a start-up circuit is necessary. The bias and start-up circuits are shown in Fig. 4-10 and its details are presented in Table 4-5.

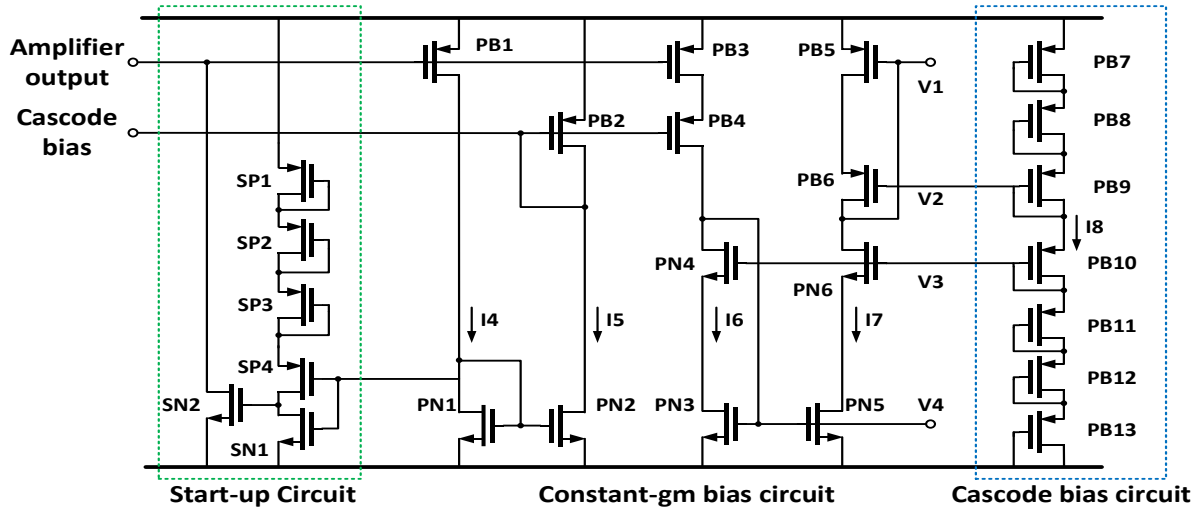


Fig. 4-10: Biasing circuit of the op-amp

Table 4-5: Component details of the biasing and start-up circuit

Name	M	W(µm)	L(µm)	Name	M	W(µm)	L(µm)
PB1	1	0.768	30	PN1, PN2	1	0.768	120
PB2	2	0.768	150	PN3, PN5	1	0.768	150
PB3	2	0.768	30	PB7-13	1	0.768	0.16
PB4	2	0.768	0.8	SP1-4	1	0.768	1
PB5	1	0.768	30	SN1	1	0.768	1
PB6	1	4	2	Sn2	1	0.768	4
Name	**I (nA)**		**Name**	**I (nA)**		**Name**	**I (nA)**
I4-5	33		I6-7	66		I8	30

The circuit shown in Fig. 4-10 consists of a startup circuit, a constant-g_m bias generator and a cascode bias generator. The startup circuit senses the voltage developed over the NMOS-diode, PN1, and if this is less than 0.3V, pulls down the amplifier output. The output of the op-amp is mirrored into a 'high swing' cascode biasing circuit [32]. The current source (FP5-6) and the sink (FN3-4) of the op-amp are biased using these constant-gm biasing voltages (V1 and V4). Since the cure of current mirror to generate the biasing for the cascodes will result in additi onal branches, to conserve area, a diode-connected PMOS chain is used to generate the bias voltages for the cascodes (V2 and V3) from a single branch. The detailed dimensions of the biasing network are provided in Table 4-5

4.5 Alternating op-amp operation

As discussed in section 3.2.4, the two op-amps used in this design are trimmed by alternating their position in the circuit. The switches (S1-5) used to do this are minimum sized (W = 0.768um L = 0.16um) since their on-resistance does not result in any error, as they are in series with the high impedance inputs of the op-amp.

The configuration of the switching circuit at the outputs of the op-amps is shown in Fig. 4-11. These also employ minimum-size switches.

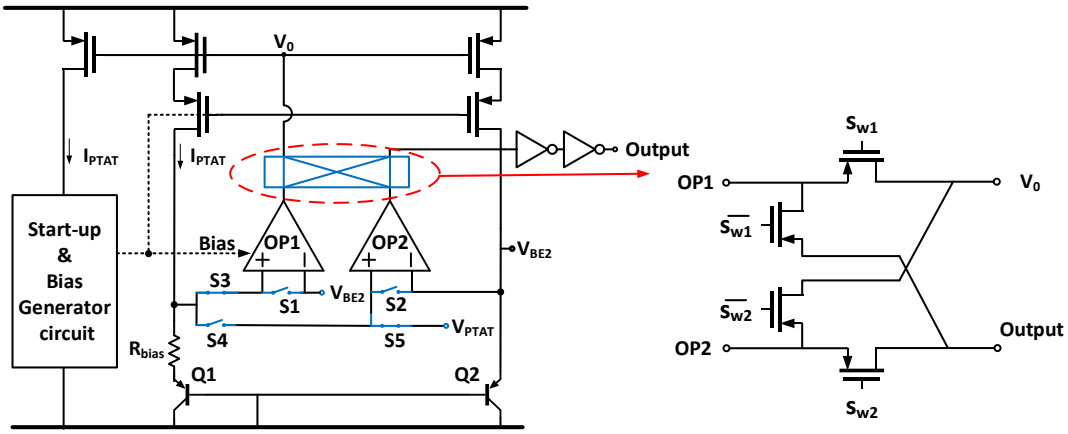


Fig. 4-11: Switching circuit at the outputs of the op-amps

The outputs of the op-amps, OP1 and OP2, are connected to the bias generation circuit, V_0, or the digital buffer, output, via switches S_{w1} and S_{w2}, respectively. However, during the offset cancellation phase of OP1, the switches connect the output of OP1 to the digital buffer while OP2 biases the circuit and vice-versa.

4.6 Segmented DAC

The segmented DAC is used to adjust the temperature threshold and to trim out PTAT errors. The voltage range of V_{BE} over the operating temperature range and corners is 400mV to 800mV as shown in Fig. 4-12.

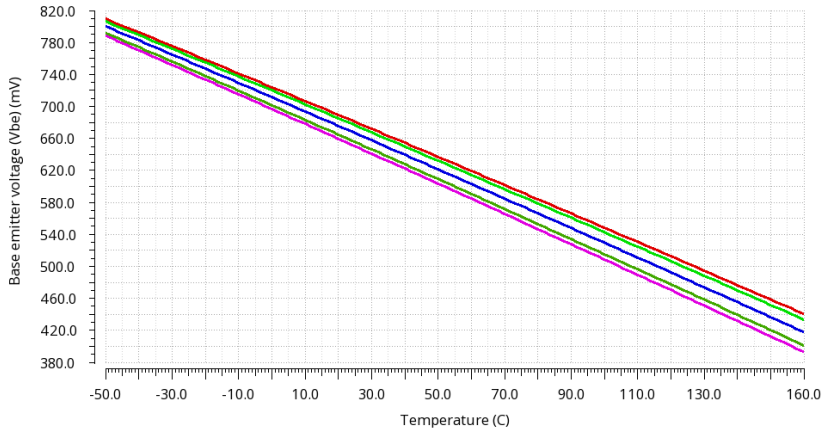


Fig. 4-12: Change in V_{BE} over corners and the operating temperature range.

At room temperature (27ºC) V_{BE2} spreads by 32mV due to the spread in the PNP's saturation current, which is trimmed out using the segmented DAC. The trimming resolution, k, is defined by the required correction accuracy of PTAT error, V_{LSB}, and the spread in V_{BE} due to various PTAT error sources, V_{spread}. The resolution [18] is given by Eq. 4.3

$$k - 1 = \frac{ln\left(\frac{V_{spread}}{V_{LSB}}\right)}{ln2} \tag{4.3}$$

To get a trimming accuracy of ±0.3 °C from -40°C to 150°C, an LSB voltage V_{LSB} of 0.200mV is required, which translates into 9-bit resolution. In the segmented DAC, this is obtained with

a 7-bit current DAC and a 2-bit tapped resistor ladder. The implementation of the IDAC and the tapped resistor is discussed in the following sub-sections

4.6.1 Current DAC(IDAC)

The 7-bit IDAC is used to perform a coarse-PTAT trim. It is also used to set the temperature threshold and to cover a voltage range of 0.4V to 0.8V. To realize this voltage-range a binary IDAC is chosen. The choice of currents depends on the R_{th} and leakage current. If a low current is used, a large R_{th} will be required to generate the required voltage range, while a large current will result in higher leakage current at 150°C. Based on these trade-offs, a current of 2.14µA was chosen to set the temperature threshold at 150°C. This implied a current of 6.95µA is required to generate the -40°C temperature threshold, for the same R_{th}. Based on these requirements, a binary IDAC with an I_{LSB} of 33nA and I_{MSB} of 4.28µA was designed.

The dimensions of the current source (CS2-10), in the IDAC, have been chosen such that it remains in strong inversion to minimize mismatch [21]. Cascodes (C3-10) are used to increase the output impedance of the current sources and thus reduce their susceptibility to the changes in the drain-source voltage. To reduce area, the cascodes of minimum size are used. The IDAC is shown in Fig. 4-13 while its dimensions are presented in Table 4-6

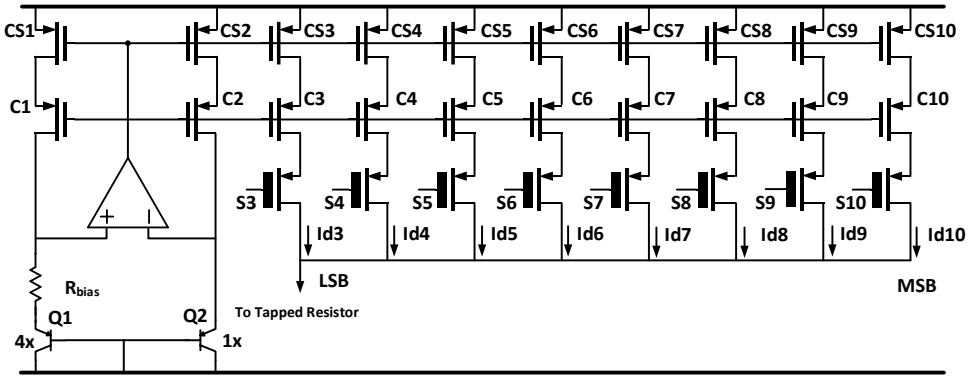


Fig. 4-13: The design for the current DAC

Table 4-6: Components details of the IDAC

Name	M	W (µm)	L (µm)	Name	M	W (µm)	L (µm)	Name	M	W (µm)	L (µm)
CS3	1	0.768	30	C3	1	0.768	0.16	S3	1	0.768	20
CS4	2	0.768	30	C4	2	0.768	0.16	S4	2	0.768	20
CS5	4	0.768	30	C5	4	0.768	0.16	S5	4	0.768	20
CS6	8	0.768	30	C6	8	0.768	0.16	S6	8	0.768	20
CS7	16	0.768	30	C7	16	0.768	0.16	S7	16	0.768	20
CS8	32	0.768	30	C8	32	0.768	0.16	S8	32	0.768	20
CS9	64	0.768	30	C9	64	0.768	0.16	S9	64	0.768	20
CS10	128	0.768	30	C10	128	0.768	0.16	S10	128	0.768	20
Current	**I (nA)**		**Current**	**I (nA)**		**Current**	**I (µA)**		**Current**	**I (µA)**	
Id3	33		Id5	125		Id7	0.5		Id9	2.14	
Id4	66		Id6	250		Id8	1.07		Id10	4.28	

As mentioned earlier, the leakage current from the IDAC can cause a high inaccuracy at 150°C. This leakage current is the subthreshold leakage [33] of the switches when they are turned 'OFF' and is given by Eq 4.4

$$I_{leak} = \left\{\mu C_{ox}\left(\frac{W}{L}\right)(m-1)\left(V_t{}^2\right)\right\} \times \left\{e^{(V_g - V_{th})/mV_t}\right\} \times (1 - e^{V_{ds}/V_t}) \qquad 4.4$$

Where 'm' is the body effect coefficient, 'V_t' is the thermal voltage, 'V_g' is the gate voltage, 'V_{th}' is the threshold voltage and 'V_{ds}' is the drain to source voltage. The impact of this subthreshold leakage can be reduced, by increasing the length and/or increasing the threshold voltage of the switches.

If the length is increased, the impact of V_{ds} on the leakage current decreases. While a higher threshold voltage exponentially reduces the leakage current. However, V_{th} can be increased by opting for a different transistor with a high threshold voltage. A comparison of the different transistor flavours and their threshold voltages is shown in Table 4-7.

Table 4-7: Threshold voltages of different PMOS flavours

Sr. No.	PMOS flavours in 160 nm technology	Threshold Voltage
1.	PMOS	450mV
2.	Low leakage PMOS	542mV
3.	Ultra-low leakage PMOS	622mV
4.	Thick gate oxide PMOS	690mV

While the subthreshold leakage current for these flavours is shown in Fig. 4-14.

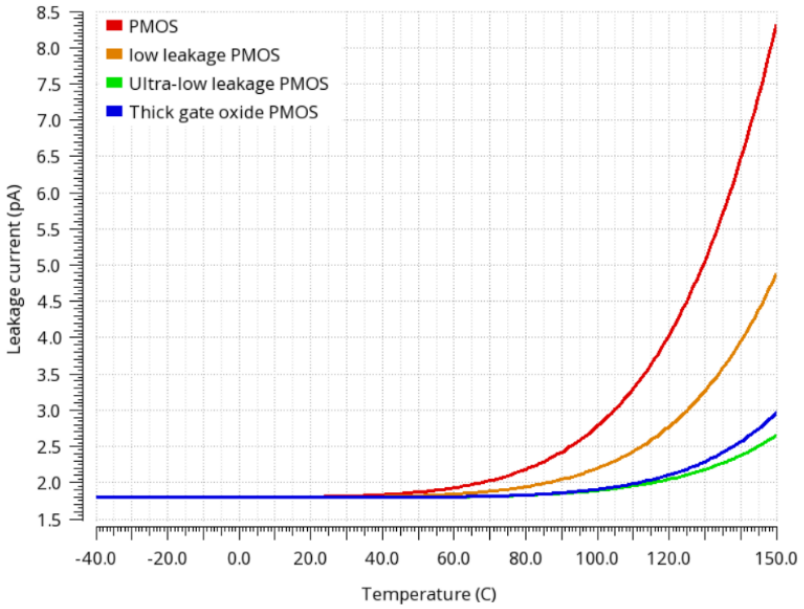


Fig. 4-14:The subthreshold Leakage current for different PMOS flavours

The best performance is observed for the Ultra-low leakage PMOS. However, a drawback of this flavour is the alteration in the normal process flow of manufacturing. Hence this flavour is not always available for utilization. The thick gate oxide is the next best option for low leakage PMOS. Since the thick gate oxide PMOS does not require process alteration, it is available in this technology. Hence, it is used to make high threshold voltage switches.

4.6.2 Tapped resistive ladder

The tapped resistive ladder is used to ensure a fine resolution in the segmented-DAC while performing a PTAT trim. To get the desired resolution of 200µV, the current supplied by the IDAC, as well as the unit element of the tapped resistive ladder, needs to be defined. Since the PTAT trim is to be performed at room temperature by changing the V_{PTAT} and equating it to V_{BE}, the current through the IDAC is chosen based on V_{BE} and R_{th}. A current of 4.49uA is chosen at room temperature to perform the PTAT trim, implying that a unit element of 80 Ω is used to get the desired resolution.

Once the configuration for the required resolution is obtained the number of taps for the structure needs to be defined. The addition of taps increases the range of voltage covered by the resistive ladder and does not affect the resolution of the device. The number of taps is chosen such that when the current through the IDAC changes by an LSB, there is sufficient overlap of the voltages generated on the taps in the two IDAC settings. 16 taps were deemed sufficient to ensure an optimum overlap between two IDAC settings. The structure for the tapped resistive ladder and the overlapping behaviour of the taps for different IDAC settings is shown in Fig. 4-15.

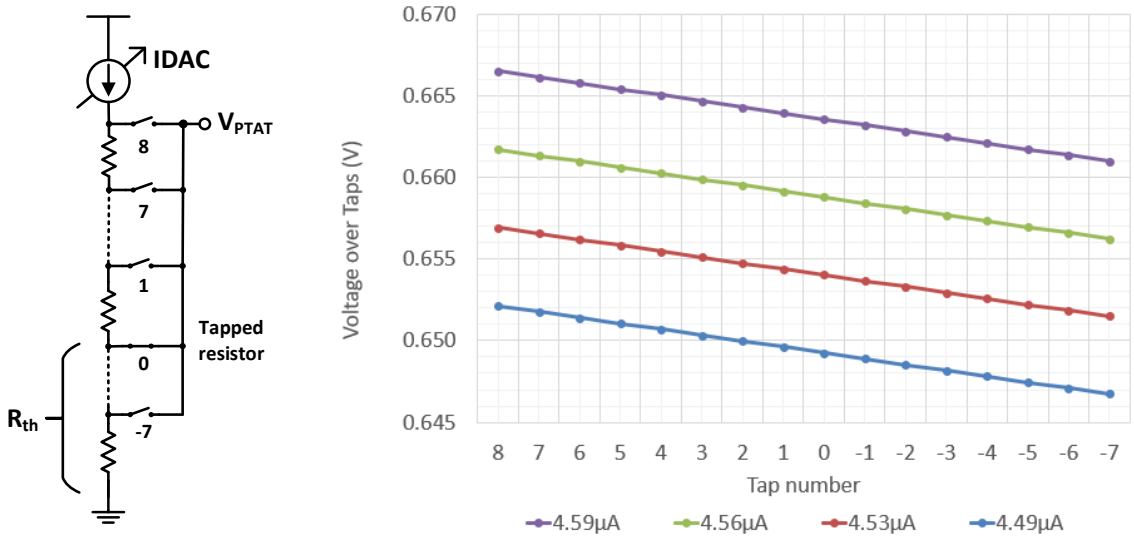


Fig. 4-15: (a)Tapped resistor structure (b) voltage developed over the 16 taps for different IDAC currents

Table 4-8: Details of the tapped resistive ladder

Name	M	W(µm)	L(µm)		Resistor	R(Ω)		Resistor	R(kΩ)
S1-31	1	0.768	0.16		R_{unit}	80		R_{th}	144.6

Fig. 4-15(b) shows the voltage behaviour of the tapped resistive ladder after adding an I_{LSB} to the current of 4.49µA. Each line represents different current setting while each point on the lines indicate the voltage developed over a particular tap.

4.7 Hysteresis circuit

At the point of temperature detection, the difference between V_{BE2} and V_{PTAT} is of the order of few micro-volts, which makes the comparator output susceptible to noise. To ensure that the presence of noise at the point of temperature detection does not affect the accuracy of the system, a hysteresis circuit is added to the system. The hysteresis circuit is shown in Fig. 4-16 (marked in blue) while its details are presented in Table 4-19

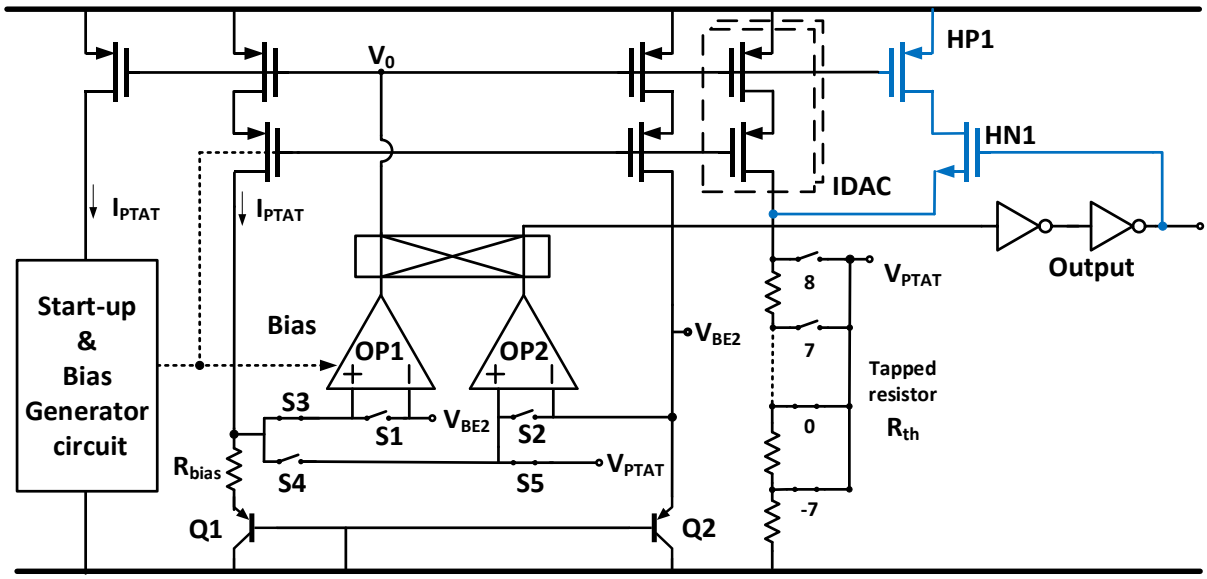


Fig. 4-16: Hysteresis circuit

Table 4-9: Details about the hysteresis circuit

Name	M	W(µm)	L(µm)		Name	M	W(µm)	L(µm)
HP1	1	0.768	120		HN1	1	0.768	2

In the circuit, the transistor HN1 operates as a switch and allows the current to from HP1 to flow in R_{th} when the comparator's output is high. This additional current helps to counteract the effect of noise during the comparison of V_{BE2} and V_{PTAT}.

4.8 Conclusion

Based on the system-level specification derived in Chapter 3, the implementation of different blocks is discussed in this chapter.

The next chapter will showcase the efficacy of this design using simulation results.

Chapter 5 Simulation Results

In this chapter, the performance of the temperature switch is evaluated with the aid of simulations. The chapter presents simulations results about the start-up behaviour of the system and the gain and phase response of the op-amps. This is followed by a simulation showing the impact of offset, before and after trimming, on temperature detection. After the op-amp offset is trimmed, PTAT error sources like the saturation current spread, resistor mismatch are trimmed and the efficacy of the system is shown. The chapter concludes with the comparison of the simulated performance of this work with the prior art.

5.1 Start-up behaviour op-amp

The sensor core uses self-biased op-amps, i.e. op-amps whose biasing voltages and currents are generated from their outputs. To prevent a potential latch-up condition when the power is turned on, a start-up circuit is used. The start-up behaviour of the circuit is observed by performing a transient analysis. Fig. 5-1 shows the start-up behaviour of the op-amp output (V0) and its biasing voltages (V1-4).

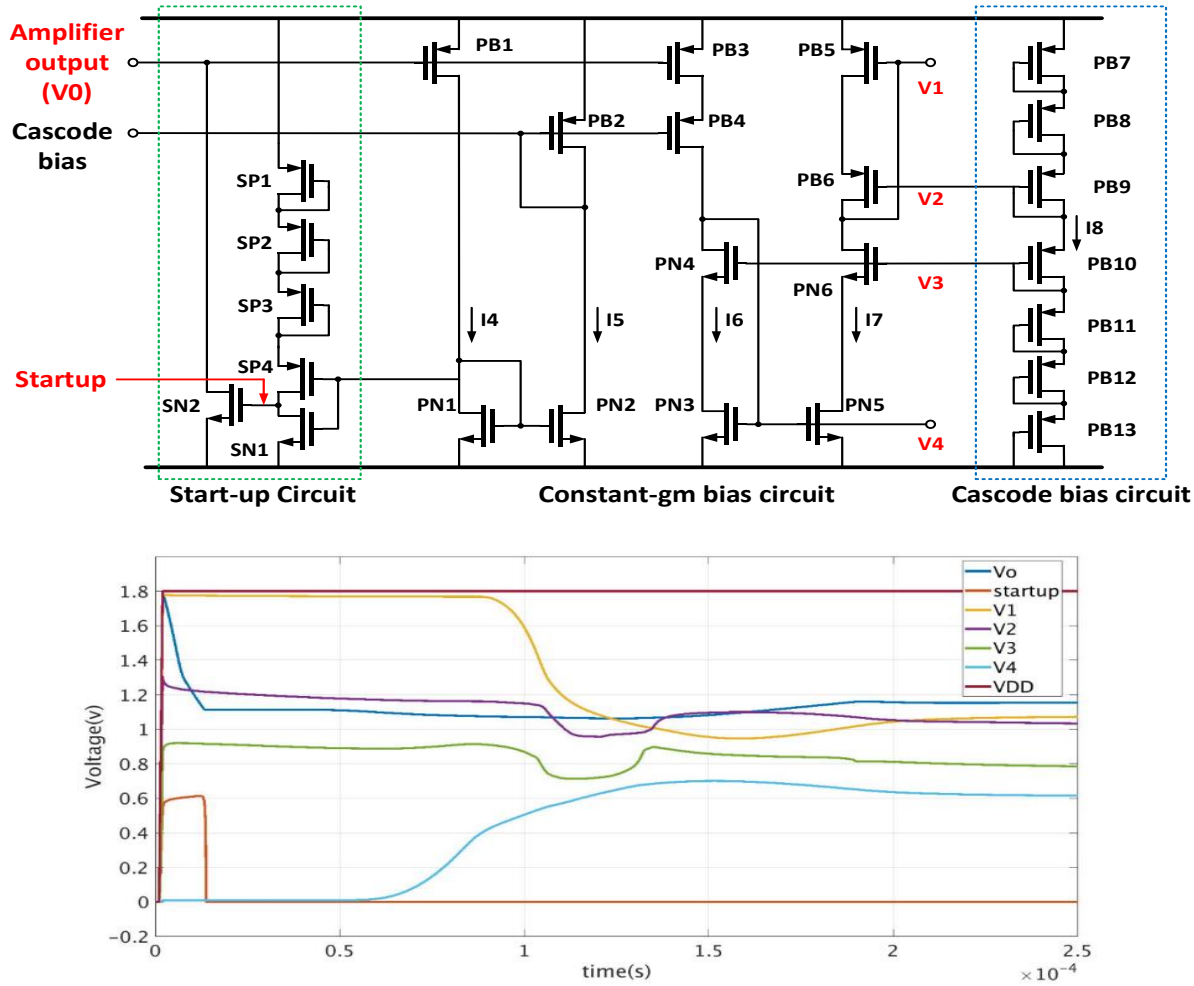


Fig. 5-1: Biasing circuit and start-up behaviour

The supply for the system was ramped up from the ground to VDD in 20ns and the response of the biasing circuit is shown in Fig. 5-1. The curves highlight the voltages used for biasing the op-amp and the output of the op-amp itself. The curves also show the behaviour of the start-up circuit when the supply is ramped. If the drain voltage on PN1 is less than 500mV, the start-

up circuit pulls the amplifier's output to ground, thus forcing current flow into the BJTs and kick starting the circuit. From Fig. 5-1, it can be seen that the output and biasing voltages of the op-amp stabilize after 200us.

5.2 Op-amp stability

Since the device has to operate at extreme temperatures, the loop-gain and phase response of the op-amp are evaluated at -40°C and 150°C to ensure the stability of the device. For the nominal corner, Fig. 5-2 shows the gain and phase response of the op-amp over three temperatures.

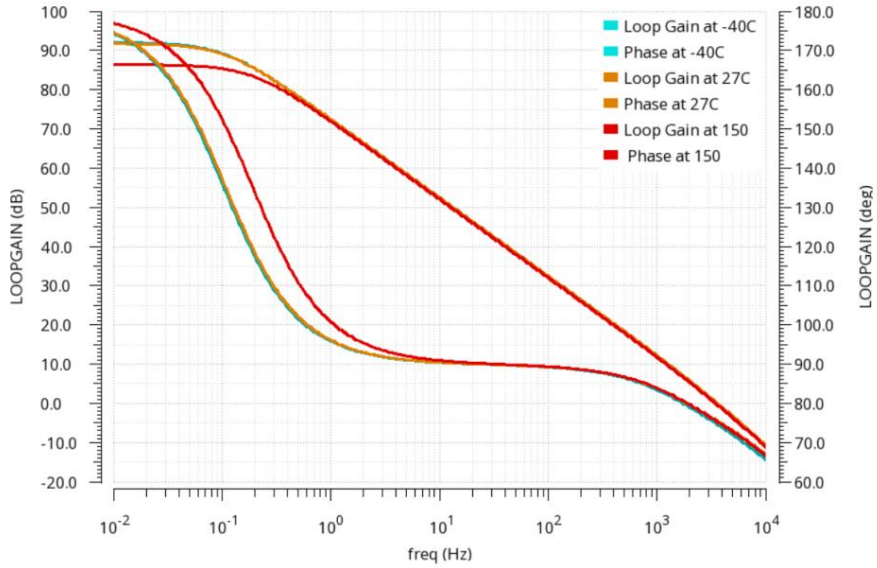


Fig. 5-2: Gain and phase response of the opamp over different temperatures.

It was seen that even in the worst-case scenario at 150°C, in the fast-corner, the op-amp has a gain of 79 dB and a phase margin of 72°, which illustrates the robustness of the design.

5.3 Offset and PTAT Trimming

In section 4.3 and 4.6, trimming techniques were proposed for mitigating the effect of offset and PTAT errors due to saturation current spread, resistor mismatch etc. This section discusses the impact of these error sources on the temperature threshold detection and also the efficacy of the trimming circuits used to mitigate these errors. The trimming process begins by correcting the non-PTAT error sources (op-amp and comparator offset) since these errors will limit the accuracy of the PTAT trim.

5.3.1 System performance in the presence of offset

As discussed in section 4.3, the maximum acceptable op-amp offset before trimming is 700uV. This ensures that the drift of the residual offset doesn't exceed the error budget of 0.5°C. The offset of the op-amp is shown in Fig. 5-3. Since the op-amp and the comparator are similar in structure, it is assumed that their offset is similar. Fig. 5-3 shows that the 3-sigma offset is roughly 700uV. The main contributors are the threshold mismatch between the input pair (50%), the current source (8%) and the current sink (7%). The remaining offset is due to residual current-factor mismatch.

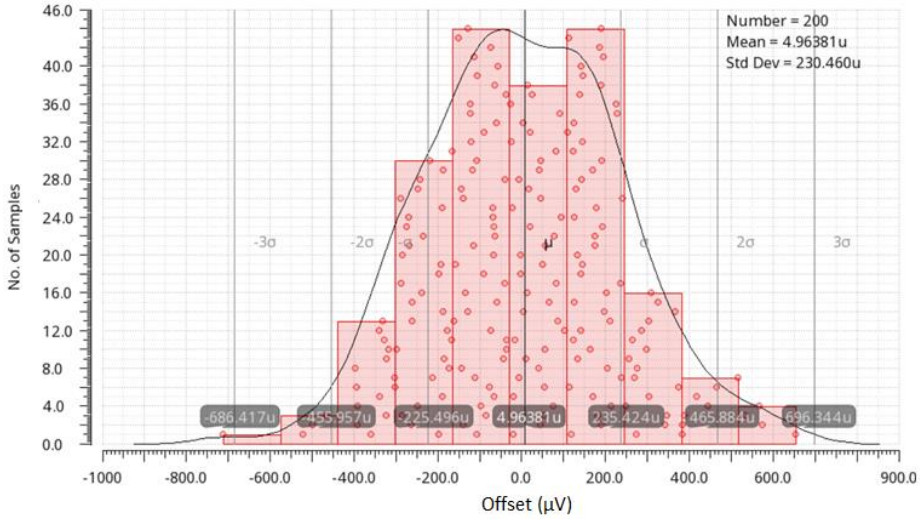


Fig. 5-3: Offset

The resulting temperature detection error is shown in Fig. 5-4

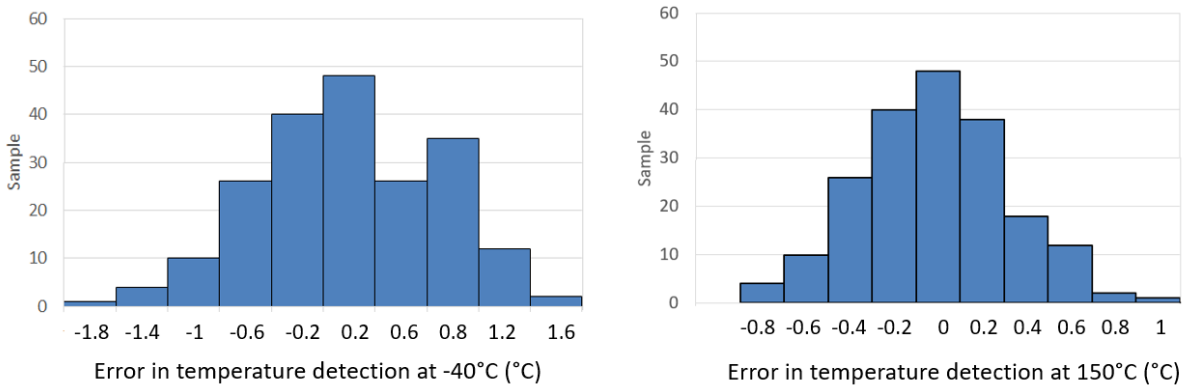


Fig. 5-4: Error in temperature detection due to op-amp offset

The untrimmed offset results in ±1.8°C and ±0.8°C error at -40°C and 150°C, respectively.

As discussed in section 3.2.4, the offset is trimmed out in two phases, in phase-1, OP1 is trimmed and in phase-2, OP2 is trimmed. The configuration of the switches and the op-amps is shown in Fig. 5-5.

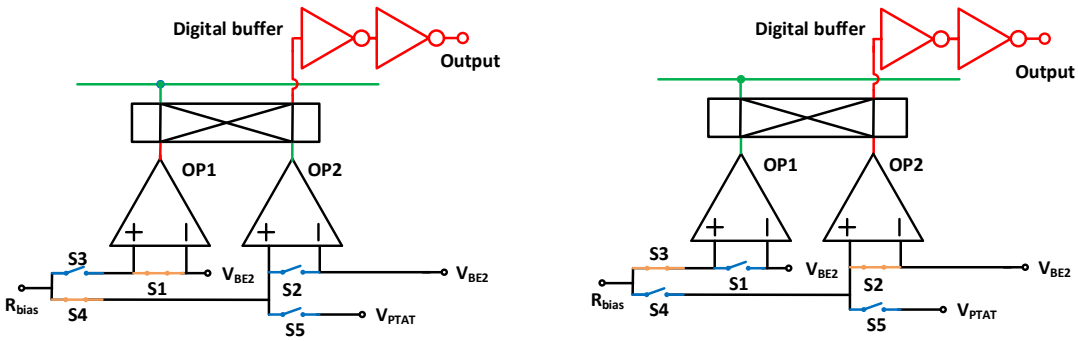


Fig. 5-5: Phase-1 and Phase-2 of the offset trimming

Phase-1: The inputs of OP1 are shorted and its output is connected to the digital buffer. While OP1 is in this open-loop configuration, OP2 is connected to V_{BE2} and R_{bias} and provides the required biasing to the system. Based on the polarity of the output, the inputs of OP1 are

trimmed, using the reconfigurable differential pair (RDP) until the polarity of the digital output is reversed. This completes the offset trim for OP1.

Phase-2: Now that OP1's offset is trimmed; it is switched into the bias circuit in place of OP2, while the inputs of OP2 are shorted and its output is connected to the digital buffer. The same process, as done in Phase-1 is implemented for OP2. Once the offset of OP2 is trimmed, its input terminals are connected to V_{BE2} and V_{PTAT}, so that it behaves as a comparator.

The simplicity of this trimming techniques lies in the fact that no analog measurement is required, only the digital output of the device needs to be monitored.

Once the op-amp offset is trimmed, the drift of the residual offset over temperature is observed, which is shown in Fig. 5-6.

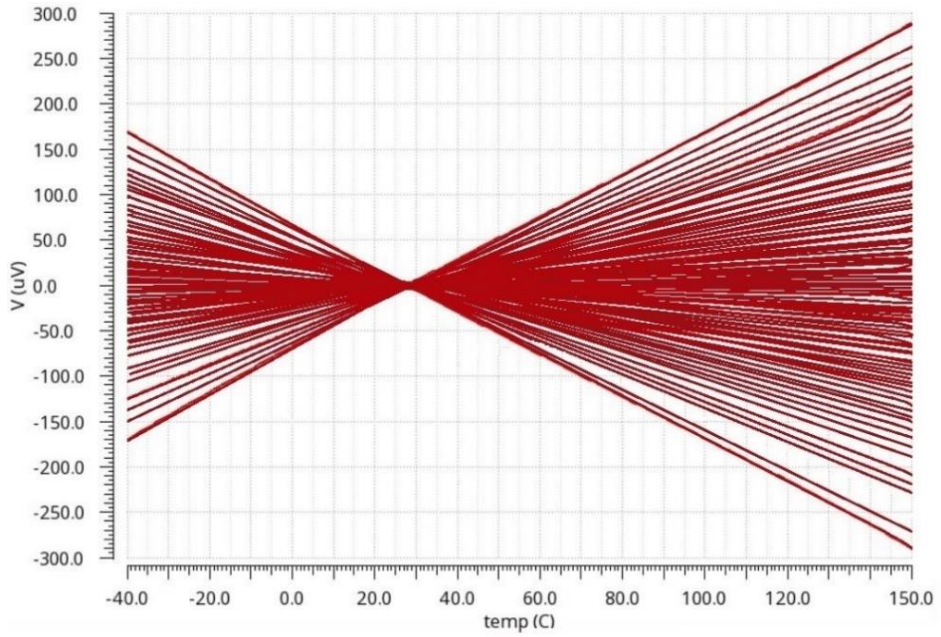


Fig. 5-6: Drift of the residual offset over temperature

From Fig. 5-6, it can be seen that, once the offset is trimmed at room temperature, it spreads to 160µV at -40°C and 300µV at 150°C. The resulting error in temperature detection at those two temperatures is shown in Fig. 5-7.

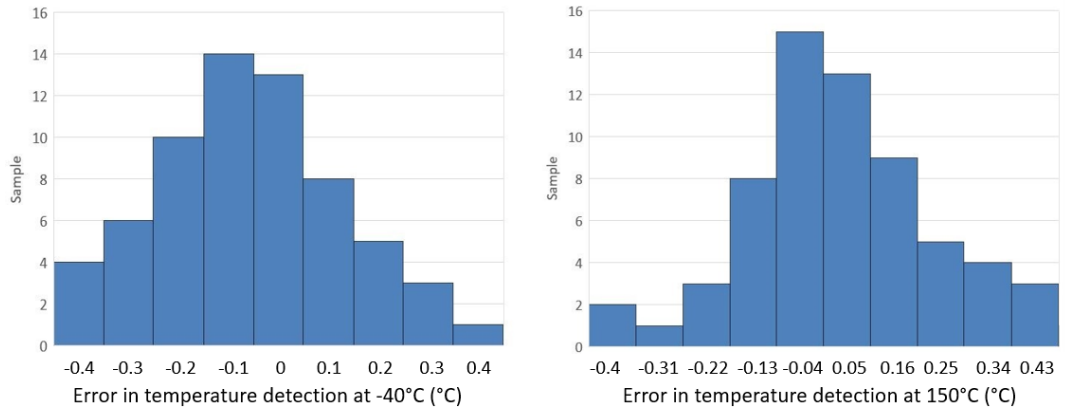


Fig. 5-7:Error in temperature detection due to drift of residual offset

From Fig. 5-7, the maximum error in the detected temperature threshold at -40°C and 150°C is then ±0.4°C and 0.43°C, respectively. The corresponding errors in V_{PTAT} are 2.07mV and 1.24mV respectively. This is within the error budget of the op-amp offset.

The comparator sees similar spread in its trimmed offset, however, the temperature detection error due to its offset is less than ±0.1°C. The error due to comparator offset is less than the op-amp offset because the comparator offset does not see the ($\gamma \cdot R_{th}/R_{bias}$) amplification seen by the op-amp offset. Here 'γ' is the ratio of the current through the IDAC and the current through R_{bias}. Thus, the overall temperature error caused by offset is less than ±0.5°C at both temperature extremes.

5.3.2 System performance in the presence of PTAT error sources.

Once the op-amps, OP1 and OP2, are calibrated for offset, the PTAT errors can be trimmed. As mentioned in section 3.3.3, the PTAT trim is performed using the segmented DAC.

One of the prominent PTAT error sources is the spread in saturation current. The change in the base-emitter voltage of the BJT due to the spread in the saturation current is shown in Fig. 5-8

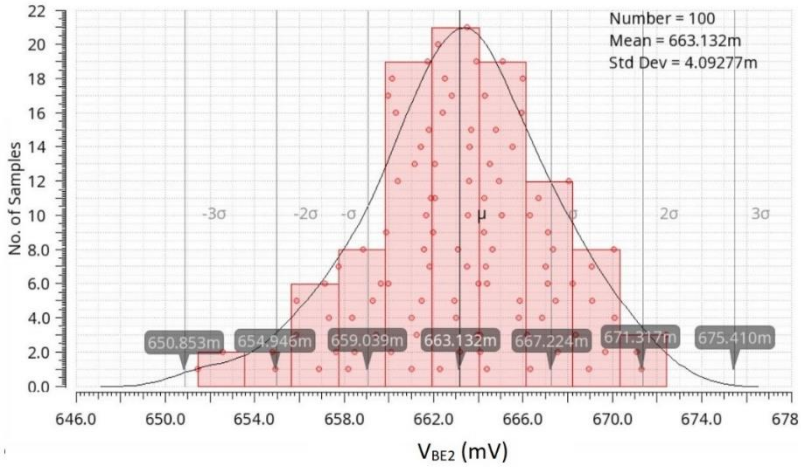


Fig. 5-8: Change in V_{BE2} due to spread in the saturation current

The spread in V_{BE2} is simulated by ensuring that all the other components are ideal. The 3-sigma spread in V_{BE2} is observed to be 12.27mV (1.85%) at room temperature. The resulting error in temperature detection at 150°C due to saturation current spread along will be roughly 4°C.

Apart from the saturation current spread the error introduced by the resistor mismatch is also mitigated by the PTAT trim. The variation in V_{PTAT} due to resistor mismatch is shown in Fig. 5-9

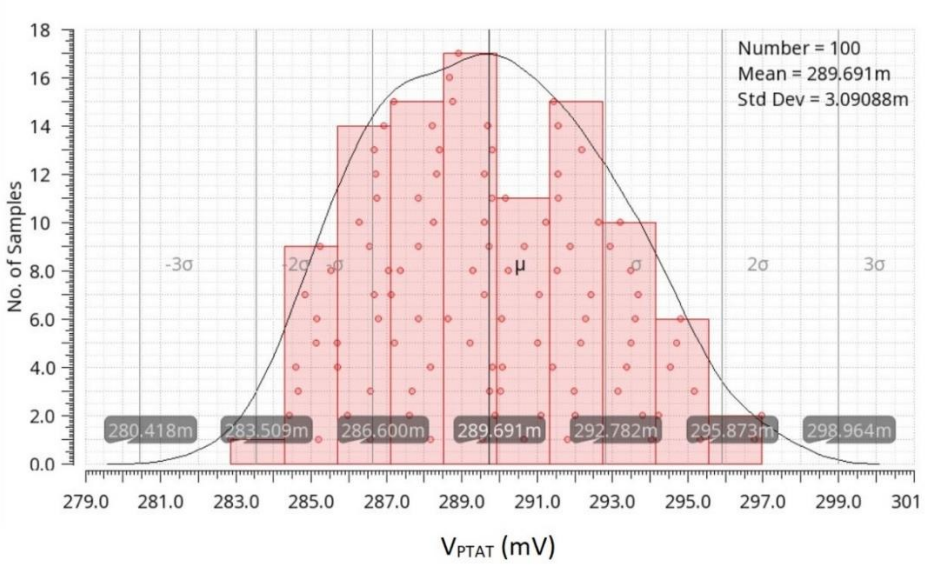


Fig. 5-9: Spread in V_{PTAT} due to resistor mismatch

The graph shows, that the mismatch in resistors R_{bias} and R_{th} and the resultant 3-sigma spread of V_{PTAT}; 9.27mV, translates as a 3.2% mismatch in the resistors.

The current source mismatch is also partly tackled by the PTAT trim. At room temperature, the mismatch in the current sources can be gleaned from the spread in the current. For the purpose of observing the current source mismatch, the I_{MSB} of the IDAC was chosen and is shown in Fig. 5-10.

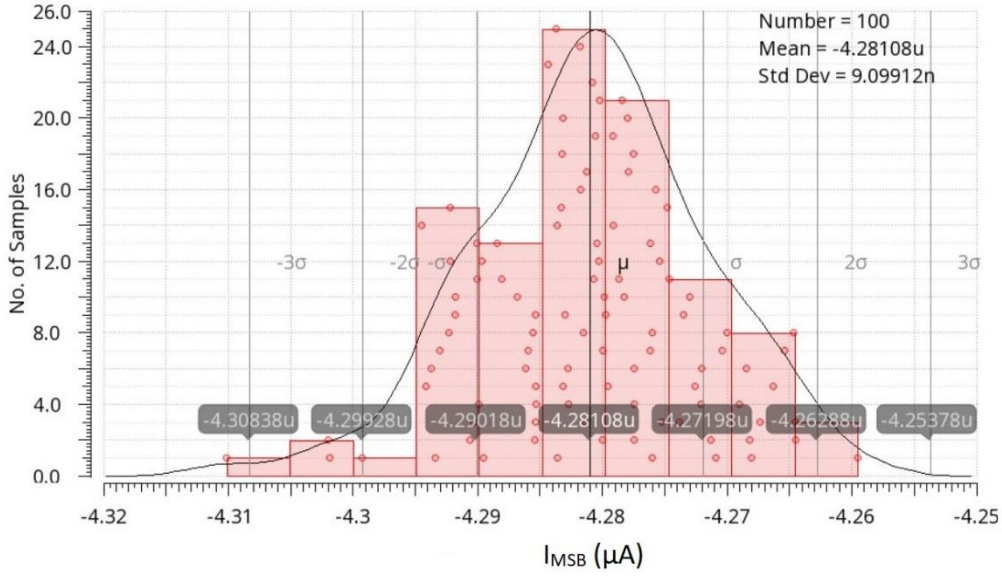


Fig. 5-10: Spread in I_{MSB} due to CS mismatch

The 3-sigma spread in current is observed to be 27.29nA, which translates as a 0.63% mismatch in the current sources. The primary source of this current mismatch is the threshold voltage mismatch of CS1 (31%) (shown in Fig. 4.1). The resulting 3-sigma error in V_{PTAT} due to the mismatch current is approximately 4mV.

As shown in section 2.4, the PTAT error source changes the slope of either V_{PTAT} or V_{BE2}. Thus, to counter the impact of these error sources on temperature detection, the slope of V_{PTAT}

must be trimmed. The PTAT trim is carried out at room temperature, by using the functionality of the temperature switch itself. The device is then in its normal mode of operation, i.e. OP1 is biasing the system and OP2 is used as a comparator. The current through the IDAC is configured to be 3.21µA. Typically, in the absence of any error, this current would ensure that V_{PTAT} is equal to V_{BE2} at room temperature.

The comparator compares V_{PTAT} and V_{BE2}.

A. If the comparator outputs a digital high, it implies that V_{PTAT} is higher than V_{BE2}. To ensure equality at room temperature, the nominal position of the tap in the tapped resistive ladder is first decreased, to decrease V_{PTAT}, until the polarity of the comparator output changes.
B. If the comparator output does not change polarity, the current through the IDAC is decreased using I_{LSB} steps to ensure that the PTAT error is trimmed out.
C. A similar procedure is followed if the comparator outputs a digital low. However, in this scenario the position of the tap is increased with respect to its nominal position, to increase V_{PTAT}. If the range of the tapped resistive ladder proves insufficient, the current is increased, through the IDAC, to remedy the situation.
D. The trim code is then integrated with the temperature threshold programming code.

As in the case of offset trimming, only the output of the comparator has to be observed while the trimming is performed.

Once the PTAT trim is completed, the error in temperature detection, due to the PTAT error sources is shown in Fig. 5-11.

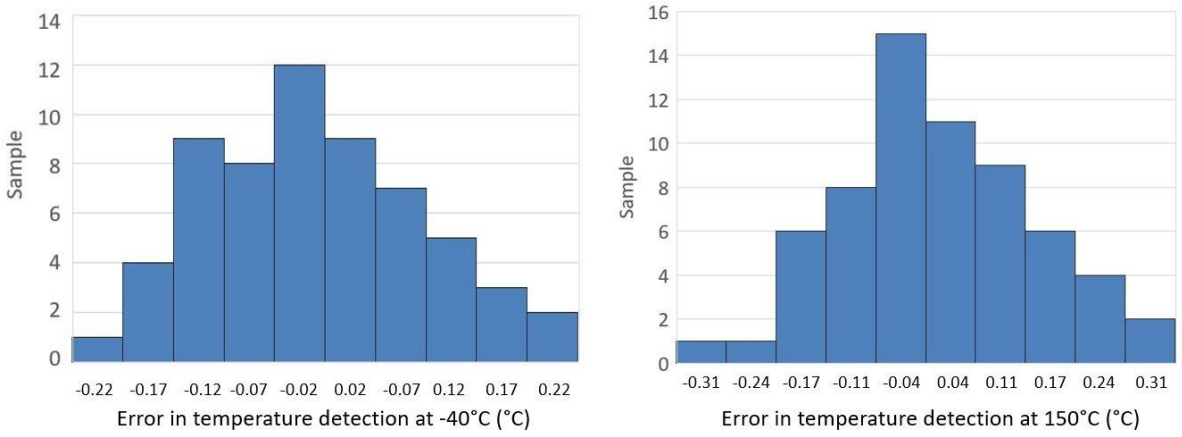


Fig. 5-11: Error in temperature detection after a PTAT trim is performed.

Observing the error in temperature detection at -40°C and 150°C, it can be seen that the maximum error is observed at 150°C and is ±0.3°C, which is in line with the proposed error budget for the PTAT errors. 36% of the residual PTAT error is due to the non-PTAT temperature behaviour of CS mismatch. While the remaining error may be due to the limited resolution of the trim and to a small part due to the thermal coefficient of the resistors. The resulting error in V_{PTAT}, 1.14mV and 0.89mV at -40°C and 150°C, is within the stipulated error budget for PTAT error sources.

5.3.3 System performance in the presence of offset and PTAT errors

In the earlier sections, the offset and PTAT error sources were considered individually. In this section, the combined impact of all the error sources on the temperature threshold detection

has been presented. The same trimming procedure as mentioned earlier has been used (first the op-amp offset trimming is done, followed by the PTAT trimming) after which the temperature threshold is detected. Fig. 5-12 shows the inaccuracy of the temperature thresholds at -40°C and 150°C.

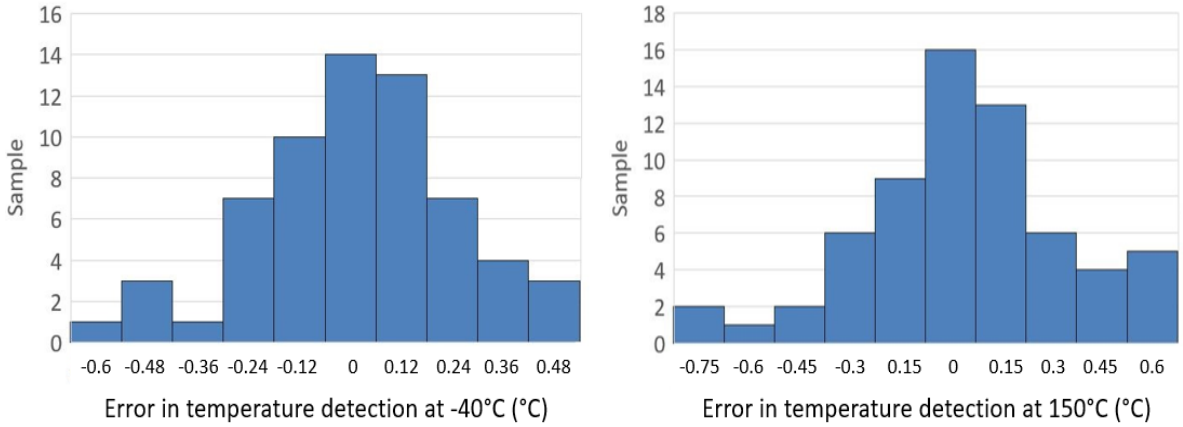


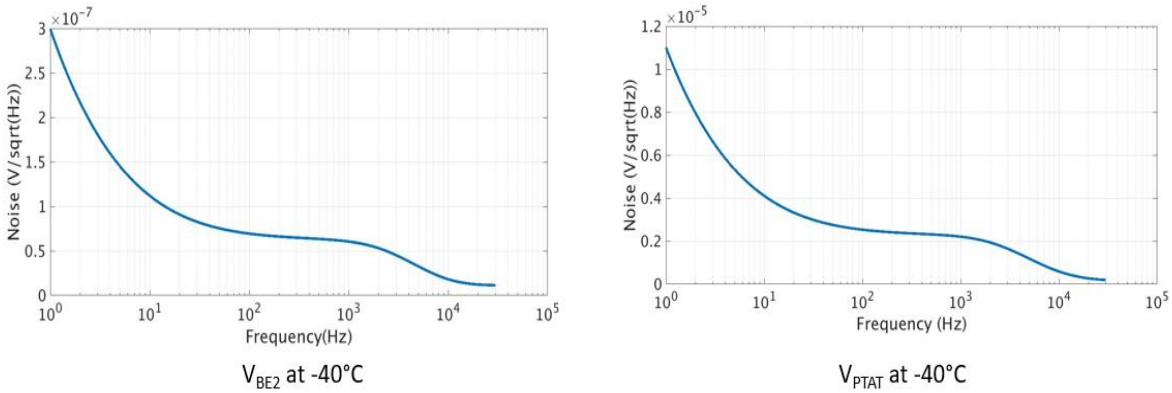
Fig. 5-12: Error in temperature detection after offset and PTAT trim.

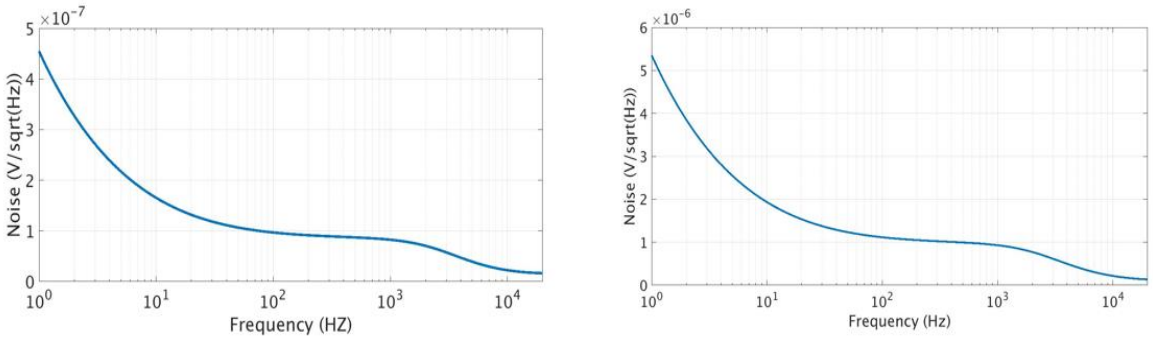
Based on Fig. 5-12, the inaccuracy in the temperature thresholds at -40°C and 150°C is ±0.75°C. This is slightly larger than the expected inaccuracy (0.6°C) based on the two earlier simulation results (offset and PTAT error sources individually). A possible cause for this may be the impact of the residual comparator offset on the PTAT trim. This would result in an extra PTAT error; however, this is not enough to account for the entire 0.15°C deviation.

5.4 Impact of noise on temperature detection

Until now only the static errors were tackled using trimming, however, noise at the cross-over point during the temperature detection will result in unwanted switching near the temperature thresholds. Hence investigating the noise at -40°C and 150°C is important.

Fig. 5-13 shows the noise on V_{BE2} and V_{PTAT} at -40°C and 150°C respectively.



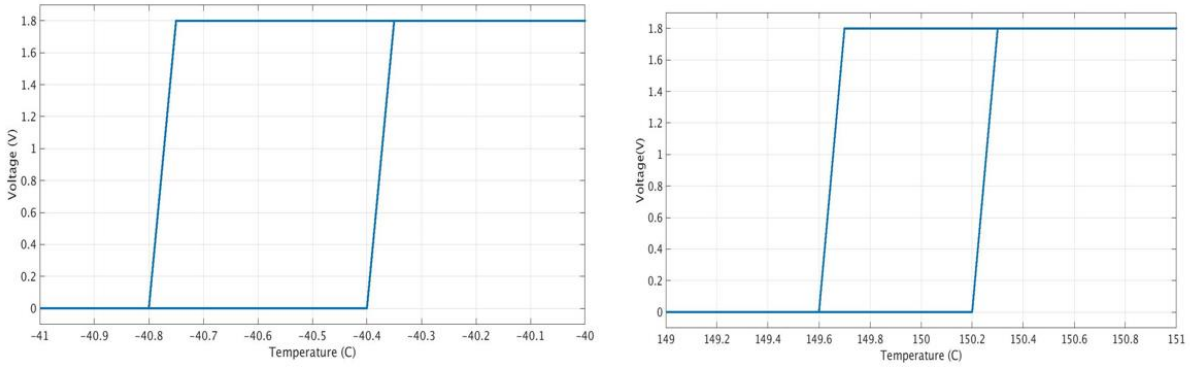


V_{BE2} at 150°C

V_{PTAT} at 150°C

Fig. 5-13: Noise over V_{BE2} and V_{PTAT} at -40°C and 150°C

The integrated noise of V_{BE2} at -40°C and 150°C is 4.15µV and 5.15µV respectively. While the integrated noise of V_{PTAT} at -40°C and 150°C is 56.6µV and 64µV. While the noise in V_{BE2} is lower, the noise in V_{PTAT} can cause a temperature detection error of 0.05°C. To prevent this from affecting the system, a hysteresis-loop of 0.2°C and 0.3°C is introduced at -40°C and 150°C, which is shown in Fig. 5-14.



±0.2°C hysteresis at -40°C

±0.3°C hysteresis at 150°C

Fig. 5-14: Hysteresis at -40°C and 150°C

5.5 Impact of power supply variation

The impact of the power supply variation on the temperature threshold measurement must be assessed. In this scenario, the supply voltage is increased and decreased by 200mV above the nominal value to see the performance of the temperature switch.

The performance of the temperature switch for a temperature threshold of -40°C and 150°C, over the power supply variations is shown in Fig. 5-15.

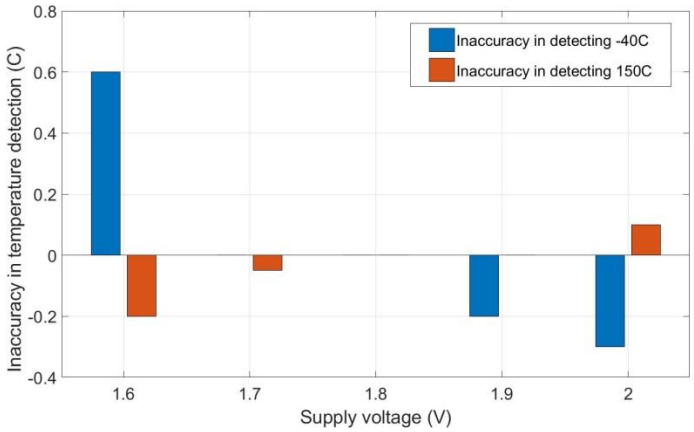


Fig. 5-15: Impact on temperature detection due to power supply variation

While the performance of the switch is good for the 150°C temperature threshold, a low supply voltage severely impacts the -40°C temperature threshold. This is because at -40ºC, the PMOS cascodes of op-amp are not in saturation, as a result of which the gain of the op-amp drops to 60dB. This loss of gain results in an error of 0.6°C at a supply of 1.6V.

5.6 Comparison

Based on the achieved results, a comparison of various thermal sensors for thermal management is presented in Table 5-1.

Table 5-1: Comparative analysis with prior art

	Schinkel et al. [13]	Duarte et al. [14]	Bass et al. [15]	Lu et al. [16]	Canio et al. [17]	This work
Technology (nm)	180	65	65	22	28	160
Output type	1-bit	1-bit	8-bit	8-bit	1-bit	1-bit
Temperature range (°C)	125	30-105	-10-110	-30 to 120	-40-125	-40-150
Trimming Type	NA	2-point	2-points	1-point		1-point
3-sigma inaccuracy (°C)	±4.6	±1.1	±1.35	±1.07	±4.0	±0.75
Relative inaccuracy (%)	3.68	1.33	1.12	0.71	2.42	0.48
Power Consumption at 27°C (µA)	13	1200	86	50	72	7
Dynamic techniques	NA	chopping	NA	NA	NA	NA
Area estimate(mm^2)	0.03	0.027	0.003	0.0043	-	0.05

It can be seen that the designed temperature switch provides the maximum temperature range with a relative inaccuracy of 0.48%. The temperature detection inaccuracy is within the error budget of ±1.0°C. Furthermore, this design has the lowest current consumption.

Chapter 6 Conclusion and Future work

6.1. Conclusion

In this thesis, a programmable temperature switch with a high-temperature range, low inaccuracy and minimum power consumption is presented. Using a top-down design approach, system-level specifications were defined that outperform the prior art. Block-level circuits were designed to tackle various error sources like the offset, the saturation current spread and other PTAT errors and also provide the required temperature threshold programmability. These block-level designs were realized on a transistor level and simulated in Cadence. The simulated performance of the system was then compared with the prior art.

The designed system has a temperature threshold detection accuracy of ±0.75 °C over the temperature range of -40°C to 150°C. This was achieved using a single point temperature trim and without the use of any dynamic techniques. The trimming procedure was simplified due to the use of a one-bit response from the comparator, on acquiring the targeted trimming values. The trimming coupled with the two way use of the segmented DAC, for setting the temperature threshold and correcting for PTAT errors, has resulted in this performance.

6.2. Future work

Based on the temperature threshold detection errors presented in chapter 5, it can be seen that the accuracy of the sensor is limited by the op-amp offset rather than the PTAT error sources. This error is a result of the high-temperature spread of the residual offset. Hence a design that can tackle the threshold mismatch without requiring large area needs to be investigated.

The requirement for the low area of the temperature switch stems from the fact that multiple thermal sensors are required on the same die to detect hot-spots. However, this requirement can be mitigated if remote sensing elements can be used. This would conserve the area while achieving the desired functionality.

While the design is not overly large, it can be substantially reduced by increasing the power consumption of the device. For example, a 3-fold increase in current will result in smaller transistor sizes of the current sources while keeping them in saturation. This will result in a significant area saving.

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