Load insensitive power amplifiers

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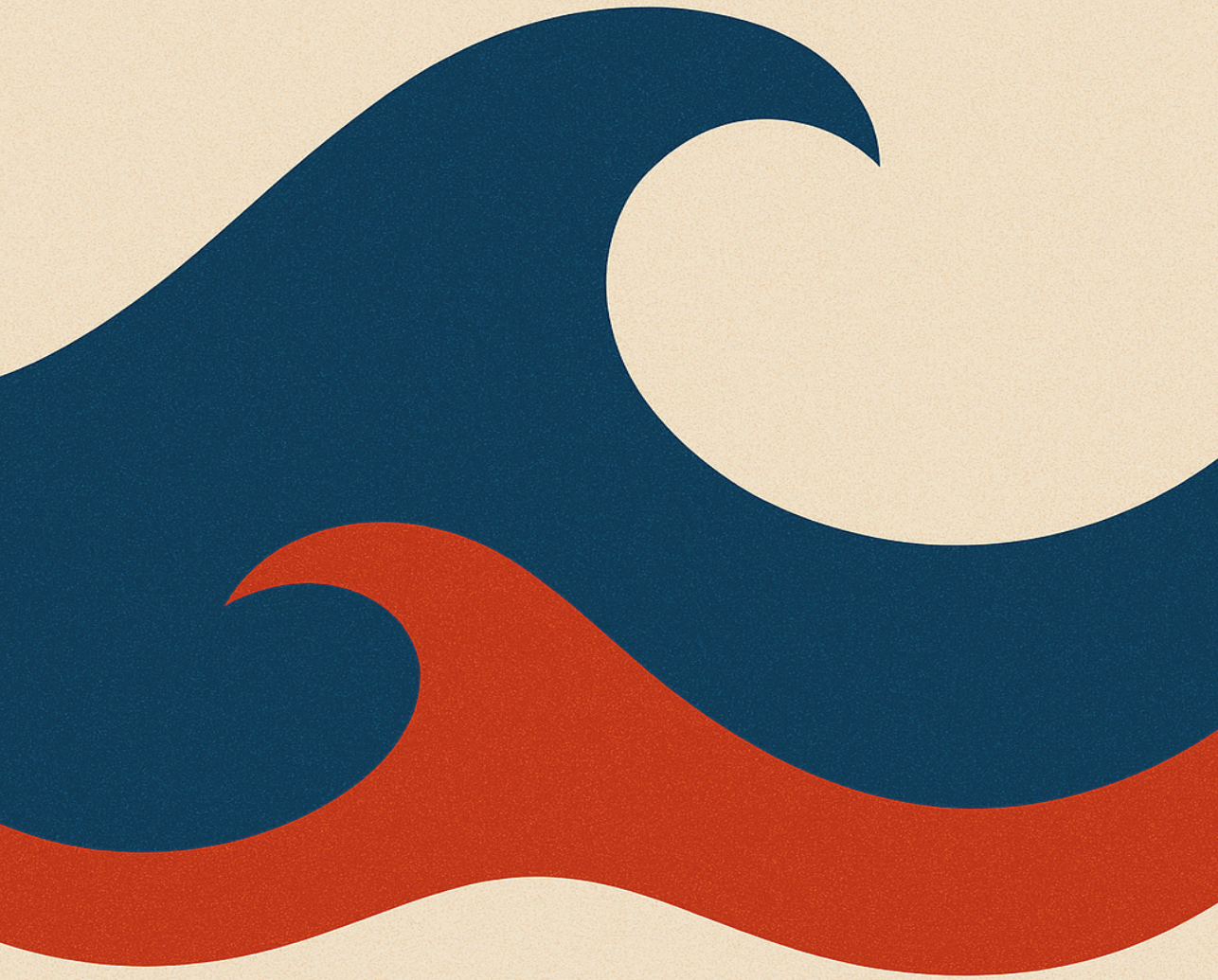

Gagan Deep Singh

LOAD INSENSITIVE POWER AMPLIFIERS

GAGAN DEEP SINGH

LOAD INSENSITIVE POWER AMPLIFIERS

Proefschrift

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft,
op gezag van de Rector Magnificus Prof. dr. ir. T. H. J. J. van der Hagen,
voorzitter van het College voor Promoties,
in het openbaar te verdedigen op

Donderdag 12 Juni om 12:30 uur

door

Gagan Deep SINGH

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This work is dedicated to everyone's implicit and explicit contributions.

Gagan Deep Singh

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INTRODUCTION

1.1. MOTIVATION

Telecommunication technology has touched every aspect of the modern society. It is generally considered one of the key drivers of global economic growth. Its revolution began with the introduction of wireline technology [1] which was followed by steadfast adoption of wireless services over the last three decennia, yielding today's highly connected infrastructure [1]. It is, therefore, not surprising that telecommunication affected all industries, including healthcare, automotive, manufacturing, transportation, agriculture, and many more, increasing their productivity while yielding significant cost savings. Given this, industry 4.0 [2] (i.e. smart manufacturing and intelligent factories) is currently directing the further digitization of all application fields. This steadfast adoption of wireless services over time has led to an exponential growth of data traffic, which is mostly handled by increasing the data rates of these electronic systems (see Fig. 1.1). Consequently, even during the disruptive times, when COVID-19 [4] brought the

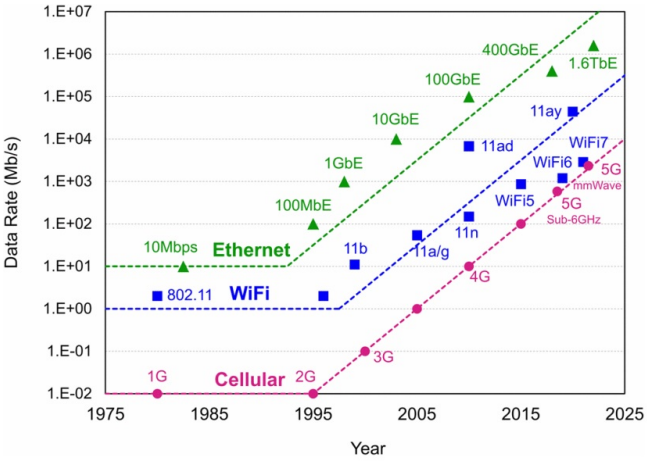

Figure 1.1. The increasing date rate of wireless communication over the past two decades[3].

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world to a standstill, broadband communication played a vital role in running all kinds of activities remotely. More recently, large investments in artificial intelligence (AI) have pushed the demand to gather, i.e., through the Internet-of-Things (IoT), and analyze vast amounts of data even more. As such, large investments in telecommunication technologies like 5G and its successors are being demanded to meet the expectation. In 2030, 5G will contribute $1.3tn to the global gross domestic product (GDP) [5]. Unfortunately, the adoption of new broadband wireless solutions comes with a steeply increased energy consumption. As such, 5G electricity usage is expected to surpass the consumption of all previous wireless generations (see Fig. 1.2). This is a highly undesirable development in view of the climate change. Consequently, new technology solutions are needed to reduce the energy consumption of wireless networks. To obtain insight into the energy

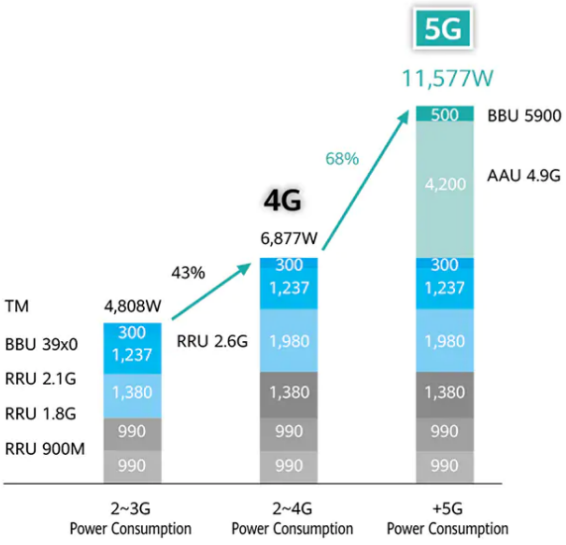

Figure 1.2. The growing base station energy consumption of advanced communication technology [6].

use of a mobile operator, consider Fig. 1.3, which splits this energy consumption for its key components, namely the radio network, core network, data centers, and other operations. Clearly, the radio network, along with its radio units (base stations), dominates. Note that the power amplifiers are responsible for ≈ 59 % of the power consumption in a radio unit (Fig. 1.3 (b)). In the 5G communication network, the base station power consumption is expected to grow by more than ≈ 65 % [5].

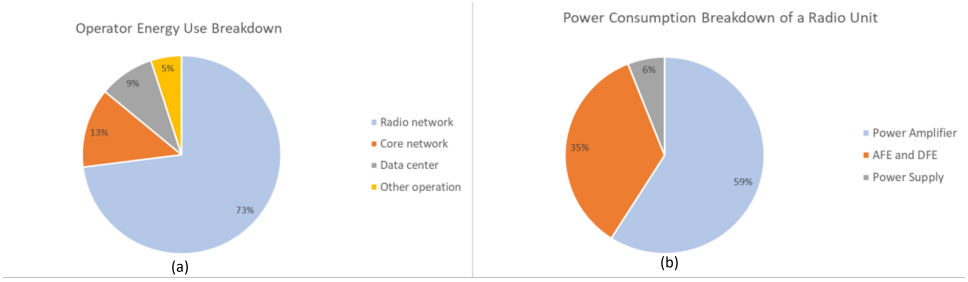

Figure 1.3. Breakdown of the power consumption of a wireless communication network in its key components [7]. (b) Power breakdown of a radio unit, which its power amplifier, antenna front-end, digital front-end and power supply.

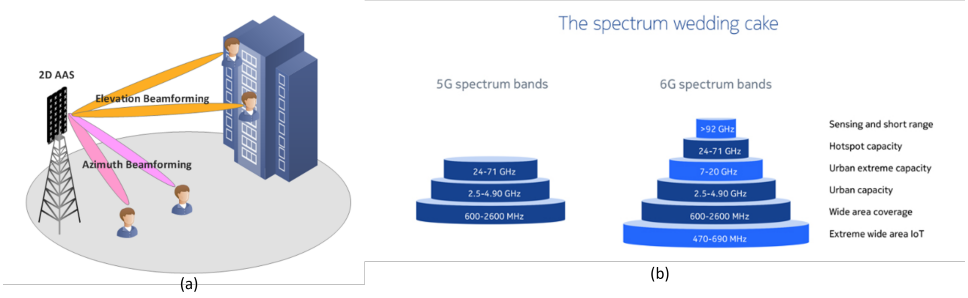

Figure 1.4. 5G/6G beamforming base station with active antenna array [8]. Spectrum allocation of 5G and 6G networks [9].

1.2. BASE STATIONS

In Fig. 1.2 the increase in power consumption of the radio access network (RAN) can be explained by the introduction of higher modulation bandwidths, the use of higher operating frequencies, and the adaptation of (massive) multiple-input-multiple-output system architectures (mMIMO) (see Fig. 1.4(a)), which allow to improve for link budget and data capacity. However, mMIMO also yields a massive increase in the number of transmitters and receivers and the base station complexity. At this moment, a state-of-the-art 5G mMIMO base station has 8 x 12 x 2 = 192 antenna elements with their related transmitters and receivers. It is known from that undesired coupling of antenna elements in a 2-Dimensional active antenna system (2D-AAS) [10], with changing beam patterns, yields variations in the impedances that these antenna elements offer to their RF front ends. Therefore, to the best of the author's knowledge, all base stations below 10GHz make use of isolators between their RF front-ends and antenna elements to guarantee the optimum performance of their transmitter/receiver in all circumstances. Consequently, the introduction of mMIMO caused massive growth in the isolator market (see Fig. 1.5). Despite their many advantages, the use of isolators also yields cost, form

factor, integration, bandwidth, and loss challenges in wireless systems. It is, therefore, the general expectation that when going up in frequency to address new communication bands (Fig. 1.4(b)) or increasing the number of TX/RX units for the realization of 6G Extreme-mMIMO systems (with up to 1024 AE), or when targeting for multi-band operation, the use of isolators becomes less attractive and at some point, impractical.

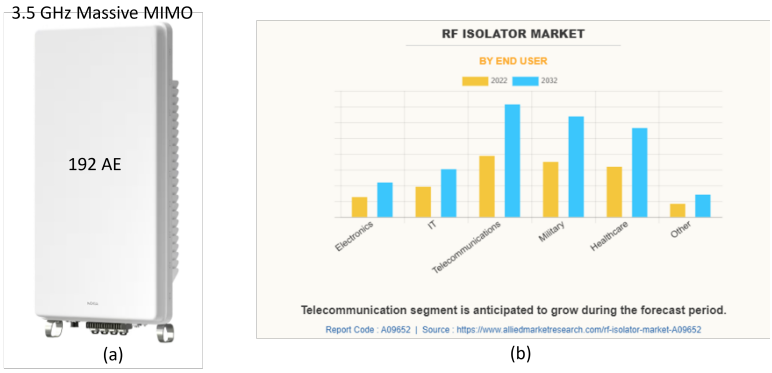

Figure 1.5. (a) High-end 5G mMIMO base station. (b) Growth in isolator demand across different verticals [11].

1.3. HANDSETS

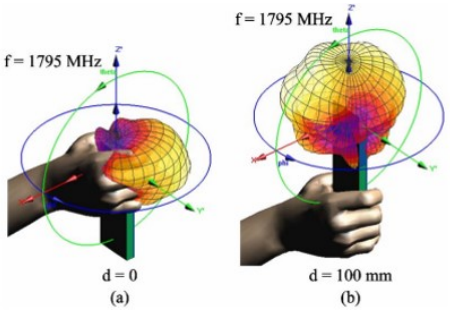

Figure 1.6. Change in the input impedance of the antenna due to hand effect [12].

Although the global energy consumption of handsets is significantly lower than that of base stations, the fact that they are battery operated, puts strong attention on the energy consumption of their PAs. In view of this, handset antennas provide the optimum loading impedance to their PAs when pointed into free space. However, the phone's antenna proximity to surrounding materials and the way the user might hold a hand on

the mobile phone can cause severe obstruction of the free space condition, yielding reflections that cause a change in the impedance provided by the handset antenna [12] (see Fig. 1.6), which affect the operating conditions thus the energy efficiency of the PA. Since the input impedance of the antenna depends on changes in the physical environment of the antenna, these changes will be relatively slow, e.g., in the millisecond range. Furthermore, for specific antennas, the change in impedance tends to follow a certain trajectory on the Smith chart, somewhat elevating the need for a generic solution [13]. Also, in the handset segment, multi-input-multi-output antenna systems are more and more adopted, but since the form factor in a handset is much more constrained than in a base station, the number of antenna elements is also restricted. To the best of the author's knowledge, using isolators in handsets is uncommon for cost, form factor, and band coverage reasons.

1.4. LITERATURE: LOAD RESILIENT POWER-AMPLIFIER

From the above, it is evident that there is a clear need for transmitter solutions for both base stations and handsets that can handle varying load impedance conditions without sacrificing their performance in terms of RF output power, efficiency, signal accuracy, and spectral purity. This need has triggered a global search for identifying these solutions, yielding various proposed techniques to handle such a load variation. To place these techniques in the right context, we will first discuss a simple Class-B amplifier line-up under nominal and mismatch conditions. Next, we discuss its improved performance when applying an ideal isolator. Then, we continue with a brief overview of the state-of-the-art load-resilient amplifiers.

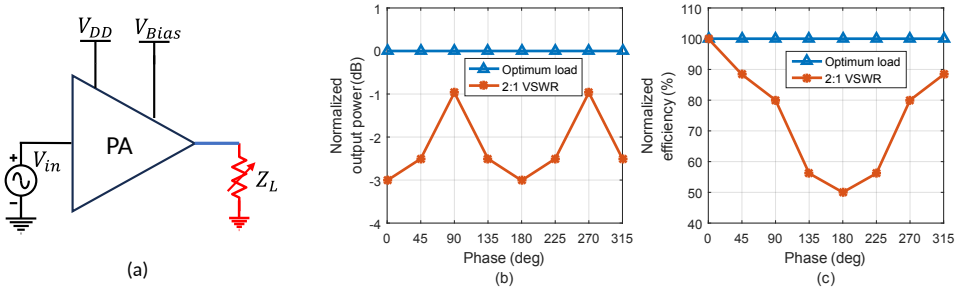

Figure 1.7. Analysis of an ideal class-B PA designed for the optimum load ($Z_l = R_{opt}$) and when subjected to a VSWR.

Class-B PA: An ideal class-B power amplifier (see Fig. 1.7) is designed for nominal load impedance ($Z_L = R_{opt}$) for a given supply voltage (V_{DD}) and maximum saturation current (denoted by $I_{d_{max}}$), which is typically dictated by the active device(s) in the output stage of the transmitter. The normalized output power and efficiency for optimum load and a VSWR of 2:1 across 0°-360° phase angle is shown in Fig. 1.7(b) and (c). It can be observed

that the worst drop in output power and efficiency is ≈ 50 %. This drop in performance is due to the non-optimum voltage and current waveforms (see Fig. Fig. 1.8(a)) which deviates from the point where the active devices can reach/touch both voltage and current saturation (see Fig. 1.8(b) for the load-line trajectory).

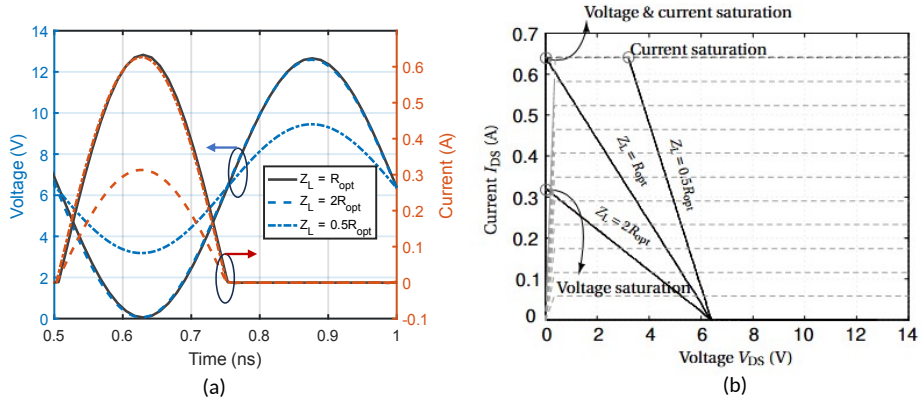

Figure 1.8. The class-B PA (a) transient voltages and currents. (b) load line ($Z_L = R_{opt}$) with its deviation for $Z_L = 0.5R_{opt}$ and $Z_L = 2R_{opt}$ case.

1.4.1. IDEAL ISOLATOR

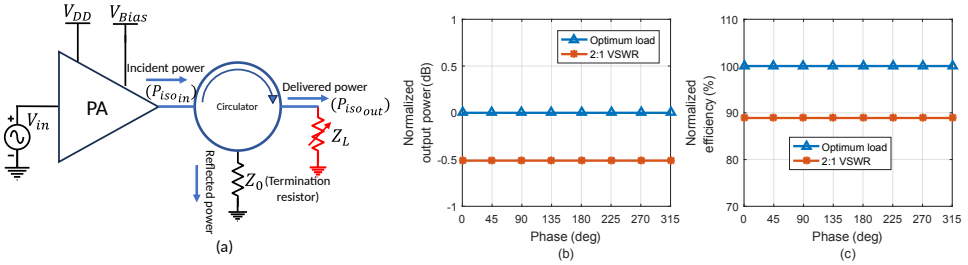

Figure 1.9. Class-B PA output matching network replaced with a (a) circulator with the third port terminated with optimal impedance to absorb any reflection. (b) normalized power and (c) drain efficiency across optimum load and VSWR

The most common way to deal with the changing loading conditions is to break the reciprocity of the output matching network. This can be achieved using the anisotropic material properties of a ferrite in an isolator. Such an isolator has in the ideal case the following unidirectional two-port scattering matrix,

$$[S] = \begin{bmatrix} 0 & 0 \\ 1 & 0 \end{bmatrix} \tag{1.1}$$

Since the scattering matrix is non-unitary, the isolator acts like a lossy device, since all the reflected power will be absorbed and dissipated in the termination resistor of the isolator (see port-3 in Fig. Fig. 1.9(a)) . For a given load reflection (Γ) coefficient and input power ($P_{\text{iso}_{\text{in}}}$), the output power from the isolator is given by

$$P_{\text{iso}_{\text{out}}} = (1 - |\Gamma|^2) P_{\text{iso}_{\text{in}}} \tag{1.2}$$

The power dissipated in the isolator ($|\Gamma|^2 P_{\text{iso}_{\text{in}}}$) will lower the efficiency of an ideal class-B amplifier by

$$\eta_{\text{TX}} = (1 - |\Gamma|^2) \eta_{\text{ClassB}} \tag{1.3}$$

The simulation results of a class-B PA with an isolator (circulator with third port terminated in 50 Ω) (see Fig. 1.9(a)) in its output matching network is shown in Fig. 1.9(b) and (c). It can be observed that the worst case output power and efficiency penalty for a VSWR of 2:1 is only ≈ 11 %. The performance benefits of the isolator has led to its growing demand isolators in telecommunication systems (see Fig. 1.5).

1.4.2. TUNABLE MATCHING NETWORK

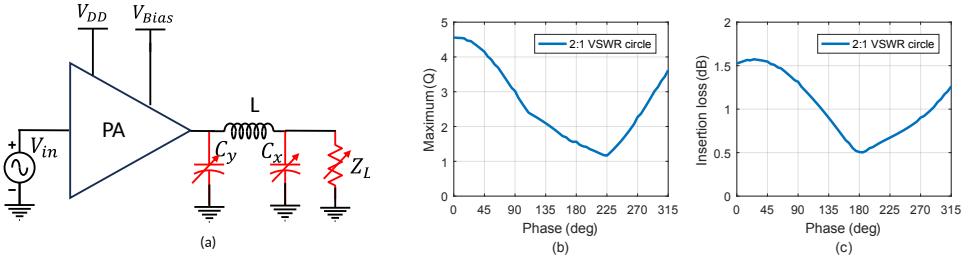

Figure 1.10. A tunable π-match network to overcome the load sensitivity of the PA. (b) related maximum matching Q condition in the network and (c) insertion loss (dB) for component quality factor of 40.

Ideally, a tunable matching network (TMN) [14–18] can offer a perfect solution to overcome the load-sensitivity of the PA. In theory the TMN can match any load impedance to the most optimal load the PA needs to see to maintain its performance. An example of a single stage π-match TMN with two adjustable capacitor and a fixed inductor is shown in Fig. 1.10(a). However, matching any point on the smith chart to a constant 50 Ω load comes at the expense of high-Q conditions across these TMN (see Fig. 1.10(b)). The high-Q matching conditions pose two challenges, firstly, due to the finite quality factor of these matching network, the circulating currents in these reactive components lead to significant power loss (see Fig. 1.10(c)). Moreover, the power loss is dependent on the phase angle of the VSWR, causing significant power variation if used in a phased array. Secondly, large voltage swings limit the power handling capacity of these networks, due to restrictions in the tunable components. One way to reduce the high-Q conditions is to perform matching over multiple stages by cascading TMN at the expense of higher series losses [19]. For the above reasons high power (> 30 dBm) TMN find limited usage.

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1.4.3. BALANCED PA

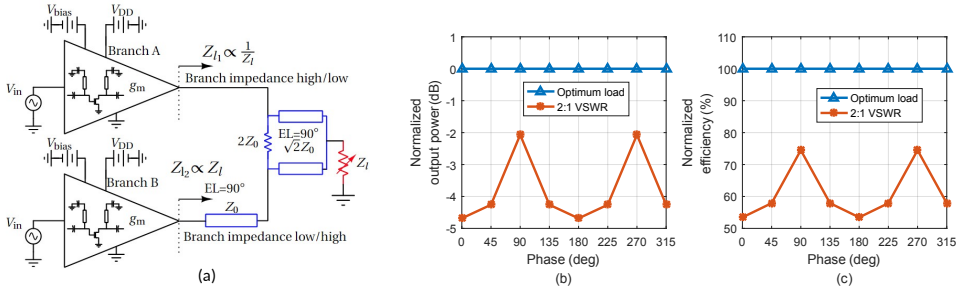

Figure 1.11. A Power amplifier using a balanced structure. It consisting of two class-B PA branches (A and B) and a power combiner network. (b) Normalized output power and (c) efficiency across optimum load and a VSWR of 2:1, when including voltage and current saturation of the output stages.

The balanced power amplifier [20–25] is often proposed to achieve load-resilient behavior. It makes use of two PAs with a 90-degree hybrid coupler / Wilkinson with a 90° transmission line. In Fig. 1.11(a) it can be seen that the branch PA impedance A (Z_{L_1}) and B (Z_{L_2}) moves in the opposite direction for an applied (ohmic) mismatch in the load (Z_L). Due to this opposite behavior and loss in the system to absorb any mismatch, the RF output power of the overall configuration remains close to constant (follows isolator) as long as the individual branch PA does not clip due to voltage or current saturation. The simulation results of the balanced PA output power and efficiency across the optimum load and 2:1 VSWR circle are shown in Fig. 1.11(a) and (b) respectively. It can be observed that balanced-PA performs worse than a class-B in both peak output power and efficiency. Moreover, in a mMIMO architecture, the loading offered by an antenna element can be anywhere between a VSWR of 1:1 to 2:1, which still introduces RF output power variations even when clipping conditions for the individual PA branches are avoided. Unfortunately, for energy-efficient operation, both branch amplifiers need to operate very close to voltage saturation, yielding clipping when a load mismatch is presented. Due to these limitations and the required over-dimensioning of the PA branches, the balanced PA configuration finds, in spite of popularity in literature, very limited use in practical wireless systems.

1.4.4. RE-CONFIGURABLE PA

Recently re-configurable Class-B PA's [26] and Dohety PAs [25, 27, 28], have received considerable interest. Using a N-port concept, these PA's can be modelled as multiple active devices and a power combining network (see Fig. 1.12). The sub-PA's are configured in such a way that they can overcome voltage-saturation of PA's in load mismatch situation. This will allow partial/full recovery of output power depending on the configuration. A large variety of configurations are possibly. Namely, trans-conductance (g_m) and phase adjustments (tunable phase shifter) of the carrier and peaking amplifiers [27]. A recon-

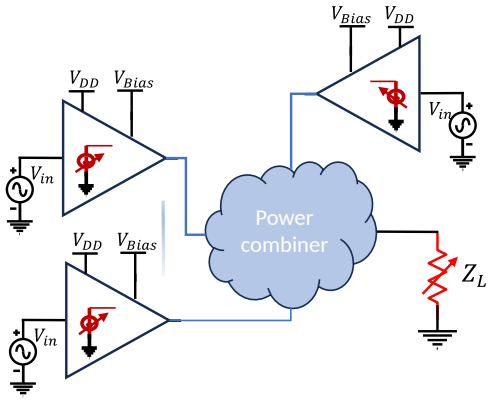

Figure 1.12. A re-configurable PA network consisting of multiple PA units and a power combiner network to relax the load sensitivity of the PA.

figurable series/parallel switchable Doherty [25, 28] or to enhance the performance of this concept even further, a switchable series/parallel Doherty using a coupler with complex impedance termination at the isolation port and adjustable gate bias was proposed in [24]. Furthermore, switching between a balanced PA and DPA configuration using a silicon-on-insulator (SOI) based single-pole-double-throw (SPDT) switch proposed in [22], and multi-port active load-pull introduced in [29]. In conclusion all these techniques do not fully restore the PA/DPA performance from the impact of the applied load mismatch but rather try to "soften" the consequences of this load mismatch.

1.5. THESIS OBJECTIVE AND RESEARCH QUESTIONS

Load-resilient transmitters: From the above overview, one can conclude that in order to handle VSWR conditions, previously proposed transmitter solutions leverage redundancy (see Fig. 1.13, with redundant components highlighted in blue), i.e., some extra circuit components have been added to tolerate/handle/avoid the changing loading conditions across the PA stage. Moreover, two realms of operation are utilized.
Firstly, breaking the reciprocity of the network (i.e., by using an ferrite-based isolator or but using fast in-RF-cycle switching-based isolators [30]) to ensure that no reflections are seen by the PA under load mismatch.

Secondly, by using a reciprocal network and explore circuit redundancy to handle load mismatch.

Since isolators are bulky, costly, lossy and yield bandwidth restrictions, while, fast switching-based circulator are troubled by high losses, and RF-output power constraints. Furthermore, they demand high local oscillator (LO) power for their switches, the focus of this thesis is on the second realm, which uses circuit redundancy to handle the load mismatch." In practical circuits, this will demand tunability/re-configurability of the PA core or the network connecting the PA core to the load.

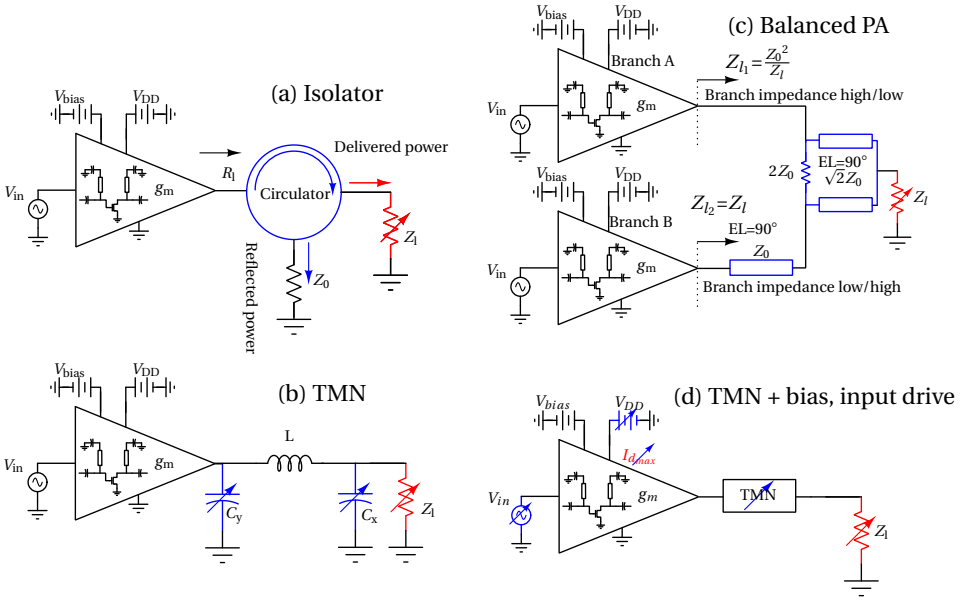

Figure 1.13. Typical use case example of redundancy for RF power amplifiers to handle a VSWR. (a) Isolator, (b) balanced PA, (c) PA with TMN, and (d) PA with bias, input drive, and adjustable TMN.

Research objective: This thesis aims to find isolator-free load resilient transmitter solutions that are energy efficient and wideband in nature.

As such, the transmitter linearity, output power, and efficiency should stay constant regardless of its loading conditions and offer beyond isolator-level performance. A special point of attention is to preserve the linear transfer of the transmitter, such that its DPD correction does not need any adjustments when load mismatch occurs. If this is the case, a single DPD can handle multiple transmitters in phased array systems allowing a dramatic reduction of the (mMIMO) system complexity, and power consumption. The PA efficiency enhancement techniques that will be considered in this work include voltage-supply modulation (envelop tracking) and load line modulation (Doherty).
As a reference, in this work we will the identified load insensitive PA configurations against a conventional PA with an isolator.

Sensing of the load impedance: To control a wireless transmitter to adapt to its changing load, it is necessary to sense the applied load impedance. There are two main categories of impedance sensing in literature, namely; active and passive sensing. Active sensing employs mixer-based down conversion for base-band amplitude and phase detection. Meanwhile, passive sensing only relies on magnitude detection only. Although active sensing techniques [31, 32] are conceptually simple, they are more complicated and expensive in their use when dealing with large signal bandwidth. In stark contrast,

passive magnitude-only detection methods do not require any knowledge of the modulated signal content and can handle very large bandwidths. However, traditionally passive impedance sensing needs extensive calibration and computation to determine the applied loading [33][34].

Research Objective This thesis aims to find full-range load impedance sensing of wireless transmitters with low-complexity, low-loss wideband magnitude detectors. The combined research objectives of this disseration results in the following related research questions.

Research questions

- How can we achieve maximum VSWR handling for a TX line-up yielding the lowest Q conditions in the matching network?
- How, to incorporate back-off efficiency enhancement technique in wide-band VSWR resilient PA's?
- How, to achieve ultra-fast VSWR adaptation?
- How can we achieve VSWR-resilient PA's that allow constant load impedance trained digital pre-distortion (DPD)?
- How to sense the load mismatch without pre-knowledge of the TX signal?

1.6. THESIS ORGANIZATION

The organization of this dissertation is as follows:

1.6.1. WIRELESS SIGNALS AND SYSTEMS

Chapter 2, gives the background theory and context needed to place the results of the following chapters in the proper context. It addresses the modulated signals and systems concepts used in wireless applications and networks. The choice of system architecture dictates the varying loading conditions seen by the PA. Furthermore, it highlights that traditional digital pre-distortion (DPD) solutions become impractical in addressing the load sensitivity of MIMO systems. This underscores the need for inherently load-insensitive or resilient PA's capable of maintaining performance across the changing VSWR, allowing them to function effectively even when paired with DPD systems trained for a constant impedance (e.g., 50 Ω).

1.6.2. IMPEDANCE SENSORS

Chapter 3, introduces a vital block for load-insensitive transmitters, i.e., the impedance sensor, which provides information about the complex impedance seen by the PA. Knowing this impedance is essential for the techniques introduced in the following chapters

that aim to recover the performance of the PA under load mismatch conditions. Chapter 3 starts with discussing the active and passive impedance sensors. Next, two novel passive impedance sensing methods are proposed. To show their effectiveness, both are analyzed, and their experimental verification is provided.

1.6.3. LOAD-INSENSITIVE CLASS-B PA

Chapter 4, discusses a technique for a self-healing power amplifier with integrated load mismatch detection and correction. The varying (complex) load is first compensated for its unwanted susceptance, followed by adjustment of the transistor output stage to handle the ohmic load variation. The latter is achieved by modifying the output stage supply voltage and drive level. This two-step approach avoids the high-Q conditions that occur in tunable matching network solutions, which aim to correct for both the real and imaginary load deviation by adjusting their element values. Consequently, a lower insertion loss and voltage stress can be achieved. Next, to facilitate a fully automated load mismatch detection and correction without the need for (pre-)calibration, a modified two-tap six-port network for impedance detection and a control loop approach is introduced. As proof of principle, a prototype 900-MHz class-AB power amplifier featuring the proposed correction technique, as well as the six-port reflectometer with the control loop, has been implemented as a PCB demonstrator. Measurement results show that the self-healing PA, in the event of a load mismatch, recovers the output stage performance in terms of efficiency, output power, and linearity and, as such, approaches the performance of the amplifier when terminated with a 50 Ω resistor.

1.6.4. LOAD-INSENSITIVE DOHERTY PA

Chapter 5, provides the load-sensitivity analysis of a DPA. From these insights, it is understood that the loads of the main and peaking stages move in opposite directions when exposed to an impedance mismatched load. Consequently, the DPA can be made insensitive to ohmic load variation by adjusting its supply voltage and input drive of the main and peaking stages in a mirrored approach. Moreover, a low-loss TMN is employed to cancel out any reactive part of the load. Using the proposed concept, it can be shown that the ideal Doherty operation can always be recovered for any load mismatch. The simulated and measurement results demonstrate a constant output power and improved efficiency and linearity performance over the 2:1 VSWR range linearity.

1.6.5. LOAD-INSENSITIVE WIDEBAND DOHERTY PA

Chapter 6, presents an inverted Doherty power amplifier (IDPA) made load-insensitive up to 2:1 VSWR across its fractional (≈ 11 %) bandwidth with an output power combining network including an embedded load-impedance sensor. To correct for load variation, a low-loss tunable resonator (TR) is used to resonate out any reactance and to offer a close to ohmic load to the main and peaking stages at the center frequency of operation. At off-center frequencies, the TR offers a purely ohmic load to the main stage while a digitally adjustable phase shifter is used to align the main and peaking stage's current summation in the output power combining network. To handle the ohmic load variation, the main and peaking stage supply voltages, and input drives are adjusted to recover the Doherty

output power and efficiency and obtain a comparable performance as in the 50 Ω nominal loading case across the bandwidth. To implement the control of these techniques, a wideband impedance sensor is proposed that uses the orthogonality of incident and reflected waves and requires only four peak detectors. As proof of principle, a prototype 850- 950 MHz IDPA featuring the proposed correction technique, the impedance sensor, and the control loop has been implemented as a PCB demonstrator. Measurement results show that the IDPA can maintain constant output power with a tolerance of only ± 0.2 dB while improving the drain efficiency and linearity across the entire fractional bandwidth (11 %) for a VSWR range of 2:1.

1.6.6. ACTIVE LOAD CONTROL TO ENHANCE THE PA PERFORMANCE ACROSS VSWR CONDITIONS

In chapter 7, an alternative PA correction technique is introduced. It only relies on the active devices of three independently controlled PA stage(s) to recover from load mismatch, without needing any other circuit adjustment. The primary goal of this technique is to achieve a load-insensitive PA that is compatible with higher output powers and fast-changing load conditions. For this purpose, it utilizes a main PA, two auxiliary PAs, and a coupler. By adjusting the input drive levels of these three PAs, it can recover the output power and, to a great extent, the efficiency of the main PA even when exposed to 2:1 VSWR mismatch conditions. When connected to 50 Ω loading, only the main PA is active; for a load impedance below or above 50 Ω, besides the main amplifier, one of the auxiliary PAs needs to be activated. The power generated by the auxiliary PA adds in phase to the output power of the main PA, allowing the output power to be constant at the expense of a minor efficiency penalty.

1.6.7. CONCLUSION & FUTURE WORK

Chapter 8 discusses and summaries the contributions of this dissertation. Followed by recommended directions for future research on the topic of load-insensitive power amplifiers.

2

WIRELESS SIGNALS AND SYSTEMS

2.1. INTRODUCTION

This chapter discusses the key ingredients and aspects of 5G/6G networks—specifically, wireless signals such as OFDM and wireless system architectures like SISO and MIMO, focusing on their impact from a power amplifier (PA) perspective. As the use of wide-band, complex modulated signals (e.g., OFDM) with high-order constellations (e.g., 256, 1k, and 4k) becomes increasingly prevalent, the demands on RF front-ends, particularly the PA, for linearity and efficiency intensify. Additionally, the shift towards multi-input-multi-output (MIMO) architectures in 5G and the anticipated 6G systems aims to enhance link budgets through techniques such as beam-forming and multi-path transmission, which also significantly raise the system hardware complexity.

Moreover, the deployment of densely packed antenna elements, as seen in 5G base stations, and antennas exposed to environmental changes, such as those in mobile handsets, introduce dynamic changes in load impedance, which can impair PA performance unless countermeasures are applied. Furthermore, it highlights that traditional digital pre-distortion (DPD) solutions become impractical in addressing the load sensitivity of MIMO systems. This underscores the need for load-insensitive or resilient PAs capable of maintaining performance across changing VSWR conditions, allowing them to function within specifications, even when their DPD's are only trained for the constant nominal loading condition.

This chapter delves into the wireless signals and architectures utilized in current and future network generations, examining the specific demands they place on power amplifiers regarding error vector magnitude (EVM), adjacent channel power ratio (ACPR), and load resilience.

2.2. WIRELESS SIGNALS

Shannon's law states that the capacity (C) of a wireless channel is finite (2.1) and depends on the available bandwidth (Hertz) and the signal-to-noise ratio (SNR).

$$C = BW \log_2(1 + SNR) \tag{2.1}$$

From (2.1) it is evident that to meet the growing data rate demand (see Fig. 1.1), the channel capacity of a wireless system needs to be augmented by either increasing the bandwidth or increasing the modulation order of the signals used. Consequently, the signals in these systems must be spectral efficient and resilient to multipath fading, inter-symbol interference (ISI), frequency selective fading, and provide some adaptability to changing channel conditions without requiring complex equalization filters. Moreover, the signals need to be compatible with various standards 3G/4G/5G/6G, and be adaptable in bandwidth. Although more bandwidth is available at very high frequencies (e.g., mm-wave bands [35]), there is growing interest in utilizing the low-band (up to 7 GHz) and upcoming mid-band (up to 20 GHz) spectrum to benefit from lower path losses, and avoid the need of using the more power-hungry power-hungry millimeter-wave frequency bands.

2.2.1. OFDM

A waveform technology that can meet the requirements mentioned above is orthogonal frequency division-multiplexing (OFDM) [36]. Namely, OFDM allows the simultaneous use of multiple modulated subcarriers with minimal interference, which is visualized in the spectrum Fig. 2.1.

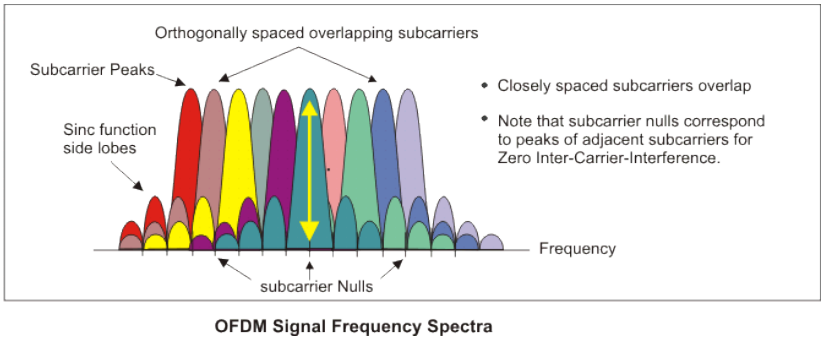

Figure 2.1. Concepts of orthogonal frequency division-multiplexing and 802.11 wireless local-area network [36].

PA requirements: Spectrally efficient signals like OFDM have two characteristics: first, the average radiated power is much lower than their peak power (e.g. 10 dB less in OFDM signal [37]), and second, they require high linearity from the wireless system and its components (e.g., the power amplifier) to avoid nonlinear distortion and spectral spreading. This demands a power amplifier to operate in back-off, yielding low efficiency. To overcome this performance degradation, efficiency enhancement techniques like supply modulation [38] or load-line modulation (e.g. Doherty) [39, 40] can be employed.

When having headroom in the SNR (see eq. 2.1) the modulation order of the communication signal can be increased to enhance data capacity. However, also this demands higher signal quality and, thus, also a further increase of the linearity requirements of the

transmitter and receiver in terms of error vector magnitude (EVM) and adjacent power rejection ratio (ACPR), which are explained below.

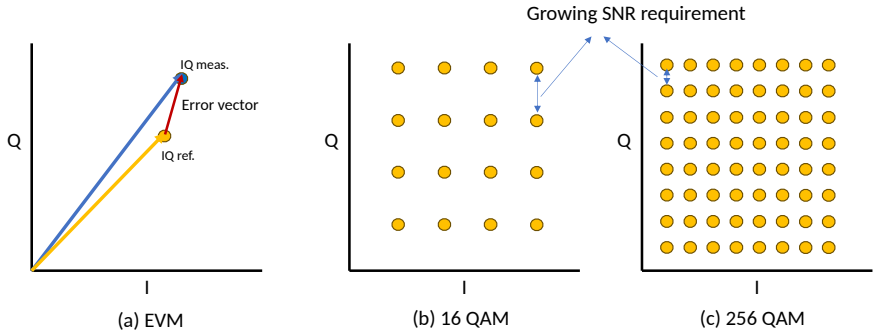

Figure 2.2. EVM (a) is a measure of the normalized error vector of the IQ reference and measured signal. b) a 16-QAM modulated signal, and the growing SNR requirement, when going to c) a higher order modulation, here a 64-QAM signal constellation is shown.

EVM

Modulation quality is defined by the difference between the measured carrier signal and a reference signal, which can be expressed as error vector magnitude (EVM) error vector magnitude (EVM) (see Fig. 2.2(a)). The EVM is a measure of the normalized difference between the ideal symbols and the measured symbols after equalization (see Fig. 2.2(a)) [41]. The EVM requirement specification for 5G NR for various modulation schemes is given in the Tab. 2.1.

ACLR

The adjacent channel leakage ratio (ACLR) is defined as the ratio of the filtered mean power centered on the assigned channel frequency to the filtered mean power centered on an adjacent channel frequency. As shown in Fig. 2.3, the ratio of the square filtered adjacent channel power to the main channel power needs to be less than -45 dB[41] for base station transmitters.

Table 2.1. The 3GPP TS 38.101-1 EVM requirements for various 5G modulation schemes

Modulation	EVM %
QPSK	17.5
16 QAM	12.5
64 QAM	8.5
256 QAM	3.5

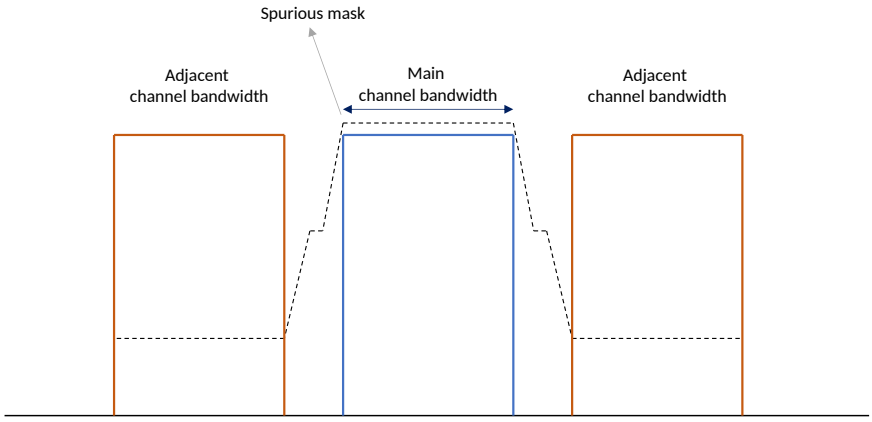

Figure 2.3. Spurious emission mask for adjacent channel leakage ratio (ACLR) .

2.3. WIRELESS SYSTEM ARCHITECTURES

As explained in section 2.2, radio frequency bandwidth is a scarce resource specially for the wide coverage lower GHz frequencies and needs to be used efficiently across the network. Therefore, network operators reuse frequencies in a hexagonal grid network, as shown in Fig. 2.4.

For dense urban networks, smaller wireless cells can be used, but this increases the number of base station locations, and acquiring new base station sites in densely populated neighborhoods comes with high real estate costs and the handling of many regulations. Moreover, wireless cells require a power plug connection and fiber optic or mm-wave point-to-point link to stream their data. To lower the need for adding many new base station site locations, over time, innovative wireless transceiver architectures have been adopted to enhance the capacity within the existing wireless cells.

2.3.1. SISO

A single-input single-output (SISO) is the simplest implementation form of a wireless communication system. It is mostly deployed in rural, sparsely populated locations to achieve network area coverage at low costs. This architecture has found widespread adoption in both base stations and handsets.

(SISO) BASE STATION

These older base stations (e.g., 3G) have one transmitter (TX) per sector antenna (no moving beams) Fig. 2.5. Consequently, the load impedance of their transmitters is fixed. Nevertheless, they include isolators for convenience or to enable full duplex operation of the RF front-end using a single antenna. In these (Marco) base stations, digital pre-distortion DPD (per transmitter line-up) is used to correct the imperfections in the high-power PAs and to operate them close to compression, improving efficiency without severely degrading the transmit signal quality. In these applications, the DPD is trained

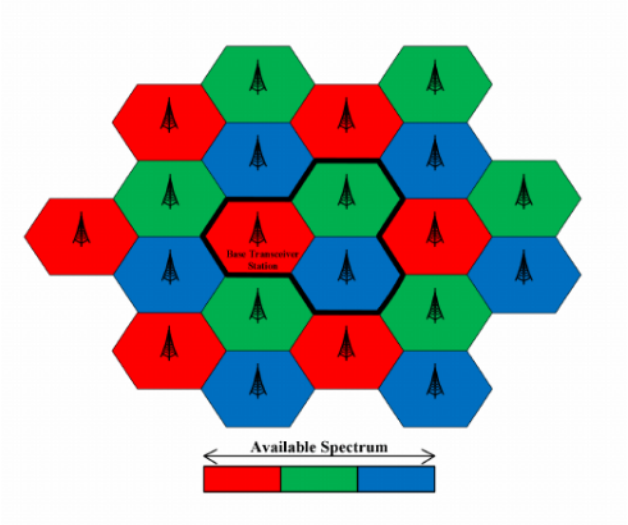

Figure 2.4. A single cluster comprising various base stations is highlighted in colour code. Interference is reduced by utilizing separate frequencies in adjacent cells.

for a fixed loading condition (typically 50 Ω).

(SISO) HANDSETS

In contrast to the SISO base station case, handsets do not experience constant loading for their PA(s) due to the user hand effect, which can change the impedance provided by the SISO antenna [12]. To handle these changes, in most commercial handsets, a very robust and conservatively designed PA is used and, thus, at best, offers only moderate efficiency. Alternatively, in more advanced handsets, a compact antenna tuner circuit is introduced between the PA and antenna [14–16]. This method is viable when the change in antenna impedance is constrained to a limited region of the Smith Chart. Also, some DPD, consisting of an observation receiver and a controller, is sometimes added to a handset to (pre-)correct the TX signal. However, such a DPD will guarantee the signal quality, but it cannot recover the penalty in PA performance due to power losses and efficiency drop for the non-optimum loading conditions.

2.3.2. MIMO

Multiple-input and multiple-output (MIMO) have evolved from single-input and single-output wireless communication technologies as a technique to improve the reliability and capacity of the network. It uses multiple transmitters and receivers with their antennas to simultaneously transmit and receive signals, as such increasing the number of signal paths/communication channels [43]. MIMO is a very generic term; it has been around for a few decades since its first introduction [44]. It also has evolved into several variants, including single-user MIMO (SU-MIMO), multi-user MIMO (MU-MIMO),

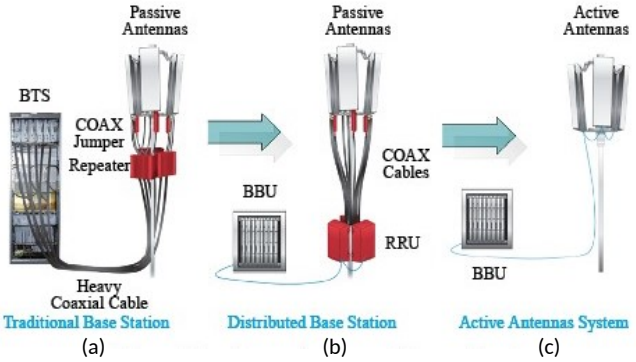

Figure 2.5. Passive antenna in traditional base station (3G) (a) and distributed base station (b) vs (c) active antenna (5G/6G) base stations [42]

cooperative MIMO (CO-MIMO), and massive MIMO. MU-MIMO has found widespread adaptation in Wi-Fi 4 (802.11n) and 4G LTE standards. The actual implementation of MIMO variants is very dependent on the number of (independent) antenna elements with their transmitters and receivers (see Tab. 2.2). Namely, when including beam forming functionality, more antenna elements are needed in a base station, yielding the massive multiple-input/multiple-output (mMIMO) systems, with an increasing number of transmitters (TX) and receivers (RX), e.g., 64, 128, or 256 configurations are used in 5G systems. When going to 6G, the number of TX/RX units for a base station can even rise to 1024 or beyond ("Extreme mMIMO") [45].

In mMIMO and Extreme mMIMO systems, to keep the side lob levels of the beams limited, the spacing between the individual antenna elements needs to be equal or below $\lambda/2$ (with λ being the wavelength of the center frequency), yielding mutual coupling between the closely spaced antenna elements. This coupling, depending on the signal conditions at these (neighboring) antennas, causes (changing) loading conditions for the individual PAs. As a result, in a beam steering system, the loading that a PA sees will dynamically change with the beam steering angle, resulting in effective VSWR conditions in the order of 2:1 [10]. It is evident that the strong increase in antenna elements also yields an exploding system complexity. To handle this complexity the following beamforming techniques are in use in wireless systems.

Table 2.2. Diversity and multiplexing with their impact on the capacity of wireless links

Method	Capacity (bits/sec)
SISO	$BW \cdot \log_2(1 + SNR)$
Diversity (1xN or Nx1)	$BW \cdot \log_2(1 + SNR \cdot N)$
Diversity (NxN)	$BW \cdot \log_2(1 + SNR \cdot N^2)$
Multiplexing (MIMO)	$N \cdot BW \cdot \log_2(1 + SNR)$

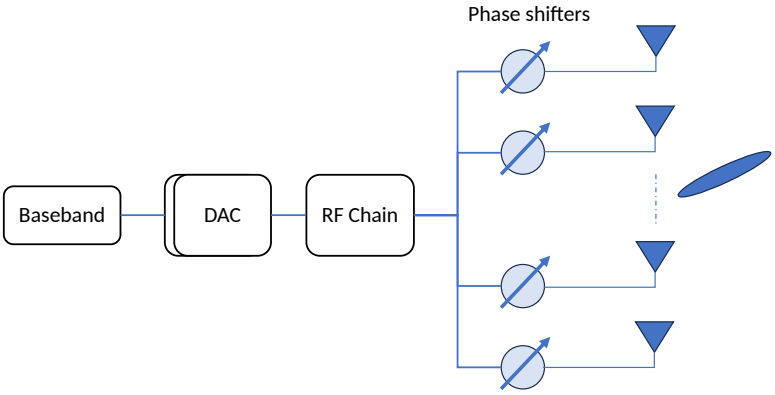

Figure 2.6. Analog beam forming architecture.

ANALOG BEAM FORMING

Base Stations: An analog beam-forming base station architecture is given in Fig. 2.6, which consists of N PAs or antennas driven by a single digital-based band unit. As such, all the antennas handle a copy of the phase-adjusted coherent signal. Pointing the transmitted signal in a specific direction yields the following capacity gain for such an antenna array.

$$C = BW \cdot \log_2(1 + SNR \cdot N_{\mathrm{TX}}) \tag{2.2}$$

A similar beam steering architecture can also be used on the receive side (N_{RX}) yielding.

$$C = BW \cdot \log_2(1 + SNR \cdot N_{\mathrm{TX}} \cdot N_{\mathrm{RX}}) \tag{2.3}$$

PA loading: due to the fact that all the antenna signals are coherent, the loading impedances offered to the PA's only change with the beam steering angle, since the beam steering action is aimed at tracking a user or a vehicle, its adjustment is relatively slow (much slower than the bandwidth of the communication signal itself), this allows the use of slower load adaptation techniques in the PA's (assuming that no isolators are used).

Handsets: due to the limited form factor of a handset, its maximum number of antennas is typically limited to 2 or 4 at most, resulting in a wide beam and low antenna gain.

PA loading: using an analog beam-former, all antenna signals are again phase coherent; further, since the beam needs to track a physical location, the beam steering will be similar to the base station case (relatively slow). Furthermore, the hand effect also depends on physical human reflexes events that are slow. Consequently, a slow adaptation of the PA for changing load conditions is allowed in this application scenario.

DPD Requirements: In an analog beam-forming system, the pre-distorter (if present) is included in the digital base-band domain; as such, a single DPD should linearize all the N PAs simultaneously. This lowers the hardware complexity, but the linearization is only sub-optimal as the system is essentially an under-determined problem [46], even when multiple observation receivers are added.

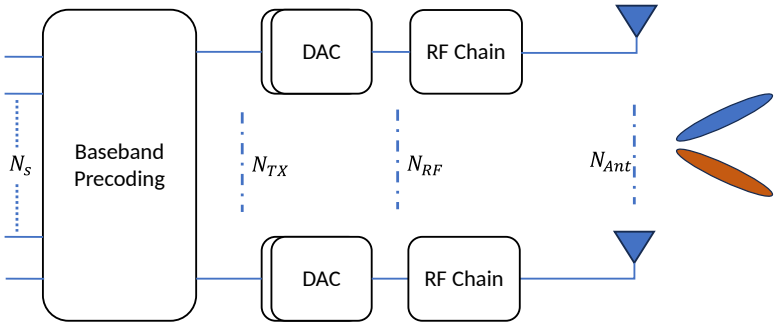

Figure 2.7. A digital beam forming architecture.

DIGITAL BEAM FORMING

A wireless system with a digital beam-forming architecture is shown in Fig. 2.7. It consists of a N_{Ant} transmit antennas radiating through N_{TX} independent transmit chains. The N_{TX} transmit chains allow the base station to communicate with N_{TX} user terminals simultaneously.

$$N_{\text{TX}} \leq N_{\text{RF}} \leq N_{\text{Ant}} \tag{2.4}$$

The resulting channel capacity is given by,

$$C = N_{\text{TX}} \cdot BW \cdot \log_2(1 + SNR) \tag{2.5}$$

This is possible due to the superposition of multiple beams in the digital domain (note that such a superposition would be very complicated and hardware-intensive to implement in a (modified) analog beamforming system).

As an example, let S_1 and S_2 represent signals to be received by the user terminals UT_1 and UT_2. A weight vector (W_{x}) is required for each UT to generate the two beams. The signal transmitted by each antenna in the base station is $S = S_1\ W_1 + S_2\ W_2$ [47]. The reflection coefficient of the antenna is now a function of S_1 and S_2 and their beam steering angles. The general N_{TX} beam transmitter (simplifying to narrow-band case, i.e., represented by a single frequency) can be understood from the following relation. Where, $c_{\text{N}_{\text{TX}}}$ denotes the complex symbols to be transmitted in N_{TX} beams. The weights for the complex symbols to be transmitted are given by the pre-coding matrix **W**. The pre-coding matrix for the beamforming case (analog beamforming, $N_{\text{TX}} = 1$) is reduced to a column

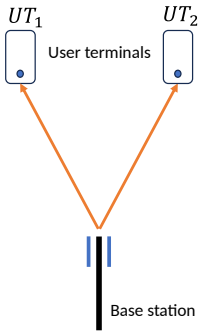

Figure 2.8. Digital beam forming architecture enables multi-user communication.

vector.

$$\begin{bmatrix} s_{1,N_{TX}} \\ s_{2,N_{TX}} \\ s_{3,N_{TX}} \\ . \\ s_{N_{Ant},N_{TX}} \end{bmatrix} = \begin{bmatrix} w_{1,1} & w_{1,2} & w_{1,3} & . & w_{1,N_{TX}} \\ w_{2,1} & w_{2,2} & w_{1,3} & . & w_{1,N_{TX}} \\ w_{3,1} & w_{3,2} & w_{3,3} & . & w_{3,N_{TX}} \\ . & . & . & . & . \\ w_{N_{Ant},1} & w_{N_{Ant},2} & w_{N_{Ant},3} & . & w_{N_{Ant},N_{TX}} \end{bmatrix} \begin{bmatrix} c_{1,N_{Ant}} \\ c_{2,N_{Ant}} \\ c_{3,N_{Ant}} \\ . \\ c_{N_{TX},N_{Ant}} \end{bmatrix}. \tag{2.6}$$

For the simple two transmitter case, different sub-scenarios can be considered here, namely

- S_1 and S_2 overlap or use the same frequency band. This scenario offers the highest data capacity, with more beams pointing in different directions, reusing the same frequency band. However, depending on the signal processing technique applied the signals at the antenna can be either coherent or non-coherent.
- S_1 and S_2 use different frequency bands (frequency multiplexing). In this scenario, the impedance's in the frequency band of S_1 will be dependent on the beam steering of S_1, and in the frequency band of S_2 dependent on the beam steering angle of S_2. This scenario has a lower data capacity but yields more relaxed system requirements for creating independent beams.

PA loading: in the first scenario, unwanted antenna coupling will yield a fast, dynamically changing load impedance vs. frequency if the signals are non-coherent, which is also subject to the beam steering parameters that change the composition of the transmit signal. Furthermore, if the signals are coherent, the active antenna impedance seen by the PA is similar to the analog beamforming scenario. In the second scenario, the effective loading impedance of the PA will change/jump from one frequency band to the next band, depending on the beam steering parameters used in these different bands.

DPD Requirements: In [48], fully digital beamforming is described, having a dedicated DPD unit for each transmitter. Consequently, the required complexity quickly scales

with the number of transmitters. As discussed, since such a structure can handle multiple beams simultaneously, it no longer has perfectly coherent signals that only have a phase shift with respect to each other. In contrast, it will be a "linear" superposition of coherent signals with varying superposition between subcarriers over the various antenna elements. Consequently, when the mutual coupling between the antenna elements is present, the correcting DPD will require a complex cross-over DPD [49], which can dramatically increase the overall power consumption. For example, it was shown in [50] that the DPD-related power consumption can exceed the overall PA power consumption, even when handling only two antennas. This is one of the key reasons why most practical mMIMO systems aim for simpler and less power-hungry DPD/system solutions, like having one beam per (sub)panel.

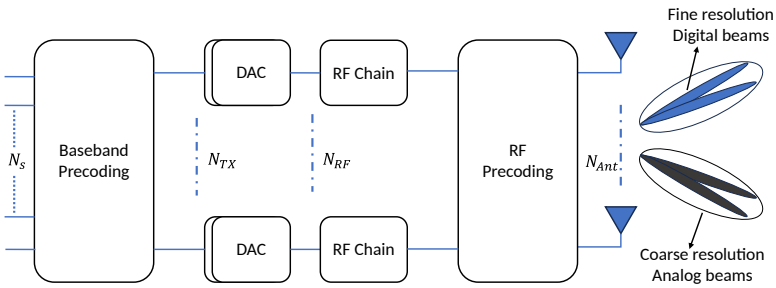

Figure 2.9. A hybrid beam forming architecture.

HYBRID BEAM FORMING

A hybrid beam forming architecture shown in Fig. 2.9 is a fusion of analog and digital beam forming architecture [51]. It consist of N_{RF} antennas and N_{TX} transmitters.

$$N_{\text{TX}} \leq N_{\text{RF}} < N_{\text{Ant}} \tag{2.7}$$

The total number of N_{RF}/ N_{Ant} antennas are responsible for coarse resolution analog beams (improving the directional gain), whereas, N_{TX} transmit chains perform the fine user selection using digital beams. The resulting channel capacity is given by,

$$C = N_{\text{TX}} \cdot BW \cdot \log_2(1 + SNR \cdot N_{\text{Ant}}) \tag{2.8}$$

PA loading: if the hybrid beam former operates similar to digital beam-former (see section 2.3), unwanted antenna coupling will yield a fast (from non-coherent beam) and slow (from analog beam), dynamically changing load impedances vs. frequency. For the frequency multiplexing scenario (also explained in section 2.3), the effective loading impedance of the PA will change/jump from one frequency band to the next band depending on the beam steering parameters used in these different bands.

DPD Requirements: The system, as shown in Fig. 2.10, will have a DPD engine per transmitter chain. The DPD engine needs to linearize all the N_{RF} PAs. However, this is

not achievable even with multiple observation receivers or a single observation receiver with analog superposition of all the transmitted signals [46]. Moreover the DPD engine also needs to handle the cross-talk from other transmitter chains in the multi-user multi-user communication link.

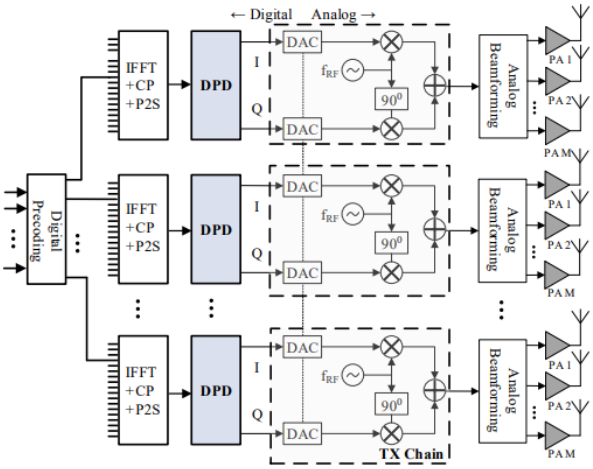

Figure 2.10. Digital-pre-distortion hybrid MIMO transmitter architectures [46].

2.4. CONCLUSION

From the OFDM signal discussion, it is clear that a wireless transmitter PA must be linear and offer high efficiency also in power back-off. These are already challenging tasks when dealing with perfect (constant) loading of the PA by the antenna. However, in practical wireless systems, the antennas interact with their physical surroundings and other nearby antennas (e.g., in MIMO systems), which affects the PA loading conditions when no isolators are included.

PA loading: when the power amplifier loading is influenced solely by coherent signals from neighboring antennas, only the beam-steering mechanism impacts the PA loading. Since these adjustments respond to physical movements, such as the position of a user or vehicle, the resulting changes tend to be gradual (typically spanning more than microseconds). In such scenarios, slower PA adaptation techniques are viable. Conversely, when PA loading is affected by coupling with non-coherent signals, rapid fluctuations in effective PA loading can occur, necessitating ultra-fast correction methods, if feasible.

In cases where slow PA adaptation techniques are appropriate, adjustments to PA bias conditions or the PA matching network can be made by modifying parameters or switching circuit elements in or out. For applications requiring rapid PA adaptation, it is often more effective to focus on solutions that address dynamic load mismatches by modifying the PA input signal conditions. This thesis will present examples of both adaptation approaches.

3

IMPEDANCE SENSORS

3.1. INTRODUCTION

Impedance sensing plays a crucial role in dynamically adjusting power amplifier settings to match the load for optimal power transfer, efficiency, and signal integrity. When the PA is tuned to match the impedance of its load accurately, it minimizes signal reflection and ensures that more power is delivered to the antenna, thereby enhancing transmission quality and reducing energy loss. Impedance sensors are especially valuable in systems with changing load conditions, such as those involving beam steering, where antenna coupling and varying impedance profiles can disrupt PA efficiency and linearity.

3.1.1. TYPES OF IMPEDANCE SENSORS

There are two primary types of impedance sensing techniques: active and passive.

ACTIVE IMPEDANCE SENSING:

Active techniques involve complex detection methods [31, 32], typically using frequency down-conversion mixer-based circuits to measure both the amplitude and phase of the reflected signal. This enables precise tracking of the complex impedance but is more challenging to implement in systems with wide modulation bandwidths, as it requires synchronization with high-frequency, modulated signals. Despite these challenges, active methods can provide highly accurate impedance measurements, which can be used in real-time control loops to optimize PA performance.

PASSIVE IMPEDANCE SENSING:

Passive techniques measure only the magnitude of the reflected signal and do not provide phase information in a direct way. These techniques are generally simpler to implement and do not require knowledge of the signal content, making them well-suited for high-bandwidth applications. However, passive methods typically require extensive calibration and computational resources [33, 34] to infer the complex impedance from the magnitude-only data.

In this chapter[1], two novel impedance sensing techniques are introduced. The first is a narrowband, two-tap, six-port network-based impedance sensor that leverages the orthogonality of incident and reflected waves. The second technique uses this same wave orthogonality principle within a network that also performs output power combining in an inverted Doherty power amplifier (IDPA), enabling easy integration into an IDPA with minimal overhead.

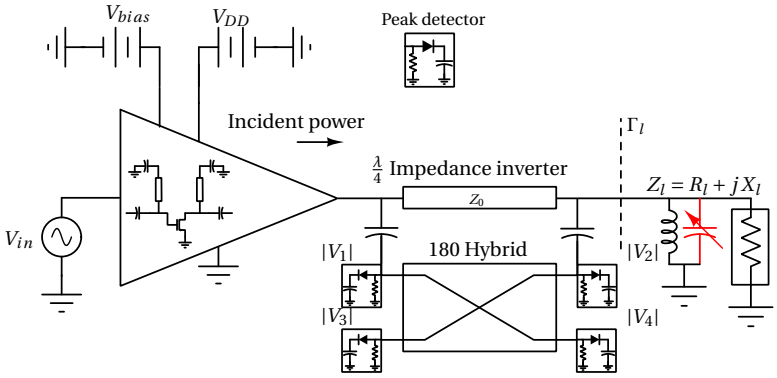

Figure 3.1. The PA with the proposed six-port reflectometer, comprising of an $\lambda/4$ impedance inverter, and capacitively coupled 180 hybrid with 4 peak detectors.

3.2. STANDALONE IMPEDANCE SENSOR

It is possible to determine the VSWR of the load by tapping the voltage swing at the two endpoints of a 90° transmission line as shown in Fig. 3.1. However, to determine the complex load, we also need to determine the phase of the reflected signal. In this work, we propose a phase detection concept that exploits the orthogonal property of two signals. Namely, if signals $x_1(t)$ and $x_2(t)$ are orthogonal to each other, the sum and difference of these two signals can be written as.

$$y_1(t) = x_1(t) + x_2(t) \tag{3.1}$$

$$y_2(t) = x_1(t) - x_2(t) \tag{3.2}$$

Using the orthogonal property (3.1) and (3.2) can also be written as

$$|y_1(t)|^2 = |x_1(t)|^2 + |x_2(t)|^2 \tag{3.3}$$

[1]This chapter consists of material previously published as the author submitted version from "G. D. Singh, et al. "An Inverted Doherty Power Amplifier Insensitive to Load Variation With an Embedded Impedance Sensor in Its Output Power-Combining Network". In: IEEE Trans. Microw. Theory Techn. (2023), pp. 1–15" and "G. D. Singh, et al. "A Low-Loss Load Correction Technique for Self-Healing Power Amplifiers Using a Modified Two-Tap Six-Port Network". In: IEEE Trans. Microw. Theory Techn. 69.9 (2021), pp. 4069–4081."

$$|y_2(t)|^2 = |x_1(t)|^2 + |x_2(t)|^2 \tag{3.4}$$

If we take the ratio of $|y_1(t)|^2$ and $|y_2(t)|^2$, we find,

$$\frac{|y_1(t)|^2}{|y_2(t)|^2} = 1 \tag{3.5}$$

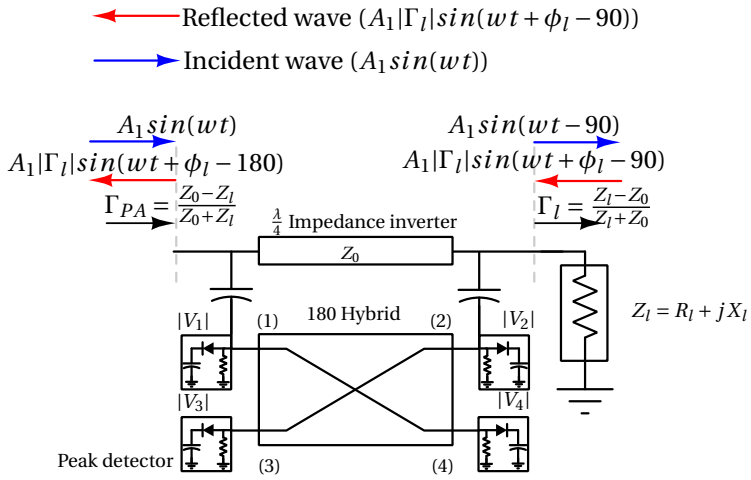

Figure 3.2. The proposed six-port reflectometer comprising an impedance inverter and weakly capacitive coupled 180°-hybrid with 4 peak detectors.

Any varying load impedance with an imaginary part will offset the orthogonal phase relation and the related ratio will no longer be equal to unity. Using this fact it is possible to determine the susceptance of the load. A simple method to realize the sum and difference of RF signals is the use of a 180° hybrid like a rat-race as shown shown in Fig. 3.1. Furthermore, the transmission-line-based rat-race hybrid couplers are very bulky for an integrated circuit implementation. This limitation can be overcome by using lumped equivalents of 90° transmission lines [52] and a rat-race hybrid [53] respectively.

The proposed six-port network-based impedance sensor's analytical solution is as follows. Let $A_1 \sin(wt)$ be the incident wave at the reference plane of the power amplifier (see Fig. 3.3) and let $A_1|\Gamma_l|\sin(wt+\phi_1-90)$ be the reflected wave. Where $|\Gamma_l|$ and ϕ_1 denote the reflected waves' magnitude and phase. The phase relation between the incident and the reflected wave due to the 90° transmission line at the PA and load reference planes are shown in Fig 3.2. Let port (3) and port (4) be the sum and difference ports of the hybrid. Even though only capacitive coupling is shown in Fig 3.2, the coupling can also be achieved using a resistive/inductive network. To maximize the power delivery to the load the coupling factor (C) is assumed to be very small, such that it will not affect the signal propagation in the 90° TL. For this condition the incident and reflected signals coupled at ports (1), (2), (3), and (4) are given by $CV_1\sin(wt+\alpha_1)$, $CV_2\sin(wt+\alpha_2)$,

$CV_3\sin(wt+\alpha_3)$, and $CV_4\sin(wt+\alpha_4)$. Normalizing the coupled signals at all the ports by a coupling factor (C) we get.

$$V_1\sin(wt+\alpha_1) = A_1\sin(wt) - A_1|\Gamma_1|\sin(wt+\phi_1) \tag{3.6}$$

$$V_2\sin(wt+\alpha_2) = -A_1\cos(wt) - A_1|\Gamma_1|\cos(wt+\phi_1) \tag{3.7}$$

$$\begin{aligned} V_3\sin(wt+\alpha_3) &= A_1[\sin(wt)-\cos(wt)] \\ &\quad -A_1|\Gamma_1|[sin(wt+\phi_1)+\cos(wt+\phi_1)] \end{aligned} \tag{3.8}$$

$$\begin{aligned} V_4\sin(wt+\alpha_4) &= A_1[\sin(wt)+\cos(wt)] \\ &\quad -A_1|\Gamma_1|[\sin(wt+\phi_l)-\cos(wt+\phi_l)] \end{aligned} \tag{3.9}$$

Rearranging the terms of (3.6), (3.7) ,(3.8) and (3.9) we can resolve V_1, V_2, V_3, and V_4 as follows

$$V_1^2 = (A_1 - A_1|\Gamma_1|\cos(\phi_1))^2 + (-A_1|\Gamma_1|\sin(\phi_1))^2 \tag{3.10}$$

$$V_2^2 = (-A_1 - A_1|\Gamma_1|\cos(\phi_1))^2 + (-A_1|\Gamma_1|\sin(\phi_1))^2 \tag{3.11}$$

$$\begin{aligned} V_3^2 &= (A_1 - A_1|\Gamma_1|(\cos(\phi_1)-\sin(\phi_1)))^2 \\ &\quad +(-A_1 - A_1|\Gamma_1|(\sin(\phi_1)+\cos(\phi_1)))^2 \end{aligned} \tag{3.12}$$

$$\begin{aligned} V_4^2 &= (A_1 - A_1|\Gamma_1|(\cos(\phi_l)+\sin(\phi_l)))^2 \\ &\quad +(A_1 + A_1|\Gamma_1|(\cos(\phi_1)+\sin(\phi_1)))^2 \end{aligned} \tag{3.13}$$

Taking the ratios V_1/V_2, and V_3/V_4, we get two independent equations (3.14) and (3.15), which have the unkowns $|\Gamma_1|$ and ϕ_1.

$$\frac{V_1}{V_2} = \sqrt{\frac{(1-|\Gamma_1|\cos(\phi_1))^2 + (|\Gamma_1|\sin(\phi_1))^2}{(1+|\Gamma_1|\cos(\phi_1))^2 + (|\Gamma_1|\sin(\phi_1))^2}} \tag{3.14}$$

$$\frac{V_3}{V_4} = \sqrt{\frac{(1-|\Gamma_1|(\cos(\phi_1)-\sin(\phi_1)))^2 + (1+|\Gamma_1|(\cos(\phi_1)+\sin(\phi_1)))^2}{(1-|\Gamma_1|(\cos(\phi_1)+\sin(\phi_1)))^2 + (1+|\Gamma_1|(\cos(\phi_1)-\sin(\phi_1)))^2}} \tag{3.15}$$

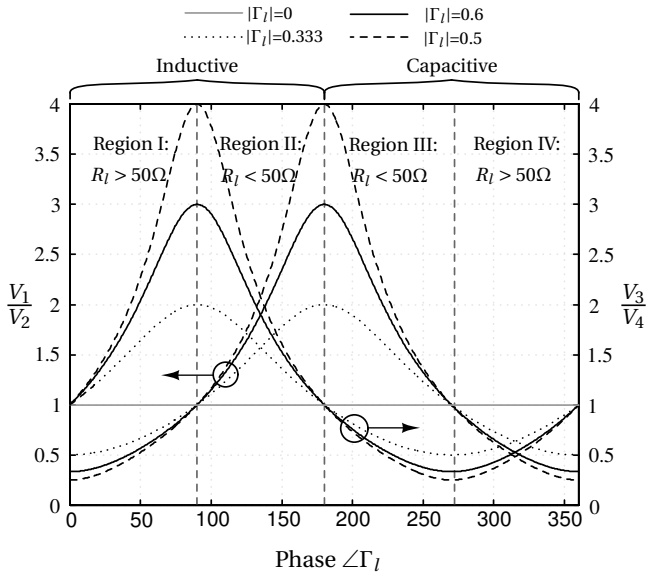

Figure 3.3. Analytical voltage ratios V_1/V_2 and V_3/V_4 for a given $|\Gamma_l|$/VSWR and phase angle (ϕ_l).

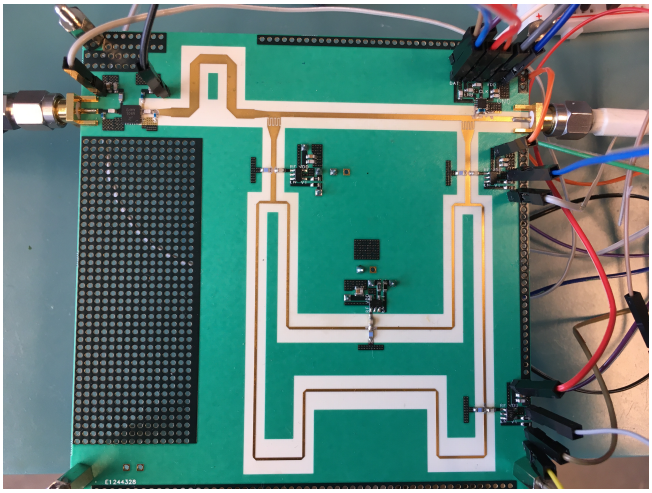

Figure 3.4. The realized PCB includes the 900 MHz LDMOS PA, the six-port reflectometer, and a tunable shunt resonator.

Consequently, if we know the magnitude ratios of V_1/V_2 and V_3/V_4, we can determine the applied load impedance. The analytical voltage ratios V_1/V_2 and V_3/V_4 plots for a given $|\Gamma_l|$/VSWR and phase angle (ϕ_l) are shown in Fig. 3.3. We can see that the points where the voltage ratio V_3/V_4 goes to unity relate to the points where the phase of the reflection coefficient is either 0° or 180°. Furthermore, close inspection of the ratios V_1/V_2, and V_3/V_4 reveals that they point to 4-regions. Namely, Region I: load > 50 Ω, and inductive ($V_1/V_2 < 1$, and $V_3/V_4 > 1$), Region II: load < 50 Ω, and inductive ($V_1/V_2 > 1$, and $V_3/V_4 > 1$), Region III: load < 50 Ω, and capacitive ($V_1/V_2 > 1$, and $V_3/V_4 < 1$), and Region IV: load > 50Ω, and capacitive ($V_1/V_2 < 1$, and $V_3/V_4 < 1$). Therefore, it can be concluded that the proposed six-port network provides the ability to determine the complex load by solving (3.14) and (3.15).

3.2.1. SIX-PORT REFLECTOMETER DESIGN

To validate the proposed impedance sensing concept. A prototype six-port reflectometer is implemented using a 50 Ω transmission line of length $\lambda/4$ (see Fig. 3.4). The transmission line at its two-end points is weakly coupled to a microstrip hybrid ring. The coupling capacitors are implemented using an interdigitated finger structure as shown on the PCB. They are sized to provide a coupling factor of -30 dB. The RF peak detectors used for measuring the RMS voltages are from analog devices, i.e. LTC5505-2. They provide a dynamic range of 40 dB [54]. The analog output voltages from the peak detectors are digitized using an ADC for readout.

3.2.2. MEASUREMENT RESULTS

To validate the performance of the fabricated impedance sensor, a calibrated Maury (MT982E) load tuner is used to present varying load impedances. Fig. 3.5(a), and 3.5(b) shows the measurement results of voltage ratios V_3/V_4 and V_1/V_2 of the six-port network. For reference analytically computed voltage ratios are also added. The input power to the PA is set to 9 dBm at 900 MHz. The $|\Gamma|$ are set to 0.0, 0.1, 0.2, and 0.333, while the phase angles are swept from 0° to 360° in steps of 45°. It can be observed that the measurement results show good agreement with the analytical results. The phase cross-over points of V_3/V_4 ratio are aligned with respect to the theory. However, there is a little misalignment in the phase crossover of V_1/V_2 ratio at 270^o. From Fig. 3.5(a), and 3.5(b), (input power = 9 dBm) and Fig. 3.6(a), and 3.6(b) (input power = 16 dBm) we observe that the voltage ratio exhibit a gain error that depends on the input driving level. These deviations in phase crossover and gain of the voltage ratio are traced back to component tolerances, board parasitics, and gain variation of the peak detectors. A common technique to overcome these deviations is to calibrate the peak detectors for different power levels or the impedance sensor using a look-up table.

Furthermore, it is also possible to use this impedance sensor to independently compensate for the reactance and resistance part of the presented load impedance. In Fig. 3.6(a) the presented reactance part of the load is compensated using a tunable shunt resonator. It can be observed that the voltage ratio V_3/V_4 goes to unity when the reactance part of the load is compensated. Whereas the resistive part of the load changes only relatively due to matching to the ohmic line (see Fig. 3.6(b)).

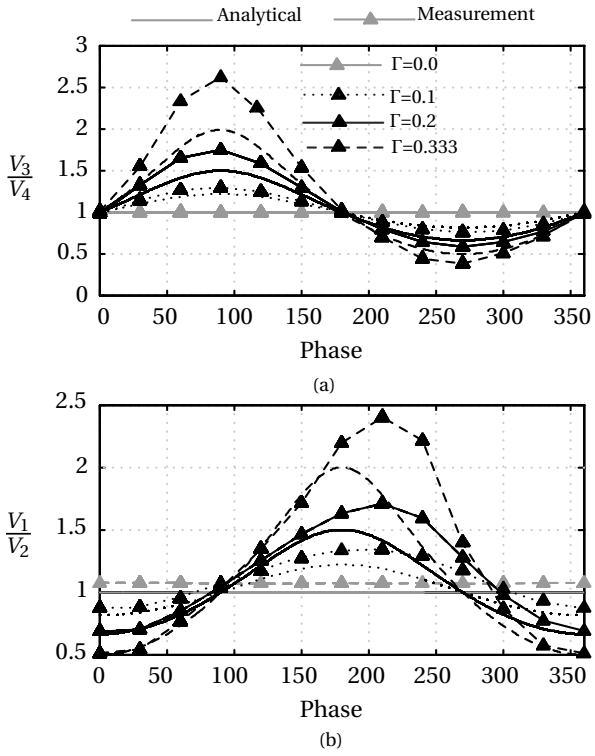

Figure 3.5. Six port reflectometer analytical and measured results at 9 dBm input power of the PA when operating at 900 MHz. (a) V_3/V_4 ratio points to the phase of the VSWR and (b) V_1/V_2 points to the VSWR.

3.3. WIDEBAND IMPEDANCE SENSOR

In the prior section, a great deal of attention was given to the standalone impedance sensor. However, it comes with considerable overhead in terms of implementation area, even though it can be integrated on a chip. It is highly desirable to be able to embed the sensing technique in the output matching network or power combiner to minimize the area overhead. Moreover, these impedance sensors need to be operational across wide RF frequencies. To meet these requirements this section introduces a wideband impedance sensor, that can be embedded in the output power combining network (OPCN) of an inverted Doherty power amplifier (IDPA).

The complex varying load impedance ($Z_L = R_L + jX_L$) requires two independent equations to determine its resistive (R_L) and reactance part (X_L). The proposed impedance sensor (see Fig. 3.7) uses the orthogonality of incident and reflected waves. Only four voltages need to be sensed, which can be achieved using peak detectors, and resistance-based voltage combining networks (see Fig. 3.7). Equivalent capacitive or inductive voltage-combining networks can also replace the here proposed resistive networks. The

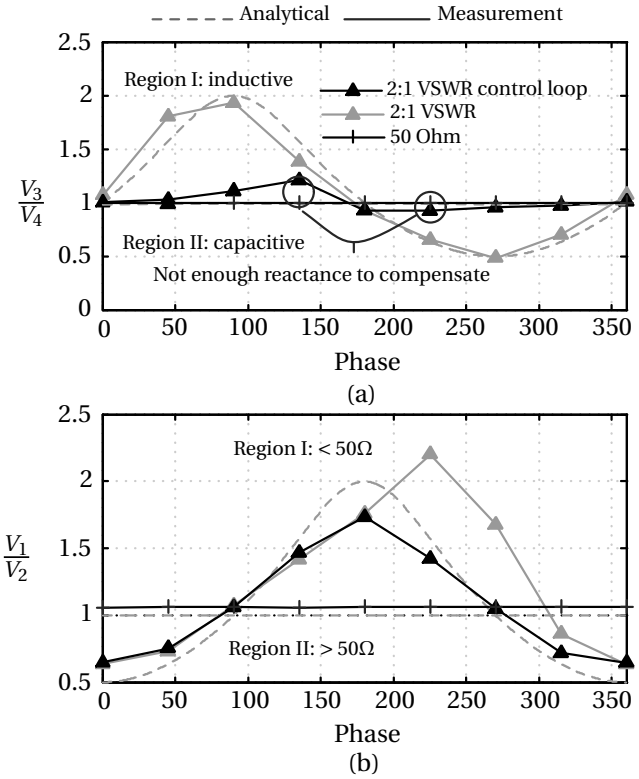

Figure 3.6. Six-port reflectometer results when PA is subjected to 50 Ω and loads on a 2:1 VSWR circle (a) V_3/V_4 points to load reactance (Region I: (> 1) is inductive and Region II: (< 1) is capacitive) (b) V_1/V_2 points to the VSWR(Region II: (< 1) higher than 50 Ω and Region I: (> 1) lower than 50 Ω.

organization of this section is as follows. First, we demonstrate the concept at the center frequency. Second, the proposed concept is extended to wide-band operation by analyzing the sensor-voltage relations for a given operating frequency. As such, the theoretical peak detector voltage ratios for an applied load will be derived for both the center-frequency and the wide-band case. To simplify the analysis, the following assumptions have been made.

- The output power combining network of an inverted Doherty power amplifier [55] is restricted to the three transmissions line configuration as shown in Fig. 3.7.
- It is assumed that the peak stage is in its off-state, and as such, it does not provide any RF output current ($I_P = 0$).
- The resistance-based combining network has a very high impedance, so t does not affect the power combiner operation and any current flowing through it is ignored.

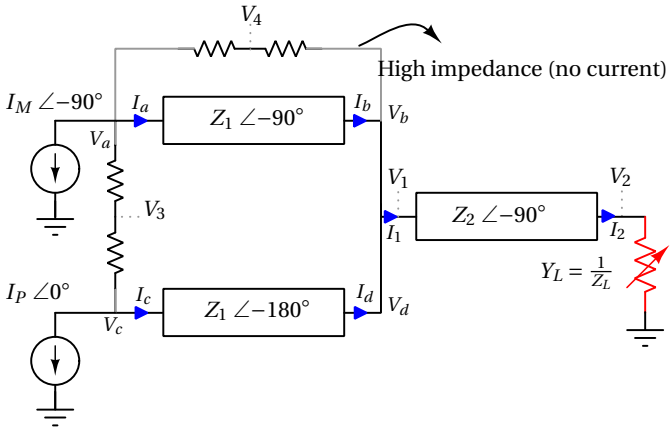

Figure 3.7. Schematic of the wideband impedance sensor to analyze the dependence of voltage ratios $|V_1/V_2|$ and $|V_3/V_4|$ on Z_L and operating frequency.

CENTER-FREQUENCY OPERATION

$$\begin{bmatrix} V_x \\ I_x \end{bmatrix} = \begin{bmatrix} \cos(\beta l) & jZ_{xy}\sin(\beta l) \\ j(1/Z_{xy})\sin(\beta l) & \cos(\beta l) \end{bmatrix} \begin{bmatrix} V_y \\ I_y \end{bmatrix}. \tag{3.16}$$

For the center frequency (0.9 GHz) operation, when only the main PA is active, using the schematic in Fig. 3.7 and the ABCD matrix for a lossless transmission line [56], (3.16) with $\beta l = \pi/2$, we can find the expression for the voltages V_1, V_2, V_3, and V_4. Taking the subsequent ratios of V_1/V_2 and V_3/V_4 the following equations are derived.

$$\frac{V_1}{V_2} = -j\frac{Z_L}{Z_2} \tag{3.17}$$

$$\frac{V_3}{V_4} = \frac{Z_L + jZ_2^2/Z_1}{Z_L - jZ_2^2/Z_1} \tag{3.18}$$

Substituting ($Z_L = R_L + jX_L$) in (3.17) and (3.18) and taking the magnitude we get,

$$\left|\frac{V_1}{V_2}\right| = \frac{\sqrt{R_L^2 + X_L^2}}{Z_2} \tag{3.19}$$

$$\left|\frac{V_3}{V_4}\right| = \frac{\sqrt{R_L^2 + (X_L + Z_2^2/Z_1)^2}}{\sqrt{R_L^2 + (X_L - Z_2^2/Z_1)^2}}. \tag{3.20}$$

From (3.19) and (3.20), it can be observed that the ratio $|V_1/V_2|$ is sensitive to both R_L and X_L, i.e., $|\Gamma|$, whereas $|V_3/V_4|$ is only sensitive to X_L, i.e., $\angle\Gamma$. The $|V_3/V_4|$ ratio becomes

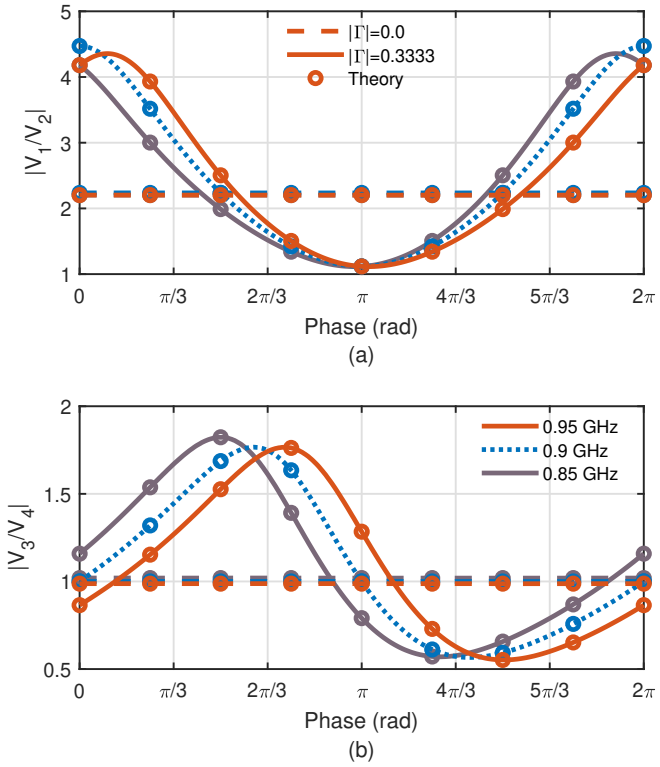

Figure 3.8. The theoretical (circles) and simulated (solid and dotted lines) voltages ratio at three operational frequencies 0.85 GHz, 0.9 GHz (center frequency), and 0.95 GHz. (a) $|V_1/V_2|$ pointing to the $|\Gamma|$ and (b) $|V_3/V_4|$ pointing to the $\angle\Gamma$ for $|\Gamma|$ of 0.0 (dashed line) and 0.3333 (solid and dotted lines) as a function of the phase of Γ.

unity when $X_L = 0$, for any value of R_L (due to the orthogonal relation between Z_L and jZ_2^2/Z_1). The theoretical and simulated (using the schematic in Fig. 3.7) magnitude of these voltages ratios are plotted in Fig. 3.8 for $|\Gamma|$ set to {0.00, 0.33} with $\angle\Gamma$ swept from 0° to 360°, with the transmission lines impedance set to $Z_1 = 1/Y_1 = 20\,\Omega$ and $Z_2 = 1/Y_2 = (25Z_1)^{0.5}$. It can be seen that when the IDPA is matched to the load, i.e., 50 Ω ($|\Gamma| = 0$). The voltage ratios $|V_1/V_2|$ (see Fig. 3.8(a)) and $|V_3/V_4|$ (see Fig. 3.8(b)) are constant across all the phase angles. The voltage ratio $|V_1/V_2|$ settles at 2.24 while $|V_3/V_4|$ settles at 1.00. It can be observed from (3.17) and (3.18) that the $|V_1/V_2|$ is dependent on transmission line impedance Z_2, while the $|V_3/V_4|$ ratio is independent of the transmission line impedance since $Z_2 = (25Z_1)^{0.5}$. Using (3.17) and (3.18), it can be concluded that by only sensing the magnitude of these four voltages and taking their ratios ($|V_1/V_2|$, $|V_3/V_4|$), the magnitude and phase of the applied load reflection coefficient can be determined.

WIDE-BAND OPERATION

Also, in the wide-band analysis, the OPCN transmission line model in Fig. 3.7 is used together with the transmission line ABCD matrix [56] (3.16). Furthermore, in this case βl is formulated as $0.5\pi(f/f_0)$ and $\pi(f/f_0)$ for transmission line lengths of $\lambda/4$ and $\lambda/2$ respectively. Consequently, we can determine the voltages V_1, V_2, V_3, and V_4 and subsequently the voltage ratios of interest: V_1/V_2 and V_3/V_4 yielding,

$$\frac{V_1}{V_2} = \frac{1}{\cos(\frac{\pi}{2}\frac{f}{f_0}) + \mathrm{j}Y_L Z_2 \sin(\frac{\pi}{2}\frac{f}{f_0})} \tag{3.21}$$

$$\frac{V_3}{V_4} = \frac{V_{34N}}{V_{34D}} \tag{3.22}$$

where V_{34N} and V_{34D} are given in (10) and (11),

$$\begin{aligned} V_{34\mathrm{N}} = \frac{V_2}{V_1}\left(\cos(\frac{\pi}{2}\frac{f}{f_0}) + \cos(\pi\frac{f}{f_0})\right) + \mathrm{j}Z_1\sin(\frac{\pi}{2}\frac{f}{f_0})\Big(\mathrm{j}Y_2 sin(\frac{\pi}{2}\frac{f}{f_0}) \\ + Y_L\cos(\frac{\pi}{2}\frac{f}{f_0}) + \mathrm{j}Y_1\frac{V_2}{V_1}\tan(\pi\frac{f}{f_0})\Big) + \frac{V_2}{V_1}\tan(\pi\frac{f}{f_0})\sin(\pi\frac{f}{f_0}) \end{aligned} \tag{3.23}$$

$$\begin{aligned} V_{34\mathrm{D}} = \frac{V_2}{V_1}\left(1 + \cos(\frac{\pi}{2}\frac{f}{f_0})\right) + \mathrm{j}Z_1\sin(\frac{\pi}{2}\frac{f}{f_0})\Big(\mathrm{j}Y_2\sin(\frac{\pi}{2}\frac{f}{f_0}) \\ + Y_L\cos(\frac{\pi}{2}\frac{f}{f_0}) + jY_1\frac{V_2}{V_1}\tan(\pi\frac{f}{f_0})\Big) \end{aligned} \tag{3.24}$$

When $f = f_0$, i.e., at the center frequency of operation (3.21) and (3.22) can be reduced to (3.19) and (3.20), therefore, as explained in the former section (III.A) the voltage ratios ($|V_1/V_2|$ and $|V_3/V_4|$) point to $|\Gamma|$ and $\angle\Gamma$ respectively. The theoretical and simulated magnitude of these voltages ratios ($|V_1/V_2|$ and $|V_3/V_4|$) at three operational frequencies 0.85 GHz, 0.9 GHz, and 0.95 GHz are shown in Fig. 3.8(a) and 3.8(b), for $|\Gamma|$ set to {0.00, 0.33} with $\angle\Gamma$ swept from 0° to 360°. It can be observed that the voltage ratio pattern at the off-center frequency closely resembles the voltage ratio pattern at the center frequency. Furthermore, it can be concluded that by using (3.21) and (3.22), only sensing the magnitude of these four voltages and taking their ratios ($|V_1/V_2|$, $|V_3/V_4|$), and using the operation frequency (f/f_0) information along with the designed OPCN impedance $Z_1 = 1/Y_1$. The magnitude and phase of the applied load ($Z_L = 1/Y_L$) can be determined.

3.3.1. WIDEBAND IMPEDANCE SENSOR DESGIN

To verify the proposed wideband impedance sensor concept. A prototype wideband IDPA is designed to operate at a center frequency of 900 MHz with a fractional bandwidth of 11 %. The IDPA has an an optimum load impedance ($R_{L_{opt}}$) close to 25 Ω. Consequently, the transmission lines impedances are set to $Z_1 = 1/Y_1 = 25\,\Omega$ and $Z_2 = 1/Y_2 = (25Z_1)^{0.5} = 25\,\Omega$. The impedance sensor voltages V_1, V_2, and V_4 are extracted using capacitive coupling at the indicated points of the 90° transmission lines (see Fig. 3.9).

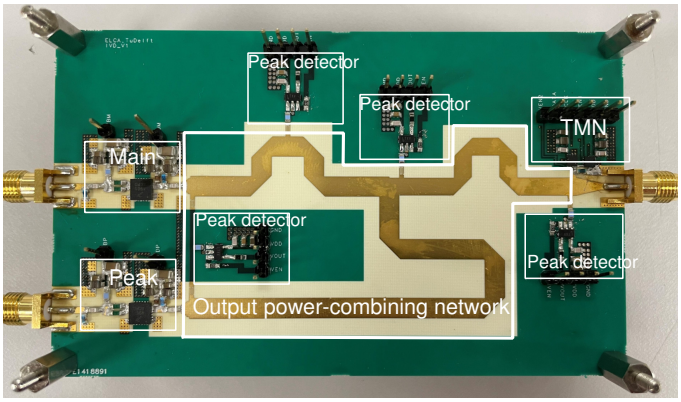

Figure 3.9. Schematic of the wideband impedance sensor to analyze the dependence of voltage ratios $|V_1/V_2|$ and $|V_3/V_4|$ on Z_L and operating frequency.

The sensing voltage V_3 is obtained by capacitive coupling of the main and peaking stage output nodes and combining them using a transmission line (see Fig. 3.9). The coupling capacitors are implemented using an inter-digitated finger structure on the PCB, as shown in Fig. 3.9. They are sized to provide a coupling factor of -30 dB. The RF peak detectors for measuring the RMS voltages are from analog devices, i.e., LTC5505-2. They provide a dynamic range of 40 dB. Moreover, the analog output voltages from the peak detectors are digitized using an ADC for readout.

3.3.2. MEASUREMENT

CENTER FREQUENCY

Fig. 3.10(a) and 3.10(b) compare the actual measurement and idealized simulation results of voltage ratios $|V_1/V_2|$ and $|V_3/V_4|$ of the proposed embedded impedance detector at 900 MHz. $|\Gamma|$ is set to 0.00, and 0.33, while the phase angles are swept from 0° to 360° in steps of 45°. The measurement results show excellent agreement with the idealized simulation results. The phase crossover points of the $|V_3/V_4|$ ratio is aligned with respect to the theory. However, there is a slight misalignment in the phase crossover points of the $|V_1/V_2|$ ratio at 90° and 270°. The deviations between measurement and idealized simulated results can be traced back to gain variation of the peak detectors, component tolerances, as well as, PCB parasitics.

WIDE-BANDWIDTH OPERATION

Fig. 3.11(a) and 3.11(b) show the measurement results of voltage ratios $|V_1/V_2|$ and $|V_3/V_4|$ of the proposed embedded impedance sensor from 850 −950 MHz. $|\Gamma|$ is set to 0.00, and 0.33, while the phase angles are swept from 0 −360° in steps of 45°. It can be observed that the voltage ratio pattern resembles the center frequency voltage ratio pattern (section 3.3). Therefore, these voltage ratios can determine loading impedance across a

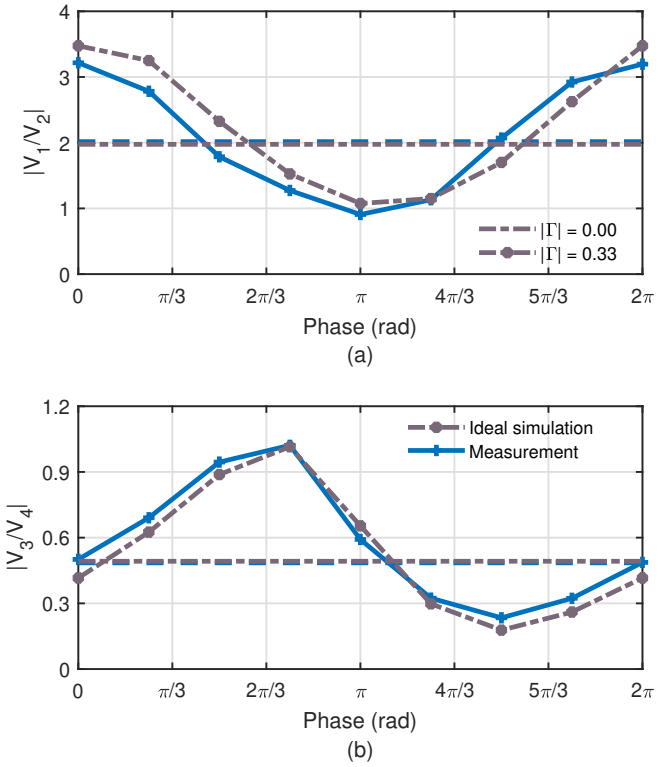

Figure 3.10. Embedded impedance sensor idealized simulation and measurement results of the IDPA when operating at 900 MHz with 22 dBm output power. The voltage ratios vs. phase ($\angle\Gamma$) (a) $|V_1/V_2|$ and (b) $|V_3/V_4|$.

wider bandwidth.

3.4. CONCLUSION

In this chapter, the concept of an impedance sensor was demonstrated. Passive impedance sensing methods are preferred over active methods to meet the large modulated signal bandwidth requirement. However, they work at narrower RF bandwidth and require extensive calibration/computation. To relax these limitations two novel passive impedance sensors using the orthogonal summation of the incident and reflected wave were introduced. First, a standalone impedance sensor requires just two equations to determine the presented load impedance. Second, a wideband impedance sensor that can be embedded in the OPCN of an IDPA to minimize the implementation overhead and be operational across a wider RF bandwidth. The working principle of the impedance sensor is validated using theory/simulation/measurement data. In terms of applications the proposed impedance sensors are suitable for phased array/mobile handset.

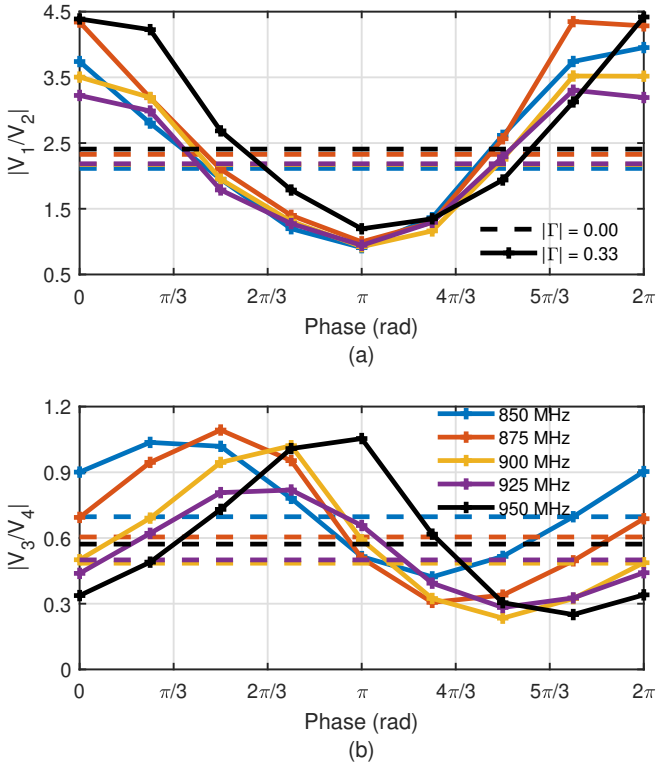

Figure 3.11. The measurement results of the wideband embedded impedance sensor from 850 MHz-950 MHz. The voltage ratios vs. phase ($\angle\Gamma$) (a) $|V_1/V_2|$ and (b) $|V_3/V_4|$.

4

LOAD-INSENSITIVE CLASS-B POWER AMPLIFIER

4.1. INTRODUCTION

In wireless base station applications, the use of an isolator is favored. Namely, it provides the optimum impedance to the PA core and as such can preserve TX linearity over the frequency band of interest (typically 5 - 40% depending on the VSWR specification). However, phased arrays require an isolator for each PA section in the chain, this comes at high costs, low integration due to a larger form factor, as well, extra insertion loss. Moreover, the reflected power due to impedance mismatch needs to be dissipated in the isolator-connected load. To avoid the isolator in small form-factor mMIMO applications balanced PAs have been proposed. The balanced PA, when considered from the antenna port behaves like an isolator for small signal operation. However, from the PA point of view, it does not provide any suppression of the load mismatch. Therefore at large signal conditions depending on the VSWR, the individual branch PA will hit voltage or current saturation, as shown in Fig. 4.1 respectively. Consequently, the balanced PA needs to be operated at power back-off to preserve its linearity, which comes with an efficiency penalty. In contrast, a tunable matching network, at least in theory always provides the optimum loading conditions for the transistor output stage. Consequently, ideally, this solution would not yield any efficiency or linearity penalty. However, being able to match any point on the Smith chart comes in practical cases, when using network elements with constrained tuning range, with high-Q conditions in the PA matching network (TMN-Q). This degrades the achievable insertion loss and bandwidth of the TX (transmitter) lineup while increasing the voltage stress for the tunable elements. [1]

Some solutions have been proposed to handle load mismatch while omitting high TMN-Q conditions, e.g. in [57] a supply voltage adaptation method for $> 50\ \Omega$ in combination with an adjustable pre-driver was proposed to prevent collector voltage saturation. This technique was extended further in [58] to include also $< 50\ \Omega$ cases. How-

[1] This chapter consists of material previously published as the author submitted version from "G. D. Singh, H. M. Nemati, and L. C. N. de Vreede. "A Low-Loss Load Correction Technique for Self-Healing Power Amplifiers Using a Modified Two-Tap Six-Port Network". In: IEEE Trans. Microw. Theory Techn. 69.9 (2021), pp. 4069–4081.

ever, both of these works assume the impedance variation to be only along the real axis. Moreover, to recover the PA performance which is strongly linked to the phase of the load impedance, the use of an adaptive tunable network or a phase shifter for maintaining the optimum phase at the output was proposed in [59].
In contrast, this chapter provides full-range impedance sensing (taken from Chapter 2) and PA correction within a given VSWR limit while maintaining low-Q matching conditions in the TMN. This is achieved by using a combination of susceptance compensation, supply voltage adjustment, and gain/input drive correction. It will be theoretically shown that by using these techniques the lowest insertion loss and voltage stress can be achieved.

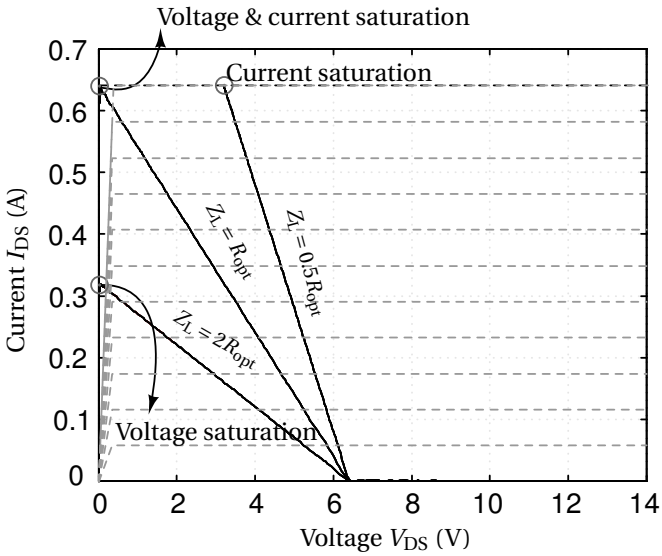

Figure 4.1. The ideal class-B load line ($Z_L = R_{opt}$) with its deviation for $Z_L = 0.5R_{opt}$ and $Z_L = 2R_{opt}$ case.

4.2. LOAD VARIATION ANALYSIS

In this section, we study the effect of varying load impedance on the performance of an ideal class-B power amplifier. For this analysis, we assume an ideal device with zero knee-voltage but includes current saturation (denoted by $I_{d_{max}}$) and a breakdown voltage $V_{dd_{break}}$. In our analysis, the output stage device is assumed to deliver its output power within the constraints of $I_{d_{max}}$ and a given supply voltage V_{dd}. To deliver 1-watt of output power to a load impedance of R_{opt}= 20 Ω (this value will be also used in the prototype design). The needed supply voltage can be obtained (1b) yielding V_{dd} = 6.4 V.

Consequently, the maximum device current is (1a) $I_{\mathrm{d_{max}}} = 0.64\ A$.

$$R_{\mathrm{opt}} = \frac{2V_{\mathrm{dd}}}{I_{\mathrm{d_{max}}}},\ (a)\quad P_{\mathrm{out}} = \frac{V_{\mathrm{dd}}^2}{2R_{\mathrm{opt}}} = I_{\mathrm{R}}^2 R_{\mathrm{opt}}\ (b) \tag{4.1}$$

Except for the fundamentals, all harmonics of the PA are short-circuited. With R_{opt} as reference impedance, next, we will study the impact of a 2:1 VSWR mismatch condition on the PA performance. First, we will assume the load to be purely ohmic, followed by the inclusion of the complex part.

4.2.1. LOAD-IMPEDANCE: REAL

The maximum and minimum load impedance seen by a PA for a 2:1 VSWR condition will be $2R_{\mathrm{opt}}$ and $0.5R_{\mathrm{opt}}$ respectively. When the PA sees its optimum load impedance (R_{opt}) it is on the edge of voltage and current saturation and as such reaches its maximum output power and efficiency simultaneously, while still providing linear operation (Fig. 4.1). When the PA sees a load

$Z_{\mathrm{l}} > R_{\mathrm{opt}}$

A higher load impedance (e.g. $Z_{\mathrm{l}} = 2R_{\mathrm{opt}}$) can still yield maximum efficiency due to voltage saturation of the output stage. However, the output power will be 3 dB (1b) lower than for the reference load, while signal distortion will occur. To maintain the output power equal, the supply voltage needs to be increased by a factor of $\sqrt{VSWR}$ while the input drive needs to be reduced by a factor $\sqrt{VSWR}$ i.e. $\sqrt{2}$. This sets the optimum load condition (1a) to:

$$2R_{opt} = \frac{2\sqrt{2}V_{dd}}{\frac{1}{\sqrt{2}}I_{d_{max}}} \tag{4.2}$$

$Z_l < R_{opt}$

A lower load impedance (e.g. $Z_l = \frac{1}{2}R_{opt}$) can neither deliver maximum output power nor maximum efficiency because of current saturation in the output transistor. In this case, we need to decrease the supply voltage by $\sqrt{VSWR}$ and increase the input drive by a factor $\sqrt{VSWR}$ i.e. $\sqrt{2}$. This sets the optimum load condition (1a) to:

$$\frac{1}{2}R_{opt} = \frac{2\frac{V_{dd}}{\sqrt{2}}}{\sqrt{2}I_{d_{max}}} \tag{4.3}$$

Since the output current is limited by $I_{d_{max}}$, we need to physically over-dimension the output stage device by a factor $\sqrt{2}$. This can be done by activating extra device width (e.g. in a digital intensive approach[60]) or by choosing a bigger device right from the beginning and operating it at $I_{\mathrm{d_{max}}}/\sqrt{2}$ or $P_{\mathrm{out}}/2$.

From the above analysis, we can conclude that by adjusting the output stage to the load, we can always recover the optimum PA operation. Wherein the supply voltage and

the drain current is bounded by,

$$V_{\mathrm{dd}} = [V_{\mathrm{dd}}/\sqrt{VSWR}, \sqrt{VSWR}V_{\mathrm{dd}}] \tag{4.4}$$

$$I_{\mathrm{d_{max}}} = [I_{\mathrm{d_{max}}}/\sqrt{VSWR}, \sqrt{VSWR}I_{\mathrm{d_{max}}}]. \tag{4.5}$$

When applying the proposed approach to handle VSWR mismatch conditions, this active device needs to be over-dimensioned in a first-order approximation with a factor $\sqrt{VSWR}$ for its gate width (W_g) and breakdown voltage ($V_{\mathrm{dd_{break}}}$) at the minimum. Over dimension W_{g} results in larger capacitance at the input, feedback, and output, which need to be resonated out by the input and output matching networks, yielding somewhat higher matching losses. Over dimension for the breakdown voltage of the active device, yields lower device speed, higher drain resistance and will reduce to some extent its current handling capability. Note that the latter might demand an even larger over-dimension of W_{g} than the original factor $\sqrt{VSWR}$ to compensate for reduced current handling capability. Consequently, the proposed technique is most effective when the active device technology used for the output stage has a lot of performance headroom (e.g. GaN). However, also more conventional technologies (e.g. LDMOS), can provide excellent results for low to medium VSWR values (e.g. VSWR = 2) as shown in this work. At high VSWR values (e.g. VSWR > 4) the use of advanced output stage technologies with sufficient performance headroom become mandatory in order to be effective with the proposed technique.

4.2.2. LOAD-IMPEDANCE: COMPLEX

In the event of a complex load impedance (e.g. $Z_{\mathrm{l}} = R_{\mathrm{l}} + \mathrm{j}X_{\mathrm{l}}$), the PA will experience a load-line deviation which is dependent on the $|Z_{\mathrm{l}}| = (R_{\mathrm{l}}^2 + X_{\mathrm{l}}^2)^{0.5}$. Namely, the transistor needs to handle the extra voltage swing due to the reactance, while this does not contribute to more output power, yielding a drop in efficiency.

To be aligned with practical design implementations, we restrict the matching network to the inclusion of switchable capacitor banks only. We will match the reactive load to a purely ohmic situation which is located on the line indicated in Fig. 4.4. This can be done by using a tunable shunt resonator (Fig. 4.2(a)) or by using a lumped version of a $\lambda/4$ impedance inverter (π-network) with two tunable capacitor banks (Fig. 4.2(b)). We can derive the required tuning range of the tunable capacitor, the insertion loss, and the Q requirements of a tunable shunt resonator as follows.

Let the shunt resonator inductance (L_{X}) and capacitance (C_{X}), having quality factors $Q_{\mathrm{L_X}}$ and $Q_{\mathrm{C_X}}$, be given by $L_{\mathrm{X}} = 1/\omega B_X$ and $C_{\mathrm{X}} = B_{\mathrm{X}}/\omega$ respectively (Fig. 4.2(a)). Consequently, the unloaded quality factor of the shunt resonator is given by $Q_{\mathrm{N}} = Q_{\mathrm{L_X}} || Q_{\mathrm{C_X}}$, with related losses modeled by a shunt conductance $G_{\mathrm{L_X C_X}}$ (Fig. 4.2a). Moreover, to determine the loaded quality factor Q_{l} of the total network and the corresponding insertion loss for a given VSWR ($|\Gamma_{\mathrm{l}}|$, ϕ_{l}). The ratio of susceptance over the conductance, when looked into the load, is used as the definition of loaded quality factor (Q_{l}) in this analysis. For a given $VSWR$ and a characteristic admittance Y_0 the related Γ_l and load admittance $Y_{\mathrm{l}} = G_{\mathrm{l}} + \mathrm{j}B_{\mathrm{l}}$ are given by,

$$|\Gamma_l| = \frac{|VSWR-1|}{|VSWR+1|} \quad (a), \quad Y_{\mathrm{l}} = Y_0 \frac{1-\Gamma_l}{1+\Gamma_l} \quad (b) \tag{4.6}$$

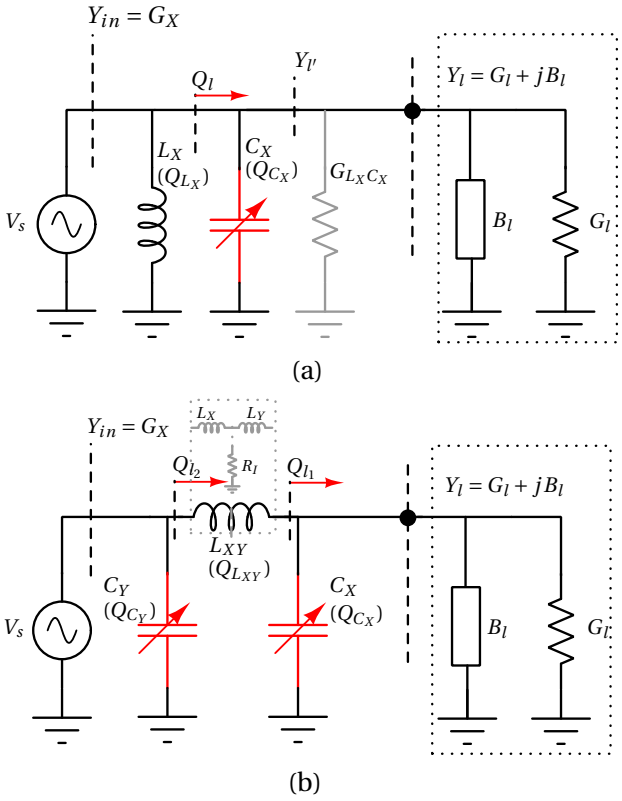

Figure 4.2. (a) Shunt resonator with a tunable capacitor bank, and (b) a π-TMN with two tunable capacitor banks.

Consequently, for a given $|\Gamma_l|$ and ϕ_l (0-360°), at any instant, the susceptance presented by the load is given by,

$$B_x = B_l(|\Gamma_l|, \phi_l) \tag{4.7}$$

The susceptance in (5) needs to be compensated to match the ohmic line of (Fig. 4.4). Resulting in a capacitance value and loaded network Q_l that can be computed for every ϕ_l by,

1. $0 \leq \phi_l \leq 180$ the load susceptance (B_l) is negative (inductive) and we need to add more susceptance to the shunt resonator. This is achieved by increasing the capacitance ($C_X = B_X/\omega$)

$$C_X = \frac{B_X}{\omega} + \frac{|B_x|}{\omega} \tag{4.8}$$

Consequently, the net susceptance in the loaded network increases, causing an increase in the loaded quality factor compared to a situation of a purely ohmic load,

$$Q_l = \frac{B_X + B_l(|\Gamma_l|, \phi_l)}{G_l(|\Gamma_l|, \phi_l)} \tag{4.9}$$

2. 180 < $\phi_1 \leq$ 360 the load susceptance (B_1) is positive (capacitive) and we need to remove susceptance from the shunt resonator. This is achieved by reducing the capacitance ($C_X = B_X/\omega$),

$$C_X = \frac{B_X}{\omega} - \frac{|B_x|}{\omega} \tag{4.10}$$

Consequently, the net susceptance in the loaded network remains constant, and the loaded quality factor remains equal to the situation of a purely ohmic load,

$$Q_1 = \frac{B_X}{G_1(|\Gamma_1|, \phi_1)} \tag{4.11}$$

The required capacitance tuning range can be computed by determining the maximum susceptance out of all the Γ_1 points on the VSWR circle.

$$B_{l_{max}} = max(|B_l(|\Gamma_l|, \phi_l)|) \tag{4.12}$$

Therefore, we get $B_X = B_{l_{max}}$ and the minimum and maximum value of the tunable shunt capacitor bank and the shunt inductor are given by,

$$[C_{X_{min}}, C_{X_{max}}] = [0, \frac{2B_{l_{max}}}{2\pi f}] \tag{4.13}$$

$$L_X = \frac{1}{(2\pi f)B_{l_{max}}} \tag{4.14}$$

Using (4.13) and (4.14) we can design the tunable shunt resonator at a given frequency (f). In the case that we want to cover a frequency range (e.g. f_1 to f_2). Then we should design the tunable shunt resonator at f_1 and choose a tunable capacitor with a finer step size corresponding to f_2. Moreover, for a given unloaded network quality factor Q_N and loaded network quality factor Q_1, we can determine the insertion loss as follow,

$$\text{IL} = 10\log_{10}(\frac{1}{1 + \frac{Q_l}{Q_N}}) \tag{4.15}$$

In practical implementations the unloaded quality factor of the tunable shunt resonator will be limited, resulting in a parasitic conductance (Fig. 4.2a) in shunt with the load. This is given by,

$$G_{L_X C_x} = \frac{B_{l_{max}}}{Q_N} \tag{4.16}$$

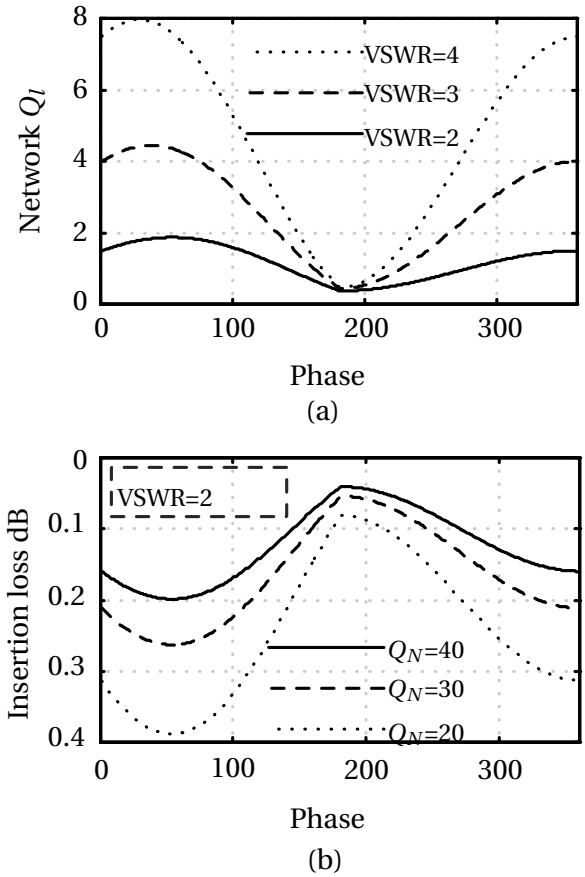

Figure 4.3. (a) Loaded network Q_l for the proposed shunt resonator approach (Q_N = 20) when considering a 2:1, 3:1, and 4:1 VSWR circle, (b) insertion loss for all the phase angles on a 2:1 VSWR circle for a given unloaded network Q_N.

Table 4.1. Comparison between TMN technique, an isolator, and the proposed technique

VSWR	2:1				3:1				4:1			
Configuration	|| Proposed	π Proposed	Isolator	π-TMN	|| Proposed	π Proposed	Isolator	π-TMN	|| Proposed	π Proposed	Isolator	π-TMN
Match point	ohmic range	ohmic range	50 Ω	50 Ω	ohmic range	ohmic range	50 Ω	50 Ω	ohmic range	ohmic range	50 Ω	50 Ω
$\frac{V_{dd_{max}}}{V_{dd_{min}}}$	2	2	Fixed	Fixed	3	3	Fixed	Fixed	4	4	Fixed	Fixed
$\frac{V_{in}g_{m_{max}}}{V_{in}g_{m_{min}}}$	2	2	Fixed	Fixed	3	3	Fixed	Fixed	4	4	Fixed	Fixed
$I_{d_{max}}$	+ 41.14 %	+ 41.14 %	Fixed	Fixed	+ 73.20 %	+ 73.20 %	Fixed	Fixed	+ 100 %	+ 100 %	Fixed	Fixed
$V_{dd_{break}}$	+ 41.14 %	+ 41.14 %	Fixed	Fixed	+ 73.20 %	+ 73.20 %	Fixed	Fixed	+ 100 %	+ 100 %	Fixed	Fixed
Q_l	≤ 1.88	≤ 2.31*	NA	≤ 4.78*	≤ 4.44	≤ 3.55*	NA	≤ 8.35*	≤ 7.97	≤ 4.78*	NA	≤ 12.34*
B_x ‡	0 - 0.030	0.005 - 0.035	NA	0.029 - 0.063	0 - 0.054	0 - 0.047	NA	0.036 - 0.092	0 - 0.076	0 - 0.058	NA	0.041 - 0.119
B_y ‡	NA	0.020	NA	0.031 - 0.063	NA	0.020 - 0.023	NA	0.037 - 0.092	NA	0.020 - 0.038	NA	0.044 - 0.119
IL †† dB	≤ 0.39	≤ 0.61*	0.30	≤ 1.58*	≤ 0.87	≤ 0.82*	0.30	≤ 2.44*	≤ 1.46	≤ 1.04*	0.30	≤ 3.26*
RL † dB	NA	NA	0.51	NA	NA	NA	1.25	NA	NA	NA	1.93	NA
$IL + RL$ dB	≤ **0.39**	≤ 0.61*	0.81	≤ 1.58*	≤ 0.87	≤ **0.82***	1.55	≤ 2.44*	≤ 1.46	≤ **1.04***	2.23	≤ 3.26*

‡ $C_x = B_x/\omega$; $C_y = B_y/\omega$; NA = Not Applicable; †† IL=Insertion loss for unloaded network $Q_N = 20$; † RL=Reflection loss; * Approximation

and will modify the effective admittance presented by the load VSWR to, (shown in Fig. 4.2a)

$$Y_{l'} = Y_l + G_{L_X C_x} \tag{4.17}$$

The analytical results for the loaded network Q_l from (4.9) and (4.11) on the given VSWR circles are shown in Fig. 4.3a. The highest loaded Q_l is 1.87, 4.44, and 7.97 for a VSWR of 2, 3, and 4 respectively, for an unloaded network Q_N of 20. The insertion loss of the shunt resonator, when matched to the 50 Ω, is 0.18 dB on a 2:1 VSWR circle. For the same Q_N the overall insertion loss when the resonator is used to match from the 2:1 VSWR circle to the ohmic case (Fig. 4.4) can be as high as ≤ 0.39 dB (Fig. 4.3b). Which is approaching the insertion loss of a commercially available isolator with a loss of about 0.3 dB. However, these isolators will introduce an additional reflection loss given by 10log(1 - $|\Gamma|^2$) (0.51) dB when handling a 2:1 VSWR condition. The comparison between the proposed technique, an isolator, and the π TMN (Fig. 4.2a) in terms of supply voltage, input drive, and component tunability is shown in Table 4.1. For the tunable π-TMN with a fixed inductor, we have determined the effective loaded network quality factor that matches the complex load either to an ohmic line and to a 50 Ω as follows.

π-TMN (MATCH TO THE OHMIC LINE)

In this case, we have assumed the initial π-TMN component values to be equal to the lumped equivalent of a 90° transmission line, where the inductance $L_{XY} = 1/Y_0\omega$ is fixed, whereas capacitance C_X and C_Y are tunable whose values are given by $C_X = C_{x'} + C_x$, and $C_Y = C_{y'} + C_y$ where $C_{x'} = C_{y'} = Y_0/\omega$. The values of $C_x = B_x/\omega$ and $C_y = B_y/\omega$ are dependent on the VSWR presented as follow,

1. **$0 \le \phi_l \le 180$:** then $B_x = |B_l(|\Gamma_l|, \phi_l)|$
2. **$180 < \phi_l \le 360$:** if $|B_l(|\Gamma_l|, \phi_l)| < Y_0/\omega$ then $B_x = -|B_l(|\Gamma_l|, \phi_l)|$ and $B_y = 0$ else $B_x = -\frac{Y_0}{\omega}$ and $B_y = |B_l(|\Gamma_l|, \phi_l)| - Y_0/\omega$

Note that by making both the capacitors tunable, a lower tuning range is required for these tunable capacitances, making their implementation more relaxed.

π-TMN (MATCH TO THE 50 Ω)

In this traditional solution, we need to design the tunable π-TMN with a fixed inductor (L_{XY}) and two tunable capacitors $C_X = C_{x'} + C_x$ and $C_Y = C_{y'} + C_y$ (Fig. 4.3a). Where the inductance is given by $L_{XY} = 1/(B_{xy}\omega)$, whereas the capacitance consists of two parts. Firstly, the values $C_{x'} = B_{x'}/\omega$ and $C_{y'} = B_{y'}/\omega$ are used to match the conductance part of the load. Secondly, $C_x = B_x/\omega$ and $C_y = B_y/\omega$ are used to compensate for the susceptance part of the load. Let Q_π be the loaded quality factor of the π-TMN that can be set independently. Since Q_π can be set independently, multiple solutions exist for the inductance L_{XY} that can cover the ohmic impedance on the endpoints of a given VSWR. We have numerically swept the Q_π e.g. (from 2-20 in steps of 0.1) and computed the related inductance L_{XY} that can cover the ohmic impedance on the endpoints of a given VSWR. Then we compute the minimum L_{XY} out of all the possible solutions. This would

correspond to the lowest possible quality factor and insertion loss while matching the endpoints of a given VSWR. When the load is conductive/ohmic in nature the design set $\{B_{xy}, B_{x'}, B_{y'}\}$ is a function of (Q_π, Y_l, Y_0). Moreover to compensate for the susceptance part of the load the design set $\{B_x, B_y\}$ is given by,

1. **$0 \leq \phi_l \leq 180$:** then $B_x = |B_l(|\Gamma_l|, \phi_l)|$
2. **$180 < \phi_l \leq 360$:** if $|B_l(|\Gamma_l|, \phi_l)| < B_{x'}$ then $B_x = -|B_l(|\Gamma_l|, \phi_l)|$ and $B_y = 0$ else $B_x = -B_{x'}$ and $B_y = |B_l(|\Gamma_l|, \phi_l)| - B_{x'}$

Now we know all the component values for a given admittance (Y_l), we can calculate the individually loaded quality factors when looking into one end of the network for a given VSWR with 0°-360° mismatch trajectory as shown in Fig. 4.2b. Where, the loaded network quality factor (Q_l) is given by $Q_l = \max(Q_{l_1}, Q_{l_2})$. Moreover, the insertion loss is given by $IL = IL_{Q_{l_1}} + IL_{Q_{l_2}}$ from (9). Note that this approximation follows from modeling the loaded π-TMN as a cascaded stage of two L-MN techniques. The reported insertion loss might deviate from full circuit simulation for smaller Q_N. Since, Q_{l_1} and Q_{l_2} were determined assuming the network to be lossless. At finite Q_N, the parasitic conductance (4.16) will fold over in the network (15) and will modify Q_{l_2}. In TABLE 4.1, it can be seen that the proposed method with a tunable shunt resonator (|| proposed) provides the lowest Q_l and insertion loss for a 2:1 VSWR. For higher VSWR the proposed method using a tunable shunt resonator becomes less effective due to fixed shunt inductance, and π-TMN which matches back to the ohmic line is the most favorable choice. Compared to earlier approaches that aim to match back to the optimum loading of the PA (e.g., to the 50 Ω point), the proposed methods, due to their lower loaded Q_l, outperform the traditional solution in terms of matching losses in all cases.

Correction for (high) VSWR conditions, however, yields always an increase in the voltage swings for a given RF output power. So higher breakdown voltages for the tunable capacitors are needed to handle these. The proposed technique drastically reduces the quality factor requirement of tunable capacitors in comparison to earlier techniques [61–64]. This is important since for practical devices there is a direct trade-off between breakdown voltage and series losses of the tunable capacitor. E.g. in this work, we will use silicon on insulator (SOI)-based capacitive switch banks [65]. They use stacked field effect transistor (FET) devices to handle these voltage swings, so trading off their quality factor. Also here, the use of high-end (III-V) technologies, like gallium arsenide (GaAs) or GaN, can relax this trade-off, allowing the handling of larger VSWR values.

4.3. DESIGN DETAILS

To validate the concepts described in sections II and III a prototype PA with an active control loop has been designed. Fig. 4.6 shows the complete schematic of the proposed load-insensitive PA. It consists of the transistor output stage, the proposed six-port reflectometer, and a parallel resonator with a tunable capacitor. Rogers RO4350B with 0.508 mm thickness is chosen as the PCB substrate. In this work, the load deviation to correct for is assumed to be the result of antenna mismatch in a handset or mutual coupling in an antenna array using antenna beam steering with coherent signals. The resulting load deviations will vary only at a slow speed (much lower than the modulated

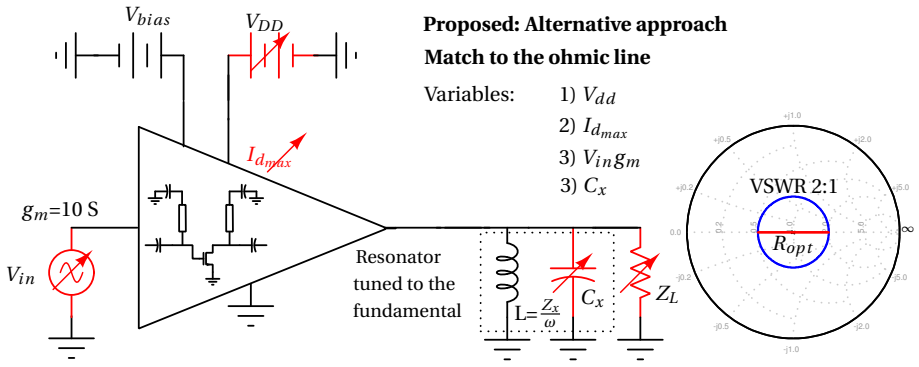

Figure 4.4. The proposed load-insensitive PA with a tunable, supply voltage, input drive, and the matching network.

4

TX signal itself). Therefore, the direct current (dc)-dc converter for supply adjustment can have a slow response time / low bandwidth. The efficiency of such a "slow" dc-dc converter can be very high, typically in the order of 98 % percent). Consequently, the power dissipated by the supply modulator (P_{SR}) is low and will change the overall conclusions by 2-3 %. To keep our analysis simple, we will ignore this power consumption in the remaining analysis.

4.3.1. LDMOS PA

The implemented PA is designed for Class-AB and delivers an output power of 700 mW at 900 MHz. The load impedance to achieve this output power from a 5.3 V supply turns out to be close to 20 Ω. The transistor is a commercial AFIC901N packaged laterally-diffused metal-oxide semiconductor (LDMOS) device. The input of the PA is impedance matched to 50 Ω, with emphasis on achieving unconditional stable behavior. At the output, a $\lambda/4$ transmission line is used to transfer the 50 Ω load to the desired 20 Ω impedance level to be offered to the PA stage.

4.3.2. SIX-PORT REFLECTOMETER

The six-port reflectometer is implemented using an additional 50 Ω 90° transmission line, which at its two-end points is weakly coupled to a microstrip hybrid ring. The coupling capacitors are implemented using an interdigitated finger structure as shown on the PCB. They are sized to provide a coupling factor of -30 dB. The RF peak detectors used for measuring the RMS voltages are from analog devices, i.e. LTC5505-2. They provide a dynamic range of 40 dB [54].

4.3.3. TUNABLE SHUNT RESONATOR

From (4.13) and (4.14) on the 2:1 VSWR circle ($B_{l_{max}} = 0.015$) the required inductance and capacitance range for the parallel resonator at 900 MHz turn out to be 12 nH and 0

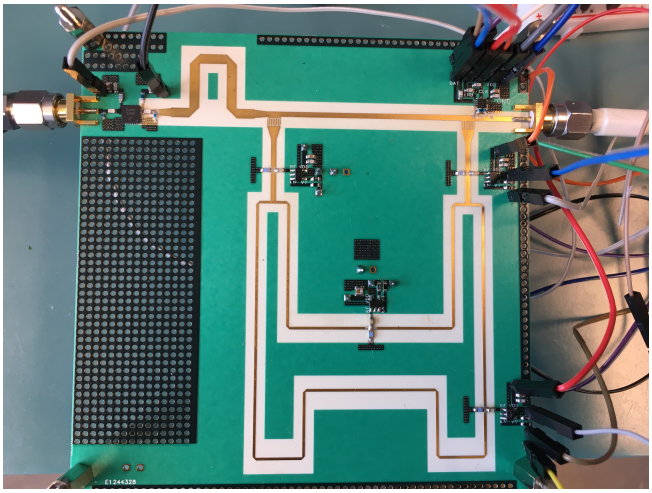

Figure 4.5. The realized PCB includes the 900 MHz LDMOS PA, the six-port reflectometer, and a tunable shunt resonator.

- 5.2 pF respectively. Switched capacitor banks from pSemi were chosen for the implementation of the tunable capacitor. E.g. PE64906 [65] offers a C_{min} = 0.8 pF and C_{max} = 5.4 pF at 900 MHz with a step size of 119 fF, (estimated from the datasheet plots[65]), yielding an effective capacitance range of 4.6 pF. This component was selected for its fine step size, allowing the best demonstration of our proposed method. However, a capacitance range short-fall of 300 fF is expected when aiming to compensate for the highest susceptance value occurring on the 2:1 VSWR circle. The required inductance is 9 nH. To implement them 0603DC high-Q inductors from coil-craft are selected.

The designed PCB with PA, the six-port reflectometer, and the tunable shunt resonator are shown in Fig. 4.5.

4.4. MEASUREMENT RESULTS

The measurement setup is shown in Fig. 4.6. It consists of the designed PCB, an Agilent E8257D analog signal generator, an Agilent E3631A triple channel power supply, an Agilent E4446A spectrum analyzer, and an MT982E Maury load tuner. The instrument control is performed via MATLAB through the GPIB and USB interface. An Arduino MKR Zero board based on Cortex-M0+ 32bit low power Arm microcontroller is used to control the tunable pSemi capacitor via serial peripheral interface (SPI). The voltage readings of the four power detectors are collected using a TI ADS1115 4-channel 16-bit ADC.
In this work, we will first evaluate the performance of the class-AB PA, and the voltage readings of the six-port reflectometer separately. Next, the overall operation including the actuation method is elaborated, which is used to recover the 50 Ω PA operation when the external load impedance moves over the 2:1 VSWR circle. The power added efficiency

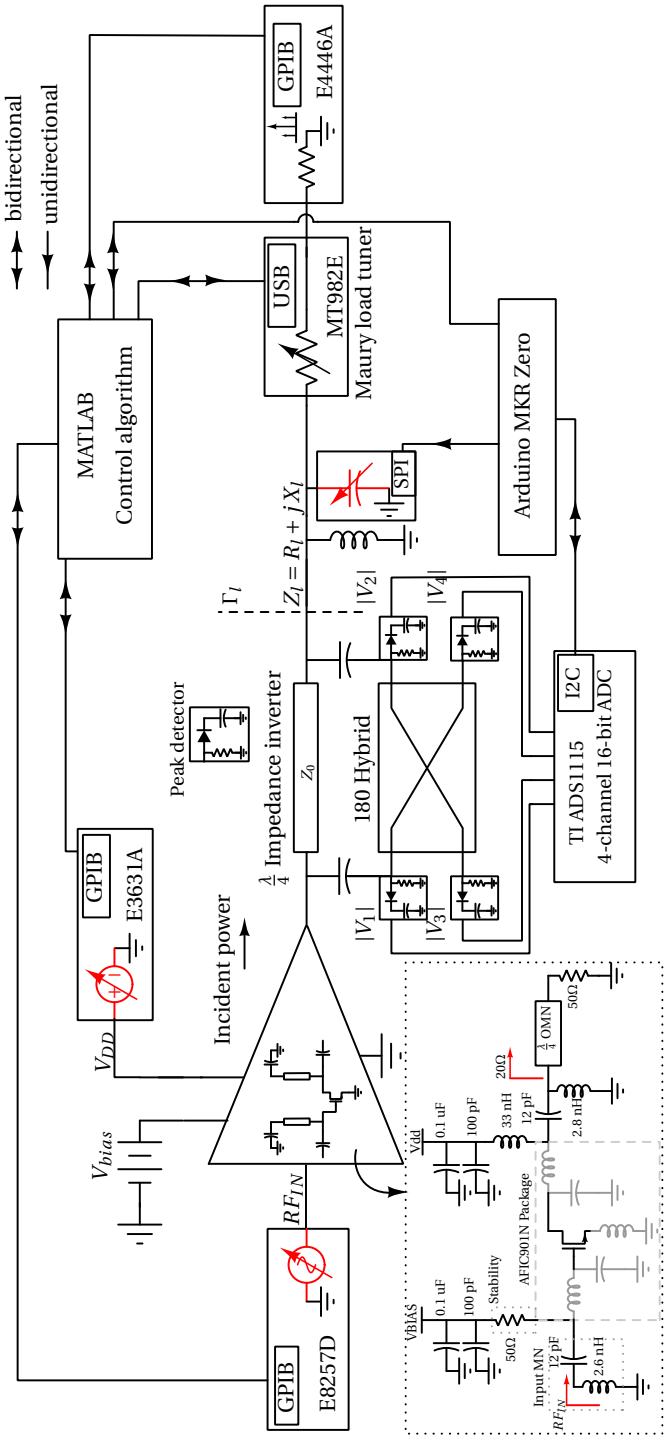

Figure 4.6. The detailed schematic of the PA, proposed six-port reflectometer with RF peak detectors, and a parallel resonator with a tunable capacitor. The measurement instruments and the actuation control loop are also shown.

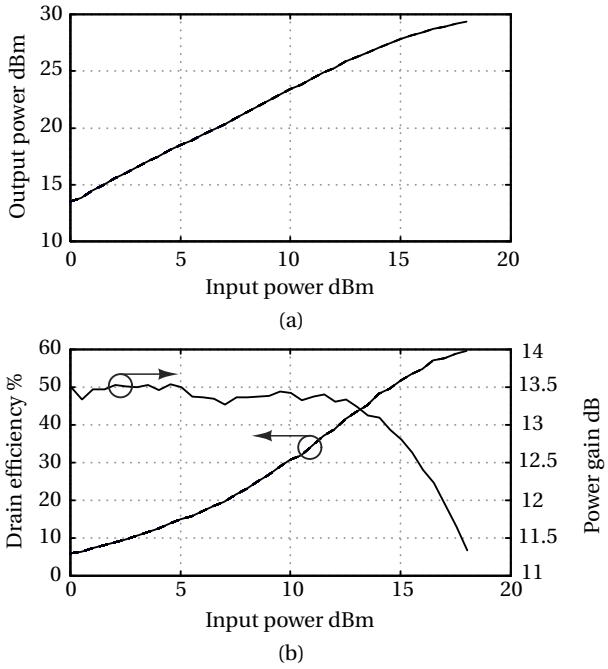

Figure 4.7. (a) PA output power, (b) drain efficiency, and power gain versus input power (V_{dd} = 5.3 V and I_{d_q} = 64 mA).

(PAE) of the proposed technique is determined as follows,

$$PAE = \frac{P_{out}}{P_{DC} + P_{in} + P_{SR} + P_{PKD} + P_{CB}} \tag{4.18}$$

where P_{out} is the output power of the PA, P_{DC} is the dc input power to the PA, P_{in} is the input drive power of the PA, P_{SR} is the power dissipated by the supply regulator, P_{PKD} is the power consumed by the peak detectors, and P_{CB} is the power consumed by the capacitor bank. Moreover, we have assumed $P_{SR} \approx 0$ (section IV). However, in practical implementation, the dc-dc supply modulator will dissipate some amount of power, which can be included to arrive at a more accurate PAE. The peak detectors and the capacitor bank consume 2 (4x0.5) mA and 140 uA from a 2.7 V power supply respectively.

4.4.1. PA PERFORMANCE

4.4.2. ACTUATION METHOD

The process of recovering the 50 Ω PA operation in the event of a load mismatch is a two-step method. Wherein, we first match the complex load to the ohmic case (red line in the Smith chart of Fig. 4.4). Next, we adjust the supply voltage and the input drive of the PA to meet the required performance specifications. The proposed method is designed to

recover slow VSWR variation. Since the current setup is limited by the operational speed of instrument control via Matlab and to a lesser extent by the lower sampling speed of the ADS1115 analog to digital converter (ADC) (860 samples per second).

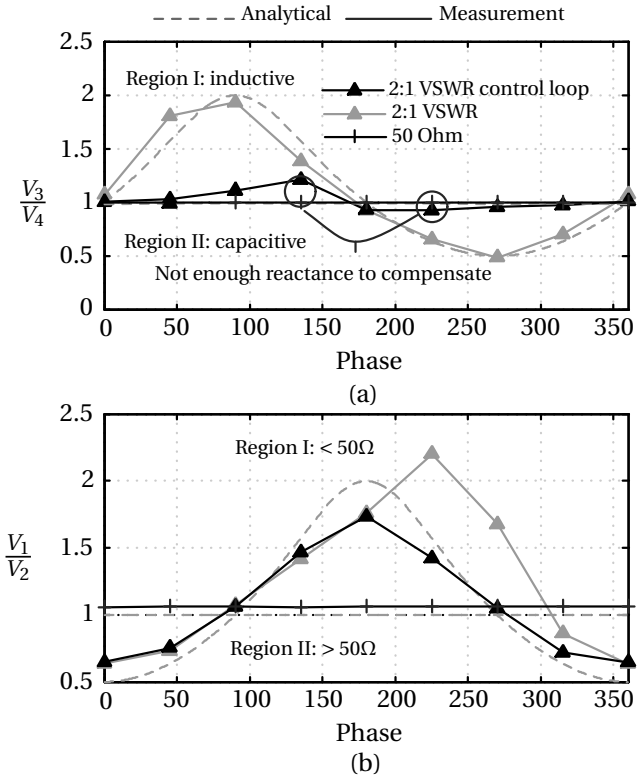

Figure 4.8. Six-port reflectometer results when PA is subjected to 50 Ω and loads on a 2:1 VSWR circle (a) V_3/V_4 points to load reactance (Region I: (> 1) is inductive and Region II: (< 1) is capacitive) (b) V_1/V_2 points to the VSWR(Region II: (< 1) higher than 50 Ω and Region I: (> 1) lower than 50 Ω.

MATCH TO THE OHMIC CASE

Fig. 4.8 shows the analytical and measurement results when the PA load is set to 50 Ω and on a 2:1 VSWR circle with and without correction. The PA input power level was 12 dBm at 900 MHz in both measurements. When the voltage ratio $V_3/V_4 > 1$ we know that the complex load is inductive. We can start adding capacitance to the shunt resonator to match to the ohmic case. On the other hand, when the voltage ratio $V_3/V_4 < 1$, the load is capacitive in nature. We can start removing capacitance from the shunt resonator. If we perform this operation on the 2:1 VSWR circle till the point voltage ratio $V_3/V_4 \approx 1$ or max/min capacitance bank limit is reached. We see that we can always match to the

ohmic case. At 135° and 225° phase angles the corrected ratio V_3/V_4 deviates somewhat from unity. At these points, the capacitive bank fails to provide sufficient tuning range to add or remove the susceptance of the shunt resonator. This shortfall is ≈ 300 fF (section IV).

SUPPLY VOLTAGE AND INPUT DRIVE ACTUATION

with the complex load matched to the ohmic case. To adjust the output stage of the PA to the load we need to first determine if the impedance is > 50 Ω or < 50 Ω. The voltage ratio V_1/V_2 provides this information. If the ratio is > 1 then, we need to reduce the power supply voltage and increase the input drive power as the impedance is < 50 Ω. And if the ratio is < 1, we need to increase the supply voltage and reduce the input drive power, as the impedance is > 50 Ω.

The ideal response of the amplifier on a load change has been already discussed in section II. There we found that, for example, a doubling in the load impedance should result in a 3dB gain enhancement and a 3dB drop in output power. Practical amplifier implementations, however, will deviate from this ideal behavior due to parasitics in their amplifying device(s). Consequently, the optimum scaling parameter deviates from the $VSWR^{0.5}$ parameter described in section II. However, this can be overcome by using an iterative procedure in the control of the PA input power and supply voltage while monitoring the gain in the power back-off and the position of the 1 dB compression point (P1dB). Moreover, the optimum scaling parameters found in the measurement deviate indeed somewhat from the theoretical $VSWR^{0.5}$ factor as described earlier in section II, resulting in a somewhat higher drive level and supply voltage. These higher values are needed to compensate for the somewhat increased losses in the circuitry when deviating from the 50 Ω condition. The control loop finds these optimum settings by using an iterative procedure for achieving the same $P_{1\text{dB}}$ or average output power in the case of a modulated signal as in the reference case.

The results of the PA performance on a 2:1 VSWR circle, with and without the control loop method are shown in Fig. 4.9. We have also shown the performance of the PA when matched to the 50 Ω load for comparison. Fig. 4.9(a), 4.9(d), and 4.9(g) show the PA output power, power gain, and drain efficiency from power back-off to saturation. Fig. 4.9(b), 4.9(e), and 4.9(h) show the PA output power, power gain, and drain efficiency when the PA is driven by a 64-QAM 3.86-MHz signal with an input power of 9 dBm. Moreover, for the same input signal, ACPR performance is shown in Fig. 4.10. Meanwhile, Fig. 4.9(c), 4.9(f), and 4.9(i) show the PA output power, power gain, and drain efficiency at the output power 1 dB compression point. The control loop can recover the PA performance in terms of output power and power gain with a variation of less than ≤ ± 0.1 dB for a linear output power of 22 dBm. However, it suffers from decreased efficiency at some of the phase points, which can be related to the cases where R_{Load} is well below (< 50 Ω). Here, the increased I^2R losses and the non-linear characteristic of the transistor knee voltage, negatively impact the efficiency, especially at higher drive levels. Moreover, for the cases where R_{Load} is well above (> 50 Ω) insertion loss of the shunt resonator increases which negatively impacts the efficiency.

Note that all measurements have been performed with the realized hardware demonstrator of Fig. 9. This approach yields the most consistent results since all experiments

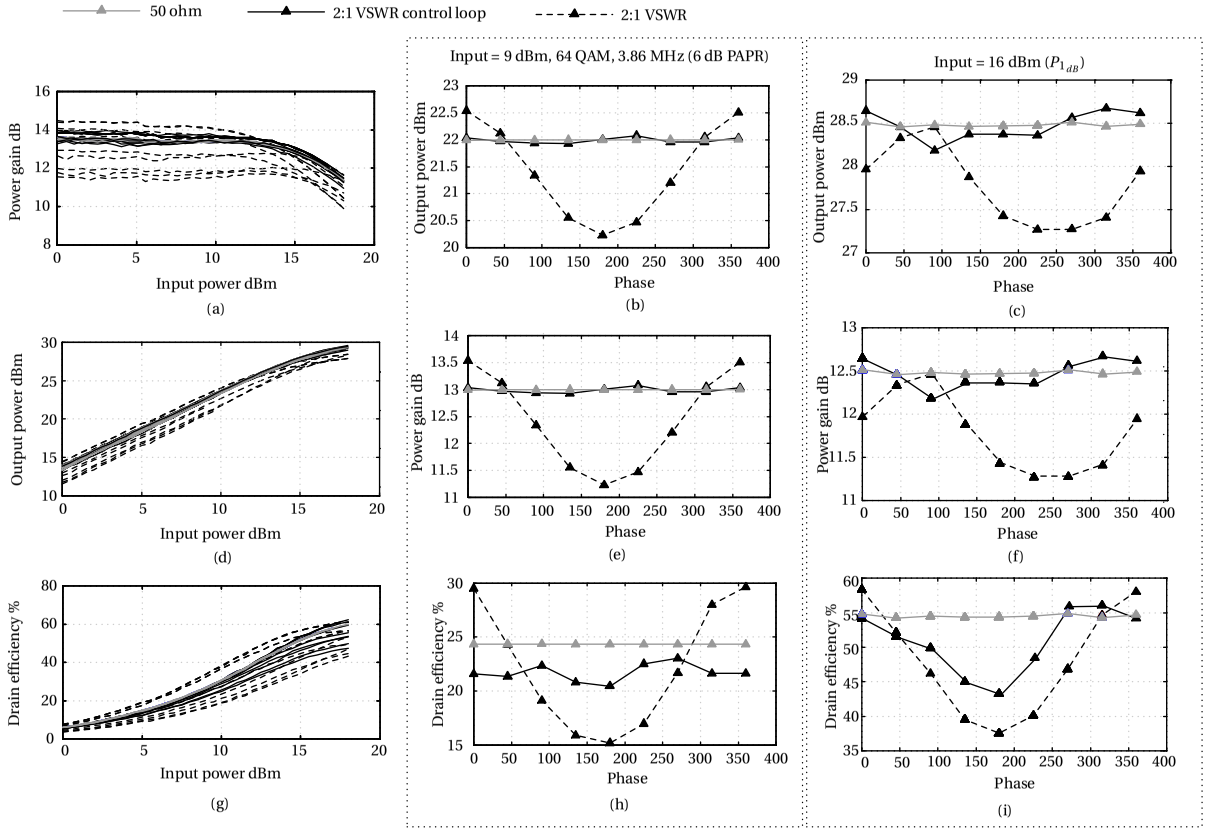

Figure 4.9. PA performance when the load is matched to the 50 Ω, on a 2:1 VSWR circle for a phase step of 45° with and without the proposed actuation method. (a), (d), and (g) show the PA output power, power gain, and drain efficiency vs. input power. (b), (e), and (h) show the PA output power, power gain, and drain efficiency when the PA is driven by a 64 QAM 3.86 MHz signal with an input power of 9 dBm. (c), (f), and (i) show the PA output power, power gain, and drain efficiency at the output power 1 dB compression point.

Table 4.2 Comparison with the state of the art load insensitive PAs

Comparison	Ideal isolator		**This work**		[63]		[62]		[20]		[22]		[66]	
Technique	Reference case††		|| **Proposed**		2-stage π-match‡		3-stage π-match‡		Balanced ‡		Doherty-Balanced ‡		Supply Adaptation ‡	
Freq GHz	0.9		0.9		1.95		1.95		1.95		3.5		3.55	
Signal	1-tone CW		1-tone CW		1-tone CW		1-tone CW		1-tone CW		1-tone CW		1-tone CW	
Z_l	50 Ω	2:1	**50** Ω	**2:1**	50 Ω	2.5:1	50 Ω	2.5:1	50 Ω	2.5:1	50 Ω	2:1	50 Ω	25-100 Ω
P_{sat} dBm	29.37	28.86	**29.4**	**29.4[+0.2,-0.4]**	30.8	30.0[+0.2,-0.1]	NR	NR	28.4	NR	41.9	NR	40 †	40[0.4,-0.1] †
DE/PAE %	59.1/56.2	52.5/50.2	**59.1/56.2**	**46.5-61.3/44.1-58.3**	-/47	-/39-42	NR	NR	-/40.7	NR	70/-	NR	66.5/-	56.6-69.5/-
Signal	64 QAM 3.86 MHz		64 QAM 3.86 MHz		WCDMA		WCDMA Rel'99		WCDMA		LTE 10 MHz		OFDM 20 MHz	
PAPR	6		6		3.5		3.5		3.5		NR		9.4	
P_{out} dBm	22	21.5	**22**	**22± 0.1**	27.9	27.9[0,-0.5]	28.5	28.5	26.6	26.6[0.5,-0.5]	34.5	32.5 - 35.1	NR	33.1-33.5
DE/PAE %	24.4/23.9	21.7/21.2	**24.4/23.9**	**21-23/20.4-22**	-/38	-/31.5-32.5	-/42.9	-/28.6-33.5	-/35	NR	42.4/-	22-39/-	NR	23-29/-
$ACPR$ dBc	-48	-48	**-48**	**< -45**	NR	< -40	-41.9	< -37	-36	-33	-37	NR	-32	-30.8

‡ Results are estimated from plots; † 1 dB compression point; NR = Not Reported; NA = Not Applicable; †† Ideal isolator for reference case, considering prototype PA 50 Ω performance (VSWR 1:1) as the reference, and the calculated reflection loss for a 2:1 VSWR to be 0.51 dB;

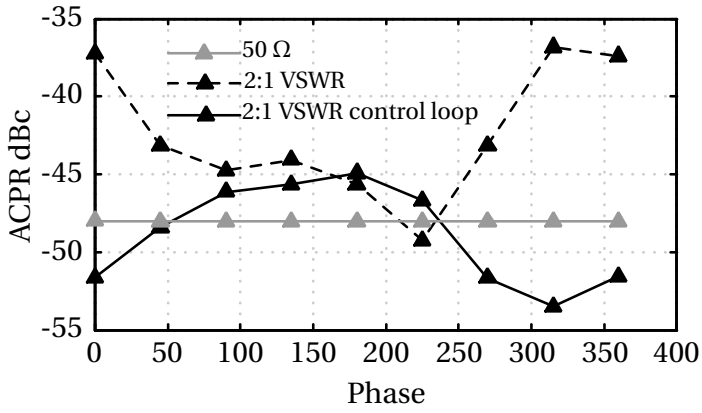

Figure 4.10. ACPR with 64 QAM 3.86 MHz signal with an input power of 9 dBm for PA operation at 50 Ω, 2:1 VSWR, and 2:1 VSWR with control loop.

are done on the same hardware. Logically, a PA without an oversized active device, reflectometer, and shunt mismatch correction network would have lower losses in its output. These losses are estimated to be L_{ext} (= extra matching loss + reflectometer loss + shunt resonator) dB lower than for the proposed solution. Namely, in our approach to compensate for a 2:1 VSWR mismatch condition, the active device needs to be oversized for its gate width by $\sqrt{VSWR}$ (41.42%), yielding an increase in output capacitance of 41.42%. The loaded Q of the output matching network to resonate out this capacitance will increase by the same amount. Assuming a Q of 30 for the reactive components used to implement this matching network, an extra matching loss of 0.1 dB is estimated for our proposed method. In addition, the reflectometer and shunt resonator adds 0.046 dB and 0.174 of losses, yielding L_{ext} dB additional loss in the 50 Ω load case. In the worst case condition VSWR = 2 ($|\Gamma_l| = 0.333, \phi_l = 90^o$), output power and efficiency losses rise to 0.576 dB and 5.76 % (assuming 1% for 0.1 dB drop in output power) in the worst condition when corrected back to an ohmic condition. Consequently, using the same hardware demonstrator in the comparison, output power and efficiency of a stand-alone PA are underestimated by ≈ 0.32 dB and 3.2 % respectively in the 50 Ω case.
In Table 4.2, a comparison with the state of the art is provided, it comprises of an ideal isolator as a reference case, the balanced PA, and a tunable matching network technique. Note that in this comparison the power dissipations of the control loop power and dc-dc converters ($P_{SR} \approx 0$) are assumed to be very small compared to the power dissipation of the self-healing PA, yielding a slight overestimation of the performance that can be achieved with practical implementations of the proposed concept. When compared to the isolator this work achieves better constant output power and average efficiency. Whereas the tunable matching network techniques in [62][63] approach the 50 Ω output power performance, however, this is at the expense of multi-stage tunable matching network. Even with the use of multi-stage TMN, this technique suffers from degradation in efficiency and ACPR performance. Moreover, the balanced PAs have a much higher

output power variation. In brief, we can conclude that the proposed technique achieves the best overall performance in terms of providing constant linear output power, drain efficiency, and ACPR in the events of load mismatch on 2:1 VSWR circle when compared to the reference 50 Ω performance.

4.5. CONCLUSION

This chapter has demonstrated a linear Class-AB PA, which is made insensitive to load variations. The fully automated control algorithm was able to recover from the load variation on a 2:1 VSWR circle and could reduce the gain and output power variation to less than ± 0.1 dB when compared to the 50 Ω reference case. The proposed combination of, matching network tuning, supply voltage, and drive level adjustment drastically reduces the high-Q requirements found in previously presented tunable MN networks.

5

LOAD-INSENSITIVE DOHERTY POWER AMPLIFIER

5.1. INTRODUCTION

The ever-growing demand for higher data rates has led to the increased use of spectrally efficient complex modulated signals, which are characterized by large peak to average power ratio (PAPR). To amplify these signals in an energy-efficient manner envelope tracking (ET) and Doherty power amplifier (DPA) architectures are employed. ET architectures using dynamic supply modulation can provide high performance for signals with a limited modulation bandwidth (< 40 MHz), however, face difficulties when dealing with higher bandwidths due to the very rapidly increasing demands on their supply modulator. Consequently, DPAs are typically preferred when operating with signals that have both high PAPR and video bandwidth [1].

However, DPAs are very sensitive to load impedance variation [67], specifically to the magnitude of the load, and therefore rarely found without additional measures in applications that demand VSWR resilience i.e., mobile handset (antenna mismatch) and phased array operation (e.g. due to mutual coupling within a column of antenna elements handling the beam elevation steering). In the sub-6 GHz range, isolator arrangements are usually applied to handle the impact of load variations, but this increases the form factor, and costs, while hampering the system integration. A tunable matching network (TMN), in theory, can correct for changing VSWR conditions and does not introduce reflection losses [14–16, 62, 63]. However, high-Q conditions in the TMN arise, when correcting for arbitrary complex load values within a given VSWR range [68]. Consequently, their successful low-loss realization relies heavily on the availability of tunable reactive devices with extremely high Q and high breakdown voltages [68]. As such, practical TMNs that target the correction of arbitrary complex loads have high insertion losses, which overshadow their potential benefits.

Recently, in view of the requirements of 5G applications, there has been a growing interest in developing DPA architectures that offer VSWR resilience. An obvious choice is

[1] This chapter consists of material previously published as the author submitted version for from "G. D. Singh, et al. "A Load Insensitive Do- herty Power Amplifier with better than -39 dBc ACLR on 2:1 VSWR Circle using a Constant 50 Ω Trained Pre-distorted Signal". In: Proc. Eur. Microw. Conf. (EuMC). 2022, pp. 222–225.

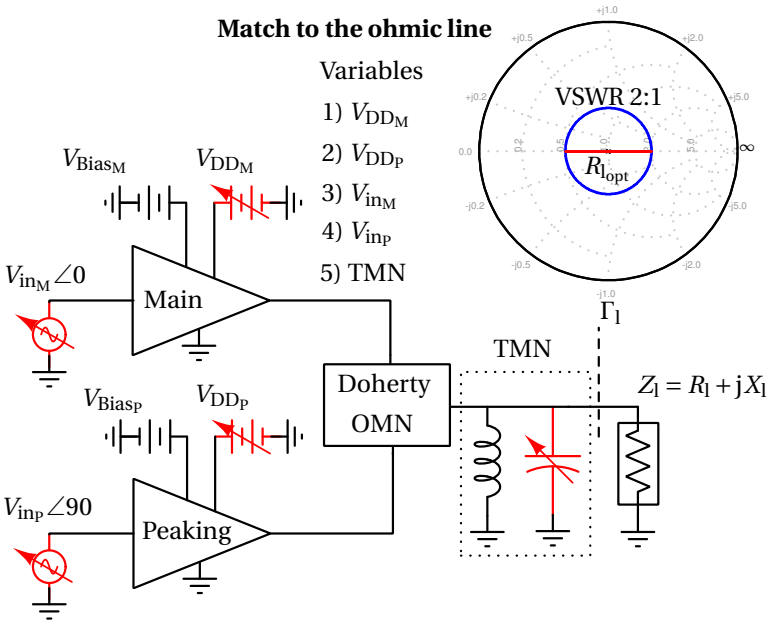

Figure 5.1. The proposed low-loss load-insensitive Doherty PA consists of a tunable input drive, supply voltage, and tunable matching network.

to use DPA's in a balanced architecture [23]. This will ensure that at least in power back-off mode the individual branch PAs in the DPA do not experience any voltage or current clipping. However, the hybrid coupler is a bit lossy and occupies a significant area. It is of desirable interest if similar performance can be achieved through some reconfiguration. The easiest approach is through current mode redundancy and reconfigurability. By adjusting the main and peaking stages g_m and the relative phase (using a tunable phase shifter), some degree of VSWR resilience can be achieved [27]. Restricting to current mode reconfigurability limits this technique to impedance ranges that do not cause the main stage voltage to clip. To handle impedance that clips the main stage voltage, an extra degree of freedom needs to be added, for example, reconfigurable series/parallel switchable Doherty [28]. By default, parallel DPA mode is active, the impedance range for which the main stage voltage clips, the series mode gets activated. Furthermore, DPA can also be designed using a hybrid coupler instead of a 90° transmission line. This is achieved by using a silicon-on-insulator (SOI) based single pole double throw (SPDT) switch [22] at the isolated port of the hybrid coupler. The switch terminates this port in either an open or short circuit. If an extra impedance is added to the switch say 50 Ω. Then it is possible to switch between a balanced PA and DPA configuration. For the varying load impedance, the topology that offers the best performance can be chosen. Finally, on the same fundamentals of current reconfigurability, it is also possible to actively adjust a DPA loading condition using a multi-port active load-pull [69]. In summary, a

close inspection of the above techniques shows that these can be categorized as pseudo-load-insensitive techniques, as they do not fully restore the DPA performance from the impact of the applied load-mismatch, but rather try to "soften" the consequences of this load-mismatch. The individual branch PA voltage clipping condition is the primary limiting factor of these approaches.

In this chapter voltage and current mode redundancy and reconfigurability are explored, to make the DPA insensitive to load variation operation. The proposed technique relies on a DPA topology, which features controlled supply voltages and gain/input-drive levels of the main, and peaking output stage that act on the (slow) changes of the applied VSWR. To accommodate the behavior of the impedance inverter-based DPA power combiner, ohmic load variations need to be handled by a kind of mirrored control of the supply voltages and drive levels of the main and peaking devices. Furthermore, reactive deviations of the load are canceled by a single tunable capacitive switch bank located directly at the output of the DPA (see Fig. 5.1). Using the combination of these techniques, the (optimum) Doherty operation can always be restored for any complex load-mismatch event, within the control range of the capacitive bank and supply voltages.
The outline of this chapter is as follows. First, we look at the sensitivity of the Doherty power amplifier. Next, the solution is provided to restore the optimum Doherty operation, even when load-mismatch conditions are present, as such ensuring load-insensitive behavior. A printed circuit board (PCB) DPA prototype based on this principle is designed. Followed by measurement results and conclusion.

5.2. DPA LOAD VARIATION ANALYSIS

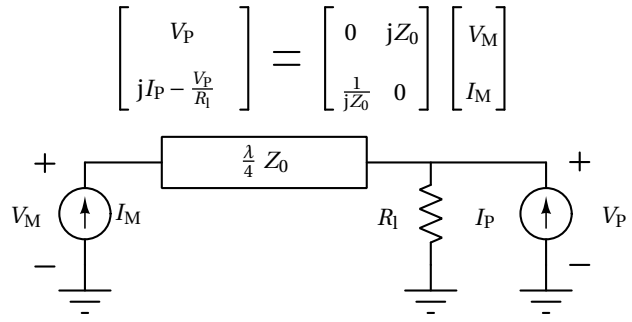

Figure 5.2. An ideal Doherty PA.

For an ideal conventional (asymmetrical) two-way DPA using identical supply voltages (V_{DD}) for its main (V_{DD_M}) and peaking device (V_{DD_P}), a standard Doherty design procedure based on the desired voltage and current relations can be followed (see Fig. 5.2). This procedure is briefly repeated below to provide the basis for our load sensitivity analysis.

$$V_P = jZ_0 I_M \tag{5.1}$$

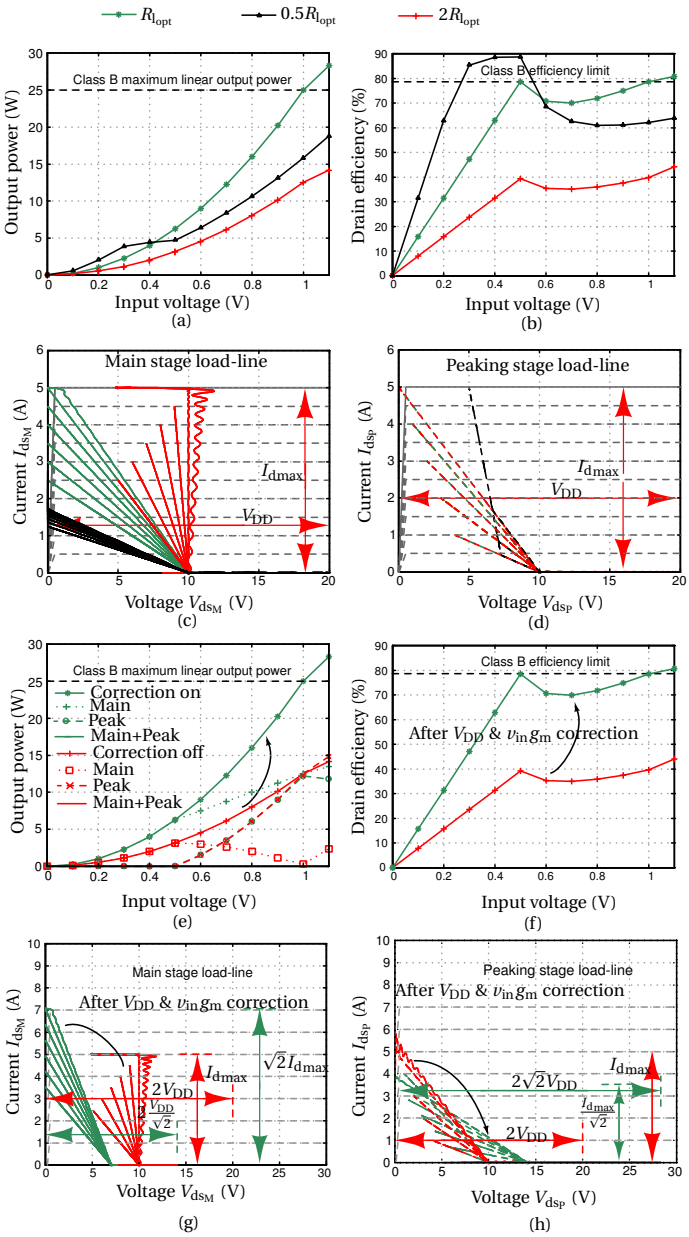

Figure 5.3. DPA performance in terms of (a) output power, (b) drain efficiency, (c) load-line of the main output stage, and (d) load-line of the peaking output stage, for $R_l = R_{l_{opt}}$ (green), $R_l = 2R_{l_{opt}}$ (red), and $R_l = 0.5R_{l_{opt}}$ (black). DPA performance in terms of (e) output power, (f) efficiency, (g) main stage load-line, and (h) load-line of the peaking output stage, when applying the mismatch condition ($2R_{l_{opt}}$) without (red) and with (green) the proposed correction-technique.

$$V_{\mathrm{M}} = Z_0\left(\frac{Z_0}{R_{\mathrm{l}}} I_{\mathrm{M}} - I_{\mathrm{P}}\right) \tag{5.2}$$

For the normalized input voltage $v_{\mathrm{in}} = \hat{v_{\mathrm{in}}} / \hat{v_{\mathrm{in}_{\mathrm{max}}}}$ exceeding α, with $\hat{v_{\mathrm{in}_{\mathrm{max}}}}$ being the maximum input voltage, the peaking device is activated. Consequently, high-efficiency peaking will occur at $20\log_{10}(\alpha)$ dB power back-off. For a DPA with a maximum output power ($P_{\mathrm{out}_{\mathrm{max}}}$) and a high-efficiency range that starts at P_{outback}, we can determine, α as: $\alpha = (P_{\mathrm{outback}}/P_{\mathrm{outmax}})^{1/2}$. At $v_{\mathrm{in}} = \alpha$, the peaking amplifier does not deliver any power, so we can write $P_{\mathrm{outback}} = P_{\mathrm{out}_{\mathrm{M}}\,back} = 0.5(\alpha I_{\mathrm{M}_{\mathrm{max}}} V_{\mathrm{DD}_{\mathrm{M}}})$. Furthermore, at maximum power we have, $P_{\mathrm{outmax}} = P_{\mathrm{out}_{\mathrm{M}}\mathrm{max}} + P_{\mathrm{out}_{\mathrm{P}}\mathrm{max}}$ in which, $P_{\mathrm{out}_{\mathrm{M}}\,max} = \alpha P_{\mathrm{out}_{\mathrm{max}}}$, and $P_{\mathrm{out}_{\mathrm{P}}\mathrm{max}} = (1-\alpha)P_{\mathrm{out}\,max}$. Making use of the fact that $V_{\mathrm{DD}_{\mathrm{M}}} = V_{\mathrm{DD}_{\mathrm{P}}}$, we find, $I_{\mathrm{M}_{\mathrm{max}}} = \alpha I_{\mathrm{Tot}_{\mathrm{max}}}$, and $I_{\mathrm{P}_{\mathrm{max}}} = (1-\alpha) I_{\mathrm{Tot}_{\mathrm{max}}}$ With, $I_{\mathrm{Tot}_{\mathrm{max}}} = 2P_{\mathrm{out}_{\mathrm{max}}}/V_{\mathrm{DD}}$ being the total current budget of the DPA assuming pure class-B operation for both the main and peaking device. Using the voltage saturation condition for the main device to reach high efficiency, we can, using (5.2) write for the power back-off point α.

$$I_{\mathrm{M}_{\mathrm{back}}} = I_{\mathrm{M}_{\mathrm{max}}}\alpha = I_{\mathrm{Tot}_{\mathrm{max}}}\alpha^2 \tag{5.3}$$

$$I_{\mathrm{P}_{\mathrm{back}}} = 0 \tag{5.4}$$

$$V_{\mathrm{M}_{\mathrm{back}}} = V_{\mathrm{DD}} = \frac{Z_0^2}{R_{\mathrm{l}}} I_{\mathrm{M}_{\mathrm{max}}}\alpha = \frac{Z_0^2}{R_{\mathrm{l}}} I_{\mathrm{Tot}_{\mathrm{max}}}\alpha^2 \tag{5.5}$$

and at full power, using the voltage saturation condition for both the main and peaking device,

$$I_{\mathrm{M}_{\mathrm{full}}} = I_{\mathrm{M}_{\mathrm{max}}} = I_{\mathrm{Tot}_{\mathrm{max}}}\alpha \tag{5.6}$$

$$I_{\mathrm{P}_{\mathrm{full}}} = I_{\mathrm{Tot}_{\mathrm{max}}}(1-\alpha) \tag{5.7}$$

$$\begin{aligned} V_{\mathrm{M}_{\mathrm{full}}} = V_{\mathrm{DD}} &= \frac{Z_0^2}{R_{\mathrm{l}}} I_{\mathrm{M}_{\mathrm{max}}} - Z_0 I_{\mathrm{P}_{\mathrm{max}}} \\ &= I_{\mathrm{Tot}_{\mathrm{max}}} Z_0\left(\frac{Z_0}{R_{\mathrm{l}}}\alpha - (1-\alpha)\right) \end{aligned} \tag{5.8}$$

$$V_{\mathrm{P}_{\mathrm{full}}} = V_{\mathrm{DD}} \tag{5.9}$$

Satisfying (5.2) for V_{M} at both power back-off and full power, yields the well-known condition for the characteristic impedance of the transmission line (Z_0) and the optimum

loading impedance, namely: $Z_0 = R_{l_{opt}}/\alpha$, with $R_l = R_{l_{opt}} = V_{DD}/I_{Tot_{max}}$. Using these values, the loading conditions for the main and peaking device of a (asymmetrical) two-way DPA are defined and can be evaluated as a function of the normalized v_{in} at the power back-off point and at full power, namely:

$$Z_M = \frac{R_{l_{opt}}^2}{\alpha^2 R_l} - \frac{R_{l_{opt}}}{\alpha}\frac{I_P}{I_M} \Rightarrow \left[\frac{R_{l_{opt}}}{\alpha^2}\Big|_{v_{in}=\alpha}, \frac{R_{l_{opt}}}{\alpha}\Big|_{v_{in}=1}\right] \tag{5.10}$$

$$Z_P = R_{l_{opt}}\frac{I_M}{I_P} \Rightarrow \left[\infty\Big|_{v_{in}=\alpha}, R_{l_{opt}}\frac{\alpha}{1-\alpha}\Big|_{v_{in}=1}\right] \tag{5.11}$$

When an ohmic VSWR condition is applied the loading impedance R_l will deviate from its optimum value $R_{l_{opt}}$. For a given VSWR value, the ohmic part of R_l will vary from $R_{l_{opt}}/VSWR$ to $R_{l_{opt}}.VSWR$. For example, when we consider a VSWR of 2, we find, a halving or doubling of the offered R_l, depending on the phase of the offered load reflection coefficient. For the situation that $R_l = 2R_{l_{opt}}$, we find,

$$Z_{M(R_l=2R_{l_{opt}})} = \frac{R_{l_{opt}}^2}{\alpha^2 R_l} - \frac{R_{l_{opt}}}{\alpha}\frac{I_P}{I_M} \Rightarrow \left[\frac{R_{l_{opt}}}{2\alpha^2}\Big|_{v_{in}=\alpha}, R_{l_{opt}}\frac{2\alpha-1}{2\alpha^2}\Big|_{v_{in}=1}\right] \tag{5.12}$$

$$Z_{P(R_l=2R_{l_{opt}})} = R_{l_{opt}}\frac{I_M}{I_P} \Rightarrow \tag{5.13}$$

$$\left[\infty\Big|_{v_{in}=\alpha}, R_{l_{opt}}\frac{\alpha}{1-\alpha}\Big|_{v_{in}=1}\right] \tag{5.14}$$

From this result (5.12) we can conclude that e.g. for a symmetric DPA ($\alpha = 0.5$) at $v_{in} = 1$, the offered impedance to the main device becomes zero, as such entirely obstructing the desired Doherty operation. This high sensitivity of a Doherty amplifier for its provided load is also illustrated in Fig. 5.3, for the symmetrical DPA ($\alpha = 0.5$) case. The related DPA performance such as output power, drain efficiency, load-line of the main output stage, and load-line of the peaking output stage, for $R_l = R_{l_{opt}}$(green), $R_l = 2R_{l_{opt}}$(red), and $R_l = 0.5R_{l_{opt}}$(black) is shown in Fig. 5.3(a), (b), (c), and (d) respectively.

5.2.1. SOLUTION

To cure the Doherty amplifier for ohmic mismatch due to R_l deviations, and restore its basic properties in terms of output power ($P_{out_{max}}$), and efficiency vs. power back-off, the following strategy can be applied. Voltage saturation ($V_M = V_{DD_P}$) should occur at the power back-off point for the main device when delivering its $P_{out_{M\,back}}$. At full power, voltage saturation should occur for both the main ($V_M = V_{DD_P}$) and peaking device ($V_P = V_{DD_P}$) when delivering $P_{out_{M\,max}}$ and $P_{out_{P\,max}}$, respectively to the loads Z_M

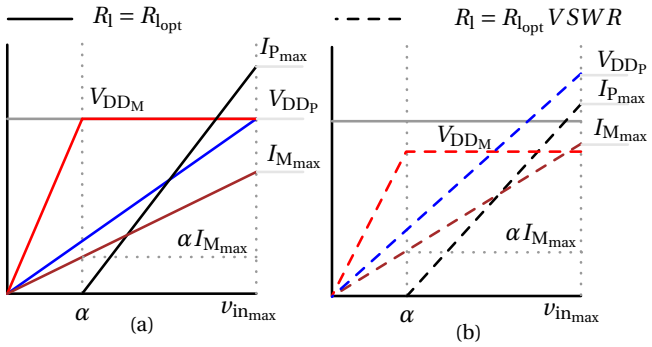

Figure 5.4. (a) An idealized alternating current voltage and current profile vs. input voltage for an asymmetric DPA under the nominal (optimum) loading condition $R_l = R_{l_{opt}}$. (b) Modified AC voltage and current profile condition vs. input voltage to maintain 'ideal' DPA operation under miss-match condition $R_l = R_{l_{opt}}.VSWR$ (in the graph we have used $VSWR = 2$ and $\angle\Gamma_l = 0$).

5

and Z_P that result from the applied R_l. To enable these conditions for a R_l value that deviates from $R_{l_{opt}}$, modification of the individual bias supply conditions of the main and peaking devices, V_{DD_M} and V_{DD_P} respectively is needed. Also $I_{M_{max}}$ and $I_{P_{max}}$ will be modified. Consequently, we use for the ohmic case the following conditions for the powers to be delivered in back-off and peak-power,

$$P_{out_{M\,back}} = \frac{1}{2} V_{M back} I_{M back} \tag{5.15}$$

$$P_{out_{P\,full}} = \frac{1}{2} V_{P full} I_{P full} \tag{5.16}$$

Using the assumptions above, for a purely ohmic load and sinusoidal signal, we find using the fact that $P_{out_{M\,back}}=V_{DD_M}^2/2\mathrm{Re}(Z_{M back})$, with $Z_{M back}$ given by (11) with I_P=0, yielding:

$$V_{DD_M R_l} = \sqrt{\frac{2P_{out_{M}\,back} R_{l_{opt}}^2}{\alpha^2 R_l}} = V_{DD_M R_{l_{opt}}} \sqrt{\frac{R_{l_{opt}}}{R_l}} \tag{5.17}$$

In which we have used the fact that

$$V_{DD_M R_{l_{opt}}} = \sqrt{\frac{2R_{l_{opt}} P_{out_{M}\,back}}{\alpha^2}} \tag{5.18}$$

which represents the supply voltage for the nominal loading condition (R_l=$R_{l_{opt}}$). The related $I_{M R_l}$ can be found in a similar way, namely,

$$I_{M R_l}\Big|_{v_{in}=\alpha} = \alpha I_{M R_{l_{opt}}} \sqrt{\frac{R_{l_{opt}}}{R_l}}, \tag{5.19}$$

yielding,

$$I_{\mathrm{M}_{\max}R_{\mathrm{l}}} = I_{\mathrm{M}_{\max}\mathrm{R}_{\mathrm{l}_{\mathrm{opt}}}}\sqrt{\frac{R_{\mathrm{l}_{\mathrm{opt}}}}{R_{\mathrm{l}}}}, \tag{5.20}$$

Note that indeed both the $V_{\mathrm{DD}_{\mathrm{M}}}$ as well as $I_{\mathrm{M}_{\max}}$ have been modified to handle the new R_{l} and provide the same power for the main device in the power back-off point. In a similar way, we can find the new conditions for the supply voltage and required current of the peaking device. Again assuming ohmic conditions, sinusoidal signals, and voltage saturation for the peak device at full power, we use for the peak device output power $P_{\mathrm{out}_{\mathrm{P}_{\mathrm{full}}}}$=$V_{\mathrm{DD}_{\mathrm{P}}}/2I_{\mathrm{P}_{\max}}$, and use (2) to find, $V_{\mathrm{DD}_{\mathrm{P}_{\mathrm{full}}}}$=j$Z_0 I_{\mathrm{M}_{\max}}$ yielding,

$$I_{\mathrm{P}_{\max}} = \frac{P_{\mathrm{out}_{\mathrm{P}_{\mathrm{full}}}}}{\mathrm{j}Z_0 I_{\mathrm{M}_{\max}\mathrm{R}_{\mathrm{l}}}} = \frac{P_{\mathrm{out}_{\mathrm{P}_{\mathrm{full}}}}}{\mathrm{j}Z_0 I_{\mathrm{M}_{\max}\mathrm{R}_{\mathrm{l}_{\mathrm{opt}}}}\sqrt{\frac{R_{\mathrm{l}}}{R_{\mathrm{l}_{\mathrm{opt}}}}}} \tag{5.21}$$

Since $P_{\mathrm{out}_{\mathrm{P}_{\mathrm{full}}}}$ should stay unchanged we can use the fact that $I_{\mathrm{P}_{\max}\mathrm{R}_{\mathrm{l}_{\mathrm{opt}}}} = \frac{P_{\mathrm{out}_{\mathrm{P}_{\mathrm{full}}}}}{\mathrm{j}Z_0 I_{\mathrm{M}_{\max}\mathrm{R}_{\mathrm{l}_{\mathrm{opt}}}}}$, which yields:

$$I_{\mathrm{P}_{\max}\mathrm{R}_{\mathrm{l}}} = I_{\mathrm{P}_{\max}\mathrm{R}_{\mathrm{l}_{\mathrm{opt}}}}\sqrt{\frac{R_{\mathrm{l}_{\mathrm{opt}}}}{R_{\mathrm{l}}}} \tag{5.22}$$

consequently, we find (5.23) which completes our solution for load-insensitive operation. From the resulting equations we can note that the derived solution is independent of α.

$$V_{\mathrm{DD}_{\mathrm{P}}\mathrm{R}_{\mathrm{l}}} = V_{\mathrm{DD}_{\mathrm{P}}\mathrm{R}_{\mathrm{l}_{\mathrm{opt}}}}\sqrt{\frac{R_{\mathrm{l}}}{R_{\mathrm{l}_{\mathrm{opt}}}}} \tag{5.23}$$

In Fig. 5.4 we show the ideal Doherty voltage and current profile for maintaining the ideal DPA operation when $R_{\mathrm{l}} = R_{\mathrm{l}_{\mathrm{opt}}}$ and $R_{\mathrm{l}} = R_{\mathrm{l}_{\mathrm{opt}}}.VSWR$.

5.2.2. IDEAL-DOHERTY RECOVERY PROCEDURE

The recovery procedure for restoring the ideal Doherty performance under VSWR conditions can be summarized as follows. Given a DPA with an optimum load impedance $R_{\mathrm{l}} = R_{\mathrm{l}_{\mathrm{opt}}}$, then for a given VSWR condition, we find for the DPA performance recovery when the DPA sees an ohmic impedance,

- $R_{\mathrm{l}} = R_{\mathrm{l}_{\mathrm{opt}}}VSWR$
  - Main stage
    - Scale down V_{DD} by $(VSWR)^{1/2}$
    - Scale up input-drive by $(VSWR)^{1/2}$
  - Peaking stage
    - Scale up stage V_{DD} by $(VSWR)^{1/2}$

- Scale down input-drive by $(VSWR)^{1/2}$

- And when, $R_l = R_{l_{opt}}/VSWR$, we find
  - Main stage
    - Scale up V_{DD} by $(VSWR)^{1/2}$
    - Scale down input-drive by $(VSWR)^{1/2}$
  - Peaking stage
    - Scale down V_{DD} by $(VSWR)^{1/2}$
    - Scale up input-drive by $(VSWR)^{1/2}$

A simulation example of this recovery procedure when the DPA is subjected to a $2R_{l_{opt}}$ load impedance with (green) and without (red) tuning the voltage and drive parameters for the main and peaking device is shown in Fig. 5.3. The resulting DPA output power, drain efficiency, and main and peaking stages load-line plots after correction are also shown (green) in Fig. 5.3(e), (f), (g), and (h), respectively. It can be seen that the proposed technique can indeed recover the ideal Doherty operation and does not suffer from any performance degradation. However, in a practical implementation, the used transistor technology needs to handle increased breakdown voltage and current levels, which at some point will still constrain the maximum VSWR handling capability of the proposed technique.

5.3. DESIGN DETAILS

A prototype load-insensitive Doherty PA with an impedance matching control loop has been designed and implemented on a Rogers RO4350B substrate with 0.508 mm thickness (see Fig. 5.6). It consists of a symmetrical Doherty topology, using two fully independent drive signals for the main and the peaking devices, a six-port reflectometer, and a parallel resonator with a tunable capacitor (see Fig. 5.5). The maximum voltage ratings of the capacitor switch bank (pSemi) limit the prototype output power to a few watts at most. Further to benefit from a good quality factor of the capacitive-switch bank, the operating frequency was set to 900 MHz. Concerning these constraints, commercially packaged LDMOS devices of the type AFIC901N were selected to implement the main and peaking devices. The inputs of these devices are impedance matched to 50 Ω. The resulting Doherty configuration achieves an output power of 33 dBm from a 5.0 V supply, and has an optimum load impedance ($R_{l_{opt}}$) close to 20 Ω. A $\lambda/4$ transmission line transfers this impedance level to 50 Ω, in order to be compatible with the six-port reflectometer and tunable shunt resonator, similar to the work in [68]. The load impedance fluctuations due to antenna impedance variations, e.g., due to mutual coupling in beam-steering scenarios are considered to be slow (below 100 kHz) when comparing it to the bandwidth of the modulated signal itself (> 1 MHz). Consequently, the dc-dc converters that provide the supply voltages of the main and peaking devices can have limited bandwidth. This allows the use of very energy-efficient dc-dc converters since they do not need to follow the envelope of the modulated signal. Efficiencies as high as 98.4 % have

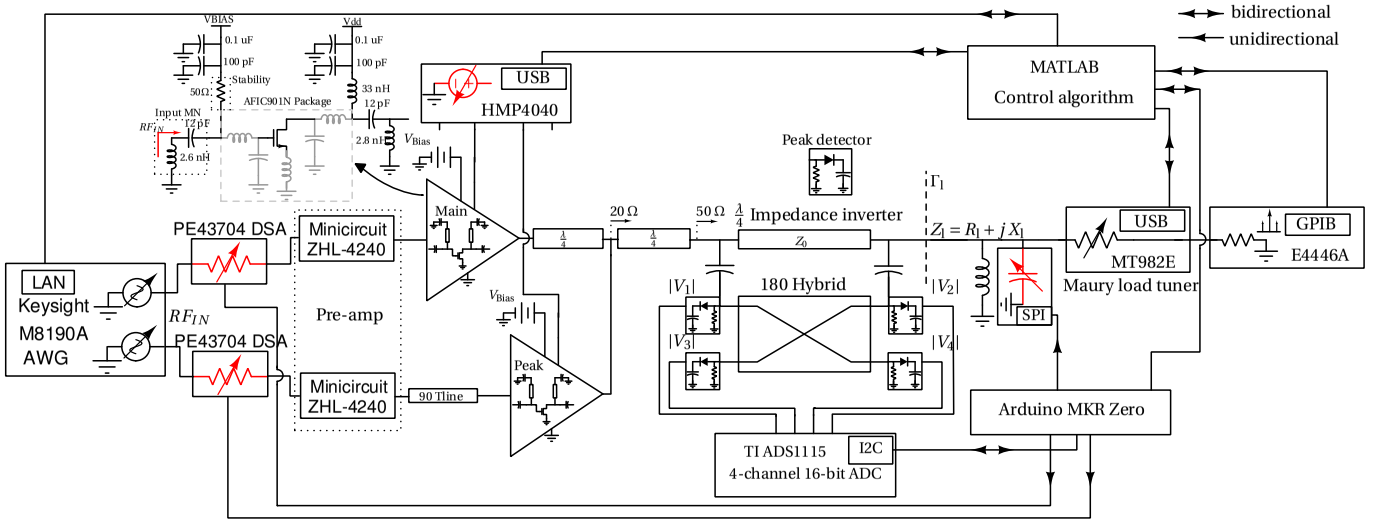

Figure 5.5. The detailed schematic of the Doherty PA, six-port reflectometer with RF peak detectors, and parallel resonator with a tunable capacitor. The measurement instruments and the control loop implementation are also shown.

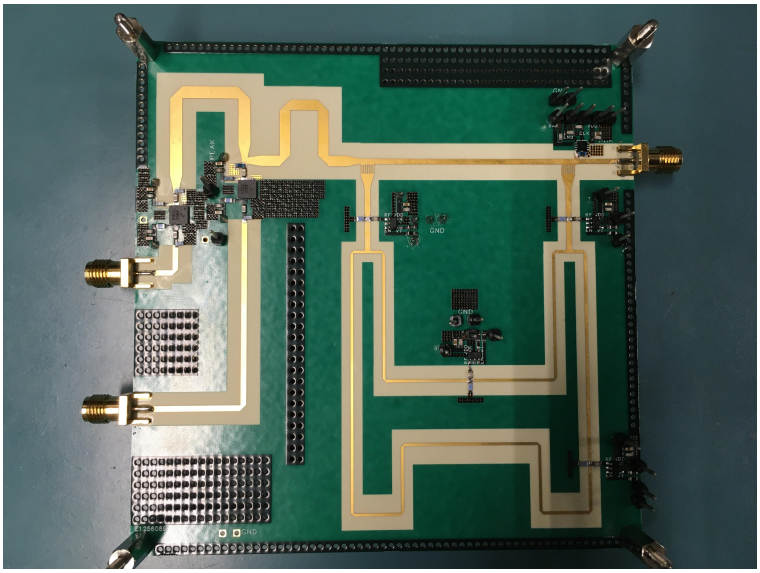

Figure 5.6. The realized PCB including the 900 MHz Doherty LDMOS PA with dual inputs, the six-port reflectometer, and a tunable shunt resonator.

been reported for a dc-dc converter with 500 kHz bandwidth [66]. In this work, the dc-dc supply modulators are considered not to be within the focus of this research and they have been replaced with regular lab supplies, which are controlled via MATLAB. Furthermore, we have simply assumed that they are 100 % efficient setting their dissipated power (P_{SR}) to 0.

5.4. MEASUREMENT RESULTS

The load-insensitive DPA with its measurement setup is shown in Fig. 5.5. It consists of the designed Doherty PA, output match, six-port reflectometer and capacitive switch bank, a dual-channel keysight M8190A arbitrary waveform generator, a Rohde & Schwarz HMP4040 quad-channel power supply, an Agilent E4446A spectrum analyzer, MT982E Maury load tuner and digital tunable attenuator from pSemi with a step of 0.25 dB with a Minicircuit pre-amplifier (ZHL-4240). The instrument control is performed via MATLAB through the general purpose interface bus (GPIB) and universal serial bus (USB) interfaces. An Arduino MKR Zero board based on Cortex-M0+ 32-bit low-power ARM microarchitecture is used to control the tunable pSemi capacitor and the tunable attenuator via a serial peripheral interface (SPI). The voltage readings of the four power detectors are collected using a TI ADS1115 4-channel 16-bit ADC (860 samples/s). Moreover, the power-added efficiency (PAE) reported in this work includes the RF losses in the six-port reflectometer and the tunable capacitor bank. Next, we will evaluate the performance of the Doherty PA under 50 Ω load conditions, followed by a discussion of

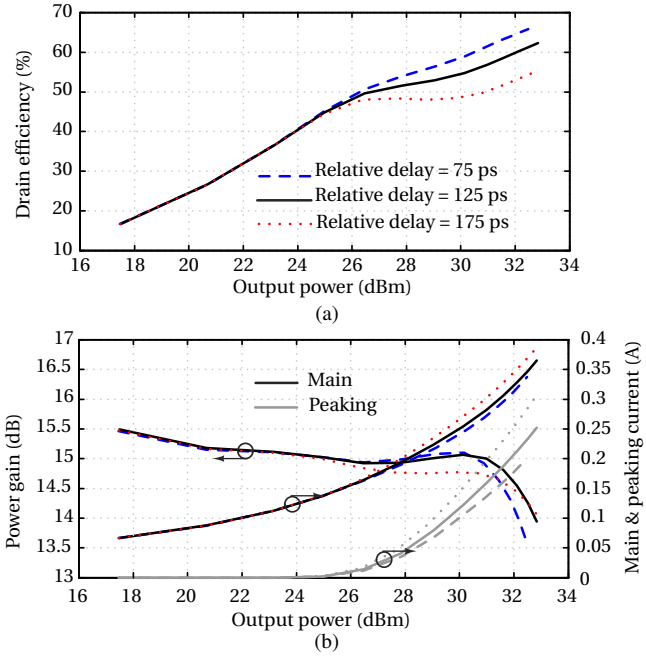

Figure 5.7. Doherty PA (a) drain efficiency, (b) power gain, and main (black) and peaking (grey) stage drain current versus output power for a relative delay adjustment between the main and peaking stage of 75 ps, 125 ps, and 175 ps respectively. $V_{\mathrm{DD_M}} = 5.0\,\mathrm{V}$, $V_{\mathrm{DD_P}} = 5.0\,\mathrm{V}$, $I_{\mathrm{d_q}} = 44\,\mathrm{mA}$ and $f = 900\,\mathrm{MHz}$.

its load-insensitive operation using the control loop. The latter is used to recover the 50 Ω PA operation when the external load impedance is rotated over the 2:1 VSWR circle.

5.4.1. CONTROL LOOP METHOD

The method to recover the nominal 50 Ω performance in the event of load-mismatch has been elaborated in [68]. It is a two-step method. We first regulate the complex load presented to the DPA back to a 'pure' ohmic load (red line in the Smith chart of Fig. 5.1). Next, we adjust the supply voltage and the input drive of the DPA to recover the desired 50 Ω performance in terms of output power, efficiency, and linearity.

SUPPLY VOLTAGE AND INPUT DRIVE CONTROL

As stated, the complex load is first matched to the ohmic case using the tunable resonator with switchable capacitor banks. This is done by monitoring the measured voltages of the six-port reflectometer at port-3 and port-4 i.e., $V_3/V_4 \approx 1$ [68]. In practice, DPA performance will deviate somewhat from the ideal DPA performance under load mismatch, mainly due to device and package parasitics. Consequently, for this work, an offline trained look-up table (LUT) based control algorithm was adopted. The LUT

takes the voltage ratios V_1/V_2 and V_3/V_4 as input, and returns the optimum setting for the switchable-capacitor bank, as well as, the input drive levels and supply voltages for the main and peaking output stages.

This LUT control algorithm is implemented in MATLAB and achieves back the 50 Ω DPA performance within specified tolerances. The measured DPA performance for the load trajectory on the 2:1 VSWR circle, with and without the actuation method, is shown in Fig. 5.8. We have also provided the performance of the DPA when matched to a 50 Ω load for comparison. Fig. 5.8(a), (b), and (c) show the DPA output power, power gain, and drain efficiency from power back-off to beyond the 1 dB compression, for different loading conditions on the VSWR = 2 circle. Fig. 5.8(d), (e), and (f) show, as a function of the load phase for a VSWR = 2 condition the DPA single-tone; output power, power gain, and drain efficiency at 6 dB output power back-off from the 1 dB compression point. For a 64-QAM 4 MHz modulated signal, first a simple static AM-AM and AM-PM based DPD was performed for the DPA when connected to a 50 Ω load. This resulted in a set of pre-distorted drive signals for the main and peaking devices, which remain unaltered in the following VSWR measurements. Fig. 5.8(g), (h), and (i) show the resulting DPA output power, drain efficiency, and EVM in dB when the PA is driven by a pre-distorted 64-QAM 4 MHz signal with an input power of 9 dBm. Moreover, for the same input signals, the DPA ACLR performance is shown for a 2:1 VSWR condition at different phase angles of the load in Fig. 5.9.

From the measurement results it can be concluded that. When activated, the VSWR control loop can recover the DPA performance in terms of output power and gain with a variation of less than ± 0.1 dB for a linear output power of 24.4 dBm. However, it suffers from decreased efficiency at peak output (see Fig. 5.8(a)) for some of the phase points $\angle\Gamma_l = \{0, 180, 360\}$. Closer inspection shows that this degradation can be related to conditions where the active devices need to handle larger currents, yielding higher I^2R losses. Moreover, for the cases where R_l is well above (> 50 Ω) insertion loss of the shunt resonator increases, which also negatively impacts the efficiency. At 6 dB power back-off, these phenomena are much less pronounced (see Fig. 5.8(d), (e), and (f)) simply due to lower peaking currents and voltages involved.

It is known that the linear performance of a PA/DPA when excited by a modulated signal is load-dependent. Consequently, load variation in a mMIMO beamforming array due to beam-forming action will require complex cross-over DPD [49] to correct for these changes. Moreover, it was shown in [50] that overall DPD power consumption in these cases can exceed the overall PA power consumption, even in the case of just two antennas. In this work, we show that we can maintain the DPA performance and linearity on a VSWR circle without employing these complex DPD schemes. Namely, when a $VSWR = 2$ condition is applied to the DPA, we see that with the correction loop activated, we can keep the output power constant (see Fig. 5.8(g)), as well as, the efficiency (see Fig. 5.8(h)). Also, we find an improvement in the linearity in terms of EVM (Fig. 5.8(i)), however, it is still somewhat degraded at $\angle\Gamma_l = \{135, 180\}$. This is also true for the related ACLR (see Fig. 5.9). Compared to the 50 Ω reference case, which was used to extract the DPD correction, which is kept constant afterward, this degradation can be traced back for these angles to increased changes in AM-PM distortion (see Fig. 5.10(a)). Note that these changes in AM-PM behavior appear to be more significant,

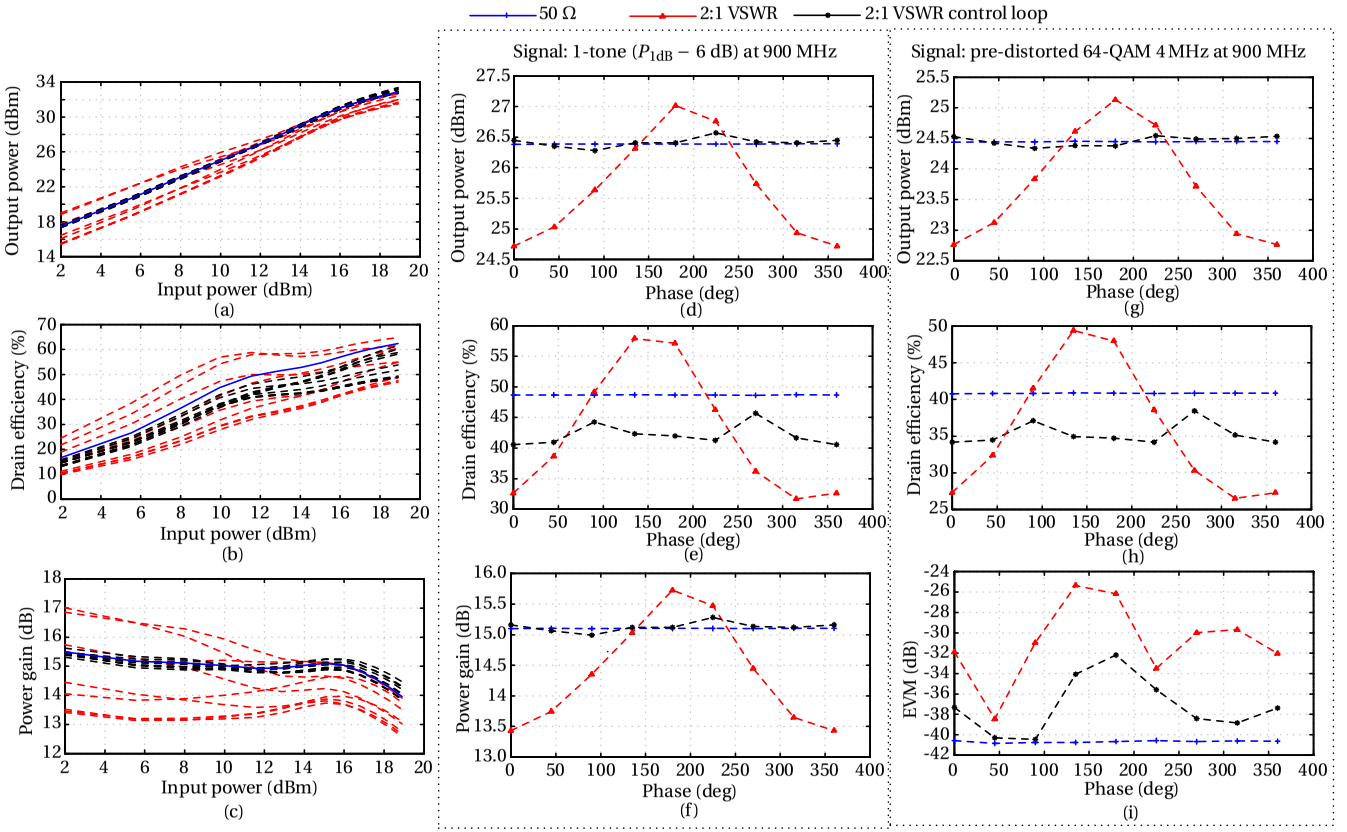

Figure 5.8. DPA performance when the load is matched to the 50 Ω, and on a 2:1 VSWR circle for a phase steps of 45° with and without the proposed control loop method. (a), (b), and (c) show the DPA output power, power gain, and drain efficiency vs. input power. (d), (e), and (f) show the DPA output power, drain efficiency, and power gain when the DPA at 6 dB power back-off from the output power 1 dB compression point. (g), (h), and (i) shows the DPA output power, drain efficiency, and EVM when the DPA is driven by a pre-distorted 64-QAM 4 MHz with an input power of 9 dBm at 900 MHz.

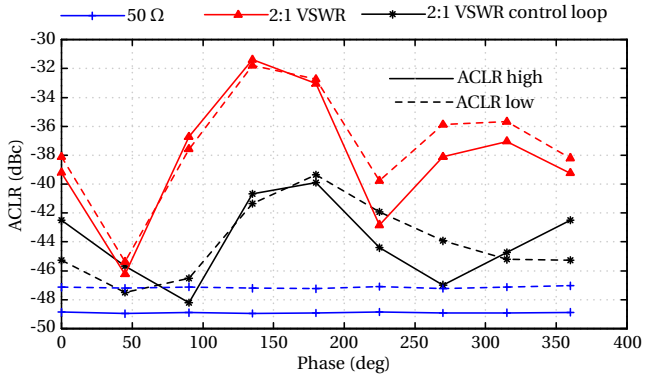

Figure 5.9. ACLR at 1 MHz offset using a pre-distorted 64-QAM 4 MHz signal with an input power of 9 dBm for DPA operation at 50 Ω. The same input signals are used in the measurements of the 2:1 VSWR condition at different phase angles of the load, with and without the VSWR control loop.

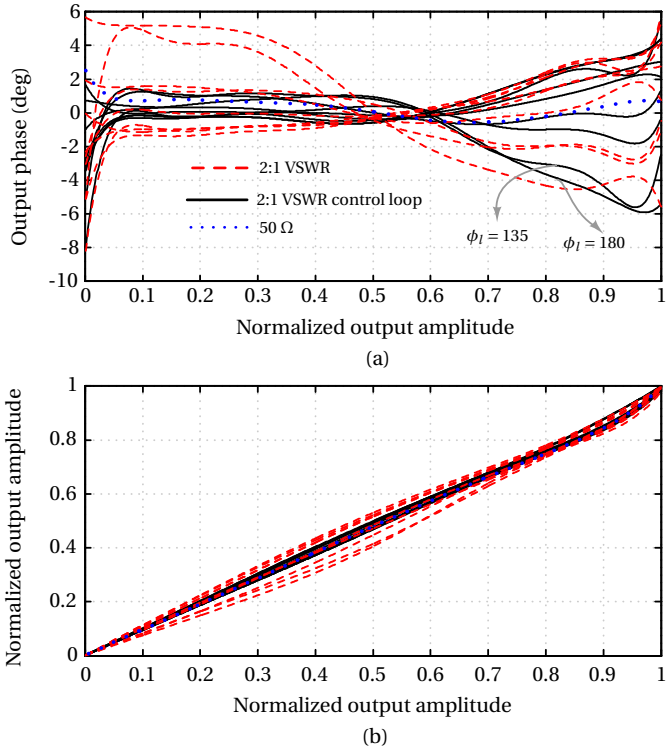

Figure 5.10. Dynamic, (a) output phase (AM-PM) distortion in degree, and (b) normalized output amplitude extracted using a pre-distorted 64-QAM 4 MHz signal with an input power of 9 dBm for DPA operation at 50 Ω, 2:1 VSWR, and 2:1 VSWR with control loop.

Table 5.1. Comparison with the state of the Art Load-insensitive DPAs

Comparison	**This work**		[24] TMTT-2021		[70] TMTT-2021		[22] TMTT-2020	
Technique	**Proposed**		QB-DPA ‡		Supply + Input drive-DPA ‡		Doherty-Balanced ‡	
Technology	**LDMOS-PCB**		GaN-PCB		GaN-PCB		GaN-PCB	
Impedance detector	**yes**		no		yes		no	
Freq GHz	**0.9**		3.5		3.6		3.5	
Z_l/VSWR	50 Ω	**2:1**(0°-360°)	50 Ω	2:1(0°-360°)	50 Ω	25 Ω-100 Ω	50 Ω	2:1(0°-360°)
CW signal	**1-tone CW**		1-tone CW		1-tone CW		1-tone CW	
$P_{out_{1dB}}$ dBm	**32.3**	**32.3[0.4,-0.2]**	40.7	38.8-40.4	43.5	42.6-43.4	41.9†	NR
DE/PAE %	**61/60**	**48-59/47-58**	68.4/-	51-59/-	68.0/-	54-64/-	70/-†	NR
Modulated signal	**64-QAM** 4 MHz		64-QAM 20 MHz		LTE 5 MHz		LTE 10 MHz	
DPD	**static**		no		no		no	
PAPR	7.3		NR		5.5		8.4	
P_{out} dBm	**24.4**	**24.4±0.1**	35	33-34.2	NR	NR	34.5	32.5-35.1
DE_{avg}/PAE_{avg} %	**41/40**	**34-39/33-38**	45	32.5-42.5/-	46.4/-	40.2-43/-	42.4/-	22-39/-
$ACLR$ dBc	**-46.9**	**< -39.3**	-41.0	NR	-31.8	<-30.1	-37	NR
EVM dB/%	**-40.9/**	**< -32.3/**	-/1.48	-/1.75-4	NR	NR	-32.5/	<-26/

‡ results are estimated from plots; NR = not reported; † saturated performance; †† with PA 50 Ω performance (VSWR 1:1) as the reference, the reflection loss for a 2:1 VSWR will be 0.51 dB;

than the spread found for the related AM-AM (see Fig. 5.10(b)) with an activated correction loop. This can be understood by considering the impact of the non-linear output capacitance (C_{ds}) of the main and peaking devices. Namely, it acts as a catalyst for the output phase distortion. In a practical DPA, the output phase is a function of R_l, g_m, C_{gs}, and C_{ds} (of which the latter has a dominant role) [71]. Consequently, a change in C_{ds} and R_l (due to active load modulation) yields a change in the phase distortion [71] (see appendix for further details).

In Table 5.1, a comparison with the state-of-the-art load-insensitive Doherty PAs is provided. An ideal isolator performance and class-AB PA performance [68] is also provided as a reference. It can be seen that the balanced configuration using DPA, as branch PAs [23] is only effective in deeper power back-off (P_{1dB}-PAPR). Switching between the Doherty-Balanced [22] configuration is capable of providing higher output power when compared to the balanced-only configuration. However, this is achieved at the expense of degraded efficiency and EVM. Reconfigurable DPAs [27, 28] are much more resilient than balanced configuration, yet the performance degradation is much higher when compared to their 50 Ω performance. Although [68], using a class-AB stage with "adjustable supply and TMN" approaches the 50 Ω performance it does not offer any back-off efficiency enhancement. The proposed technique achieves the best performance in terms of constant linear output power with a variation of only ± 0.1 dB, with an average drain efficiency of ≈ 35 % over the 2:1 VSWR circle which is very close to the efficiency that would be achieved with this DPA in combination with an isolator (36 %) on the 2:1 VSWR circle compared to the 50 Ω case.

5.5. CONCLUSION

This chapter has demonstrated a Doherty PA with built-in self-healing capability. The DPA is insensitive to load variation by tuning the input drive level and supply voltage of the main and peaking stages in a mirrored approach. As a result, it was shown, both in theory and experiments, that we can always recover the ideal Doherty operation for any load mismatch. The prototype DPA and LUT-based fully-automated control algorithm was able to recover from the load variations on a 2:1 VSWR circle and could reduce the gain and output power variation to less than $\pm$ 0.1 dB (driven by a complex modulated signal) when compared to the 50 Ω reference case. Furthermore, it was shown that the proposed method allows performing DPD on this Doherty when connected to a nominal 50 Ω condition, and reuse the same DPD correction without any modification in VSWR conditions, without any significant linearity degradation. To maximally benefit from the proposed technique, it is best to use devices for the DPA output stages with sufficient performance headroom in breakdown voltage, and maximum current handling while offering a relatively constant output capacitance over their operating range.

6

LOAD-INSENSITIVE WIDEBAND INVERTED DOHERTY PA

6.1. INTRODUCTION

The ever-growing demand for higher data rates is being addressed through the increased use of spectrally efficient signals, larger modulation bandwidths, higher operating frequencies, and spatial diversity based on beam steering. This combination of techniques enforces stringent performance requirements on the radio frequency (RF) power amplifiers (PAs) which need to amplify signals with large peak-to-average power ratio (PAPR), video bandwidth, RF bandwidth, and be tolerant to changing VSWR conditions in handsets from the antenna input impedance variation due to hand effect [12] or in base-stations, due to the undesired mutual coupling in the multi-antenna beam steering structures [72, 73].

The Doherty power amplifier (DPA) is a popular choice to satisfy most of these requirements [39, 40], since it can efficiently amplify signals with large video bandwidth and PAPR; moreover, its high bandwidth operation is not limited by the need for a fast, as well efficient dc-modulator as required in the envelope tracking architecture [38]. However, conventional DPAs can be used only over a narrow RF bandwidth. Therefore, inverted Doherty PA (IDPA) topologies offering higher RF bandwidths have gained popularity [74–77]. Unfortunately, DPAs are very sensitive to changing VSWR conditions [67, 78]. Various techniques exist in the literature to overcome the VSWR sensitivity of the DPA/PA. [1] These can be broadly classified into five groups.

The first and most traditional technique is using an isolator to break the reciprocity of the network, thereby isolating the DPA from the load and presenting a constant impedance to the DPA. However, isolators are bulky, expensive, and need a third port termination to dissipate the reflected power from load mismatch. They also have a magnetic field around them, posing integration challenges. Recent works have demonstrated magnetic-free isolators, but those suffer from higher insertion loss [79, 80]. Secondly, in theory, a

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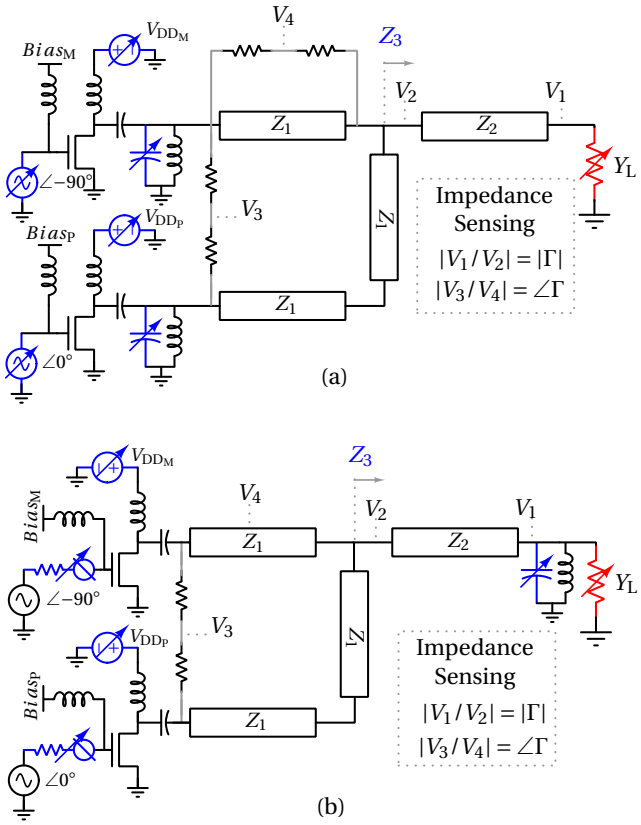


Figure 6.1. The proposed (a) load-insensitive IDPA with the wideband impedance sensor embedded into its output power-combining network. The voltage ratios $|V_1/V_2|$ and $|V_3/V_4|$ point to the $|\Gamma|$ and $\angle\Gamma$ respectively and (b) the finally implemented circuit with digitally tunable input amplitude and phase.

tunable matching network (TMN) can correct for changing VSWR conditions and omits any reflection losses [14–16, 18, 62, 63]. However, a successful low-loss TMN realization relies heavily on the availability of tunable components with extremely high-Q, high-tuning range and breakdown voltage [68]. Therefore, practical TMNs have high insertion losses [14–16, 18, 62, 63]. To reduce the insertion loss of TMN, a hybrid approach of using an adjustable supply voltage and input drive in combination with a low-loss tunable resonator (TR) was proposed in [68] for a class-B PA and in [81] for a DPA, but only across a narrow RF bandwidth. Thirdly, a balanced configuration can function as an isolator, but does this correctly only in power back-off conditions, as its branch PAs still see (opposite) changing loading conditions [21, 23]. Fourthly, re-configurable DPAs, have recently received considerable interest. Various concepts have been reported, namely, transconductance (g_m) and phase adjustments (tunable phase shifter) of the carrier and

peaking amplifiers [27]. A reconfigurable series/parallel switchable Doherty [25, 28]. In addition, to enhance the performance of this concept even more, a switchable series/parallel Doherty using a coupler with complex impedance termination at the isolation port and adjustable gate bias is proposed in [24]. Switching between a balanced PA and DPA configuration using a silicon-on-insulator (SOI) based single-pole-double-throw (SPDT) switch [22], and multi-port active load-pull [29]. All these techniques do not fully restore the DPA performance from the impact of the applied load mismatch but rather try to "soften" the consequences of this load mismatch. Fifthly, concepts have been introduced that strongly rely on the use of digital pre-distortion (DPD). Namely, it is known that the load sensitivity of a DPA will affect its output power, when applied in a beam-forming antenna array [82] causing (large) variations in the direction of the main beam, its nulls, and side lobes levels. Correcting this change requires a complex cross-over DPD [49], which increases the overall power consumption. For example, it was shown in [50] that the DPD-related power consumption can exceed the overall PA power consumption, even when handling two antennas.

To overcome the formerly discussed challenges of the DPA's load-sensitivity. This chapter proposes a wideband DPA load correction technique based on an inverted Doherty power amplifier (IDPA) with embedded wideband load-mismatch sensing in its output power combining network (OPCN) (see Fig. 6.1). It can act on the (slow, milli/micro-second) load changes caused by the hand effect or beam steering. It builds on the techniques proposed in [68, 70, 81]. This work builds on the low-loss TR from [68] and load insensitive DPA concept from [70, 81] and extend them to wideband operation. The most important contributions of this work compared to the prior state-of-the-art [24, 68, 70, 81] are,

1. A low-loss tunable resonator (TR) facilitating low-Q impedance matching across VSWR and frequency has been integrated into a wideband inverted Doherty power combiner to present ohmic loading conditions to the main stage under all conditions.

2. An embedded tunable phase shifter in the input allows realignment of the main and peaking stage output currents across VSWR and frequency, lowering the requirements on the capacitance-tuning range and Q-factor of the TR.

3. The novel, wideband impedance sensor described in Chapter 2, section 3.3, is embedded in the power combiner to implement this technique with minimum overhead.

The proposed DPA combination provides so far, unseen functionality. Namely, a standalone DPA capable to deliver constant output power over the full VSWR ≤ 2 range and the IDPA bandwidth, while simultaneously improving drain efficiency and linearity. The realized demonstrator features a single RF input, and single external supply, and has embedded mismatch VSWR detection. As such, it allows the use of an unaltered $50\,\Omega$ DPD correction set for any load within the 2:1 VSWR (0°-360°) circle. Furthermore, the phase control is also helpful in accommodating the relatively large changes in the output capacitance [83] of the PA stages when adjusting their supply voltages.

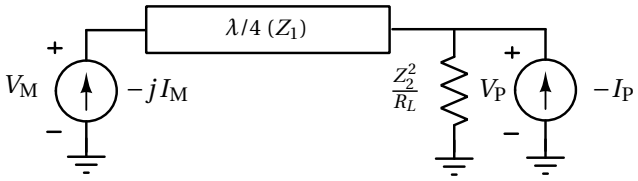


Figure 6.2. IDPA circuit (Fig. 6.1(a)) modeled as an ideal DPA circuit for the center frequency of operation.

6.2. WIDEBAND LOAD-INSENSITIVE IDPA

In this section, the IDPA performance is analyzed, and it is shown that the proposed technique can recover the IDPA performance from load mismatch over its entire fractional operation bandwidth. To analyze the proposed circuit of Fig. 6.1, the main and peaking stages are modeled as ideal current sources. At its center frequency the circuit in Fig. 6.1 can be reduced to the configuration shown in Fig. 6.2. Using the transmission line ABCD parameters [56] and the circuit shown in Fig. 6.2, the following matrix is found

$$\begin{bmatrix} V_M \\ -jI_M \end{bmatrix} = \begin{bmatrix} 0 & jZ_1 \\ j(1/Z_1) & 0 \end{bmatrix} \begin{bmatrix} V_P \\ I_P + V_P[R_L/(Z_2)^2] \end{bmatrix}. \tag{6.1}$$

Using (6.1), the voltages across the main and peaking PA stages for ohmic loading conditions are found to be,

$$V_P = -Z_1 I_M\ (a),\ V_M = -jZ_1(I_M \frac{Z_1 R_L}{Z_2^2} - I_P)\ (b). \tag{6.2}$$

From (6.2(a)) and (6.2(b)) and the topology shown in Fig. 6.2 it can be observed that at the center frequency, the circuit is basically equivalent to [70, 81]. To make the DPA insensitive to load variation at its center frequency of operation, the procedure in [70, 81] needs only minor adjustments. Namely, the required supply voltages (V_{DD_M,R_L}, V_{DD_P,R_L}) and current drives (I_{M,R_L}, I_{P,R_L}) needed to handle an arbitrary load (R_L), can be found by keeping the main and peak PA output powers constant ($P_{out_M} = 0.5 V_M I_M$) in power back-off ($I_P = 0$) and at peak power conditions. Using (6.2(a)) and (6.2(b)), and expressing these quantities in terms of the nominal loading condition ($R_{L_{opt}}$) with voltages (V_{DD_M}, V_{DD_P}) and currents (I_M, I_P), yields:

$$V_{DD_M,R_L} = V_{DD_M}\sqrt{\frac{R_L}{R_{L_{opt}}}}\ (a),\ I_{M,R_L} = I_M\sqrt{\frac{R_{L_{opt}}}{R_L}}\ (b) \tag{6.3}$$

$$V_{DD_P,R_L} = V_{DD_P}\sqrt{\frac{R_{L_{opt}}}{R_L}}\ (a),\ I_{P,R_L} = I_P\sqrt{\frac{R_L}{R_{L_{opt}}}}\ (b). \tag{6.4}$$

The output power and drain efficiency can be determined by using (6.1) and (6.2) to obtain the loading impedance of the main (Z_M) and peaking (Z_P) stage and substituting

them in (6.5), (6.6), and (6.7) where $I_{\mathrm{Mfund,R_L}}$ and $I_{\mathrm{Pfund,R_L}}$ are the amplitudes of the fundamental components of $I_{\mathrm{M,R_L}}$ and $I_{\mathrm{P,R_L}}$,

$$P_{\mathrm{out}} = \frac{1}{2} I^2_{\mathrm{Mfund,R_L}} \mathrm{Re}(Z_{\mathrm{M}}) + \frac{1}{2} I^2_{\mathrm{Pfund,R_L}} \mathrm{Re}(Z_{\mathrm{P}}) \tag{6.5}$$

while the overall dc-power consumption can be calculated using the (average) dc-currents of the main and peak devices. For ideal class-B operation (rectified current sine-wave) these can be written in terms of their fundamental amplitude and supply voltages (6.6) allowing the calculation of the efficiency (6.7).

$$P_{\mathrm{dc}} = \frac{2}{\pi} (I_{\mathrm{Mfund,R_L}} V_{\mathrm{DD_M,R_L}} + I_{\mathrm{Pfund,R_L}} V_{\mathrm{DD_P,R_L}}) \tag{6.6}$$

$$\eta_{\mathrm{drain}}(\%) = \frac{P_{\mathrm{out}}}{P_{\mathrm{dc}}} 100. \tag{6.7}$$

To verify the former principle of operation, the IDPA schematic of Fig. 6.1(a) is used with the following nominal circuit parameters; $V_{\mathrm{DD_M}} = 6.4\,\mathrm{V}$, $V_{\mathrm{DD_P}} = 6.4\,\mathrm{V}$, $g_{\mathrm{m}} = 0.64\,\mathrm{S}$, and the transmission line impedances set to; $Z_1 = 20\,\Omega$ and $Z_2 = (25 Z_1)^{0.5}$. The transmission line Z_2, acts only as a pre-match, converting the external (nominal) $50\,\Omega$ load to Z_3, which needs to be $Z_1/2$ (representing the conventional symmetrical Doherty matching conditions). Furthermore, all the harmonics are short-circuited (ideal class-B operation).

Using these settings, the IDPA performances is tested for the $50\,\Omega$ nominal loading condition across its fractional bandwidth, which is defined in this work by the frequencies at which the output power drops by 1 dB, and was found to be $\approx 22\,\%$ centered around 900 MHz frequency. The simulated IDPA performances with ideal components for its nominal loading $R_{\mathrm{L_{opt}}}$, in terms of output power and drain efficiency at 900 MHz (solid gray line), and 845 MHz (dashed blue line) are shown in Fig. 6.3. Next, at its design center frequency (900 MHz), the IDPA is subjected to ohmic mismatch ($R_{\mathrm{L}} = 100\,\Omega$), yielding a performance degradation (see Fig. 6.3(a) and 6.3(b), dashed gray line). Using (6.3) and (6.4) it is possible to recover and approach the ideal Doherty characteristics by adjusting the supply voltage and input drive of the DPA branches in a mirrored fashion (solid gray line). For complex loads, it is also possible to recover the performance, by first compensating for the reactance/susceptance part by using a low-loss TR/TMN [81] (see Fig. 6.1(a)). Next, the remaining ohmic (mismatch) can be handled again by adjustment of the supplies and input drive levels using (6.3) and (6.4). However, these techniques work only over a narrow frequency band. Moving away from the design frequency even at ohmic loads, the IDPA power combining network will present non-ohmic loading conditions to its PA branches. This is verified in simulation by subjecting the IDPA operating at 845 MHz to a mismatched load of $100\,\Omega$. This is shown in Fig. 6.3 (dashed-dotted black line). It can be observed that both the IDPA output power and drain efficiency degrade considerably. The supply and input drive adjustment technique using (6.3) and (6.4) is applied to recover the performance. It can be seen that it only partially recovers the performance (dotted green line). The complex impedance seen by the main stage ($Z_{\mathrm{L_M}}(f)$)

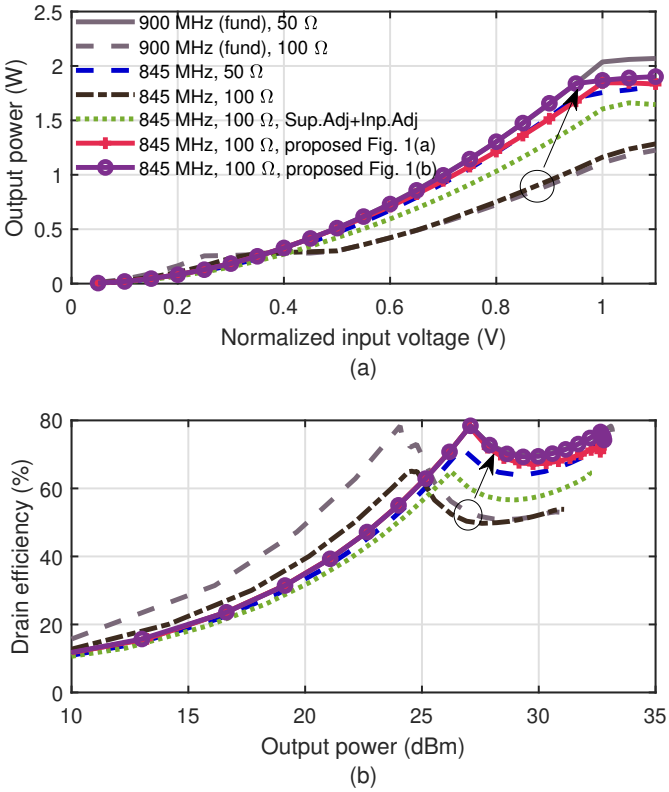


Figure 6.3. Simulated inverted Doherty (a) output power in watts and (b) drain efficiency, assuming ideal class-B operation across bandwidth and impedance mismatch, for four cases. 1) IDPA operated at its center frequency of 900MHz and load set to its nominal value of 50 Ω, 2), load mismatched to 100 Ω @ 900 MHz, 3) load mismatched to 100 Ω @ 845 MHz with input drive and supply adjustment for the main and peaking stage, and 4) load mismatched to 100 Ω @ 845 MHz with input drive and supply adjustment along with TR/TMN matching to the ohmic line.

as a function of frequency in power back-off (peak stage turned off) can be derived as follows,

$$Z_{\mathrm{L_M}}(f) = Z_1 \frac{Z_{\mathrm{L_4}}(f) + \mathrm{j}Z_1 \tan(\frac{\pi}{2} f/f_0)}{Z_1 + \mathrm{j}Z_{\mathrm{L_4}}(f)\tan(\frac{\pi}{2} f/f_0)}. \tag{6.8}$$

where, $Z_{\mathrm{L_4}}(f) = Z_{\mathrm{L_2}}(f) \,||\, Z_{\mathrm{L_3}}(f)$, $Z_{\mathrm{L_3}}(f) = -\mathrm{j}Z_1 \cot(\pi f/f_0)$, and $Z_{\mathrm{L_2}}(f)$ in (6.9) is a function of Z_{L}.

$$Z_{\mathrm{L_2}}(f) = Z_2 \frac{Z_{\mathrm{L}} + \mathrm{j}Z_2 \tan(\frac{\pi}{2} f/f_0)}{Z_2 + \mathrm{j}Z_{\mathrm{L}} \tan(\frac{\pi}{2} f/f_0)}. \tag{6.9}$$

The theoretical/simulated impedance profile of the main stage across frequency as pro-

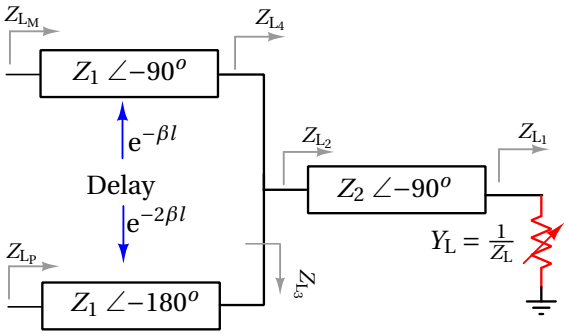


Figure 6.4. IDPA OPCN (see Fig. 6.1) used to formulate the compensating shunt susceptance and relative phase between main and peaking stages as a function of frequency.

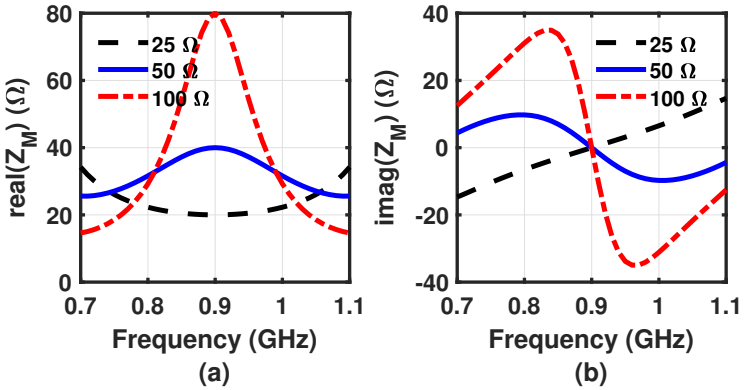


Figure 6.5. Impedance offered to the main stage vs. frequency. (a) Real part and (b) imaginary part in power back-off.

vided by the output power combiner in deep-power back-off is shown in Fig. 6.5. It can be observed that the main stage impedance is ohmic only at the center frequency (f_0) of operation. This is especially the case when dealing with a higher load impedance (e.g., 100 Ω). The main stage sees a varying, highly complex load vs. frequency in this case. To also handle this condition, we propose to compensate for the complex loading across

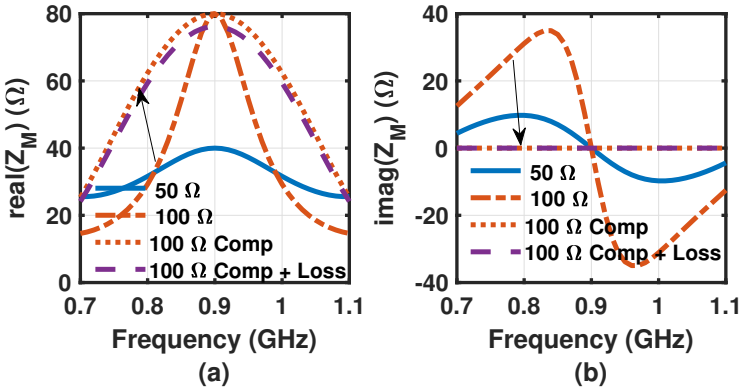


Figure 6.6. Impedance offered to the main stage vs. frequency. (a) Real part and (b) imaginary part after matching (100 Ω load) to the ohmic line using a TR/TMN with and without loss (see Fig. 6.1).

the main stage using a low-loss TR (see Fig. 6.1(a)). The required susceptance (B_{M_X}) to be compensated across frequency at the main stage (see Fig. 6.1(a)) can be determined using the impedance presented to the main stage $Z_{L_M}(f)$ (see Fig. 6.4).

$$B_{M_x}(f) = -\mathrm{Im}[\frac{1}{Z_{L_M}(f)}]. \tag{6.10}$$

By doing this (using a loss-less TR), an ohmic loading impedance can be maintained at the main stage (for e.g., 100 Ω load) as shown in Fig. 6.6(a) and 6.6(b). The impact of losses in the TR (assuming a tunable capacitor with a quality factor of 20) is also shown (dashed purple line). The required supply voltages and current drives can be found by substituting $R_L = \{[1]/\mathrm{Re}[1/Z_{L_M}(f)]\}$ in (6.3) and (6.4). Moreover, low-loss TR can also be used at the peaking stage to compensate for the reactive loading (see Fig. 6.1(a)). Consequently, it is possible by using the proposed technique to recover the IDPA performance across the fractional bandwidth of interest. This is verified using the simulation results shown in Fig. 6.3. It can be seen that for the 845 MHz frequency of operation, the proposed technique not only follows the 50 Ω loading output power of the IDPA for the mismatched 100 Ω loading case, it also improves the efficiency (> 15 % compared to the technique in [70, 81]) in the power back-off. However, having multiple tunable components in the output power combining stage also increases the losses in practical implementations due to their finite quality factor. To reduce the number of tunable components required, the circuit in Fig. 6.1(b) is proposed, which has the TR placed at the Z_L port. This placement lowers the currents flowing in the OPCN under (highly) reactive VSWR loading conditions, as such lowering the losses. The required susceptance $B_{M_X}(f)$

in this configuration can be found by equating the imaginary component of $Z_{L_M}(f)$ to be zero i.e., $\mathrm{Im}[Z_{L_M}(f)] = 0$ and solving for $B_{M_X}(f)$. The required supply voltages and current drives can be found again by substituting $R_L = \{[1]/\mathrm{Re}[1/Z_{L_M}(f)]\}$ in (6.3) and (6.4). Note that in this analysis, we have assumed the TR to be lossless. When the TR has losses, this can be modeled as an extra shunt conductance in parallel to R_L, so effectively lowering its value.
Moreover, the non impedance matched transmission lines in the path of the main and peaking stages provide a frequency-dependent delay. This delay needs to be compensated by the adjustable phase shifter for perfect in-phase current combining of main ($I_M \exp(-j\phi_M)$) and peaking ($I_P \exp(-j\phi_P)$) stage current vectors. The following frequency-dependent phase relationship can be derived using the circuit in Fig. 6.4, when accounting for the transmission line frequency-dependent phase delay.

$$\phi_M - \phi_P = -\frac{\pi}{2}\frac{f}{f_0}. \tag{6.11}$$

Moreover, it can be summarized that the TR is used to present ohmic loads to the main and peaking stages at the center frequency of operation. At off-center frequency, TR is used to present an ohmic load for the main stage while the digitally adjustable phase shifter is used to (re)align the main and peaking stage's current summation in the output power combining network (e.g., see Fig. 6.1(b)). Using this technique, the lowest loss from a TR/TMN in practical circuit implementation can be achieved. For practical implementations, a look up table (LUT) can be created that stores the required TR capacitance value, the relative phases between the main and peaking stages, and also their supply voltages with input drive profile for the expected range of load impedance's (Z_L) and operational frequency (f). The impedance sensor voltage ratios can provide the link to the load impedance and is used for the LUT. Furthermore, the LUT data content can be adjusted to account for the parasitic in a practical implementation.

6.3. DESIGN DETAILS

To demonstrate the concepts described in Section 6.2, a prototype IDPA with a digital control loop has been designed (see Fig. 6.7). The digital control loop algorithm is implemented in MATLAB. Fig. 6.7 shows the complete schematic of the proposed wideband load-insensitive IDPA. It comprises the Doherty transistor output stages, the inverted Doherty power combining network with an embedded orthogonal summation-based impedance sensor (see Chapter 2, section 3.3), and a parallel output resonator with a tunable capacitor. Rogers RO4350B with 0.508 mm thickness is chosen as the PCB substrate. The input power splitter with phase control, digitally controlled attenuators, and voltage-controllable dc-dc converters are implemented on external PCBs. This design is restricted to handle a VSWR range of ≤ 2 due to the performance of the commercially available technologies. This enables to avoid too severe performance trade-offs, such as available quality factor and power handling of the TR, as well as, the voltage/current headroom of the active devices in the output stages, facilitating the demonstration of a clear IDPA performance improvement over the targeted VSWR range.

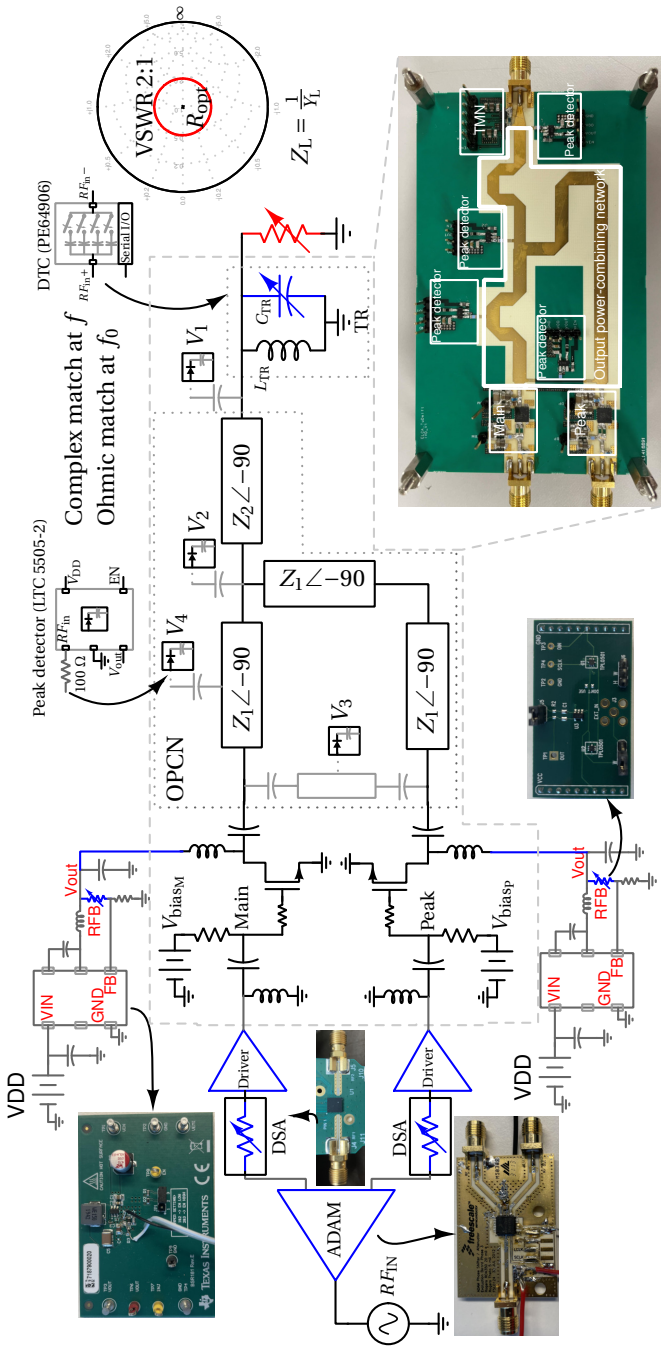


Figure 6.7. The schematic of the proposed wideband load-insensitive inverted Doherty PA. The input signal splitter is implemented using an ADAM (advanced Doherty alignment module [84]). Fine-level control of the input signal is implemented through a digital step attenuator (DSA [85]). The adjustable supplies are implemented as dc-dc buck converters [86], in which the feedback resistor that sets the supply voltage has been replaced by a digitally programmable potentiometer [87]. The voltage ratios ($|V_1/V_2|$ and $|V_3/V_4|$) are used to sense the presented load impedance to the PA. The TR/TMN cancels the complex part of the load at the fundamental.

6.3.1. INVERTED DOHERTY PA

The IDPA is designed using commercial packaged LDMOS devices (AFIC901N [88]), that are used to implement the main and peaking devices. This choice is made to respect later on the voltage/RF-power limitations of commercially available switch capacitor banks. The inputs of these devices are impedance matched to 50 Ω. The resulting Doherty configuration achieves an output power of 32 dBm from a 6.4 V supply, and has an optimum load impedance ($R_{L_{opt}}$) close to 25 Ω. An additional $\lambda/4$ transmission line transfers this impedance level to 50 Ω. The output capacitance of the devices is resonated out using the dc-feed inductor.

6.3.2. TUNABLE SHUNT RESONATOR

To cover the worst-case susceptance/reactance on the 2:1 VSWR circle. The maximum required capacitance of the parallel resonator to cover the entire operational band from 850 MHz-950 MHz in this design is 5.96 pF. Consequently, the required inductor (L_{TR}) value at 900 MHz is found to be 5.25 nH. The switched capacitor banks from pSemi were selected to implement the tunable capacitor. These switchable capacitors have quality factors ranging from 15 to 40 for the smallest and the largest values. PE64906 [65] offers a C_{min} = 0.8 pF and C_{max} = 5.4 pF at 900 MHz with a step size of 119 fF (estimated from the datasheet plots [65]), yielding an effective capacitance tuning range of 4.6 pF. The maximum voltage and RF power for these components are 30 V and 34 dBm. Two of these banks are connected in parallel to cover the entire capacitance range of 5.96 pF. Furthermore, a 0603DC high-Q inductor from coil craft was selected to implement the resonant inductor (L_{TR}).

6.3.3. INPUT SPLITTER & DIGITAL STEP ATTENUATOR

To achieve the required two independently controllable RF inputs for the main and peak stage in the proposed load-insensitive inverted Doherty PA, a wide-band advanced Doherty alignment module (ADAM) [84] is used. It contains a 90° coupler, followed by a digitally selectable phase shifter in its output (7° least significant bit (LSB) step with 49° maximum range), and step attenuators (0.5 dB LSB step with 7.5 dB maximum range). For finer amplitude control in steps of 0.25 dB, a digital step attenuator (DSA) [85] from pSemi is added directly after the ADAM module.

6.3.4. DC-DC CONVERTER

TI dc-dc buck converters (LMR54410) [86] in combination with a digitally tunable feedback resistor (TPL0501) [87] were used to control the supply voltage of the IDPA branches statically. Note that these dc-dc converters can be relatively slow since they do not need to track the envelope of the modulated RF signal, allowing high-efficiency operation. These converters are operable from 4.5 V to 36 V with a current limit of 1 A.

6.4. MEASUREMENT

This section presents the measurement results of the implemented IDPA with an embedded wideband impedance sensing network. First, the performance in standard op-

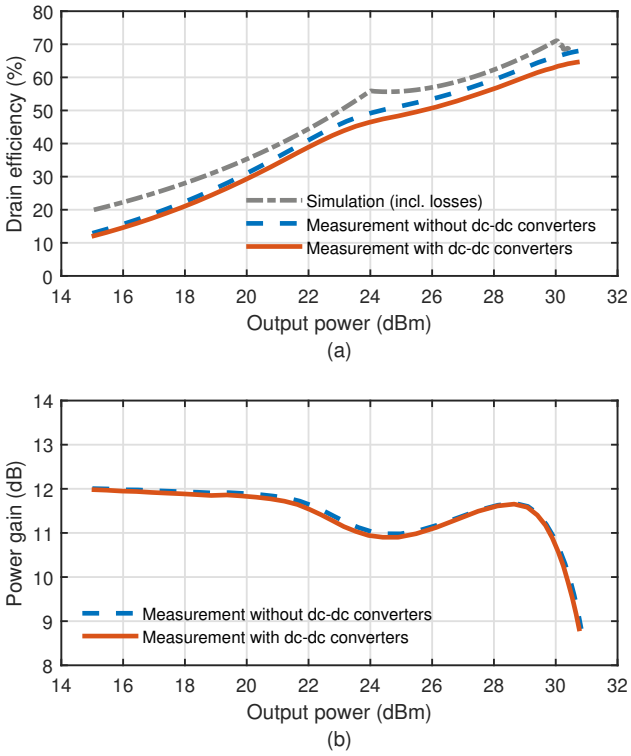


Figure 6.8. The measured inverted Doherty results at the designed center frequency of 900 MHz vs. output power (red color). (a) Drain efficiency and (b) power gain. Also, the measured and simulated (inclusive losses) efficiency performance of the IDPA without the dc-dc converter is included for reference.

eration of the IDPA is shown across its bandwidth. Second, the performance of the proposed concept, the load-insensitive wideband IDPA is demonstrated.

6.4.1. IDPA

The main stage of the IDPA is biased in the class-AB mode with a quiescent current (I_{D_M}) of 28 mA. While the peaking stage is biased in the class-C mode with a quiescent current (I_{D_P}) of 0 mA. Both stages use $V_{DD} = 6.4$ V in the $R_L = 50\,\Omega$ loading condition. The applied supply voltage is 7.7 V, and the dc-dc converters, convert these voltages to the required 6.4 V level. The voltage drop across the dc-dc converter is measured to be ≈ 0.2 V.

CENTER FREQUENCY

The performance of the IDPA at its design frequency is shown in Fig. 6.8. It can be seen that the IDPA without the dc-dc converters has a power gain of 12 dB (see Fig. 6.8(b)) and delivers a peak output power of 30.95 dBm (see Fig. 6.8(a)) with a 68.1 % drain efficiency

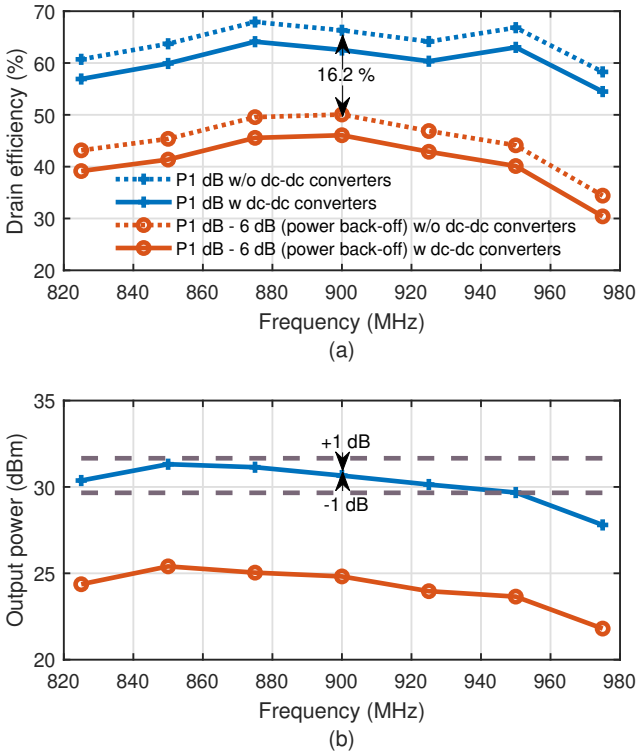


Figure 6.9. The inverted Doherty performance vs. frequency. (a) Drain efficiency with and without the dc-dc converters at 1dB output power compression and 6 dB power back off from the 1dB output power compression. (b) 1dB and 6 dB back-off output power, also shown are the ± 1 dB variation lines from 900 MHz the center frequency.

when matched to its nominal 50 Ω load. At the center frequency, the drain efficiency at the 1 dB compression and 6 dB power back-off points are 66.5 % and 50.3 %, respectively (not including the impact of the dc-dc converters). The 16.2 % efficiency degradation at 6 dB power back-off can be attributed to the output losses of the LDMOS output stage devices [89] and the shunt inductor used to resonate out their output capacitance, the losses from the embedded impedance sensor (≈ 0.075 dB), and the TR losses (≈ 0.44 dB). These losses can be represented by equivalent shunt resistances of, 150 Ω, 2870 Ω, and 468 Ω respectively at the output of the main LDMOS stage. This yields (including the impedance transformation of the OPCN) an effective parasitic shunt loading resistance of ≈ 120 Ω). The related analytical equations are given in the Appendix B. The simulated impact of these losses on the drain efficiency (see Fig. 6.8(a)), correlates well with the measured efficiency curve. However, when including the power dc-dc converters, the output power, and drain efficiency are slightly reduced to 30.9 dBm and 63.7 %, respectively. In this case, the dc-dc converters down-convert a 7.7 V supply to 6.4 V in the 50 Ω loading case. Note that all further measurement results include the power consumption

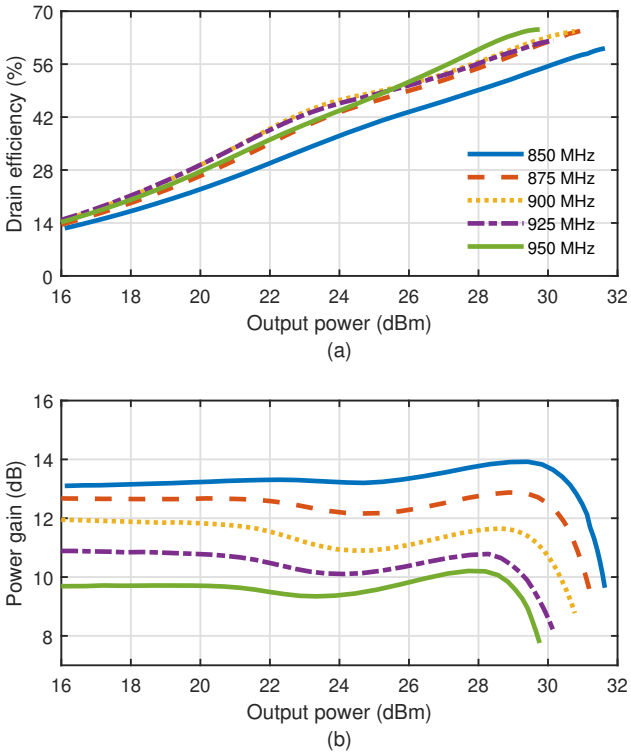


Figure 6.10. The inverted Doherty PA 1 dB power bandwidth performance vs. output power. (a) Drain efficiency and (b) power gain.

of the dc-dc converters.

WIDE-BANDWIDTH OPERATION

The IDPA performance across frequency is shown in Fig. 6.9. The measurement results show that the fabricated IDPA has a 1 dB power bandwidth of 100 MHz around a 900 MHz center frequency (see Fig. 6.9(b)). Translating to a fractional bandwidth of ≈ 11.1 %. This lower bandwidth, compared to the ≈ 22 % in section II, is caused by the inclusion of the output capacitance of the LDMOS devices and the added TR. At the 1 dB compression the drain efficiency is more than 60 % over the entire fractional bandwidth, while the 6 dB power back-off drain efficiency remains more than 40 %. The measured IDPA drain efficiency and power gain over the fractional bandwidth (i.e., 850 MHz-950 MHz) is shown in Fig. 6.10(a) and 6.10(b) respectively.

6.4.2. IDPA PERFORMANCE UNDER 2:1 VSWR

To implement the proposed technique, a look-up table (LUT) based control algorithm is implemented in MATLAB to restore the 50 Ω IDPA performance within specified ± 0.2 dB

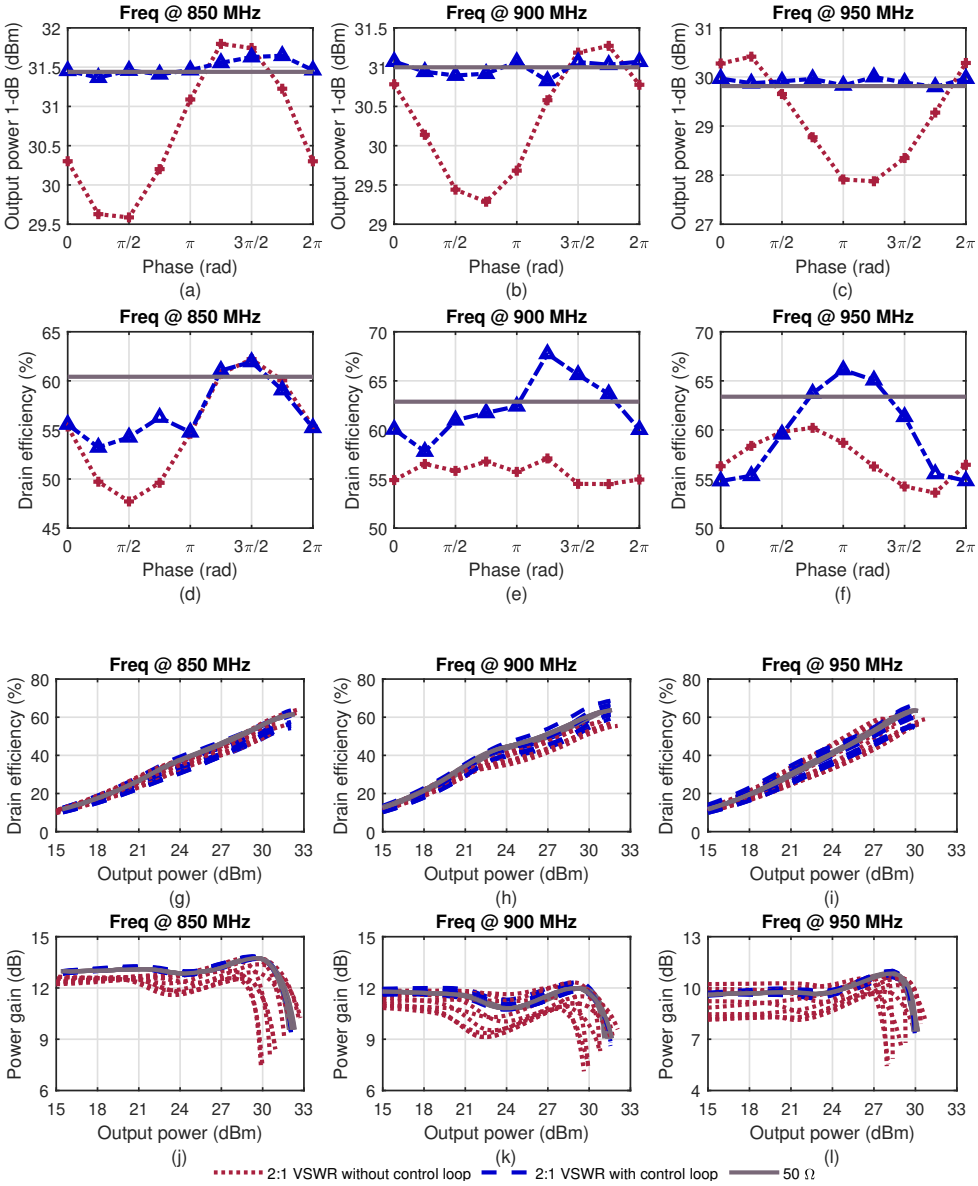


Figure 6.11. IDPA performance at the operation frequencies 850 MHz, 900 MHz, and 950 MHz as such covering the entire fractional bandwidth of the PA. At these frequencies, the IDPA is subjected to the following loading conditions. Firstly, 50 Ω; secondly, on a 2:1 VSWR circle with 45° phase steps without the control loop activated; and thirdly, with the control loop active on a 2:1 VSWR with 45° phase steps. (a), (b), and (c) IDPA output power vs. phase ($\angle\Gamma$). (d), (e), and (f) drain efficiency for a given phase ($\angle\Gamma$). (g), (h), and (i) drain efficiency vs. output power. (j), (k), and (l) power gain vs. output power.

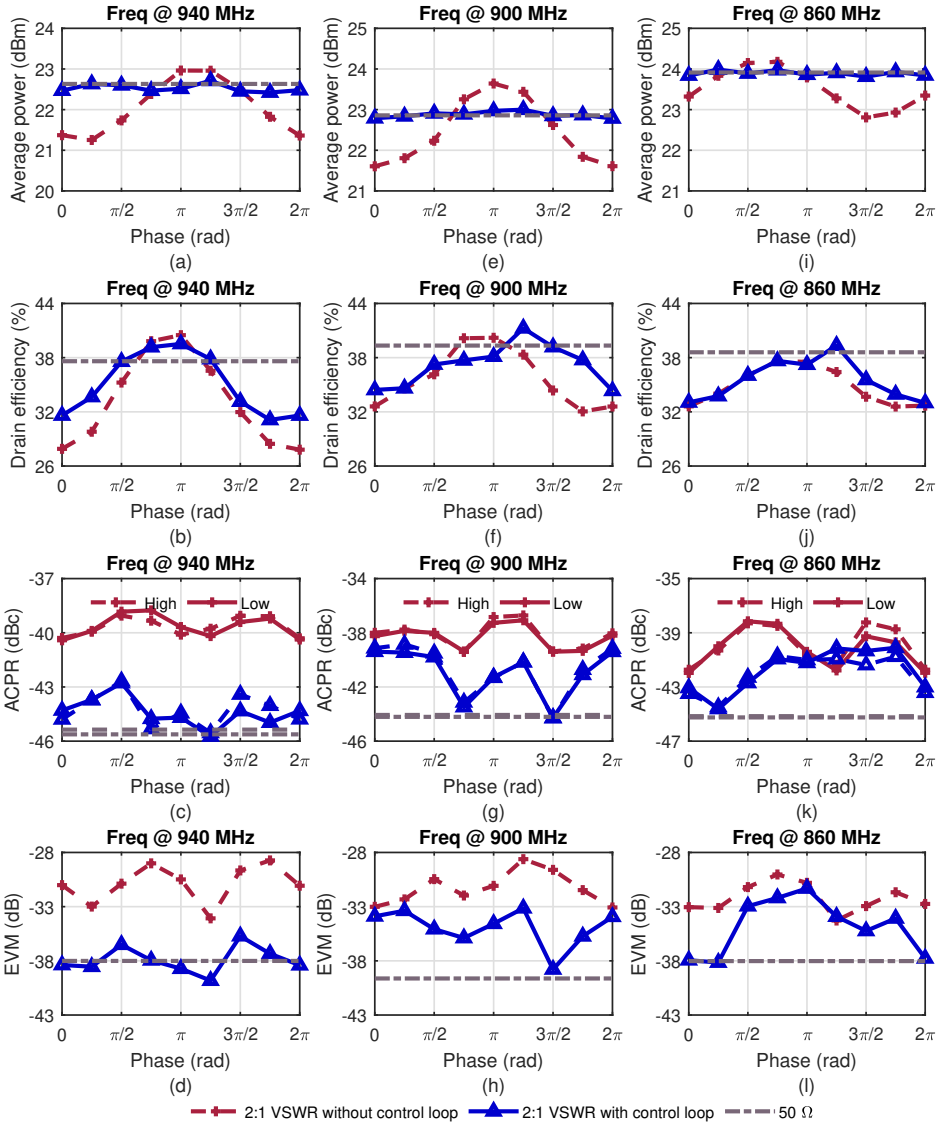


Figure 6.12. IDPA performance when driven by a modulated signal (64-QAM 2 MHz) at the operating frequencies 940 MHz, 900 MHz, and 860 MHz as such covering the entire fractional bandwidth of the PA. At these frequencies, the IDPA is subjected to the following loading conditions. Firstly, 50 Ω; secondly, on a 2:1 VSWR circle with 45° phase steps without the control loop activated and thirdly, with the control loop active on a 2:1 VSWR with 45° phase steps. (a), (e), and (i) IDPA output power. (b), (f), and (j) drain efficiency. (c), (g), and (k) ACPR. (d), (h), and (l) EVM.

tolerance in the output power. The LUT takes three (3) inputs $\{|V_1/V_2|, |V_3/V_4|, f\}$ and provides seven (7) control variables $\{V_{DD_M}, V_{DD_P}, \phi_M, \phi_P, DSA_M, DSA_P, C_{TR}\}$ as output. These control variables act on the main and peaking stages, adjusting; supply voltages $\{V_{DD_M}, V_{DD_P}\}$, relative phases, $\{\phi_M, \phi_P\}$, input amplitudes $\{DSA_M, DSA_P\}$ and capacitance value (C_{TR}) of TR to present an ohmic impedance to the main stage. The initial values of the control variables $\{V_{DD_M}, V_{DD_P}, \phi_M, \phi_P, DSA_M, DSA_P, C_{TR}\}$ were generated using the equations as formulated in section II for Fig. 6.1(b). Next, they were mapped to the input variables $\{|V_1/V_2|, |V_3/V_4|, f\}$ using the equations as formulated in Chapter 2, section 3.3 for Fig. 3.7. Finally, these values were slightly adjusted to accommodate the impact of parasitics and PCB tolerances. The objective of the control loop algorithm for single-tone operation is to maximize drain efficiency while tracking the output power and power gain profile within the set tolerance limit. Whereas, for the modulated signals, the objective of the control algorithm is to keep the average output power constant (i.e., within the tolerance bound) while improving the drain efficiency and linearity simultaneously.

SINGLE-TONE

The IDPA performance at the operating frequencies 850 MHz, 900 MHz, and 950 MHz is presented in Fig. 6.11. Covering the fractional bandwidth (≈ 11 %) of the IDPA. Furthermore, the IDPA is subjected to three loading conditions, i.e., firstly, 50 Ω, secondly, on a 2:1 VSWR circle with 45° phase steps without the control loop, and thirdly, with activated control loop on a 2:1 VSWR circle using 45° phase steps. The measurement results of these loading conditions are as follows, Fig. 6.11(a), (b), and (c) show the IDPA 1 dB compression output power vs. loading phase angle ($\angle\Gamma$) at the frequencies 850 MHz, 900 MHz, and 950 MHz, respectively. Similarly, Fig. 6.11(d), (e), and (f) show the drain efficiency. Whereas, Fig. 6.11(g), (h), and (i) show the drain efficiency vs. output power at the frequencies 850 MHz, 900 MHz, and 950 MHz respectively. Similarly, Fig. 6.11(j), (k), and (l) show the power gain vs. output power. From the above results, we can conclude that the proposed technique with the control loop meets the objective of maintaining constant output power within the tolerance band of ± 0.2 dB while tracking the power gain profile of the IDPA across frequencies. Moreover, this objective is met while improving or at least maintaining the efficiency performance of the IDPA across different loading conditions.

MODULATED SIGNAL

The measured IDPA performance when driven by modulated signals at the operating frequencies 940 MHz, 900 MHz, and, 860 MHz and for the load trajectory (45° phase steps) on the 2:1 VSWR circle, with and without the control loop activated, is shown in Fig. 6.12. Also provided is the performance of the IDPA when matched to a 50 Ω load for comparison. For these measurements, a 64-QAM 2 MHz modulated signal is used. First, a simple static AM-AM and AM-PM, LUT-based DPD was performed for the IDPA when connected to a 50 Ω load. This resulted in a set of pre-distorted drive signals for the main and peaking devices, which remain unaltered in the following VSWR measurements. At 940 MHz operational frequency, the IDPA output power, drain efficiency, adjacent channel power ratio (ACPR), and error vector magnitude (EVM) are shown in Fig. 6.12(a), (b),

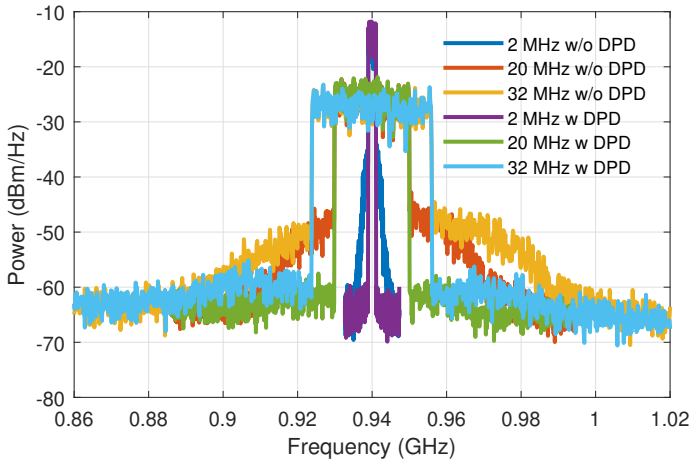


Figure 6.13. The measured power spectral density on the 50 Ω load with and without the DPD from 2 MHz-32 MHz video bandwidth with the IDPA operating at 940 MHz carrier frequency.

(c), and (d), respectively. It can be seen that the proposed method can track the 50 Ω loading performance of the IDPA on a 2:1 VSWR circle within a tolerance of ± 0.2 dB, while simultaneously improving the drain efficiency and the linearity performance. Similarly, at 900 MHz and 860 MHz with activated control loop, the nominal IDPA 50 Ω load performance can be approximated when operated on the 2:1 VSWR circle within a tolerance of ± 0.2 dB while improving the drain efficiency, and linearity performance, see Fig. 6.12(e), (f), (g), and (h), and Fig. 6.12(i), (j), (k), and (l), respectively.

The IDPA is also tested with a 50 Ω trained pre-distorted modulated 64-QAM signals having higher video bandwidths, the power spectral density with and without the DPD for 50 Ω matched load is shown in Fig. 6.13. The linearity improvement of the EVM and ACPR on the 2:1 VSWR circle in steps of 45° from 2 MHz-32 MHz video bandwidth for the IDPA operating at 940 MHz carrier frequency is also given in 6.14(a) and 6.14(b). In these experiments, the IDPA output power across bandwidth is kept constant within ± 0.2 dB of its nominal 50 Ω performance. It can be observed that the proposed technique is effective even across wide video bandwidth signals.

From the measurement results, it can be concluded that when activated, the VSWR control loop can recover the IDPA performance in terms of output power and gain with a variation of less than ± 0.2 dB across the entire fractional bandwidth of the IDPA. However, it suffers from decreased efficiency for some of the phase points. This degradation can be linked to two causes. First, the phase points where the active devices need to handle larger currents yield higher I^2R losses [68]. Second, the LDMOS device has a sizeable non-linear output capacitance; changing the supply voltage, yields a change in the output capacitance, causing reactive loads. Even though this can be adjusted in the TR, adding capacitance incurs extra losses. Moreover, for the cases where R_L is well above (>) 50 Ω, the insertion loss of the shunt resonator is higher, which also negatively

Table 6.1. Comparison with the state-of-the-art load-insensitive Doherty PAs

Comparison	**This work**						[81] EUMC-2022		[24] TMTT-2021		[22] TMTT-2020		[27] TMTT-2015	
Technique	**Supply + TR/TMN**						Supply + TMN		QB-DPA ‡		Doherty-Balanced ‡		Re-configurable-DPA	
Freq (GHz)	**0.85-0.95**						0.9		3.5		3.5		3.6	
Fractional BW	**11 % (1 dB P_{out} variation)**						NR		NR		NR		NR	
Impedance Sensor	**Wideband & embedded**						Narrowband & external		No		No		No	
CW signal	**1-tone CW**						1-tone CW		1-tone CW		1-tone CW		1-tone CW	
Freq (GHz)	**0.85**		**0.9**		**0.95**		0.9		3.5		3.5		3.6	
Z_L	**50 Ω**	**2:1**	**50 Ω**	**2:1**	**50 Ω**	**2:1**	50 Ω	2:1	50 Ω	2:1	50 Ω	2:1	50 Ω	2:1
$P_{out_{1dB}}$ (dBm)	**31.5**	**31.5 ± 0.2**	**30.9**	**30.9 ± 0.2**	**29.9**	**29.9 ± 0.2**	32.3	32.3[0.4,-0.2]	40.7	38.8-40.4	41.9‡‡	NR	27.1‡‡	NR
DE (%)	**60.5**†	**53.3-62**†	**63.5**†	**57.8-67.2**†	**63.4**†	**55-66.1**†	61	48-59	68.4	51-59	70‡‡	NR	30.9‡‡	NR
Freq (GHz)	**0.94**						0.9		3.5		3.5		3.6	
Modulated signal	**64-QAM 2 MHz**		**64-QAM 20 MHz**		**64-QAM 32 MHz**		64-QAM 4 MHz		64-QAM 20 MHz		LTE 10 MHz		16-QAM 1 MHz	
DPD (static)	Yes						Yes		No		No		No	
PAPR	**7.3**						7.3		NR		8.4		5.4	
P_{out} (dBm)	**22.7**	**22.7 ± 0.2**	**22.7**	**22.7 ± 0.2**	**22.6**	**22.6 ± 0.2**	24.4	24.4 ± 0.1	35	33-34.2	34.5	32.5-35.1	21.9	20-20.8
DE_{avg} (%)	**37.6**†	**31.6-39.5**†	**37.7**†	**31.5-39.5**†	**37.3**†	**31.1-39.2**†	41	34-39	45	32.5-42.5	42.4	22-39	18.2	NR
P_{out} variation (dB)	**NA**	**± 0.2**	**NA**	**± 0.2**	**NA**	**± 0.2**	NA	± 0.1	NA	1.2	NA	2.6	NA	0.8
ACLR (dBc)	**-45.6**	**< -42.7**	**-36.2**	**< -34.4**	**-33.6**	**< -32.1**	-46.9	< -39.3	-41.0	NR	-37.0	NR	-35.3	< -30.3
EVM (dB)	**-38.0**	**<-35.8**	**-31.9**	**<-28.8**	**-28.6**	**<-25.2**	-40.9	< -32.3	-36.6	< -27.9	-32.5	<-26.0	-28.2	< -25.0

‡ results are estimated from plots; NR = not reported; NA = not applicable; † including dc-dc converter's power consumption; ‡‡ saturated performance;

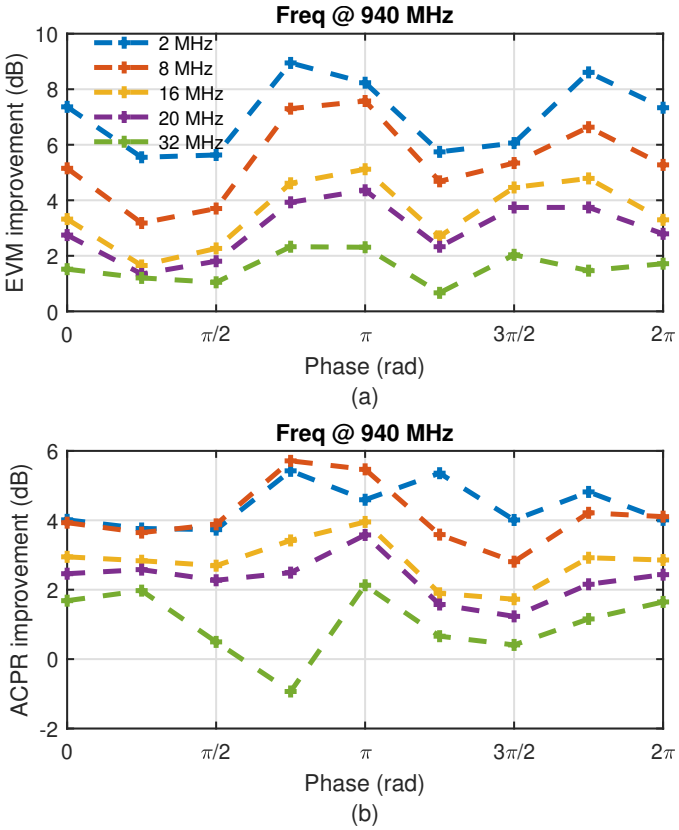


Figure 6.14. The measured linearity improvement (a) EVM and (b) ACPR on the 2:1 VSWR circle with phase steps of 45° across 2 MHz-32 MHz video bandwidth with IDPA operating at 940 MHz carrier frequency (IDPA output power across bandwidth was kept constant within ± 0.2 dB tolerance of 50 Ω nominal loading).

impacts the efficiency [68].
Table 6.1, provides a comparison with the state-of-the-art load-insensitive Doherty PAs. Switching between the Doherty-Balanced [22] configuration is capable of providing higher output power when compared to the balanced-only configuration. However, this is achieved at the expense of degraded efficiency and EVM. Reconfigurable DPAs [24, 27] are much more resilient than the balanced configuration, yet the performance degradation is much higher when compared to their 50 Ω performance. Moreover, when compared to [81], which does not include the power consumption of dc-dc converters, the proposed technique works over a wider bandwidth, and furthermore, this work presents for the first time an embedded wide-band impedance sensor, input amplitude and phase adjustment for the main and peaking stages. The proposed technique achieves the best state-of-the-art performance in terms of constant linear output power with a variation of only

± 0.2 dB, over the 2:1 VSWR circle across the fractional bandwidth of 11 %. Furthermore, with a 50 Ω trained pre-distorted 64-QAM signals, the demonstrator meets the -33 dBc ACLR for the handset [62] on the 2:1 VSWR circle for upto 20 MHz video bandwidth while delivering the 50 Ω load power and improving efficiency.

6.5. CONCLUSION

This chapter has demonstrated a wideband load-insensitive inverted Doherty PA with built-in wideband impedance sensing capability and controlling circuitry. The DPA is insensitive to load variation by tuning the input drive level and supply voltage of the main and peaking stages and adjusting its TR. As a result, it was shown, both in theory and experiments, that we can always recover the ideal Doherty operation for any load mismatch across the fractional bandwidth. The prototype DPA and LUT-based control algorithm recovered from all the load variations on a 2:1 VSWR circle. It could reduce the gain and output power variation to less than ± 0.2 dB (driven by a complex modulated signal), when compared to the 50 Ω reference case, while, improving the efficiency and linearity simultaneously. This allows the use of a simple LUT DPD, which can remain unaltered over the entire 2:1 VSWR circle. To the best of the author's knowledge, achieving all the functionalities, within a single DPA design has not been reported before (see Table 6.1), making the proposed load-insensitive IDPA with an embedded impedance sensor an interesting candidate for VSWR-tolerant mobile handset and beam steering base station applications.

7

ACTIVE LOAD CONTROL TO ENHANCE THE PA PERFORMANCE ACROSS VSWR CONDITIONS

7.1. INTRODUCTION

5G communication systems offer spatial multiplexing of their mobile users by adopting phased-array/massive multiple-input multiple-output (mMIMO) techniques [43]. Unfortunately, the (undesired) mutual antenna coupling in these systems, yields the feed impedances of the antennas to change with the beam steering angle. The power amplifier (PA)s driving the antenna elements are typically very sensitive to load changes, yielding to performance degradation in mismatch conditions [90]. Isolators are used to break the reciprocity of the PA-antenna network, as such presenting a constant impedance-matched load to the PAs. However, isolators are expensive and difficult to integrate. To avoid suboptimal PA performance under impedance mismatch, TMN [14] are proposed for low-power applications. To reduce the insertion loss of the TMN and to relax the tuning range requirements, a combination of a TMN, supply, and input drive adjustment was proposed in [68]. For higher power applications supply adjustment was used in [58]. However, these two latter techniques require the use of a dc-dc converter to adjust the PA supply voltage to the applied mismatch condition, in combination with an proper input drive adjustment.

In this work[1], a mismatch adjustment technique is proposed (see Fig. 7.1) to recover the PA performance under load mismatch by only adjusting the input drive levels of a limited number of active devices/PAs. Although higher number of active devices present more degree of freedom in terms of re-configuration. The conceptual technique in this chapter is limited to three (3) active devices. It makes use of a main PA and two auxiliary PAs, named PA_{low}, PA_{high}, and a coupler acting as power combiner (see Fig. 6.1).

[1] This chapter consists of material previously published as the author submitted version from "G. D. Singh, et al. "G. D. Singh, H. M. Nemati, M. S. Alavi, and L. C. de Vreede. "PA Output Power and Efficiency Enhancement Across the 2:1 VSWR Circle using Static Active Load Adjustment". In: IEEE Int. Microw. Symp. Dig. Tech. Papers (IMS). 2023, pp. 211–214."

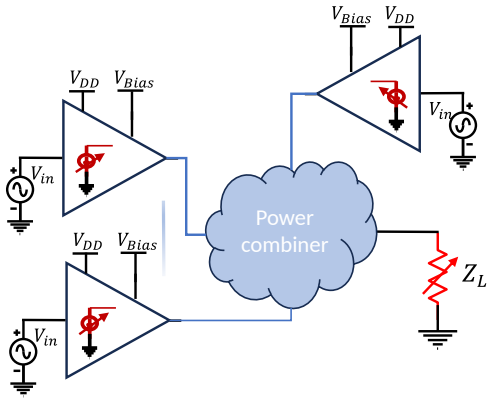


Figure 7.1. A mismatch adjustment technique consisting of multiple PA units (although only 3 are shown in this configuration) and an arbitrary power combiner network to relax the load sensitivity of the PA.

The drive levels of the main and auxiliary PAs are adjusted based on the applied loading. Three scenarios are considered,

1. R_L is 50 Ω, only the PA_{main} is activated as shown in Fig. 6.1(a)

2. R_L is between 25 Ω-50 Ω, PA_{main} and PA_{low} are both active as shown in Fig. 7.2(b). In this operation mode PA_{low} increased the loading impedance of PA_{main}. Here two operation modes are possible, namely;
   - Both PA_{main} and PA_{low} are kept out of voltage clipping.
   - Only PA_{main} is kept out of voltage clipping.

3. R_L is between 50 Ω-100 Ω PA_{main} and PA_{high} are both active as shown in Fig. 6.1(c), PA_{high} lowers the loading impedance of PA_{main}. Also here two operation modes are possible, namely;
   - Both PA_{main} and PA_{high} are kept out of voltage clipping.
   - Only PA_{main} is kept out of voltage clipping.

In the cases that both PAs are kept out of voltage clipping, the output power can be kept constant at the cost of a (small) efficiency penalty. In the case that only the PA_{main} is kept out of voltage clipping, the efficiency penalty is even less while the output power only marginally fluctuates.
The outline of this chapter is as follows. In section 6.2a, the static load adjustment technique to recover the PA performance is introduced and the equations for the idealized case are derived and verified in simulation. In section 6.3 a measurement-based proof of concept is given using a commercially available coupler and gallium nitride (GaN)-based evaluation boards. The paper is concluded in section 6.4.

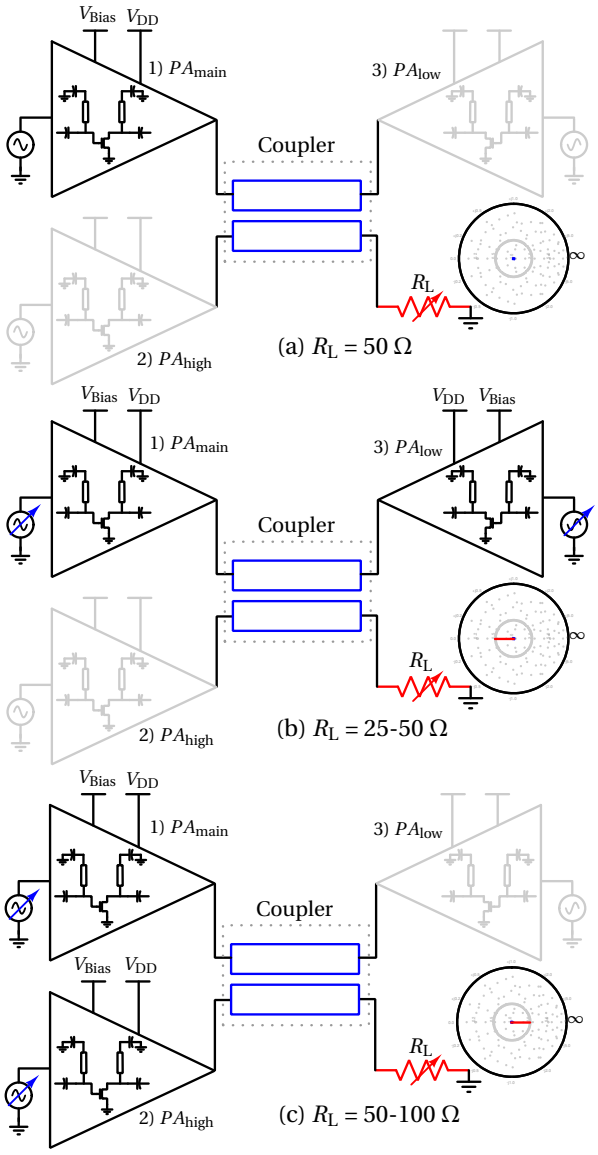
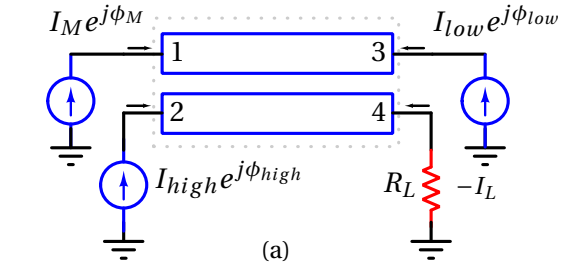


Figure 7.2. The proposed concept of using active auxiliary devices for static load adjustment. (a) case 1: PA_{main} is active only to drive the matched load, (b) case 2: for a load mismatch between 25 Ω-50 Ω PA_{main} and PA_{low} are active with adjusted input drive levels and (c) case 3, for a load mismatch between 50 Ω-100 Ω PA_{main} and PA_{high} are both active with customized drive level.

7.2. THEORY



(a)

$$\begin{bmatrix} V_M \\ V_{high} \\ V_{low} \\ V_L \end{bmatrix} = \frac{Z_0}{\sqrt{1-C^2}} \begin{bmatrix} 0 & 0 & -j & -jC \\ 0 & 0 & -jC & -j \\ -j & -jC & 0 & 0 \\ -jC & -j & 0 & 0 \end{bmatrix} \begin{bmatrix} I_M e^{j\phi_M} \\ I_{high} e^{j\phi_{high}} \\ I_{low} e^{j\phi_{low}} \\ -I_L \end{bmatrix}$$

(b)

Figure 7.3. The proposed circuit (a) coupler with current sources representing the PAs and the connected variable load. (b) Z-matrix of the coupler used in the analysis.

We will assume the use of a coupled line coupler as power combiner with the three PA sources connected for analyzing the proposed concept as in Fig. 7.3(a).

$$\begin{bmatrix} V_M \\ V_{high} \\ V_{low} \\ V_L \end{bmatrix} = \frac{Z_0}{\sqrt{1-C^2}} \begin{bmatrix} 0 & 0 & -j & -jC \\ 0 & 0 & -jC & -j \\ -j & -jC & 0 & 0 \\ -jC & -j & 0 & 0 \end{bmatrix} \begin{bmatrix} I_M e^{j\phi_M} \\ I_{high} e^{j\phi_{high}} \\ I_{low} e^{j\phi_{low}} \\ -I_L \end{bmatrix} \tag{7.1}$$

The Z-matrix [91, 92] (7.1), where C is the coupling coefficient. The currents supplied by the PA_{main} and the two auxiliary PAs are represented by current sources and are I_{M}, I_{low}, and I_{high} respectively. We can write the following equations for the voltages from the Z-matrix in terms of I_{M}, I_{low}, and I_{high}, while making use of the relation $V_{\text{L}} = -I_{\text{L}} R_{\text{L}}$.

$$V_M = \frac{Z_0}{\sqrt{1-C^2}} \left(-j I_{low} e^{j\phi_{low}} - \frac{C^2 Z_0}{R_l \sqrt{1-C^2}} I_M e^{j\phi_M} - \frac{C Z_0}{R_l \sqrt{1-C^2}} I_{high} e^{j\phi_{high}}\right) \tag{7.2}$$

$$V_{high} = \frac{Z_0}{\sqrt{1-C^2}} \left(-jC I_{low} e^{j\phi_{low}} - \frac{C Z_0}{R_l \sqrt{1-C^2}} I_M e^{j\phi_M} - \frac{Z_0}{R_l \sqrt{1-C^2}} I_{high} e^{j\phi_{high}}\right) \tag{7.3}$$

$$V_{low} = \frac{Z_0}{\sqrt{1-C^2}} \left(-j I_M e^{j\phi_M} - jC I_{high} e^{j\phi_{high}}\right) \tag{7.4}$$

$$V_L = \frac{Z_0}{\sqrt{1-C^2}} \left(-jC I_M e^{j\phi_M} - j I_{high} e^{j\phi_{high}}\right) \tag{7.5}$$

From (7.2), (7.3), (7.4), and (7.5) we can observe that to add the currents constructively, the terms with ϕ_{M} and ϕ_{high} need to be in phase with that of ϕ_{low}, we set them as $\phi_{\mathrm{M}} = \phi_{\mathrm{high}} = 90°$ and $\phi_{\mathrm{low}} = 0°$. The delivered power ($P_{\mathrm{out}} = {V_{\mathrm{L}}}^2/2R_{\mathrm{L}}$) to the load is given by,

$$P_{out} = \frac{Z_0^2}{2R_L(1-C^2)}(CI_M + I_{high})^2 \tag{7.6}$$

Furthermore, the resulting impedances offered to the PAs are,

$$Z_M = \frac{C^2}{1-C^2}\frac{Z_0^2}{R_L} + \frac{C}{1-C^2}\frac{Z_0^2}{R_L}\frac{I_{high}}{I_M} - \frac{Z_0}{\sqrt{1-C^2}}\frac{I_{low}}{I_M} \tag{7.7}$$

$$Z_{high} = \frac{1}{1-C^2}\frac{Z_0^2}{R_L} + \frac{C}{1-C^2}\frac{Z_0^2}{R_L}\frac{I_M}{I_{high}} - \frac{C}{\sqrt{1-C^2}}Z_0\frac{I_{low}}{I_{high}} \tag{7.8}$$

$$Z_{low} = \frac{Z_0}{\sqrt{1-C^2}}\left(\frac{I_M}{I_{low}} + C\frac{I_{high}}{I_{low}}\right) \tag{7.9}$$

With these voltages and impedance's, we can obtain the optimum drive profiles versus the loading R_{L}, for $Z_0 = 50\,\Omega$ and C = $1/2^{0.5}$,

7.2.1. OHMIC LOAD

CASE 1, $R_{\mathrm{L}} = 50\,\Omega$

In this case $\mathrm{PA_{main}}$ is active (see Fig. 6.1(a)), while, I_{low}, and I_{high} are both zero. Consequently, the impedance seen by the main stage and the power delivered using (7.7) and (7.6) are,

$$Z_{\mathrm{M}} = 50\,\Omega\ (a);\ \ P_{\mathrm{out}} = \frac{1}{2}I_{\mathrm{M}}^2 R_{\mathrm{L}} = \frac{V_{\mathrm{DD}}^2}{2R_{\mathrm{L}}}\ (b) \tag{7.10}$$

As a result of this matched condition, PA_{main} can achieve maximum output power and efficiency simultaneously.

CASE 2, R_{L} IS BETWEEN 25 Ω-50 Ω

In this case PA_{main} and PA_{low} are both active (see Fig. 6.1(b)), while, I_{high} is zero. Since, the maximum P_{out} needs to be equal to that of the 50 Ω case, substitution of R_{L} in (7.6) yields the new value of I_{M}. Furthermore, since V_{M} should not clip after substitution of R_{L} in (7.2), I_{M} and I_{low} are found as,

$$I_{\mathrm{M}} = \sqrt{\frac{P_{\mathrm{out}}2R_{\mathrm{L}}}{Z_0^2}}\ (a),\ \ I_{\mathrm{low}} = \frac{I_{\mathrm{M}}}{\sqrt{2}}\left(\frac{Z_0}{R_{\mathrm{L}}} - \frac{V_{\mathrm{DD}}}{\sqrt{2P_{\mathrm{out}}R_{\mathrm{L}}}}\right)\ (b) \tag{7.11}$$

However, since the voltage V_{low} depends on I_{M} its voltage swing is given as,

$$V_{\mathrm{low}} = \sqrt{2}Z_0 I_{\mathrm{M}} = \sqrt{2}Z_0\frac{V_{\mathrm{DD}}}{R_L} \tag{7.12}$$

Using these conditions the output power can be kept constant for variation of R_{L} in the interval of 25 Ω-50 Ω.

CASE 3, R_L IS BETWEEN 50 Ω-100 Ω

In this case both PA_{main} and PA_{high} are active, while PA_{low} is inactive (see Fig. 6.1(c)). Since, P_{out} needs to be constant, substitution of R_L in (7.6) yields the value of I_{high} while keeping I_M equal to the previously discussed 50 Ω loading condition. Furthermore, since V_{high} should not clip after substitution of R_L in (7.3), I_{high} and V_{high} are found as,

$$I_{high} = \frac{I_M}{\sqrt{2}}\left(\sqrt{\frac{R_L}{Z_0}} - 1\right) \ (a), \quad V_{high} = Z_0\sqrt{\frac{2Z_0}{R_L}}I_M = Z_0\sqrt{\frac{2Z_0}{R_L}}\frac{V_{DD}}{R_L} \ (b) \tag{7.13}$$

From (7.10), (7.12) and (7.13), it can be observed that the maximum voltage swing across PA_{high} and PA_{low} is $\sqrt{2}$ higher than the nominal PA_{main}. Therefore, the supply voltages for $VDD_{high} = VDD_{low} = \sqrt{2}\,VDD_{main}$.

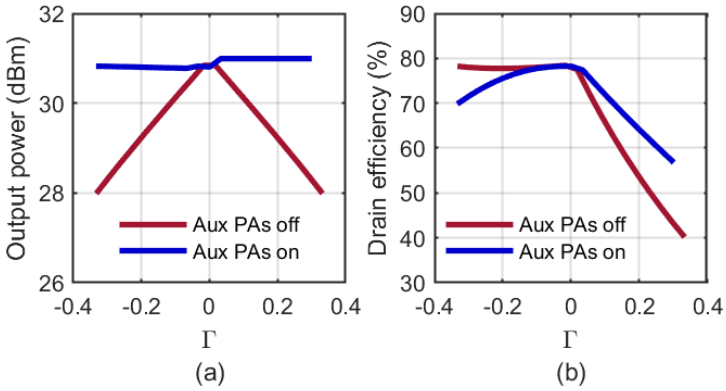


Figure 7.4. Simulated (a) output power and (b) drain efficiency of the proposed concept across the Γ range from [-0.333 0.333] with and without the auxiliary PAs activated.

7.2.2. SIMULATION RESULTS

The proposed concept is verified in simulation using an ideal 3 dB coupler and ideal class-B operation with all harmonics short-circuited for the main and auxiliary PAs. Using the previously derived drive conditions for PAs for the various loading conditions. Fig. 7.4(a) and 7.4(b) show the simulated output power and drain efficiency for a Γ sweep over the real axis of the Smith chart from [-0.333 0.333]. When avoiding voltage clipping for both the main PA and auxiliary PAs, as such ensuring perfectly linear operation, e.g., by using two constant supply voltages (V_{DD} = 11 V (7.10) and $V_{DD_{high}} = V_{DD_{low}}$ = 15.56 V (7.13, 7.12)) the RF output power can be kept perfectly constant at the cost of a (small) penalty in efficiency.

Moreover, for the in-between loading conditions in the range 25 −50 Ω [-0.333 0.0], and the range of 50 −100 Ω [0.0, 0.333], the proposed technique yields significant improvements in both the output power and efficiency. Note that, using a matching network or an asymmetric coupler in connection to the auxiliary PAs. The proposed concept can

also work with a single supply.
When considering complex varying loads, ideally a compensating low loss susceptance is placed in parallel to the presented load (see Fig. 6.1) [68]. However, since these are not yet (commercially) available for larger power levels, an alternative approach is to use a somewhat higher static supply voltage for the auxiliary PAs compared to PA_{main} to accommodate the extra voltage swing, needed to handle reactive part of the loading without any voltage clipping. This is discussed in the following section briefly.

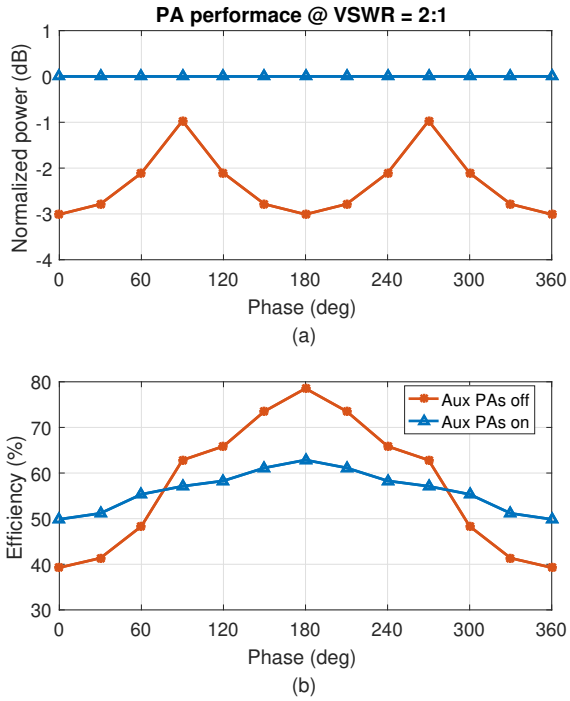


Figure 7.5. Analytical (a) output power and (b) drain efficiency of the proposed concept across the 0°-360° phase variation on a 2:1 VSWR circle with and without the auxiliary PAs activated.

7.2.3. COMPLEX LOAD

For complex load, the power delivered to the load is given by $P_{\text{out}} = 0.5 {I_{\text{L}}}^2 \text{Re}(Z_{\text{L}})$ is given by,

$$P_{\text{out}} = \frac{Z_0^2}{2|Z_{\text{L}}|^2(1-C^2)}(CI_{\text{M}} + I_{\text{high}})^2 Re[Z_{\text{L}}] \tag{7.14}$$

and the dc-power consumption is given by,

$$P_{\text{dc}} = \frac{2}{\pi}(I_{\text{M}} V_{\text{DD}_{\text{M}}} + I_{\text{low}} V_{\text{DD}_{\text{low}}} + I_{\text{high}} V_{\text{DD}_{\text{high}}}) \tag{7.15}$$

From (7.14) and (7.15) the efficiency can be computed.

$$\eta_{\text{DE}}(\%) = \frac{P_{\text{out}}}{P_{\text{dc}}} 100 \tag{7.16}$$

By following the activation procedure for $|Z_{\text{L}}|$ described in section (7.2.1) using output power (7.16) and efficiency (7.14) equations. The required current $\{I_{\text{M}}, I_{\text{high}}, I_{\text{low}}\}$and voltage $\{V_{\text{DD}_{\text{M}}}, V_{\text{DD}_{\text{high}}}, V_{\text{DD}_{\text{low}}}\}$ can be obtained. Across the 0°-360° VSWR phase the maximum of each voltage $\{V_{\text{DD}_{\text{M}}}, V_{\text{DD}_{\text{high}}}, V_{\text{DD}_{\text{low}}}\}$ is used to accommodate for the higher voltage swing resulting from the complex loading. The analytical output power and efficiency is plotted is Fig. 7.5 (a) and (b) respectively. For fair comparison, the performance without auxiliary PAs enabled is shown. It can be observed that the proposed PA performance enhancement technique can maintain constant output power across the entire 2:1 VSWR circle while significantly improving the efficiency. However, the PA when is subjected to 50 Ω load, the higher supply voltages on the main stage will incur a small efficiency penalty of 8 %. In communication systems that can tolerate some output power ripples across VSWR circle. The slightly lower power supplies can be used to enhance the efficiency.

7.3. PA CONCEPT AND MEASUREMENT

7.3.1. PROTOTYPE PA CONCEPT

The measurement setup of Fig. 7.7(a) was assembled to validate the proposed concept. Three Cree's CGH40006P evaluation boards, housing the 28 V 6 W GaN high electron mobility transistor (HEMT) devices, are used for the main and the two auxiliary PAs. These boards are broadband matched from 0.8 −6.0 GHz. The broadband coupler (0.5 −3.0 GHz) used in these experiments is from Innovative power products (IPP-2160). A Keysight M8190A 4-Channel arbitrary waveform generator (AWG) generates the control signals with excellent phase coherence. These input signals are amplified using instrumentation amplifiers in the feeds that connect to the PAs. A Maury load tuner provides the varying load impedance (Z_{L}). A power meter monitors the RF output power delivered to the load.

7.3.2. MEASUREMENT RESULTS

For the VSWR circle measurement, the PA_{main} operates with a 17 V supply, while the auxiliary PAs use 21 V supplies. When an auxiliary PA is supposed to be inactive, its gate voltage is set to −4.1 V to switch it off, as such zeroing its power consumption. While active, the auxiliary PAs operate at ≈ 65 mA quiescent drain current. The measured overall PA configuration performances, in terms of output power and drain efficiency at 2 GHz, are shown in Fig. 7.7(b), 7.7(c) and 7.8, respectively. Moreover, the drain efficiency of the

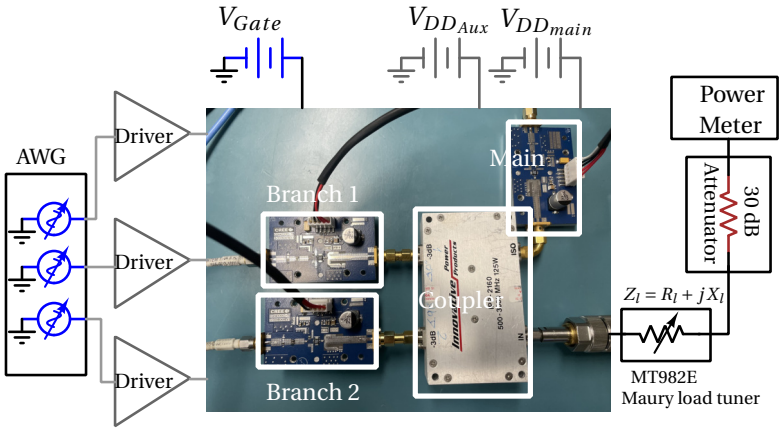


Figure 7.6. (a) Test setup used to evaluate the proposed PA load adjustment concept using a commercially available coupler and evaluation boards. Measured (b) output power and (c) drain efficiency of the proposed concept across the whole 2:1 VSWR circle in phase steps of 45° with and without the auxiliary PAs activated. Also shown is the standalone PA performance for the same loading conditions.

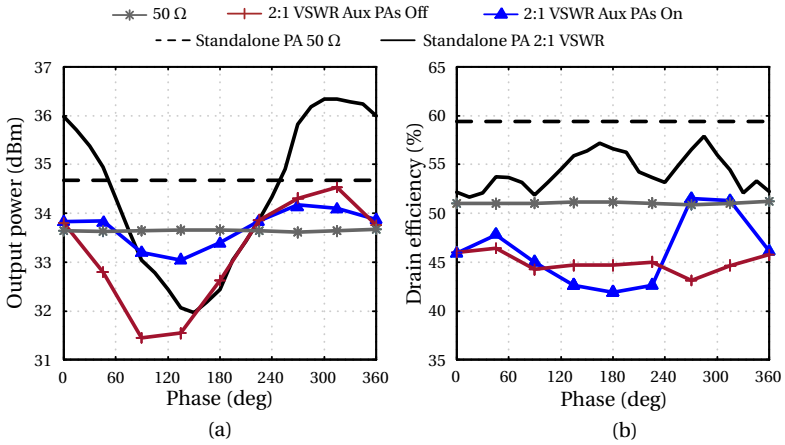


Figure 7.7. (a) Test setup used to evaluate the proposed PA load adjustment concept using a commercially available coupler and evaluation boards. Measured (b) output power and (c) drain efficiency of the proposed concept across the whole 2:1 VSWR circle in phase steps of 45° with and without the auxiliary PAs activated. Also shown is the standalone PA performance for the same loading conditions.

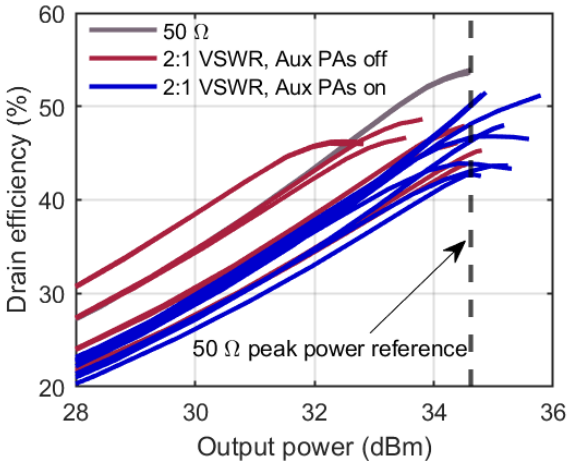


Figure 7.8. Measured drain efficiency vs. output power of the proposed concept across the whole 2:1 VSWR circle in phase steps of 45° with and without the auxiliary PAs activated.

overall PA configuration is calculated as follows.

$$\eta_D = \frac{P_{\text{out}}}{P_{\text{DC}_\text{M}} + P_{\text{DC}_\text{low}} + P_{\text{DC}_\text{high}}} 100\ \% \tag{7.17}$$

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CASE 1: $Z_\text{L} = 50\,\Omega$

Using a 17 V supply, the PA_main delivers for the matched condition an output power of 33.7 dBm at an efficiency of 51 %. When operated standalone (without coupler etc.), the PA_main efficiency is 59.5 % at an output power level of 34.8 dBm. The reduction in output efficiency and output power is due to the coupler losses (≈ 0.7 dB) and the losses in the outputs of the auxiliary PAs when they are switched off (their gate voltages set to −4.1 V). Yielding a total loss of 1.3 dB. The loss can be reduced by co-designing the PAs with the coupler in future work.

CASE 2: Z_L ON THE 2:1 VSWR

When the proposed PA configuration is exposed to a 2:1 VSWR loading condition with 45° phase steps of Γ_L when the auxiliary PAs are not activated, the PA output power varies more than 3 dB (see Fig. 7.7(b)). Also, the efficiency is degraded (see Fig. 7.7(c)). Using an intelligent activation scheme for the drive levels of the main and auxiliary PAs, the PA output power can be significantly enhanced (see Fig. 7.8 and 7.7(b)), yielding a variation of only 0.6 dB worst case (see Fig. 7.7(b)). Also, while improving the output power, the overall efficiency of the PA configuration has been enhanced (Fig. 7.7(c)) at some of the $\angle\Gamma_\text{L}$ points. Furthermore, the reduced efficiency is linked to the extra bias current required by the auxiliary PAs when active and the complex loading across both the main and auxiliary PAs. However, the worst-case efficiency degradation due to the varying

load is only 8.5 % with reference to the 50 Ω loading. In a more advanced implementation, an impedance sensor [68] in combination with a variable gain pre-driver stage can be used to control the main and auxiliary PAs input drive dynamically. Note that in case of fast-changing VSWR conditions, smooth transitions (soft turning on and off the Aux. PAs) must be applied to avoid discontinuities when making the transitions in activation of the various PAs.

7.4. CONCLUSION

In this chapter an active load adjustment technique to recover the power amplifier (PA) performance due to load mismatch was proposed. Using a combination of the coupler, main PA, and auxiliary PAs and an intelligent driving scheme, the PAs output power and efficiency can be simultaneously enhanced under varying loading conditions. Since the proposed technique only relies on adjustments of the input signals, it is suitable for applications with very fast-changing loading conditions. The effectiveness of the proposed technique was demonstrated for both ohmic and complex loads.

8

Conclusion & Future Work

This dissertation provides an analysis of power amplifier (PA) load sensitivity and reviews existing solutions in the literature. The PA topologies selected—class-B and Doherty PA (DPA)—represent some of the most widely used in RF communication applications. Of these, the study reveals that the DPA is particularly sensitive to load variations due to the impedance inverter that combines power from the main and peaking devices. When exposed to a 2:1 VSWR load mismatch, a condition often encountered in phased arrays, both Class-B and Doherty PAs experience significant performance degradation, with output power losses of up to 50 %. This degree of loss imposes considerable constraints on the communication link budget and thermal management in phased-array transmitters.

Additionally, due to device non-linearity, the linearity of these PA configurations becomes load-dependent. While digital pre-distortion (DPD) is typically employed to mitigate this non-linearity, using an active DPD loop with an observation receiver for each PA in large arrays is impractical, as it would greatly increase power consumption.

To alleviate the load sensitivity of PA's, the most promising approach is to leverage redundancy. In view of this we can operate the PA's in two realms. In case 1, we are operating the PA in a non-reciprocal regime, in this case, the PA does not see the reflection coming in from the load mismatch. In case 2, the PA operates in the reciprocal regime, the reflections are seen by the PA, causing a VSWR condition.

The solutions proposed in this dissertation pertain to case-2, which involves the reciprocal regime. To enhance the VSWR tolerance of power amplifier (PA) topologies under these conditions, reconfigurable voltages and currents are utilized in the output stages of the PA. By employing both voltage and current control, the output power and efficiency can be accurately restored under any mismatch conditions. The adjustment of the output stages in response to fluctuating VSWR is managed through an impedance sensor.

In conclusion this dissertation presents two primary contributions. First, it proposes two passive impedance sensing methods—standalone and embedded—for self-healing power amplifiers. Second, it demonstrates load-insensitive class-B and Doherty PA's that use redundancy in their voltage and current modes within the output stages. The varying complex load is preferably first compensated for its undesirable susceptance, followed by an adjustment of the transistor output stage to accommodate variations in the ohmic load. This adjustment is achieved by modifying the supply voltage and drive level of the

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output stage. This two-step process circumvents the high-Q conditions typically associated with tunable matching network solutions that aim to correct both real and imaginary load deviations by adjusting element values.

To facilitate wide-band load-insensitive Doherty PAs, an additional degree of freedom is introduced through combining a low-Q, complex-to-ohmic tunable matching network with tunable phase shifters. Finally, it is demonstrated that PAs with distributed current mode redundancies can be made VSWR tolerant, by relying solely on the active devices of three PA stages to recover from load mismatches. The primary objective of this approach is to create a load-insensitive PA capable of handling higher output powers and rapidly changing load conditions.

8.1. THESIS OUTCOME

IMPEDANCE SENSORS

Chapter 3, discusses a vital block for load insensitive PAs i.e., an impedance sensor, which provides information about the complex impedance seen by the PA when subjected to load mismatch. By knowing the presented complex load impedance it is possible to control the load correction techniques that are discussed in the subsequent chapters. Both active and passive impedance sensors are discussed by listing the advantages of each concept. Two novel passive impedance sensing methods are proposed namely, a two-tap six-port network based impedance sensor and embedded impedance sensor in the IDPAs output matching network. Furthermore, their analysis and measurement results are provided.

LOAD-INSENSITIVE CLASS-B PA

Chapter 4, proposes a low-loss correction for a self-healing class-B load-insensitive power amplifier. Wherein the varying (complex) load is first compensated for its unwanted susceptance part, followed by adjustment of the transistor output stage to the ohmic load variation, by modifying its supply voltage and drive level. This two-step approach avoids the high-Q conditions that typically occur in tunable matching network solutions, which aim to correct for both the real and imaginary load deviation, as such providing lower insertion loss and voltage stress. Next, to facilitate a fully automated load mismatch correction without the need for pre-calibration, a modified two-tap six-port network for impedance detection (discussed in chapter 2) and a control loop approach is proposed. As proof of principle, a prototype 900-MHz class-AB power amplifier featuring the proposed correction technique, as well as, the six-port reflectometer and the control loop have been implemented as a PCB demonstrator. Measurement results show that the self-healing load-insensitive PA in the events of load mismatch significantly improves the performance and approaches the 50 Ω performance.

LOAD-INSENSITIVE DOHERTY PA

In Chapter 5, a low-loss load-insensitive DPA was introduced. This DPA is in-sensitive to ohmic load variation by adjusting its supply voltage and input drive of both the main and peaking stages in a mirrored approach. Moreover, a low-loss TMN is employed to

cancel out any reactive part of the load. Using the proposed concept, it can be shown that the ideal Doherty operation can always be recovered for any load mismatch within the range of 2:1 VSWR (this VSWR range is only limited by practical device constraints). To validate this technique a printed circuit board (PCB) based demonstrator consisting of the DPA, a six-port reflectometer, and a tunable shunt resonator have been fabricated. When the DPA is driven with a pre-distorted 64-QAM 4-MHz signal trained for the 50 Ω loading condition. The DPA delivers an output power of 24.4 ± 0.1 dBm with a 34-42 % drain efficiency, across both 50 Ω and 2:1 VSWR loading range. This output power and efficiency is achieved with linearity performance i.e., EVM/ACLR better than -32.3 dB/-39.3 dBc for all the loading conditions.

WIDEBAND LOAD-INSENSITIVE DOHERTY PA

Chapter 6, presents an inverted Doherty power amplifier (IDPA) made load-in-sensitive up to 2:1 VSWR across its fractional (11 %) bandwidth with a wideband impedance sensor directly embedded directly in its output power combining network. To correct for load variation, a low-loss tunable resonator (TR) is used to ensure ohmic loads to the main and peaking stages at the center frequency of operation. At off-center frequencies, the TR is used to present an ohmic load for the main stage, while, a digitally adjustable phase shifter is used to (re)align the main and peaking stage's current summation in the output power combining network. For ohmic load deviations, the main and peaking stage supply voltages and input drives are adjusted to maintain the ideal Doherty's output power and efficiency profile related to nominal 50 Ω loading across the bandwidth. To implement the control of the formerly mentioned technique, a wideband impedance sensor is proposed, that uses the orthogonality of incident and reflected waves and requires only four peak detectors. As proof of principle, a prototype 850-950 MHz IDPA featuring the proposed correction technique, the impedance sensor, and the control loop, has been implemented as a PCB demonstrator. Measurement results show that the IDPA can maintain constant output power with a tolerance of only ± 0.2 dB while improving the drain efficiency and linearity across the entire fractional bandwidth (11 %) for a VSWR range of 2:1.

ACTIVE LOAD CONTROL TO ENHANCE THE PA PERFORMANCE ACROSS VSWR CONDITIONS

In Chapter 7, an innovative PA correction technique that relies on only active devices to recover from load mismatch is introduced. The primary motivation for this technique is to demonstrate load-insensitive PA for very high output power without the need for any high voltage tunable devices. It utilizes a main PA, two auxiliary PAs, and a coupler. By adjusting the input drive levels of the PAs it can recover the output power and to a great extent the efficiency of the main PA even when exposed to 2:1 VSWR mismatch conditions. When connected to 50 Ω loading, only the main PA is active, for impedance below or above 50 Ω, besides the main amplifier, one of the auxiliary PAs is also activated. The power generated by the auxiliary PA adds in phase to the output power of the main PA, as such allowing the output power to be constant at the expense of a minor efficiency penalty.

8.2. SUGGESTIONS FOR FUTURE DEVELOPMENT

The load insensitive PA concepts demonstrated in this thesis are all based on adding hardware redundancy to the PA and can act as a foundation for future developments to obtain new opportunities to enhance transmitter performance. Some possibilities for future research are listed below. Whether these possibilities are worth investigating is in the hands of the reader.

- In chapter 4, tunable matching networks were used to match the complex load to ohmic condition using a SOI based switchable capacitor. However, these are limited in power handling capacity. It needs to be investigated if a GaN based tunable capacitor can offer a comparable or even better figure of merit ($R_{\text{on}}C_{\text{off}}$), at higher power levels.

- In chapter 3, the six-port network in combination with a control loop offers calibration free, VSWR-resilient PA performance. However, the sensing network works only over a limited bandwidth. Passive-networks that offer a similar functionality over a wider-bandwidth are needed to enable wide-band VSWR-resilient performance enhancement.

- In chapter 5, it was demonstrated that adapting the supply voltage and current, the output power and efficiency performance of Doherty PA can be recovered for a changing load. However the linearity degradation of the involved active devices due to the changing ohmic load impedances limits the achievable performance in EVM and ACLR. Adopting an analog AM-PM cancellation technique that can accommodate for the changing load will improve both the EVM and ACLR of the proposed technique.

- In chapter 6, the measurement involves sweeping all the seven (7) $\{V_{\text{DD}_\text{M}}, V_{\text{DD}_\text{P}}, \phi_\text{M}, \phi_\text{P}, DSA_\text{M}, DSA_\text{P}, C_\text{TR}\}$ control variables to account for the impact of circuit imperfections. To shorten the measurement time more intelligent algorithms are needed.

- In chapter 7, a load mismatch adjustment technique based-on a power combiner and three independently controlled active devices was introduced. It is worth investigating if a higher number of active devices can offer more efficiency enhancement compared to the proposed configuration with 3 devices. Moreover, a figure of merit can be developed for the number of active device, and their related reduction in power utilization, needed to handle a given 0°-360° VSWR circle.

A

APPENDIX

A.1. DISTORTION ANALYSIS

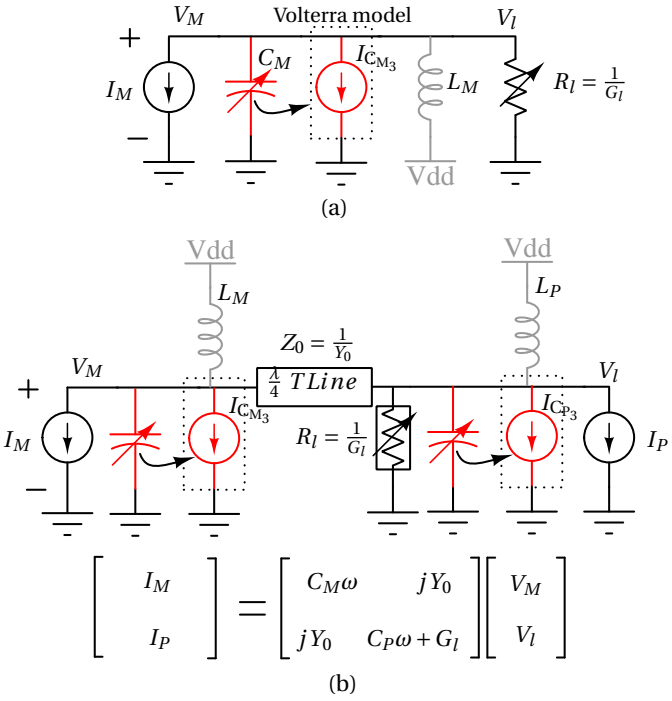

Figure A.1. Simplified circuit models for the calculation of the output phase ($\angle V_l$): (a) single-stage class-B amplifier, (b) Doherty amplifier with the Volterra admittance matrix.

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A.1.1. DISTORTION ANALYSIS SINGLE-STAGE CLASS-B AMPLIFIER

The VSWR correction used in this work for a DPA configuration is an extension of the technique proposed in [68] for a single-stage class-B line-up. It uses a two-step method. First, any susceptance at the active device output is canceled by a resonator with an adjustable capacitor (e.g., switch bank with capacitors). Next, the desired output power level is restored by adjusting the class-B stage supply voltage and drive level. For a practical output stage device (e.g., LDMOS or GaN), C_{ds} is a non-linear function of the drain-source voltage and, to a lesser extent its drain current. In this work, we assume only voltage dependence for C_{ds}. To raise an understanding of the AM-PM distortion of the DPA, we will first consider the AM-PM distortion of a single class-AB stage using the proposed technique in [68]. For this purpose, the output stage capacitance (C_{ds}) has been measured as a function of the applied voltage (V_{ds}) using a dedicated test board (see Fig. A.2(a)). The measured C_{ds} as a function of V_{ds} is given in Fig. A.2c and in a first-order approximation be modeled as,

$$C_{ds} = \frac{C_{ds0}}{(1+\frac{V_{ds}}{\phi_B})^m} \tag{A.1}$$

where, C_{ds0} = 20.3 pF, ϕ_B = 2.14 , and m = 0.454

From Fig. A.2d, it is evident that with increasing output power, the effective output capacitance C_{ds} (average value of $C_{ds}(V_{ds}(t))$ along the load-line increases (see Fig.A.2b)). Since a static output matching network can only compensate for a single C_{ds} value, AM-PM variation occurs due to the changing C_{ds} with output power (among other secondary causes). Assuming that the C_{ds} change dominates, the AM-PM behavior for a single output stage can be analyzed by applying the Volterra series method [93] to the simplified class-B circuit in Fig. A.1a. In the Volterra analysis, perfect shorts for the second-order harmonics are assumed. Moreover, the non-linear output capacitance is modeled up to the third order (see Fig. A.1a) using a Taylor series approximation of (A.1) for the applied bias point (V_{DD}). Using these simplifications the phase of V_l is given by,

$$\phi_l = -\tan^{-1}\left(\frac{\frac{3}{4}(C_{M_3}(V_{DD}))\omega}{G_l}\right) \tag{A.2}$$

Note that only C_{M_3} appears to be relevant for the phase of V_l (after resonating out C_{M_1} by the TMN), which is given as,

$$C_{M_3}(V_{DD}) = \frac{1}{2}\frac{C_{j0}}{(1+\frac{V_{DD}}{\phi_B})^{m+2}}\frac{m(m+1)}{\phi_B^2}(V_{ds}-V_{DD})^2 \tag{A.3}$$

Using (A.2), we can note that the output phase ($\angle V_l$), after resonating out the linear capacitance is a function of both the nonlinear output capacitance term C_{M_3} and the applied load ($R_l = \frac{1}{G_l}$). In the proposed VSWR correction technique the output transistor stage V_{DD} and drive level is adjusted to the changing external load.

So V_{DD} and R_l will be a function of the VSWR and C_{M_3} changes accordingly (A.3), affecting the phase of V_l (A.2). Since for a load mismatch of 2:1 VSWR, the change in R_l is $[0.5R_l, 2R_l]$, while the relative change in C_{ds} is significantly smaller (see Fig.A.2c)), we can conclude from (A.2), that non-linear output capacitance term C_{M_3} acts as a catalyst for

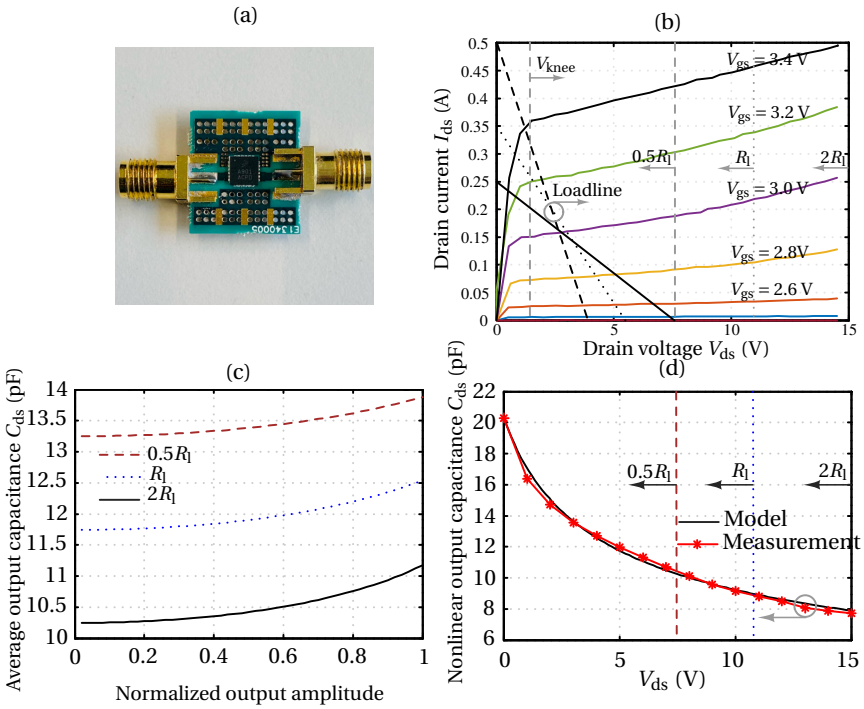

Figure A.2. (a) Dedicated test board for nonlinear output capacitance (C_{ds} extraction), (b) measured I-V curve for a given V_{gs}, the changing ideal load-lines which are dependent on applied load R_l are also added, (c) measured and modeled nonlinear output capacitance as a function of drain-source voltage (V_{ds}), and (c) average nonlinear output capacitance C_{ds} as a function of normalized output amplitude for a given R_l.

the changing loading conditions (VSWR), yielding the changing AM-PM behavior. Logically, an output stage transistor technology with a very low or very linear C_{ds} will benefit the proposed correction technique.

A

A.1.2. DISTORTION ANALYSIS DPA

AM-PM distortion due to Doherty load modulation was analyzed in [71]. In [71], it was demonstrated that the non-linear device parameters (g_m), the input capacitance (C_{gs}, and output capacitance (C_{ds}) of the main and peaking active devices are all responsible for the AM-PM behavior has been demonstrated. However, assuming again, that in our experiments the non-linear behavior of C_{ds} dominates we find using Volterra series on the Doherty admittance matrix of Fig. A.1(b), assuming the even harmonics to be short-circuited, and the linear terms of the C_M and C_P to be resonated out, the output phase of

the DPA ($\angle V_{\mathrm{l}}$) as,

$$\phi_{\mathrm{l}} = \tan^{-1}\left(\frac{Y_0^2}{\frac{3}{4}\omega G_l C_{\mathrm{M_3}}(V_{\mathrm{DD}})}\right) \tag{A.4}$$

In the proposed VSWR correction, the output stages of the main and peaking amplifier are adjusted for their supply voltages to the changing load R_{l} which is bounded by $[R_{\mathrm{l}}/VSWR,\ R_{\mathrm{l}}VSWR]$. Consequently, from (A.4), we can conclude that the DPA output phase dependence results from the presence of main device non-linear output capacitance (C_{M}) and (again) highly depends on the load R_{l}. Without further compensation, the AM-PM distortion will considerably change with the R_l value. In a DPA configuration, where the main device dictates the linearity to a large extent, this condition is most severe for (VSWR = 2, $\angle\Gamma = 180$). Namely, due to the impedance inverter, this (low) external impedance will effectively yield high ohmic loading for the main device. This observation is also consistent with the measurement results (see Fig. 5.10), where the worst-case AM-PM distortion is found for (VSWR = 2, $\angle\Gamma = 180$).

B

APPENDIX

B.1. DPA BACK-OFF EFFICIENCY LOSS ANALYSIS

The impact of losses in the power combining network originating from the active devices (R_D), tunable resonator (R_{TR}), and peak detectors (R_{PK}) on the back-off efficiency of the main PA can be derived using the following assumptions,

- The knee-effect ($R_{on} = 0$) of the device can be neglected.
- The device output network can be modeled as lossy output admittance/impedance with compensated susceptance/reactance.
- The losses of the distributed peak detectors can be combined into a single equivalent loss resistor (R_{PK}) in parallel to the load.

Using the schematic in Fig. 6.1(b), and incorporating the losses. The IDPA back-off efficiency expression assuming class-B operation for the main PA can be derived as follows,

$$\eta_{M,back-off} = \alpha \frac{\pi}{4} \tag{B.1}$$

in which α is,

$$\alpha = \frac{1}{1 + \frac{R_L}{R_{TR}} + \frac{R_L}{R_{PK}} + \frac{Z_1^2 R_L}{Z_2^2 R_{D_M}} + \frac{Z_1^2}{R_{D_M} R_{D_P}} (1 + \frac{R_L}{R_{TR}} + \frac{R_L}{R_{PK}})}$$

and R_{D_M}, R_{D_P}, R_{TR}, and R_{PK} represent the equivalent losses originating from the main device, peak device, tunable resonator, and peak detectors respectively.

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Acronyms

ACLR adjacent channel leakage ratio

ADAM advanced Doherty alignment module

ADC analog to digital converter

AI artificial intelligence

AWG arbitrary waveform generator

dc direct current

DPA Doherty power amplifier

DSA digital step attenuator

ET envelope tracking

EVM error vector magnitude

FET field effect transistor

GaAs gallium arsenide

GaN gallium nitride

GDP gross domestic product

GPIB general purpose interface bus

HEMT high electron mobility transistor

IDPA inverted Doherty power amplifier

ISI inter-symbol interference

LDMOS laterally-diffused metal-oxide semiconductor

LSB least significant bit

LUT look up table

mMIMO massive multiple-input multiple-output

OPCN output power combining network

PA power amplifier

PAE power added efficiency

PAPR peak to average power ratio

SISO single-input single-output

SNR signal-to-noise ratio

SOI silicon on insulator

SPDT single pole double throw

SPI serial peripheral interface

TMN tunable matching network

USB universal serial bus

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SUMMARY

The fifth generation (5G) wireless networks and their successors will drive global economic growth, creating jobs while enhancing productivity. As such, they will positively impact society and industry worldwide by bringing extended wireless capacity and connectivity. To achieve this, 5G networks leverage orthogonal frequency division multiplexing (OFDM) and beam-forming technologies, which require robust linear amplification and wireless transmission. As such, the power amplifier (PA) becomes the performance-determining component in a radio frequency (RF) front-end since it needs to efficiently amplify wideband OFDM signals with high peak-to-average power ratio (PAPR) while being tolerant to changes in the antenna loading and environmental conditions.

PA tolerance to changing loading conditions is hardly addressed in today's PA design and analysis methods. For this reason, placing an isolator in the PA output is currently the only widely used method to achieve PA load resilience. This isolator shields the PA from changes in its load, providing a close to constant RF performance at a marginal RF output power penalty when reflections are present. However, using isolators is problematic in handsets or high-frequency phased-array applications, due to their poor integration, form factor, and costs. When no isolator is used, the linearity of the PA degrades due to its sensitivity to load changes; as such, the digital predistortion unit typically used to linearize the PA must be extended for its algorithm to handle the impact of a changing load. Considering the many PAs with their associated DPD units in a phased array, the overall power consumption of these systems dramatically increases when omitting their isolators.

To tackle the above challenges, this dissertation identifies new PA circuit topologies resilient to changing loading environments. Isolator-like performance can be achieved by introducing load detection and redundancy in the PA circuitry, as described in the following Chapters.

Chapter 2, gives the background theory and context needed to place the results of the following chapters in the proper context. It addresses the modulated signals and systems concepts used in wireless applications and networks. The choice of system architecture dictates the varying loading conditions seen by the PA. Furthermore, it highlights that traditional digital pre-distortion (DPD) solutions become impractical in addressing the load sensitivity of MIMO systems. This underscores the need for inherently load-insensitive or resilient PA's capable of maintaining performance across the changing VSWR, allowing them to function effectively even when paired with DPD systems trained for a constant impedance (e.g., 50 Ω).

Chapter 3, introduces an essential component for adapting the PA to a changing load, i.e., an impedance sensor. These impedance sensors provide information about the complex load impedance seen by the PA when subjected to a mismatch. Various active and passive impedance sensing techniques have been described in the literature. In

this work, passive impedance sensing is used, due to its ability to handle large 5G video bandwidths without requiring power-hungry down conversion and broadband ADCs for signal detection. However, passive impedance sensing traditionally requires a more extensive computation and is bulky. To relax those drawbacks, a new impedance sensing concept based on orthogonality is exploited, allowing the independent determination of the real and imaginary parts of the load. This orthogonal load-detection concept is demonstrated in two networks. First, a standalone sensor network that can be added to an impedance matching network, and second, the impedance sensing has been embedded directly in an output power combining network of an inverted Doherty amplifier.

Chapter 4, introduces a low-loss correction technique for a self-healing power amplifier with a modified two-tap six-port network for load-impedance detection. In this approach, the varying (complex) load is first compensated for its unwanted susceptance, followed by adjustment of the transistor output stage to the provided ohmic load condition, through modifying its supply voltage and drive level. This two-step approach avoids the high-Q conditions that occur in conventional tunable matching networks that aim to correct for both the real and imaginary load deviation in a single step. As such, the proposed solution provides a lower insertion loss and voltage stress. Next, to facilitate a fully automated load mismatch correction without the need for calibration, a modified two-tap six-port network for impedance detection and control loop approach is proposed. As proof of principle, a prototype 900-MHz class-AB power amplifier featuring the proposed correction technique, as well as the six-port reflectometer and control loop, has been implemented as a PCB demonstrator. Measurements show that the self-healing load-insensitive PA under load mismatch exhibits significantly improved PA performance and even approaches the initial PA performance under 50-ohm nominal loading conditions.

Chapter 5, starts with a load-sensitivity analysis of a DPA. From these insights, it is understood that the load line of the main and peaking stages moves in opposite directions for a mismatch condition at the load. Therefore, the DPA can be made insensitive to ohmic load variation by adjusting its supply voltage and input drive of the main and peaking stages in a mirrored approach. Moreover, a low-loss TMN is employed to cancel out any reactive part of the load. Using the proposed concept, it can be demonstrated that the ideal Doherty operation can always be recovered under load mismatch. Measurements of the realized demonstrator show constant output power over a 2:1 voltage standing wave ratio (VSWR) load, with significantly improved efficiency and linearity.

Chapter 6, presents an inverse Doherty power amplifier (IDPA) made load-in-sensitive up to 2:1 VSWR across its fractional bandwidth using a wideband impedance sensor embedded in its output power combining network. To correct for load variation, a low-loss tunable resonator (TR) is used to ensure ohmic loads to the main and peaking stages at the center frequency of operation. At off-center frequencies, the TR is used to restore an ohmic load for the main stage, and the digitally adjustable phase shifter is used to (re)align the main and peaking stage current summation in the output power combining network. The main and peaking stage supply voltages and input drives are adjusted for the ohmic load deviations to maintain the ideal Doherty's output power and efficiency profile associated with 50-ohm nominal loading. To implement the control of this load-correction technique, a wideband impedance sensor has been developed that

offers orthogonality in the detection of the incident and reflected waves while only having four peak detectors. As proof of principle, a prototype 850-950 MHz IDPA has been implemented as a PCB demonstrator featuring the proposed correction technique, the impedance sensor, and the control loop.

Chapter 7, introduces an innovative PA load-correction technique that only relies on the active devices of the PA itself to recover from load mismatch and does not need tunable network elements or supply voltage adjustments. The primary motivation for this technique is to demonstrate load-insensitive PA for high output powers or fast-changing loading conditions. It utilizes a main PA, two auxiliary PAs, and a coupler. Proper adjustment of the input drive levels of the PAs can recover output power and efficiency to a great extent, even when exposed to 2:1 VSWR mismatch conditions. When connected to a 50-ohm load, only the main PA is active. For impedances below or above 50 ohms, besides the main amplifier, one of the auxiliary PAs is activated. The power generated by the auxiliary PA adds in phase to the output power of the main PA, thus allowing the output power to be constant at the expense of a minor efficiency penalty.

Chapter 8, provides an overview of the load-insensitive PA developments in this dissertation and recommends future research and development in this area.

SAMENVATTING

De vijfde generatie (5G) draadloze netwerken en hun opvolgers zullen de wereldwijde economische groei stimuleren, banen creëren en tegelijkertijd de productiviteit verhogen. Daarmee zullen ze een positieve impact hebben op de samenleving en de industrie wereldwijd, door een uitbreiding in draadloze capaciteit en connectiviteit mogelijk te maken. Om dit te realiseren maken 5G-netwerken gebruik van "orthogonal frequency division multiplexing" (OFDM) en bundelvorming-technologieën, die robuuste lineaire versterking en draadloze transmissie vereisen. Hierdoor wordt de vermogensversterker (PA) het prestatiebepalende onderdeel in een radiofrequentie- (RF) keten, aangezien deze efficiënt breedbandige OFDM-signalen met een hoge "peak-to-average power ratios" (PAPR) moet kunnen versterken, terwijl hij tolerant moet zijn voor variaties in antenne impedantie en omgevingscondities.

De tolerantie van de PA voor veranderende belasting wordt nauwelijks behandeld in de huidige ontwerp- en analysemethoden voor PA's. Daarom is het plaatsen van een isolator aan de uitgang van de PA momenteel de enige wijdverbreide methode om ongevoeligheid voor belasting variaties te bereiken. Deze isolator schermt de PA af van veranderingen in zijn belasting en zorgt voor vrijwel constante RF-prestaties met slechts een marginale daling in het RF-uitgangsvermogen wanneer reflecties optreden. Het gebruik van isolatoren is echter problematisch in mobieltjes of bij hoogfrequente phased-array's vanwege de slechte integreerbaarheid, formaat en kosten van een isolator. Wanneer geen isolator wordt gebruikt, verslechtert de lineariteit van de PA door zijn gevoeligheid voor veranderingen in zijn belasting; daarom moet de digitale voorvervormingseenheid (DPD), die normaal gesproken wordt gebruikt om de PA te lineariseren, worden uitgebreid met een algoritme dat rekening houdt met de impact van een veranderende belasting. Gezien het grote aantal PA's met bijbehorende DPD-eenheden in een phased-array, stijgt het totale energieverbruik van deze systemen aanzienlijk als de isolatoren worden weggelaten.

Om bovenstaande uitdagingen aan te pakken, identificeert dit proefschrift nieuwe PA-circuit topologieën die bestand zijn tegen een veranderende belasting. Prestaties vergelijkbaar met die van een isolator kunnen worden bereikt door belastingdetectie en redundantie in de PA-circuits te introduceren, zoals beschreven in de volgende hoofdstukken.

Hoofdstuk 2 biedt de theoretische achtergrond en context die nodig zijn om de resultaten van de volgende hoofdstukken in de juiste context te plaatsen. Het behandelt de gemoduleerde signalen en systeemconcepten die worden gebruikt in draadloze toepassingen en netwerken. De keuze van de systeemarchitectuur bepaalt de wisselende belastingscondities waarmee de vermogensversterker (PA) te maken krijgt. Bovendien wordt benadrukt dat traditionele digitale voorvervorming (DPD)-oplossingen onpraktisch worden bij het aanpakken van debelastingsgevoeligheid van MIMO-systemen. Dit onderstreept de noodzaak van intrinsiek belasting-ongevoelige of veerkrachtige PA's die

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hun prestaties kunnen behouden bij veranderende VSWR-waarden, waardoor ze effectief kunnen functioneren, zelfs in combinatie met DPD-systemen die zijn getraind voor een constante impedantie (bijvoorbeeld 50 Ω).

Hoofdstuk 3 introduceert een essentieel onderdeel voor het aanpassen van de PA aan een veranderende belasting, namelijk de impedantiesensor. Deze sensoren geven informatie over de complexe belastingimpedantie die de PA ondervindt bij een mismatch. In de literatuur zijn verschillende actieve en passieve technieken voor impedantie-detectie beschreven. In dit werk wordt gekozen voor passieve impedantiedetectie, vanwege de eigenschap om signalen met grote 5G-videobandbreedtes aan te kunnen zonder stroomverslindende frequentieomzetting en breedbandige ADC's. Passieve impedantiedetectie vereist echter traditioneel meer berekeningen en neemt veel ruimte in. Om deze nadelen te beperken, wordt een nieuw concept voor impedantiedetectie op basis van orthogonaliteit toegepast, waarmee de reële en imaginaire delen van de belasting onafhankelijk kunnen worden bepaald. Dit orthogonale belastingsdetectieconcept wordt gedemonstreerd in twee uitvoeringen. Eerst als een los sensornetwerk dat kan worden toegevoegd aan een impedantiematchingsnetwerk, gevolgd door een voorbeeld waarbij de impedantiedetectie direct is ingebouwd in het vermogenscombinerend netwerk van een "Inverted Doherty" -versterker.

Hoofdstuk 4 introduceert een correctietechniek voor een zelfherstellende vermogensversterker met een aangepaste twee-taps "six-port" netwerk voor belastingimpedantiedetectie. In deze benadering wordt de variërende (complexe) belasting eerst gecompenseerd voor de ongewenste susceptantie, gevolgd door aanpassing van de uitgangstrap van de transistor aan de aangeboden ohmse belasting, d.m.v. het aanpassen van de voedingsspanning en het aanstuurvermogen. Deze tweestapsbenadering vermijdt de hoge-Q omstandigheden die optreden in conventionele afstembare matchingnetwerken die proberen zowel de reële als imaginaire belastingafwijkingen in één stap te corrigeren. De voorgestelde oplossing zorgt voor lagere verliezen en peakspanningen. Vervolgens wordt, om een geautomatiseerde correctie van belastingmismatch mogelijk te maken zonder kalibratie, een "two-tap-six-port" netwerk voor impedantiedetectie en controle voorgesteld. Om de werking van dit concept aan te tonen is een prototype 900-MHz klasse-AB vermogensversterker gerealiseerd, welke is voorzien van de voorgestelde correctietechniek, namelijk de "six-port reflectometer" met bijbehorende regelkring. Metingen tonen aan dat de zelfherstellende, voor belasting ongevoelige PA onder mismatchomstandigheden aanzienlijk verbeterde prestaties levert en zelfs de oorspronkelijke PA prestaties bij een nominale belasting van 50 ohm benaderd.

Hoofdstuk 5 begint met een belastingsgevoeligheidsanalyse van een Doherty-versterker (DPA). Uit de verkregen inzichten blijkt dat de belastingen van de hoofd- en piekversterker in tegengestelde richtingen bewegen bij een mismatch aan Doherty uitgang. Hierdoor kan de DPA ongevoelig worden gemaakt voor ohmse belastingvariatie door de voedingsspanning en het ingangssignaal van de hoofd- en piektrappen op een gespiegelde manier aan te passen. Daarnaast wordt een afstembaar matchingnetwerk (TMN) ingezet om het reactieve deel van de belasting te compenseren. Met het voorgestelde concept wordt aangetoond dat de ideale Doherty-werking altijd hersteld kan worden bij belastingmismatch. Metingen van de gerealiseerde demonstrator tonen een constant uitgangsvermogen voor een 2:1 voltage standing wave ratio (VSWR)-belasting met een

aanzienlijk verbeterde efficiëntie en lineariteit.

Hoofdstuk 6 presenteert een Inverse-Doherty-versterker (IDPA) die ongevoelig is gemaakt voor belastingsvariaties tot een VSWR van 2:1 over zijn gehele fractionele bandbreedte. Dit is bereikt door gebruik te maken van een breedbandige impedantiesensor die is geïntegreerd in het uitgangsvermogen combinerend netwerk. Voor correctie van belastingvariatie wordt een verliesarme afstembare resonator (TR) gebruikt om een ohmse belasting aan de hoofd- en piektrappen te garanderen op de centrale frequentie. Bij afwijkende frequenties wordt de TR gebruikt om de hoofdtrap opnieuw een ohmse belasting te geven en wordt een digitaal instelbare fasedraaier gebruikt om de stroomsommatie in het vermogens combinerende netwerk van de hoofd- en piektrap weer uit te lijnen. De voedingsspanningen en ingangsaansturingen van de hoofd- en piektrappen worden aangepast voor ohmse belastingafwijkingen, om zo het ideale Doherty-uitgangsvermogens- en efficiëntieprofiel dat bij 50 ohm nominale belasting hoort te behouden. Voor de aansturing van deze belastingcorrectietechniek is een breedbandige impedantiesensor ontwikkeld die orthogonaliteit biedt in de detectie van invallende en gereflecteerde golven, terwijl slechts vier piekdetectoren nodig zijn. Als bewijs van het concept is een prototype 850–950 MHz IDPA gerealiseerd als PCB-demonstrator, voorzien van de voorgestelde correctietechniek, de impedantiesensor en de regelkring.

Hoofdstuk 7 introduceert een innovatieve belastingcorrectietechniek voor PA's die alleen gebruik maakt van de actieve componenten van de versterker om te herstellen van belastingmismatch en dus niet langer afstembare netwerkcomponenten of aanpassingen van de voedingsspanning nodig heeft. De belangrijkste motivatie voor deze techniek is het demonstreren van een belasting ongevoelige PA voor hoge uitgangsvermogens of snel veranderende belastingscondities. Het systeem maakt gebruik van een hoofdversterker, twee hulpversterkers en een koppelingselement. Door de ingangsniveaus van de versterkers correct af te stemmen, kan het uitgangsvermogen en de efficiëntie grotendeels worden behouden, zelfs bij een 2:1 VSWR-mismatch. Bij aansluiting op een 50-ohm belasting is enkel de hoofdversterker actief. Bij een impedantie lager of hoger dan 50 ohm wordt, naast de hoofdversterker, één van de hulpversterkers geactiveerd. Het door de hulpversterker opgewekte vermogen wordt in fase toegevoegd aan het uitgangsvermogen van de hoofdversterker, waardoor het uitgangsvermogen constant blijft met slechts een kleine efficiëntie degradatie.

Hoofdstuk 8 biedt een overzicht van de ontwikkelingen op het gebied van voor belasting ongevoelige PA's in dit proefschrift en doet aanbevelingen voor toekomstig onderzoek en verdere ontwikkeling op dit gebied.

List of Publications

Journal

1. G. D. Singh, H. M. Nemati, M. S. Alavi, and L. C. N. de Vreede. "An Inverted Doherty Power Amplifier Insensitive to Load Variation With an Embedded Impedance Sensor in Its Output Power-Combining Network". In: *IEEE Trans. Microw. Theory Techn.* (2023), pp. 1–15. DOI: 10.1109/TMTT.2023.3277081

2. G. D. Singh, H. M. Nemati, and L. C. N. de Vreede. "A Low-Loss Load Correction Technique for Self-Healing Power Amplifiers Using a Modified Two-Tap Six-Port Network". In: *IEEE Trans. Microw. Theory Techn.* 69.9 (2021), pp. 4069–4081. DOI: 10.1109/TMTT.2021.3096949

Conference

1. G. D. Singh, H. M. Nemati, M. S. Alavi, and L. C. de Vreede. "PA Output Power and Efficiency Enhancement Across the 2:1 VSWR Circle using Static Active Load Adjustment". In: *IEEE Int. Microw. Symp. Dig. Tech. Papers (IMS)*. 2023, pp. 211–214. DOI: 10.1109/IMS37964.2023.10188045

2. G. D. Singh, D. Mul, H. M. Nemati, M. S. Alavi, and L. C. de Vreede. "A Load Insensitive Doherty Power Amplifier with better than -39 dBc ACLR on 2:1 VSWR Circle using a Constant 50 Ω Trained Pre-distorted Signal". In: *Proc. Eur. Microw. Conf. (EuMC)*. 2022, pp. 222–225. DOI: 10.23919/EuMC54642.2022.9924452

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Gagan Deep Singh was born in Wander Jatana, Punjab, India in 1992. He received a B.E. degree in electronics and communication engineering from Visvesvaraya Technological University (VTU), Belgavi, Karnataka, India (2010-2014), and an M.Tech degree in RF & Photonics from the Indian Institute of Technology (IIT), Guwahati, Assam, India (2016-2018). He worked as a software engineer with L&T Infotech, Pune, Maharashtra, India from 2014-2016 and as a Technologist at Tata Steel, Jamshedpur, Jharkhand, India from 2018-2019. Currently, he is working towards his Ph.D. degree at Delft University of Technology, Delft, The Netherlands. His research interests include analog and radio frequency (RF) integrated circuits.

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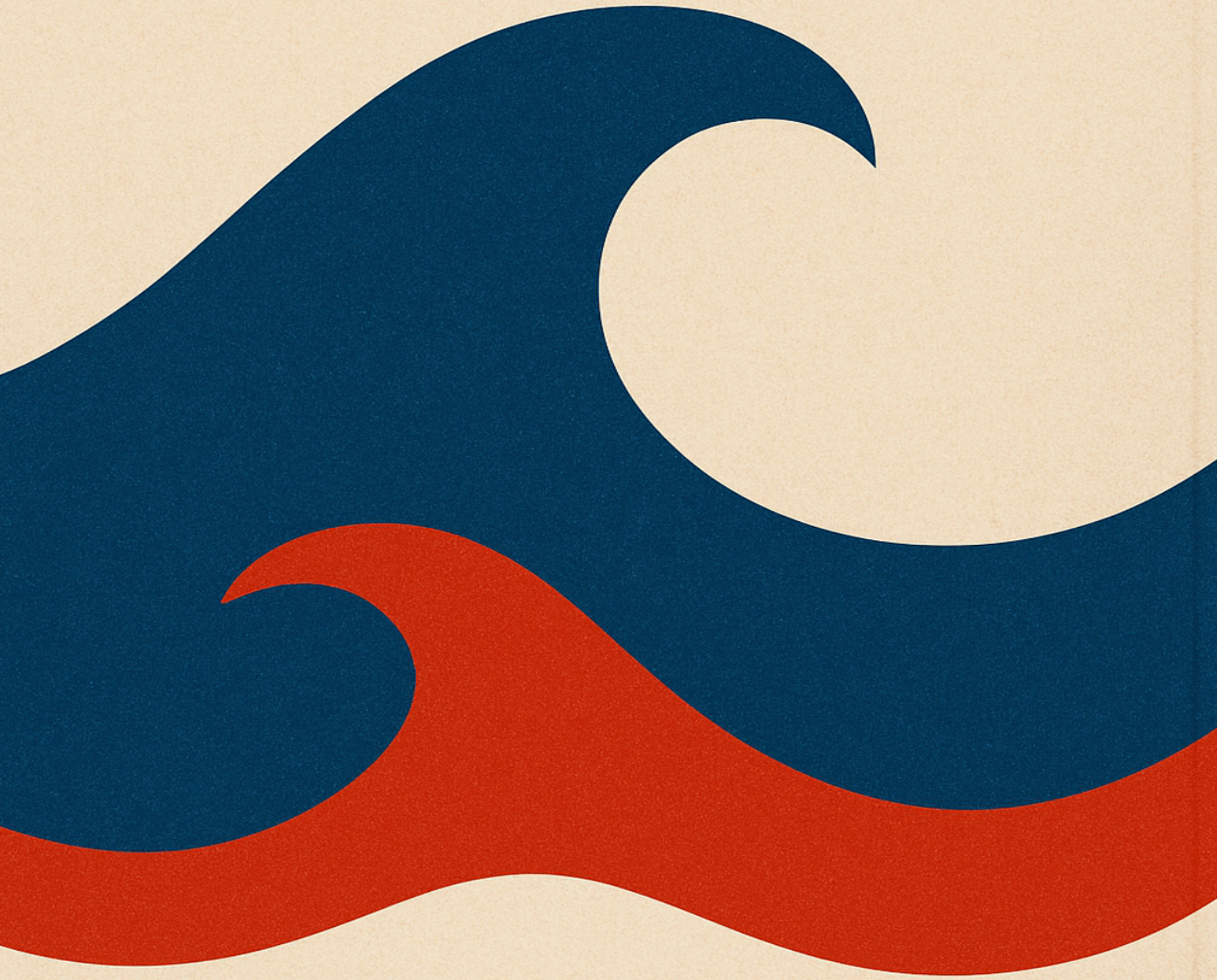

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