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# Integrated Waveguide Power Combiners with Artificial Dielectrics for mm-Wave Systems

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***Abstract*—In this contribution we present a new class of N:1 power combiner based on synthetic waveguides integrated in silicon technologies back-end-of-line. The input feeding is based on (N) E field probes employing capacitive resonance, feeding a waveguide with artificial dielectrics (ADs). The signal summation occurs on a single transverse plane, thus providing insertion losses which do not scale with the number of inputs. This results in a combiner more compact and without restriction in the number of inputs compared to the traditional power of two ($2^N$) combiners. The power combiner operation is presented in a BiCMOS technology implementation and analyzed by means of full wave electromagnetic (EM) simulations.**

**Finally, the experimental results of an integrated 4:1 back-to-back-combiner operating in the 240-310GHz band is presented and compared with the full EM model.**

***Index Terms*—Integrated circuit, BiCMOS, waveguide, artificial dielectric, power combiner, (sub)millimeter-wave.**

## I. Introduction

The continuous advance of the maximum oscillation frequency of silicon-based technologies (i.e., BiCMOS and RF-CMOS) is paving the way for the deployment of mm-wave frequency systems in large volume commercial applications, i.e., FMCW automotive radars and 5G communications.

One of the remaining challenges for such systems, in both sensing and communication applications, is the limited output power that can be achieved, due to the low supply voltage and limited breakdown of the active devices. For this reason, combining techniques are exploited to increase output power, while maintaining high stage gain (small size/ high $f_{max}$ transistors) and low impedance transformation ratios (reducing the insertion losses due to the finite $Q$ of the components).

Power combining was achieved using transformer based circuitry in [1], [2] and with corporate transmission lines based combiners in [3], [4]. Both approaches are based on cascading 2:1 combiners (i.e., transformer or transmission line combiners), providing increased losses with increasing number of amplifier cells. Moreover, both techniques are only suited to sum power of 2 elements ($2^N$), thus not optimizing area consumption when a specific power level, set by the application, is required. In this contribution we present a novel combining technique, employing synthetic waveguide integrated in the back-end-of-line (BEOL) of a BiCMOS technology, capable of achieving

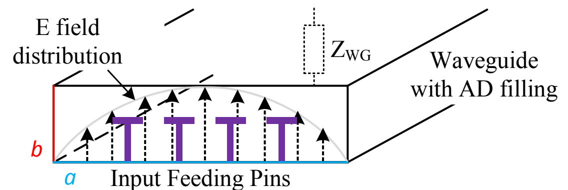


Fig. 1. Sketch of the combiner topology based on multiple feeding (E field) probes inside a waveguide using ADs to engineer the effective permittivity.

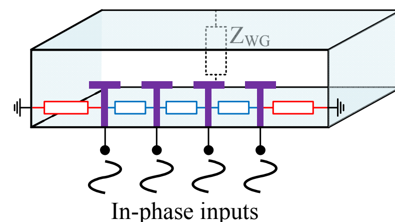


Fig. 2. Sketch of the mutual interactions among feeding pins, when the combiner is driven with in-phase signals.

insertion losses almost independent of the number of input elements. The integrated waveguide employs artificial dielectrics (ADs) [5], [6] to provide an extra design parameter to control the waveguide width and impedance at a given frequency. The manuscript is organized as follows: first we present the signal summation concept, then, different integrated combiners ($N$:1) are described and modelled by full-wave electromagnetic (EM) simulations. Finally, a prototype 4:1 back-to-back power combiner, integrated in the back-end-of-line (BEOL) of a BiCMOS technology, is presented, and the experimental results in the 240-310 GHz band are compared with the full EM model.

## II. Waveguide In-Phase Power Combiners

Probe feeding to a waveguide environment, such as the one employed in conventional coaxial to waveguide transitions, consists of a pin entering from the broad side of a rectangular waveguide. Typically, the probe is located in the center of the broadside wall, where the electric field is maximum and located $\lambda/4$ away from a back short, opposite to the direction of propagation. The pin is usually terminated with a capacitive plate, to resonate out the inductive contribution of the feed. When multiple feeding pin are employed, as shown in Fig. 1, each feeding

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point will experience a different *E*-field intensity along the well-known half sine distribution.

The ADs consist of sub-wavelength metallic inclusions whose spatial density can be engineered to synthetize a material with a desired relative permittivity $\varepsilon_{r,eff}$. When filling the waveguide with ADs, the guided wavelength ($\lambda_g$), and thus the cutoff frequency for a given width *a* (Fig. 1), can be tuned via the permittivity boosting factor ($\varepsilon_{r,eff}/\varepsilon_r$). Note that also the waveguide impedance ($Z_{WG}$) can be engineered when using ADs due to the dependence of the cutoff wavenumber ($k_c$) on *a* and *b*, see Fig. 2. When in-phase signals are considered at the input of the feeding pins (i.e., zero-phase combiner), the loading impedance at the center pins will be given by the waveguide impedance ($Z_{WG}$) times the number of feeding pins (*N*). This allows to scale up the usually low impedance (due to the condition that $b<<a/2$) of BiCMOS integrated waveguide, thus providing the proper loading condition to the amplifier stages. The edge pins will see a lower loading condition, due to the decrease of the *E*-field, and a higher capacitive loading due to the coupling to the sidewalls which are not bootstrapped by the in-phase feeding, as can be seen in Fig. 2.

## III. BiCMOS Integrated N:1 Power Combiners

The BEOL of the considered technology, see Section IV, consists of six copper layers (M1-M6) and a top aluminum layer (AL), with M2 and AL used as bottom and top broadside walls of the waveguide, respectively.

The AD pillars are realized using the M3 to M6 layers including the vias, as shown in Fig. 3, providing the capability of engineering the $\varepsilon_{r,eff}$ as well as helping with DRC density requirements. Differently from the sketch in Fig. 1 a connected capacitive plate is employed to minimize area. The dimensions of the waveguide section (tradeoff between size reduction and increased losses due to the ADs) are shown in Fig. 3.

The *N*:1 power combiner is then realized using the arrangement of input and output pins shown in Fig. 3 (where a 4:1 is considered in the specific case). Three different combiner topologies are then considered for the EM analysis, a 2:1, a 4:1 and a 6:1, with the combining pin distribution as shown in Fig. 4.

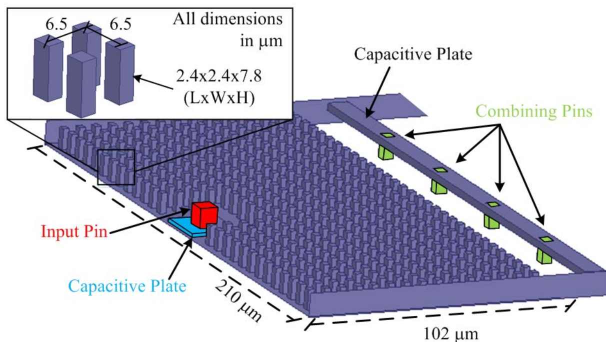


Fig. 3. EM structure of the BiCMOS integrated 4:1 power combiner, with AD layer used in HFSS. Lumped port excitation used at the feeding pin locations.

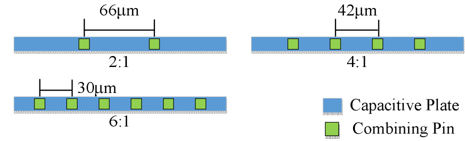


Fig. 4. Distribution of the combining pins for the different BiCMOS integrated power combiners, the waveguide width is kept constant at 210 µm.

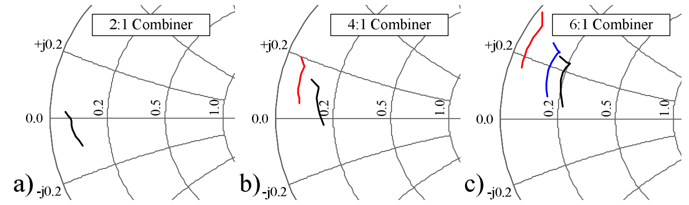


Fig. 5. Active impedance seen at the combining pins for the a) 2:1, b) 4:1, c) 6:1 combiner. Due to symmetry impedance of mirror pins are removed.

All the structures were analyzed using Ansys HFSS full wave EM simulator. The active impedance seen at each port, when all (combining) ports are driven in phase is shown in Fig. 5. From the normalized Smith chart (50 Ohm) it can be seen how the center pins (black line) experience an increasing impedance with the number of pins, as described in Section II. The edge pins (red curve), are located closer to the waveguide walls, thus experience a lower impedance (due to the half-sine *E*-field variation) and a higher capacitive loading, as can be seen by the increased phase rotation. The intermediate pins in the 6:1 combiner (blue line) present a load impedance closer to the center pins. Impedance asymmetries can be minimized by reducing the lateral distance among the pins, while phase rotation of the edge pins can be compensated by tapering their capacitive plate. The insertion losses of the various structures are computed using the maximum available gain formulation, which allows to remove the losses due to mismatch at the input and combining pins. The EM simulated insertion losses for the three considered combiners are shown in Fig. 6.

The insertion loss variations between the three combiners is less than 1dB in the 240-310 GHz range, and is not linked to the number of inputs, as is the case for the transformer and transmission line combiners.

## IV. Integrated Prototype

A prototype structure of a 4:1 power combiner was fabricated in the BEOL of Infineon 130 nm SiGe BiCMOS technology B11HFC, providing a six-layer copper metallization. To allow the characterization of the power combiner in a two port VNA environment, a 4:1 back-to-back power combiner operating between 240 and 310 GHz was designed. The half structure is described in Fig. 7, and the entire chip micrograph is shown in Fig. 8. The prototype consists of a ground-signal-ground input (probe pads), followed by a microstrip line impedance transformer to connect the input feeding pin to a waveguide section with AD layer. The feeding pin is loaded with a capacitor (constructed with a patch in layer M3) to tune out the inductance of


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the feeding pin. The waveguide is loaded with AD pillars (from layer M3 to M6) achieving an $\varepsilon_{r,eff}$ of 14, chosen as a tradeoff between lateral size reduction and increased ohmic losses (due to current on the finite conductivity AD pillars). At the end of the (102µm) waveguide section, four identical feeding pins are equally spaced along the waveguide transverse direction. These feeding pins are reversed (compared to the input one) providing an output to layer M2, to provide a low loss interface when active circuitry is employed, while the capacitive load is placed on layer M6. To minimize the space occupancy in the longitudinal direction the patches at M6 are connected in a unique strip extending close to the waveguide walls. A back short is placed at a $\lambda/4$ (at 280 GHz) distance, to maximize the coupling to the four feeding pins. The four equi-spaced probes are then connected with CPW lines (i.e., using M2 and M3 layers) to the symmetric/mirrored combiner to realize the back-to-back structure.

The quarter wavelength waveguide is also filled with AD pillars (M6) that enhance the effective permittivity to 5.45. The large permittivity ratio of the two AD sections surrounding the pins further reinforces the coupling between the primary waveguide section and the pins.

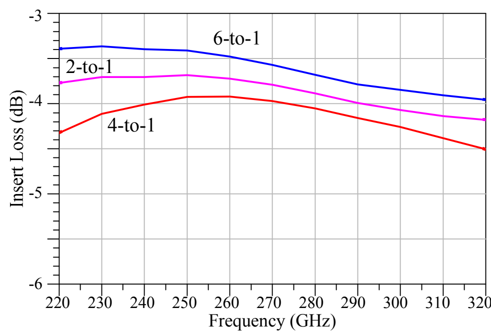


Fig. 6. Simulated insertion loss of the various combiners using the EM model of Fig. 3, computed using the max available gain formulation.

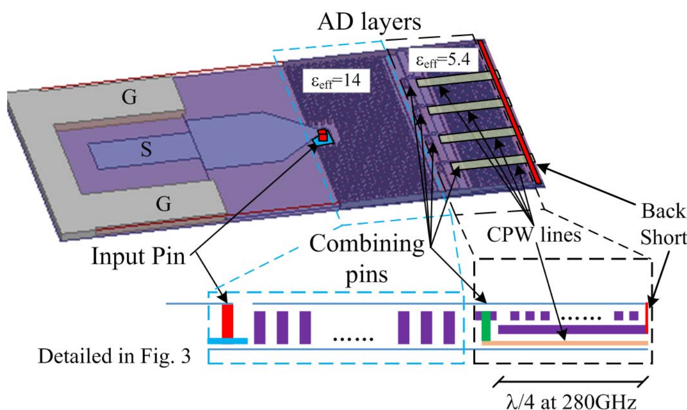


Fig. 7. Half structure of the integrated prototype of 4:1 power combiner with integrated waveguide. Inset of the side view of the power combiner and the back-to-back connector.

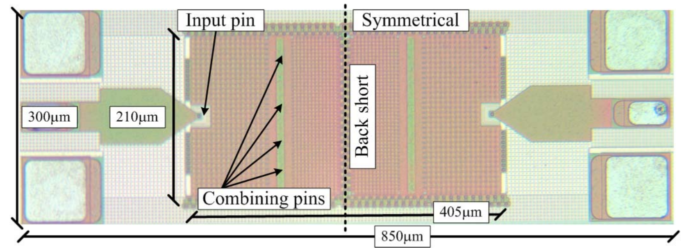


Fig. 8. Chip micrograph of the implemented prototype.

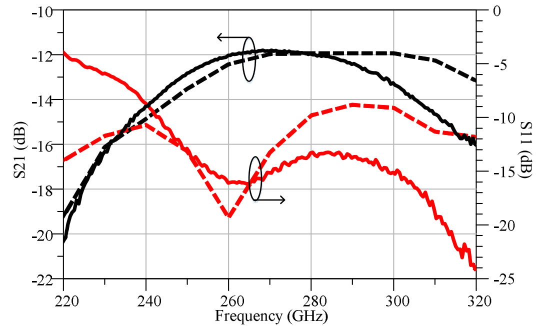


Fig. 9. Simulation (dashed lines) and measurement (solid lines) results of the 4:1 back to back prototype, simulation and measurement performed both at the pads reference plane.

## V. Experimental Results

The prototype shown in Fig. 8 was measured using a Keysight network analyzer (PNA) and OML Inc. mm-wave module extenders in the WR3 band. Wafer probes from GGB Industries were employed to provide the required coplanar ground-signal-ground (GSG) signal. The results of the back-to-back structure are shown in Fig. 9 and compared with full wave 3D simulations performed with Ansoft HFSS. The measured results agree well with the simulated results (using homogenous frequency tabulated tangent loss material).

The discrepancies from 300GHz could be given by the different reactive loading, around the pins in the homogenous dielectric. The agreement between the measured and simulated structure provides a direct validation of the EM based analysis presented in Section III, which cannot be directly verified due to extreme complexity of measuring structures with more than two ports at mm-wave frequencies. The measured structure includes additional losses (i.e., input pads/line and CPW structures), when removed results agree with data in Fig. 6.

## VI. Conclusion

In this contribution we introduced $N$:1 combiners based on BEOL integrated waveguide employing ADs. Important advantages of this solution is that the combiner is not limited to $2^n$ inputs and presents insertion losses that do not increase proportionally to the number of inputs. A back to back 4:1 combiner was integrated in the BEOL of a BiCMOS technology, and characterized in the WR3 band. The measured results are in


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good agreement with the prediction from full-wave simulations.

## ACKNOWLEDGMENT

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