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M.Sc. Thesis

A Methodology for Early Exploration of TSV Interconnects in 3D Stacked ICs

Radhika S. Jagtap

Abstract

Planar scaling of semiconductor ICs for achieving higher integration seems to be on the brink of saturation. As an alternative solution, three-dimensional (3D) integration follows a *more than Moore* strategy in which circuit layers are stacked vertically. Although, 3D integration technology has moved from *Lab to Fab*, a complete supply chain is yet to fall in place. Due to the lack of a fully automated 3D IC design flow, realistic performance estimation at an early stage becomes imperative to ensure an efficient end-to-end design cycle. In this thesis, an approach is shown for early performance and cost estimation of a 3D stacked IC in order to allow critical technology parameters to influence system design decisions. A novel methodology is proposed which explores *Through-Silicon-Via* (TSV) placement topologies for a 2-tier vertical interconnect across two performance corners of the TSV technology. It estimates electrical performance and TSV area penalty which are then translated to system design metrics. The methodology is applicable to digital ICs and offers *flexibility* in selection of the CMOS technology node and the 3D stacking granularity. The implementation of the methodology in SystemC efficiently achieves *parameterizability* and enables its integration into a high-level system simulation framework. By applying the methodology to a case of a 7-port 3D router it was found that, the most preferred TSV placement topology in terms of performance and cost is *Isolated* for 45 *nm* technology node and *Shielded* for 32 *nm* technology node.

A Methodology for Early Exploration of TSV Interconnects in 3D Stacked ICs

Thesis

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requirements for the degree of

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in

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by

Radhika S. Jagtap
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This work was performed in:

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The undersigned hereby certify that they have read and recommend to the Faculty of Electrical Engineering, Mathematics and Computer Science for acceptance a thesis entitled **"A Methodology for Early Exploration of TSV Interconnects in 3D Stacked ICs"** by **Radhika S. Jagtap** in partial fulfillment of the requirements for the degree of **Master of Science**.

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Acknowledgments

An impression that 3D integration technology is a fantastically brilliant idea had made me pick it up as an essay topic 2 years ago for the *Introduction to Microelectronics* class. The impression still holds. I am thrilled that I got a chance to explore this field in the Circuits and Systems Research Group!

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Finally, I would like to dedicate my thesis to my grandparents.

Radhika S. Jagtap
Delft, The Netherlands
21/09/2011

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Abbreviations

3D	Three Dimensional
3D IC	3D Integrated Chip
3D MPSOC	3D Multi-Processor System-On-Chip
3D NOC	3D Network On Chip
3D-SIC	3D Stacked IC
3D-SOC	3D System On Chip
3D-WLP	3D Wafer Level Packaging
AMS	Analog Mixed Signal
BC	Best Case
BEOL	Back End Of Line
DE	Discrete Event
ELN	Electrical Linear Network
ITRS	International Technology Roadmap for Semiconductors
KOZ	Keep-Out-Zone
RDL	Redistribution Layer
RLC	Resistance, Inductance, Capacitance
SOI	Silicon-On-Insulator
TSV	Through-Silicon-Via
WC	Worst Case

1 Introduction

1.1 Motivation

1.1.1 3D Integration Technology

Conventional mainstream VLSI chips have had performance gains largely based on technology scaling. Scaling involves shrinking the transistor length which results in smaller and faster transistors. With this, a higher level of integration can be achieved on the same area of Silicon thus reducing costs. However, this legacy of planar scaling which has been fulfilling the prophecy in Moore's Law seems to be nearing saturation. One of the primary reasons is that physics involved in semiconductor lithography puts a limit to transistor dimensions. Another issue related to scaling is regarding interconnect, i.e. on-chip wiring that establishes connections between devices on the chip. Interconnect does not scale at the same pace as transistors as a result of which communication blocks cannot keep up with increasingly faster computation blocks. Looking towards future high performance systems, *three dimensional (3D) chip integration* can be an alternative solution to planar scaling and can also complement it to achieve higher integration.

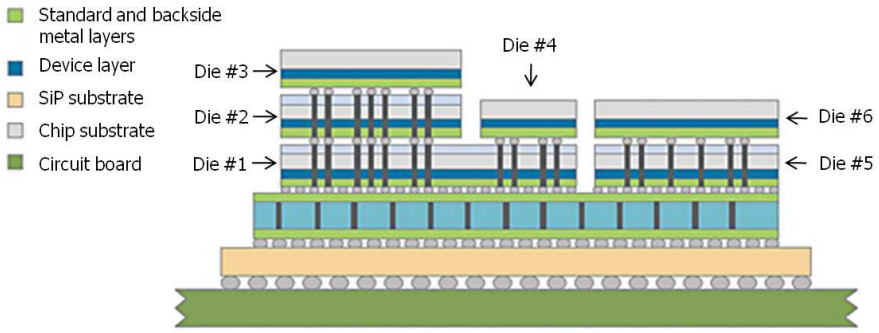


Figure 1.1: Conceptual diagram of a 3D stacked IC.

3D technology involves integrating multiple conventional circuits by stacking them and thus growing the chip in the third, i.e. vertical direction as shown in Figure 1.1. These circuits are called as device layers and conventionally may be on different semiconductor dies or may be different functional blocks on the same die. Interconnections between circuits in the layers of a stack are implemented through a vertical interconnect composed of *Through-Silicon-Vias* (TSVs). Such a vertical interconnect can potentially be much faster and consume lower power due to its short length compared to horizontal interconnect in large complex designs. 3D architectures have been

explored in [1, 2, 3], where placing multiple processing elements and a communication fabric in a 3D stack is projected to achieve higher system performance. The immediate intuitive reaction to the concept of 3D integration is that it could be the next scaling engine for semiconductor technology [1].

1.1.2 Performance Estimation

A shift in paradigm such as from 2D to 3D needs to be supported with research on the type of applications it can benefit and the implications on design methodologies. Challenges are associated with adapting several segments in the chip design flow in order to *conceive* chips as 3D as opposed to merely stacking conventional 2D chips. Meanwhile advances and pitfalls of new processes in fabrication technology are uncovered which result in a revision of technology models and methodologies. Thus, the primary reason for the lack of a fully automated 3D chip design flow is that 3D technology is still not sufficiently mature for a complete supply chain to be in place. However, several methodologies, tools and algorithms for physical design have been developed [4, 5, 6, 7, 8, 9] which have been significant contributions towards EDA for 3D technology.

With the advent of 3D, architecture space exploration must take into account the benefits of 3D stacking. The main purpose of architecture exploration is to evaluate if and how the ideal functions and algorithms can be mapped onto a system architecture and to verify the actual functionality for an architecture. Next, non-ideal properties of the structures and interfaces for an architecture can also be incorporated into the exploration. Architecture space exploration involves simulating different architectures to find out the trade-offs between one or more typical performance parameters like execution time, throughput and speedup. The typical cost functions like area, power, cost, complexity and design time are evaluated. A performance estimate and cost analysis is performed at a system level at an early stage of design to evaluate a technology and an architecture for a given application. Eventually, accurate performance results are obtained only after completion of a comprehensive chip design flow for a chosen architecture and a target technology. Long execution times and re-work are characteristic to any such comprehensive chip design flow. On the other hand, system simulations and architecture space explorations can provide early and quick estimates with the help of models. This makes it critical to have better *simulation methodology* and *models* at system and architecture levels in order to have an efficient end-to-end design cycle.

1.2 Problem Definition

The objective of this work is to solve the following research problems:

- To estimate the performance and cost of a TSV-based vertical interconnect in the context of 3D architecture exploration for high performance digital systems.

- To find a set of design considerations that directly impact performance and cost of such a vertical interconnect e.g., technology parameters and guidelines.

- To show an approach for a 3D system simulation methodology that abstracts important technology parameters and translates them into system performance and cost metrics.

1.3 Solution

Since *Through-Silicon-Via* (TSV) is a key technology enabler for 3D chip integration, understanding the electrical performance of TSV-based interconnect is of prime importance in order to solve the problem of performance estimation of a 3D chip stack. Physical effects of TSVs that influence performance and cost need to be taken into account to judge the gain and overhead coming from 3D technology. After studying a variety of contemporary TSV models, an electrical model of TSV is selected which matches closely with the requirements of high performance digital systems. Moreover, this model expresses the parasitic components like resistance (R), capacitance (C) and inductance (L) of a TSV as a function of parameters like geometry, material properties and clock edge rate. Thus the objective of highlighting important technology parameters can be met.

TSV-based vertical interconnect can be utilized for three levels of stacking granularity which are studied in this thesis. These are as follows.

1. 3D Wafer Level Packaging (3D-WLP) is used for stacking dies and is a *Packaging level* solution.

2. 3D System-On-Chip (3D-SOC) is used for stacking tiles or IP cores and is a *Global interconnect level* solution.

3. 3D Stacked IC (3D-SIC) is used for stacking smaller logic blocks and is an *Intermediate interconnect level* solution.

A methodology is proposed for simulation of 3D-SOC and 3D-SIC with interconnect topology exploration. By sweeping TSV parameters in a realistic range, *Best Case* and *Worst Case* corners are derived which result in minimum and maximum delay through the TSV respectively. Thus the proposed methodology gives results for two corners of TSV technology.

Performance of TSVs in isolation can be misleading to evaluate the performance of a 3D architecture. Hence a *tier-to-tier vertical channel* is implemented which incorporates a CMOS driver at the source end and a CMOS loading gate at the destination end. The presented electrical circuit of this path is built using key parasitic components in order to simplify the overall path model while still achieving reasonable accuracy for taking an early design decision. The presented vertical channel path which is implemented as an RLC network is validated by comparing to a SPICE simulation of its gate level netlist. To study the impact of planar circuit technology on 3D architecture performance, the driver and loading gates as well as the horizontal interconnect are explored across 45 nm and 32 nm CMOS technology nodes. Design considerations like *capacitive cross-talk* and *Keep-Out-Zone* for thermo-mechanical stress must be evaluated as they directly impact performance and area metrics respectively. Different TSV placement structures are analyzed with respect to trade-offs between performance and area. The proposed

methodology generates 4 TSV placement topologies termed as *Border*, *Bundle*, *Shielded* and *Isolated* for a 2 tier 3D-SOC.

The RLC path model is simulated in *SystemC-AMS*, a high-level simulation environment. This paves the way for further integrating such a methodology into a tool for 3D system simulation. Thus, the objective of showing an approach for 3D system simulation by employing selected technology parameters that are translated into system performance and cost metrics is achieved. The proposed methodology is applied to a relevant case of TSV interconnect design for a *7-port 3D router*. The performance and cost analysis as a result of the exploration methodology leads to the selection of the most preferred topology for the given router. The translation of the performance and cost estimates to *system-level metrics* is also highlighted.

The solution designed has attributes like flexibility to add or update technology parameters related to 2D and 3D technology and low design complexity which is achieved through coarse-grained floorplan algorithms for exploring fixed set of TSV-placement topologies. A contribution to research in this area is well motivated and challenging since it requires combining knowledge of electrical circuit level design and TSV technology to provide a bottom-up insight for high-level system design of 3D ICs.

1.3.1 Contributions

The main contributions of this work to the current state of the art are as follows.

1. An idea of exploration of *TSV placement topologies* is realised. The area penalty of TSVs including the Keep-Out-Zone and the capacitive coupling induced noise is combined in a unique manner to create topologies which represent a few extreme points in the design space.

2. An approach is shown for a simulation methodology which generates a vertical interconnect model for a set of fixed topologies for a given design. The simulated electrical performance of the TSV interconnect and the TSV area overhead are translated to useful *system metrics* for performance and cost. These metrics in turn facilitate a more informed decision at system-level compared to related work in 3D system performance estimation.

3. A novel methodology is proposed which offers a selection of *stacking granularity* (Global or Intermediate) and CMOS process *technology node* (45 *nm* or 32 *nm*). It provides electrical performance of the TSV interconnect and the TSV area overhead for 4 explored topologies across 2 *performance corners* of the TSV technology.

4. The proposed methodology is implemented in SystemC which uses a mix of C++ functions and Analog Mixed Signal primitives which provides for abstraction, hierarchical designing, scalability and parameterizability. This enables a potential integration of the methodology into a *high-level system simulation* framework.

1.4 Thesis Organization

This thesis is organized in the form of the following chapters:

Chapter 2 gives a brief overview of 3D integration technology and identifies three levels of 3D stacking which are the focus of this work. This chapter also gives a critical analysis of related work and outlines the approach employed to solve the defined research problem.

Chapter 3 analyzes parameterized electrical models of TSVs and derives two performance corners of the TSV technology. It also presents and validates the tier-to-tier path model of the vertical channel that is further employed by the simulation methodology.

Chapter 4 discusses the factors that lead to the development of several TSV placement topologies which vary in arrangement of TSVs and spacing between them. Then a comparison of these topologies in terms of electrical performance and area penalty incurred by TSVs is carried out and finally the SystemC methodology which incorporates exploration of TSV interconnects is proposed.

Chapter 5 describes a relevant case of a 7-port 3D router and applies the proposed simulation methodology. The resulting estimates of performance and cost are translated to system design metrics and a recommendation for the most preferred TSV placement topology for the 3D router is made for 45 nm and 32 nm technology nodes.

Chapter 6 summarizes the thesis by highlighting the objectives that were achieved and providing the larger scope of the work.

2 Background

This chapter describes the relevant work in 3D technology and hierarchical taxonomy for stacking. It also describes the prior art which is the inspiration for this work. Lastly, it describes the approach employed to achieve the objectives of this work.

2.1 2D and 3D Technology

Conventional planar on-chip interconnect is in the form of metallization layers also known as Back End Of Line (BEOL). It is typically 9-12 metal layers starting from the lowest called M1 which has the minimum dimensions. Since M1 is the first metal layer next to the device layer it is also termed as local interconnect. The next 3-4 layers are termed intermediate and have the same pitch as M1 layer, that is 1x M1. Then onwards, higher layers for an MPU chip have a pitch of 1.5x M1 to about 2 μm and are called global interconnect. BEOL terminology varies for an ASIC where the next 2-3 layers after the Intermediate are termed semi-global (pitch of 2x M1) and remaining layers till the highest are termed global. The RC delay and capacitance per unit length for these interconnect types are summarized in Table 2.1 [10].

Year of Production	2010	2012	2015
Capacitance in pF/cm for global wire	2.0	2.0	1.9
RC Delay in ps for 1 mm length global wire	10	10	10
Capacitance in pF/cm for intermediate wire	2.0	1.8	1.7
RC Delay in ps for 1 mm length intermediate wire	1892	4428	12851
Capacitance in pF/cm for M1 wire	2.0	1.8	1.7
RC Delay in ps for 1 mm length M1 wire	2100	5068	14474

Table 2.1: Roadmap for RC delay and capacitance for planar interconnect [10].

Moving from 2D to 3D, early works approached vertical stacking from the packaging perspective wherein pre-packaged ICs are stacked. Some examples of these are the 3D MCM-V a vertically stacked multi-chip module technology for packaged devices [11] and die stacking using fine-pitch flip chip interconnects [12]. IMEC in Leuven has contributed significantly towards research in the area of 3D Packaging [13]. The other approach, which is the focus of this work, is to build a monolithic fully-integrated 3D IC where the fabrication process is adapted for stacking of multiple device layers and formation of vertical interconnect prior to packaging. There are many methods to establish connectivity between inter-chip layers, such as wire-bonding, edge connect, capacitive or inductive coupling method and direct contact using Through-Silicon-Via

(TSV).

TSV is a deep hole etched through Silicon which is filled with metal and provides electrical connection to the face or back or both. Face refers to the interconnect metallization side of the chip while back refers to the substrate side. Dies are bonded back-to-face or back-to-back such that a TSV formed through Silicon substrate establishes high speed interconnect between two tiers by virtue of a very small wire length of about 20-100 μm. This bonding can be done between two wafers (W2W), between a wafer and a die (D2W) or between two dies (D2D). Besides bonding, another processes that is critical in TSV formation is wafer or die thinning. More information on the process steps in wafer-to-wafer bonding technology can be found in [14, 15, 16, 7].

TSV technology provides high bandwidth die-to-die interconnect since TSV diamater ranges between 1 μm upto 50 μm [17, 14, 18, 19]. In conventional planar design, off-chip signaling between two dies is constrained in bandwidth due to large chip pads ranging from 20 μm to 130 μm [10] which limit the pin count. Also, off-chip signaling through long wires on a PCB results in slower interfaces. On the contrary, delay through a TSV-based vertical interconnect and the power dissipation in it are both reduced since the parasitic resistance and capacitance are each potentially one order or more smaller than on-chip planar interconnect [20]. Moreover, 3D technology offers heterogeneous integration. This means that multiple dies utilizing same or disparate technologies can potentially be integrated to get a high performance System-on-Chip (SOC). Thus, a functional block can be designed by fully optimizing the technology best suited for it and fabricated on a separate die. A typical example that can benefit dramatically from high bandwidth low latency TSV-based interconnect is high density DRAM memory stacked on a processor fabricated in high speed SOI CMOS technology [21, 22, 23]. To summarize, there have been a fair amount of developments in TSV technology and it has shown promising results so far. Hence, this work is centred around TSV as a means to establish connectivity between inter-chip layers.

To estimate such performance benefits electrical characteristics of TSV-based interconnects must be known. Typical performance parameters for a wire are delay through the wire, capacitive cross-talk between wires, mutual inductance etc. In order to analyze electrical behavior, it is desirable to apply well established practices in EDA for planar chip design to model the physical TSV structure as an equivalent circuit with lumped parasitic components. Hence compact models to obtain TSV parasitic components as a function of physical geometries and material properties are essential to perform fast simulation and computation of performance metrics.

2.2 Taxonomy and Roadmaps

The International Technology Roadmap for Semiconductors (ITRS) provides an Interconnect Roadmap for planar, 3D and alternative emerging interconnect technologies. The technology parameters used for this work are based on 2010 ITRS Update for years 2009 to 2015 [10] as these are of great research interest and are also well supported from the point of view of manufacturability.

The technology projections for years 2010, 2012 and 2015 are given in Table 2.2.The

Year of Production	2010	2012	2015
DRAM 1/2 Pitch (nm)	45.0	35.7	25.3
MPU/ASIC Metal 1/2 Pitch (nm)	45.0	31.8	21.2
MPU Physical Gate length (nm)	26.5	22.1	16.8
Inferred Technology Node (nm)	45	32	22

Table 2.2: Technology projections from ITRS 2010 Update [10].

22 nm technology node however is not included in this work because it is still in research stage and circuit technology is projected to deviate from CMOS towards more vertical gate structures like FinFETS. CMOS technology models corresponding to 45 nm and 32 nm nodes are used for modeling in this work.

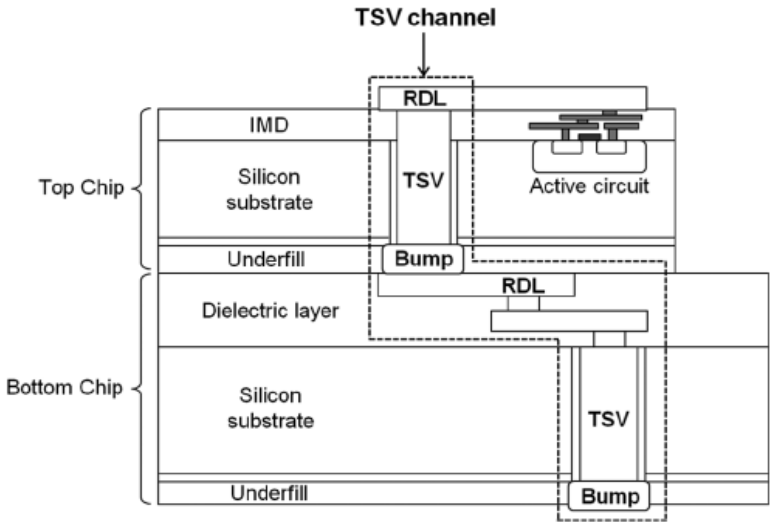


Figure 2.1: TSV channel in a 3D-WLP including TSV, bump and RDL [24].

The ITRS 2010 Update also provides a taxonomy of 3D interconnect technologies based on interconnect hierarchy [10]. At the highest level, there is 3D Packaging (3D-P) which does not employ TSVs and is based on traditional packaging techniques like wire-bonds located on the periphery to connect dies. 3D Wafer-level Packaging (3D-WLP) makes for an attractive option since there is flexibility in placement of TSV over the area of the chip as compared to 3D-P.

The vertical interconnect for 3D-WLP stacking technology requires TSVs, bumps and a Redistribution Layer (RDL). A bump provides a joint between stacked chips and the RDL provides a horizontal interconnection to redistribute the signals between different I/O pin locations on heterogeneous dies as shown in Figure 2.1.

Figure 2.2a illustrates the 3D System-On-Chip (3D-SOC) technology which is a stacking solution at the global interconnect level. 3D-SOC technology is targeted for

Level	Name	Supply Chain	Key characteristics
Package	3D Packaging (3D-P)	OSAT Assembly PCB	Traditional packaging. Also includes die in PCB integration. No TSVs.
Bond pad	3D Wafer-level Package (3D-WLP)	Wafer-level Packaging	WLP infrastructure (RDL and bump) Post-IC fabrication (via last process) TSV density follows bond pad requirement, Pitch of 20 μm-100 μm (Table A.1)
Global	3D System-on-Chip (3D-SOC)	Wafer Fab	Stacking of IPs, tiles, memory banks Unbuffered I/O drivers (Low capacitance) High density TSV, Pitch of 4 μm-16 μm (Table A.2)
Intermediate	3D Stacked IC (3D-SIC)	Wafer Fab	Stacking small blocks (parts of IPs) Mainly wafer-to-wafer stacking Very high density TSV, Pitch of 1 μm-4 μm (Table A.3)
Local	3D Integrated Circuit (3D-IC)	Wafer Fab	Stacking of transistor layers Common interconnect stack on multiple layers of active devices Density level of local interconnects

Table 2.3: 3D interconnect technologies based on interconnect hierarchy [10].

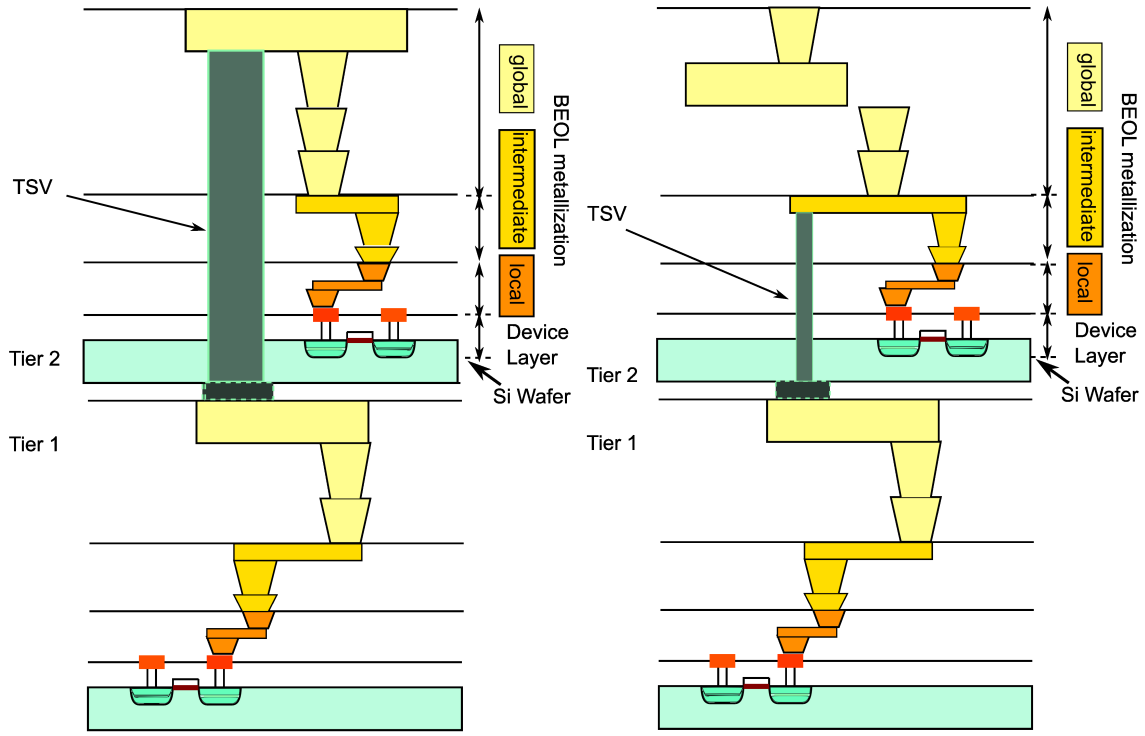
SOC integration i.e., to stack IP cores and achieves a very high TSV density. About 10K such fine-pitch TSVs (pitch of around 10 μm) can be formed on a Silicon area of 1 mm^2 compared to 2K ultra fine micro-bumps (pitch of around 20 μm) used in 3D-WLP.

Figure 2.2b illustrates the 3D Stacked IC (3D-SIC) technology which is a scaled down version of 3D-SOC. It is meant for stacking smaller circuit blocks (parts of IP cores) and has pitch requirements (around 2 μm) smaller than 3D-SOC.

At the lowest level in the chip hierarchy, 3D Integrated Circuit (3D-IC) involves an entirely different approach. In this, device layers are stacked, direct drain/source connections are implemented and is still in early stages of research. This taxonomy of 3D technology and the key features summarized in Table 2.3.

Of these stacking technologies, 3D-WLP, 3D-SOC and 3D-SIC are selected for this study. Each is of interest for solving the research problem of 3D interconnect performance estimation for high performance digital systems defined in Section 1.2. Also in contrast to the remaining two technologies i.e., 3D-P and 3D-IC, each employs TSVs for vertical interconnect formation and as noted in Section 2.1, extensive research and development has been carried out in 3D integration with TSVs.

ITRS has defined Roadmaps for TSVs [10] in relation to the interconnect hierarchy level served by them. The Roadmaps for 3D-WLP, 3D-SOC and 3D-SIC are provided in the Appendix (Tables A.1, A.2 and A.3) and are used as a guideline for TSV modeling in this work.



(a) Vertical channel in a 3D-SOC.

(b) Vertical channel in a 3D-SIC.

Figure 2.2: (a) TSV channel in a 3D System-On-Chip (3D-SOC) which is a global interconnect level stacking technology and (b) TSV channel in a 3D Stacked IC (3D-SIC) which is an intermediate interconnect level stacking technology.

2.3 Related Work

Work related to performance and cost estimation of 3D ICs falls into three broad categories, namely, system-level, architecture-level and physical-level. A system design methodology typically performs exploration by selecting different HW/SW IP blocks and communication blocks from high-level model libraries. During the literature study, the author has not found any work which utilizes a parameterizable electrical model of the 3D vertical interconnect for system-level design. The approach in this work is thus novel since no other work in system design which is exactly parallel is found. The work is inspired by the idea of bridging the gap between the works done at architecture-level and physical-level. Several architecture-level works propose 3D architectures utilizing the TSV-based interconnect which show a boost in the overall system performance compared to their 2D counterparts. However, these do not take into account the electrical performance and signal integrity of such a vertical interconnect which can be key issues as explained in the following discussion.

In [3], Li et al. propose a 3D Network-in-Memory architecture which employs a

communication pillar spanning a 3D stack having two schemes of implementation, namely, 2 layers and 4 layers. This communication pillar is composed of 178 high density TSVs (pitch less than 10 μm) which are placed in a closely packed bundle i.e., with minimum spacing of 5 μm between the TSVs. An improvement of 18% was reported in the performance metric Instructions Per Cycle (IPC) for the 3D architecture over its 2D counterpart. Along the same approach, a Cluster Mesh Inter-layer Topology (CMIT) for 3D stacked architectures is proposed in [25] where four routers share a vertical channel. The results show minimal performance penalty with 75% saving of the TSV area footprint achieved due to the sharing. The TSV bundle footprint is estimated for a TSV with a pitch of 8 μm and spacing of 3 μm between the TSVs. Both [3] and [25] assume a negligible delay through the TSV bundle and overlook the aspect of its signal integrity. Moreover, they calculate area overhead for the bundle with minimum pitch without accounting for a Keep-Out-Zone (KOZ) surrounding the TSV. However, KOZ is a critical *design constraint* as mechanical stress caused during TSV formation process can impact integrity of devices surrounding the TSV [26].

Several recent works on physical analysis and characterization of TSVs indicate that noise between TSVs due to capacitive coupling through the substrate cannot be neglected. In [27], a peak normalized noise voltage of 0.2 is reported on a victim TSV when spacing between two coupled TSVs is 5 μm. This is reported for a TSV height of 50 μm which typically connects 2 adjacent layers. The peak normalized noise voltage on a victim TSV reported for a 4 layer stack is greater than 0.5. Although the noise reported in the former case might be acceptable, the latter case implies that the switching point for the digital gates might be crossed leading to a logical error. It can be anticipated that the normalized noise voltage will be higher for a victim TSV surrounded by multiple aggressors in the bundle topology described earlier. This can potentially cause a degradation in the interconnect timing performance or in the worst case render it a functional failure.

In [28], Liu et al. perform a TSV-to-TSV noise analysis for a 45 nm 2-tier 3D IC which shows a significant impact on full chip timing performance and total noise voltage. The TSV is 4 μm in diameter and has a pitch of 10 μm which is in the same range as high density TSVs discussed in this Section. They present two effective ways to mitigate capacitive coupling induced noise, namely, buffer insertion and shielding TVSs with 8 ground TSVs. As noted in their work, additional buffers and ground TSVs to mitigate noise can result in appreciable increase in area penalty. This area penalty can be steep if a large number of shield TSVs are employed in order to keep the power consumption lower than when buffers are inserted. In their work, it is also pointed out that increasing the spacing is an inefficient solution to alleviate noise.

In conclusion, TSV-based interconnect topologies e.g., a bundle of closely spaced TSVs, have significant implications on the timing of the TSV interconnect and its signal integrity due to capacitive coupling noise. This in turn impacts the performance of the system which must be estimated upfront. Also, realistic area penalty incurred due to TSVs is higher as the KOZ for mechanical stress [26] and possible insertion of buffers or shield TSVs [28] must be taken into account. This indicates that the accuracy of performance and cost estimation for a 3D stack compared to its 2D counterpart in [3], [25] and other similar works can be improved.

2.4 Approach

In this work, the approach for realizing a more accurate 3D stack performance estimation is to estimate the electrical performance and area penalty incurred due to TSVs for the TSV vertical interconnect. Thus the technology dependant electrical characteristics of the vertical interconnect can dictate aspects of the communication architecture to be employed. Such an approach makes the design flow more inclined to be *first-time-right*.

This work aims to contribute towards a methodology for 3D stacked IC performance estimation. Use of parameterizable models that provide electrical characteristics enables the designer to change parameters to evaluate trends and limits in performance. Predictive technology models are expected to get validated as subsequent results from manufactured prototypes of 3D chips are published. The approach adopted in this methodology makes it easier to adjust well-structured technology parameters in design files that are read by the methodology.

Additionally, an idea of exploring vertical interconnect placement topologies is incorporated in the methodology which makes it capable of simulating multiple floorplans for a given system. In this work, fixed placement topologies e.g., a bundle of closely packed TSVs are explored as against solving a complex problem of fine-grained optimum placement. This is perceived as an efficient approach to judge benefits and costs of stacking at an early stage of system design when exact architectures are not known.

The TSV models and the generated electrical simulation results must be usable in a high-level simulation setup. SystemC is implemented in the form of C++ libraries and is meant for system-level modeling of timed or untimed models of hardware architectures. It provides for high speed simulation and these models can be easily integrated with other hardware/software IPs inside one simulation framework. The Analog Mixed Signal (AMS) extension of SystemC offers modeling formalisms which are useful for modeling circuit behavior. Of these, the Electrical Linear Network (ELN) offers predefined primitives such as resistors or capacitors, nodes, switches and sinks in order to describe the electrical linear networks. This can serve the objective of modeling electrical characteristics to estimate performance during system simulation and architecture exploration phase. The Discrete Event primitives (DE) can also be used effectively to generate voltage levels for given real valued data type such as *double* and vice versa. Besides ELN and DE primitives, some of the features of SystemC that are desirable for the modeling in this work are object-oriented programming that provides for parameterizability, abstraction, modularity and scalability.

3 Modeling

This chapter describes the analysis of the TSV model and the trends shown by the components of the model as a function of parameters. *Best Case* and *Worst Case* geometries for the TSV technologies re derived. It then presents the tier-to-tier path model and validates it. Lastly, it summarized the results and conclusions from the chapter.

3.1 2D Planar Interconnect

As described in Section 2.2, the 3 levels of stacking selected for this work are 3D-WLP, 3D-SOC and 3D-SIC. Of these, 3D-SOC and 3D-SIC are defined for global and intermediate interconnect level i.e., the TSV is connected through the substrate upto a metal layer in this interconnect level of a stacked die. A simple model consisting of lumped resistance R and capacitance C of the wire is considered sufficient for electrical modeling of the inter-tier path. For this, resistance per unit length R_l and capacitance per unit length C_l values for global and intermediate interconnect are required. These are computed from RC delay values given in Table 2.1 by using the relation in Equation (3.1).

$$\text{RC Delay} = (R_l \times l)(C_l \times l) \tag{3.1}$$

The resulting R_l and C_l values are summarized in the Table 3.1.

Year of Production	2010	2012	2015
Inferred Technology Node (nm)	45	32	22
Capacitance C_l ($fF/\mu m$) for global wire	0.20	0.20	0.19
Resistance R_l ($Ohm/\mu m$) for global wire	0.05	0.05	0.05
Capacitance C_l ($fF/\mu m$) for intermediate wire	0.20	0.18	0.17
Resistance R_l ($Ohm/\mu m$) for intermediate wire	9.46	24.60	75.59

Table 3.1: R_l and C_l of global and intermediate planar wires.

3.2 3D Vertical Interconnect

The metal filled TSVs are key technology enablers for the 3 levels of stacking considered for this work (Section 2.2). Motoyoshi [29] and Weerasekera et al. [19] describe the major steps in the TSV formation process. The deep holes etched through Silicon to form a TSV are filled with Copper (Cu) or Tungsten (W) and are surrounded

by a barrier layer and a dielectric liner. The dielectric liner (usually made of SiO2) provides electrical isolation from the substrate. The barrier layer is formed between the metal and the dielectric liner in order to prevent metal ions from migrating into the Si substrate which can degrade the device performance due to induced leakage. The TSV cross-section can be square or circular and can have a tapered cross-section along its length. However, invariably it is modeled as a uniform cylindrical structure [19, 18, 17, 24, 30].

3.2.1 3D-WLP Stacking

The vertical interconnect for 3D-WLP stacking technology requires modeling of TSV, bump and the Redistribution Layer (RDL) as described in Section 2.2. In [24], Kim et al. present a high frequency scalable electrical model with closed form RLGC equations. To validate the model, a test vehicle comprising of a stacked TSV channel with TSVs bumps and RDLs was fabricated. The measurements from the fabricated test vehicle and the proposed electrical model are well correlated up to 20 GHz. Also, a detailed time domain and frequency domain electrical characterization of the TSV channel has been presented in this work. The TSV model for 3D-WLP vertical interconnect channel is implemented as per [24].

3.2.1.1 RLC parameterized model

Kim et al. [24] model the resistance, inductance, capacitance, mutual inductance and coupling capacitance in the form of analytical equations for a pair of single ended TSVs connected to bumps as well as a pair of RDL wires. This work served as a broad study since many physical effects, for example substrate leakage are modeled. Moreover, the complex geometry of TSV, bumps and RDL uncover many parasitic capacitances. Since there are many parasitic components for the tier to tier vertical channel, only a few are summarized here.

Substrate leakage - For a typical substrate profile, a high resistivity epitaxial layer is formed on top of a bulk Silicon substrate. The switching activity in the TSVs is coupled to the conductive substrate through the oxide and depletion capacitance. Thus, it becomes important to consider modeling the parasitic component of substrate leakage. The substrate coupling used in the TSV model derived by Kim et al. comprises of parasitic components G_{Sisub} and C_{Sisub} as seen in Figure 3.1. This is a dynamic resistive-capacitive model which is presented and analyzed in [31]. For a given substrate, the time constant is given by σ/ϵ, the layer relaxation time or intrinsic time constant where σ is the conductivity while ϵ is the permittivity of the substrate. For a single layer substrate this model is accurate over all frequencies and has a cut-off frequency ω given by σ/ϵ.

As an example, for a typical high resistivity Silicon epitaxial layer, resistivity ρ is about 15 $\Omega.cm$ and ϵ_r for Silicon is 11.9. Conductivity σ equals $1/\rho$ and resulting value of cut-off frequency ω is 6.327 $Grad/s$ or approx. 1 GHz. For multiple layers σ for the high resistivity epitaxial layer dominates compared to the σ for low resistivity bulk substrate. The cut-off frequency for the low resistivity substrate (of the order of

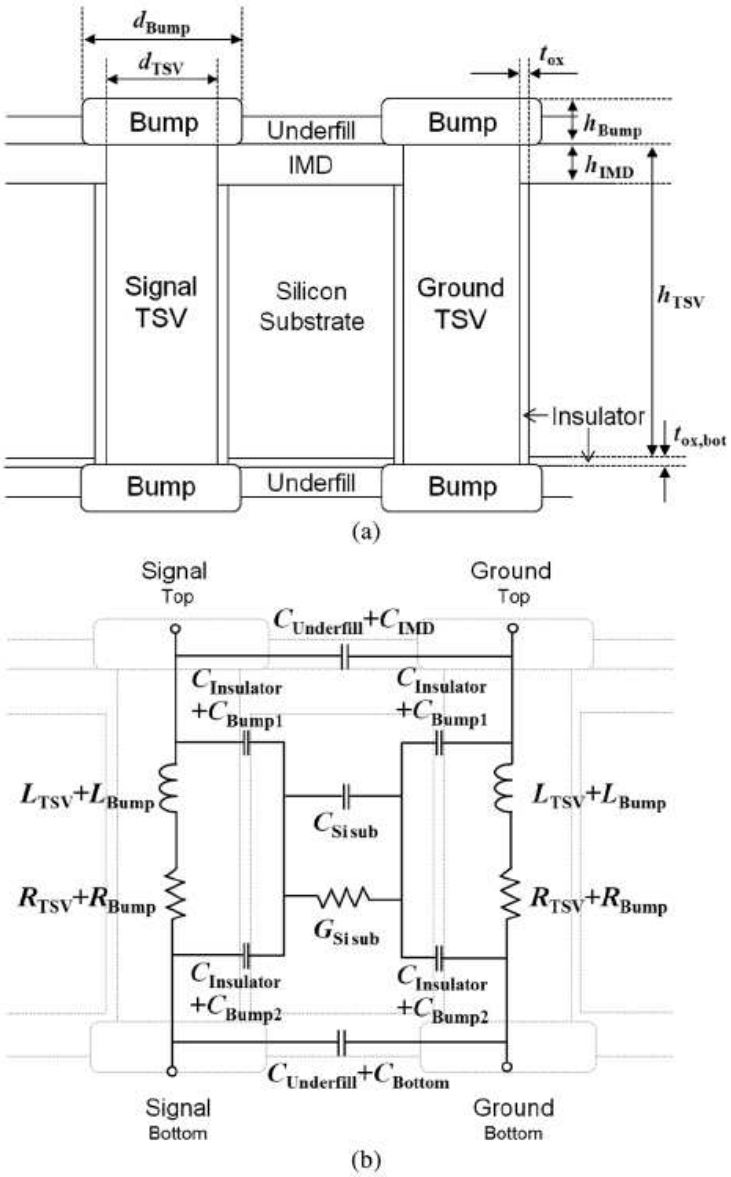


Figure 3.1: (a) Structure and parameters of a pair of single ended TSVs with bumps and (b) electrical model of the structure shown in (a) [24].

$m\Omega.cm$) is around 10^{12} rad/s or approx. 159 GHz. Thus the above model accurately represents the substrate coupling using a single time constant valid from DC to about 159 GHz.

Skin Effect - At high frequency (HF), the resistance of conductors increases due to the Skin Effect [32]. Since the application considered here is digital systems, the HF component of the signal is derived from the rise time (or fall time) of the clock and not the clock period. To accurately model the clock edge of a trapezoidal wave with rise time or fall time given by τ, the minimum frequency required is $f_{min} = 0.885/\tau$. A good rule of thumb for the frequency contained in the clock for digital circuits is

$f_{min} = 1/\tau$ [33] which will be used in this modeling work. For 3D-WLP modeling τ equal to 10 ps will be assumed as minimum clock edge width so that f_{min} of 100 GHz is within the accuracy limit for the substrate coupling model.

Depletion region capacitance - Another point to be noted with respect to physical effects is regarding capacitance of the TSV. Kim et al. model the capacitance due to dielectric layer ($C_{Insulator}$) but do not consider capacitance due to the depletion region formed in the p-type Silicon substrate [18, 30]. However, the model indicates a good match with fabricated test vehicle as presented in their work [24].

In order to achieve the goal of parameterizability of models, it is desirable to have closed form equations for resistance, inductance and capacitance as a function of-

1. TSV geometry - Diameter (d_{TSV}), pitch (p_{TSV}), height (h_{TSV}), height of metallization layers (h_{IMD}), dielectric layer thickness (t_{ox}) etc.
2. Bump geometry - Diameter (d_b), pitch (p_b), height (h_b) etc.
3. RDL geometry - Width (w_{RDL}), thickness (t_{RDL}), inter-RDL spacing (S_{RDL}) etc.
4. Material properties - Resistivity of TSV fill metal (ρ_{TSV}), Si substrate conductivity (σ_{Si}), Si substrate permittivity (ϵ_{Si}), TSV dielectric permittivity (ϵ_{ox}) etc.
5. Frequency - Clock edge rate $1/\tau$

From the point of view of implementing a vertical channel for performance estimation of 3D-WLP, there is added complexity of stacking heterogeneous dies of different sizes. Also, electrical modeling of the bump and the RDL along with their capacitive coupling requires more research regarding their individual technology parameters and guidelines. A basic TSV model for 3D-WLP is implemented and results are provided in Section B.1 in the Appendix. However, 3D-SOC/3D-SIC is given priority which further leads to applying the methodology to a 3D-router design to achieve the objective of performance estimation. As this work was time-bound, the 3D-WLP stacking granularity could not be implemented in the proposed methodology.

3.2.2 3D-SIC/3D-SOC Stacking

After study and analysis of recent works, [18, 17, 19] are found to provide closed form equations for TSV RLC parasitic components that include physical effects missing in prior work and are hence more accurate. A wide variation in TSV parasitic components values is observed which is briefly summarized as follows.

Resistance R_{TSV} - It varies between about 3 $m\Omega$ for DC to about 1 Ω for HF as a result of increased resistance due to Skin Effect.

Inductance L_{TSV} - It varies between approximately 8 pH to 40 pH due to TSV geometry.

Capacitance C_{TSV} - It varies between approximately 15 fF for high resistivity substrate (of the order of Ωcm) to 500 fF for low resistivity bulk substrates (of the order of $m\Omega cm$)

A brief analysis of the TSV models is follows.

Since Silicon-on-Insulator (SOI) technology has been adopted for high performance digital chips, TSV models for SOI will be considered and not for bulk Silicon technology. In SOI technology the substrate of the wafer is thinned down to a few μm. Thus, a TSV can have smaller diameter (D) due to shorter length (L) to abide by the constraints on aspect ratio ($A.R. = L/D$) laid down by process technology. Typically TSVs with diameter as small as 1-10 μm and length less than 50 μm can achieve the high density TSV interface discussed in Section 2.1. Weerasekera et al. [19] have presented TSV models for the diameter range of 40-80 μm which is in a higher range and hence not suitable. Moreover, they have assumed a fixed dielectric layer thickness in their work which limits its applicability.

Some early works consider capacitance of the TSV due to dielectric barrier (C_{ox}) but do not consider the depletion region formed in the p-type Silicon substrate and hence over-estimate C_{TSV} by as much as 25% to 60% [17]. Katti et al. [17] have derived the accumulation, depletion and minimum depletion capacitance (C_{depmin}). The resulting series combination of C_{TSV} and C_{depmin} is modeled as a capacitance to ground which is more accurate. However, their model does not account for leakage through substrate to ground.

Savidis and Friedman [18] have validated their TSV model in the diameter range of 1-100 μm which covers the requirement of SOI technology for this work. Also, the aspect ratio considered for simulation is in the range of 5:1 to 10:1 which is within guidelines projected by 3D-SOC and 3D-SIC Roadmaps given in Tables A.2 and A.3 in the Appendix. The depletion region capacitance is accounted for in the equation for C_{TSV}. Also, fitting parameters are included in the equations of C_{TSV} and R_{TSV} to account for distance from the ground plane and current leakage through substrate. For the above reasons, the TSV model for 3D-SIC/3D-SOC vertical interconnect channel is implemented using the equations derived by Savidis and Friedman [18].

3.2.2.1 RLC parameterized model

Similar to 3D-WLP, for 3D-SIC and 3D-SOC modeling $\tau = 10\ ps$ will be assumed as minimum clock edge width so that $f_{min} = 100\ GHz$ is within the accuracy limits. In order to achieve the goal of parameterizability of the models, it is desirable to have closed form equations for R_{TSV}, L_{TSV} and C_{TSV} as a function of -

1. TSV geometry - Diameter (D), pitch (P), length (L), dielectric layer thickness (t_{diel}), aspect ratio ($A.R.$), distance from ground plane (S_{gnd}) etc.
2. Material properties - Resistivity of TSV fill metal (ρ_m), Si substrate conductivity (σ_{Si}), Si substrate permittivity (ϵ_{sub}), dielectric permittivity (ϵ_{diel}), acceptor concentration of p-type doped substrate (N_A) etc.
3. Frequency - Clock edge rate $1/\tau$

The parasitic components with their parameters and characteristics are summarized in Table 3.2.

Parasitic Component	TSV Geometry	Material properties	Frequency	Comments	Equations (Appendix)
Resistance (R_{TSV})	D, L	ρ_m	$1/\tau$	for DC and for HF with Skin effect, fitting parameter for substrate loss	(B.14), (B.15)
Inductance (L_{TSV})	D, L			for DC and for HF, fitting parameters for non-linearity w.r.t $A.R.$	(B.18), (B.19)
Capacitance (C_{TSV})	D, L, t_{diel}, S_{gnd}	ϵ_{sub}, ϵ_{diel}, N_A		fitting parameters for non-linearity w.r.t. S_{gnd}	(B.22)
Mutual Inductance (L_m)	D, L, P			for DC and for HF, fitting parameters for non-linearity w.r.t $A.R.$ and P	(B.18), (B.19)
Coupling Capacitance (C_c)	D, L, P, S_{gnd}	ϵ_{sub}		fitting parameters for non-linearity w.r.t S_{gnd} and P	(B.27)

Table 3.2: TSV RLC parasitic components, the parameters they depend on, a few characteristics and equations for each.

3.2.2.2 TSV Model Trends

In order to observe the trend in parasitic components all parameters were swept and the significance of each is discussed below.

First a set of 6 geometries of TSV dimensions is drawn up based on Table A.2 in the Appendix. To start with, a **nominal** geometry is taken with D, P, $A.R.$ and L in the range for year 2009-2012. A twice **scaled** version of it is the 2nd set. A **thick** TSV is taken with $D = 8\ \mu m$ and a **thin** TSV with $D = 4\ \mu m$, both having the same length $L = 40\ \mu m$ that can typically connect two adjacent tiers. The pitch is always taken as $P = 2 \times D$ so as to calculate the worst case L_m and C_c. With $t_{diel} = 0.5\ \mu m$ and $t_{diel} = 1\ \mu m$, two sets of geometries are taken for thin and thick TSVs each. The 6 sets of TSV geometries are as given in Table 3.3.

The last remaining geometrical parameter is S_{gnd}. Ground can be assumed to be a backplane of a die thus giving $S_{gnd} = L$. Parasitic component values are computed as given in Table 3.4 for the 6 sets above with $S_{gnd} = L$, $\tau = 10\ ps$ and following material properties -
$\rho_m = 1.68 \times 10^{-8}\ \Omega.m$ for Cu TSV fill
$\epsilon_{sub} = 11.9 \times 8.85 \times 10^{-12}\ F/m$ for Si substrate

Dimensions	Scaled TSV		Thick TSV		Thin TSV	
	Nom	$2 \times Nom$	t_{diel}	$2 \times t_{diel}$	t_{diel}	$2 \times t_{diel}$
D (μm)	4	8	8	8	4	4
P (μm)	8	16	16	16	8	8
$A.R.$	5	10	5	5	10	10
L (μm)	20	80	40	40	40	40
t_{diel} (μm)	0.5	1	0.5	1	0.5	1

Table 3.3: A set of 6 TSV geometries considered for observing TSV RLC parasitic trends across geometrical parameters.

Component	Scaled TSV		Thick TSV		Thin TSV	
	Nom	$2 \times Nom$	t_{diel}	$2 \times t_{diel}$	t_{diel}	$2 \times t_{diel}$
R_{TSV} (Ω)	0.24	0.42	0.20	0.20	0.50	0.50
L_{TSV} (pH)	7.50	40.40	15.00	15.00	20.20	20.20
C_{TSV} (fF)	21.60	38.50	52.30	26.10	30.90	15.40
L_m (pH)	3.25	22.50	6.51	6.51	11.20	11.20
C_c (fF)	2.75	12.20	5.88	5.88	5.87	5.87

Table 3.4: Trend in TSV RLC parasitic components for a set of 6 TSV geometries.

$\epsilon_{diel} = 4 \times 8.85 \times 10^{-12}$ F/m for SiO2 substrate
$N_A = 1 \times 10^{21}$ $/m^3$ for a high resistive substrate

For a 3D stack a ground backplane for each layer is still not established [27]. A ground plane can be assumed as backplane of each die or one single ground plane at the backplane of lower most die. For a 3-tier stack, two cases can be derived assuming 50 μm as typical height for the TSV. One case with $S_{gnd} = L$ as minimum and second with $S_{gnd} = L + 150$ as maximum where ground plane is 3 tiers away. Parasitic component values are computed for the 6 sets of geometry at the 2 values of S_{gnd}. These are given in the Table 3.5. The trend shows that as distance from ground increases the C_{TSV} decreases by about 20% while the coupling capacitance C_c increases by about 20%. This implies that an assumption about a ground plane is critical especially as the stack grows and if the ground plane is several tiers away.

S_{gnd} (μm)	$Component$	Scaled TSV		Thick TSV		Thin TSV	
		Nom	$2 \times Nom$	t_{diel}	$2 \times t_{diel}$	t_{diel}	$2 \times t_{diel}$
L	C_{TSV} (fF)	21.60	38.50	52.30	26.10	30.90	15.40
	C_c (fF)	2.75	12.20	5.88	5.88	5.87	5.87
$L + 150$	C_{TSV} (fF)	15.80	35.00	41.80	20.90	26.90	13.40
	C_c (fF)	3.33	12.80	6.73	6.73	6.38	6.38

Table 3.5: Trend in TSV RLC parasitic components w.r.t. S_{gnd}.

Since a two-tier model is presented, this design consideration is not significant as the difference in C_{TSV} and C_c for the cases of $S_{gnd} = L$ μm and $S_{gnd} = 2L$ μm is less than 6%. In order to implement the TSV model for a pessimistic value of C_{TSV}, an assumption of $S_{gnd} = L$ μm is made and is maintained as a fixed parameter.

With regard to observing the trends in the parasitic components as a function of material properties no other materials are taken for substrate and dielectric layer except the typical Si and SiO2 as mentioned above. The trend with respect to doping concentration can be observed by taking a second value of $N_A = 10^{22}$ $/m^3$ which makes the Si substrate less resistive. A decrease in C_{TSV} between 7% to 16% is observed as seen in Table 3.6.

N_A $(/m^3)$	$Component$	Scaled TSV		Thick TSV		Thin TSV	
		Nom	$2 \times Nom$	t_{diel}	$2 \times t_{diel}$	t_{diel}	$2 \times t_{diel}$
1×10^{21}	C_{TSV} (fF)	21.60	38.50	52.30	26.10	30.90	15.40
1×10^{22}	C_{TSV} (fF)	18.00	36.90	46.50	23.20	28.70	14.30

Table 3.6: Trend in TSV RLC parasitic components w.r.t. N_A.

Although this a significant decrease in C_{TSV}, the assumption is made to account for the pessimistic case of C_{TSV}. Hence $N_A = 10^{21}$ $/m^3$ is carried forward and maintained as a fixed parameter.

With respect to an alternative TSV fill material, Tungsten (W) is considered with $\rho_m = 58.8 \times 10^{-}9\ \Omega.m$. For observing the trend in value of R_{TSV} because of Skin Effect, $\tau = 100$ ps is the second parameter to be considered. Skin depth is a function of both $f = 1/\tau$ and $\sigma_m = 1/\rho_m$ and R_{TSV} is a function of skin depth. As shown in Table 3.7, the maximum value of R_{TSV} caused by varying these two parameters is 15 times the minimum value of R_{TSV}. However, all values of R_{TSV} are under 1 Ω and hence are not a significant component in the electrical model of the path which is explained next.

Hence $\rho_m = 1.68 \times 10^{-8}\ \Omega.m$ for Cu TSV fill and $\tau = 10$ ps are maintained as fixed parameters.

The RLC model proposed by Savidis and Friedman [18] demonstrates fairly good accuracy for R_{TSV}, L_{TSV} and C_{TSV} compared to Ansoft Quick 3-D an electromagnetic field solver. The accuracy of each parasitic component with respect to signal frequency and its implication on the overall performance estimation of the 3D interconnect is

ρ_m ($\Omega.m$)	τ (ps)	$Component$	Scaled TSV		Thick TSV		Thin TSV	
			Nom	$2 \times Nom$	t_{diel}	$2 \times t_{diel}$	t_{diel}	$2 \times t_{diel}$
$1.68 \times 10^{-8}(Cu)$	10	R_{TSV} (Ω)	0.24	0.42	0.20	0.20	0.50	0.50
$5.88 \times 10^{-}8(W)$	10	R_{TSV} (Ω)	0.48	0.81	0.39	0.39	0.99	0.99
$1.68 \times 10^{-8}(Cu)$	100	R_{TSV} (Ω)	0.08	0.14	0.06	0.06	0.18	0.18

Table 3.7: Trend in TSV RLC parasitic components w.r.t. ρ_m and τ.

discussed below.

Resistance (R_{TSV}) - Results of [18] indicate less than 5% error for all frequencies between DC and 10 GHz after accounting for Skin Effect. Extrapolation of the linear graph gives maximum 18% error at 100 GHz. The maximum R_{TSV} value computed by sweeping parameters is 1 Ω which is comparable to the resistance of a global wire of length 20 μm. However, it is at least 2 to 3 orders smaller than the ON resistance of the CMOS gate R_{dr} (typically of the order of 10^2 to 10^3 Ω). We are interested in calculating the vertical interconnect path delay and the path includes the CMOS driver gate. Thus, as R_{dr} is in series with R_{TSV}, R_{TSV} is not a significant parasitic component in the path model and an 18% error in it does not impact path model accuracy.

Inductance (L_{TSV}) - Results of [18] indicate less than 8% error for DC as well as HF (greater than 800 MHz). The L_{TSV} value observed in Table 3.4 is upto 40 pH. At 100 GHz frequency, the impedance ωL_{TSV} is at least one or two orders smaller than R_{dr}. This implies that 8% error in the parasitic Inductance in the overall tier-to-tier path circuit can be ignored.

Capacitance (C_{TSV}) - Results of [18] indicate less than 8% error over all frequencies. C_{TSV} is the most dominant parasitic component of the TSV in the tier-to-tier path circuit. The impact of this error on performance estimation of 3D interconnect is evaluated in Section 3.3.2.

Mutual Inductance (L_m) - Results of [18] indicate less than 8% error for aspect ratio in the range of 5:1 to 10:1 for DC as well as HF (greater than 800 MHz). However, parasitic Mutual Inductance can also be ignored similar to L_{TSV}.

Coupling Capacitance (C_c) - Results of [18] indicate less than 8% error for aspect ratio in the range of 5:1 to 10:1 for equal length vias over all frequencies. In this work only equal length vias will be considered for inter-tier modeling.

3.2.2.3 TSV Technology Corner Cases

The TSV electrical model is simulated in a circuit of a vertical interconnect channel to judge its impact on performance and to derive corner cases of TSV technology based on best and worst performance.

For an initial simulation, a driver resistance of 50 Ω is connected in series with a T-model of the TSV comprising of self parasitic components R_{TSV}, L_{TSV} and C_{TSV}. TSV

RLC T-model is terminated with a load capacitance of 20 fF which is the capacitance of a 100 μm long global wire. A step signal with a rise time of 10 ps is applied to the driver resistance. The 50% Propagation Delay and 10%-90% slew of the signal through the TSV is given in the Table 3.8.

Component	Scaled TSV		Thick TSV		Thin TSV	
	Nom	$2 \times Nom$	t_{diel}	$2 \times t_{diel}$	t_{diel}	$2 \times t_{diel}$
R_{TSV} (Ω)	0.24	0.42	0.20	0.20	0.50	0.50
L_{TSV} (pH)	7.50	40.40	15.00	15.00	20.20	20.20
C_{TSV} (fF)	21.60	38.50	52.30	26.10	30.90	15.40
50% Delay (ps)	3	3	4	3	3	2
10%-90% Slew (ps)	9	9	11	9	10	8

Table 3.8: Initial estimates of delay and slew through a TSV for the set of 6 TSV Geometries. Thin TSV with $2 \times t_{diel}$ is chosen as Best Case geometry for minimum delay i.e., 2 ps. Thick TSV with t_{diel} is chosen as Worst Case geometry for maximum delay i.e., 4 ps.

It is observed that a maximum delay of 4 ps is obtained for a thick TSV with thin dielectric layer while a minimum delay of 2 ps is obtained for a thin TSV with thick dielectric layer. However, R_{TSV} shows opposite trend for these two geometries. This indicates that C_{TSV} is dominant in the RC delay through the path compared to R_{TSV}. This is also explained earlier in this Section when accuracy is discussed. The *Best Case* geometry and *Worst Case* geometry chosen for the two TSV technologies explored in this work correspond to minimum delay and maximum delay respectively. Since 3D-SIC is a scaled down version of 3D-SOC, the analysis leads to similar results. The Best Case and Worst Case TSV technology corners are summarized in Table 3.9.

Dimension	3D-SOC		3D-SIC	
	BC	WC	BC	WC
D (μm)	4	8	1	2
P (μm)	8	16	2	4
$A.R.$	10	5	10	5
L (μm)	40	40	10	10
t_{diel} (μm)	1	0.5	1	0.5

Table 3.9: *Best Case* (BC) and *Worst Case* (WC) geometries for 3D-SOC (Global level stacking) and 3D-SIC (Intermediate level stacking) TSV technologies corresponding to the minimum and maximum delay through the TSV respectively.

3.3 TSV-based Tier-To-Tier Path

The communication from a device in one tier to a device in another tier is modeled using parasitic components of the devices in the two tiers and the interconnect between them which traverses horizontal and vertical paths. In this Section, a tier-to-tier channel model is presented and validated.

3.3.1 Modeling

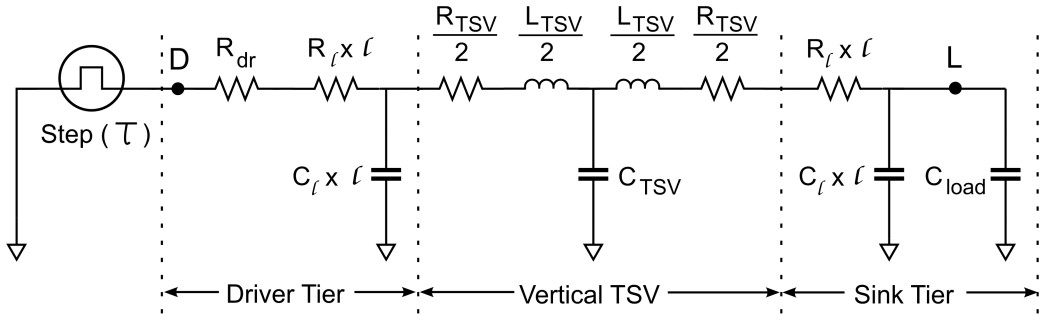


Figure 3.2: Model of tier-to-tier vertical channel which is implemented to simulate electrical performance of 3D 2-tier interconnect.

An electrical circuit representing a tier-to-tier path is shown in Figure 3.2. The digital signal input to this path is a step voltage with an edge rate of $1/\tau$. The driver gate on one tier is represented using its equivalent ON resistance R_{dr}. On the other tier, the gate capacitance of the sink gate is modeled as the load capacitance C_{load}. The RC model for horizontal wire as per Section 3.1 is connected in series on either end of the electrical RLC model of the TSV given in Section 3.2.2.1. The length of the wire is the Manhattan distance between the TSV location and gate location. Driver and load gates are typically buffers which are used to strengthen the signal and are conventionally designed as a chain of two inverters.

R_{TSV} and L_{TSV} parasitic components can be ignored as inferred in Section 3.2.2.2 and the circuit thus gets simplified. Since the path is now a network of lumped resistance and capacitance components, the 50% propagation delay of the path can be calculated. The Elmore delay model gives a good estimation of the first order RC time constant of the network from source node D (input of driver) to sink node L (input of the load) [32]. The Elmore delay for the model is given by Equation (3.2) where the RC parasitic components of horizontal wires in driver tier and tier with loading gate are indicated by subscripts d and l.

$$t_p = 0.69 \times \{(R_{dr} + R_d) \times (C_d + C_{TSV}) + (R_{dr} + R_d + R_l) \times (C_l + C_{load})\} \quad (3.2)$$

The device models referred for this work are available on the website of Predictive Technology Models [34] for 45 nm and 32 nm technology nodes. The version used here is High-k/ Metal Gate CMOS BSIM4 Models for High Performance Applications. These

Technology Node (nm)	45	32
Nominal Vdd (V)	1.0	0.9
Thickness of gate oxide t_{ox} (nm)	1.25	1.15
Effective length L (nm)	45	32
Gate-to-source overlap capacitance per unit width C_{gso} (F/m)	1.1e-10	8.5e-11
Gate-to-drain overlap capacitance per unit width C_{gdo} (F/m)	1.1e-10	8.5e-11
Relative permittivity of gate oxide ϵ_r	3.9	3.9

Table 3.10: Parameters from BSIM4 MOSFET models for 45 nm and 32 nm technology nodes [34] which are used for computation of parasitic components for circuit simulation.

models and the parameters within are used for computation and circuit simulation to estimate R_{dr} and C_{load} as follows.

3.3.1.1 Estimation of C_{load}

A load buffer for the D to L path is considered to have a minimum sized i.e., 1x CMOS Inverter as the first inverter in the chain. MOSFET gate capacitance C_g can be divided into intrinsic and extrinsic components [32]. The intrinsic capacitance, also called the gate-channel capacitance is contributed by the channel charge and is modeled using capacitance due to the gate oxide per unit area C_{ox}. The extrinsic capacitance is caused due to lateral diffusion of drain and source under the gate. It is also termed overlap capacitance as it is formed due to gate to source overlap C_{gso} and gate to drain overlap C_{gdo}. Assumption for NMOS is $W = L$ and for PMOS is $W = 1.5 \times L$ Relevant MOSFET transistor parameters used to calculate C_{load} are summarized in Table 3.10. The equations for these capacitances are given in (3.3)-(3.7).

$$C_{ox} = \epsilon_r \epsilon_0 / t_{ox} \tag{3.3}$$

$$C_g(intrinsic) = C_{ox} W L \tag{3.4}$$

$$C_g(extrinsic) = C_{gso} W + C_{gdo} W \tag{3.5}$$

$$C_g = C_g(intrinsic) + C_g(extrinsic) \tag{3.6}$$

$$C_{load} = C_g(NMOS) + C_g(PMOS) \tag{3.7}$$

The calculated values of MOSFET gate capacitances and C_{load} for 1x Inverter in 45 (nm) and 32 (nm) technology nodes are summarized in Table 3.11.

	45(nm)		32(nm)	
	NMOS	PMOS	NMOS	PMOS
Oxide capacitance per unit area C_{ox} (F)	0.0276	0.0276	0.0300	0.0300
Gate-channel capacitance $C_g(intrinsic)$ (fF)	0.056	0.134	0.031	0.074
Overlap capacitance $C_g(extrinsic)$ (fF)	0.010	0.024	0.005	0.013
Total gate capacitance C_g (fF)	0.066	0.158	0.036	0.087
Inverter gate capacitance C_{load} (fF)	0.224		0.123	

Table 3.11: C_{load} for 1x Inverter in 45 nm and 32 nm technology nodes.

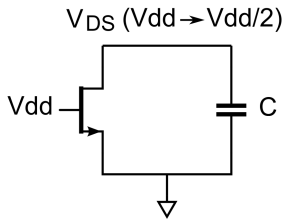


Figure 3.3: Circuit for measuring ON resistance of NMOS transistor.

3.3.1.2 Estimation of R_{dr}

A driver buffer for the D to L path is estimated looking at the capacitive load it is driving. The average of Best Case and Worst Case C_{TSV} is about 35 fF. By applying the FO4 rule of thumb, a 40x Inverter in 45 nm technology which has a gate capacitance of about 9 fF can optimally drive a load four times it's own gate capacitance i.e., 36 fF. The additional capacitance loading due to horizontal wire is not taken into account here so as to avoid over-designing. The final objective is to evaluate the performance of the vertical interconnect. Thus, by designing to drive the C_{TSV} optimally, a dominant horizontal wiring component should be clearly visible in the simulation results. Hence a 40x Inverter as a last inverter in the chain for a driver is considered reasonable.

For modeling a CMOS inverter as a driver, the average equivalent ON resistance $R_{ON_{eq}}$ needs to be derived for discharging a capacitor from Vdd to ground through NMOS transistor and charging a capacitor from 0 to Vdd through a PMOS transistor. For the case of NMOS discharging a capacitor, NMOS gate is connected to Vdd and Vds is swept with a load capacitor connected between the drain and source. The circuit is shown in Figure 3.3. The average value of the resistances at the points Vdd and Vdd/2 gives the ON resistance of the NMOS R_{ON_n} [32]. Similarly, the equivalent ON resistance of the PMOS R_{ON_p} is calculated by taking average value of the resistances at the points 0 and Vdd/2. Assumption for NMOS is $W = 40 \times L$ and for PMOS is $W = 40 \times 1.5 \times L$ where 1.5 is a factor used to make drain currents of both NMOS and PMOS approximately equal. Circuit simulations to calculate R_{ON_n} and R_{ON_p} were carried out in Cadence Spectre. The equivalent ON resistance R_{dr} of the driver gate is

given by

$$R_{dr} = R_{ON_{eq}} = \frac{R_{ON_n} + R_{ON_p}}{2} \tag{3.8}$$

The simulation results and estimated values of R_{dr} for 40x Inverter in 45 nm and 32 nm technology nodes are summarized in Table 3.12.

	45 nm		32 nm	
	NMOS	PMOS	NMOS	PMOS
ON resistance of MOSFET R_{ON} (Ω)	333	320	377	363
ON resistance of driver gate R_{dr} (Ω)	327		370	

Table 3.12: R_{dr} for 40x Inverter in 45 nm and 32 nm technology nodes.

3.3.2 Validation

To validate the tier-to-tier path model, a sample D to L path circuit shown in Figure 3.4 is simulated in Cadence Spectre and the results are compared with the simulation results of the equivalent parasitic RC circuit shown in Figure 3.5. Also, the impact of 8% error in C_{TSV} on the 50% delay t_p from D to L is evaluated.

In circuit of Figure 3.4, 40x and 1x inverters are built using PTM CMOS model for 45 nm technology. A step signal is given to the input of the 40x inverter while the 1x inverter is terminated with a capacitive load of $C_t = 0.4\ fF$. The wire connecting the output of the 40x driver and input of the 1x load is assumed to be a global wire of length 200 μm with $R_l = 0.5\ \Omega/\mu m$ and $C_l = 2 \times 10^{-16}\ F/\mu m$ (see Table 3.1). The component values of the wire RC model are,

$R_w = .05 \times 200 = 10\ \Omega$
$C_w = 2 \times 10^{-16} \times 200 = 4 \times 10^{-14} = 40\ fF$

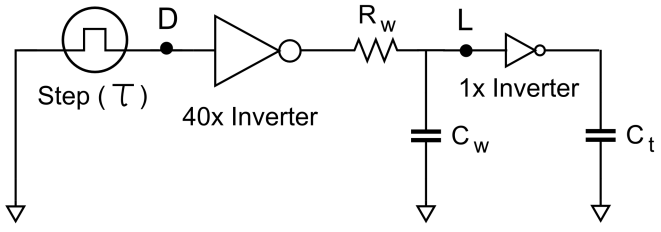


Figure 3.4: D to L path circuit using inverters.

The equivalent RC circuit for the D to L path which is composed of parasitic components is shown in Figure 3.5. The circuit is similar to tier-to-tier path shown in Figure 3.2 without including the TSV RLC Model. The 40x driver inverter in 45 nm technology is replaced by its ON resistance R_{dr} (Table 3.12) while 1x load inverter in 45

nm technology is replaced by its gate capacitance C_g (Table 3.11). These components are shown in Figure 3.5 as R_{dr} and C_{load} respectively. The input step signal and RC wire model are the same as in the circuit with inverters. This equivalent RC circuit is simulated in Cadence Spectre as well as in SystemC-AMS environment.

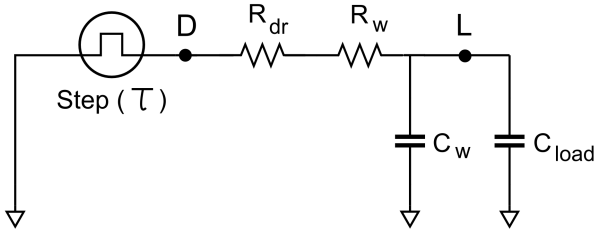


Figure 3.5: D to L path equivalent circuit using parasitic RC components.

The 50% delay t_p from D to L is measured in each of the above simulations. The analytical value of t_p is also determined using the Elmore Delay Model [32] which is given by Equation (3.9). The value of t_p is 10 ps for the equivalent RC circuit simulated in Spectre and SystemC-AMS which matches exactly with Elmore Delay. The value of t_p is 12 ps for the Spectre simulation with inverters.

$$t_p = 0.69 \times \{(R_{ON} + R_w) \times C_w + (R_{ON} + R_w) \times C_{load}\} \tag{3.9}$$

A second case is simulated where the average C_{TSV} of 35 fF is added to the value of C_w since the two parasitic capacitances are in parallel in the path circuit. The results shown in Figure 3.6 are a t_p of 18 ps for equivalent RC circuit and 20 ps for actual circuit with inverters. Thus the equivalent RC circuit results in a less pessimistic path delay t_p. It is about 83% to 90% accurate compared to actual circuit simulation and exhibits more accuracy as total wire capacitance increases.

For 1st order analysis of digital circuits, it is considered acceptable to have an error of approximately 10 % [32]. This validates the equivalent RC circuit of Figure 3.5 and hence validates the tier-to-tier path model shown in Figure 3.2 which is used for implementing the proposed exploration methodology.

In order to evaluate the impact of error $\delta C_{TSV} = 8\%$ on path delay t_p, we start with Elmore delay given in Equation 3.2. The error in path delay δt_p is then deduced as follows.

$$\delta t_p = \frac{(R_{dr} + R_d) \times (C_d + \delta C_{TSV})}{(R_{dr} + R_d) \times (C_d + C_{TSV}) + (R_{dr} + R_d + R_l) \times (C_l + C_{load})}$$

For maximum impact of δC_{TSV} the denominator must be made minimum. Assuming least values of R_l and C_l equal zero implying no wiring in sink tier and neglecting C_{load} we get,

$$\delta t_p = \frac{C_d + \delta C_{TSV}}{C_d + C_{TSV}}$$

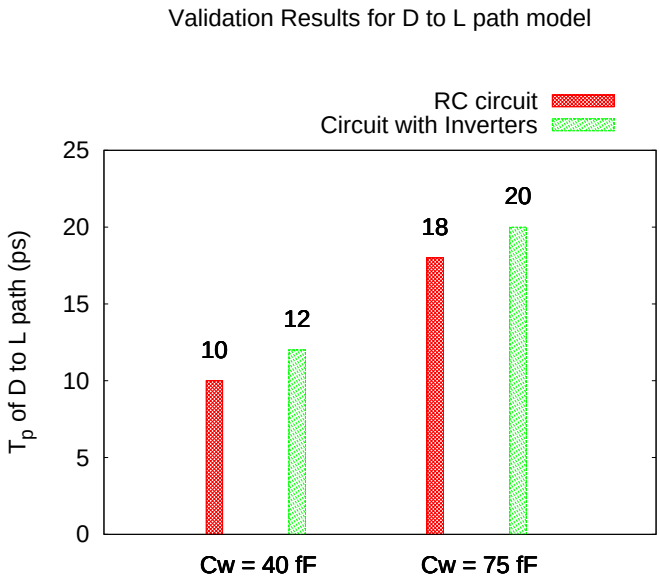


Figure 3.6: Validation results for D to L path model. The accuracy of parasitic RC circuit compared to actual circuit is 83% and 90% for C_w of 40 fF and 75 fF respectively.

The maximum value of δt_p will result when C_d is minimum which can be assumed equal to zero implying no wiring in driving tier. Thus, the maximum percentage error in path delay t_p is equal to percentage error in C_{TSV} i.e., 8%.

3.4 Conclusions

- TSV RLC model for 3D-SIC/3D-SOC vertical interconnect channel is implemented using the model proposed by Savidis and Friedman [18] as it matches closely with the dimension and parameterizability requirements.

- Best Case and Worst Case TSV geometries are derived corresponding to minimum and maximum delay through the TSV and are given in Table 3.9. Other TSV model parameters which do not have a significant influence are kept fixed and are listed below.

  $S_{gnd} = L$ for two-tier model

  $\tau = 10\ ps$ for edge rate of clock

  $\rho_m = 1.68 \times 10^{-8}\ \Omega.m$ for Cu TSV fill

  $\epsilon_{sub} = 11.9 \times 8.85 \times 10^{-12}\ F/m$ for Si substrate

  $\epsilon_{diel} = 4 \times 8.85 \times 10^{-12}\ F/m$ for SiO2 dielectric liner

  $N_A = 1 \times 10^{21}\ /m^3$ for a high resistive substrate

- Tier-to-tier vertical path model shown in Figure 3.2 is presented comprising of the following RLC parasitic component values.

  R_{dr} which represents the 40x Inverter driver gate given in Table 3.12

  RC which models planar wires in both tiers given in Table 3.1

  TSV RLC which is the TSV model as given in Table 3.2

  C_{load} which represents 1x Inverter loading gate given in Table 3.11

  $Step$ to model input voltage source as a function of rise time

- Tier-to-tier vertical path model is validated through actual circuit simulation with inverters. A wide accuracy range (83% to 90% shown in Figure 3.6) is observed depending on the capacitive wire load. For 1st order analysis of digital circuits, it is considered acceptable to have an error of approximately 10 %. This validates the tier-to-tier path model shown in Figure 3.2

- Of all parasitic components, the accuracy of C_{TSV} is significant as it is dominant in the vertical path model. The maximum percentage error in path delay t_p due to C_{TSV} is equal to percentage error in C_{TSV} i.e., 8%.

- TSV model for 3D-WLP as presented in [24] was implemented but as this work was time-bound, the 3D-WLP stacking granularity could not be implemented in the proposed methodology.

4 3D-SOC/3D-SIC Methodology

In this chapter, a methodology is proposed for the exploration of interconnect architectures for a 2-tier 3D-SOC/3D-SIC for CMOS circuit technology. The methodology uses the tier-to-tier path model presented in Section 3.3 to estimate delay, slew and cross-talk due to capacitive coupling for vertical interconnect paths. Cost is estimated in terms of Silicon area occupied by TSVs and vertical interconnect capacitance which contributes to dynamic power of the chip.

Exploration of the following aspects is carried out in the proposed methodology:

TSV technology - The TSV technology is explored for two corners i.e., Best Case (BC) and Worst Case (WC) geometries which are given in Table 3.9. The stacking granularity i.e., Global or Intermediate level must be provided as an input to the methodology which implies the selection between 3D-SOC and 3D-SIC respectively.

Planar circuit and interconnect technology - In order to estimate the electrical performance it is required to take into account the parasitic components of the planar technology. The technology nodes explored are 45 nm and 32 nm. Tables 3.1, 3.11 and 3.12 give the parasitic components for planar circuit and interconnect technology.

TSV placement topologies - Several TSV placement topologies have been experimented with and their comparison is provided. Four of these are chosen for implementation in the exploration methodology. They are discussed during the course of this chapter.

4.1 TSV Placement Topologies

4.1.1 Capacitive Coupling

The switching activity of signal TSVs can be capacitively coupled through the Silicon substrate to other signal TSVs in their proximity which is termed cross-talk. Closely packed TSVs have a higher coupling capacitance between them since it is inversely proportional to the TSV spacing (see Equation (B.27)). The switching of aggressor TSVs in a cluster impacts the signal integrity of a victim TSV to a larger extent than when the TSVs are distributed and widely spaced. When deciding on a placement topology, it is a better practice to verify through simulation that the impact of cross-talk on signal integrity does not affect the functionality of the design.

The circuit for simulating the capacitive coupling between two TSVs is shown in Figure 4.1(a). The RLC T-model of the Best Case (or Worst Case) TSV geometry is

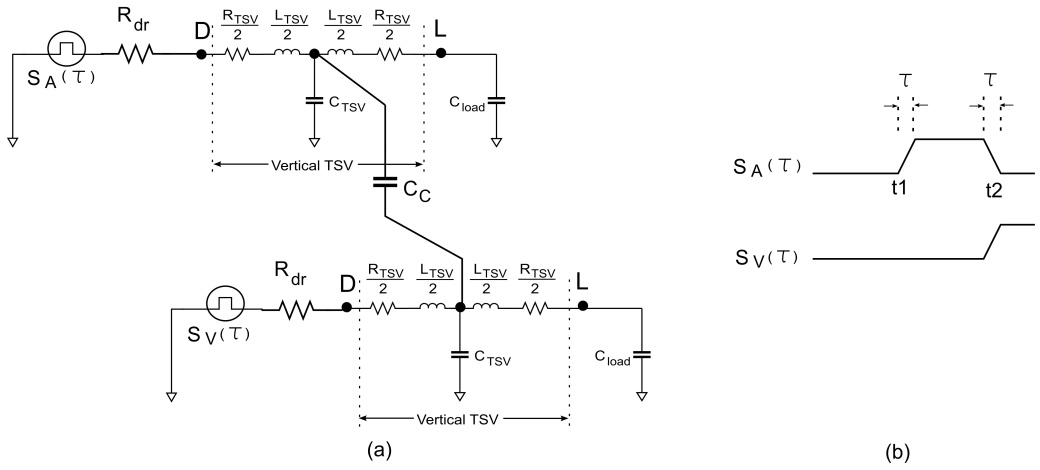


Figure 4.1: (a) Circuit for simulating capacitively coupled TSVs and (b) Input waveforms $S_A(\tau)$ and $S_V(\tau)$ for the aggressor and victim TSVs respectively.

used for simulating the capacitive coupling for the Best Case (or Worst Case) as per Table 3.8. Both aggressor and victim TSVs are driven by a 40x Inverter at node D and are loaded with a 1x Inverter at node L as shown in Figure 4.1(a). The ON resistance of the driver Inverter R_{dr} and the gate capacitance of the loading Inverter C_{load} are technology dependant. These are estimated for the 45 nm and 32 nm nodes and are given in Tables 3.12 and 3.11. The waveforms $S_A(\tau)$ and $S_V(\tau)$ are given at the input of the aggressor and victim TSVs respectively as shown in Figure 4.1(a). The rise/fall time τ of the edge taken as 10 ps which is maintained the same as the step input assumed in the TSV modeling in Section 3.2.2.1. The horizontal wires in the tiers are not considered for the estimation of capacitive cross-talk.

The 50% propagation delay in the vertical path is affected due to the capacitive coupling between two TSVs and can lead to timing issues. In addition to transient timing of a signal, the voltage level of a silent line can change because of capacitive coupling induced noise which could be large enough to cause functional failure. In order to cover these tests for functionality, the following cross-talk parameters are estimated through simulation.

1. The capacitive coupling induced noise voltage on a silent line due to switching of all aggressors is estimated. After time t1 of the input waveform shown in Figure 4.1(b), the peak change in voltage at output node L of the victim TSV is measured. This gives the worst case noise due to capacitive coupling.

2. Increase in delay that is seen when all aggressor TSVs switch simultaneously in a direction opposite to the signal in the victim TSV is estimated. This occurs at time t2 of the input waveform shown in Figure 4.1(b). The delay is measured from D to L of the victim TSV. This gives worst case delay due to capacitive coupling. The delay from D to L for a de-coupled TSV for the same values of the RLC TSV model, R_{dr}, C_{load} and τ is also simulated. The difference in the two delays gives the worst case increase in delay due to capacitive coupling.

For estimating the above worst case cross-talk parameters, only immediate neighbours are considered for simulating the impact of capacitive coupling. For TSVs placed in a bundle, the capacitive cross-talk due to immediate neighbours is more significant than that due to non-adjacent TSVs as shown in [19]. A 3x3 matrix similar to [19] is used as a representative structure for simulating cross-talk in a bundle topology. Thus the impact of 8 aggressors on the victim TSV at the centre of the bundle is estimated. In case of TSVs placed in a single row, the adjacent TSVs on both sides are considered as aggressors.

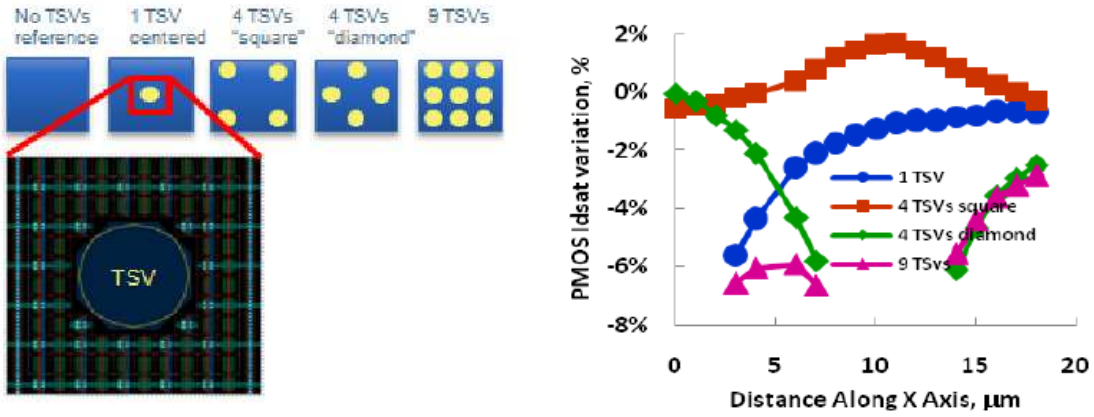
4.1.2 TSV Keep-Out-Zone

Besides signal integrity, placement and proximity of TSVs also impacts integrity of devices and interconnects due to thermal and mechanical effects depending on material properties. Mechanical stress is induced during the processes involved in TSV formation due to the mismatch in Coefficient of Thermal Expansion (CTE) of Copper and surrounding Silicon. Copper contracts faster and pulls the surface of Silicon surrounding the TSV causing tensile stress. Mercha et al. [26] have performed an analysis of the impact of thermo-mechanical stress on carrier mobility and performance of adjacent devices. The TSVs were etched using a Bosch process in a 300 mm High-k/ Metal Gate First CMOS via middle process, details of which can be found in [26].

For the design of digital 3D ICs, the Keep-Out Zone (KOZ) has been defined as the area around a TSV where the change in saturation current $\Delta Idsat$ for MOSFETs is greater than 5%. Digital FETs must be placed outside this KOZ in order to maintain device functionality. Also as pointed out in [26], TSV-induced $Idsat$ variation is always more for PMOS than for NMOS transistors. For TSVs arranged in a row or a matrix topology the stress components add up propagating to larger distances into the surrounding Silicon. For a 0.5 μm PMOS FET and a TSV with diameter D equal to 5 μm, the KOZ increases from 6 μm for a single TSV to 20 μm for a large matrix of TSVs.

KOZ guidelines used in this work are inferred from Figure 4.2 [26] which shows the impact of TSVs on 40 nm PMOS FETs for different TSV placement structures. 40 nm FET can be considered close to 45 nm and 32 nm technology nodes and so the guidelines for the exploration in this methodology are reasonably reliable. The TSVs fabricated by Mercha et al. [26] had a length equal to 40 μm, diameter equal to 5.2 μm and a thickness of the dielectric liner equal to 0.2 μm. These are reasonably suited for Global level stacking as they are in the same dimension range but are not suited for Intermediate level stacking where TSVs have smaller dimensions i.e., diameter of 1-2 μm and length of 10 μm (Table 3.9). However, due to the limited number of studies for very high density vias, tentatively the KOZ dimensions are scaled down by a factor of 4 to match the TSV scaling.

The KOZ guidelines are estimated from the plot in Figure 4.2 by performing interpolation and addition of $\Delta Idsat$ variation. The KOZ is measured as an area around the TSV until the point where the aggregate $\Delta Idsat$ is approximately 5%. The guidelines are as follows.



(a) (b)

Figure 4.2: (a) An array of digital 40 nm FETs with various TSV placement structures and (b) The effect of TSV proximity on $\Delta Idsat$ variation wherein X-axis originates at the centre of each TSV placement structure shown in (a).[26]

1. The plot for diamond shows that $\Delta Idsat = 0\%$ at the centre of the structure. Thus $\Delta Idsat$ is equal in magnitude but opposite in sign when the TSV is placed perpendicular or parallel to the direction of drain current in the PMOS. Thus KOZ is equal along both axes of the TSV.

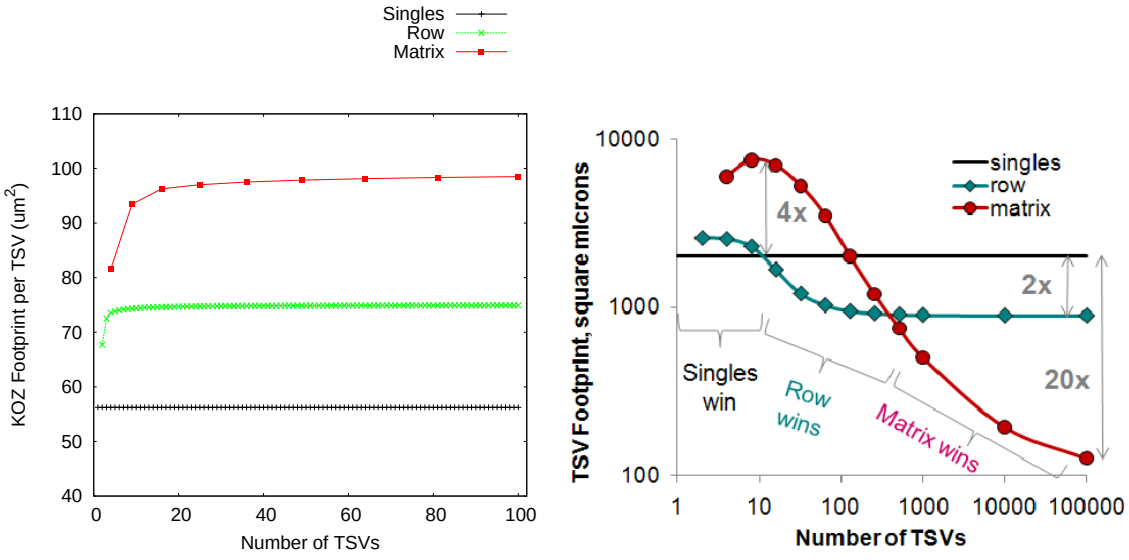
2. As $\Delta Idsat > 5\%$ is observed from the plot for 9 TSVs, devices cannot be placed in the substrate between two TSVs when spacing $S = D$. By adding the Idsat variation using the plot for 1 TSV, we can infer
   For the case $S = 2 \times D$, KOZ per TSV is $KOZ_{2D} = 2.5\ \mu m$.
   For the case $S = 3 \times D$, KOZ per TSV is $KOZ_{3D} = 2.0\ \mu m$.
   For the case $S \geq 4 \times D$, KOZ per TSV is minimum given by $KOZ_1 = 1.25\ \mu m$.

3. For 2 TSVs placed in a row with $S = D$, KOZ on either side along the direction of the row is given by $KOZ_2 = 1.53\ \mu m$.

4. For 3 TSVs placed in a row with $S = D$, KOZ on either side along the direction of the row is given by $KOZ_3 = 2.0\ \mu m$.

5. For 4 or more TSVs placed in a row with $S = D$, KOZ on either side along the direction of the row is given by $KOZ_4 = 2.125\ \mu m$.

Figure 4.3a shows a plot of the area footprint per TSV versus the number of TSVs computed according to above guidelines for single, row and matrix with minimum spacing of $S = D$. When the design uses analog FETs, the KOZ requirement as per [26] is much larger because $\Delta Idsat$ threshold is 0.5% as compared to 5% for digital FETs. In contrast to the KOZ values for larger analog FETs shown in Figure 4.3b [26], the asymptotic minimum KOZ footprint per TSV for digital 40 nm MOSFETs is achieved for single TSVs as is evident from Figure 4.3a.



(a) (b)

Figure 4.3: (a) KOZ footprint per TSV (μm^2) for digital 40 nm MOSFETs and (b) KOZ footprint per TSV (μm^2) for analog 0.5 μm MOSFETs [26]

4.1.3 Topology Options

Several regular topologies can be created by arranging the TSVs in rows or matrices and by changing the spacing between them. At all times the minimum pitch requirement must be maintained. The topologies considered for this work are explained below along with an example layout for each. The scheme employed for estimating maximum impact due to cross-talk for each topology is indicated with a simple top-view diagram. For each example, a calculation of the total area penalty due to TSVs is also provided.

4.1.3.1 Border

This topology consists of a single row of TSVs with $S = D$ i.e., with minimum TSV pitch P and is termed *Border*.

In this topology, the TSVs are placed along the periphery of the die or block. This topology is based upon the rationale that if the TSVs are placed along the periphery like I/O pins then a rectangular Silicon area obtained by blocking out the periphery can be used for placement of devices in its entirety. Hence this topology is termed Border. Thus, existing planar design practices and algorithms can be retained. Once the periphery is completely occupied, subsequent rows are separated by a distance of $S = 5 \times D$ such that stress components do not add up.

For e.g., a row of 3 TSVs with $S = D$ and the KOZ required is shown in Figure 4.4(a). Here, $KOZ_3 = 2.0$ μm is applicable along the axis of the row. In the direction perpendicular to the row, spacing between TSVs is $S \geq 4 \times D$ and so minimum $KOZ_1 = 1.25$ μm is applicable. Figure 4.4(b) shows the scheme used for cross-talk simulation.

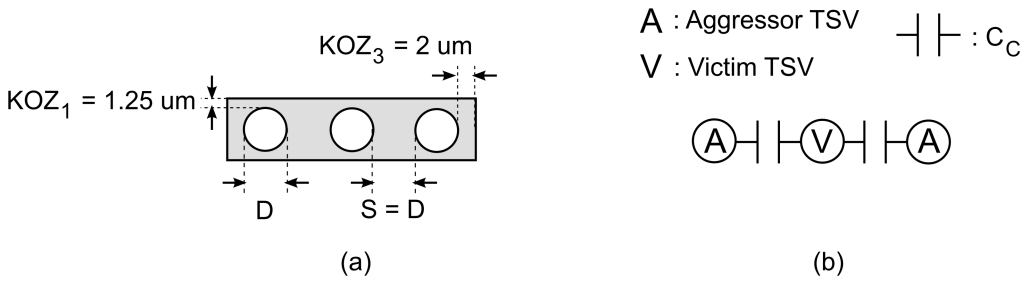


Figure 4.4: (a) The KOZ for a row of 3 TSVs and (b) The top view of cross-talk simulation scheme for a *Border* topology.

Total area consumed by TSVs and the KOZ is given by,

$$A_{tot} = (2 \times P + D + 2 \times KOZ_3) \times (D + 2 \times KOZ_1)$$

In general, for N TSVs and $N \geq 4$,

$$A_{tot} = ((N-1) \times P + D + 2 \times KOZ_4) \times (D + 2 \times KOZ_1)$$

Considering the number of TSVs (N) tending to infinity, the area per TSV is given by,

$$A_{TSV} = P \times (D + 2 \times KOZ_1)$$

4.1.3.2 Bundle

This topology consists of a square matrix of TSVs with $S = D$ i.e., with minimum TSV pitch P and is termed *Bundle*.

With a closely packed bundle of TSVs, an enclosure around the bundle including the KOZ can be blocked out for placement of devices. It is likely that the position of such a bundle is highly dependant on the design constraints. A bundle positioned at the centre of the die or block is considered as a viable topology for exploration purposes in this work.

For e.g., a 3x3 matrix of TSVs and the required KOZ is shown in Figure 4.5(a). Here, $KOZ_3 = 2.0\ \mu m$ is applicable along both axes i.e., row and column. Figure 4.5(b) shows the scheme used for cross-talk simulation.

Total area consumed by TSVs and the KOZ is given by,

$$A_{tot} = (2 \times P + D + 2 \times KOZ_3)^2$$

In general, for N TSVs and $N \geq 4$,

$$A_{tot} = ((\sqrt{N} - 1) \times P + D + 2 \times KOZ_4)^2$$

Considering the number of TSVs (N) tending to infinity, the area per TSV is given by,

$$A_{TSV} = P \times P$$

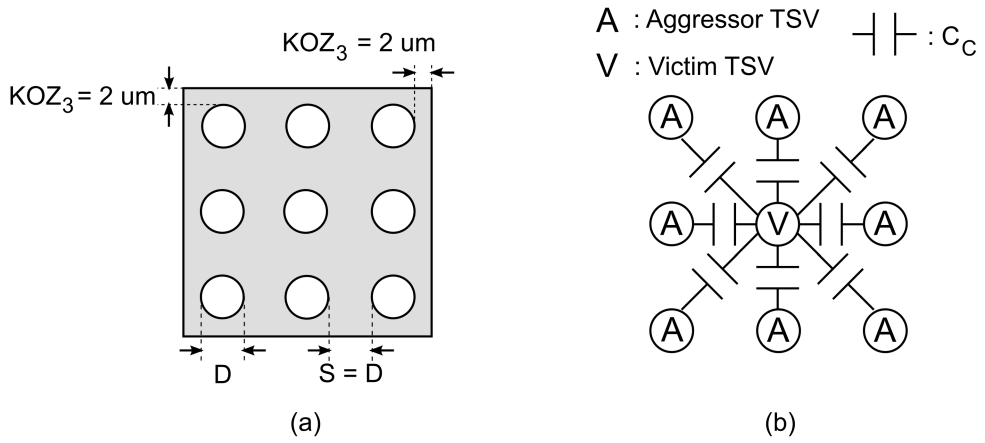


Figure 4.5: (a) The KOZ for a bundle of 3x3 TSVs and (b) The top view of cross-talk simulation scheme for a *Bundle* topology.

4.1.3.3 Bundle 1.5

This topology consists of a square matrix of TSVs with $S = 2 \times D$ i.e., with TSV pitch of $1.5 \times P$ and is termed *Bundle 1.5*.

The total area penalty is considered based upon the same rationale that an enclosure around the bundle including the KOZ can be blocked out for placement of devices.

For e.g., a 3x3 matrix of TSVs and the required KOZ is shown in Figure 4.6. Here, $KOZ_{2D} = 2.5\ \mu m$ is applicable along both axes i.e., row and column. The scheme used for cross-talk simulation is the same as *Bundle* topology shown in Figure 4.5(b).

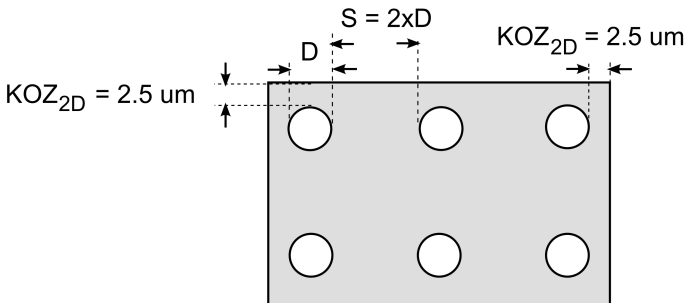


Figure 4.6: The KOZ for 3x3 TSVs in a *Bundle 1.5* topology.

Total area consumed by TSVs and the KOZ is given by,

$$A_{tot} = (2 \times (1.5 \times P) + D + 2 \times KOZ_{2D})^2$$

In general, for N TSVs and $N \geq 4$,

$$A_{tot} = ((\sqrt{N} - 1) \times (1.5 \times P) + D + 2 \times KOZ_{2D})^2$$

Considering the number of TSVs (N) tending to infinity, the area per TSV is given by,

$$A_{TSV} = 2.25 \times P \times P$$

4.1.3.4 Bundle 2

This topology consists of a square matrix of TSVs with $S = 3 \times D$ i.e., with TSV pitch of $2 \times P$ and is termed *Bundle 2*.

The total area penalty is considered based upon the same rationale that an enclosure around the bundle including the KOZ can be blocked out for placement of devices.

For e.g., a 3x3 matrix of TSVs and the required KOZ is shown in Figure 4.7. Here, $KOZ_{3D} = 2.0\ \mu m$ is applicable along both axes i.e., row and column. The scheme used for cross-talk simulation is the same as *Bundle* topology shown in Figure 4.5(b).

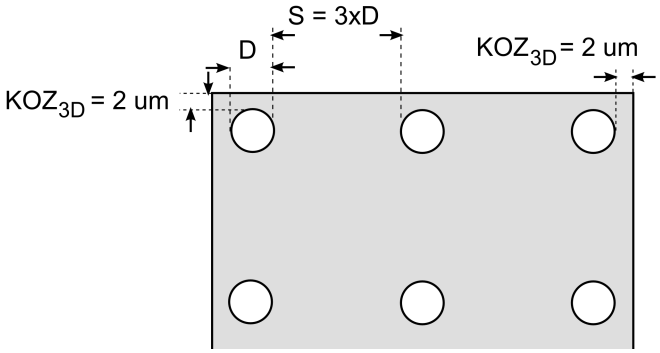


Figure 4.7: The KOZ for 3x3 TSVs in a *Bundle 2* topology.

Total area consumed by TSVs and KOZ is given by,

$$A_{tot} = (2 \times (2 \times P) + D + 2 \times KOZ_{3D})^2$$

In general, for N TSVs and $N \geq 4$,

$$A_{tot} = ((\sqrt{N} - 1) \times (2 \times P) + D + 2 \times KOZ_{2D})^2$$

Considering the number of TSVs (N) tending to infinity, the area per TSV is given by,

$$A_{TSV} = 4 \times P \times P$$

4.1.3.5 Shielded

This topology consists of a matrix of TSVs with $S = D$ with alternate rows of shield TSVs that are connected to ground and is termed *Shielded*.

Shielding breaks the capacitive coupling through the substrate between 2 signal TSVs along the y axis as shown in Figure 4.8(a). Thus the victim TSV is capacitively coupled to two neighbouring signal TSVs along the x axis. However, its capacitance to

ground increases by $2 \times C_c$ due to the coupling to neighbouring shield TSVs along y axis. Thus, *Shielded* topology is similar to a row of signal TSVs with two aggressors at the cost of an increased capacitance to ground and doubling the total number of TSVs. The scheme used for cross-talk simulation is as shown in Figure 4.8(b).

The total area penalty is considered based upon the same rationale that an enclosure around the bundle including the KOZ can be blocked out for placement of devices.

For e.g., a 6x3 matrix of signal and shield TSVs and the required KOZ is shown in Figure 4.8. The shield TSVs are shaded dark grey in the figure. Here, $KOZ_3 = 2.0$ μm is applicable along both axes i.e., row and column. The scheme used for cross-talk simulation is the same as *Shielded* topology shown in Figure 4.8(b).

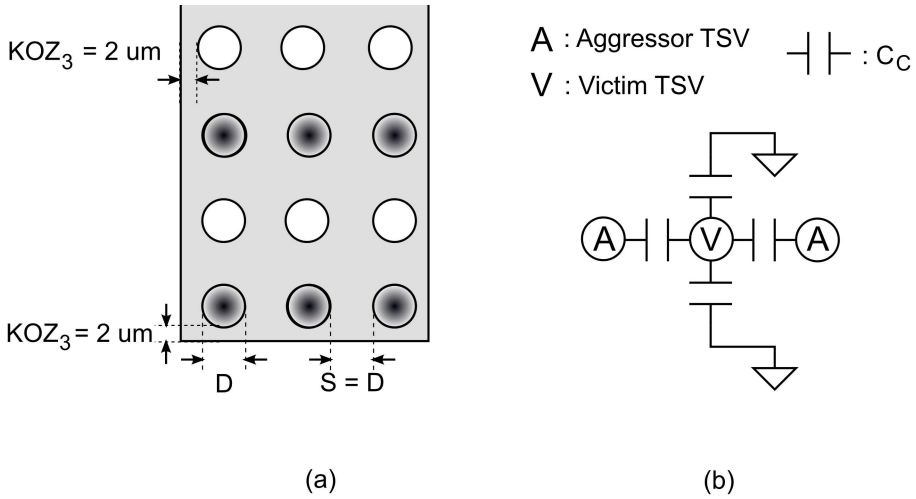


Figure 4.8: (a) The KOZ for 6x3 TSVs and (b) The top view of cross-talk simulation scheme for a *Shielded* topology.

Total area consumed by TSVs and the KOZ is given by,

$$A_{tot} = (5 \times P + D + 2 \times KOZ_3) \times (2 \times P + D + 2 \times KOZ_3)$$

In general, for N TSVs and $N \geq 4$,

$$A_{tot} = ((2\sqrt{N} - 1) \times P + D + 2 \times KOZ_4) \times ((\sqrt{N} - 1) \times P + D + 2 \times KOZ_4)$$

Considering the number of TSVs (N) tending to infinity, the area per TSV is given by,

$$A_{TSV} = 2 \times P \times P$$

4.1.3.6 Isolated

This topology consists of TSVs with $S = 5 \times D$ i.e., with TSV pitch of $3 \times P$ and is termed *Isolated*.

When $S \geq 4 \times D$, the minimum KOZ of $KOZ_1 = 1.25$ μm is applicable along both axes of each TSV as shown in Figure 4.9. TSVs are sufficiently spaced out such

that stress components do not add up and hence this topology is termed *Isolated*. Alternatively, it could also take the name *Bundle 3* following the series of topologies with increased spacing. However, this distinction is made since the area penalty for the isolated TSV topology is not derived from an enclosed rectangle but instead as the aggregate of individual TSV areas. The rationale behind this topology is that there is flexibility in placing the TSVs enabling an optimized TSV placement. On the downside, with this topology there is maximum disruption of existing placement and routing practices and algorithms. The scheme used for cross-talk simulation is the same as in *Bundle* topology shown in Figure 4.5(b).

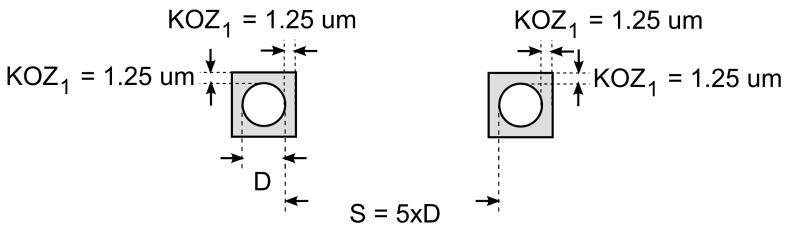


Figure 4.9: KOZ for TSVs in *Isolated* topology.

Total area consumed by N TSVs and their KOZ is given by,

$$A_{tot} = N \times (D + 2 \times KOZ_1)^2$$

The area per TSV is given by,

$$A_{TSV} = (D + 2 \times KOZ_1)^2$$

4.1.4 Topology Comparison

The 6 topology options discussed above are compared in terms of incurred area penalty and capacitive coupling induced noise voltage on the victim TSV. Finally, 4 topologies are selected for exploration in the proposed methodology.

For comparing topology options, 100 TSVs are considered with the Best Case (BC) geometry for Global level stacking i.e., a diameter of 4 μm. Capacitive coupling is simulated for 45 nm technology and Best Case (BC) geometry for Global level stacking. For these conditions, the resulting component values in the simulation circuit for capacitive coupling shown in Figure 4.1 are summarized in Table 4.1. These can be found in Tables 3.12, 3.11 and 3.8.

Coupling noise figures from simulations with worst case geometry are observed to be lower than those from the best case geometry. This is on account of the higher self capacitance (C_{TSV}) of TSVs with the WC geometry, as well as the nearly equal coupling capacitance (C_c) that yields a smaller noise spike in the victim TSV. Hence results for BC, which is the more pessimistic case are presented. On the other hand, an area penalty incurred for the WC geometry roughly doubles for all topologies. This

Component	Value
R_{TSV} (Ω)	0.50
L_{TSV} (pH)	20.20
C_{TSV} (fF)	15.40
C_c (fF)	5.87
R_{dr} (Ω)	327
C_{load} (fF)	0.224

Table 4.1: Component values for coupling simulation as per circuit shown in Figure 4.1.

follows from the fact that diameter and hence minimum pitch for the WC geometry is twice that of the BC geometry. A plot of the area penalty for each topology normalized to Bundle topology and capacitive coupling noise normalized to supply voltage Vdd is shown in Figure 4.10. It can be noted that normalized noise decreases non-linearly as the spacing between TVSs in a bundle increases as depicted in the plot.

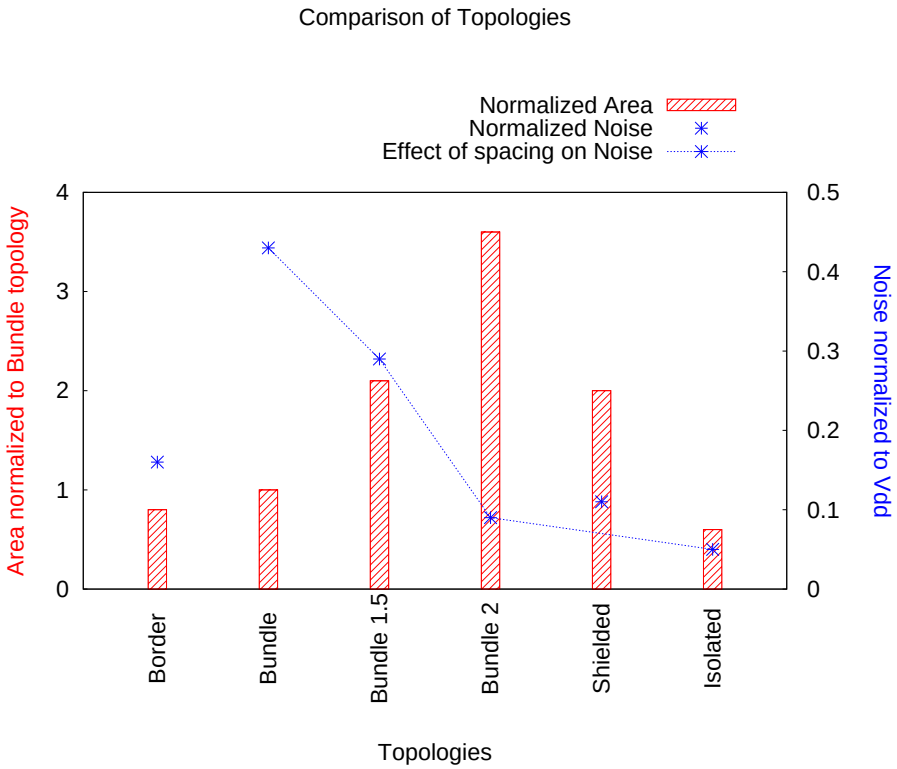


Figure 4.10: Area of 100 TSVs normalized to Bundle topology and capacitive coupling noise normalized to supply voltage Vdd for the 6 TSV placement topologies considered.

The Isolated and Border topologies both have less area as well as noise voltage compared to the remaining topologies. Also these 2 topologies have contrasting im-

plications on placement and routing of the planar design. Hence they are chosen for exploration. From the remaining 4 which can be categorized as bundled topologies, Bundle qualifies for minimum area and hence it is retained for exploration. Bundle 1.5 has an area equal to 2.1 times Bundle and normalized coupling noise equal to 0.29. Shielded topology has an area equal to 2 times Bundle and normalized coupling noise equal to 0.11. Thus Shielded will always be a better choice than Bundle 1.5 and hence is retained for exploration. While Bundle 2 has a coupling noise equal to .09, its area penalty is 3.6 times Bundle which makes it an inefficient topology in terms of area penalty. In general, it can be concluded that increasing the spacing to reduce the noise voltage is an inefficient solution compared to shielding.

The 4 topologies selected for exploration methodology wherein the horizontal wires are also routed and complete tier-to-tier interconnect electrical performance is estimated are Border, Bundle, Shielded and Isolated.

4.2 Implementation

The proposed methodology for exploring 3D interconnect topologies and estimating performance requires design and technology data which is provided via input text files.

The design-specific data required from the user includes the following.

1. The signal interface between vertically stacked tiers indicating input/output port.
2. The target technology nodes for the circuits in the tiers.
3. The level of 3D stacking (Global or Intermediate).
4. The floorplans of the tiers.

The technology data required includes the following.

1. The TSV technology parameters which are the Best Case (BC) and Worst Case (WC) geometries given in Table 3.9 and other parameters like material properties which are considered fixed and are listed in Section 3.4.
2. The planar technology parameters for 45 nm and 32 nm nodes, namely, R and C of the planar wires, C_{load} of the load gate and R_{dr} of the driver gate are given in Tables 3.1, 3.11 and 3.12.

Figures 4.11 and 4.12 show a flowchart for *implementation* of the methodology in the SystemC environment. TSV floorplans for *Border*, *Bundle*, *Shielded* and *Isolated* placement topologies that are described in Section 4.1.3 are generated in Step 1. The computation of the components for the RLC TSV model, the planar wire lengths in both the tiers and the gate parasitic components are performed in Step 2. The output of Step 2 is a parameterized driver (D) to load (L) model implemented as per the tier-to-tier path model shown in Figure 3.2.

In Step 3, SystemC-AMS simulation to estimate delay and slew is carried out by instantiating the parameterized D to L path model for each vertical TSV-based net.

Cross-talk simulation and calculation of Silicon area occupied by the TSVs and the KOZ as described in Section 4.1.3 is also performed in this step. In addition, the total capacitance of the vertical interconnect by summation of all nets is calculated. The results of the simulation methodology for the four 3D interconnect architectures resulting from the topologies are obtained at the end of Step 3. These results are obtained in the form of output text files and plots.

The tier-to-tier path is implemented using systemC-AMS *Electrical Linear Network* (ELN) primitives as described in Section 2.4. For e.g., SystemC Module of the TSV model, termed *sc_tsv*, accepts a list of parameters which are used by C++ functions within the module to calculate the values of the parasitic components. Further, a SystemC Module for the tier-to-tier path is built by instantiating an object of Module *sc_tsv*. By instantiating remaining resistors and capacitors in the path, a SystemC Module *sc_path* is built. In order to simulate a complete vertical interface with N number of TSVs, an array of objects belonging to the Module *sc_path* is instantiated. The size of the array N is set by a variable, thus facilitating scalability. The model also has a built-in performance calculation function which calculates delay and slew from node D to node L.

The *conceptual idea* for integrating this methodology into a high-level system simulation framework is also shown in Figure 4.12. The parameterized D to L model for each vertical TSV-based interconnect is interfaced with two adapters on either end. The standard logical (L) ports of SystemC/C++ behavioural modules can be interfaced with the electrical (E) nodes of SystemC-AMS D to L model through interfacing adapters. These adapters which are Logical (L) to Electrical (E) and vice versa can be built using systemC-AMS *Discrete Event* (DE) primitives as described in Section 2.4.

4.2.1 Algorithm for Topologies

The algorithms employed to generate the TSV placement topologies take as input the floorplans of the two tiers and a file in which all the vertical nets are listed. The sequence of TSV placement follows the sequence of the nets in the file. The goals of these algorithms are to maintain the fixed structure of the topology while keeping the wire length minimum. It also ensures that no two TSVs overlap. For each net, first the (x,y) co-ordinates of the end-points on both the tiers are taken. The quadrants in which the two end-points lie are determined. Thus each net is associated with a *quadrant pair*. The algorithms for Border, Bundle and Shielded topologies are based on placing the TSV depending on the quadrant pair of its net.

For the Border topology, a TSV is placed along the edge (L for left, R for right, T for top and B for bottom). Table 4.2 shows all combinations of quadrants pairs and a priority list of edges on which the TSV should be placed. If an edge is fully occupied with TSVs, the next edge in the priority list is checked. In order to provide flexibility, in the input file the user can specify *windows* where TSV placement is allowed. A window is specified using two points along any of the edges. The first TSV on an edge is placed at the mid-point of the window while the subsequent ones are distributed

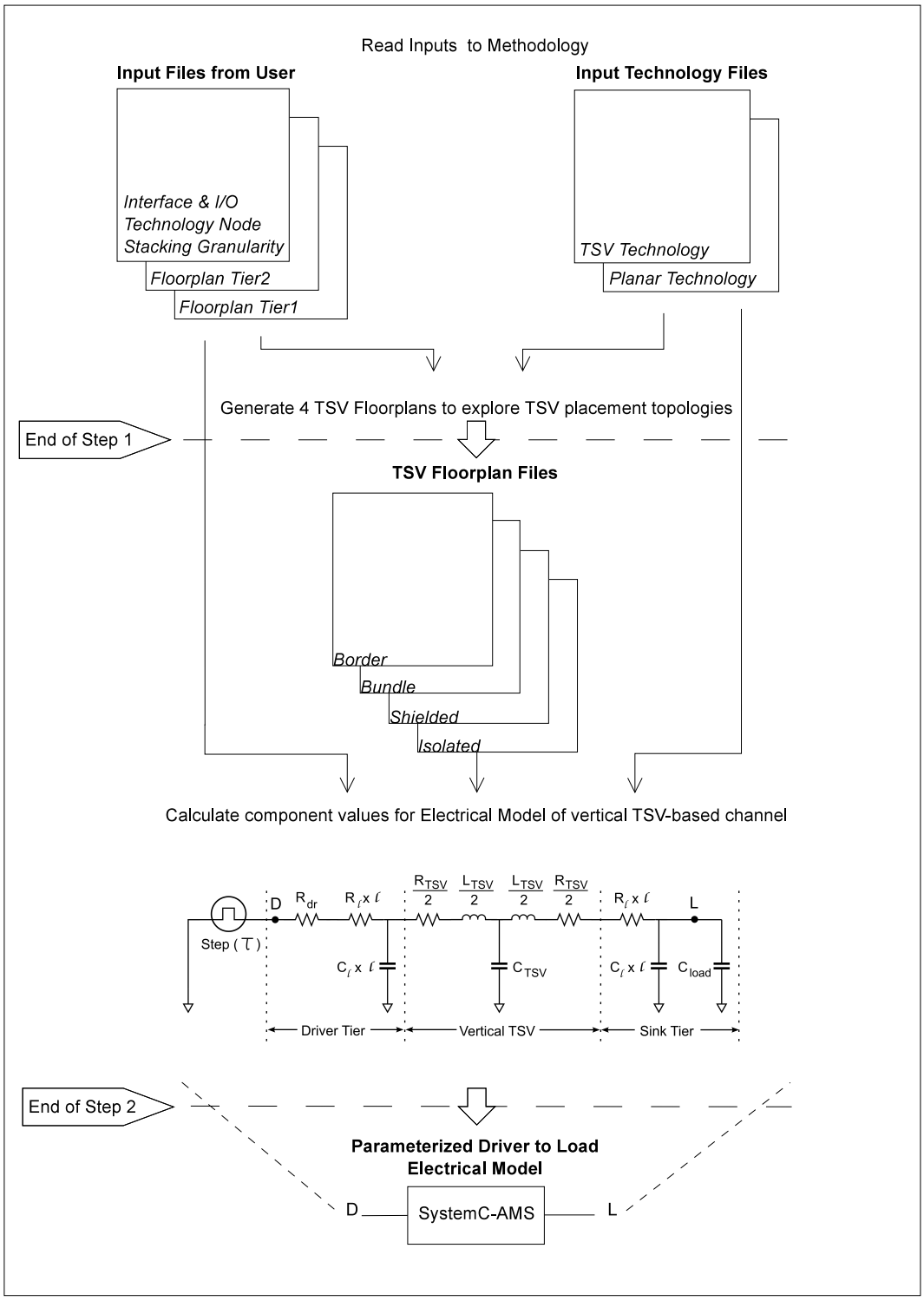


Figure 4.11: Step1: TSV floorplanning for *Border*, *Bundle*, *Shielded* and *Isolated* placement topologies. The output is TSV floorplans. Step2: Computation of RLC TSV model, planar wire lengths in both tiers and buffer parasitic components. The output is D to L tier-to-tier path model.

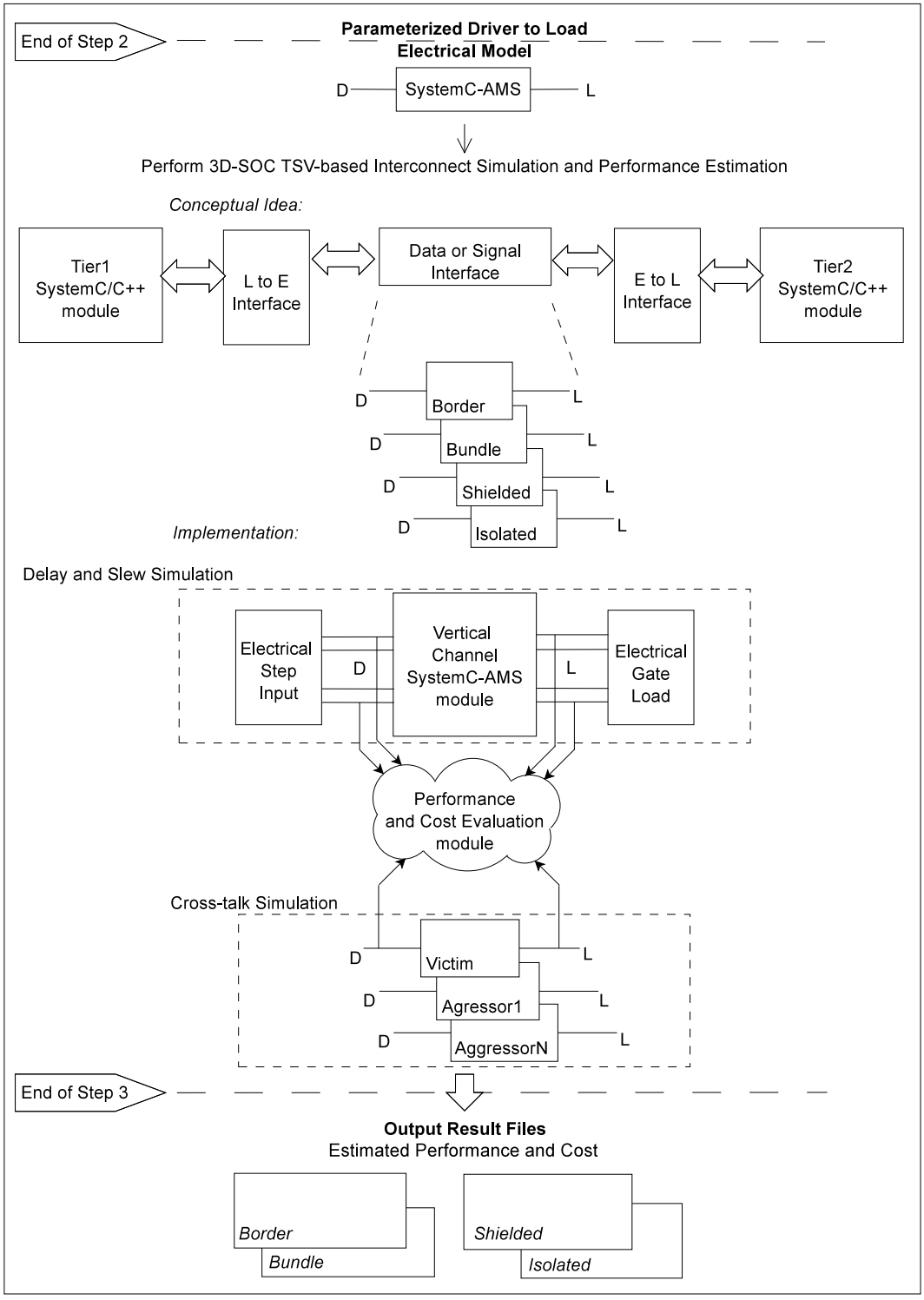


Figure 4.12: Step 3: Simulation to estimate delay, slew and cross-talk. Performance and cost evaluation module is built-in. The output is detailed performance and cost for explored topologies.

Quadrant Pair	Edge				Quadrant			
(0, 0)	L	B	T	R	0	1	3	2
(1, 1)	T	L	R	B	1	2	0	3
(2, 2)	R	T	B	L	1	2	0	3
(3, 3)	B	R	L	T	3	0	2	1
(0, 1)	L	T	B	R	0	1	2	3
(1, 2)	T	R	L	B	1	2	3	0
(2, 3)	R	B	T	L	2	3	0	1
(3, 0)	B	L	R	T	3	0	1	2
(2, 0)	T	B	L	R	0	2	1	3
(1, 3)	L	R	T	B	3	1	2	0

Table 4.2: Edge priority list and Quadrant priority list for Border topology and Bundle topology respectively for TSV placement corresponding to a given end-point Quadrant pair.

alternately on both sides of the mid-point.

For the Bundle, Bundle 1.5 and Bundle 2 topologies, the bundle or matrix of TSVs is arranged in a square at the centre with spacing between TSVs $S = D$, $S = 2 \times D$ and $S = 3 \times D$. This bundle is also considered as comprising of quadrants which are aligned to the quadrant numbers of the tier floorplan. The TSV is placed in the quadrant of the bundle according to priority Table 4.2. For the Shielded topology, the bundle structure of TSVs that is generated is rearranged to have the rows separated by $S = 2D$ so as to accommodate shield TSVs in alternate rows. For the Isolated topology, TSV placement is carried out at a legal TSV position closest to the mid-point of the line joining the two end-points in the net.

Thus, the placement algorithm minimizes the length of the interconnect and hence delay, subject to the constraint of maintaining the topology. Each TSV location is determined independently of the others using the basic algorithm described here such that no two TSVs overlap. Time complexities of the algorithms for the 4 topologies vary linearly with number of TSVs to be placed assuming that each TSV is placed within a minimum time step. The SystemC simulation time for the step one i.e., generating the TSV floorplans for the 4 topologies and steps 2 and 3 combined i.e., computing component values and running the AMS simulation for two cases, one with 74 TSVs and other with 1000 TSVs is summarized in Table 4.3. The number of TSVs increase by a factor of 13.5 while the simulation time increases by a factor of 7.4.

No. of TSVs	Simulation Time (s)		
	Step 1	Steps 2 and 3	Total
74	2	31	33
1000	17	226	243

Table 4.3: Simulation time for the proposed SystemC simulation methodology.

4.2.2 Methodology Results

This Section describes the results of the methodology and explains the use of the estimated performance and cost metrics in system design. It also provides a summary of a simple test case of 16 vertical TSV-based interconnects. The results of this test case are discussed briefly to give a general overview. A full case study of a 7-port 3D router is presented in the Chapter 5.

The following results of the simulation methodology provide the electrical performance of the interconnect.

1. Minimum and maximum net capacitance (fF) - Firstly, the net with maximum capacitance dictates the maximum delay and hence the operating frequency of the complete vertical interconnect, for e.g., the operating frequency of a bus that communicates between two tiers. Secondly, the net with the minimum capacitance and the net with the maximum capacitance give an indication of the relative slack difference across the vertical interconnect taking into account for timing. A large ratio between the two indicates that a closer look must be taken to evaluate the suitability of the placement topology for the particular design. On the other hand, a ratio close to unity indicates that the topology was well-suited for the design and the slack across all wires in the vertical interconnect is balanced.

2. Minimum and maximum net delay (ps) - The delay through the net is a representative number as it is dependant on the R_{dr} i.e., the ON resistance of the driver. However, based on the assumption that the driver is a 40x Inverter, an estimation of the achievable frequency can be made. By adding a setup time of the latch or flip-flop to the maximum net delay, the clock period and in turn the achievable frequency of the vertical interconnect can be estimated. This is an important metric for system design as the operating frequency of the communication interface can be a design consideration for the IP cores of a 3D-SOC or for the functional blocks of a 3D-SIC.

3. Minimum and maximum net slew (ps) - Similar to delay, the slew is a representative number as it is dependant on the R_{dr} i.e., the ON resistance of the driver. A degraded slew implies that the short circuit current when both PMOS and NMOS are conducting during the switching of the gate flows for a longer time. This increases the power dissipation due to direct paths. This contributes to the total power of the chip and hence it is useful for system power estimation.

4. Maximum delay increase due to coupling (ps) - The worst case increase in delay due to coupling can be used for calculating the maximum interconnect delay with noise and hence the achievable frequency with noise. As it projects the worst case achievable frequency, maximum delay increase due to coupling is an important result of the electrical simulation.

5. Capacitive coupling induced noise voltage normalized to Vdd - A silent net termed as a victim experiences a noise voltage due to the switching activity in other nets in its proximity termed aggressors. The capacitive coupling induced noise can cause functional failure if it is not within the noise margin specification for the circuit

technology. Although this can be solved during circuit design, the estimated worst case capacitive coupling induced noise voltage normalized to Vdd can be used for estimating the cost of having buffers or other circuit level solutions earlier in the system design stage.

The following results of the simulation methodology provide the cost of the interconnect in terms of area and power dissipation.

1. Total capacitance (fF) - The total vertical interconnect capacitance is the sum of the capacitances of all the nets. The dynamic power due to the switching activity in the interconnect is directly proportional to the total capacitance. The dynamic power contributes to the total power of the chip and hence it is useful for system power estimation.

2. Total TSV area (μm^2) and percent TSV area - The area occupied by the TSVs including the KOZ is an important result for estimating the Silicon area for the individual dies. Thus, besides estimating die area for the logic gates, the area penalty coming from TSVs and the KOZ also must be added.

A test case considered to demonstrate the methodology is summarized as follows.

Tier 1 size of $500\mu m \times 500\mu m$ is assumed to be built using 45 nm CMOS technology.

Tier 2 size of $500\mu m \times 500\mu m$ is assumed to be built using 32 nm CMOS technology.

The stacking granularity is Global.

16 TSV based interconnects of which 8 nets are directed from Tier 1 to Tier 2 and 8 from Tier 2 to Tier 1.

A detailed report of the 16 vertical nets is obtained at the output of the methodology in the form of text files. The report provides the capacitance of each net split into its three components i.e., the capacitance of horizontal interconnect in each tier and the capacitance of TSV. For each topology, the results are provided across both corners of the TSV geometry that are derived in Section 3.2.2.3. Best Case TSV geometry gives a TSV capacitance of 16 fF and Worst Case TSV geometry gives a TSV capacitance of 53 fF. However, for the Shielded topology, these capacitance values increase to 28 fF and 65 fF respectively after accounting for the increase it capacitance to ground as explained in Section 4.1.3.5. The net which has maximum total capacitance in the design and the net which has minimum total capacitance are reported. The detailed report also gives the delay through and slew of each net. The maximum impact of coupling capacitance on a net going from tier 1 to tier 2 as well as a net going from tier 2 to tier 1 is reported. Finally, the total interconnect capacitance and area penalty due to the TSVs and the KOZ is reported. The most important results are summarized in the Table 4.4. Detailed reports and plots showing the TSV placement are provided in Appendix C. The electrical performance and cost results are briefly discussed as follows.

Results of Methodology	Border		Bundle		Shielded		Isolated	
	BC	WC	BC	WC	BC	WC	BC	WC
Performance								
Min. Capacitance (fF)	32	71	76	109	84	115	19	60
Max. Capacitance (fF)	192	237	166	203	178	215	118	155
Min. Delay (ps)	8	17	19	26	21	27	6	14
Max. Delay (ps)	55	67	42	51	45	54	29	38
Min. Slew (ps)	24	53	57	80	62	84	17	44
Max. Slew (ps)	167	206	129	157	138	166	90	116
Max. ΔDelay due to coupling (ps)	6	4	24	21	8	7	1	1
Percent voltage change	17	07	43	22	11	5	5	2
Cost								
Total capacitance (fF)	1833	2407	1783	2352	1967	2542	1093	1702
Total TSV area (μm^2)	811	2487	1040	3630	2072	7486	676	1763
Percent TSV area	0.3	1.0	0.4	1.5	0.8	3.0	0.3	0.7

Table 4.4: Methodology results for a test case of 16 nets. 3D interconnect performance and cost is estimated for the test case with $500\mu m \times 500\mu m$ dies in 45 nm and 32 nm CMOS technologies respectively for the explored topologies.

Net capacitance, delay and slew - The values of these parameters for the BC TSV are upto 2 times those of the WC TSV. There are two reasons for this. Firstly, the TSV pitch for WC is two times that of the BC and hence the placement grid for WC is only half as fine as BC. This results in longer wires. Secondly, the TSV capacitance for WC is greater than BC by 37 fF. With regards to the topologies, the Isolated topology has the minimum capacitance, delay and slew values. This is because of the flexibility in placement offered by this topology. In general, a worst case net for the Border topology will be the net travelling across the length of the block or die. In case of the Bundle and Shielded topologies the worst case net will be the net travelling half the length of the block or die. However, these performance parameters are design dependant in a way that certain topologies are well-suited for certain design scenarios. For e.g., the Border topology can be suitable for a block which does not communicate to any other block in the design other than the one it is vertically stacked on. In such a design scenario, input TSVs can be placed along one edge and output TSVs along the opposite edge while the logic in the path can be efficiently placed in the area in between.

Impact of capacitive coupling - The Isolated topology has the least impact of noise due to the spacing between TSVs $S = 5 \times D$ as explained in Section 4.1.1. The Shielded topology comes next which has a noise less than Border topology. This follows from the explanation in the previous paragraph that the TSV capacitance to ground increases due to shielding and hence the noise spike is smaller. The Bundle topology has the maximum noise.

Total capacitance - The total capacitance of the interconnect obtained by summing

all the net capacitances is the least for Isolated. It increases by about 90 % for Shielded and about 80% for Border and Bundle topologies. The average wire length for Bundle and Shielded can be approximated as equal as both are located at the centre. The increase seen in the Shielded topology can once again be explained as occurring due to the increased capacitance to ground.

TSV area - The comparison of area penalty due to TSVs and the KOZ is discussed in Sections 4.1.3 and 4.1.4. The area penalties normalized to the Bundle topology for Border, Shielded and Isolated are 0.8, 2.0 and 0.65 respectively which are in agreement with the topology comparison analysis in Section 4.1.4. It can be noted that the WC TSV exploration results in a percentage TSV area utilization of upto 3% while the BC TSV exploration results in a percentage TSV area utilization of upto 0.8%. Although Isolated topology has the best performance and the least cost in terms of area, it must be noted that the design complexity associated with physical design when TSV placement is flexible is an added cost as discussed in Section 4.1.3. However, this could not quantified given the scope of this work.

4.3 Conclusions

- Design considerations for placement of TSVs such as capacitive coupling and TSV Keep-Out-Zone are discussed in Sections 4.1.1 and 4.1.2. These factors along with the design complexity involved in planar place and route lead to the exploration and experimentation of several topology options described in Section 4.1.3.

- The TSV placement topology options are analyzed in Section 4.1.3. It is found that the normalized noise decreases non-linearly as spacing between TVSs in a bundle increases 4.1.4. Also, increasing the spacing to reduce the noise voltage is an inefficient solution compared to shielding.

- In Section 4.1.4, four topologies are selected based on trade-offs between one or more performance and cost metrics. These topologies are termed Border, Bundle, Shielded and Isolated. These represent extreme points in the exploration design space such that performance and cost metrics of other topologies lie in between these and can be interpolated.

- The methodology flow is divided into 3 steps. Steps 1 and 2 shown in Figure 4.11 involve executing algorithms for floorplanning and computations which are implemented using C++ functions. Step 3 shown in Figure 4.12 uses a mix of C++/SystemC-AMS to simulate vertical interconnect with a built-in performance and cost evaluation module.

- Design-specific input data and selection of significant technology parameters offer flexibility for exploration. By constraining the placement to fixed structures, complexity of algorithms is kept minimal keeping in mind an early stage of design. Parameterizability and scalability is achieved in an efficient manner within an integrated system simulation environment.

- A text report which gives detailed performance of each net as well as a table which gives highlights such as minimum, maximum and total values for metrics for Best Case and Worst Case is provided as a result of the methodology. Important results and their significance in system design are explained in Section 4.2.2. An overview for a sample test case is shown in Table 4.4 and the results are discussed.

5 Application and Results

This chapter describes a case of a TSV interconnect based 7-port router within a 3D NOC mesh for a stacked MP-SOC. The proposed methodology is applied and the explored TSV placement topologies are compared on the basis of electrical performance in terms of delay, slew and cross-talk as well as cost in terms of area and power. From the analysis of the results it is concluded that Isolated topology is most preferred and gives the best performance and minimum cost.

5.1 7-port 3D router

5.1.1 Motivation for the case

For multi-processor systems, Network on Chip (NoC) has been proposed as a scalable communication fabric to solve the problem of interconnect scaling and performance degradation seen in a bus when the number of nodes in a multi-processor system increases beyond 10 [36, 37]. Work related to NOC architectures for 3D-SOCs can be found in [38, 39, 3].

In [35], Kumar and van Leuken have presented an architecture of a router for a 3D stacked MP-SOC. Conventionally, planar routers have 5 ports, namely, North, South, East, West and Local. The presented 3D router has two additional ports, Up and Down such that a 3D NOC can be achieved by stacking of meshes as shown in Figure 5.1. The 3D router uses TSV technology for these Up and Down links to communicate with routers above and below it in the 3D mesh. The addition of two links i.e., Up and Down to a conventional planar router can lead to contention and arbitration issues for the data traffic in the NOC. These are solved by adopting a suitable router architecture. On the other hand, issues related to delay through the router and additional area

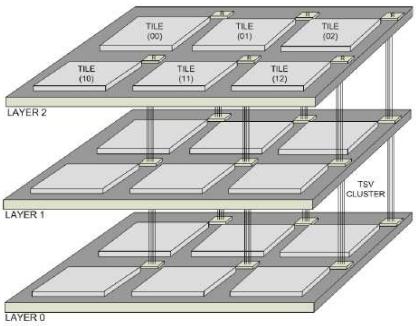
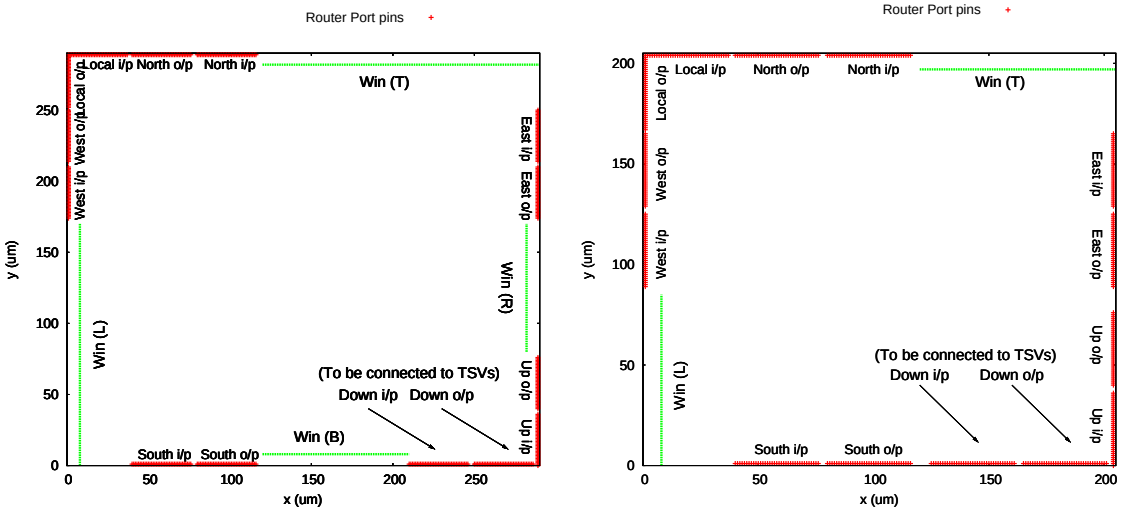


Figure 5.1: Illustration of 3D MP-SOC with 7-port routers in a 3D mesh [35].



(a) 290 $\mu m\times$ 290 μm 3D router in 45 nm node. (b) 205 $\mu m\times$ 205 μm 3D router in 32 nm node.

Figure 5.2: Floorplans of 3D router on the upper tier with locations of all 7 ports and placement windows for Border topology. For 45 nm node the allowed windows are Win(L), Win(R), Win(T) and Win(B) while for 32 nm node the allowed windows are Win(L) and Win(T).

overhead depend on the interconnect technology and placement. In their work, Kumar and van Leuken have evaluated the performance and limitations of the 3D NOC from an architectural point of view. The area penalty coming from TSVs is also estimated by implementing 3 full custom configurations of a TSV in UMC 90 nm technology.

The constraints coming from the floorplan of the router create challenges in TSV placement. Firstly, ports are located along the edges since horizontal wires going outwards establish connectivity to the tile and other routers within the planar mesh. As shown in Figure 5.2a, the planar ports are mirrored about horizontal and vertical axes, for e.g., North and South ports are mirrored about horizontal axis. This ensures that for the adjacent routers the North output of one router exactly faces the South input of the other router. Thus from the output buffer of North port to input buffer of South port, a shortest possible global wire length between the two routers can be achieved. The switch in the router is implemented as a cross-bar, i.e., each input port has connections to all other output ports. Maintaining the symmetry in port locations of the router, the added Up and Down ports are also located along the edge.

Secondly, the Up and Down ports of the vertically stacked routers must be exactly aligned. This ensures that the minimum wire length between them in the vertical direction could be achieved. Such a vertical path would be through the metal vias upto a global metal layer and then the vertical TSV itself going through the Silicon wafer and connecting the bump on the lower tier. Thirdly, the arbitration logic and buffers for the ports in the planar router design are placed close to the ports. With this placement, a

majority of the devices are placed along the periphery. Thus, it is expected that white space would be available in the central portion. However, the central portion has dense wiring of the router cross-bar. In addition to placement challenges, an estimation at an early stage for migrating the design to subsequent technology nodes can provide useful insights for architecture design. These critical aspects make a case for exploring TSV placement topologies for the 3D router.

Thus there is a need to find a solution to the placement of TSVs for the given 3D router by evaluating possible TSV placement options when an initial floorplan of the design is known. The proposed methodology is thus directly applicable for this case because electrical performance and cost estimation of the interconnect can potentially give an added perspective to system design of the 3D MP-SOC.

5.1.2 Design details

Goal - The objective of this case study is to apply the simulation methodology proposed in Chapter 4 and present the results. This is carried out across 45 nm and 32 nm nodes. The focus is on the analysis and comparison of explored TSV placement topologies and technology nodes. Moreover, the results obtained at the output of the methodology are translated into performance and cost metrics useful for system design. This serves the objective of this work as defined in Section 1.2.

The 3D 7-port router in [35] has a width of 37 bits which includes data as well as flow control. Thus each port width is 37 and considering unidirectional input and output lines, 74 TSVs need to be placed for the Down port of the router. The area of a die or logic block can be estimated as a function of gate count N_g [40] and is given by Equation (5.1). A_g is an empirical parameter given by $A_g = 3125\lambda^2$ where λ is half of the feature size for a specific technology node. Assuming the floorplan of the 3D router to be a square and gate count of around 50K, its area and dimensions are given in Table 5.1.

$$A_{die} = N_g \times A_g \tag{5.1}$$

Technology Node (nm)	Parameter A_g (μm^2)	Area of Router A_r (mm^2)	Dimensions of Floorplan (mm)
45	1.582	0.0838	0.290 × 0.290
32	0.800	0.0424	0.205 × 0.205

Table 5.1: Estimated 7-port 3D router dimensions across 45 nm and 32 nm technology nodes.

The following design-specific data is provided as input to the simulation methodology proposed in Chapter 4.

1. The signal interface between vertically stacked tiers consists of 74 TSVs where input and output signals are 37 each.

2. The technology nodes for the circuits in the tiers are 45 *nm* and 32 *nm* in two separate runs of the methodology.

3. The stacking granularity is taken to be Global level as the router gate count is about 50K gates which results in an appreciable die area. Also planar wiring between two routers is established with global wires which makes the selection of stacking granularity convincing.

4. The router floorplans are shown in Figure 5.2.

   Run 1 for 45 nm - Figure 5.2a shows the windows allowed for TSV placement for the Border topology which are along left (L), right(R), top(T) and bottom(B).

   Run 2 for 32 nm - Figure 5.2b shows the windows allowed for TSV placement for the Border topology only along L and T edges. This was provided as a user input since it is not feasible to place TSVs on the edges B and R due to congestion.

5.2 Results

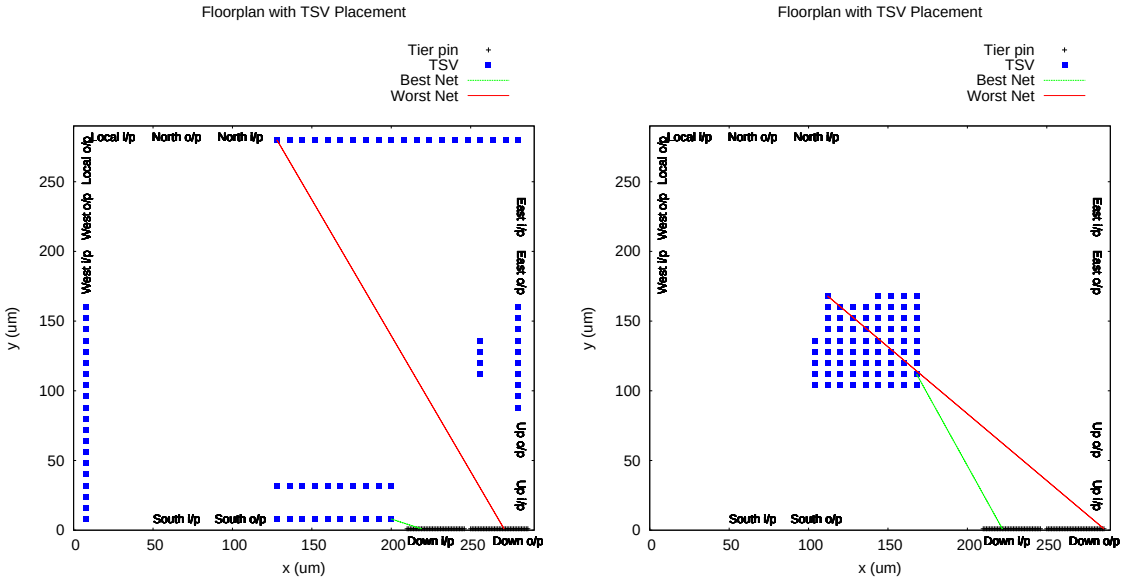
In this Section, methodology results for 45 *nm* run and Best Case TSV technology (Section 3.2.2.3) are used to perform a critical analysis of topologies and recommend the most suitable topology. The basis of this is the electrical performance and cost metrics. Further, these are also translated to metrics usable for system-level and architecture-level design. Also, the similarities and differences between the results of 45 *nm* and 32 *nm* nodes are highlighted.

5.2.1 Topology Comparison

5.2.1.1 Maximum Net Capacitance

Performance metric	*Border*	*Bundle*	*Shielded*	*Isolated*
Min. Capacitance (fF)	26	80	80	26
Max. Capacitance (fF)	184	152	176	186
Min. Delay (ps)	7	20	19	7
Max. Delay (ps)	47	38	44	47
Min. Slew (ps)	21	61	60	21
Max. Slew (ps)	143	116	135	144
Order of preference	3	1	2	4

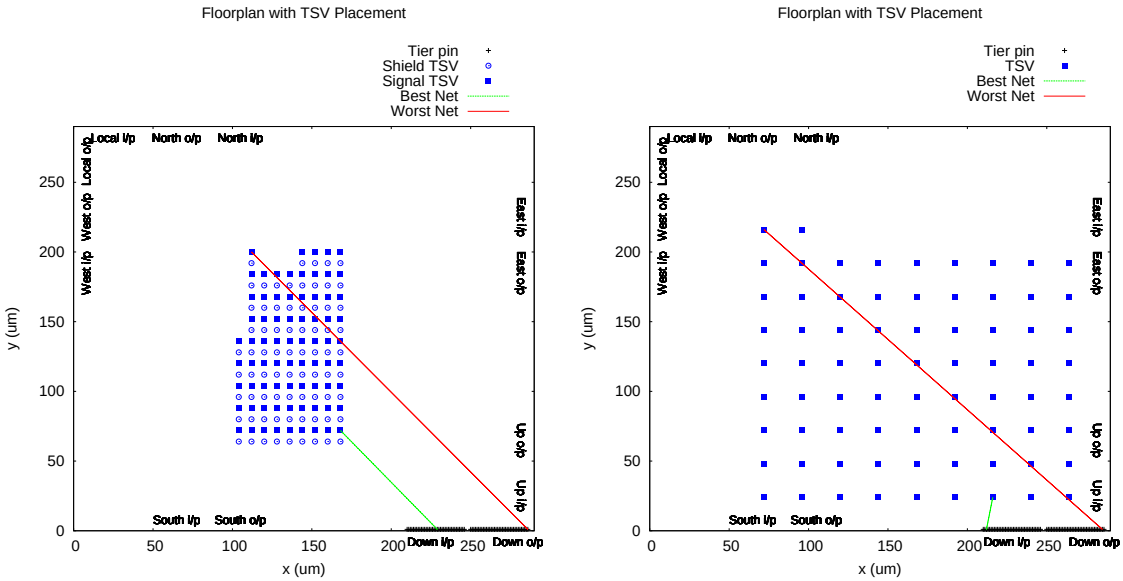
Table 5.2: Maximum and minimum capacitance, delay and slew for the 7-port router for the Best Case TSV performance corner and 45 *nm* technology node. Judging from the maximum capacitance, *Bundle* is the most preferred topology.



(a) Border topology.

(b) Bundle topology.

Figure 5.3: Floorplan of 3D router showing TSV placement with (a) *Border* topology and (b) *Bundle* topology in 45 *nm* technology. The highlighted nets have maximum (Worst) and minimum (Best) capacitance and hence have maximum and minimum delay/slew respectively.



(a) Shielded topology.

(b) Isolated topology.

Figure 5.4: Floorplan of 3D router showing TSV placement with (a) Shielded topology and (b) Isolated topology in 45 *nm* technology. The highlighted nets have maximum (Worst) and minimum (Best) capacitance and hence have maximum and minimum delay/slew respectively.

Analysis across topologies - From Table 5.2 it can be seen that, for Border and Isolated topologies, maximum delay is about 7 times the minimum delay while for Bundle and Shielded topologies, maximum delay is about 2 times the minimum delay. Figures 5.3 and 5.4 clearly show the differences in planar lengths for each topology which cause the best (shortest wire) and worst (longest wire) delay. Thus, the delay through the vertical interconnect is non-uniform throughout the Down port. However, as explained in Section 5.1, the delay through the horizontal interconnect in the 3D mesh is uniform throughout the port. If it is desirable to achieve the same for the vertical interconnect, the results from the methodology can be used as a feedback to consider a re-plan of the placement of the Down port. The maximum capacitance for the Isolated topology is the highest while the maximum capacitance for the Border topology is only marginally lower. The maximum capacitance for the Bundle topology is the lowest while that of the Shielded topology lies in between Bundle and Border.

Judging from the maximum capacitance, the *order of preference* of topologies is as shown in Table 5.2.

Translation to system metrics - Delay through the vertical path from a driver inverter to a load inverter is an indication of the achievable operating frequency. In order to estimate the clock period, the setup time of the latch or flip-flop must also be taken into account. A setup time of 25 ps for 45 nm technology [41] is added to the maximum net delay. The achievable operating frequencies obtained for the vertical interconnects for each topology are given in Table 5.3. The Bundle topology has the highest achievable operating frequency. The achievable operating frequency of the interconnect is an important metric for system design as it can be used for making decisions about the communication between tiers. For e.g., if vertical links between routers can be operated at a higher frequency, potential architectural enhancements can be made to take advantage of this.

A degraded slew implies that the short circuit current when both PMOS and NMOS are conducting during the switching of the gate flows for a longer time. This increases the power dissipation due to direct paths given by Equation (5.2) where t_{sc} is the time for short circuit, I_{peak} is the peak short circuit current, Vdd is the supply voltage and f is the frequency of switching. This contributes to the total power of the chip and hence is useful for system power estimation.

$$P_{dp} = t_{sc} \times Vdd \times I_{peak} \times f \tag{5.2}$$

It should be noted that the delay and slew are representative because an assumption about the driver resistance R_{dr} is made in the simulation methodology. Delay and slew are dependent on the size of the driver buffer or insertion of buffers which are circuit-level optimizations. On the other hand, the capacitance is an absolute metric which can be compared with the horizontal interconnect capacitance to make a design decision for the 3D NOC mesh. For e.g., performance of the vertical and horizontal interconnects between the routers can directly be compared using maximum capacitance. Assuming an average size for a single-core tile to

be $1.5\mu m \times 1.5\mu m$ [42, 43], the router to router horizontal wire capacitance is calculated for a length equal to 1.5 μm. By using capacitance per unit length C_l for global interconnect (refer to Table 3.1), the resulting capacitance is about 300 fF. This estimate is 1.6 to 2 times that of the maximum capacitance of the vertical interconnect.

In conclusion, the achievable operating frequency of vertical interconnect (Table 5.3) for the most preferred Bundle topology is about 2 times that of the horizontal interconnect and least preferred Isolated topology is about 1.6 times that of the horizontal interconnect.

System metric	*Border*	*Bundle*	*Shielded*	*Isolated*
Operating frequency of vertical interconnect (GHz)	13.9	15.8	14.5	13.9

Table 5.3: The Achievable operating frequencies of the vertical interconnect for the 7-port router. For the Bundle topology the achievable frequency is about 2x that of the horizontal interconnect and for the Isolated topology it is about 1.6x that of the horizontal interconnect.

5.2.1.2 Capacitive Coupling Noise

Performance metric	*Border*	*Bundle*	*Shielded*	*Isolated*
Max. ΔDelay due to coupling (ps)	5	23	8	1
Noise induced voltage normalized to Vdd	0.16	0.42	0.11	0.05
Order of preference	3	4	2	1

Table 5.4: Maximum ΔDelay and Noise induced voltage normalized to Vdd for the 7-port router for the Best Case TSV performance corner and 45 nm technology node. Judging from the noise induced voltage normalized to Vdd, *Isolated* is the most preferred topology.

Analysis across topologies - From Table 5.4, the worst impact of the capacitive coupling is observed for the Bundle topology and the least is observed for the Isolated topology. The noise due to the Border topology is more than the Shielded topologies. Sections 4.1.1 and 4.1.3 cover the simulation and analysis of the capacitive coupling noise.

Judging from the impact of capacitive coupling, the *order of preference* of topologies is as shown in Table 5.4.

Translation to system metrics - Delay through the vertical interconnect increases due to the capacitive coupling which is given in Table 5.4 as ΔDelay. As shown in Table 5.5, the achievable frequency is reduced due to noise which is an important

system metric. The capacitive coupling induced noise can cause functional failure if it it not within the noise margin. For 45 nm technology node, the noise margin is approximately 0.34 [44]. From Table 5.4 it can be seen that the noise voltage normalized to Vdd for the Bundle topology is 0.42 which violates the noise margin.

In conclusion, for the worst case noise simulated all the topologies except Bundle are within the noise margin for 45 nm technology node. The achievable operating frequency decreases due to capacitive coupling. From Table 5.5 it can be seen that achievable frequency with noise is 27% lower for the Bundle topology and 1% lower for the Isolated topology as compared to achievable frequency without noise.

System metric	*Border*	*Bundle*	*Shielded*	*Isolated*
Operating frequency without noise (GHz)	13.9	15.8	14.5	13.9
Operating frequency with noise (GHz)	13.0	11.6	12.9	13.7
Percent decrease	7	27	11	1

Table 5.5: The achievable frequency with noise is 27% lower (maximum difference) for the Bundle topology and 1% lower (minimum difference) for the Isolated topology as compared to achievable frequency without noise.

5.2.1.3 Total Capacitance

Cost metric	*Border*	*Bundle*	*Shielded*	*Isolated*
Total capacitance (fF)	8080	8276	9092	6970
Order of preference	2	3	4	1

Table 5.6: The total capacitance for the 7-port router for the Best Case TSV performance corner and 45 nm technology node. Judging from this, *Isolated* is the most preferred topology as it has the least total capacitance.

Analysis across topologies - From Table 5.6, it can be seen that the Isolated topology has the least total capacitance because the flexibility in TSV placement leads to a more optimal TSV placement. The Border topology has several long wires that traverse across the router area, for e.g., to connect the Down port located in the bottom right corner to TSVs on the top edge. However, this is compensated by TSVs placed along bottom and right edges which result in extremely short wire lengths to the Down port of the router located in the bottom right corner. Hence the total capacitance for the Border topology is lower than Bundle or Shielded topologies. The Shielded topology has the maximum total capacitance due to the

increased capacitance to ground of each TSV as a result of neighbouring shield TSVs which are connected to ground.

Judging from the total capacitance, the *order of preference* of the topologies is as shown in Table 5.6.

Translation to system metrics - The total vertical interconnect capacitance is relevant for system design since it contributes to dynamic power which is due to switching activity. Dynamic power is given by Equation (5.3) where C_{tot} is total capacitance, Vdd is supply voltage and f is frequency of switching. The dynamic power in the vertical interconnect for each topology normalized to the Isolated topology is shown in Table 5.7.

$$P_{dyn} = C_{tot} \times Vdd^2 \times f \tag{5.3}$$

In conclusion, the Border and Bundle topologies result in approximately 1.2 times the dynamic power dissipation compared to the Isolated topology. The Shielded topology which has the maximum total capacitance results in 1.3 times the dynamic power dissipation compared to the Isolated topology.

System metric	*Border*	*Bundle*	*Shielded*	*Isolated*
Dynamic power normalized to the Isolated topology	1.16	1.18	1.34	1

Table 5.7: Dynamic power of the vertical interconnect for each topology normalized to the Isolated topology.

5.2.1.4 Area Penalty

Cost metric	*Border*	*Bundle*	*Shielded*	*Isolated*
Total TSV area (μm^2)	3328	5220	10422	3126
Percent TSV area	4.0	6.2	12.4	3.7
Order of preference	2	3	4	1

Table 5.8: The total area occupied by TSVs and percent TSV area of total router area for the 7-port router for the Best Case TSV performance corner and 45 nm technology node. Judging from the area, Isolated is the most preferred topology as it has the least TSV area penalty.

Analysis across topologies - From Table 5.8, it can be seen that the Isolated topology occupies the minimum area for TSVs with KOZ and the Border topology is the

next in terms of area penalty. The maximum area penalty is seen for the Shielded topology which occupies roughly twice the area of the Bundle topology. Sections 4.1.2 and 4.1.3 cover the analysis of TSV and KOZ area. The percentage of router area utilized by TSVs is significant, 3.7% for Isolated topology and 12.4% for Shielded topology.

Judging from the total area penalty, the *order of preference* of the topologies is as shown in Table 5.8.

Translation to system metrics - The area utilized by the TSVs and the KOZ is an important metric for estimation of die size during system design. After taking into account this additional area due to the TSVs and the KOZ, a decision regarding growing the size of the die can be taken. Alternatively if the area overhead is too high, the re-design of the 3D NOC itself can be considered which means a feedback into architecture-level design.

In conclusion, area penalty incurred due to the TSVs and the KOZ is an important metric for system and architectural level design. The Isolated topology gives the least area overhead for the vertical interface followed by the Border, Bundle and Shielded topologies.

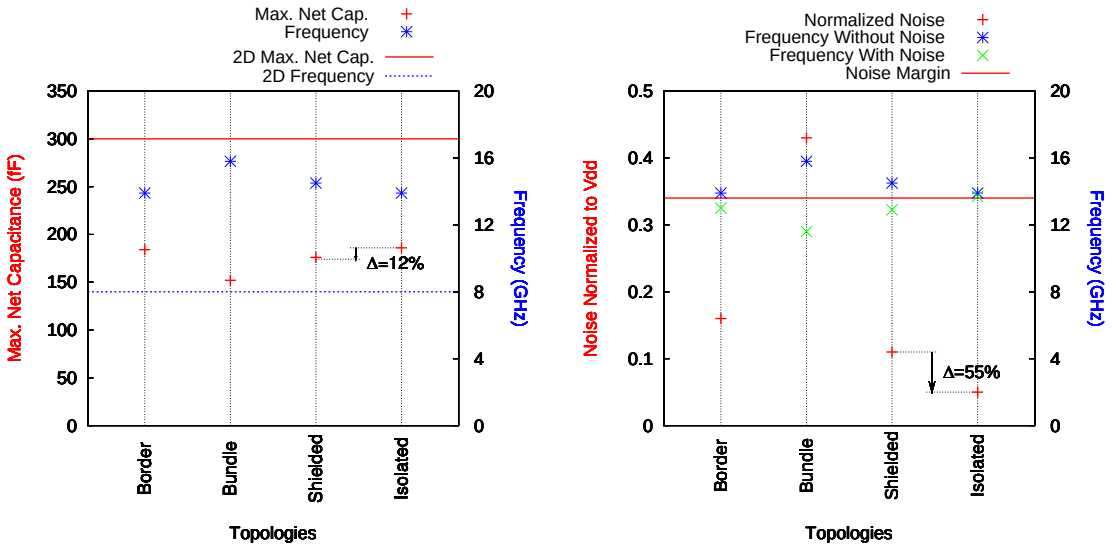
5.2.2 Most preferred topology

As pointed out in Section 5.2.1.2, the Bundle topology has a worst case noise that violates the noise margin and hence it is not a preferred topology. As for the Border topology, Section 5.1 explains the constraints which make it an unsuitable topology for the given router. The remaining topologies i.e., Shielded and Isolated are compared with the help of Figures 5.5 and 5.6 as follows.

Performance metrics: *Max. Net Capacitance* - From Figure 5.5a, it can be seen that the maximum net capacitance of the Shielded topology is 12% lower than that of the Isolated topology. *Capacitive Coupling Noise* - From Figure 5.5b, it can be seen that normalized noise voltage for the Isolated topology is 55% lower than that of the Shielded topology.

Cost metrics: *Total Capacitance* - From Figure 5.6a, it can be seen that total capacitance of the Isolated topology is 23% lower than that of the Shielded topology. *Area Penalty* - From Figure 5.6b, it can be seen that area penalty due to the TSVs and KOZ for the Isolated topology is 70% lower than that of the Shielded topology.

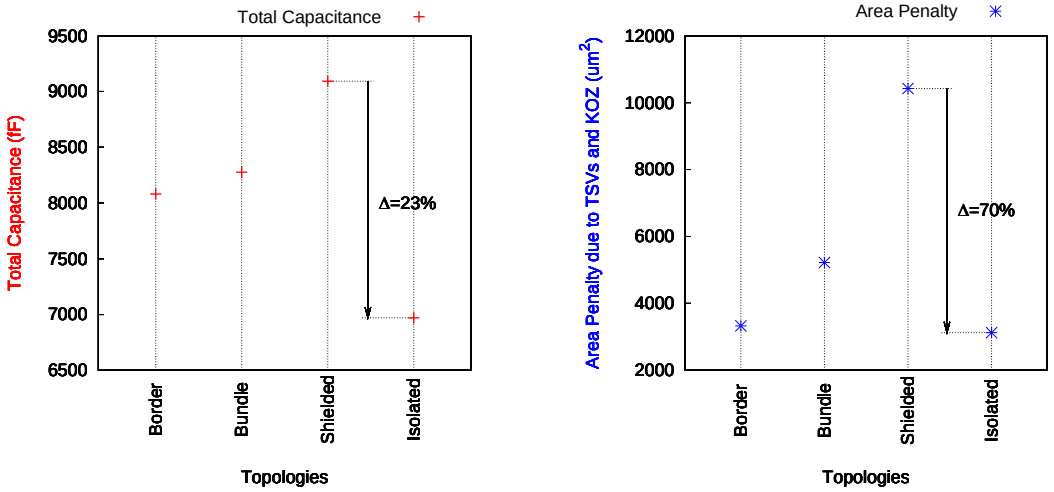
Thus, the *Isolated topology* is the most preferred topology for the given 7-port router for the Best Case TSV performance corner and 45 *nm* technology node. However, as described in Section 4.1.3 the disadvantage of this topology is that it implies maximum disruption of the existing conventional place and route tools. If a migration of existing place and route tools is not a feasible solution for the physical design flow of the given 7-port router, the Shielded topology is the next most preferred topology. The rationale



(a) Max. Net Capacitance.

(b) Capacitive Coupling Noise.

Figure 5.5: Performance metrics for the given 7-port router for 45 nm technology node.



(a) Total Capacitance.

(b) Area Penalty.

Figure 5.6: Cost metrics for the given 7-port router for 45 nm technology node.

behind the Shielded topology is that an enclosure around the closely packed bundle of signal and shield TSVs which also includes the KOZ can be blocked out for placement of devices. This approach involves lower design complexity if existing conventional place and route tools are to be migrated.

5.2.3 Technology Node Comparison

The methodology reports that the Isolated topology cannot be accommodated for the given input floorplan. As a result of the shrinking of the router die area for 32 *nm* compared to 45 *nm* node, only 64 of the 74 TSVs can be placed in the Isolated topology. The results of the remaining 3 topologies for second run of the methodology i.e., for the 32 *nm* technology node are summarized in Table 5.9.

Methodology Results	*Border*	*Bundle*	*Shielded*
Performance metrics			
Min. Capacitance (fF)	62	46	52
Max. Capacitance (fF)	112	118	148
Min. Delay (ps)	17	13	14
Max. Delay (ps)	31	32	41
Min. Slew (ps)	52	40	44
Max. Slew (ps)	94	100	127
Max. ΔDelay due to noise (ps)	7	26	9
Noise induced voltage normalized to Vdd	0.17	0.43	0.11
Cost metrics			
Total capacitance (fF)	5986	5760	7050
Total TSV area (μm^2)	3854	5220	10422
Percent TSV area	9.2	12.4	24.8

Table 5.9: Performance and cost estimation results for the 7-port router for the Best Case TSV technology corner for 32 *nm* technology node.

Similar to 45 *nm* technology, the Border topology is unsuitable for the router for 32 *nm* node since the design constraints explained in Section 5.1 apply for both the nodes. For 32 *nm* technology node, the noise margin is 0.30 compared to 0.34 for 45 *nm* technology node [44]. Since the results for the 32 *nm* node show a noise induced voltage normalized to Vdd of 0.43, the Bundle topology is not feasible similar to the 45 *nm* node.

Thus, the most preferred topology for the 32 *nm* design of the router is the *Shielded topology*. The area penalty due to the TSVs and KOZ for both the nodes is the same with the exception of the Border topology because the TSV Best Case geometry has been employed for both nodes. The reason for a difference in the area penalty for 32 *nm* and 45 *nm* for the Border topology is that the number of TSV rows and the number of TSVs in each row results in different KOZ area.

5.3 Conclusions

- The electrical performance metrics (*Max. Net Capacitance* and *Capacitive Coupling Noise*) and cost metrics (*Total Capacitance* and *Area Penalty*) are compared across the four TSV placement topologies for the Best Case TSV technology corner

for the given 7-port 3D router.

- The achievable operating frequency of vertical interconnect (Table 5.3) for the most preferred Bundle topology is about 2 times that of the horizontal (2D) interconnect and least preferred Isolated topology is about 1.6 times that of the horizontal (2D) interconnect.

- All the topologies except Bundle are within the noise margin for 45 *nm* technology node. The achievable operating frequency decreases due to capacitive coupling. The achievable frequency with noise is 27% lower for the Bundle topology and 1% lower for the Isolated topology as compared to achievable frequency without noise (Table 5.5).

- The Border and Bundle topologies result in approximately 1.2 times the dynamic power dissipation compared to the Isolated topology while this figure is approximately 1.3 for the Shielded topology (Table 5.7).

- Isolated topology gives the least area overhead for the vertical interface followed by the Border, Bundle and Shielded topologies (Table 5.8). The percentage of router area utilized by TSVs is significant, 3.7% for Isolated topology and 12.4% for Shielded topology.

- In general, the metrics *maximum net capacitance* (hence achievable frequency) and *total capacitance* (hence dynamic power) of the interconnect are largely dependent on the floorplan of the stacked tiers.

- In general, the *area penalty* due to the TSVs and KOZ as well as the impact of *capacitive coupling noise* are largely dependent on the TSV placement topology.

- The most preferred topology for the 7-port 3D router given in [35] in 45 *nm* technology node is the Isolated topology (Section 5.2.2). The Shielded topology is the next most preferred topology. A significant advantage of the Isolated topology is its flexibility, enabling optimization of TSV placement. However, such optimization comes at the cost of increased disruptions to existing placement and routing practices as well as algorithms.

- Going from 45 *nm* to 32 *nm* for the 7-port 3D router, shrinking of the die size poses a challenge to finding the optimum TSV placement topology. For the 32 *nm* technology node, the Shielded topology is the most preferred topology (Section 5.2.3).

6 Conclusions and Future Work

This chapter summarizes the thesis by highlighting the objectives that were achieved and providing the larger scope of the work.

6.1 Conclusions

1. The technology parameters were analyzed and those that were found to be critical were abstracted by modeling them to provide a vertical interconnect path model. Also, a few design considerations and guidelines that were identified as critical to the performance and area overhead estimation were analyzed.

   Best Case and *Worst Case* TSV geometries were derived corresponding to minimum and maximum delay through the TSV (Table 3.9). Other TSV model parameters which do not have a significant influence were kept fixed. Dominant parasitic components of devices in 45 nm and 32 nm CMOS technology nodes required for modeling the electrical tier-to-tier path were calculated.

   The presented tier-to-tier vertical path model was validated through actual circuit simulation with inverters. A wide accuracy range (83% to 90%) was observed depending on the capacitive wire load.

   Design considerations for placement of TSVs such as capacitive coupling and TSV Keep-Out-Zone were derived (Sections 4.1.1 and 4.1.2).

2. Performance and cost estimation of TSV-based vertical interconnect in the context of 3D architecture exploration for high performance digital systems was achieved using the derived models and design guidelines.

   Four topologies were selected based on trade-offs between one or more performance and cost metrics, namely, Border, Bundle, Shielded and Isolated (Section 4.1.4). These represent a few extreme points in the exploration design space for TSV placement topologies. The performance and cost metrics of other topologies considered during the exploration fall in between these and can be interpolated.

   Flexibility was achieved by accepting design-specific inputs from user as well as selection of the 3D stacking granularity and circuit technology node at the input of the methodology. *Parameterizability* and *scalability* were achieved in an efficient manner within an integrated SystemC simulation environment. By constraining the placement to fixed structures, complexity of algorithms was kept minimal to enable fast exploration at an early stage of design.

3. An approach was shown for a 3D system simulation methodology that abstracts important technology parameters, provides results for electrical performance and cost such these can enables more accurate system-level design.

   The performance metrics (*Max. Net Capacitance* and *Capacitive Coupling Noise*) and the cost metrics (*Total Capacitance* and *Area Penalty*) were compared across the four TSV placement topologies for the Best Case TSV technology corner for the given case of a 7-port 3D router.

   The achievable operating frequency of vertical interconnect without noise (Table 5.3) was about 2 times (highest) that of the horizontal (2D) interconnect for the Bundle topology and about 1.6 times (lowest) that of the horizontal (2D) interconnect for the Isolated topology.

   All the topologies except Bundle had a worst case noise within the noise margin for 45 *nm* technology node (Section 5.2.1.2).

   The Border, Bundle and Shielded topologies resulted in approximately 1.2 times the dynamic power dissipation compared to the Isolated topology (Table 5.7).

   Isolated topology gave the least area overhead for the vertical interface followed by the Border, Bundle and Shielded topologies (Table 5.8).

   The most preferred topology for the 7-port 3D router given in [35] in 45 *nm* technology node is the Isolated topology (Section 5.2.2). The Shielded topology is the next most preferred topology.

   Going from 45 *nm* to 32 *nm* for the 7-port 3D router, shrinking of the die size poses a challenge to finding the optimum TSV placement topology. For the 32 *nm* technology node, the Shielded topology is the most preferred topology (Section 5.2.3).

In conclusion, the objectives defined in 1.2 were satisfactorily achieved. With that a methodology was proposed which incorporates a novel idea of exploring 3D interconnect technology options, namely, TSV technology corners and TSV placement topologies. Other dimensions added to the exploration were the stacking granularity and the circuit technology for the two tiers.

6.2 Future Work

The methodology in this work was proposed keeping in mind architecture exploration and system simulation of 3D stacked ICs. Thus the future scope of this work is to incorporate this methodology into such a system simulation framework. Future work also involves updating the TSV models and design guidelines to keep up with advancements in technology.

1. The methodology can be preceded with a step wherein 3D architecture space exploration is performed. Such a step would typically involve intelligent partitioning of the design and decision making on the placement of blocks in the stack. The performance of each such 3D stack can be potentially simulated by extending existing 2D design tools to incorporate the proposed methodology.

2. 3D-Wafer Level Packaging (Section 3.2.1) can be implemented to add another level of stacking granularity to the proposed exploration methodology. Advanced architectures for TSVs can be implemented and added to the TSV technology options to be explored, e.g. coaxial TSVs conceptualized in [27].

3. In order to make the methodology more robust, some other physical effects that can be evaluated are thermal conduction through TSVs [45] and its influence on performance/cost metrics as well as design considerations for TSV-to-device capacitive coupling noise [27].

3D Integration Technology Roadmaps

A

A.1 3D Wafer level packaging (3D-WLP)

3D-WLP is a 3D technology for bond-level stacking. The 3D-TSV roadmap should therefore follow the chip I/O bondpad Roadmap as shown in Table A.1.

A.2 3D System on Chip (3D-SOC)

3D-SOC for connecting at the global interconnect level is 3D stacking technology for IP blocks to build a 3D System on Chip (3D-SOC). This technology allows for W2W, D2W and D2D stacking. This 3D-TSV process is typically integrated in the Si-wafer fabrication line. The 3D stacking process is generally done outside the standard Si-process line. The Roadmap is as shown in Table A.2.

A.3 3D Stacked IC (3D-SIC)

3D-SIC is a 3D stacking technology for intermediate interconnect level. An example of this is 3D stacking of smaller circuit blocks. This technology is mainly for W2W stacking. Both the 3D-TSV process and the 3D stacking are typically integrated in the Si-wafer fabrication line. The Roadmap is as shown in Table A.3.

Year of Production	2010	2012	2015
1-row wedge-bond pitch (μm)	20	20	20
1-row ball pitch (μm)	40	35	25
2-row staggered pitch (μm)	45	40	40
Three-tier pitch (μm)	60	50	45
Area array flip-chip (μm)	130	110	100

Table A.1: 3D-WLP via pitch requirement based on chip pad pitch trend[10].

Global Level, W2W, D2W or D2D 3D-stacking	2009-2012	2012-2015
Minimum TSV diameter (μm)	4-8	2-4
Minimum TSV pitch (μm)	8-16	4-8
Minimum TSV depth (μm)	20-50	20-50
Maximum TSV aspect ratio	5:1-10:1	10:1-20:1
Bonding overlay accuracy (μm)	1.0-1.5	0.5-1.0
Minimum contact pitch (thermocompression) (μm)	10	5
Minimum contact pitch (solder μbump) (μm)	20	10
Number of tiers	2-3	2-4

Table A.2: Global interconnect level 3D-SOC Roadmap [10].

Intermediate Level, W2W 3D-stacking	2009-2012	2012-2015
Minimum TSV diameter (μm)	1-2	0.8-1.5
Minimum TSV pitch (μm)	2-4	1.6-3.0
Minimum TSV depth (μm)	6-10	6-10
Maximum TSV aspect ratio	5:1-10:1	10:1-20:1
Bonding overlay accuracy (μm)	1.0-1.5	0.5-1.0
Minimum contact pitch (μm)	2-3	2-3
Number of tiers	2-3	8-16 (DRAM)

Table A.3: Intermediate interconnect level 3D-SIC Roadmap [10].

TSV interconnect Modeling

B

B.1 3D-WLP TSV Model

The TSV RLC model implemented is based on the closed form equations proposed by Kim et. al [24]. The electrical model proposed in their work is shown in Figure B.1. The capacitances $C_{Underfill}$, C_{IMD} and C_{Bottom} are formed due to electric fields between signal and ground bumps. As a first step to implement a basic model of an isolated signal TSV with bumps, these are not included in the implementation. Also, substrate leakage is not taken into consideration. Thus, the TSV model implemented comprises of a resistance equal to $R_{TSV} + R_{Bump}$, an inductance equal to $L_{TSV} + L_{Bump}$ and the two capacitances connected on either side as shown in Figure B.1. These capacitances i.e., $C_{Insulator} + C_{Bump1}$ and $C_{Insulator} + C_{Bump2}$ are connected to ground.

The values for geometry and material parameters assumed for this implementation are given in Table B.1.

Geometry Parameter (μm)	Value	Material Parameter	Value
TSV diameter d_{TSV}	10	Conductivity of Si substrate σ_{Si} (S/m)	10
TSV height h_{TSV}	10	Resistivity of TSV fill metal ρ_{TSV} $(\Omega.m)$	1.68e-8
TSV Pitch p_{TSV}	90	Resistivity of Bump ρ_{Bump} $(\Omega.m)$	1.68e-8
TSV Insulator thickness t_{ox}	1	Resistivity of RDL ρ_{RDL} $(\Omega.m)$	1.68e-8
Bump diameter d_{Bump}	30	Relative permittivity of Si substrate $\epsilon_{r,Si}$	11.9
Bump height h_{Bump}	10	Relative permittivity of Insulator $\epsilon_{r,ox}$	4
IMD height h_{IMD}	7	Relative permittivity of IMD $\epsilon_{r,IMD}$	4
Bottom SiO2 thickness $t_{ox,bot}$	0.5	Relative permittivity of Underfill $\epsilon_{r,Und}$	7

Table B.1: Model parameters and their values used for the implementation of an isolated signal TSV with Bump based on [24] for 3D-WLP.

The capacitance of the TSV $C_{Insulator}$ (F) is given in Equation (B.1).

$$C_{Insulator} = \frac{1}{2}\left\{2\pi\epsilon_{ox}\frac{h_{TSV} - h_{IMD}}{\ln(\frac{d_{TSV}/2+t_{ox}}{d_{TSV}/2})}\right\} \tag{B.1}$$

The capacitance of the Bumps C_{Bump1} (F) and C_{Bump2} (F) are given in Equations

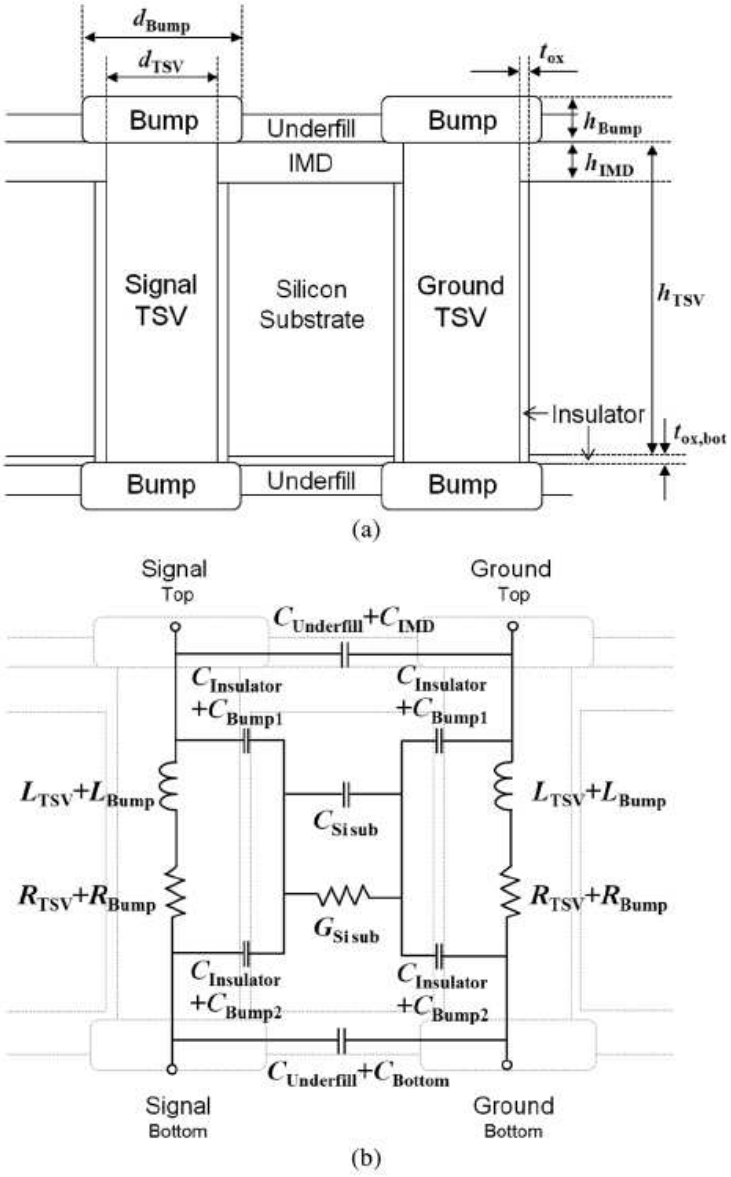


Figure B.1: (a) Structure and parameters of a pair of single ended TSVs with bumps and (b) electrical model of the structure shown in (a) [24].

(B.2) and (B.3) respectively.

$$C_{Bump1} = \pi\epsilon_0\epsilon_{r,IMD}\frac{\left\{(d_{Bump}/2)^2 - (d_{Bump}/2 + t_{ox})^2\right\}}{h_{IMD}} \tag{B.2}$$

$$C_{Bump2} = \pi\epsilon_0\epsilon_{r,ox}\frac{\left\{(d_{Bump}/2)^2 - (d_{Bump}/2 + t_{ox,bot})^2\right\}}{t_{ox,bot}} \tag{B.3}$$

The resistance of TSV and Bump R_{TSV} (Ω) and R_{Bump} (Ω) are given in Equations (B.4) and (B.8) respectively.

$$R_{TSV} = \sqrt{(R_{dc,TSV})^2 + (R_{ac,TSV})^2} \tag{B.4}$$

where,

$$R_{dc,TSV} = \rho_{TSV} \times \frac{h_{TSV}}{\pi \times (\frac{d_{TSV}}{2})^2} \tag{B.5}$$

$$R_{ac,TSV} = \left(p_{TSV} \times \frac{h_{TSV}}{2\pi \times \frac{d_{TSV}}{2} \times \delta_{skindepth,TSV} - \pi(\delta_{skindepth,TSV})^2}\right) \tag{B.6}$$

$$\delta_{skindepth,TSV} = \frac{1}{\sqrt{\pi f \sigma_{TSV}}} \tag{B.7}$$

$$R_{Bump} = \sqrt{(R_{dc,Bump})^2 + (R_{ac,Bump})^2} \tag{B.8}$$

where,

$$R_{dc,Bump} = \rho_{Bump} \times \frac{h_{Bump}}{\pi \times (\frac{d_{Bump}}{2})^2} \tag{B.9}$$

$$R_{ac,Bump} = \left(p_{Bump} \times \frac{h_{Bump}}{2\pi \times \frac{d_{Bump}}{2} \times \delta_{skindepth,Bump} - \pi(\delta_{skindepth,Bump})^2}\right) \tag{B.10}$$

$$\delta_{skindepth,Bump} = \frac{1}{\sqrt{\pi f \sigma_{Bump}}} \tag{B.11}$$

The inductance of TSV and Bump L_{TSV} (H) and L_{Bump} (H) are given in Equations (B.12) and (B.13) respectively.

$$L_{TSV} = \frac{1}{2}\left\{\frac{\mu_0}{2\pi} \times h_{TSV} \times \ln(\frac{p_{TSV}}{d_{TSV}/2})\right\} \tag{B.12}$$

$$L_{Bump} = \frac{1}{2}\left\{\frac{\mu_0}{2\pi} \times h_{Bump} \times \ln(\frac{p_{TSV}}{d_{Bump}/2})\right\} \tag{B.13}$$

The resulting values of the parasitic components for the geometry and material parameters in Table B.1 are summarized in Table B.2. For simulating the delay and

Parasitic component	Value
R_{TSV} $(m\Omega)$	20
R_{Bump} $(m\Omega)$	0.2
L_{TSV} (pH)	29.0
L_{Bump} (pH)	1.8
$C_{Insulator}$ (fF)	57.0
C_{Bump1} (fF)	3.2
C_{Bump2} (fF)	42.7

Table B.2: Parasitic component values for the model of an isolated signal TSV with Bump based on [24] for 3D-WLP.

slew through the TSV, R_{dr} of 327 Ω is assumed which is the ON resistance of a CMOS 40x Inverter in 45 nm technology (Table 3.12). For terminating the TSV with a load, a capacitance of 25 fF was assumed. The input signal is a step function with rise time of 10 ps. The resulting delay and slew observed are 18 ps and slew is 55 ps respectively.

B.2 3D-SIC/3D-SOC TSV Model

The electrical RLC model implemented is based on the closed form equations proposed by Savidis and Friedman in [18]. The geometry and material parameters are given in Table B.3.

Parameter	Symbol
TSV diameter (m)	D
TSV radius (m)	R
TSV pitch (m)	P
TSV length (m)	L
Spacing between two TSVs (m)	S
TSV thickness of dielectric layer (m)	t_{diel}
Distance of TSV from ground plane (m)	S_{gnd}
Conductivity of Si substrate (S/m)	σ_{Si}
Resistivity of TSV fill metal $(\Omega.m)$	ρ_m
Doping concentration of p-type Si substrate $(/m^3)$	N_A
Permittivity of Si substrate (F/m)	ϵ_{sub}
Permittivity of dielectric layer (F/m)	ϵ_{diel}
Permeability of free space (H/m)	μ_0
Clock edge (s)	τ

Table B.3: 3D-SOC/3D-SIC Model parameters with their symbols.

B.2.1 Resistance of TSV

Resistance of the TSV at DC R_{DC} (Ω) and at high frequency (HF) R_{HF} (Ω) is given in (B.14) and (B.15) respectively.

$$R_{DC} = \frac{\rho_m L}{\pi R^2} \tag{B.14}$$

$$R_{HF} = \begin{cases} \alpha \frac{\rho_m L}{\pi[R^2-(R-\delta)^2]} & \text{if } \delta < R \\ \alpha \frac{\rho_m L}{\pi R^2} & \text{if } \delta \geq R \end{cases} \tag{B.15}$$

where δ (m) is skin depth given by

$$\delta = \frac{1}{\sqrt{\pi(1/\tau)\mu_0(1/\rho_m)}} \tag{B.16}$$

and α is fitting paramter given by

$$\alpha = \begin{cases} 0.0472 D_{\mu m}^{0.2831} \ln(\frac{L}{D}) + 2.4712 D_{\mu m}^{-0.269} & \text{if } \delta < R \\ 0.0091 D_{\mu m}^{1.0806} \ln(\frac{L}{D}) + 1.0518 D_{\mu m}^{0.092} & \text{if } \delta \geq R \end{cases} \tag{B.17}$$

B.2.2 Inductance of TSV

Expressions for DC abd HF partial self (L_{11}) (H) and mutual (L_{21}) (H) inductances of the TSV are provided in B.18 and B.19 respectively.

$$DC: \begin{cases} L_{11} = \alpha \frac{\mu_0}{2\pi} \left[\ln(\frac{L+\sqrt{L^2+R^2}}{R}) L + R - \sqrt{L^2+R^2} + \frac{L}{4} \right] \\ L_{21} = \beta \frac{\mu_0}{2\pi} \left[\ln(\frac{L+\sqrt{L^2+P^2}}{P}) L + P - \sqrt{L^2+P^2} \right] \end{cases} \tag{B.18}$$

$$HF: \begin{cases} L_{11} = \alpha \frac{\mu_0}{2\pi} |\ln(\frac{2L}{R}) - 1| L \\ L_{21} = \beta \frac{\mu_0}{2\pi} \left[\ln(\frac{L+\sqrt{L^2+P^2}}{P}) L + P - \sqrt{L^2+P^2} \right] \end{cases} \tag{B.19}$$

where α and β are given by B.20 and B.21

$$\alpha = \begin{cases} 1 - e^{\frac{-4.3L}{D}} & \text{if } f = DC \\ 0.94 + 0.52 e^{-10|\frac{L}{D}-1|} & \text{if } f = HF \end{cases} \tag{B.20}$$

$$\beta = \begin{cases} 1 & \text{if } f = DC \\ 0.1535 \ln(\frac{L}{D}) + 0.592 & \text{if } f = HF \end{cases} \tag{B.21}$$

B.2.3 Capacitance of TSV

Capacitance of the TSV is given in B.22

$$C = \alpha\beta \frac{\epsilon_{diel}}{t_{diel} + \frac{\epsilon_{diel}}{\epsilon_{sub}} x_{dTp}} 2\pi RL \tag{B.22}$$

where α and β are given by B.23 and B.24

$$\alpha = \left(-0.0351\frac{L}{D} + 1.5701 \right) {S_{gnd}}_{\mu m}^{\;\; 0.0111\frac{L}{D} - 0.1997} \tag{B.23}$$

$$\beta = 5.8934 {D_{\mu m}}^{-0.553} \left(\frac{L}{D} \right)^{-(0.0031 D_{\mu m} + 0.43)} \tag{B.24}$$

and depletion region depth in p-type silicon x_{dTp} is given by

$$x_{dTp} = \sqrt{\frac{4\epsilon_{sub}\phi_{f_p}}{qN_A}} \tag{B.25}$$

$$\phi_{f_p} = V_{th} \ln(\frac{N_A}{n_i}) \tag{B.26}$$

The expression for coupling capacitance between two 3D vias is given in B.27

$$C_c = 0.4\alpha\beta\gamma \frac{\epsilon_{sub}}{S} \pi DL \tag{B.27}$$

where α, β and γ are given by

$$\alpha = 0.225 \ln \left(0.97\frac{L}{D} \right) + 0.53 \tag{B.28}$$

$$\beta = 0.5711 \left(\frac{L}{D} \right)^{-0.988} \ln({S_{gnd}}_{\mu m}) + \left(0.85 - e^{-\frac{L}{D} + 1.3} \right) \tag{B.29}$$

$$\gamma = \begin{cases} 1 & \text{if } \frac{S}{D} \leq 1 \\ \zeta \left[\ln(\frac{L}{D} + 4e^{-\frac{S_{\mu m}}{9}} + 2.9) - 10.625 {S_{\mu m}}^{-0.51} \right] & \text{if } \frac{S}{D} > 1 \end{cases} \tag{B.30}$$

where ζ is given by

$$\zeta = \left(1 + e^{[(0.5 + |\frac{P}{D} - 4|)\frac{L}{D}]} \right) \tag{B.31}$$

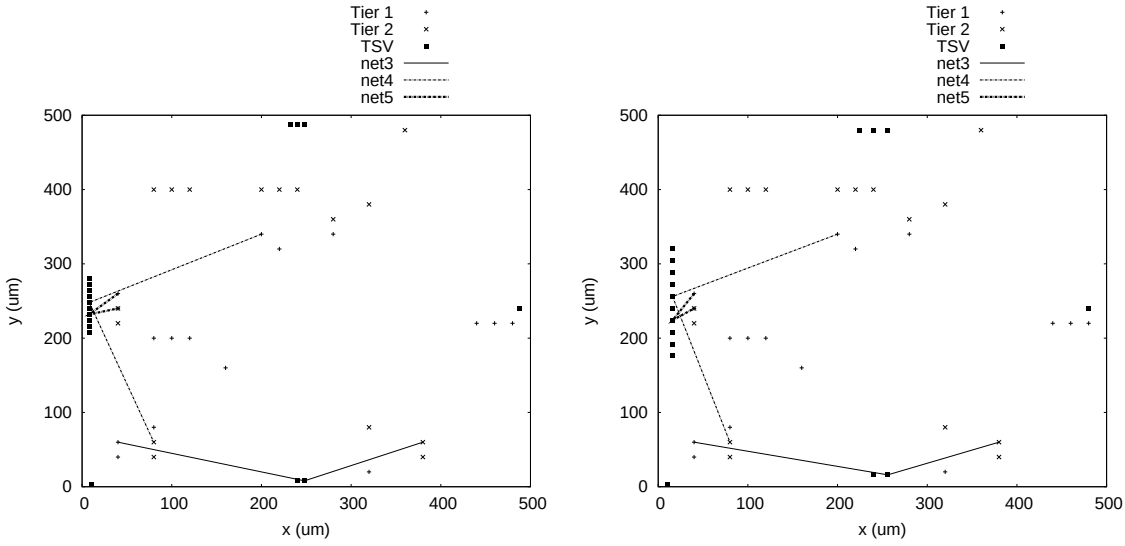
C Methodology Test Case Results

C.1 Border topology

Figure C.1 shows the floorplans for Best Case and Worst Case TSV geometries for the Border topology for the considered test case. Tables C.1-C.5 provide the results for performance estimation and area penalty for the same.

C.2 Bundle topology

Figure C.2 shows the floorplans for Best Case and Worst Case TSV geometries for the Bundle topology for the considered test case. Tables C.6-C.10 provide the results for



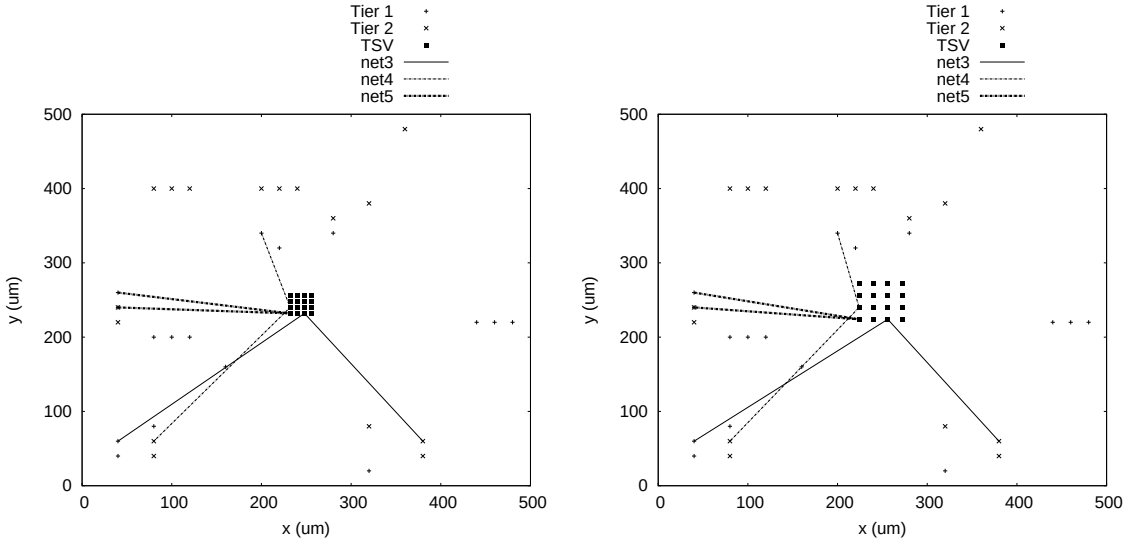
(a) Best Case TSV geometry.

(b) Worst Case TSV geometry.

Figure C.1: Floorplan for the *Border* topology.

Net	Delay(ps)	Slew(ps)	T1 Cap(fF)	TSV Cap(fF)	T2 Cap(fF)	Net Cap(fF)
net1	29	90	47	16	55	118
net2	15	46	16	16	28	60
net3	26	78	53	16	35	104
net4	31	93	55	16	53	124
net5	8	24	10	16	6	32
net6	22	68	39	16	35	90
net7	20	62	51	16	15	82
net8	34	107	92	16	30	138
net9	34	106	59	16	63	138
net10	30	94	81	16	25	122
net11	50	153	88	16	71	175
net12	52	160	100	16	67	183
net13	55	167	95	16	81	192
net14	25	78	34	16	42	92
net15	23	71	17	16	51	84
net16	28	84	39	16	44	99
Net with Min. Capacitance:						
net5	8	24	10	16	6	32
Net with Max. Capacitance:						
net13	55	167	95	16	81	192

Table C.1: Delay and slew for Best Case for all the nets in the vertical interconnect.



(a) Best Case TSV geometry.

(b) Worst Case TSV geometry.

Figure C.2: Floorplan for the *Bundle* topology.

Net	Delay(ps)	Slew(ps)	T1 Cap(fF)	TSV Cap(fF)	T2 Cap(fF)	Net Cap(fF)
net1	36	112	44	53	52	149
net2	23	72	16	53	28	97
net3	33	103	51	53	33	137
net4	38	118	53	53	51	157
net5	17	53	11	53	7	71
net6	30	92	35	53	35	123
net7	29	89	51	53	15	119
net8	43	133	91	53	28	172
net9	42	131	59	53	59	171
net10	38	120	76	53	27	156
net11	60	185	87	53	75	215
net12	61	188	102	53	63	218
net13	67	206	98	53	86	237
net14	34	105	37	53	35	125
net15	35	108	17	53	57	127
net16	36	112	44	53	36	133
Net with Min. Capacitance:						
net5	17	53	11	53	7	71
Net with Max. Capacitance:						
net13	67	206	98	53	86	237

Table C.2: Delay and slew for Worst Case for all the nets in the vertical interconnect.

Direction	Best Case			Worst Case		
	Delay min.	Delay max.	%ΔVoltage	Delay min.	Delay max.	%ΔVoltage
Tier 1 to 2	5	10	16	13	17	7
Tier 2 to 1	5	12	17	14	19	7

Table C.3: Impact of coupling capacitance induced noise on TSV signal.

Best Case	Worst Case
1833	2407

Table C.4: Total capacitance of vertical interface (fF).

Best Case	Worst Case
811	2487

Table C.5: Total area penalty of TSVs with KOZ (μm^2).

Net	Delay(ps)	Slew(ps)	T1 Cap(fF)	TSV Cap(fF)	T2 Cap(fF)	Net Cap(fF)
net1	42	129	79	16	71	166
net2	30	91	58	16	46	120
net3	38	116	75	16	60	151
net4	27	81	26	16	66	108
net5	24	75	43	16	39	98
net6	19	57	18	16	42	76
net7	30	91	62	16	42	120
net8	21	65	43	16	28	87
net9	26	78	23	16	66	105
net10	29	90	38	16	65	119
net11	27	84	39	16	44	99
net12	27	84	44	16	39	99
net13	28	86	55	16	31	102
net14	30	92	37	16	55	108
net15	33	101	43	16	60	119
net16	29	91	36	16	54	106
Net with Min. Capacitance:						
net6	19	57	18	16	42	76
Net with Max. Capacitance:						
net1	42	129	79	16	71	166

Table C.6: Delay and slew for Best Case for all the nets in the vertical interconnect.

performance estimation and area penalty for the same.

C.3 Shielded topology

Figure C.3 shows the floorplans for Best Case and Worst Case TSV geometries for the Shielded topology for the considered test case. Tables C.11-C.15 provide the results for performance estimation and area penalty for the same.

C.4 Isolated topology

Figure C.4 shows the floorplans for Best Case and Worst Case TSV geometries for the Isolated topology for the considered test case. Tables C.16-C.20 provide the results for

Net	Delay(ps)	Slew(ps)	T1 Cap(fF)	TSV Cap(fF)	T2 Cap(fF)	Net Cap(fF)
net1	51	157	79	53	71	203
net2	37	115	56	53	44	153
net3	46	142	75	53	57	185
net4	34	105	24	53	64	141
net5	33	101	43	53	39	135
net6	26	80	16	53	40	109
net7	38	116	60	53	40	153
net8	30	93	46	53	25	124
net9	33	100	18	53	64	135
net10	38	117	44	53	59	156
net11	37	115	34	53	49	136
net12	37	115	41	53	42	136
net13	39	119	58	53	31	142
net14	39	119	39	53	50	142
net15	43	133	46	53	57	156
net16	40	124	41	53	52	146
Net with Min. Capacitance:						
net6	26	80	16	53	40	109
Net with Max. Capacitance:						
net1	51	157	79	53	71	203

Table C.7: Delay and slew for Worst Case for all the nets in the vertical interconnect.

Direction	Best Case			Worst Case		
	Delay min.	Delay max.	%ΔVoltage	Delay min.	Delay max.	%ΔVoltage
Tier 1 to 2	5	28	42	13	33	22
Tier 2 to 1	5	31	43	14	36	22

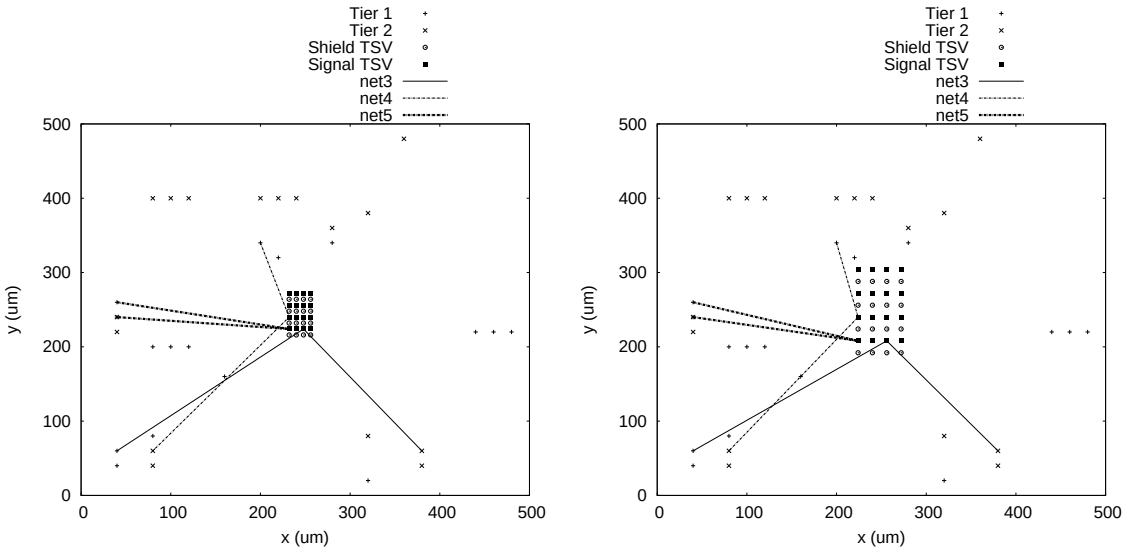
Table C.8: Impact of coupling capacitance induced noise on TSV signal.

Best Case	Worst Case
1783	2352

Table C.9: Total capacitance of vertical interface (fF).

Best Case	Worst Case
1040	3630

Table C.10: Total area penalty of TSVs with KOZ (μm^2).



(a) Best Case TSV geometry.

(b) Worst Case TSV geometry.

Figure C.3: Floorplan for the *Shielded* topology.

Net	Delay(ps)	Slew(ps)	T1 Cap(fF)	TSV Cap(fF)	T2 Cap(fF)	Net Cap(fF)
net1	45	138	79	28	71	178
net2	32	99	58	28	46	132
net3	40	123	74	28	59	161
net4	29	90	26	28	66	120
net5	28	86	45	28	41	114
net6	21	62	28	28	40	84
net7	32	97	60	28	40	128
net8	24	74	44	28	27	99
net9	29	87	21	28	67	116
net10	32	98	41	28	62	131
net11	30	94	37	28	46	111
net12	30	94	44	28	39	111
net13	31	96	56	28	30	114
net14	33	101	40	28	51	119
net15	36	112	46	28	57	131
net16	32	100	39	28	51	118
Net with Min. Capacitance:						
net6	21	62	16	16	40	84
Net with Max. Capacitance:						
net1	45	138	79	16	71	178

Table C.11: Delay and slew for Best Case for all the nets in the vertical interconnect.

Net	Delay(ps)	Slew(ps)	T1 Cap(fF)	TSV Cap(fF)	T2 Cap(fF)	Net Cap(fF)
net1	54	166	79	65	71	215
net2	40	125	56	65	44	165
net3	47	146	72	65	54	191
net4	37	113	24	65	64	153
net5	37	115	47	65	43	155
net6	27	84	13	65	37	115
net7	40	123	57	65	42	164
net8	33	101	49	65	22	136
net9	35	109	15	65	67	147
net10	41	126	51	65	52	168
net11	38	119	35	65	52	152
net12	37	115	41	65	42	148
net13	39	119	61	65	28	154
net14	39	119	45	65	43	153
net15	43	133	52	65	51	168
net16	40	124	47	65	46	158
Net with Min. Capacitance:						
net6	25	76	13	53	37	103
Net with Max. Capacitance:						
net1	51	157	79	53	71	203

Table C.12: Delay and slew for Worst Case for all the nets in the vertical interconnect.

Direction	Best Case			Worst Case		
	Delay min.	Delay max.	%ΔVoltage	Delay min.	Delay max.	%ΔVoltage
Tier 1 to 2	5	13	11	13	19	5
Tier 2 to 1	5	14	11	14	22	5

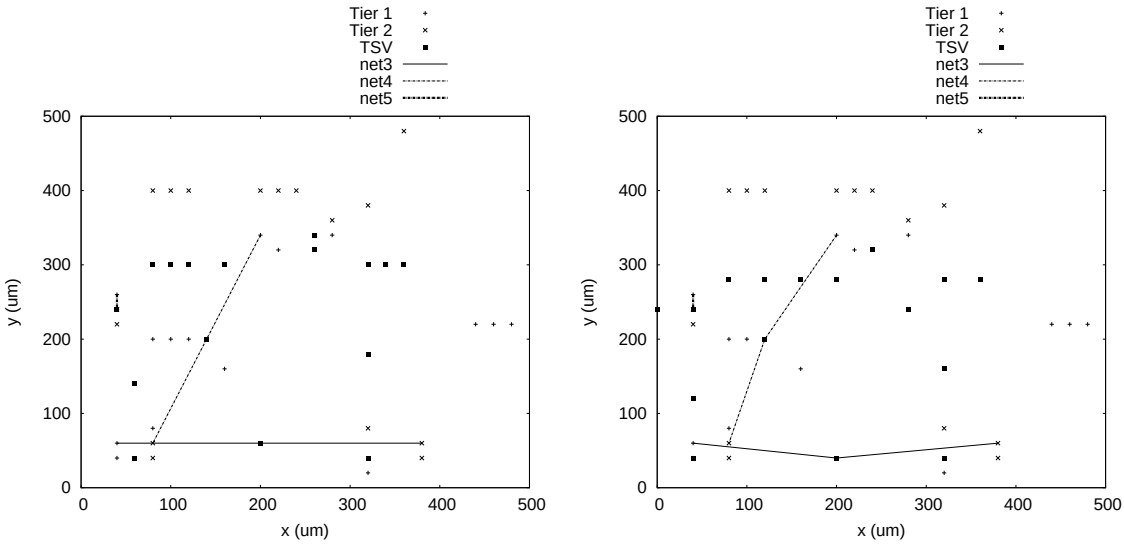
Table C.13: Impact of coupling capacitance induced noise on TSV signal.

Best Case	Worst Case
1967	2542

Table C.14: Total capacitance of vertical interface (fF).

Best Case	Worst Case
2072	7486

Table C.15: Total area penalty of TSVs with KOZ (μm^2).



(a) Best Case TSV geometry.

(b) Worst Case TSV geometry.

Figure C.4: Floorplan for the *Isolated* topology.

performance estimation and area penalty for the same.

Net	Delay(ps)	Slew(ps)	T1 Cap(fF)	TSV Cap(fF)	T2 Cap(fF)	Net Cap(fF)
net1	6	19	3	16	3	22
net2	7	22	3	16	7	26
net3	20	62	31	16	35	82
net4	23	71	39	16	39	94
net5	6	17	3	16	0	19
net6	12	35	11	16	19	46
net7	13	38	15	16	19	50
net8	21	65	35	16	35	86
net9	23	71	39	16	39	94
net10	29	90	51	16	51	118
net11	27	84	39	16	43	98
net12	27	84	39	16	43	98
net13	27	84	39	16	43	98
net14	15	47	19	16	19	54
net15	15	47	19	16	19	54
net16	15	47	19	16	19	54
Net with Min. Capacitance:						
net5	6	17	3	16	0	19
Net with Max. Capacitance:						
net10	29	90	51	16	51	118

Table C.16: Delay and slew for Best Case for all the nets in the vertical interconnect.

Net	Delay(ps)	Slew(ps)	T1 Cap(fF)	TSV Cap(fF)	T2 Cap(fF)	Net Cap(fF)
net1	14	44	0	53	7	60
net2	15	47	3	53	7	63
net3	31	96	35	53	39	127
net4	32	98	43	53	35	131
net5	14	41	3	53	0	56
net6	20	62	3	53	27	83
net7	21	64	15	53	19	87
net8	30	92	31	53	39	123
net9	32	98	43	53	35	131
net10	38	116	31	53	71	155
net11	37	115	35	53	47	135
net12	37	115	39	53	43	135
net13	37	115	35	53	47	135
net14	27	83	19	53	27	99
net15	25	77	7	53	31	91
net16	25	77	15	53	23	91
Net with Min. Capacitance:						
net1	14	44	0	53	7	60
Net with Max. Capacitance:						
net10	38	116	31	53	71	155

Table C.17: Delay and slew for Worst Case for all the nets in the vertical interconnect.

Direction	Best Case			Worst Case		
	Delay min.	Delay max.	%ΔVoltage	Delay min.	Delay max.	%ΔVoltage
Tier 1 to 2	5	6	5	13	14	2
Tier 2 to 1	5	7	5	14	16	2

Table C.18: Impact of coupling capacitance induced noise on TSV signal.

Best Case	Worst Case
1093	1702

Table C.19: Total capacitance of vertical interface (fF).

Best Case	Worst Case
676	1763

Table C.20: Total area penalty of TSVs with KOZ (μm^2).

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