High-Precision ΣΔ Modulator with Improved Linearity

by

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Introduction

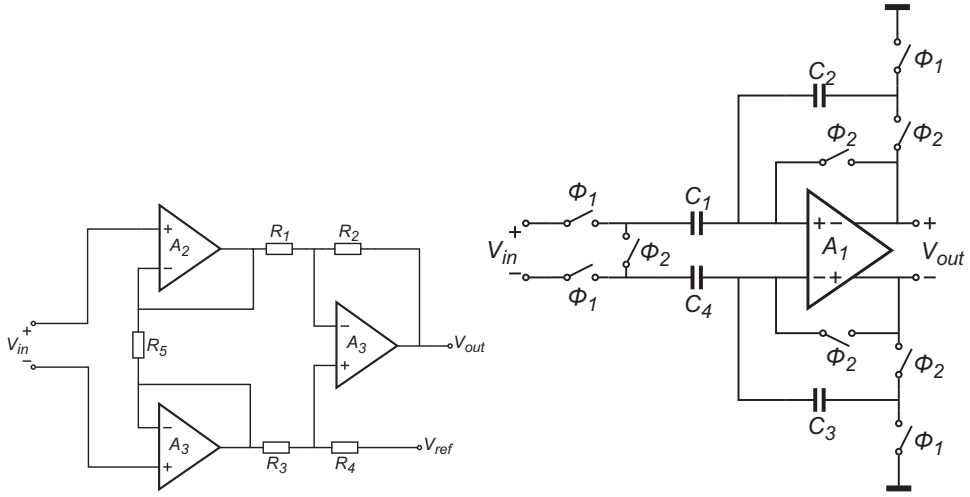
1.1 Preface

The output of sensor systems is often a weak differential signal accompanied by a strong common-mode (CM) signal. Amplifiers designed to amplify such weak signals are known as instrumentation amplifiers (IAs). The general requirements for IA are very low DC offset, low drift, low noise, very high open-loop gain, very high common-mode rejection ration, and very high input impedance. There are three general ways to implement instrumentation amplifiers [1]; IA with voltage feedback via resistors, switch-capacitor IA and IA with current-mode feedback via transconductors.

The most well-known example of the first topology consists of three Op-Amps [2], two of which are arranged to buffer the input nodes and one which generates the desired output as shown in Fig. 1.1a. This architecture has a good linearity but it also has some disadvantages. For example two high-gain low-noise Op-Amps are needed which makes this structure inefficient in terms of power consumption.

The second topology, uses switched-capacitor circuits to overcome the common mode level issue [3]. A simple schematic of this IA is shown in Fig. 1.1b. To achieve low offset, auto-zero methods can be applied since the switches and capacitors are already present in the implementation. However one problem is that it can not be used for continuous-time applications and the other disadvantage is that the CM level can be as high as 30V in some applications. Lastly not all technologies support capacitors capable of handling such voltages.

The third topology generally uses transconductances in the input and



(a) (b)

Figure 1.1: (a)Resistive feedback and (b)Switched-capacitor instrumentation amplifier

feedback paths. A simplified schematic for a current-feedback IA is shown in Fig. 1.2. In this class of instrumentation amplifiers the CM input and output levels are defined independently. As an example, an IA with this topology has been defined for a high-side current-sensing application where the input CM voltage range is from 1.9V to 30V [4]. Its common-mode rejection ratio (CMRR) is determined by isolation and better CMRR can be achieved compared to resistive feedback IAs. In the same work, a CMRR of about 140dB is achieved which with the other topologies would require component trimming.

To process the output of a sensor the general solution is to amplify the weak sensing signal with an instrumentation amplifier and then convert the resulting signal to a digital signal. Hence one IA and one analog-to-digital converter (ADC) are required in the read-out circuitry of a sensor as shown in Fig. 1.3. In this way the noise and accuracy requirements on the ADC are more relaxed and the resolution and speed of the ADC determine which type of data converters suits for the application.

One alternative way to extract the analog signal in sensor applications might be to use high-precision ADC directly after the sensor. This puts stringent specifications on the ADC such as very low input offset, high CMRR, high input impedance and all other requirements mentioned above for the instrumentation amplifier. At first glance it might seem very difficult to design such an ADC, but a survey over the different classes of instru-

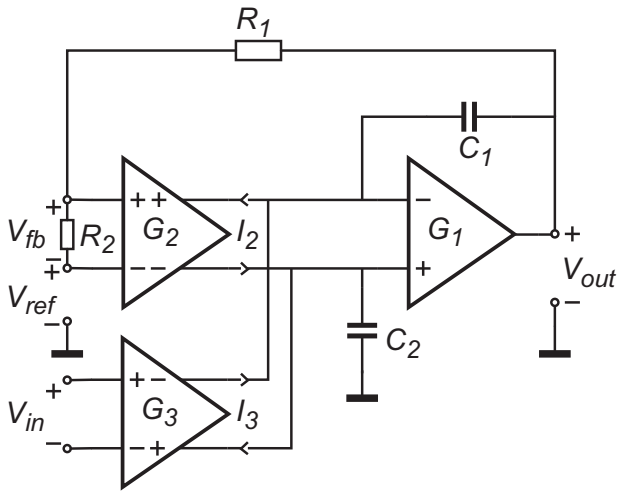


Figure 1.2: Two-stage operational amplifier with an additional feed-forward input stage to implement a current-feedback instrumentation amplifier

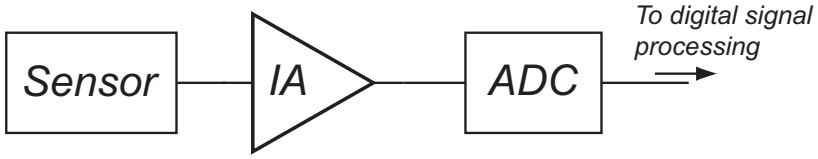


Figure 1.3: Read out interface of a sensor

mentation amplifiers and A/D converters shows that the current-feedback IA have similarities to continuous-time $\Sigma\Delta$ modulators. This class of converters are known for high resolution in a small signal bandwidth and they look suitable for sensor applications.

1.2 Project Description

Since the 1970s, different topologies has been proposed for current-feedback instrumentation amplifiers (CFIA). They can be divided into two main categories; indirect and direct CFIAs, [1]. They use transconductance stages in cascade and cascode configuration, respectively. One of the recent designs of the indirect CFIA is proposed in [5] where a three stage operational amplifier with nested miller compensation is converted to a CFIA by an additional feed-forward input stage. The simplified diagram of this IA is shown in Fig. 1.4. The chopping, dynamic element matching, and ripple reduction loop circuitry are not included in this figure for the sake of simplicity.

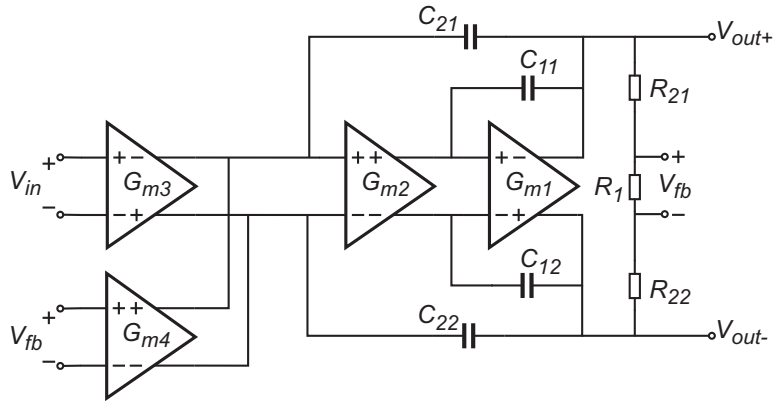


Figure 1.4: Current-feedback instrumentation amplifier implemented with a three stage Op-Amp

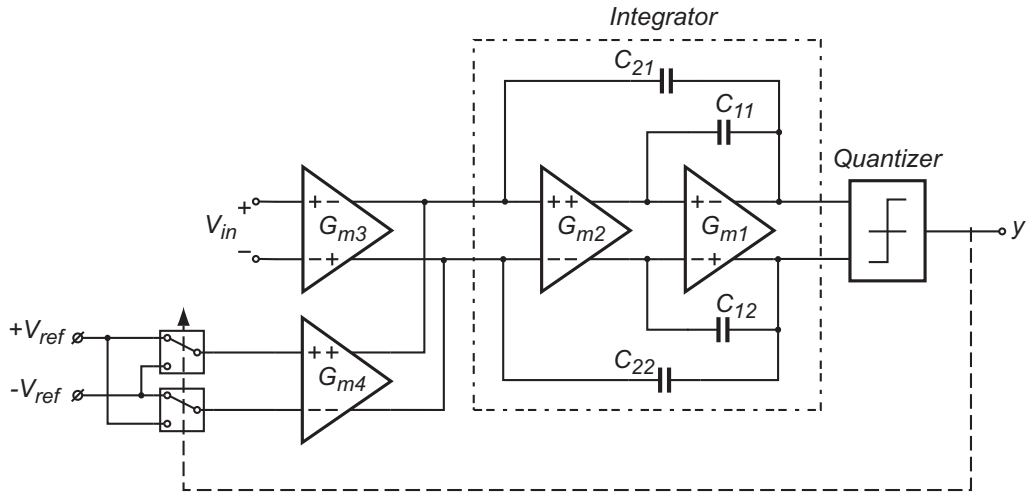


Figure 1.5: First-order CT ΣΔ modulator

The similarity of this structure to a CT ΣΔ modulator can be seen in this schematic. If the resistive feedback is broken and a single-bit quantizer and digital-to-analog converter (DAC) are substituted, the miller compensated OpAmp will work as an integrator. In this way a first-order ΣΔ modulator is obtained as shown in Fig. 1.5

Since the same blocks can be used in the input and feed-forward paths, it is expected that the noise performance, common-mode rejection ratio, input referred offset, and gain error will stay the same. The main challenge associated with this approach concerns the linearity of the system. The transconductance in the feedback path is only operated at two points and consequently it functions linearly. However, if the input transconductance has any nonlinearity, which is usually the case, it influences the linearity of

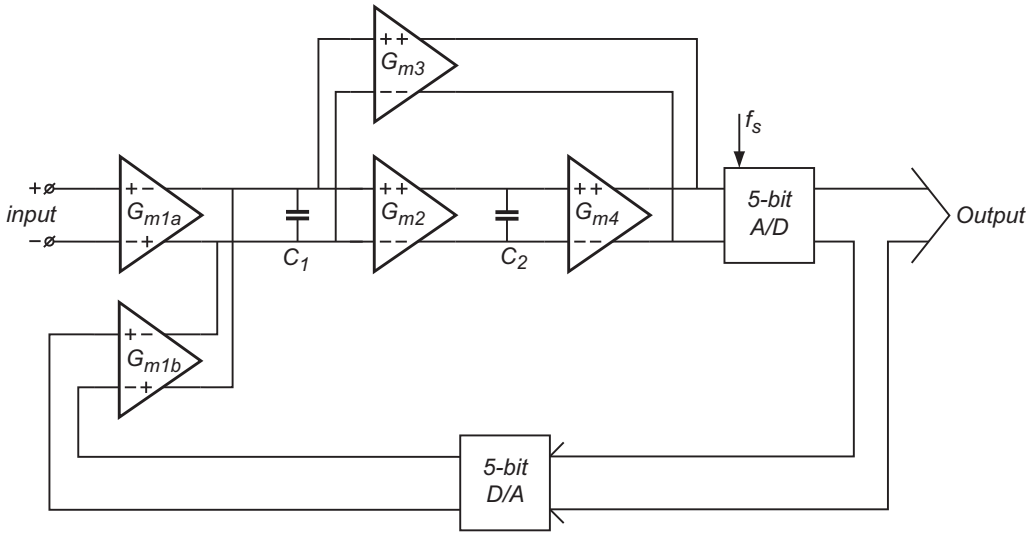


Figure 1.6: Second order 5-bit ΣΔ modulator

the system. It is not an issue in a CFIA, because the loop gain forces the input of the feedback transconductance to be a replica of the input signal. If the nonlinearity of the input and feedback stages are identical, then the nonlinearity is canceled.

One solution is to find a way to generate an analog or multilevel signal in the feedback. This has been done in [6] by using a 5-bit quantizer in the modulator. They designed a second-order ΣΔ modulator based on Gm-C integrators as illustrated in Fig. 1.6. Hence 32 levels will be applied to the input of the feedback transconductance and so it will generate an approximation of the input nonlinearity. Indeed with more levels, even better linearity can be achieved. However, there are challenges with multi-bit ΣΔ modulators. One important issue is the linearity of the feedback DAC which is limited by the mismatch of the unit elements. This nonlinearity is introduced at the summing node and will not be suppressed by the loop gain. Hence it can result to harmonics and tones in the spectrum which is highly undesirable. There are different solution for this problem but all of them increase the complexity of the system.

One other possibility is to extract the baseband analog signal from the bit-stream and apply it to the feedback transconductance. Considering identical operational transconductance amplifiers (OTA) at the input and feedback stage, the nonlinearity can then be compensated.

In this work, this idea is implemented in a low-pass ΣΔ modulator by placing a low-pass RC-filter (LPF) after the DAC to extract the baseband

Table 1.1: Performance of CT ΣΔ modulators with input Gm-stage and a current-feedback IA

	[6] CT ΣΔ	[7] CT ΣΔ	[8] CT ΣΔ	[5] CFIA
noise floor /resolution	$<10\mu V_{pp}$	12-bits	11-bits	$15\text{nV}/\sqrt{(Hz)}$
input range	±1.2V	NA	400mV	50mV
offset	340μV	NA	NA	5μV
bandwidth	500kHz	6.4MHz	2MHz	—
linearity (Harmonic Distortion)	< -70dB	< -70dB	< -86dB	NA
power	12.7 mW	25.2 mW	11mW	1.15 mW

signal. Merely adding an LPF in the feedback path affects the loop's stability since it introduces another pole. In this thesis we have investigated how the modulator can be stabilized with an LPF in the feedback path and also how much the linearity of the modulator can be improved.

Table 1.1 shows the specifications of three CT ΣΔ modulators with input transconductors and one instrumentation amplifier. are given in this table. Since the final goal of this thesis is to merge an IA and an ADC in to one high-precision ADC, it is advantageous to compare the performance of a state-of-the-art IA with, that of similar ΣΔ modulators.

The modulators given in this table are for high bandwidth applications but they give insight into the performance of a CT ΣΔ modulator. As Described earlier, [6] uses a second order structure with 5-bit quantization, where the input is a degenerated transconductor. [7] is a third order modulator based on a time encoding quantizer. RC active integrators are used in the loop filter. The important point is that to implement the time encoding quantizer, an RC-filter has been used in the feedback path. [8] has presented a fifth order Gm-C CT ΣΔ modulator in which a linearized input transonductor has been used.

The specifications of a ΣΔ modulator fulfilling the requirements of an IA, can be established from table 1.1. The noise floor, offset and input range should be equal to those of the CFIA, which are $15\text{nV}/\sqrt{(Hz)}$, 5μV and 50mV, respectively. The AC linearity in terms of (harmonic distortion) HD can be aimed for less than -80dB. The power consumption should also be in the range of the CFIA, i. e. about 1mW.

1.3 Organization of the report

Chapter 2 is a brief survey of the basic concepts of Analog-to-Digital conversion followed by the fundamentals of $\Sigma\Delta$ modulators such as oversampling and noise shaping. The trade-offs between modulator order, multi-level quantization and continuous-time versus discrete-time are also described in this chapter.

Chapter 3 explains the techniques used to implement high-precision $\Sigma\Delta$ modulators. The non-linearity of continuous-time modulator with input transconductors is discussed and a new method to overcome this is proposed. This technique is investigated in first and second-order CT modulators.

Chapter 4 presents a design review of the continuous-time $\Sigma\Delta$ modulator with improved linearity. The system level design is described including the individual block requirements and challenges. The transistor level design of the major blocks are given briefly followed by the noise analysis. The simulation results are given at the end of this chapter.

Chapter 5 summarizes the measurement results. The performance of the modulator with and without the proposed technique is measured and compared. Issues related to the layout and non-idealities which have not been considered in the design are addressed.

Chapter 6 concludes with a summary of the achievements and further improvement are proposed for future work.

Chapter 2

$\Sigma\Delta$ Modulation

A/D converters are separated into two main groups; Nyquist-rate converters and Oversampling converters [9]. *Nyquist-rate A/D Converters* can be defined as converters which generate a specific bit-word for each input voltage sample, i.e. there is a one-to-one correspondence between output and input. These converters operate normally at 1.5 to 10 times the input signal's Nyquist rate. On the other hand, *Oversampling converters* operate much faster than the input signal's Nyquist rate. In these converters, the Signal to Noise Ratio (SNR) is increased by filtering the quantization noise outside the signal bandwidth.

The focus in this chapter is on conventional continuous-time (CT) lowpass $\Sigma\Delta$ analog-to-digital (A/D) converters, since the proposed design is a modified version of this architecture. In the first section, the fundamental principals of A/D converters are described without considering any specific architecture or circuit, while the next section is allocated to a discussion of $\Sigma\Delta$ modulation and the basics of this class of converters. A comparison for different types of $\Sigma\Delta$ modulators is given at the end.

2.1 Basic Principals of A/D Converters

The block diagram of an ideal A/D converter is shown in Fig. 2.1, where V_{in} and V_{ref} are the analog and reference input voltages respectively and B_{out} is the generated bit-word. The relation between these signals in an ideal A/D converter is [9]:

$$V_{ref}(b_1 2^{-1} + b_2 2^{-2} + ... + b_N 2^{-N}) = V_{in} \pm V_x \tag{2.1}$$

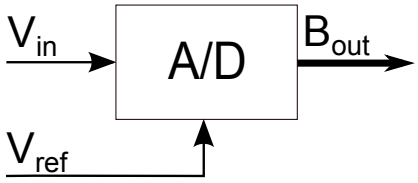


Figure 2.1: Ideal ADC

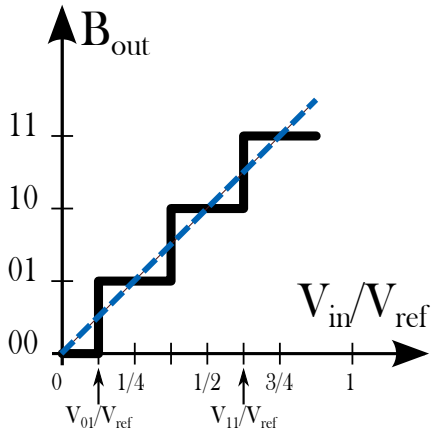


Figure 2.2: Characteristic of an Ideal 2-bit ADC

where:

$$-\frac{V_{LSB}}{2} \leq V_x < \frac{V_{LSB}}{2} \tag{2.2}$$

and V_x is known as quantization error. This error means there is an interval of input signal that generates the same output bit-word. V_{LSB} is defined to be the input voltage change that corresponds to a single LSB (Least-Significant Bit) change in the output. Mathematically it can be defined as:

$$V_{LSB} = \frac{V_{ref}}{L-1} \tag{2.3}$$

where L is the number of quantization levels and for an N-bit quantizer, $L = 2^N$.

The input-output characteristic of an ideal 2-bit A/D converter is shown in Fig. 2.2. It should be noted that the relation in Eq. 2.2 is satisfied only if the input signal is less than $\frac{7}{8}V_{ref}$ and larger than $-\frac{1}{8}V_{ref}$. In general the input signal should be within one LSB of the two last transitions, otherwise the quantizer is *overloaded* and quantization error is greater than $\frac{V_{LSB}}{2}$.

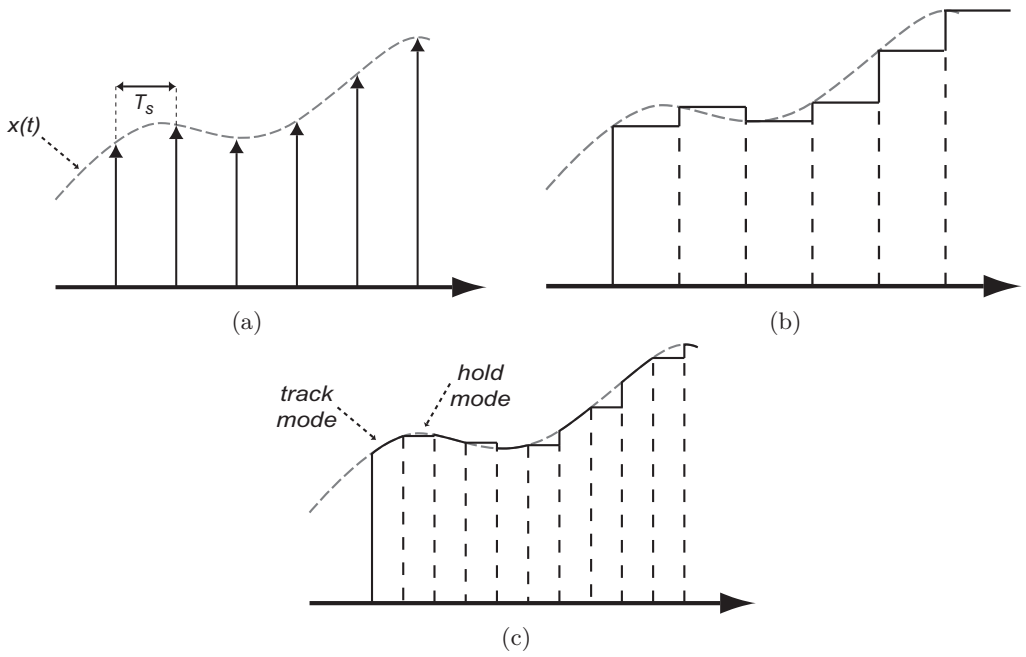


Figure 2.3: Sampling a) ideal, b)zero-order hold and c) track and hold

2.1.1 Sampling

In transforming a CT analog signal to a digital one, there exists two main operations; sampling the analog input signal and quantizing its amplitude so that it will have one of the possible finite values. A sampling circuit does the first task while quantization is carried out in the ideal A/D converter or in other words quantizer.

Main reason for sampling circuits is to adjust the timing requirements of the A/D converters. They are the interface between the analog world and signal processing circuitry. Consequently their resolution, precision and speed should fulfill the overall desired performance.

Sampling is usually a periodic function in voltage-domain (in some application it is performed also in charge-domain). A sampling circuit samples an analog signal and stores it in a memory element such as capacitor until the next sampling moment.

Sampling can be performed in three different manners, resulting in different frequency spectra. They are shown in Fig. 2.3, where Fig. 2.3a is the ideal sampling, Fig. 2.3b is zero-order hold and Fig. 2.3c is called track and hold [10].

In the ideal case, the input CT signal, $x(t)$ is multiplied by a periodic train of impulses. In the frequency domain, the signal is convolved with a

train of impulses resulting in replicating and shifting the signal spectrum by integer multiples of f_s. This method is never implemented, since generating an ideal impuls signal is not practical and also the circuits following the sampler are normally able to process signals with nonzero duration.

The other method is to capture the signal value at the sampling instant and hold it until the next sampling moment. This is equal to multiplying the CT signal with a periodic impulse train and convolve the resulting signal with a rectangle function. The resulting spectrum is like the ideal case but multiplied by a sinc function. In practice, capturing the signal in zero time is not possible and a sufficiently narrow sampling window is required to provide an approximation of the ideal zero-order hold.

In the third scheme, as shown in Fig. 2.3c, the input is tracked during the sampling phase (also known as "acquisition" or "tracking" mode) and the last value is held at the output when the circuit enters the hold mode. The waveform can be decomposed into two modified square waves with a period of T_s: one whose amplitude is multiplied by the signal, and another with an amplitude equal to the held value at the output. Hence the output spectrum contains two signal spectra multiplied by sinc functions.

As inferred from the above explanations, the output spectra of zero-order hold and track and hold schemes have sinc envelope, or in other words it is distorted. However, there is no concern when these circuits are used at the front-end of an A/D converter since these converters sense the input only at the hold mode and hence the digital output corresponds to the sample moments of the input signal. In other words, the combination of the front-end, track-and-hold and A/D converter operates as an ideal sampling circuit [10].

2.1.2 Quantization Noise

As described earlier, quantization error occurs even in ideal A/D converters (V_x in Eq. 2.1). This error (not entirely correctly) is also known as *quantization noise*. In this section, this error is treated as an additive noise and it is characterized.

It is desirable to approximate the transfer curve of a quantizer with a straight line $v = ky$, where k is the gain of the quantizer. It is shown in Fig 2.4 on the left side. The dotted line is y and the solid line is the quantized version of the input, which is named v. On the right side is the quantization error which is the difference between these two curves.

As mentioned earlier, we want to model the quantization error as an additive noise source and calculate its power. One good way for calculation is

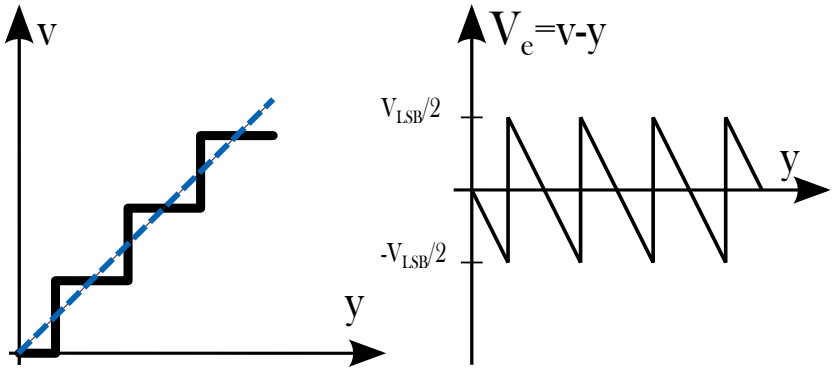


Figure 2.4: Ideal quantization transfer curve and quantization error

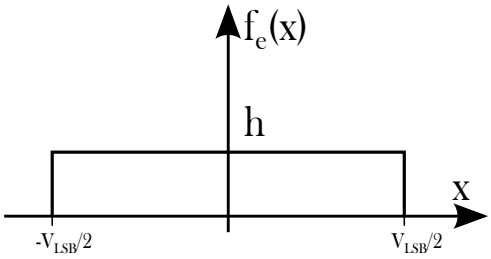


Figure 2.5: Probability Density Function for the quantization error, V_e

stochastic approach. In this approach, the input signal is considered to vary rapidly such that the quantization error signal, V_e, can be approximated as a random signal with uniform distribution between $\pm\frac{V_{LSB}}{2}$. Hence, the Probability Density Function (PDF) for this signal, $f_e(x)$, has a constant value as shown in Fig. 2.5. As long as the integration of $f_e(x)$ over the entire range should be 1, it's value can be found:

$$\int_{-\infty}^{\infty} f_e(x)dx = 1 \Rightarrow \quad h \times V_{LSB} = 1 \Rightarrow h = \frac{1}{V_{LSB}}$$

The average value of the quantization error can be found equal to zero from the PDF as follows:

$$\bar{V_e} = \int_{-\infty}^{\infty} x f_e(x)dx = \frac{1}{V_{LSB}} \left(\int_{-V_{LSB}/2}^{V_{LSB}/2} x dx \right) = 0 \tag{2.4}$$

and the rms value is:

$$V_{e(rms)} = \left[\int_{-\infty}^{\infty} x^2 f_e(x)dx \right]^{1/2} = \left[\frac{1}{V_{LSB}} \left(\int_{-V_{LSB}/2}^{V_{LSB}/2} x^2 dx \right) \right]^{1/2} = \frac{V_{LSB}}{\sqrt{12}} \tag{2.5}$$

It can be concluded from Eq. 2.5 that the quantization noise power is equal to $V_{LSB}/\sqrt{12}$ when the quantization noise has a uniform distribution over the $\pm V_{LSB}/2$ interval.

From Eq. 2.3, for each additional bit in the quantizer V_{LSB} is halved and from Eq. 2.5 it can be inferred that the quantization noise is decreased by 6 dB. It is nice to find a formula for the best possible SNR in an ideal A/D converter when the input is a sinusoidal waveform between 0 and V_{ref}. The ac power of the sinusoidal wave is $V_{ref}/(2\sqrt{2})$ and the SNR can be calculated as follows:

$$\begin{aligned} SNR &= 20log\left(\frac{V_{in(rms)}}{V_{e(rms)}}\right) \\ &= 20log\left(\frac{V_{ref}/(2\sqrt{2})}{V_{LSB}/(\sqrt{12})}\right) \\ &\approx 20log\left(\sqrt{\frac{3}{2}}2^N\right) \end{aligned}$$

$$SNR = 6.02N + 1.76dB \tag{2.6}$$

Where N is the number of bits in the quantizer. It should be reminded that Eq. 2.6 gives the best possible SNR for and N-bit A/D converter. Decreasing the input amplitude, with constant V_{ref} will result in smaller SNR value. Also note that this SNR can be improved if the input signal's bandwidth is less than the Nyquist rate by using oversampling techniques. Oversampling is going to be described in section 2.2 where the design of ΣΔ Modulators is explained.

2.1.3 Performance Parameters

In this section, some terms commonly used to describe the performance of A/D converters are defined. These definitions are required for determining the A/D converters' transfer response. Transfer response of an A/D converter can be defined by the mid-point of the quantization interval for each digital output word. Since transitions are easier to be measured than the mid-points, it is reasonable to measure the quantizer's errors in terms of the analog transition points, V_{ij} in Fig. 2.2. [9]

Resolution The *resolution* is an indication of the number of distinct analog intervals corresponding to the different digital words. For example, an N-bit resolution indicates a converter that can resolve 2^N distinct analog levels. Resolution does not determine the accuracy of the converter necessarily, but it usually refers to the number of bits of the digital word.

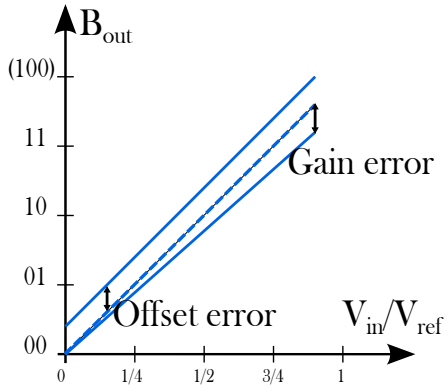


Figure 2.6: Offset and gain error for a 2-bit A/D converter

Offset and Gain Error In an A/D converter, *offset* is defined as the deviation of $V_{0..01}$ from $1/2LSB$, or mathematically:

$$E_{off} = \frac{V_{0..01}}{V_{LSB}} - \frac{1}{2}LSB \tag{2.7}$$

The *gain error* can be defined by the difference of the ideal and actual curves at the full-scale while the offset error has been reduced to zero. The gain error of a quantizer, E_{gain} (in units of LSBs), is:

$$E_{gain} = \left(\frac{V_{1..1}}{V_{LSB}} - \frac{V_{0..01}}{V_{LSB}}\right) - \left(2^N - 2\right) \tag{2.8}$$

Gain and offset errors are shown graphically in Fig. 2.6.

Accuracy The *absolute accuracy* of a converter can be defined by the difference between the expected and actual transfer responses. Offset, gain, and linearity errors are included in the absolute accuracy [9]. Sometimes the accuracy after removing the offset and gain errors is referred to *relative error* or *maximum integral nonlinearity error*. Accuracy can be expressed as a percentage of full-scale value or as a fraction of an LSB, e.g. a 10-bit accuracy determines that the quantizer's error is less than full-scale divided by 2^{10}.

Note that the accuracy can be larger than the resolution or vice versa. An accuracy larger than the resolution means that the transfer response is controlled precisely.

Integral Nonlinearity (INL) Error The *integral nonlinearity (INL) error* is the deviation from a straight line after removing the offset and gain errors. However, how should this straight line be determined? One way is to use the endpoints of the quantizer's transfer response. Another way is to

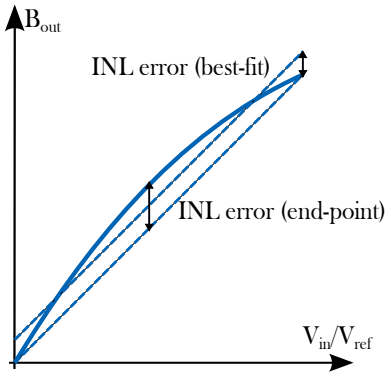


Figure 2.7: Integral nonlinearity error in a quantizer

find the best-fit straight line which minimizes the maximum difference (or the mean squared error). These two definitions are shown in Fig. 2.7.

Dynamic Range The *dynamic range* of a converter is defined when the input is the maximum sinusoidal signal. In this case, the ratio between the rms value of sine wave amplitude and the rms value of the noise plus the distortion is called dynamic range. The rms output plus distortion can be achieved by eliminating the sinusoid from the measured output. Dynamic range can also be expressed as effective number of bits by Eq. 2.6.

2.2 Fundamentals of ΣΔ Modulation

Oversampling A/D converters are usually used for high resolution and medium/low speed applications. They can not be used for high frequency application, because as also their name specifies, their operating frequency is much higher than the Nyquist rate, typically higher by a factor between 8 and 512. These converters relax the requirements on analog circuitry at the expense of more complex digital circuitry. This is a desirable trade-off since in the new process nodes, implementation of sophisticated high-speed digital circuitry is done much easier than the high-resolution analog one considering the poor analog performance of the devices. A second advantage of oversampling A/D converters is that the analog anti-aliasing filter is much more relaxed that usually even a first-order filter is enough.

The higher sampling frequency in this class of converters is exploited for higher resolution. Even extra bits of resolution can be achieved by spectrally shaping the quantization noise. This improved performance in resolution also alleviates the requirements on the matching accuracy of analog components such as resistors, current sources or capacitors.

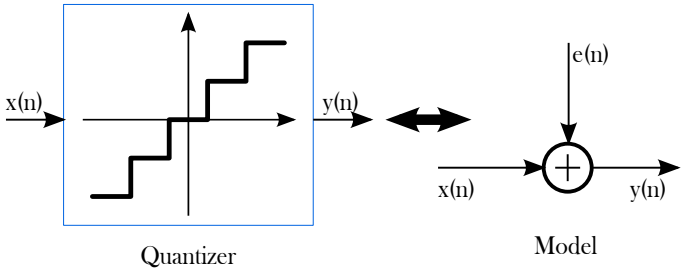


Figure 2.8: Quantizer and its linear model

2.2.1 Over-sampling

Over-sampling means that the sampling occurs at a ratio much higher than the Nyquist rate. Over-sampling ratio can be defined as follow:

$$OSR = \frac{f_s}{2f_B} \tag{2.9}$$

where f_s is the sampling frequency and f_B is the signal bandwidth. Using a greater OSR means the quantization noise is spread over a larger frequency range and it results to a higher dynamic range.

To formulate the dynamic range with respect to OSR, first we need to model the quantization noise. A linear model is illustrated in Fig. 2.8. In fact the quantization noise is the difference between the input and output. Hence the error depends on the input signal, x(n). This model is exact, but it is not an easy model for understanding. If we make some assumption on the statistics of this model, like considering an independent white-noise signal for the quantization error, the model becomes an approximate but much easier for analysis. It has been demonstrated that with some exceptions it behaves as an accurate model.

Assuming a very active input signal $x(n)$, $e(n)$ can be approximated by an independent random value distributed randomly between $\pm\Delta/2$, where Δ represents the difference between two adjacent quantization levels. From previous section it can be inferred that the power of quantization is $\Delta^2/12$ independent of the sampling frequency and its power spectral density, $S_e(f)$, is white (i.e. constant over frequency) and located within $\pm f_s/2$. The power spectral density of the white quantization noise, $S_e(f)$ is illustrated in Fig. 2.9.

The spectral density height can be calculated by considering that the total noise power is $\Delta^2/12$ and equals the area under $S_e(f)$ within $\pm f_s/2$.

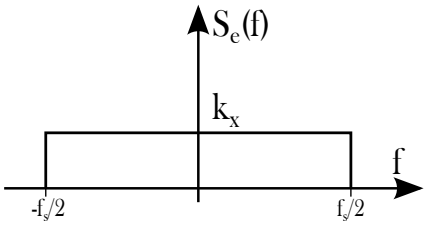


Figure 2.9: Assumed power spectral Density of quantization noise

Mathematically representing:

$$\int_{-f_s/2}^{f_s/2} S_e^2(f)df = \int_{-f_s/2}^{f_s/2} k_x^2 df = k_x^2 f_s = \frac{\Delta^2}{12} \tag{2.10}$$

$$k_x = \left(\frac{\Delta}{\sqrt{12}}\right)\sqrt{\frac{1}{f_s}} \tag{2.11}$$

Oversampling is defined to sample a signal much faster than the Nyquist rate, where the Nyquist rate is twice the bandwidth of the signal. After quantization, a filter, $H(f)$, will remove the signals (including quantization noise) beyond f_B to extract the desired signal. Filter $H(f)$ can be characterized as follow:

$$|H(f)| = \begin{cases} 1 & \text{if } |f| \leq f_B \\ 0 & \text{otherwise} \end{cases} \tag{2.12}$$

The maximum amplitude of a sinusoidal input signal will be $2^N(\Delta/2)$ and the signal power, P_s, will be:

$$P_s = \left(\frac{\Delta 2^N}{2\sqrt{2}}\right)^2 = \frac{\Delta^2 2^{2N}}{8} \tag{2.13}$$

P_s has the same power after filtering but the quantization noise power will be reduced to:

$$P_e = \int_{-f_s/2}^{f_s/2} S_e^2(f)\left|H(f)\right|^2 df = \int_{-f_B}^{f_B} k_x^2 df = \frac{2f_B}{f_s}\frac{\Delta^2}{12} = \frac{\Delta^2}{12}\left(\frac{1}{OSR}\right) \tag{2.14}$$

Thus doubling the sampling frequency, equivalent to doubling OSR, decreases the quantization noise power by a factor of one-half (3dB, or 0.5 bits).

The maximum achievable SNR in an ideal quantizer can be found by dividing P_s by P_e using equations 2.13 and 2.14:

$$\begin{aligned} SNR_{max} &= 10log\left(\frac{P_s}{P_e}\right) = 10log\left(\frac{3}{2}2^{2N}\right) + 10log\left(OSR\right) \\ &= 6.02N + 1.76 + 10log(OSR) \end{aligned} \tag{2.15}$$

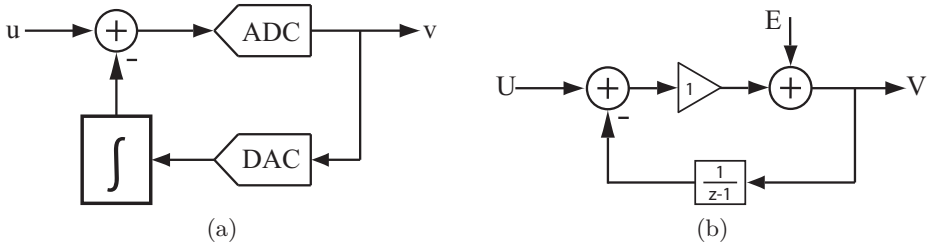


Figure 2.10: (a) A delta modulator used as an ADC and (b)its linear z-domain model

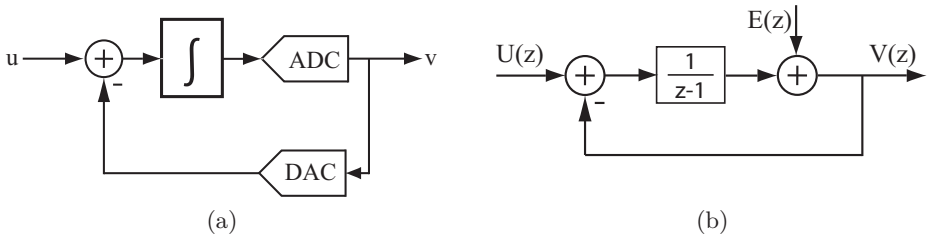


Figure 2.11: (a) A ΣΔ modulator used as an ADC and (b) its linear z-domain model

This relation is similar to Eq. 2.6 with an additional term, which represents the SNR improvement due to the OSR. Eq. 2.15 represents that the SNR increases with a slope of 3 dB/octave with increasing oversampling ratio.

2.2.2 Noise Shaping

Noise shaping is a method in oversampled converters to enhance the resolution. The general idea is to shape quantization noise to the frequencies where it can be filtered out (i.e. high frequencies for baseband input signals). There are mainly two oversampling converters, *Delta* and *Sigma-Delta*[*]. Block diagram of a Delta modulator is shown in Fig. 2.10. The details of this topology is beyond the scope of this thesis [11].

ΣΔ converters, usually named modulators, work in a feedback loop containing a loop filter and a low-resolution ADC in the feedforward path and a low resolution DAC in the feedback path. A general block diagram together with a linear model of the modulator is shown in Fig. 2.11. Exploiting the linear model shown in Fig. 2.11b and considering we have two independent input signals, we can extract a signal transfer function, $STF(z)$ and a noise

[*]Also called Delta-Sigma.

transfer function $NTF(z)$ as follow:

$$STF(z) \equiv \frac{V(z)}{U(z)} = \frac{H(z)}{1+H(z)} \tag{2.16}$$

$$NTF(z) \equiv \frac{V(z)}{E(z)} = \frac{1}{1+H(z)} \tag{2.17}$$

Where $H(z)$ is the loop filter transfer function. It is noticeable that the poles of $H(z)$ are the zeros of $NTF(z)$, i.e. when $H(z)$ goes to infinity $NTF(z)$ goes to zero. The output signal can be represented by the addition of each input signal multiplied by the corresponding transfer function in z-domain:

$$V(z) = STF(z)U(z) + NTF(z)E(z) \tag{2.18}$$

$H(z)$ can be manipulated to noise-shape the quantization noise. By choosing a filter that has very high gain in the signal band , we can make the STF approximately equal to 1 and NTF very small in the desired band. Then the quantization noise is reduced in the signal band while the signal itself is not affected. Afterwards a post-filtering stage in digital domain, removes the out-of-band quantization noise, with a negligible effect on the signal.
As an example, for a first order low-pass ΣΔ modulator the best filter is an integrator which has a high gain in the signal band. In the following the noise shaping of a first order discrete-time (DT) modulator is described and the improvement in the resolution is calculated. A DT modulator is chosen for this analysis step as long as it is easier to understand it in comparison to CT modulator while their performance is similar.
A linear first order low-pass DT ΣΔ modulator model is shown in Fig. 2.11b. The output can be represented by two inputs (U(z) and E(z)) as:

$$V(z) = z^{-1}U(z) + (1-z^{-1})E(z) \tag{2.19}$$

and it can be written in time domain as:

$$v(n) = u(n-1) + e(n) - e(n-1)$$

where n is the time index. From the time domain representation, we see that the output consists of a delayed but unchanged version of the analog input u and a differentiated version of the quantization error e. It can be inferred from this equation that the differentiation causes the error to be suppressed at frequencies much lower than the sampling frequency f_s.

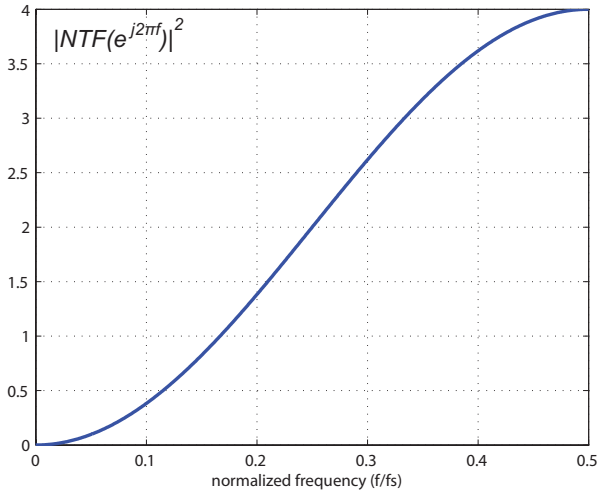


Figure 2.12: Noise shaping function of a 1^{st}-order ΣΔ modulator

From Eq. 2.19, NTF is $(1 - z^{-1})$. To find its magnitude, $|NTF(f)|$, we should first substitute z with $e^{j\omega T} = e^{j2\pi f/f_s}$ in the NTF:

$$\begin{aligned} NTF(z) &= 1 - e^{-j2\pi f/f_s} = \frac{e^{j\pi f/f_s} - e^{-j\pi f/f_s}}{2j} \times 2j \times e^{-j\pi f/f_s} \\ &= sin\left(\frac{\pi f}{f_s}\right) \times 2j \times e^{-j\pi f/f_s} \end{aligned} \tag{2.20}$$

And the magnitude of the noise transfer function will be:

$$|NTF(f)| = 2sin\left(\frac{\pi f}{f_s}\right) \tag{2.21}$$

The squared magnitude of the NTF as a function of the frequency is shown in Fig. 2.12. As this figure illustrates the NTF of a ΣΔ modulator is a high-pass function. The quantization noise power over the signal band is:

$$P_e = \int_{-f_B}^{f_B} S_e^2(f)\,|NTF(f)|^2\,df = \int_{-f_B}^{f_B} \left(\frac{\Delta^2}{12}\right)\frac{1}{f_s}\left[2sin\left(\frac{\pi f}{f_s}\right)\right]^2 df \tag{2.22}$$

Since we are assuming $OSR \gg 1$ we can use the approximation $sin((\pi f)/f_s) = (\pi f)/f_s$:

$$P_e \cong \left(\frac{\Delta^2}{12}\right)\left(\frac{\pi^2}{3}\right)\left(\frac{2f_B}{f_s}\right)^3 = \frac{\Delta^2\pi^2}{36}\left(\frac{1}{OSR}\right)^3 \tag{2.23}$$

Assuming the same maximum signal power as in Eq. 2.13, after some calculation the maximum achievable SNR is found as follow:

$$SNR_{max} = 6.02N + 1.76 - 5.17 + 30log(OSR) \tag{2.24}$$

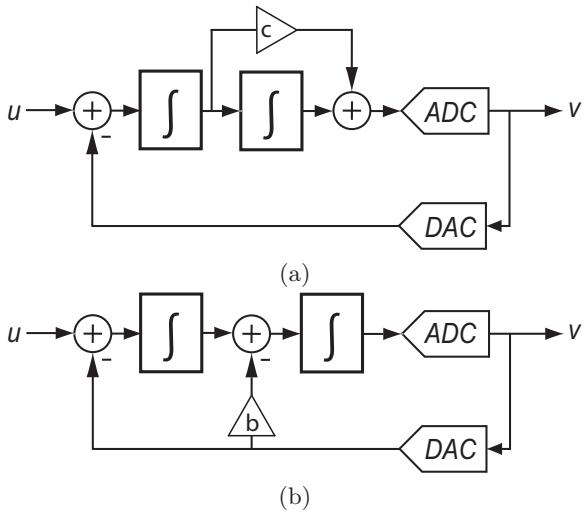


Figure 2.13: 2^{nd}-order ΣΔ modulator with a)feed-forwad and b)feedback

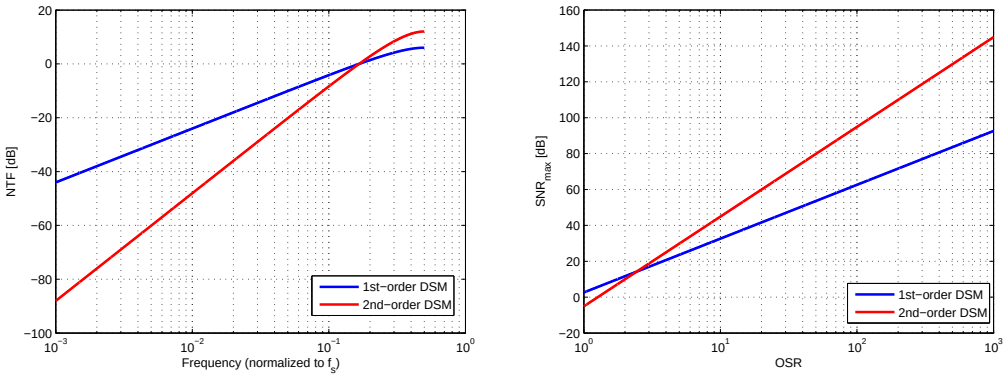
We see here that doubling the OSR for a 1^{st}-order ΣΔ modulator, increases the SNR by 9dB or equivalently 1.5 bits/octave.

2.2.3 Higher-Order Modulators

In the loop filter of the general ΣΔ modulator shown in Fig. 2.11 we can use higher order filters, instead of a single integrator. The advantage is that we can shape the quantization noise better and achieve a higher resolution. A second-order ΣΔ modulator is obtained by using a cascade of two integrators. If we don't introduce any additional path for compensation, there will be instability problem. A feed-forward (FF) or feedback (FB) path can stabilize the modulator [11]. A block diagram for a both cases is shown in Fig. 2.13.

Similar transfer functions can be implemented in both structures. Their main difference is the filtering at the output of the first integrator. The transfer function of the signal from input to the output of the first integrator in feedback configuration is a low-pass filter, while for a feed-forward structure is a high-pass filter. This means that the output signal of the integrator in a feed-forward structure is quantization noise while in the feed-back configuration it contains the signal. Hence the integrator's output swing in the feed-forward structure is inherently smaller. The second difference is that in a FF configuration, the signal transfer function has a peaking.

The other difference is in the CT topologies, where the modulator introduces an intrinsic anti-aliasing filtering. This filtering for a FF structure is



(a) (b)

Figure 2.14: (a)NTF and (b)SNR_{max} of first- and second-order sigma-delta modulators

20 dB/decade while for the FB it has a 40dB/decade slope.
Other topologies such as combination of FF and FB or a feed-forward path from input signal to the input of the quantizer are introduced in literature [11], but their discussion is beyond the scope of this thesis. However, a desired NTF for a 2^{nd}-order ΣΔ modulator is $(1-z^{-1})^2$ which can be achieved by any of the topologies shown in Fig. 2.13. The resulting SNR after some calculations similar to the previous section is:

$$SNR_{max} = 6.02N + 1.76 - 12.9 + 50log(OSR) \tag{2.25}$$

Comparisons of the 1^{st}-order and 2^{nd}-order ΣΔ modulator from the SNR and NTF point of view are given in Fig. 2.14. Higher order modulators can give better resolutions for the same OSR, but they have stability problems. The design of these modulators should be done with enough care for instability under all possible conditions and variations.

2.2.4 Continuous-Time Vs. Discrete-Time

The difference in DT and CT modulators are in the implementation of the loop filters. In CT implementation, the loop filter consists of RC active integrators or Gm-C based integrators while in DT modulators, switch-capacitor (SC) circuits are used in the loop filter. SC modulators are generally more attractive than CT counterparts, because they have better linearity and accuracy performance. Also the difference equations of the DT circuits are independent of the clock frequency. Hence they are scalable with frequency. Contrary, time-constants of the CT circuits are subject to

large variation and they don't track the clock. Thus they normally need a calibration step for a single clock frequency.
Despite the above mentioned features, CT ΔΣ modulators have gained more attention in the last decade. Two major reasons are the inherent anti-aliasing and higher bandwidth of the CT modulators. Inherent anti-aliasing eliminates the need for the preceding anti-alias filter. Theoretically the regeneration time of the quantizer and the speed of the DAC are limiting the CT modulator's clock rate. Whereas in a SC implementation the clock rate is limited by the settling time of the op-amp. Generally, a CT modulator can be clocked 2-4 times faster than a DT modulator and consequently the bandwidth is with the same factor wider.
One other issue in the CT implementation is sensitivity to loop delay. Loop delay is the time difference of the quantization moment and the moment the feedback DAC signal related to that quantization step is applied. If this delay is larger than a certain value, which is in the range of sampling period, risk of instability is increased [12].
In this thesis, one feature of the CT implementation that is manipulated is the possible high input-impedance through the use of an operational transconductance at the input. This is important, since in sensor read-out circuits we should prevent loading the previous stage. Using SC modulator for such an application is not desirable since it can load the sensor or have an inferior noise performance.

2.2.5 Single-bit Vs. Multi-bit Quantizers

The use of multi-bit quantizers in a ΣΔ modulator loop offers advantages such as reduced quantization noise, better defined loop gain, more relaxed slew rate requirement for amplifiers, and less sensitivity to clock jitter.

As given in Eq. 2.5 the rms value of the quantization error is proportional to the quantization steps (V_{LSB}) and consequently the power of the quantization noise will be proportional to the square of V_{LSB}. Doubling the number of bits will reduce the quantization noise by 6 dB and consequently the resolution (considering only quantization noise) will increase by the same value.

The variation of the effective gain of the quantizer will be less for higher number of bits. Hence the feedback loop is more linear, the system stability is more robust and the linear simulations are more precise. Due to the improved stability, more aggressive NTFs can be designed which can result in higher resolution or larger input signals.

For multi-bit quantization, the feedback DAC signal will change less from sample to sample. Thus the input op-amp may require less slew rate, which can lead to lower power consumption. Also the difference between the input signal and feedback signal will be smaller. Thus the linearity constraints on input stage of the filter is alleviated.

Although these advantages might make it look very tempting to use multi-bit quantization in ΣΔ loops, they have one big disadvantage. As shown in Fig. 2.11 the location of the feedback DAC between input and output is such that any error introduced by the DAC is subtracted from the input signal and this error is reflected to the output without any noise shaping. For example if the DAC has a linearity equivalent to 8-bit, the linearity performance of the system will be at most 8-bit.

The degradation of the performance of actual multi-bit modulators is mainly because of the mismatch in the unit cells of the DAC. This mismatch can introduce non-linearity and tonal behavior. There have been several techniques to improve the performance, depending on the application. The most useful of them can be arranged into dual-quantization [13]-[14], digital correction schemes [15]-[16] and mismatch-shaping [17]-[18].

Chapter 3

Analysis of High-Precision ΣΔ Modulator With Improved Linearity

High-precision data converters can not be implemented without techniques to improve the precision of the individual building blocks. Effects such as mismatch, nonlinearity, and finite intrinsic gain can limit their inherent resolution.

In this chapter a number of these methods are described which are related to this thesis and also a new technique is proposed to improve the linearity in a CT ΔΣ modulator with an input transconductor.

3.1 High-precision ΣΔ modulator

The non-idealities of real chips affect their performance. As an example, the mismatch of devices can give rise to offset or distortion. Techniques to improve matching can be classified into two groups; *static* and *dynamic*. In static approaches, the mismatch is alleviated considerably by using additional process/factory steps such as laser cutting or trimming. These additional steps increase the final costs since they require extra time and equipment. The dynamic approach uses circuit techniques to shape or modulate the mismatch to out-of-band frequencies. These techniques come at the cost of increased circuit complexity.

In order to implement a high-precision ΣΔ modulator, a number of techniques should be applied to the building blocks to improve their perfor-

mance. Quantization and/or thermal noise level are the determining factors for resolution, while for high-precision systems, offset, gain and linearity errors can be the challenges. In this section, techniques to overcome the above mentioned non-idealities are described. In chapter 4 these techniques are used to meet the desired specifications.

Dynamic Element Matching Mismatch errors in the circuit blocks such as multi-bit DAC can cause harmonic distortion and increased noise floor due to the intermodulation between input signal harmonics and the high frequency quantization noise. Dynamic element matching (DEM) is a technique to increase the matching property of a group of components. By this technique the power of the harmonics is either shaped or converted to a pseudo-random noise.

An example of this is the use of DEM in a multi-bit $\Delta\Sigma$ modulator. In this case, the DAC can be a dominant source of harmonics in this case. DEM can be performed easily when the input of the DAC is a thermometer digital code and the DAC consists of unit elements. i. e. k unit elements are activated when the input is k. Different algorithms can be used to determine which elements should be chosen and depending on this algorithm, mismatch error can be randomized (the harmonics can be spread over a band of frequencies) or shaped (moved to out-of-band frequencies). For example if the unit elements are chosen randomly each time, then the correlation between the signal and error of the DAC is broken and the error becomes random, i.e. the harmonics will be translated into (almost) white noise.

Chopper Stabilization One method of suppressing low-frequency error (flicker-noise and offset) is called chopper stabilization (CHS) [19]. In this technique, the input signal is first modulated to a frequency where the flicker noise and offset are not present and after amplification, the signal is demodulated back to the baseband. In Fig. 3.1 a diagram of this technique is shown. Assume a dc signal V_{in} at the input, the chopper output will be a square wave of period T (T is the inverse of chopping frequency) and amplitude V_{in}. If the amplifier has a gain of A_0, infinite bandwidth and introduces no delay, the output of the amplifier will be the same square wave with amplitude A_0V_{in}. The signal after demodulation will be a dc signal with the same amplitude, A_0V_{in}. The finite bandwidth of the amplifier generates spectral components around the even harmonics of the chopping frequency, which have to be low-pass filtered to recover the main amplified signal. The delay introduced by the amplifier will also reduce the dc gain of the overall chopped amplifier. In order to maximize dc gain, the same

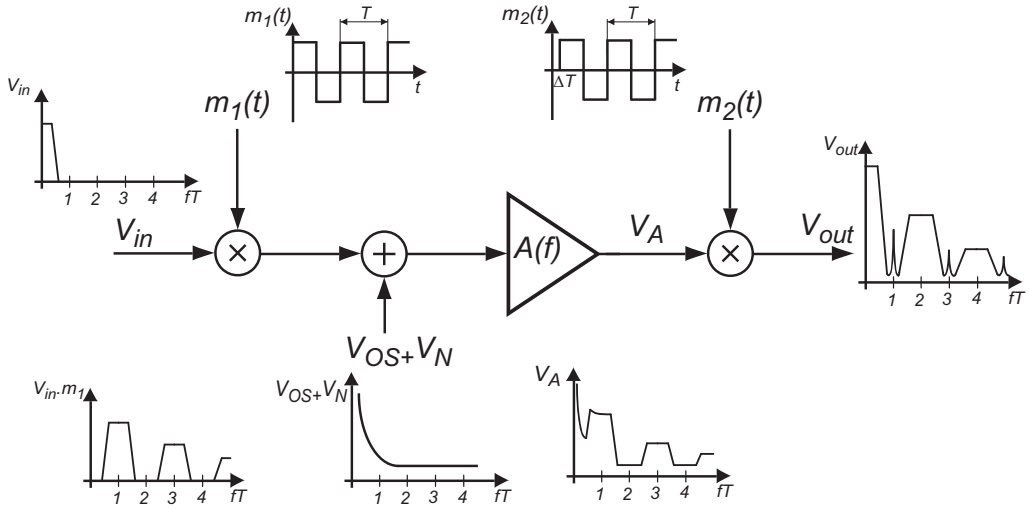


Figure 3.1: Chopper amplification principle

delay should be introduced to the demodulating square wave signal.

3.2 Linearity

In CT modulators good linearity can be achieved, if the input transconductor is a resistor connected to a good virtual ground. The main limitation is the gain and bandwidth of the amplifier constructing the integrator. If an OTA is at the input, the linearity can be a challenge. Nonlinearity of the OTA will be present at the output if enough care is not taken [20].

A CT 1^{st}-order single-bit $\Sigma\Delta$ modulator with input g_m-stage is shown in Fig. 3.2. The feedback can be implemented by a switch-capacitor circuit, current DAC (IDAC) or voltage DAC with a resistor or g_m stage. SC feedback will reduce the sensitivity to the clock jitter and it should be connected to a virtual ground node, which is the case in the schematic shown. An IDAC can be used at every node independent of presence of a signal or virtual ground. Distortion can be problematic when the signal is present at the output of the IDAC, but increasing the output impedance can solve the issue. A combination of a voltage DAC and a g_m stage can also be used as the DAC and it is similar to the IDAC. In this case the gain error can be improved by using identical g_m stages at the input and feedback. Using a resistor instead of a g_m stage may offer better power consumption but the resistor has to be connected to a virtual ground and limits the input impedance. This means that the gain and bandwidth of the opamp in the RC integrator can be a limiting issue.

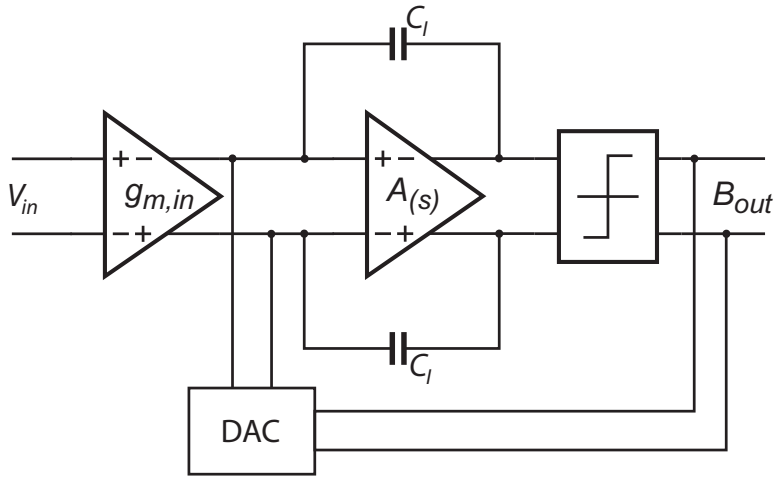
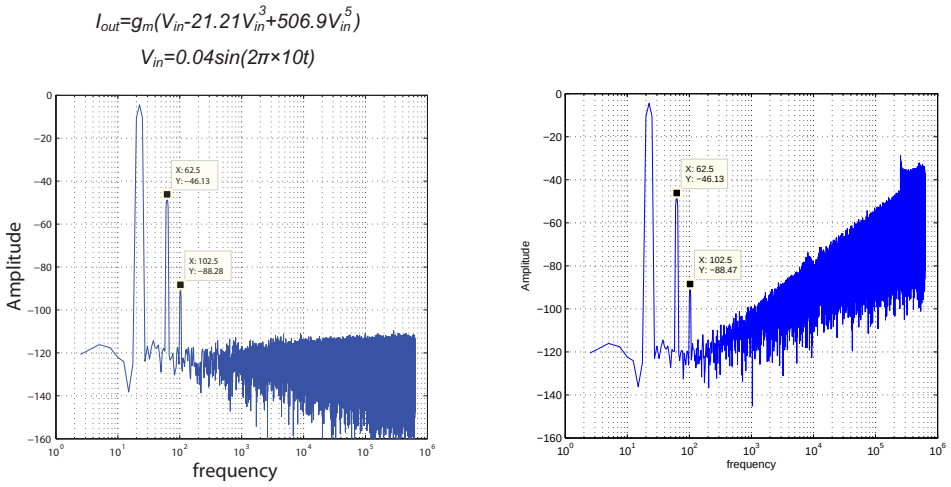


Figure 3.2: CT 1^{st}-order ΣΔ modulator

Any nonlinearity in the input OTA will enter the loop and appear directly at the output. At first glance it might seem that a combination of g_m stage and voltage DAC might be able to compensate for the input nonlinearity by introducing the same non-linearity in the feedback path. However, this is not possible for single-bit quantization, since the use of two levels makes the feedback linear. The performance will then be the same in terms of DC linearity and harmonic distortion.

When identical 5^{th} order nonlinearities are used at input and feedback path, the output spectra of the g_m stage and modulator for a 20 Hz sinusoidal input are shown in Fig. 3.3. White noise with power spectral density of $400nV^2/Hz$ is also present at the input to imitate the input referred noise of the circuitry. As illustrated in this figures, the harmonics generated at the input stage are going through the modulator without any change.

Improvement in the linearity of the overall system can be classified in two different ways; linearizing the input g_m and generating the same nonlinearity in the feedback path. An example for the first approach is [8] where triode $g_m - C$ integrator is used with a good linearity. In this design, in order to increase the input linear range of the transconductor, low-threshold NMOS devices are used which is not available in every technology, or the cost of the process increases. On the other hand, [6] has used the combination of two methods. They have used degenerated input and feedback transconductors with multi-bit quantization, hence because of the multi-bit analog input of the feedback gm-stage it can introduce nonlinearity similar to the input nonlinearity. This cancels the nonlinearity of the input and AC harmonic distortion of less than -70dB is achieved. Degeneration requires more power



(a) (b)

Figure 3.3: Output of the a) g_m stage and b) $\Delta\Sigma$ modulator

consumption or if high value resistances are used the noise level increases [21].

3.3 Proposed new method for linearity improvement

One way to compensate the nonlinearity introduced by the input stage, is to generate the same nonlinearity in the feedback path. If identical blocks are used in the input and feedback paths, a replica of the input signal should be created in the feedback path in order to generate the same nonlinearity terms. The feedback of a low-pass $\Sigma\Delta$ modulator includes the low frequency input signal and the high frequency quantization noise. Thus separating the low and high frequency feedback signals can be a good method for improvement in linearity.

As shown in Fig. 3.4, extracting the signal with a low-pass filter and introducing only this signal to the feedback nonlinearity can be a solution. However, this architecture is not stable since an extra pole is created in the feedback path. Hence a path for the high frequency signals should also be provided to stabilize the system. In the following sections alternative feedback paths are discussed.

3.3.1 LPF in parallel to HPF

Stabilizing the topology can be done by adding an additional linear high frequency feedback path. It can be a high-pass filter (HPF) as illustrated

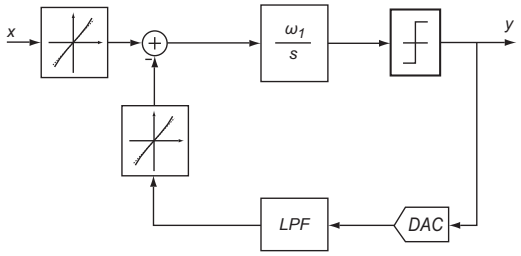


Figure 3.4: Extracting the low frequency signal from output bit-stream

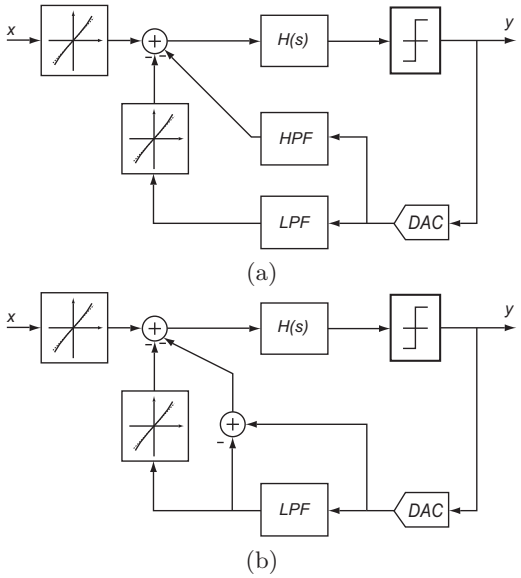


Figure 3.5: Low-pass filter in parallel to high-pass filter

in Fig. 3.5a. In order to obtain a transfer function similar to that of a conventional modulator, except for improved linearity, the feedback coefficient for all frequencies should be one. Mathematically this can be represented as:

$$LPF(f) + HPF(f) = 1 \tag{3.1}$$

If we consider a first-order LPF, its transfer function can be represented by:

$$LPF(f) = \frac{1}{1 + \frac{s}{\omega_{rc}}} \tag{3.2}$$

the transfer function for HPF can be found to be:

$$HPF(f) = \frac{\frac{s}{\omega_{rc}}}{1 + \frac{s}{\omega_{rc}}} \tag{3.3}$$

In this configuration the total feedback signal is the output bit-stream plus an estimation of the nonlinearity generated at the input. Definitely the improvement in linearity depends on how similar the nonlinearities are and how good is the signal approximation at the input of the feedback nonlinearity. These issues are discussed in detail in chapter 4.

3.3.2 LPF in parallel to (1-LPF)

One alternative to introduce a high frequency path can be inspired from Eq. 3.1. From this equation, $HPF(f)$ is equal to $1-LPF(f)$ and consequently the structure can be modified as shown in Fig. 3.5b. This topology is identical to the previous one in system level performance, but it can offer advantages in circuit level. For example if a second or higher-order LPF is used, this structure needs less components for implementation although it needs an extra DAC to implement the unity feedback coefficient. For a first order filter, this architecture also has benefits as will be shown in section 4.2.

3.3.3 LPF to the output of the integrator

Another alternative to stabilize the modulator is to provide feedback to another node of the loop filter. One possibility is to provide a feedback to the output of the first integrator. To prevent affecting the STF and NTF, the structure shown in Fig. 3.6 can be developed. Changing the summation node of the high frequency path to the output of the integrator, $HPF(s)$ should be multiplied by the transfer function of the integrator, $Int(s)$. As an example for first order LPF discussed in the previous architectures we will have:

$$HPF(s) * Int(s) = \frac{\frac{s}{\omega_{rc}}}{1+\frac{s}{\omega_{rc}}}\frac{\omega_I}{s} = \frac{\frac{\omega_I}{\omega_{rc}}}{1+\frac{s}{\omega_{rc}}} \tag{3.4}$$

Where ω_I is the unity-gain frequency of the integrator. This transfer function is identical to $LPF(s)$ with the exception of a coefficient, ω_I/ω_{rc}. Hence this feedback can be provided from the output of the $LPF(f)$. This is shown schematically in Fig. 3.6.

In this structure extra signal is added to the output of the integrator, which already contains a filtered version of the input signal. This results in greater output swing in the integrator which is not desired.

This architecture can be used for higher order, LP filters with some assumptions and considerations. In the case of a second order filter, the

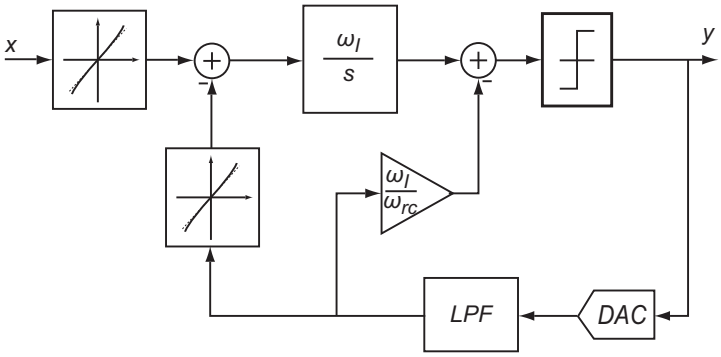


Figure 3.6: Compensation path to the output of the integrator

second pole should be located at a frequency much higher than that of the dominant pole, otherwise there will be a peak in the STF.

3.3.4 Filter choice

The different topologies described in this section have the same performance at the system level. At the circuit level, however, each have different pros and cons. For example, the third topology given in Fig. 3.6 might require a high feedback coefficient that should be implemented by a transconductor while the other two equivalent implementations do not require this feedback. The first topology shown in Fig. 3.5a may need twice the number of passive components to implement two filters while the other two structures consist of one filter. Considering these issues and a few other circuit level advantages, the second topology illustrated in Fig. 3.5b was finally chosen for the impelementation.

3.4 1^{st} order ΣΔM with filtered feedback signal

A first-order ΣΔ modulator can be easily made by substituting the loop filter in each of the structures shown in Fig. 3.5 by an integrator. Since these structures are equivalent, understanding one of them is enough for system level design. In Fig. 3.7 the first-order modulator is shown with an integrator with unity-gain frequency of ω_I. It is shown that for an input sine wave, an estimation of the sine wave is extracted from the output bit-stream by the LPF. The feedback signal applied to the transconductor contains some residual quantization noise and its amount depends on the number of quantization steps, sampling frequency, the corner frequency and the order of the filter.

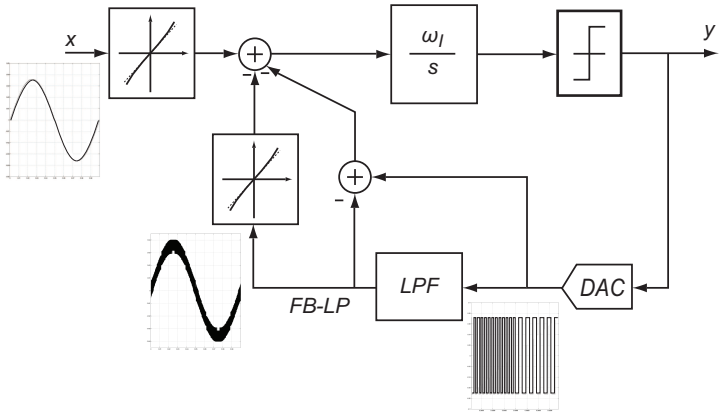


Figure 3.7: 1^{st}-order ΣΔ modulator with filtered feedback

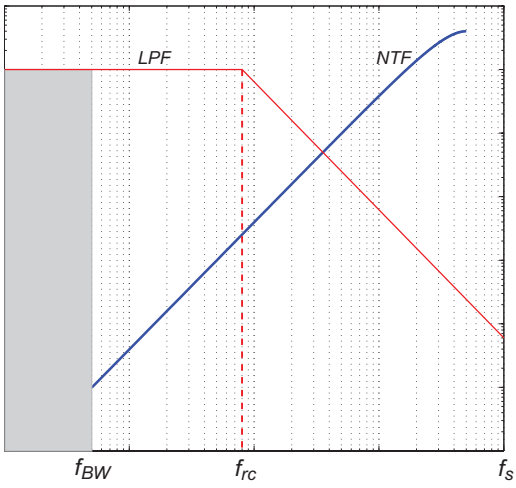


Figure 3.8: Relationships between the signal band, LPF corner frequency and sampling frequency

The relation between the signal band f_{BW}, corner frequency of the LFP f_{rc} and the sampling frequency of the modulator f_s is illustrated qualitatively in Fig. 3.8.

To maximally compensate for the input nonlinearity, the input to the feedback transconductor should be an un-delayed version of the input signal. In other words, the quantization noise should be suppressed by the LPF as much as possible. Considering every parameter to be constant and only increasing the number of quantization levels will decrease the overall quantization power. Hence the quantization noise going through the LPF will be decreased.

Use of a higher sampling frequency will shape the quantization noise to higher frequencies, and so for the same LPF corner frequency less quanti-

zation error will pass through the filter. Here we can define SCR as the sampling to LPF corner frequency ratio:

$$SCR = \frac{sampling\ frequency}{filter's\ corner\ frequency} \tag{3.5}$$

Lowering the corner frequency of the LPF can attenuate the high frequency quantization noise more, but it also introduces more delay and attenuation in the signal band which is undesirable. Then for a constant SCR ratio, higher filter corner frequency is desired. Hence we can define another parameter, CIR, which is the filter's corner frequency to the input signal frequency ratio:

$$CIR = \frac{filter's\ corner\ frequency}{input\ signal\ frequency} \tag{3.6}$$

Higher order filters have better attenuation for the quantization noise but they introduce more delay and gain deviation of unity at the signal band as well.

The filter's performance regarding the signal bandwidth can be separated into two characteristics; *gain* and *delay*. Any gain deviation from unity in the low-pass filter changes the feedback signal's amplitude. Consequently, the nonlinearity generated in the feedback path will be different from the one generated at the input, limiting the overall linearity performance. Delay in the feedback path also results in harmonics at the output.

To find out the maximum tolerable gain deviation and delay in the filter, a test system shown in Fig. 3.9 is analyzed in Simulink. The output spectrum of the Gm-stage for a 20 Hz sine wave input is shown in Fig. 3.3a. As indicated in the figure, the third harmonic has an amplitude of -46dB. To suppress the harmonics to lower than -90dB at the output of the test setup in Fig. 3.9 the gain (G) must be $0.999 \leq |G| \leq 1$ and phase shift less than 1 mrad/sec. These conditions should be valid at the signal frequency in the filter. As an example, the cut-off frequency of a first order filter should be more than three decades higher than the signal bandwidth.

In Fig. 3.10, THD in a 1^{st}-order ΣΔ modulator as a function of SCR is illustrated for both 1^{st} and 2^{nd}-order filters. CIR equals 1000, the signal amplitude is 50% of the full-scale and a single-bit quantization is used. Both poles of the 2^{nd}-order filter are considered to be at the same frequency. The nonlinearity at the input is the same used for simulations done in section 3.2 and it results to a THD equal to 42dB for a sine wave input signal. It is observable from the plot that for higher sampling frequency a better linearity can be achieved. However at SCR around 100 for the 1^{st}-order

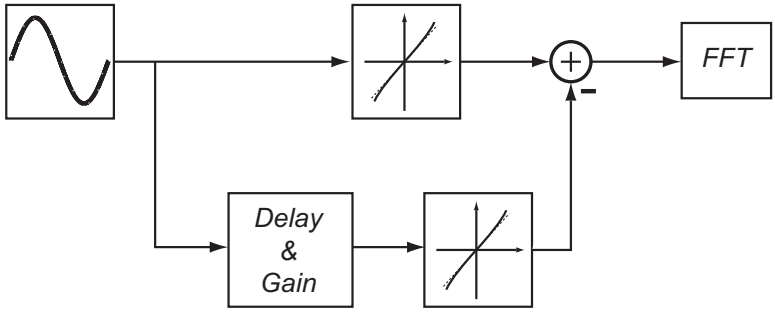


Figure 3.9: Test system to calculate maximum tolerable delay and gain deviation

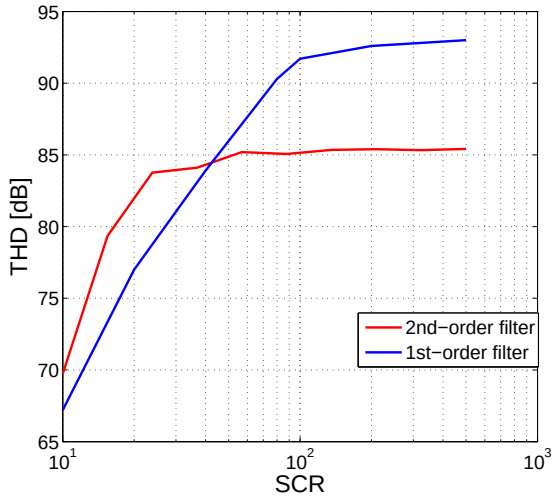


Figure 3.10: THD versus SCR for a 1^{st}-order modulator

filter and around 30 for the 2^{nd}-order filter, increasing sampling rate is not improving the THD significantly. This is because of the limitations that the filter imposes at the signal frequency, *i. e.* gain and phase shift.

Larger CIR results in less filter attenuation/delay at the signal frequency. Hence it can result in better linearity performance as shown in Fig. 3.11. In this figure, THD versus CIR is shown for both 1^{st} and 2^{nd}-order filters. For the 1^{st}-order filter SCR equal to 100 is considered while for the 2^{nd}-order one both poles are at the same frequency and SCR is 30. Since at a specified frequency a second-order filter introduces more attenuation/delay than a first-order filter with the same CIR the maximum achievable THD is lower.

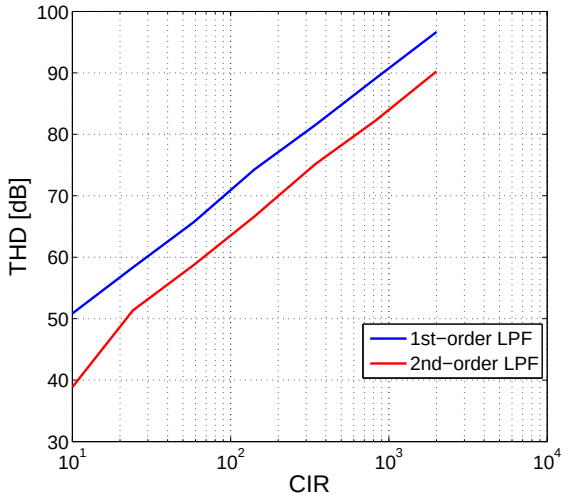


Figure 3.11: THD versus CIR for a 1^{st}-order modulator

3.5 2^{nd} order ΣΔM with filtered feedback signal

There are two different ways of implementing a 2^{nd}-order ΣΔ modulator with an input transconductor, either with the feed-forward (FF) or with the feedback (FB) compensation paths shown previously in Fig. 2.13. In fact a combination of these two is also possible but it is not popular since it does not have any advantage over each one. In the FF structure the output of the first integrator is the quantization noise while in the FB counterpart it includes the signal. Hence intrinsically the output swing of the first integrator is smaller in the FF structure. The disadvantage of this structure is that the feed-forward coefficient results to a zero in the loop and consequently a peaking in the STF can occur. Also the STF for a FB structure has a second-order filtering characteristics while the FF structure offers a first-order filtering.

In the applications where second-order anti-aliasing filtering is not required, FF structure seems to be more advantageous because of the inherent smaller swing. In sensor applications, anti-aliasing does not play an important role and FF topology is a good candidate for implementing a ΣΔ modulator. Each of the architectures mentioned in section 3.3 can be used in this topology to improve the linearity performance of the overall modulator. Two examples of 2^{nd}-order ΣΔ modulator are shown in Fig. 3.12.

The performance and the output swing of the integrators in structure of Fig. 3.12a are similar to a 2^{nd}-order CT feed-forward modulator, except that

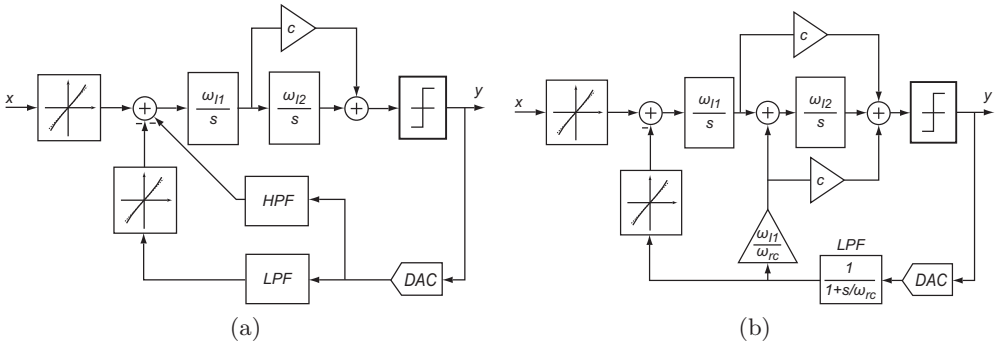


Figure 3.12: 2^{nd}-order feed-forward $\Sigma\Delta$ modulator topologies with improved linearity

the linearity is improved. In contrast, the output swing of the first integrator in Fig. 3.12b contains the input signal and it has a higher swing. That is because of the feedback signal which is supposed to be similar to the input signal. This swing can be decreased by decreasing the feedback coefficient, ω_{I1}/ω_{rc}. However at some point it is not possible, since decreasing ω_{I1} is possible with increasing the integration capacitor in the integrator and increasing ω_{rc} of the LPF requires increasing the sampling rate with the same factor.

In Fig. 3.13, THD as a function of SCR is plotted for both 1^{st} and 2^{nd}-order passive LPF while $ci = 1000$. The 2^{nd}-order filter obtains its maximum achievable THD faster since it has a sharper filtering characteristics. For $sc \geq 60$, the gain and delay introduced by the filter in the signal band is limiting the linearity. 1^{st}-order filter requires a higher SCR to saturate, but in contrast it can achieve a better linearity since it has one pole and introduces less attenuation and delay in the signal band.

In Fig. 3.14 the THD versus CIR is shown for a second-order modulator. SCR equal to 135 is chosen for this simulation. The results of this graph are similar to a first-order modulator since the effect of the filter is independent of the modulator order.

3.6 Conclusion

The delay and attenuation introduced by the filter is indeed independent of the order of the $\Sigma\Delta$ modulator. Figures 3.11 and 3.14 confirm this. They also confirm increasing the filter's corner frequency relative to the signal frequency results in a better THD.

On the other hand, the relations between the THD and SCR in figures

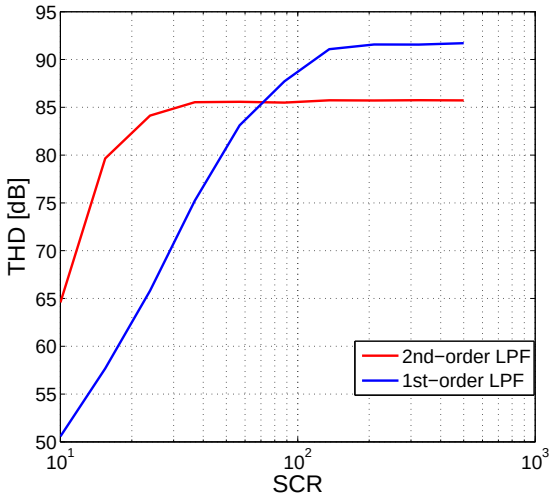


Figure 3.13: THD of 2^{nd}-order ΣΔ modulator as a function of SCR

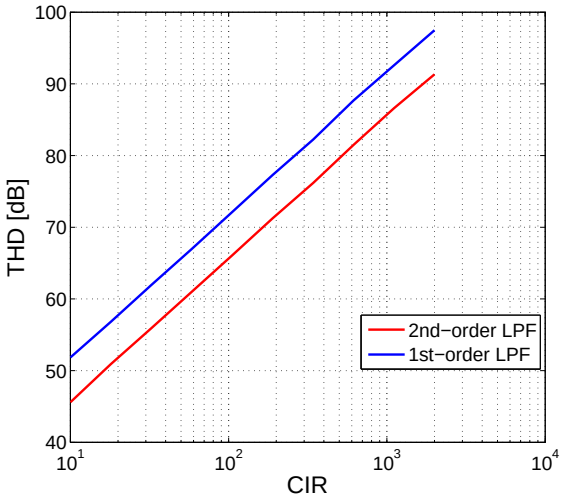


Figure 3.14: THD of 2^{nd}-order ΣΔ modulator as a function of CIR

Table 3.1: CIR and SCR ratios required to achieve 90dB THD in 1^{st} and 2^{nd}-order CT $\Sigma\Delta$ modulators

	LPF order	CIR	SCR	OSR
1^{st}-order $\Sigma\Delta$ modulator	1	900	100	45,000
	2	2000	30	30,000
2^{nd}-order $\Sigma\Delta$ modulator	1	800	135	54,000
	2	1700	30	25,500

3.10 and 3.13 show that for a given filter order and CIR ratio, increasing the modulator order does not decrease SCR significantly. In other words, to achieve a determined THD lower OSR is not obtained with a 2^{nd} order modulator. This is shown in table 3.1 for four different combinations and with the aim of achieving 90dB THD.

Chapter 4

1^{st} order $\Sigma\Delta$ modulator Implementation

As discussed in chapter 3, CT $\Sigma\Delta$ modulator has been chosen because of the advantages of high input-impedance and power-noise efficiency in comparison to DT implementations. In CT modulators with input Gm-stage, the nonlinearity of the Gm-stage goes through the system and can degrade the overall linearity performance. Thus this stages should be linearized according to the specifications, or with some technique their nonlinearity should be compensated. Here we have proposed to filter out the signal from the output bit-stream with a low-pass filter and improve the modulator's linearity by feeding the signal to the same nonlinearity in the feedback.

To find the best filter choice for our application, the filter options are reviewed and compared . According to the analysis shown in chapter 3, a 1^{st}-order single-bit $\Sigma\Delta$ modulator fulfills the desired linearity specifications without a significant increase in the OSR.

In this chapter, the implementation procedure is described and the bottlenecks and solutions are given. In the first section filter choices are evaluated and a first order filter is chosen. The overall circuit is determined next and individual block requirements are extracted from system level simulations. Issues concerning matching are described and solutions are discussed. Next the design of each block is described following the simulation results for the overall system. Layout is shown briefly in the last section.

Table 4.1: Comparison of LPF types in the system

LPF Type	Order	CIR	SCR	THD @10Hz	f_s
Passive	1	1000	100	90.1 dB	1MHz
Passive	2	2000	30	90.3 dB	600kHz
Active - Butterworth	2	1500	46.6	90.2 dB	700kHz
Active - Bessel	2	1700	47	90.8 dB	750kHz
Active - Bessel	3	2600	28.8	90.9 dB	750kHz

4.1 Filter corner frequency

The low-pass filter in the feedback has to remove the quantization noise from the output bit-stream and reproduce the analog input signal. Its corner frequency can be determined by considering two factors, *signal bandwidth* and *sampling frequency*. The non-idealities of the filter within the signal bandwidth can directly deteriorate the performance. The relation between the filter corner frequency and sampling frequency determines how much unwanted quantization noise passes through the filter.

For higher order filters, the pole frequencies should be increased since they introduce more delay and gain deviation from unity at low frequencies. On the other hand, because of better filtering characteristics, it is possible to decrease SCR. Hence there is a trade-off between the choice of filter order, its pole and sampling frequency of the modulator. In table 4.1 a comparison between passive and active filters with different orders is given. It is observable that for higher filter order, CIR should be increased to achieve the same performance while it is possible to decrease SCR. This relation leads to almost the same sampling frequency range.

Since the filter is located at the input of the feedback Gm-stage, the noise contributed from the filter directly adds up to the input referred noise of the ΣΔ modulator. Hence resistance values should be chosen small enough (in the range of $k\Omega$) to fulfill the noise performance. On the other hand the pole frequencies of the different filters are so low that with such resistance ranges, capacitance values in the range of nF are required, which is very large for integrated circuits. For each order increase, an additional pair of resistors and capacitors are needed and it means more external components, which is not desirable.

The amplifier of an active filter, introduces noise and power consumption while not improving the performance significantly. In addition, the requirement for external components is undesirable in integrated applications.

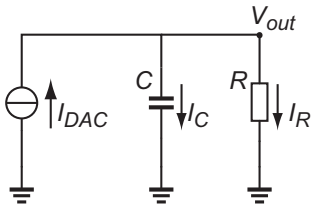


Figure 4.1: First order RC filter

Hence a first order passive filter is preferred which also has simpler implementation. For an application with a frequency band extending from dc to 10 Hz, the first-order filter's corner frequency should be at least 10 kHz to achieve a theoretical total harmonic distortion (THD) better than 90 dB. Corner radian frequency of 100 krad/sec, equivalent to about 16 kHz, is chosen in this design. As mentioned before, for noise considerations small resistors are desired for implementation.

On the other hand, the full-scale of the feedback signal is the multiplication of the filter resistor and current amplitude of the DAC. Hence for smaller resistor values, larger current should be dissipated in the DAC. To stay with a low thermal noise without dissipating too much power, the resistor is chosen to be in the range of $1/g_m$ which equals almost $2k\Omega$. Consequently the capacitor value has to be $5nF$ to implement a cut-off frequency of 16kHz.

4.2 Overall Circuit Topology

The block diagram of a 1^{st}-order $\Sigma\Delta$ modulator with low-pass and high-pass filters is described in section 3.3.1. Both LPF and HPF can be implemented with a combination of a resistor, capacitor and a current DAC as shown in Fig. 4.1. The voltage and currents shown can be calculated as follows:

$$I_R = I_{DAC}\frac{1}{1+sRC} \tag{4.1}$$

$$I_C = I_{DAC}\frac{sRC}{1+sRC} \tag{4.2}$$

$$V_{out} = I_{DAC}\frac{R}{1+sRC} \tag{4.3}$$

Eq. 4.3 shows that the voltage across the filter is a low-pass filtered version of the DAC signal while Eq. 4.2 shows that the capacitor current is a high-pass filtered DAC signal. This basic circuit can be used to implement the system in Fig. 3.5a, as illustrated in Fig. 4.2. In this figure, I_{fb-LF}

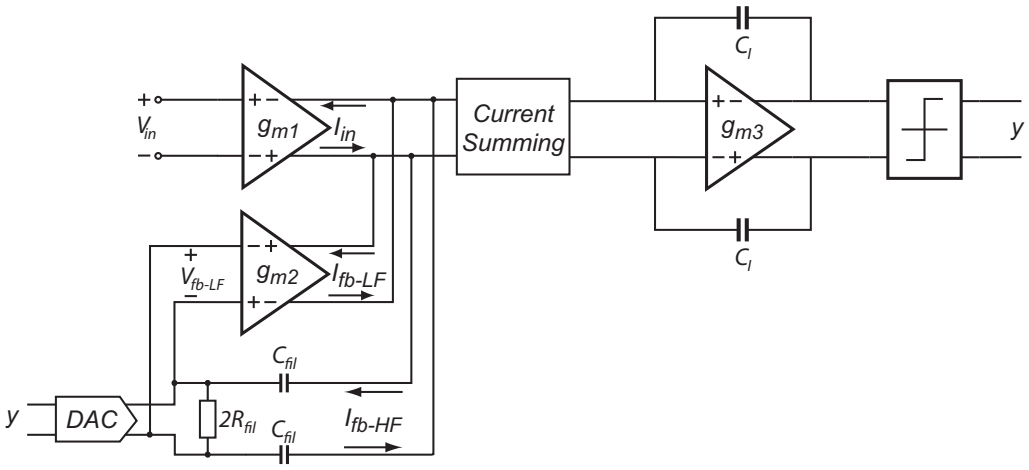


Figure 4.2: Circuit schematic of the system with parallel LPF and HPF

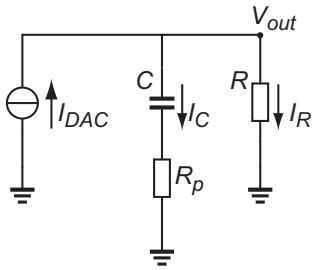


Figure 4.3: Non-ideal 1^{st}-order filter with parasitic resistor in series with capacitor

generated by the Gm-stage is the low-frequency feedback signal and the capacitor current, I_{fb-HF}, is the high-frequency feedback signal. The input and feedback Gm-stages are considered to be identical and the common part is regarded as a current summing (current buffer) block. The current of the capacitor can directly be added to the input of the current summing stage if its input impedance is small enough.

The finite input resistance of the current summing stage will result to a zero in the transfer function of the low-pass filter, which can limit the overall linearity performance. This zero simply means that the feedback signal is filtered weaker and more quantization noise can pass through the filter to the input of the Gm-stage. Hence the input of the feedback Gm-stage is a weaker estimate of the input signal and the nonlinearity generated in the input is not compensated completely.

The zero frequency can be found considering Fig. 4.3, where R_p is a parasitic resistor in series with the filter's capacitor. The currents and output voltage can be found as:

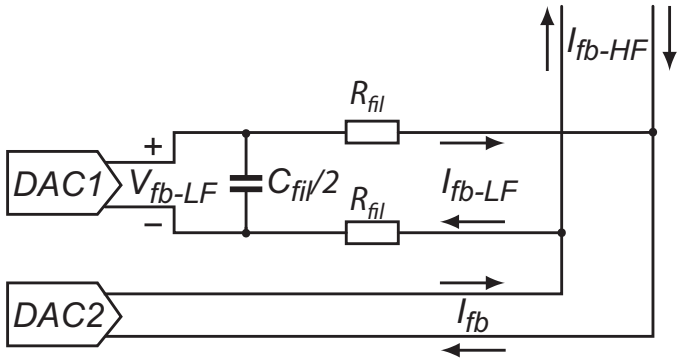


Figure 4.4: Separating high-frequency and low-frequency feedback paths

$$I_C = \frac{RCs}{1 + (R + R_p)CS} \tag{4.4}$$

$$I_R = \frac{1 + R_pCs}{1 + (R + R_p)CS} \tag{4.5}$$

$$V_{out} = R\frac{1 + R_pCs}{1 + (R + R_p)CS} \tag{4.6}$$

From Eq. 4.6 we can conclude that the ratio of the zero to the pole in the non-ideal filter is $R_p/(R+R_p)$. In order to achieve the best performance, the zero frequency should be higher than half the sampling frequency. Hence for a first-order filter, it can be inferred from table 4.1 that the ratio of the zero and the pole should be larger than 50. It translates to $R_p \leq R/50$ in Fig. 4.3.

Eventually because of the noise performance, the filter resistance value is chosen to be $2k\Omega$. Hence to have a zero frequency 50 times greater than the pole, the input resistance of the current summing stage should be less than 40Ω. In a designed gain-boosted current summing stage this is 120Ω which is not low enough for our purpose.

An alternate implementation of the system is shown in Fig. 3.7. Systematically it is equal to the previous architecture and the performance is the same. To implement the subtraction for high frequency path, we need two IDAC blocks which must have exactly the same characteristics. First order RC filter is connected to one of them and the current of the resistor (low-frequency signal) is subtracted from the current of the other IDAC as shown in Fig. 4.4.

Overall circuit including this scheme is shown in Fig. 4.5. As illustrated in this figure, the low-frequency paths are isolated from the IDAC path by the current summing stage. The reason to isolate these two paths is that

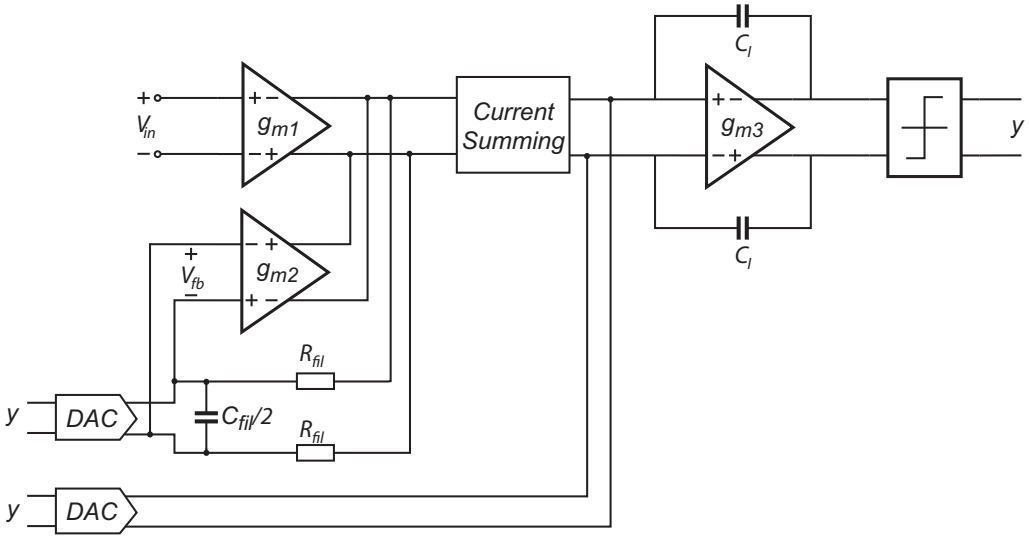


Figure 4.5: Overall 1^{st}-order CT ΣΔ modulator with improved linearity

if they are not separated, the pulse shaped current of the IDAC generates voltage spikes at the virtual ground node of the resistors and it results to distortion. With the current summing stage acting as a current buffer, these spikes are attenuated in the summing node and their effect is negligible.

The other advantage of the second solution is that it can be implemented by one capacitor which has a value of $C_{fil}/2$ in comparison to the first approach which needs two capacitances of value C_{fil}.

4.3 Circuit blocks specifications

4.3.1 Input and feedback transconductors

A good candidate for the input and feedback Gm-stages is a simple differential pair as will be described in section 4.5.1. Such a block is designed in CADENCE to evaluate it's linearity characteristics and exploit the results in the system analysis. The input referred thermal noise of this stage is proportional to $1/g_m$ and to fulfill the resolution requirement, $g_m = 0.5mS$ is chosen. The input of the designed Gm-stage is swept with dc signal and the resulting g_m as a function of input differential voltage is shown in Fig. 4.6. This data is used in MATLAB to fit the nonlinearity with a polynomial which was also used in simulations in previous sections.

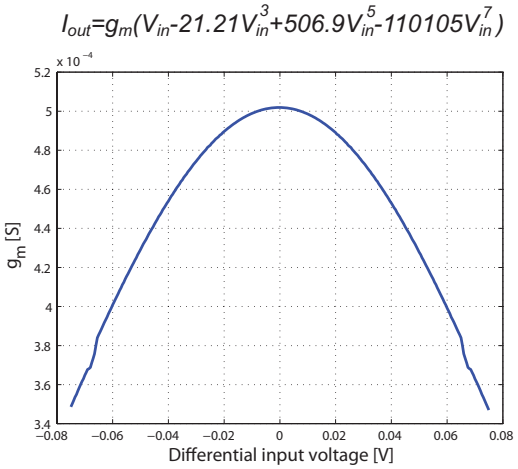


Figure 4.6: Input g_m Vs. the input differential voltage

4.3.2 Integrator

Mentioned in section 4.1, the best range for the filter resistance is $1/g_m$ which equals to $2k\Omega$. Also $100krad/sec$ is chosen for the corner frequency in the RC-filter. With these values, the capacitor $C_{fil}/2$ in Fig. 4.5 can be calculated to be $2.5nF$.

Taking into account a margin for the linearity performance, the sampling frequency is chosen to be $1.25MHz$. The output swing of the integrator is determined by its unity gain frequency and the sampling rate. In order to make the swing less than $2V_{p-p}$, the unity gain frequency of the integrator should be less than $10Mrad/sec$. In Fig. 4.5 the unity gain frequency of the integrator is g_m/C_I where g_m is the transconductance of the input or feedback Gm-stages. Hence the integration capacitor should be at least $50pF$ to limit the swing to $2V_{p-p}$.

4.3.3 Amplifier of the active integrator

In first-order DT $\Sigma\Delta$ modulators the maximum dead zone in the DC characteristics is inversely proportional to DC gain of the amplifier in the integrator. Hence to achieve INL in the range of 100ppm, a DC gain better than 80dB is required. In contrast, in CT modulators based on a passive (gm-C) integrator, the integrator leakage p, is determined by the DC output impedance of the transconductor R_{out}, the integrating capacitor C_{int}, and the sampling frequency f_s [22]:

$$p = e^{-1/f_s R_{out} C_{int}} \tag{4.7}$$

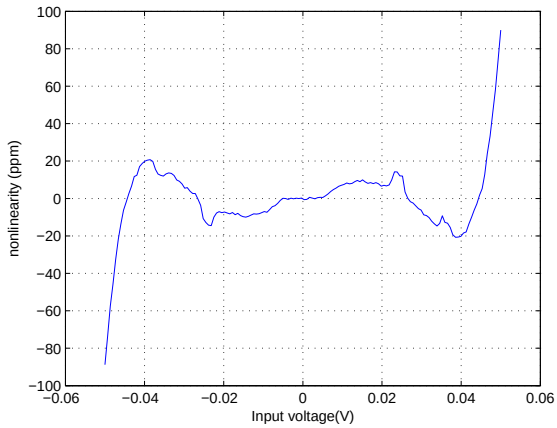


Figure 4.7: INL plot of the 1^{st}-order ΣΔ modulator

In CT modulators based on active integrators, the DC gain of the amplifier constructing the integrator, A_0, also takes part in the equation:

$$p = e^{-1/A_0 f_s R_{out} C_{int}} \tag{4.8}$$

The width of the widest dead band Δx, in the modulator's DC characteristics normalized to its reference is given by [23]:

$$\Delta x = \frac{1-p}{1+p} \tag{4.9}$$

As an example with a sampling rate of 1MHz, DC output impedance of $2G\Omega$, amplifier DC gain of 60dB and $C_{int} = 50pF$ the dead band is 5×10^{-6} of the reference value. This is equivalent to 5ppm error in the INL curve. INL is found in ppm by the following equation:

$$INL = 10^6 \frac{|y_{out-actual} - y_{out-ideal}|}{V_{Full-scale}} \tag{4.10}$$

INL plot for $f_s = 1.25MHz$, $A_0 = 60dB$ and $C_{int} = 50pF$ is shown in Fig. 4.7. The DC output impedance is considered to be ideal, infinite, and it can be seen that the INL is not limited by the dead bands. The input nonlinearity is the source of 20ppm INL.

The unity gain bandwidth (UGBW) of the amplifier in the integrator is an important determinant of the AC distortion and noise shaping characteristics of the modulator. It can change the pole location of the loop and consequently the noise shaping will be less effective. For a limited DC gain of A_0 and unity gain frequency of ω_u, the transfer function of the integrator can be found as follows:

$$Int(s) = \frac{g_m/C_I}{s\left(\frac{s}{\omega_u} + p\right)} = \frac{\omega_I}{s\left(\frac{s}{\omega_u} + p\right)} \tag{4.11}$$

Where g_m is the input transconductance, C_I is the integration capacitor and $p = 1 + 1/A_0$. The ideal transfer function for the integrator is ω_I/s and it can be approximated by Eq. 4.11 if $\omega_I \gg \pi f_s$ and $A_0 \to \infty$.

From simulations, UGBW larger than the unity gain frequency of integrator (g_m/C_I) is adequate for the desired performance. Its value from the overall schematic given in Fig. 4.5 is g_{m3}/C_I, where g_{m3} is the effective transconductance of the OTA. Hence in order to achieve the desired results, g_{m3} should be larger than g_m.

4.3.4 Quantizer

The maximum tolerable quantizer delay is also examined. It is done by simply introducing an arbitrary delay to the output of the quantizer. It is found that for delays smaller than 1/5 of the sampling period, the effect on performance is negligible.

4.4 Circuit implementation issues

Any mismatch in the input and feedback Gm-stage will degrade the overall linearity since the nonlinearity generated by them is different and is not compensated completely. On the other hand mismatch in DAC currents will be appeared as a zero in the LPF transfer function which also affects the linearity performance. In section 3.1, concept of DEM is explained as a technique to improve the matching between devices. In this section the effect of mismatch in Gm-stages and IDACs is evaluated and the improvement due to DEM is verified with simulations.

4.4.1 Mismatch in gm-stages

So far in the system analysis no mismatch in the input and feedback Gm-stages is considered. The general idea on improvement in the linearity is that if identical nonlinearity is present at the input and feedback paths they will compensate each other and the linearity performance will be improved as verified in the previous sections. Hence any mismatch in these stages means that the nonlinearity can not be compensated and consequently the overall achievable linearity will be limited.

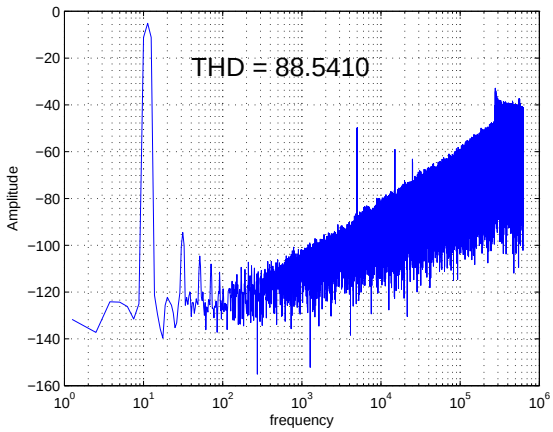


Figure 4.8: Output spectrum of the modulator including 1% mismatch in the Gm-stages and DEM at $5kHz$

To investigate the effect of the mismatch, 1% intentional change in the current source of the Gm-stage designed in CADENCE is made and the dc input is swept to formulate the nonlinearity. If identical nonlinearity is used in both input and feedback, for sampling rate of $1.25MHz$ and pass-band frequency of $16kHz$ in the first-order filter, THD equal to 89dB is achievable at 10Hz input signal. If one of the feedback or input stages is changed with the nonlinearity including 1% mismatch, THD under the same conditions is degraded to $78dB$.

Dynamic element matching can be applied to the Gm-stages to modulate their mismatch error to the DEM frequency. Using this technique, THD can be recovered to almost the ideal case. The spectrum of the output including mismatch in the Gm-stages and DEM at $5kHz$ is given in Fig. 4.8.

4.4.2 Mismatch in IDACs

Mismatch in the current amplitude of the IDACs translates to displacement of the zero in the HPF. Consider in Fig. 4.4 that IDAC1 and IDAC2 have current amplitudes equal to I and $I+\Delta I$, respectively. Hence the following equations hold:

$$I_{fb-LF} = I\frac{1}{1+R_{fil}C_{fil}s} \tag{4.12}$$

$$I_{fb} = I + \Delta I \tag{4.13}$$

$$\begin{aligned} I_{fb-HF} = I_{fb} - I_{fb-LF} &= \frac{R_{fil}C_{fil}s}{1+R_{fil}C_{fil}s} + \Delta I \\ &= \frac{\Delta I + (I+\Delta I)R_{fil}C_{fil}s}{1+R_{fil}C_{fil}s} \end{aligned} \tag{4.14}$$

Eq. 4.14 shows that the zero for high frequency path is:

$$z_{HF} = -\frac{\Delta I}{(1+\Delta I)R_{fil}C_{fil}} \tag{4.15}$$

Note that for ideal case, when there is no mismatch in the current amplitudes, the zero is located at dc. However in practice, in the presence of mismatch in the current amplitudes, the zero shifts to a higher frequency, thus limiting the improvement in the linearity.

When the zero is at dc in the high frequency path, the signal and its harmonics are maximally rejected from this path and they must pass or be generated in the low frequency feedback path. In this case, the maximum linearity can be achieved. In contrary, when the zero is at frequencies higher than the bandwidth, the suppression is less and more signal and harmonics can pass through high frequency feedback resulting in worse linearity.

Solution to improve the matching in the DACs, similar to the Gm-stages is applying DEM. By interchanging the DACs periodically, the matching can be enhanced considerably. Eq. 4.14 gives the high-frequency current in one mode and for the case that the currents of DAC1 and DAC2 are changed, it becomes:

$$I_{fb-HF} = \frac{IR_{fil}C_{fil}s - \Delta I}{1+R_{fil}C_{fil}s} \tag{4.16}$$

If the period of each mode is equal, the mean value can be found from Eq. 4.14 and 4.16:

$$\begin{aligned} \bar{I}_{fb-HF} &= \frac{\Delta I + (I+\Delta I)R_{fil}C_{fil}s + IR_{fil}C_{fil}s - \Delta I}{2(1+R_{fil}C_{fil}s)} \\ &= I\frac{R_{fil}C_{fil}s}{1+R_{fil}C_{fil}s} \end{aligned} \tag{4.17}$$

The zero will be located at dc after applying DEM. However we should note that we could made an optimistic assumption in this analysis. That is about the magnitude of mismatch in two modes. Because of the limited output impedance in the current sources in the DAC, the current amplitude changes between two modes if the common-mode level is different at the output of the DACs. When the mismatch is different, the zero is moved to

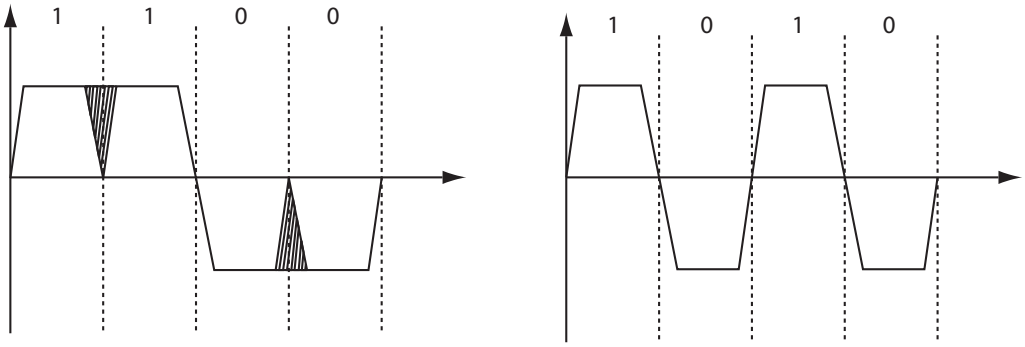


Figure 4.9: non-return to zero feedback signaling

a lower frequency instead of dc. In the implementation of IDACs in section 4.5.3, it is described how the mismatch can be made as small as possible.

4.4.3 Inter-symbol interference

Inter-symbol interference (ISI) is an issue related to DAC signaling in CT ΣΔ modulators. There are two types of DAC signals called non-return to zero (NRZ) and return-to-zero (RTZ). The former suffers from the ISI while the later is more sensitive to clock jitter.
In practice the DAC signal has a limited rise and fall time. This means that in NRZ case the effective power of each DAC feedback signal depends on whether there is a transition or not. As an example, as shown in Fig. 4.9, the energy of a "1100" sequence would be different from a "1010" pulse train. The difference is shown shadowed in the figure. Such a pattern dependent DAC signal introduces errors that are not shaped in the loop.

This problem can be solved by RTZ DAC signaling. In this technique in each sampling period the DAC feedback signal is reset to zero (i.e. no signal is injected to the feedback nodes). Hence the feedback signal power in each sampling period is independent from the previous one. The previous sequences are shown in Fig. 4.10 with RTZ method.

4.5 Transistor level blocks

The specifications required for each block are found in section 4.3. A topology for each block according to the specifications can be chosen and designed. Design of different blocks and additional considerations are explained in this section. To investigate and verify the understanding of the system, this work is implemented in a $0.7\mu m$ CMOS technology with low-threshold PMOS devices.

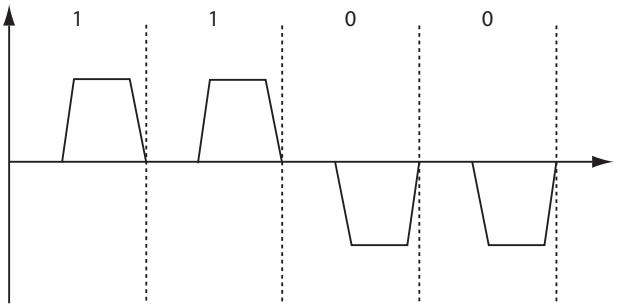


Figure 4.10: Return-to-zero feedback signaling

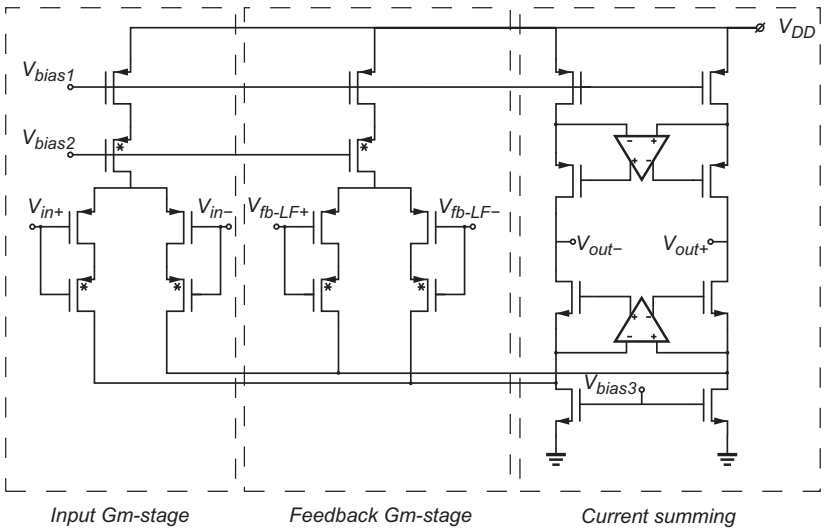


Figure 4.11: Simple differential Gm-stages for input and feedback paths

4.5.1 Input and feedback gm-stages with current summing

In Fig. 4.11, the input and feedback Gm-stages are shown together with the current summing block [24]. The Gm-stages are exploiting low-threshold transistors in order to make the transconductance insensitive to the input common-mode voltage. The current of the input transistors is determined by the tail current sources. The gate-drain voltage of the normal transistors are made constant by the low-threshold transistors and consequently their drain-source voltage is constant. The constant current and drain-source voltages result to the gm value independent of input CM level.

The Gm and current summing blocks are forming a gain-boosted folded cascade amplifier. There are two main reasons for gain-boosting; one is the suppression of the $1/f$ noise from following stages and the other is that the reduced input resistance of the current summing stage. The input resistance is important as this determines the virtual ground node of the resistor in

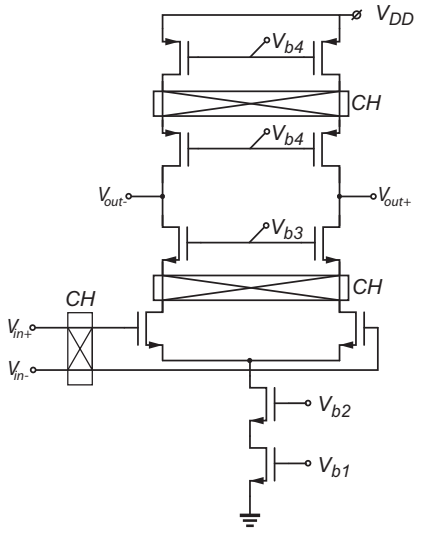


Figure 4.12: Telescopic operational amplifier

the filter. Since the filter's resistance is about $2k\Omega$ a parasitic resistance in the order of $k\Omega$ can change the frequency significantly. Using the gain-boost technique, the input resistance is decreased from a few $k\Omega$ to about 120Ω making it non dominant in the corner frequency of the filter.

4.5.2 OTA in active integrator

Determined in section 4.3 the gain of the OTA constructing the integrator should be higher than 60 dB because of the dc linearity specification. On the other hand the speed requirement puts the limitation to have a transconductance larger than the input transconductance, $0.5mS$, and the output swing in the system level simulations is determined to be $2V_{p-p}$. A telescopic amplifier shown in Fig. 4.12 can fulfill all these requirements.

In the figure, choppers are also included which will be discussed in the following sections. The input CM level is set on $1.7V$ from the previous stage and a resistive-capacitive common-mode feedback (CMFB) is used to set the output CM level on $2.9V$.

4.5.3 IDACs

Single-bit current steering DAC used in the feedback path is shown systematically in the Fig. 4.13a. This IDAC consists of two current sources and six switches. Two of the switches perform return-to-zero phase, which is explained in section 4.4.3. Thus the differential output current chooses one of the 0, $2I_{DAC}$ or $-2I_{DAC}$ values according to the digital words.

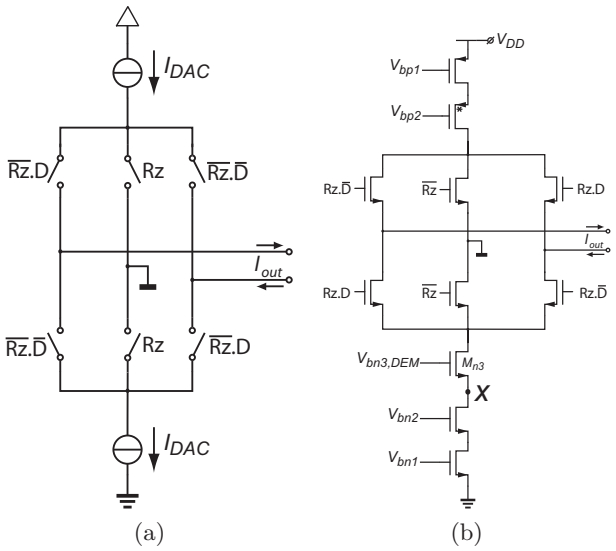


Figure 4.13: (a)System and (b)circuit of the current steering DAC

The circuit implementation of the IDAC is shown in Fig. 4.13b. Since the highest output CM voltage is less than $2V$ from a $5V$ supply, all the switches are implemented by NMOS transistors.

In section 4.4.2 the effect of the mismatch in the IDACs is explained and applying DEM is suggested as a solution to increase the matching property. In the overall circuit, there are two IDACs connected to two different nodes with different CM levels. Since the output resistance of the IDAC is limited, interchanging one of the IDACs between two nodes will change its current value and consequently the mismatch will not be improved as expected. In our simulation it was found that a 0.5% change in the currents of the NMOS transistors occurs while less than 0.1% change happens in the PMOS side.

An additional transistor, M_{n3} in Fig. 4.13b, is added to the structure to make the potential of node x independent from the output CM level. When IDAC is connected to the node with lower CM level, M_{n3} acts as a switch while in the other mode it is a cascode transistor and the biasing is such that the node x will have the same potential. Hence the current of the NMOS transistor will experience less change. With this method the NMOS current difference in two modes is less than 0.1%.

4.5.4 Quantizer

The quantizer chosen for this implementation consists of three stages; preamp, comparator and latch. The first two stages are shown in Fig. 4.14a and the latch is shown in Fig. 4.14b. The input stage provides a gain in the range

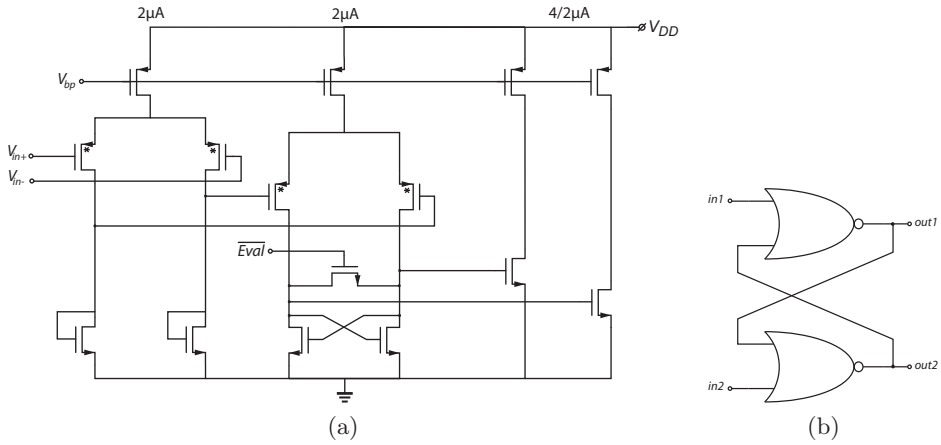


Figure 4.14: (a)pre-amp and comparator stages and (b) latch

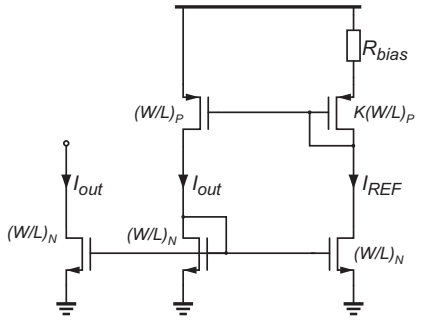


Figure 4.15: Constant-gm biasing provides bias for all the blocks

of 2-5 and it suppresses the kick-back effect. The overall quantizer delay is about $100nS$ which for a $1.25MHz$ clock signal, corresponds to $T_s/8$ time delay.

As determined in the schematic, the pre-amp and comparator dissipate less than $8\mu A$ from a $5V$ power supply.

4.5.5 Biasing

Constant-gm biasing is chosen to provide current for the whole system. A simplified schematic of this biasing circuitry is shown in Fig. 4.15. The output current of this system after some calculation can be found as following [21]:

$$I_{out} = \frac{2}{\mu_n C_{ox}(W/L)_N} \cdot \frac{1}{R_{bias}^2} \left(1 - \frac{1}{sqrt(K)}\right)^2 \tag{4.18}$$

Where R_{bias} is the resistor in biasing circuitry and K is the ratio of the PMOS transistor sizes. If the current of the input and feedback Gm-stages is

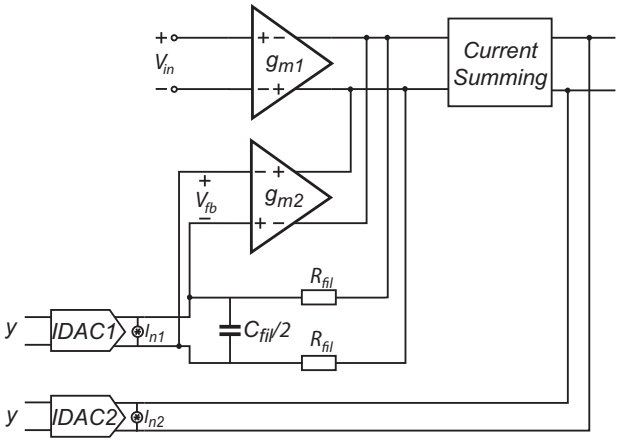


Figure 4.16: Current noise sources of IDACs

provided with a mirror ratio of the biasing output current, their transconductance will be inversely proportional to R_{bias} since $g_m = sqrt(2kI_D)$. Hence in order to make the filter resistance in the range of $1/g_m$, as concluded in section 4.2, it is necessary to match it with the biasing resistance. Careful layout consideration can match these resistors.

4.6 Noise Analysis and Chopping

The input referred noise of the input and feedback Gm-stages together with the current summing block is less than $7.3nV/\sqrt{Hz}$ in all the corners. The filter resistances together have an input noise level of $8nV/\sqrt{Hz}$. The high gain of the input Gm-stage, suppresses the noise of the following stages to a negligible value.

The input referred noise of the each IDAC is about $80nV/\sqrt{Hz}$. The input referred noise of the IDACs are an order of magnitude larger than other blocks and they can dominate the noise floor. Hence here only their noise sources are considered which can be considered as two noise current sources I_{n1} and I_{n2} as shown in Fig. 4.16. The input referred noise of IDAC1 consists two terms:

$$V_{inn,IDAC1} = \frac{I_{n1}}{g_{m1}} + I_{n1} \times R_{fil} \times \frac{-g_{m2}}{g_{m1}} = I_{n1}\left(\frac{1}{g_{m1}} - R_{fil}\right) \tag{4.19}$$

The design and layout have been such that R_{fil} is approximately equal to $1/g_{m1,2}$. Thus this term is canceled significantly. Only the noise from IDAC2 remains which is referred to input with I_{n2}/g_{m1} which is $80nV/\sqrt{Hz}$

Flicker noise corner frequency is the other parameter to be concerned in the noise performance. In the $0.7\mu m$ CMOS process used for this design, the flicker corner frequency for PMOS devices is in the range of a few kHz. Explained in section 3.1, offset and low frequency errors such as flicker noise can be modulated to a higher frequency using chopping. The first stage, consisted of the input and feedback Gm-stages with the summing stage is chopped. Simulations show that the flicker noise corner frequency after chopping is less than $1Hz$.

The flicker noise sources, except the input and feedback Gm-stages, are the IDACs and the OTA in the active integrator. Choppers are included in the OTA to assure their flicker noise does not dominate. Chopping the IDAC is not possible, but it's flicker noise is being chopped by the bit-stream. If the number of ones and zeros in the bit-stream is equal, the flicker noise is suppressed significantly. However if the input has a DC value, this noise source dominates and determines the corner frequency of the flicker noise.

The whole circuit block diagram, including the choppers and DEM is given in Fig. 4.17. DEM of the Gm-stages is implemented by enabling two of the choppers at the input periodically.

4.7 Circuit level simulations

CADENCE simulations for the circuit-level system are shown in Fig. 4.18. In this simulation no non-ideality, such as offset or mismatch, is considered. The sampling frequency is at 1MHz and the corner frequency of the filter is at 16kHz. The input sine wave has an amplitude of 40mV and NRZ feedback is applied.

In Fig. 4.19 the simulation results at three different input frequencies for both non-return to zero and return-to-zero feedback signaling are shown. The simulations should be accurate and samples in the order of million are needed for each data point. Thus only for a few points the simulations are done.

Simulation result for the system including the chopping at 25kHz, DEM Gm-stages at 2.5kHz and IDACs at 10kHz, 2mV input referred offset and 1% mismatch in the input and feedback Gm-stages is shown in Fig. 4.20. NRZ feedback is used and it can be seen with the added non-idealities that the noise floor has increased to about -100dB. Two different effects can cause this issue; intermodulation and inter-symbol-interference(ISI).

Intermodulation can occur between DEM/chopping tones and quantization noise. It can be prevented by carefully choosing the DEM and chopping

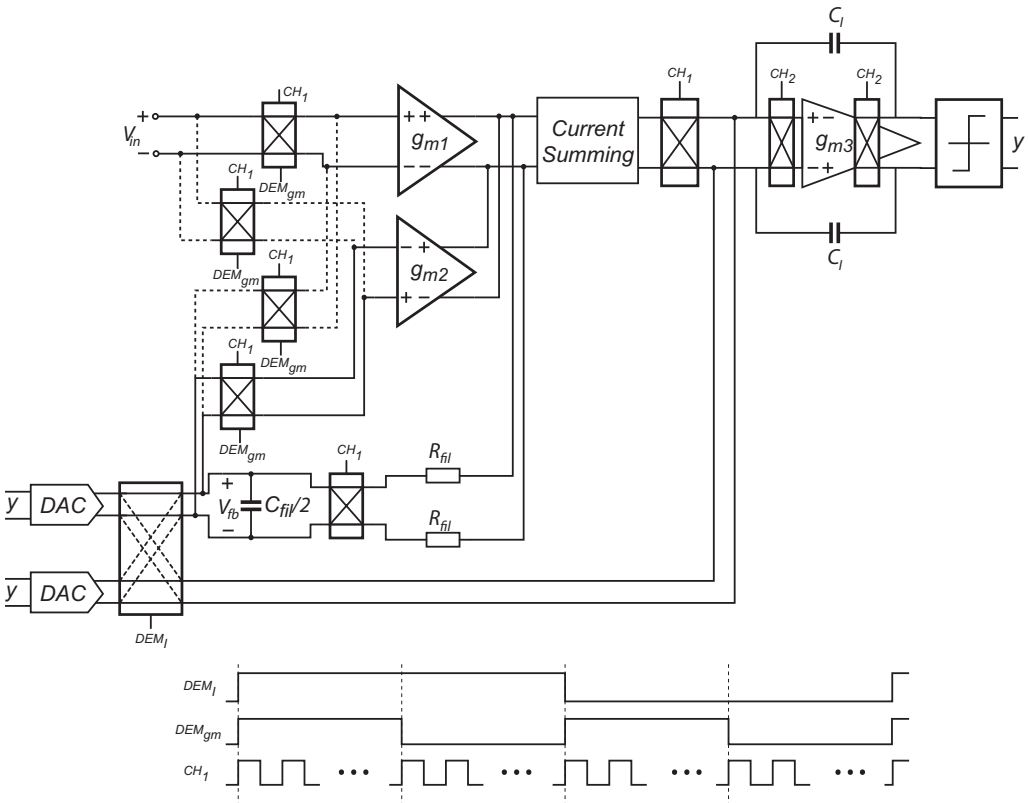


Figure 4.17: Overall circuit including the choppers and DEM

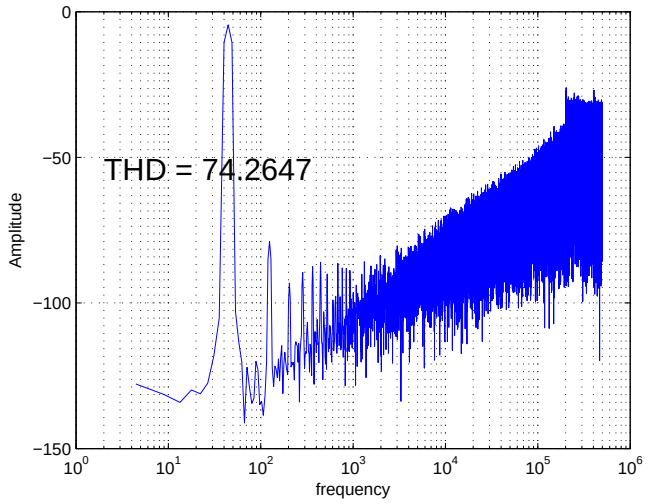


Figure 4.18: Circuit level simulation without offset and mismatches

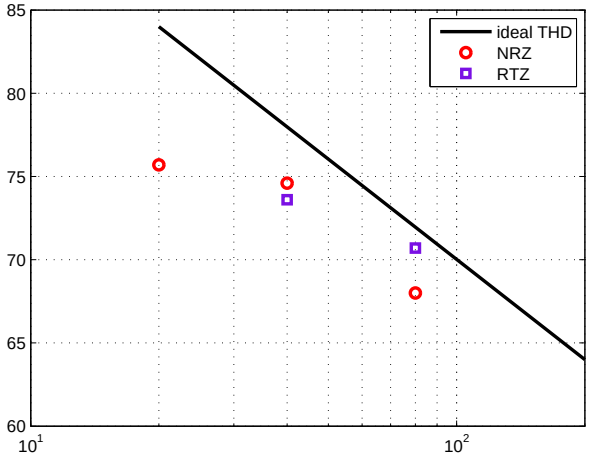


Figure 4.19: Simulation data points for ideal, non-return to zero and return-to-zero case

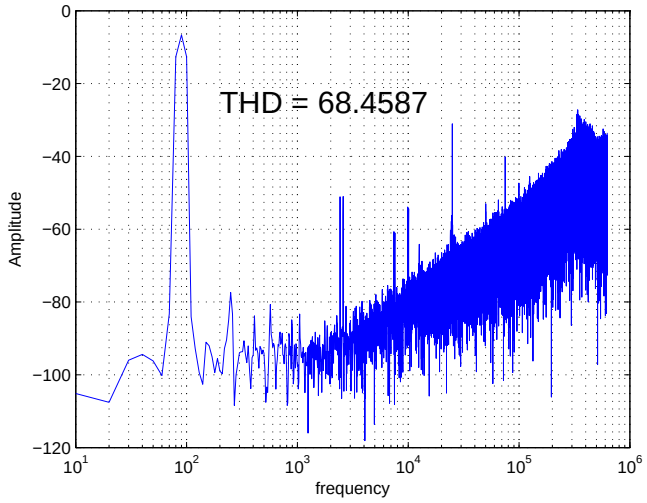


Figure 4.20: System simulation with NRZ feedback, DEM and chopping

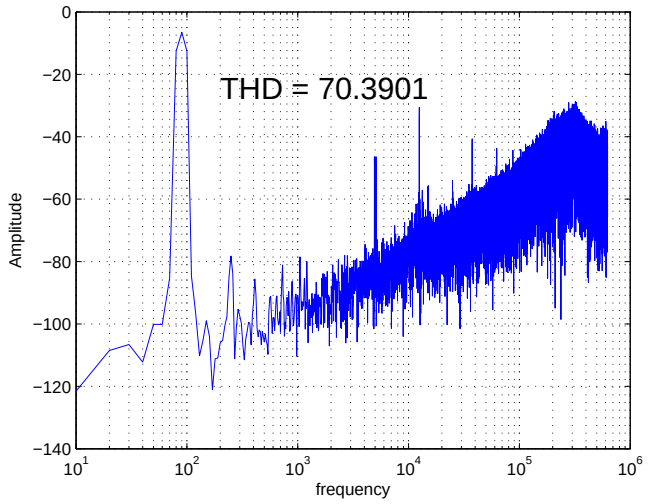


Figure 4.21: System simulation with RTZ feedback signal, chopping and DEM

frequencies so that their main tone or harmonics do not fall on each other or at high frequency with high quantization power.

ISI happens because of the non-zero rise and fall time in the DAC. However, since no intentional mismatch in the rise and fall time of the IDACs is made, the effect of ISI is less than reality. As explained in section 4.4.3, this effect can be overcome with RTZ feedback.

Simulation result with 50% RTZ feedback signal is shown in Fig. 4.21. The noise floor in this spectrum seems to be less than -110dB.

Chapter 5

Measurement results

The $\Sigma\Delta$ modulator was fabricated in a $0.7\mu m$ CMOS technology to investigate and verify the design. In this chapter the measurement setup is described followed by measurement steps to figure out the improvement in the linearity. Different test modes are experimented and finally a comparison between this work and others is given.

5.1 PCB design

To characterize the fabricated chip, a 4-layer printed circuit board (PCB) is made. The components on the PCB other than the designed chip are:

- *CPLD* A CPLD is used on the PCB to generate the signals and clock. For this purpose a product of the MAX7000 family of ALTERA is chosen which can have a clock frequency of 128MHz. Every control signal of the $\Sigma\Delta$ modulator such as sampling clock, RTZ, chopping and DEM, is generated in this CPLD.

- *Buffers* There are three buffers used in the PCB, two of which are digital buffers and one is an analog buffer. The digital buffers are between the CPLD and the chip to make the clocks sharper and also to modify the signal levels. The output of the CPLD has a high voltage of 3.3V and the digital buffers can also work as level shifters to increase the signal amplitude. Analog buffer is used at the output of the integrator to avoid loading the integrator when probing its output.

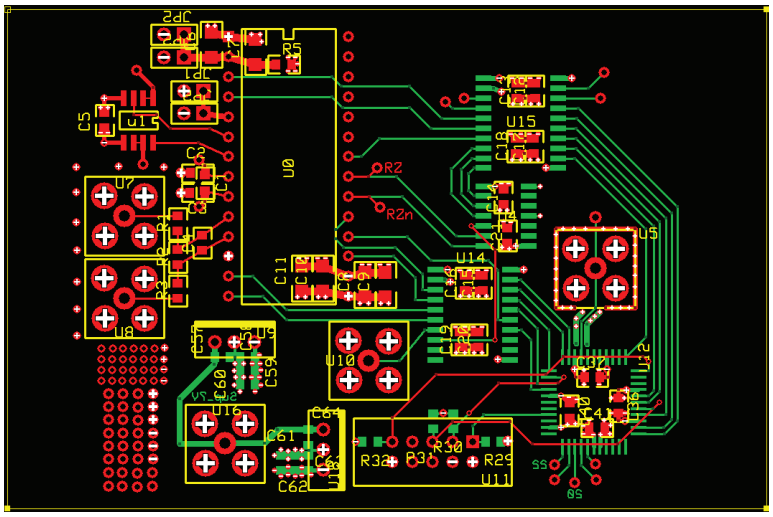


Figure 5.1: The test PCB layout

- *D flip-flop* To generate the inverting signals for RTZ signaling a D flip-flop is used on the PCB. Its advantage is that because of the latch at its output the inverting signals have very good timing.
- *Regulator* Two 5V regulators are used on the PCB to generate the supply for analog and digital circuits separately.
- There are also other components such as jumpers, supply coupling capacitors, ribbon connector for programming the CPLD, SMB connectors and resistor divider at the input connection.

In Fig. 5.1 the layout of the PCB is shown. The high frequency digital signals are on one layer and the analog signals are traced on the opposite layer. In between these two layers are the ground and supply layers. The ground is used commonly for analog and digital blocks.

5.2 Measurement results

The low-pass filter implemented in the feedback of the $\Sigma\Delta$ modulator for the purpose of improvement includes external capacitors. The reason is that this filter has a corner frequency of 16kHz and the resistor should be in the range of $2k\Omega$ because of noise considerations. Hence we have freedom to choose the capacitor or even remove it.

The advantage of removing the capacitor is that the system becomes a conventional modulator with input Gm-stage. As shown in Fig. 5.2, if the capacitor is removed, the current of the two IDACs will cancel each other

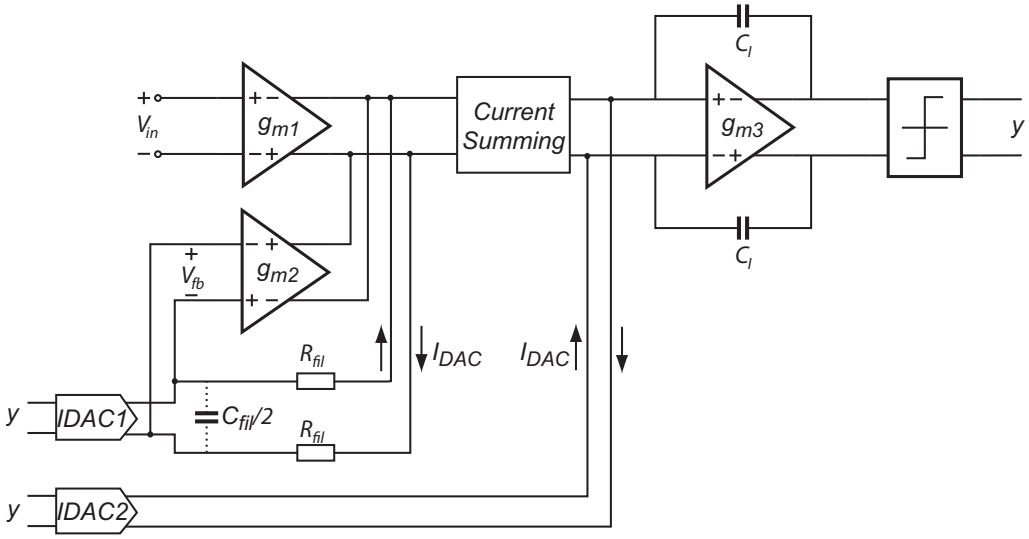


Figure 5.2: Overall ΣΔ Modulator

since they have different polarities in the loop. However, IDAC1 will produce a differential voltage on the resistors R_{fil} and this voltage is connected to the feedback transconductor. This transconductor will generate a 2-level output current that depends on the bit-stream, which is equivalent to a feedback DAC. Hence we can figure out the effect of the proposed method by simply measuring the linearity with and without the capacitor.

According to the measurements, the input residual offset with chopping changes linearly with the sampling frequency. This is shown for three random samples in Fig. 5.3. The chopping frequency for this measurement is chosen to be at $f_s/64$. To understand whether the change is a result from sweeping the sampling frequency or the change in chopping frequency is also effective, the positive and negative input offsets without chopping are measured. The residual offset after chopping should be the middle point of this two values. This is shown for two samples in Fig. 5.4. From this figure we can conclude that the offset is dominantly determined by the sampling frequency.

The reason for this relation is a non-ideality that happens once in each sampling period, such as a settling error or a timing error in the controlling signals. Doubling the sampling period makes the offset half since this error is distributed over a double time interval.

Inspecting the integrator output, it was found that the CM output does not settle fast. In Fig. 5.5a the differential and single-ended integrator output at 800kHz is shown and in Fig. 5.5b the same signals at 300kHz are

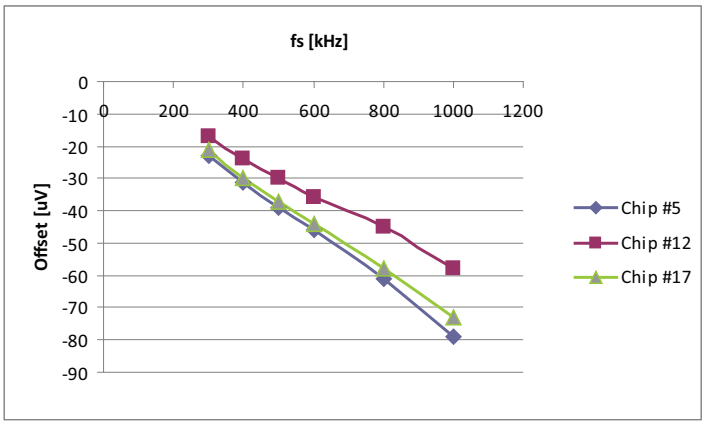


Figure 5.3: Residual offset with chopping at $f_s/64$ as a function of sampling frequency

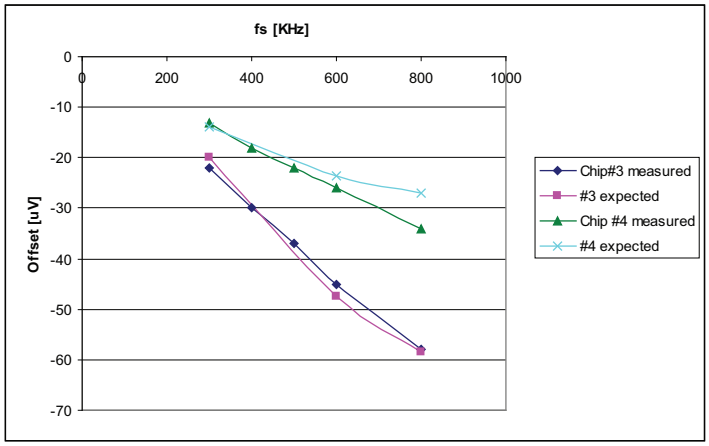
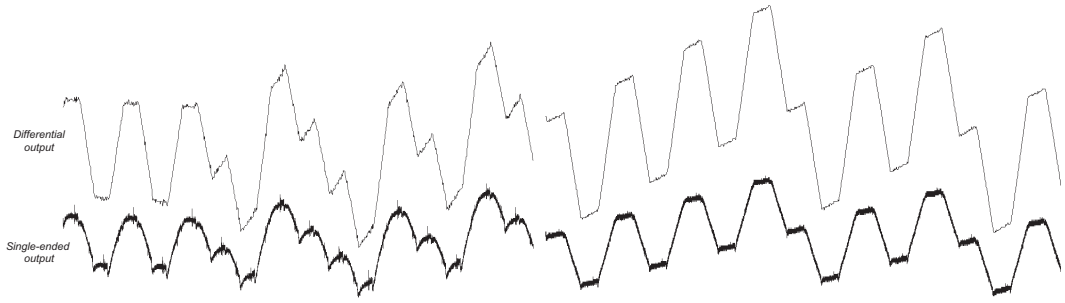


Figure 5.4: Measured and expected values for offset at different sampling frequencies

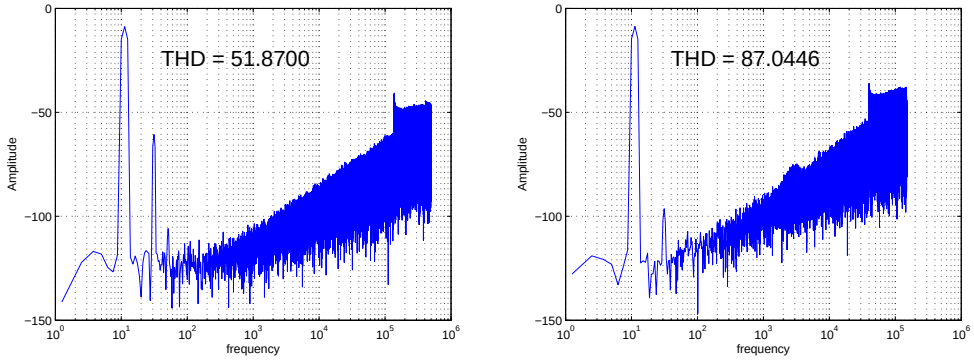
shown. The CM error can be translated to offset and even-order harmonics since there are always mismatch in the two differential paths. Still the systematic offset does not seem to be from this settling error, because if the mismatch is the reason the offset should have both positive and negative values.

In the simulation steps, the design was done for an input full-scale of about 100mV when NRZ feedback was going to be used. In the measurements, the performance is very poor for NRZ case and an RTZ feedback signal with a 50% duty cycle is used. Hence the input range is half and the transconductor at the input and feedback are more linear at this range. From MATLAB simulations for an input sine wave of 22mV, THD equal to



(a) (b)

Figure 5.5: Differential and single-ended output swing of the integrator at f_s of (a) 800kHz and (b) 300kHz



(a) Without low-pass filter (b) With filter ($f_{rc} = 8kHz$)

Figure 5.6: MATLAB simulation with 22mV input sine wave

51.8dB without filter and 87dB with filter is obtained as shown in Fig. 5.6. This is very close to the measurement values shown in the following.

In the measurements the proposed method for linearity works better at lower sampling frequency. The system was designed to be able to work at $f_s = 1.25MHz$ and improve the THD by 30dB, but the chip at this frequency can improve the THD by about 20dB. The measurements show that better than 30 dB improvement can be obtained at sampling rates lower than 600kHz. Considering also the residual offset after chopping, sampling at 300kHz becomes a good operating point. Since the sampling frequency is decreased, the corner frequency of the low-pass filter should also be decreased. Thus the external capacitor is increased to achieve the desired linearity. $C_{fil} = 10nF$ offers a good performance which is going to be described.

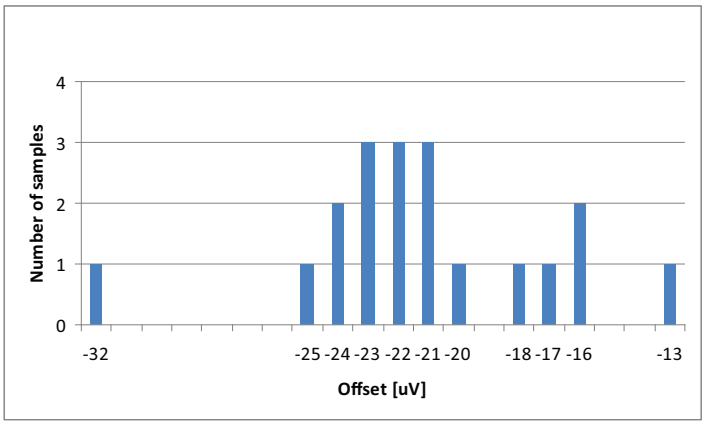
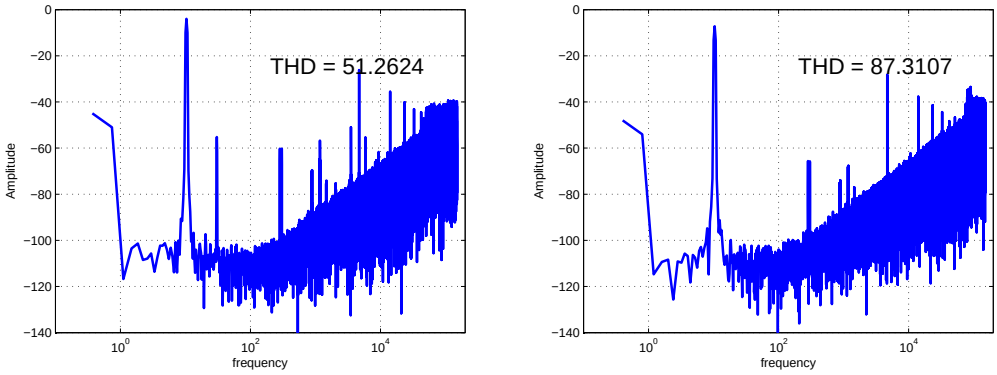


Figure 5.7: Offset distribution of the fabricated chips



(a) (b)

Figure 5.8: Output spectrum of the modulator (a) without filter capacitor and (b) with two 10nF capacitors

The input referred offset of all the samples is measured and its distribution is shown in Fig. 5.7. The mean value of the offset is $-21.15\mu V$ with a standard deviation of $\sigma = 6.79$.

The spectrum of the modulator without filter capacitor is shown in Fig. 5.8a. In this measurement the chopping frequency is at 4.69kHz, DEM for Gm-stages at 1.17kHz and DEM for IDACs at 300Hz.

By inserting the two 10nF capacitors of the filter, the harmonics are suppressed down to the noise floor. Only for high input amplitudes, when the modulator starts to become overloaded, do the harmonics rise above the noise floor. The spectrum of the modulator with 10nF capacitors is shown in Fig. 5.8b. Comparing to Fig. 5.8a the third harmonic is suppressed about 40dB.

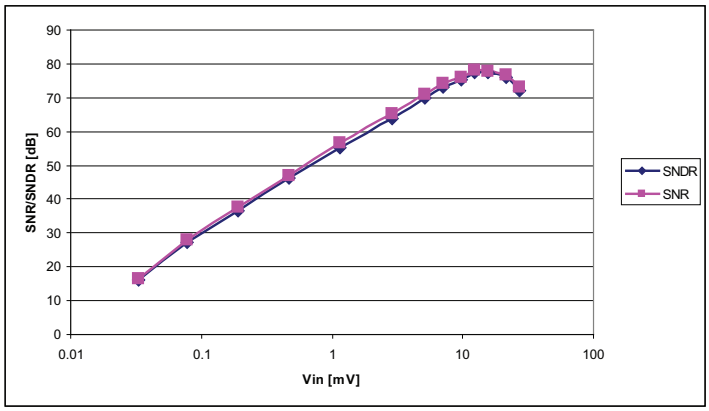


Figure 5.9: SNR and SNDR versus the input amplitude

In Fig. 5.9 it is shown that the SNDR is closely following the SNR. This means that the harmonics are smaller than the noise floor.

From the design steps and simulations it was expected to have a flicker noise corner frequency of less than 1Hz. In Fig. 5.10 the output spectrum for shorted input is shown. The flicker noise is not apparent in this resolution and due to memory problem of MATLAB, a higher resolution could not be achieved. However, the corner frequency for shorted input and AC signal is lower than $50mHz$. In case of a DC input signal the corner frequency of the flicker noise increases. The reason is that the IDACs are not chopped with the bit-stream completely since the number of ones and zeros are not equal anymore.

The chip photo is given in Fig. 5.11. The total area of the chip is $5.4mm^2$ In table 5.1 the performance of the modulator is given together with other works. The aim was to achieve the performance of [5] in an ADC. However there are two major mistakes limiting the performance. One is a systematic error which makes an offset about -21 μV at $f_s = 300kHz$ and also affects the linearity improvement at higher sampling frequencies. The other is the noise contribution of the IDACs. In the design steps, noise floor of less than $20nV/\sqrt{Hz}$ was the target for the whole system and the noise floor of the IDACs was expected to be about half of it. However, about 90% of their noise is coming from the biasing and it was not considered in the design.

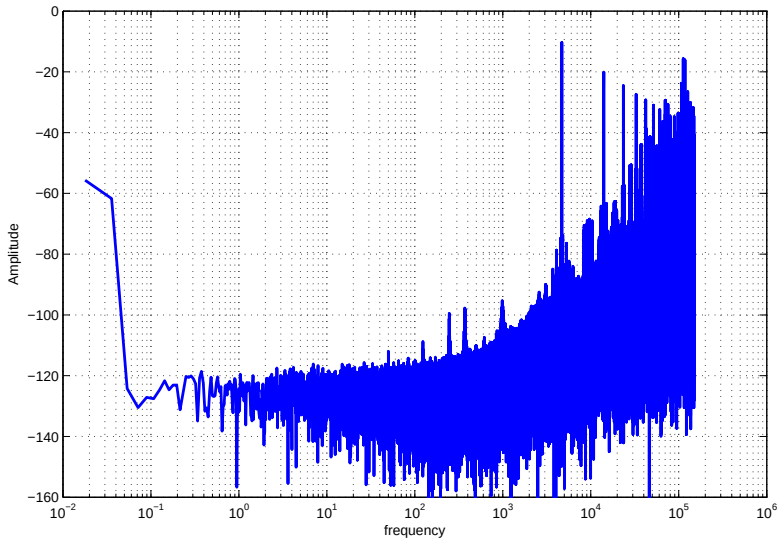


Figure 5.10: Output spectrum for shorted input

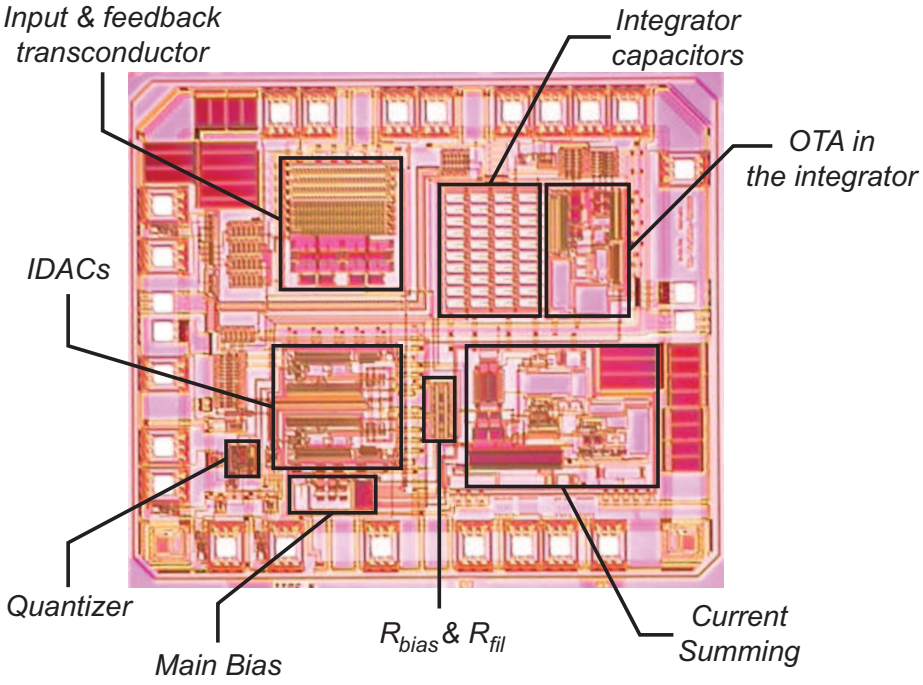


Figure 5.11: Micrograph of the CT ΣΔ modulator

Table 5.1: Table of performance

	This Work CT ΣΔ	[6] CT ΣΔ	[7] CT ΣΔ	[8] CT ΣΔ	[5] CFIA
noise floor / resolution	$90\frac{nV}{\sqrt{Hz}}$/13-bits	$<10\mu V_{pp}$	12-bits	11-bits	$15\frac{nV}{\sqrt{Hz}}$
input range	50mV	±1.2V	NA	400mV	50mV
offset	32μV	340μV	NA	NA	5μV
bandwidth	100Hz	500kHz	6.4MHz	2MHz	—
linearity (HD)	-92dB	< -70dB	< -70dB	< -86dB	NA
current consumption	400μA	2.54 mA	16.8 mA	6.1mA	230 μA
Supply voltage [V]	5	5	1.5	1.8	5
CMOS Technology	0.7 μm	0.5 μm	0.13 μm	0.18 μm	0.7 μm

Chapter 6

Conclusion

The output of sensor and actuator systems is often a weak differential signal and processing them requires amplifiers with high precision. Instrumentation amplifiers are used to amplify such sensitive signals and an ADC converts the output signal to a digital code for processing.

The current mode feedback instrumentation amplifier (CFIA) is one of the different architectures used for IA implementation. This structure has similarities to CT $\Sigma\Delta$ modulators with an input Gm-stage. They have OTA at the input and feedback and normally a miller compensated second stage. A resistor network in the feedback defines the closed-loop gain.

If the feedback path is substituted with a quantizer and DAC, the system can work as a $\Sigma\Delta$ modulator with active gm-C integrator. The issue of this modulator is that the nonlinearity of the input transconductance is not suppressed in the feedback if a single-bit quantization is used. This nonlinearity in the IA is compensated significantly if the input and feedback Gm-stages are identical and loop gain is high. In contrast, the feedback Gm-stage in a modulator with two level DAC acts as a linear stage since it works at only two points. Hence to generate the same nonlinearity in the feedback multi-level signal should be produced in the feedback. It can be done by multi-level quantization, but the complexity of the system increases with the number of levels.

In this thesis, a low-pass filter is used in the feedback to extract the signal from the bit-stream and locate it at the input of the feedback Gm-stage. Other feedback paths are provided to stabilize the system. With this method more than 35dB improvement in THD is achieved and SFDR equal to 92 dB is obtained.

The thermal noise of the IDACs dominates the noise floor and consequently the noise performance is worse than the desired specification. These stages are using the common biasing circuitry for all the system and more than 80% of the noise in the IDACs are coming from this biasing. A separate biasing for the IDACs can decrease the noise floor.

The offset is highly affected because of the CM settling problem. This error increases the input offset for higher sampling rates and to obtain the best offset, the sampling rate is decreased as much as possible. The mean value of the offset is $-21.15\mu V$ for 20 samples and the standard deviation is $\sigma = 6.79$. These specifications are achieved with a current consumption of about $400\mu A$ from a 5V power supply.

6.1 Future work

Suggestions for the future continue of this work are summarized as follow:

- Decreasing the power consumption can be done by modifying the blocks and/or changing the system. The current tail of the telescopic amplifier in the active integrator is high enough to be able to drive more than twice the IDAC current at the output. Hence this stage is consuming current twice more than what is needed. It was considered in the design steps to be able to use twice the current in the IDAC to increase the input range. However, increasing the current level increases the noise floor as well and there is no improvement in resolution. Also if higher current level is used, to prevent saturating the integrator the sampling frequency or the integrator's capacitor should be increased. In the measurements the low IDAC current level was used. However, using a two stage amplifier including a class AB output stage can decrease the power consumption by about $100\mu A$.

- If a different topology such as the diagram shown in Fig. 3.6 is used for this modulator, the feedback current steering DACs can be substituted with a voltage DAC and a transconductance to the output of the integrator. In this way the voltage DAC offer a better noise performance and the noise floor can be decreased.

- Using a multi-bit quantization can decrease f_{sc}, the sampling to LPF corner frequency ratio, offering two advantages; one is to decrease the sampling rate and the other is to increase the LPF corner frequency which results to higher bandwidth. Increasing the LPF corner

frequency by a factor of about 20 also makes the integration of the capacitor possible.

One issue with multi-bit quantization is the linearity of the feedback DAC. Using a $\Sigma\Delta$ DAC in the feedback can solve this concern but it requires another oversampling ratio for the sampling rate. Hence it is not applicable for high bandwidth applications.

Bibliography

[1] F. Witte, K. Makinwa, and J.H. Huijsing. *Dynamic Offset Compensated CMOS Amplifiers*. Springer Verlag, 2009. [cited at p. 1, 3]

[2] J.H. Huijsing. *Operational amplifiers: theory and design*. Springer Netherlands, 2001. [cited at p. 1]

[3] RC Yen and PR Gray. A MOS switched-capacitor instrumentation amplifier. *IEEE Journal of Solid-State Circuits,* VOL. 17, NO. 6, pp. 1008-1013, DEC 1982. [cited at p. 1]

[4] J.F. Witte, J.H. Huijsing, and K.A.A. Makinwa. A Current-Feedback Instrumentation Amplifier With 5μV Offset for Bidirectional High-Side Current-Sensing. *IEEE Journal of Solid-State Circuits*, VOL. 43, NO. 12, pp. 2769-2775, DEC 2008. [cited at p. 2]

[5] R. Wu, KAA Makinwa, and JH Huijsing. A chopper current-feedback instrumentation amplifier with a 1mHz $1/f$ noise corner and an AC-coupled ripple-reduction loop. In *IEEE International Solid-State Circuits Conference-Digest of Technical Papers, ISSCC 2009.*, pp. 322-323, FEB 2009. [cited at p. 3, 6, 71, 73]

[6] E.J. van der Zwan, RHM Van Veldhoven, P. Nuijten, E.C. Dijkmans, and SD Swift. A 13 mW 500 kHz data acquisition IC with 4.5 digit DC and 0.02% accurate true-RMS extraction. In *IEEE International Solid-State Circuits Conference, Digest of Technical Papers*, pp. 398-399, FEB 1999. [cited at p. 5, 6, 30, 73]

[7] E. Prefasi, L. Hernandez, S. Paton, A. Wiesbauer, R. Gaggl, and E. Pun. A 0.1 mm2, Wide Bandwidth Continuous-Time $\Sigma\Delta$ ADC Based on a Time Encoding Quantizer in 0.13 μm CMOS. *IEEE journal of solid-state circuits*, VOL. 44, NO. 10, pp. 2745-2754, OCT 2009. [cited at p. 6, 73]

[8] Y. Aiba, K. Tomioka, Y. Nakashima, K. Hamashita, and B.S. Song. A Fifth-Order Gm-C Continuous-Time $\Delta\Sigma$ Modulator With Process-Insensitive Input Linear Range. *IEEE journal of solid-state circuits*, VOL. 44, NO. 9, pp. 2381-2391, SEP 2009. [cited at p. 6, 30, 73]

[9] D.A. Johns and K. Martin. Analog integrated circuit design. *John Wiley & Sons*, 1997. [cited at p. 9, 14, 15]

[10] B. Razavi. *Principles of data conversion system design*. IEEE press New York, 1995. [cited at p. 11, 12]

[11] R. Schreier and G.C. Temes. *Understanding delta-sigma data converters*. IEEE press Piscataway, NJ, 2005. [cited at p. 19, 22, 23]

[12] W. Gao, O. Shoaei, and W.M. Snelgrove. Excess loop delay effects in continuous-time delta-sigma modulators and the compensation solution. In *IEEE International Symposium on Circuits and Systems*, pp. 65-68, AUG 1997. [cited at p. 24]

[13] A. Hairapetian and G.C. Temes. A dual-quantization multi-bit sigma delta analog/digital converter. In *ISCAS IEEE International Symposium on Circuits and Systems*, volume 5, pp. 437-440, 1994. [cited at p. 25]

[14] B.P. Brandt and B.A. Wooley. A 50-MHz multibit sigma-delta modulator for 12-b 2-MHz A/D conversion. *IEEE Journal of Solid-State Circuits*, VOL. 26, NO. 12, pp. 1746-1756, DEC 1991. [cited at p. 25]

[15] M. Sarhang-Nejad and GC Temes. A high-resolution multibit $\Sigma\Delta$ ADC with digital correction and relaxed amplifier requirements. *IEEE Journal of Solid-State Circuits*, VOL. 28, NO. 6, pp. 648-660, JUN 1993. [cited at p. 25]

[16] J. Silva, X. Wang, P. Kiss, U. Moon, and GC Temes. Digital techniques for improved $\Delta\Sigma$ data conversion. In *Proceedings of the IEEE Custom Integrated Circuits Conference*, pp. 183-190, 2002. [cited at p. 25]

[17] M.J. Story. Digital to analogue converter adapted to select input sources based on a preselected algorithm once per cycle of a sampling signal, AUG 1992. US Patent 5,138,317. [cited at p. 25]

[18] R.T. Baird and T.S. Fiez. Improved $\Delta\Sigma$ DAC linearity using data weighted averaging. In *IEEE International Symposium on Circuits and Systems, ISCAS*, volume 1, pp. 13-16, 1995. [cited at p. 25]

[19] C.C. Enz and G.C. Temes. Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization. *Proceedings of the IEEE*, VOL. 84, NO. 11, pp. 1583-1614, NOV 1996. [cited at p. 28]

[20] L. Breems and J.H. Huijsing. *Continuous-time sigma-delta modulation for A/D conversion in radio receivers*. Springer Netherlands, 2001. [cited at p. 29]

[21] B. Razavi. Design of analog CMOS integrated circuits. 2000. [cited at p. 31, 58]

[22] S.M. Kashmiri, S. Xia, and K.A.A. Makinwa. A temperature-to-digital converter based on an optimized electrothermal filter. *IEEE Journal of Solid-State Circuits*, VOL. 44, NO. 7, pp. 2026-2035, SEP 2009. [cited at p. 49]

[23] O. Feely and LO Chua. The effect of integrator leak in Σ-Δ modulation. *IEEE Transactions on Circuits and Systems*, VOL. 38, NO. 11, pp. 1293-1305, NOV 1991. [cited at p. 50]

[24] R. Wu, K.A.A. Makinwa, and J.H. Huijsing. A Chopper Current-Feedback Instrumentation Amplifier With a 1 mHz Noise Corner and an AC-Coupled Ripple Reduction Loop. *IEEE journal of solid-state circuits*, VOL. 44, NO. 12, pp. 3232-3243, DEC 2009. [cited at p. 55]

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