# A Back-Wafer Contacted Silicon-On-Glass Integrated Bipolar Process—Part I: The Conflict Electrical Versus Thermal Isolation

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Abstract—A novel silicon-on-glass integrated bipolar technology is presented. The transfer to glass is performed by gluing and subsequent removal of the bulk silicon to a buried oxide layer. Low-ohmic collector contacts are processed on the back-wafer by implantation and dopant activation by excimer laser annealing. The improved electrical isolation with reduced collector-base capacitance, collector resistance and substrate capacitance, also provide an extremely good thermal isolation. The devices are electrothermally characterized in relationship to different heat-spreader designs by electrical measurement and nematic liquid crystal imaging. Accurate values of the temperature at thermal breakdown and thermal resistance are extracted from current-controlled Gummel plot measurements.

Index Terms—Bipolar transistors, laser annealing, liquid crystal microscopy, radio frequency (RF) process integration, silicon-on-glass, silicon-on-insulator (SOI), thermal management, thermomapping.

# I. INTRODUCTION

N A QUEST for increased speed and performance, the silicon industry is not only investing in the downscaling of devices fabricated on the surface of bulk-silicon wafers, but is also looking for alternative substrates and ways of manipulating the substrate to achieve benefits such as enhanced integration of high-performance passive components, reduced crosstalk and three-dimensional device integration [1]-[6]. In many of these methods, such as processing on silicon-on-insulator (SOI) wafers and substrate transfer techniques, the direct contact between the active device silicon and that of the substrate is severed and replaced by electrically isolating dielectric layers. Compared to silicon, these layers have very poor thermal conductivity and the overall thermal resistance of the device increases significantly [7]-[11]. Today, in general, more and more compact device processing leads to an increase of the thermal resistance of the individual devices that is not compensated by a corresponding decrease in power dissipation. Hence,

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thermal management is becoming one of the major challenges facing future IC generations.

In this paper the electrothermal consequences of implementing a bulk-silicon bipolar NPN process in silicon-on-anything (SOA) [12], [13] substrate transfer technology are examined. Pure electrically the resulting process has many potential advantages for the integration of high-performance low-power radio frequency (RF) circuits. First, the lossy silicon substrate is replaced by a low-loss glass substrate. Second, the devices are fabricated in very small silicon islands where the emitter and base are contacted via the front-wafer while the collector is contacted directly under the emitter via the back-wafer. Thus, the need for a buried layer and collector plug is eliminated and the collector resistance becomes very low. Moreover, the substrate capacitance is eliminated and the collector-base capacitance is independent of the lateral extrinsic base dimensions. Both the front- and back-wafer are processed with the same high-precision lithography, and low-ohmic n- and p-type contacts are fabricated on both sides of the wafer by using high-power excimer laser annealing to activate the dopants after the wafer transfer to glass. All in all this gives a very high flexibility in the design of the devices and integrating other device types, such as high-frequency PNPs, becomes straightforward.

The electrothermal coupling in these devices is, however, forbiddingly strong. With thermal resistance values up to 100 times higher than that of corresponding bulk-silicon devices, self-heating effects and thermal runaway appear at power densities much lower than any ever witnessed before in silicon. In Part I of this paper on back-wafer contacted silicon-on-glass NPNs, the device processing and the correlation to the electrothermal device characteristics is described. In Part II [14] the experimental results are used to formulate and verify a new analytical model for the relationship between the device temperature at thermal runaway and the power dissipation. Along with providing a comprehensive view of the electrothermal behavior of the examined devices, this work also enables a clearer analysis of more conventional "low thermal resistance" devices.

#### II. DEVICE FABRICATION

# A. Process Flow

The basic process flow for the fabrication of a back-wafer contacted NPN is shown in Fig. 1, where the silicon-on-glass

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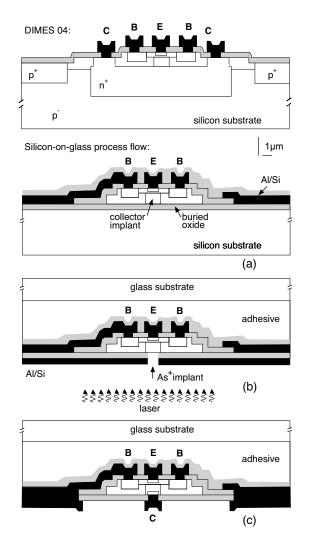


Fig. 1. Schematic cross section of a bulk DIMES-04 NPN and the process flow of the corresponding silicon-on-glass device.

structure is also compared to the corresponding bulk transistor, a 25-GHz DIMES-04 fully implanted NPN [15]. The conventional silicon wafers with buried n<sup>+</sup> layers and epi are replaced by SOI wafers with a  $0.84-\mu m$  n-doped silicon top layer. The pedestal collector region is implanted with phosphorus and extrinsic base regions are doped by a low-dose deep B<sup>+</sup> implant (to compensate the n-epi) and a high-dose shallow B<sup>+</sup> contact implant. The active device areas are isolated by means of trenches etched to the buried oxide. The emitter and base are processed and contacted following standard front-wafer processing procedures. After gluing the front-wafer onto glass, the silicon substrate is removed by TMAH etching selectively to the 0.4- $\mu$ m-thick buried oxide. The integrity of the glue restricts further back-wafer processing to temperatures below 300 °C. A technique has been developed for processing the back-wafer with the same lithography equipment (ASM PAS 5000) as the front-wafer [16]. Minimum-dimension (1  $\mu$ m in the present work) contact windows on the back-wafer can thus be aligned to front-wafer structures. The back-wafer contact processing starts with the deposition of a 0.3-\mu Al/Si reflective masking layer at room temperature onto the buried oxide. All contact windows are plasma etched to the silicon and

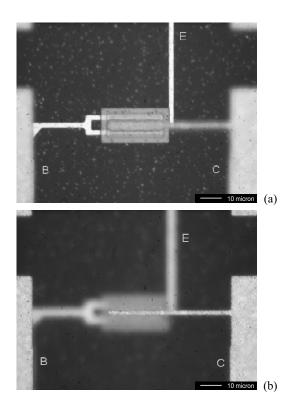


Fig. 2. Microscope images of the silicon-on-glass NPN  $(A_E=20\times 1~\mu\text{m}^2)$  bipolar transistor in a small  $(10\times 23~\mu\text{m}^2)$  silicon island. (a) The focus is on the emitter–base front-wafer metallization. (b) The focus is on the collector and bondpads back-wafer metallization.

implantations are performed with oversized resist mask. After laser annealing, a HF dip etch step is performed to remove the native oxide. In this step most of the Al/Si mask is also removed and the windows are contacted by sputtering a new layer of Al/Si(1%). The device processing is completed by opening contacts to the front-wafer metal, sputtering and patterning a final layer of  $0.8-\mu m$  Al/Si on the back-wafer.

A photo of an NPN bipolar transistor with an emitter area of  $20 \times 1~\mu\text{m}^2$ , placed in a small  $(10 \times 23~\mu\text{m}^2)$  silicon island, is shown in Fig. 2. This device has a base contact on each side of the emitter. Fig. 2(a) is focused on the front-wafer metal, i.e., the metal on the emitter side of the device, while Fig. 2(b) is focused on the back-wafer metal, i.e., the metal on the collector side of the device.

## B. Laser Annealing of Back-Wafer Contacts

The use of glue to adhere the silicon wafer to the glass wafer has the great advantage of not requiring a completely flat wafer surface. However, the low decomposition temperature of the glue, about  $300\,^{\circ}\text{C}$ , places severe limitations on the back-wafer processing temperatures. For the formation of low-ohmic contacts, two of the conventionally applied process steps are no longer permissible:

1) Thermal activation of implanted dopants, a process that requires at least 600 °C. Excimer laser annealing of implanted dopants has previously been shown to be an alternative for dopant activation by melting the contact surface without heating the bulk [17].

2) Alloying of the metallized contacts to dissolve the native oxide, which is normally performed around 400–450 °C. In the processing of the front-wafer contacts here, a 400 °C anneal is performed to avoid the precipitation of silicon from the Al/Si(1%) alloy to the silicon surface. Normally a 400 °C 30 min alloying in forming gas completes the processing. This step serves both to dissolve any native oxide formed between dip etching and metallization, and to improve the oxide passivation. In the bipolar device fabrication, all junction terminations on the oxide are alloyed at 400 °C after front-wafer metallization and for passivation purposes it is not required to repeat this step after back-wafer processing.

For the back-wafer contacts, the relation between the laser anneal energy and the alloying conditions was studied with respect to the resulting contact resistance for both boron- and arsenic-implanted contacts. In [13], 15 keV implants were studied and it was found that for a high enough laser anneal energy the minimum contact resistivity could be obtained without alloying. For the present work 5 keV implants to a dose of  $2 \times 10^{15}$  cm<sup>-2</sup> for both As<sup>+</sup>- and B<sup>+</sup>-doped contacts have been implemented. They are laser annealed with an energy of  $900 \,\mathrm{mJ/cm}^2$  using an XMR5121 XeCl excimer laser ( $\lambda = 308 \text{ nm}$ ) system. The full width at half-maximum is 60 ns and the repetition frequency is 5 Hz. The spot size is  $10 \times 3 \text{ mm}^2$  and the annealing process has been performed in a vacuum chamber at a pressure below  $10^{-7}$ Torr and at room temperature. The laser beam scans with 66% overlap in the lateral direction, so there are three shots at the same position. This is essentially a single-shot anneal since the laser energy is so high that the contact surface is melted and the surface changes from amorphous to crystalline during the resolidification of the melt-zone. The melting temperature of a-Si is much lower than that of c-Si so the subsequent two pulses are not decisive for the result.

The laser energy needed to melt the silicon surface depends on how well the generated heat can flow away from the contact window. This in turn depends on the size of the contact itself and the size of the silicon island. For decreasing contact size the laser energy must be increased to compensate for the better heat spreading to the surroundings. For decreasing silicon island size the thermal isolation is improving and lower laser energy is required. The laser energy of 900 mJ/cm<sup>2</sup> is chosen such that the minimum contact resistivity is achieved in all the present structures, i.e., for contacts down to  $2 \times 1 \mu m^2$  and silicon islands down to  $8\times3\times0.84 \ \mu\text{m}^3$ . This energy is thus excessive for large contacts in small islands, but not enough to destroy or ablate the silicon surface. The rather large thickness of the silicon layer, in which the devices are made, is here of advantage. With respect to laser annealing, a 1- $\mu$ m thick silicon layer on a glass substrate will behave approximately as bulk silicon. For layer thicknesses below 0.4  $\mu$ m the energy necessary for melting the silicon becomes very thickness sensitive. Thus, for silicon islands much smaller than the ones processed here, finding a usable laser processing window will become much more critical.

A contact resistivity of  $1.5 \times 10^{-7} \ \Omega \text{cm}^2$  was achieved for the  $\text{As}^+$ -implanted contacts and  $5 \times 10^{-7} \ \Omega \text{cm}^2$  for  $\text{B}^+$ -implanted contacts (the latter are used as collector contacts in vertical PNPs). This paper focuses only on the behavior of the NPNs.

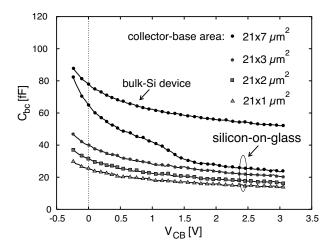


Fig. 3. Collector–base capacitance for devices with  $20 \times 1 - \mu m^2$  emitter area and various collector designs. The two devices with c-b area of  $21 \times 7 \mu m^2$  have a lightly doped n-epi around the collector implant. For all other devices the collector implant area determines the size of the c-b region.

The collector-contact implant is placed entirely within the pedestal collector region, which is doped to about  $10^{17}~\rm cm^{-3}$ . This ensures that the collector-base depletion region does not terminate in the laser annealed  $\rm n^+$  region, and no collector-base leakage related to the presence of the back-wafer contact has been observed. In this work no attempt is made to optimize the laser recrystallization process to minimize the residual damage, but ongoing research is devoted to fabricating ideal  $\rm n^+$ -p and  $\rm p^+$ -n diodes with laser annealing.

# C. Basic DC Device Parameters

The NPNs are fabricated in 1- $\mu$ m lithography and the lateral dimensions are determined by a 3- $\mu$ m metal pitch. Thus, for a  $20 \times 1 - \mu m^2$  emitter area, the total base area is  $21 \times 7 \ \mu m^2$ . In Fig. 3 the collector–base capacitance  $C_{bc}$  has been measured for different collector designs. For devices that are p-doped under the extrinsic base implant, the  $C_{bc}$  decreases with the size of the collector implant region as would be expected. For devices with n-epi under the extrinsic base, the low-voltage values of  $C_{bc}$  are high, but when the n-epi is entirely depleted the  $C_{bc}$  drops significantly. In all cases the  $C_{bc}$  is much lower than that of the corresponding bulk-Si device where the n<sup>+</sup> buried layer dominates.

In Table I, the main dc device parameters of the bulk and silicon-on-glass device are compared. Electrically the main advantages of glass processing for NPNs lie in a large reduction of the collector resistance and the collector–base capacitance. This has clear advantages for the  $f_{max}$  of the devices. The bulk NPN has an  $f_T$  and  $f_{max}$  of 25 GHz ( $V_{\rm CB}=3$  V). The exact design of the collector–base region in the silicon-on-glass devices will also influence the  $f_T$ . However, characterization and optimization of the devices with respect to the high-frequency parameters has been impeded by the strong electrothermal coupling at high currents. The device design in relationship to the electrothermal behavior is the focus of the rest of this paper. Understanding and controlling self-heating effects will be decisive for the viability of integrated silicon-on-glass circuits.

NPN processed in	bulk Si	silicon-on-glass		
Device area[ $\mu$ m <sup>2</sup> ]	21x35	8x21		
Emitter area $[\mu m^2]$	20x1	20x1		
$h_{FE} (V_{BE} = 0.8 \text{ V})$	100	100		
$V_A$ [V]	12	12		
$r_e [\Omega]$	3	3		
$r_b [\Omega]$	60	60		
$r_c [\Omega]$	20	3		
$BV_{CEO}[V]$	5	5		
$C_{bc}(V_{CB} = 0 \text{ V}) \text{ [fF]}$	75 30			
$C_{eb}(V_{CB}=0 \text{ V}) \text{ [fF]}$	88	88		
$R_{TH}$ [K/W]	~ 300	~ 10500		

## TABLE I DEVICE PARAMETERS

#### III. ELECTROTHERMAL CHARACTERIZATION

## A. Electrical Measurement of Self-Heating

Self-heating during electrical measurement of silicon-onglass NPNs is readily observed. Two factors are essentially responsible for the high thermal resistance:

- Silicon islands in which devices are formed are small and almost completely surrounded by oxide and glass, which are poor thermal conductors. Silicon itself has a good thermal conductivity. Therefore, normally low-power transistors in bulk silicon are not seriously affected by the heat they dissipate themselves.
- 2) Devices are composed of thin layers of various materials such as silicon, silicon dioxide and nitride. The thermal conductivity of a thin film is lower than that of the corresponding bulk material due to phonon scattering on imperfections and phonon boundary scattering [18].

All electrical measurements were performed with a HP4156B parameter analyzer and a Cascade probe station equipped with a thermal chuck. Typical transistor characteristics are shown in Fig. 4, where the characteristics of a bulk-silicon device are compared to the corresponding minimum dimension silicon-on-glass device. During these measurements the thermal chuck temperature was kept constant at 27 °C. In general, in silicon devices both the base and collector current increase with temperature and the current gain also increases due to bandgap narrowing in the highly-doped emitter. In both the Gummel plots and output characteristics shown in Fig. 4(a) and (4b) an excessive increase in collector current is observed in the silicon-on-glass device as compared to the bulk device. In the Gummel plot for  $V_{\rm CB}=0$  V, thermal runaway with catastrophic increase of both the collector and base current is observed at the low  $V_{BE} \approx 0.8 \text{ V}$  corresponding to a power of only  $\approx$ 2 mW. In the output characteristics both self-heating and avalanching increase the collector current. By looking at the  $I_B - V_{CB}$  characteristics of the silicon-on-glass device shown in Fig. 4(c), the breakdown voltage  $BV_{CEO}$  associated with

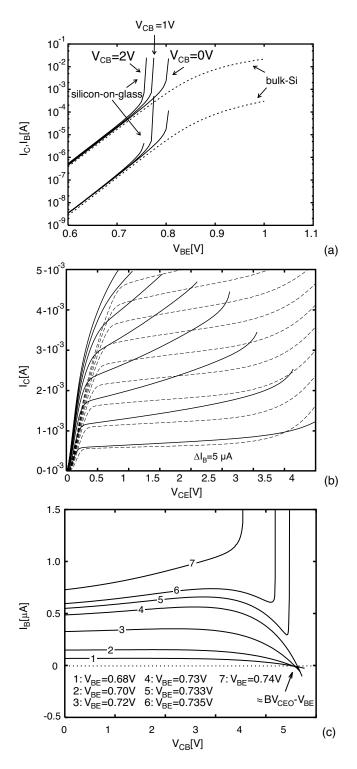


Fig. 4. (a) Gummel plots. (b) Output characteristics. (c)  $I_B-V_{\rm CB}$  characteristics of a bulk-Si (dashed lines) and silicon-on-glass device (solid lines). Emitter area is  $A_E=20\times 1~\mu{\rm m}^2$ .

avalanching can be determined from the  $I_B=0$  intersection point for low  $V_{BE}$  values. For  $V_{BE}$  values around 0.72 V, self-heating is already producing a noticeable increase in  $I_B$  and for  $V_{BE}\approx 0.733$  V the  $I_B$  no longer decreases to zero.

Although the self-heating effects and thermal runaway are clearly detected in the above measurements, these do not provide a good technique for quantifying the conditions at

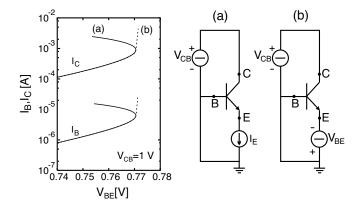


Fig. 5. Measurement circuits and Gummel plot measurements. (a) Emitter current-controlled method (solid line). (b) Base-emitter voltage-controlled method (dashed line). Emitter area is  $A_E=20\times 1~\mu\mathrm{m}^2$ .

thermal runaway. On the other hand, in current-controlled  $I_C - V_{BE}$  characteristics the thermal breakdown is detected as the snapback, or turnover, or flyback point [19]-[21]. This point is seen in Fig. 5 where the biasing circuits for both the base-emitter voltage- and emitter current-controlled measurements in common-base configuration are given together with the corresponding  $I_C - V_{BE}$  measured characteristics. In the current-controlled measurement the self-heating lowers the  $V_{BE}$  corresponding to a given collector current and above the critical temperature a negative differential resistance is observed. In Part II of this paper the flyback point is examined theoretically and it is shown that the critical power  $P_{crit}$  determined from the biasing conditions at this point can be used to calculate both the critical temperature rise  $\Delta T_{crit}$  necessary for thermal runaway and the thermal resistance  $R_{\mathrm{TH}}$  of the device. Applying the derived expressions to the device measured in Fig. 5 yields  $\Delta T_{crit} = 19.0$  K and  $R_{\rm TH} = 10440$  K/W. In Fig. 6(a) the current at the flyback point is seen to decrease as the collector-base voltage increases.

The emitter and collector series resistances are both very low in the silicon-on-glass transistor characterized in Figs. 4 and 5. This fact, and not only the high thermal resistance, is important for the clarity with which the flyback point is detected in the current-controlled Gummel plots. Ballasting resistors have a stabilizing effect on the electrothermal behavior as seen in the example in Fig. 6(b) where the effect of a  $20-\Omega$  series resistance added to either the emitter or collector terminal is shown. The collector resistance only causes a very small increase of the position of the flyback point but does, for high enough currents, deter the negative differential behavior in the current-controlled Gummel plot and correspondingly the uncontrolled current rise in the voltage-controlled measurement is tempered. Emitter ballasting eliminates the flyback point and is thus very effective in preventing thermal runaway. However, for RF applications such resistors reduce device transconductance,  $f_T$ ,  $f_{max}$ , and increase input and output resistances [22]. The choice of ballasting resistors is therefore not trivial and implies device performance trade-offs. The analytical formulation of the thermal breakdown condition given in Part II of this paper provides a handsome tool for evaluating the way in which series resistances influence the electrothermal characteristics.

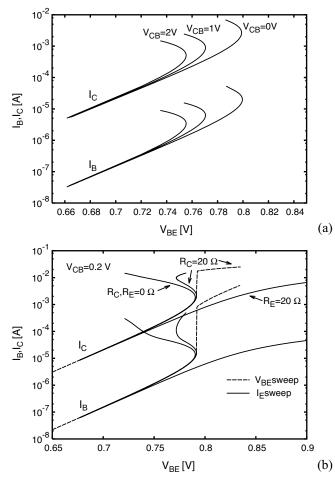


Fig. 6. (a) Current-controlled Gummel plots measured without ballasting resistors for several  $V_{\rm CB}$  values. (b) Voltage- and current-controlled Gummel plots measured with and without a 20- $\Omega$  emitter-ballasting or collector resistor. Emitter area is  $A_E=20\times 1~\mu{\rm m}2$ .

# B. The Effect of Device Surroundings on Heat Spreading

To electrothermally stabilize the silicon-on-glass NPNs the thermal resistance of the devices must be significantly reduced. In previously reported large discrete silicon-on-glass NPNs [23], [24] this has been achieved on the packaging level by placing a large metallic heat sink directly on the collector contact. For the present low-power devices, such an approach would be in conflict with the aim for low collector-base capacitance and negligible substrate capacitance in a circuit situation. Methods of spreading the heat away from the active device region to a convenient place for heat sinking are therefore preferable. Electrical interconnect metal such as that shown in Fig. 2, is not effective in doing this because the 2- $\mu$ m-narrow metal tracks have a thermal resistance of approximately 2000 K/W per micron length. Other options for achieving more effective on-chip heat spreading within the present two metal processing scheme are examined in the following.

A series of devices were designed with different surroundings as shown schematically in Fig. 7. While the basic device (a) is surrounded completely by trenches filled with thermally isolating materials, the devices (b), (c), and (g) have neighboring silicon regions, and devices (d), (e), and (f) have neighboring metal regions. From the corresponding current-controlled Gummel plots, the junction temperature rise at the thermal

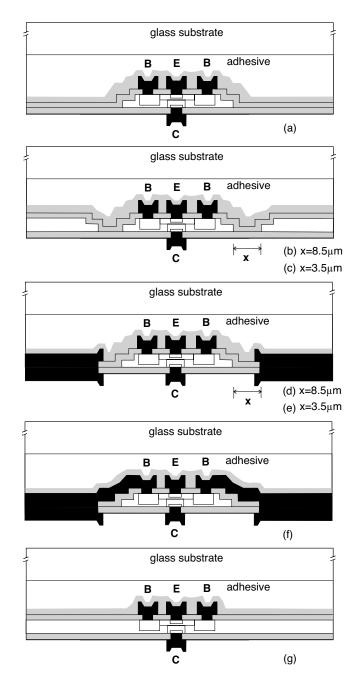


Fig. 7. Schematic of devices with different surroundings.

breakdown point and thermal resistance are calculated for each device, and the results are presented in Table II. Device (g) without trench isolation is the most effectively cooled by the direct contact to surrounding silicon. Insertion of trench isolation increases the thermal resistance even if the trench sidewalls are covered with metal as in device (f). Nevertheless, partial substitution of poor thermally conducting material in the close proximity of the active device with silicon or aluminum has a beneficial effect on  $R_{\rm TH}$ . For devices (b) to (e) the distance x to either a neighboring silicon or metal heat spreader  $(30\times80~\mu{\rm m}^2)$  is varied from 3.5  $\mu{\rm m}$  to 8.5  $\mu{\rm m}$ . The efficiency of a heat spreader decreases with increasing distance x. It is noteworthy that although aluminum has twice the thermal conductivity of bulk silicon, replacing silicon with aluminum [compare (b) and (d), (c) and (e)] is advantageous only when

TABLE II
EXTRACTED PARAMETERS FOR THE DEVICES SURROUNDED BY
DIFFERENT HEAT SPREADERS

Device	P <sub>crit</sub>	$\Delta  ext{T}_{crit}$	$R_{TH}$
	[mW]	[K]	[K/W]
(a)	1.82	19.00	10440
(b)	1.93	19.15	9920
(c)	2.09	19.37	9270
(d)	1.93	19.15	9920
(e)	2.12	19.41	9150
(f)	3.97	21.72	5470
(g)	6.73	24.85	3690

the heat spreader is close enough to the active device region. Although the reduction of  $R_{\rm TH}$  is not significant (a mere 12% difference between devices (a) and (e)), it has been achieved solely with the very limited quantity of material available in the standard two metal process. The more effective methods of (f) and (g) where large areas of thermally conducting material are added directly to the base contact are seen to give an  $R_{\rm TH}$  lowering of about 50 and 65%, respectively. These methods do not increase the collector—base capacitance, but introducing large electrically conducting regions to the device terminals may affect RF device and circuit performance.

The heat spreading in such silicon-on-glass NPNs has been visualized by using nematic liquid crystal (NLC) temperature mapping [25], [26] whereby the self-heating process during device operation can be monitored. With this method a map of the temperature rise all over the device and its surroundings can be generated. An NLC material with a clearing point  $T_C = 56.5$  °C is used. To facilitate the measurements the wafer is placed on a thermal chuck, the device under test is covered with a thin layer of NLC and subsequently biased. Areas with a temperature above the clearing point appear as dark regions when viewed under a microscope using crossed polarizer and analyzer. The method has an excellent 0.1 °C absolute temperature accuracy and a spatial resolution of about 1  $\mu$ m. Devices with three base and two emitter contacts, with an emitter area of  $2\times(20\times1~\mu\text{m}^2)$ in a  $0.84 \times 18 \times 25 - \mu \text{m}^3$  silicon island, were examined. An example of the results is given in Fig. 8. The device in Fig. 8(a1) corresponds to one represented in Fig. 7(a), while device 8(b1) corresponds to the one in Fig. 7(f). To obtain the images of Fig. 8(a2), (a3), (b2), and (b3) the hot chuck temperature is set at 46 °C. This implies that  $\Delta T = 10.5$  °C isothermal curves are detected as the boarders of dark "hot" areas as shown in Fig. 8(a2) and (b2). The device is biased in a common-base configuration where only emitter  $E_2$  is contacted. The input power is varied in steps and each corresponding isothermal curve is mapped in Fig. 8(a3) and (b3). The curves are slightly asymmetric because only the lower emitter finger is biased. Moreover, the probe needles contacting the bondpads E2, B, and C act as heat sinks and contribute to this asymmetry. This experiment clearly shows the effectiveness of on-wafer heat spreaders and demonstrates the utilization of NLC temperature mapping for studying heat spreading in micron-scale semiconductor devices.

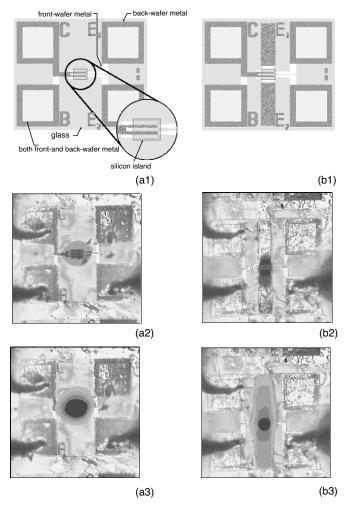


Fig. 8. Nematic liquid crystal images of a  $2\times(20\times1-\mu\mathrm{m}^2)$  emitter device n a  $18\times25-\mu\mathrm{m}^2$  silicon island, with and without large aluminum heat spreaders connected to the base as shown schematically in (b1) and (a1), respectively. The hot-chuck temperature is 46 °C and clearing point is 56.5 °C. (a2) and (b2) show dark area for P=2.2 mW. (a3) and (b3) show isothermal lines for power levels P=[1.75,2.2,2.65,3.5] mW.

In an integrated-circuit environment the individual device will be surrounded by other devices and metal tracks in varying patterns. The influence of such changes in the surroundings has been studied by considering chains of seven devices. The design of the middle device with the two neighboring devices is shown schematically in Fig. 9 for three different isolation schemes. Each set of seven devices is placed in a trenched island while the region between the individual devices is: 9(a) trench isolated, 9(b) filled with silicon and 9(c) filled with aluminum. In the corresponding current-controlled Gummel plots the flyback point is sensitive to the position of the device as well as to the isolation scheme. In Fig. 10, the flyback point of each middle device is compared to that of the device 7(g). Although the silicon island of 9(b) is quite large, the thermal resistance is higher than that of 7(g), which has no trenching at all. In 9(c) the silicon between the devices is replaced by a smaller amount of aluminum. This configuration does, however, have a slightly lower thermal resistance, showing again the large benefits of materials with high thermal conductivity.

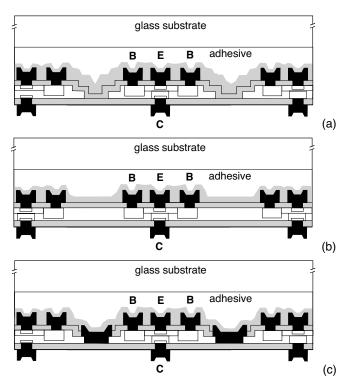


Fig. 9. Schematic of the middle device and the two neighboring devices in a chain of seven devices, for three different isolation schemes.

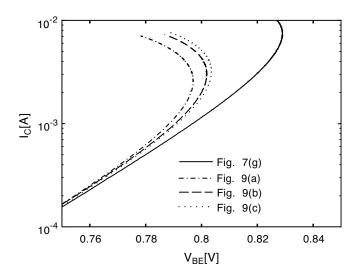


Fig. 10. Emitter-current controlled  $I_C-V_{BE}$  measurement of the middle device in device chains 9(a)–9(c). Emitter area is  $A_E=20\times 1~\mu{\rm m}^2$ .

## IV. CONCLUSIONS

Low-power, back-wafer contacted silicon-on-glass NPNs have been fabricated and characterized. Electrically, these devices exhibit the same quality as the corresponding bulk devices and their performance is enhanced by a reduction of the resistive and capacitive parasitics. In this work, the processing of the devices ends with the back-wafer aluminum interconnect layer. Aside from the first and second metallization and the thin layer of silicon, in which the active device is fabricated, the transistors are surrounded by dielectric layers with very low thermal conductivity. Thus, the resulting thermal resistance is so high that the thermal breakdown point moves to very low power levels and it is readily detected as a flyback

point in the current-controlled Gummel plot. By inserting this critical power in the analytical formulation developed in Part II of this paper, very accurate value for the thermal resistance could be determined. Different device isolation and metallization schemes were designed and even the slightest modifications, such as varying the distance to the adjacent device, could be accurately discerned and translated into the thermal resistance values. The benefits of replacing silicon with a material that has higher thermal conductivity, in this case aluminum, were apparent. However, the results show that sufficient heat spreading can only be achieved by directly contacting the active device silicon to large areas of material with high thermal conductivity. The thermal resistance of the conventional narrow metal tracks is too high and is unlikely that connecting these tracks to a heat sink outside the main circuit area will be enough to thermally stabilize even a low-current circuit. If the electrical isolation is not to be deteriorated, dielectric layers with high thermal conductivity are imperative for heat spreading. Further work in this direction is now in progress. Since such layers can be placed very close to the active device area, the heat spreading/sinking may overcome the efficiency presently achievable in bulk-silicon processes. For high-frequency performance such schemes are required for reducing the thermal resistance to values that allow the high-current device operation. Besides high-frequency circuit applications, the silicon-on-glass transistors also have great potential as high-precision thermal sensors.

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