Structured Electronic Design of High-Pass ΔΣ Converters

And their application to cardiac signal acquisition

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Challenge the future

Structured Electronic Design of High-Pass ΔΣ Converters

And their application to cardiac signal acquisition

A thesis submitted in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

in

ELECTRICAL ENGINEERING

by

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born in Cuttack, India

in
Section Bioelectronics
Department of Microelectronics
Delft University of Technology

October 25, 2016

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Abstract

Motivation: With the bandwidth of the ECG signal extending from sub-Hz to 200 Hz, a major challenge for an ECG readout system lies in implementing the high-pass (HP) cut-off frequency as this translates into the realization of large time constants on-chip.Although techniques such as those based on the use of pseudo-resistors to obtain very large time constants exist, they are heavily limited in both linearity and accuracy, which clearly dictates the need for alternative structures.

Proposed methodology: A structured electronic design approach based on state-space forms is proposed to develop HP $\Delta\Sigma$ converters targeting high accuracy of the HP cut-off frequency. Based on transfer function calculations, the various specific HP $\Delta\Sigma$ topologies namely, biquad, observable and controllable canonical and orthonormal HP $\Delta\Sigma$, can be made to satisfy the desired HP signal transfer with 2^{nd} order noise-shaping. In order to establish the noise contributions of the integrators, intermediate transfer functions, viz., from the system input to the integrator outputs, and from the integrator inputs to the system output, respectively are mathematically derived and evaluated.

Results: The evaluation of the intermediate transfer functions show that the orthonormal topology is better than the observable canonical HP $\Delta\Sigma$ topology in terms of noise. Simulations conducted in MATLAB confirm the noise behaviour of the integrators and show that, apart from the first integrator, the HP integrator significantly contributes to the total noise. Secondly, the noise and the harmonics at higher frequencies from the HP integrator are low-pass filtered. A 2^{nd} order orthonormal HP $\Delta\Sigma$ modulator with a sampling frequency of 128 kHz for a bandwidth of 1-200 Hz to be implemented in 0.18 μm technology achieves a resolution of 12-bits at the HP cut-off frequency of 1 Hz which is a major improvement over pseudo-resistors at the cost of higher area and power consumption. A robust, area-efficient and parasitic insensitive large time constant switched-capacitor Nagaraj integrator leads to a HP cut-off frequency realization determined solely by the ratio of capacitors with an accuracy upto 1%.

In conclusion, HP $\Delta\Sigma$ topologies that can be used to realize very large time constants with high linearity and accuracy which shows a major improvement over the conventionally used topologies that employ pseudo-resistors, are proposed

Keywords: ECG, State-space forms, High-Pass $\Delta\Sigma$ converters, orthonormal topology

Section Bioelectronics
TU Delft

कर्मण्येवाधिकारस्ते मा फलेषु कदाचन ।
मा कर्मफलहेतुर्भुर्मा ते सङ्गोऽसत्वकर्मणि ॥२-४७॥

karmaṇy evādhikāraste mā phaleṣu kadācana
mā karma phala hetur bhur mā te sangostva akarmaṇi

॥२-४७॥
Bhagavad-Gītā

You have the right to perform your actions,
but you are not entitled to the fruits of the actions.
Do not let the fruit be the purpose of your actions,
and therefore you won't be attached
to not doing your duty.

To my parents and grandparents

Preface

I would like to express special appreciation for my advisor Wouter Serdijn for the wonderful and exciting discussions that formed a strong base for my master thesis. A great degree of autonomy and confidence he places makes the student strive for excellence. I also thank Reza Lotfi for the discussions that made my thesis stronger. I thank Chris Verhoeven for being a part of my thesis committee. I thank Applied Biomedical Systems BV, specifically Richard, Jolanda and Leon for the meetings in the beginning. I would also like to thank Marion, Ali and Antoon for their support. I had a wonderful time being a part of the BELCA band and the music festival, canoeing in Delft canal and Christmas lunch gathering among other activities with the members of 18^{th} floor.

Ernesto, Saeed, Machiej and others made working in the MSc students lab a wonderful learning place. I am thankful to Vikram, Senad, Satoshi, Venkat, Gustavo and Earl McCune for the interactions and comments on parts of my report. A special thanks goes to Rachit for insightful discussions in times when I faced many difficulties in the project. I particularly enjoyed meeting him in Leuven @ Kofi Onan over a cup of coffee. I thank Joseph for his encouragement and support. Outside of graduate studies, I had a great opportunity to truly test my ability to swim in open-water along with Przemek and Koen from 9^{th} floor, when we formed *Team Tritons* to participate in the IRONMAN 70.3 triathlon in 2015 and 2016. While I always looked forward to the exciting event day, the disciplined training in both swimming and running helped me develop immense motivation and endurance to brave difficult times. Finally, I would like to thank my *Mama* for her continuous support and patience, my *Baba* for his encouragement for adventure and my brother for being there for me.

I would like to acknowledge the scholarship I received from the Faculty of Microelectronics during my master program. Also, I thank Wouter Serdijn for the generous funding support from the Biomedical Electronics Foundation to carry out this thesis project.

Samprajani Rout
Delft, The Netherlands
October 25, 2016

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Notations

a	Single element
$\mathbf{a}$	Vector
$\mathbf{A}$	Matrix
$\mathbf{a}^{\mathbf{T}}$	Transpose of a
$\|a\|_p$	p-norm of a
$\mathbf{A}^{-1}$	Inverse of matrix A
$\triangleq$	is defined as

1

Introduction

The human body generates electrical signals which carry vital information about the normal functioning of the body. These electrical signals can be recorded by means of external recording devices for diagnosis of specific diseases. The body signals can also be altered by the use of stimulation devices, also known as electroceuticals [1],[2] as an alternate form of treatment to pharmaceutical drugs for treating life threatening diseases that may or may not have any other form of treatment available. In this thesis, the focus will be on recording the electrical signals generated by the heart to diagnose cardiac arrhythmias.

1.1. Cardiac signal recording

Electrocardiogram (ECG) refers to the recording of the cardiac signal generated by the heart. As a diagnostic monitoring method for cardiovascular diseases, electrocardiography is used to record the ECG signal which carry specific physiological information about the working of the heart. The cardiac muscles undergo sequential activation leading to the generation of a normal ECG. The waveform of the ECG can be analyzed for diagnosis of cardiac arrhythmias. Although the first traces of electric heart activity was measured by Waller in 1899, it was Willem Einthoven who developed the first ECG recorder for clinical use and was awarded the Nobel Prize in 1924 for his research on ECG signals [3]. A complete ECG can be recorded by placing a set of electrodes (between 2 and 12) near the heart on the surface of the human body [4].

Conventional ECG recorders that are available in the hospitals are expensive and bulky. To meet the growing demand of the geriatric population, there is a need for light, inexpensive and portable patch devices that enable continuous and reliable ECG monitoring. The diagnosis of the specific cardiac arrhythmia of a patient through conventional ECG monitoring is very unlikely if the abnormality in the functioning of the heart manifests itself as an aperiodic event over a period of days or weeks. Therefore, there is a need for continuous long term monitoring of the cardiac signals before a diagnosis can be made. In this thesis, a 3-electrode, 2-channel ECG patch device for monitoring using wet gel (Ag/AgCl) electrodes will be designed for ECG recording aiding in the diagnosis of Atrial Fibrillation (A-Fib). The use of three electrodes ensures more reliable recording as compared to just two electrodes, of the information contained in the ECG signal. The use of gel based electrodes ensures continuity of the conduction path and leads to a cleaner waveform. Although dry electrodes can also be used, the recorded signals tend to be more noisy owing to the electrode tissue interface interactions.

As per the standards laid out by the International Electrotechnical Commission (IEC), the standard clinical ECG signal bandwidth extends from 0.05 mHz to 200 Hz [5]. Depending on the application of the ECG device, the signal frequency range would be a subset of $\{0.05\text{mHz} - 200\text{Hz}\}$. For the diagnosis of atrial fibrillation, a signal bandwidth of 0.5 - 200 Hz is sufficient to detect the irregularities in the R-R interval. In this project, a structured approach is taken for the implementation of the high-pass filter cut-off frequency targeting high linearity and accuracy. Therefore, special consideration is given

towards developing the high-pass filter and its strategic placement in the overall system for optimum performance.

1.2. RESEARCH OBJECTIVE

A complete front end for recording the ECG signal includes amplification, filtering and digitization that can be partitioned in several ways before the signal can be digitally processed. While the signal transfer function (STF) of a conventional ΔΣ ADC, an analog-to-digital converter, is low-pass, this thesis assumes a general filter transfer for the STF. It is of great interest to explore the high-pass (HP) ΔΣ topologies with an aim to implement the high pass cut off with good accuracy and linearity. To obtain very large time constants, one of the techniques is realization of pseudo-resistors by biasing transistors in the linear region [6], [7] to obtain very large resistances in the order of MΩs to TΩs. Although it is area efficient as compared to fabrication of resistance in polysilicon, it is heavily limited by both accuracy and linearity. Pseudo-resistors are also not very robust to PVT variations and are limited to 5-6 bits in linearity [8]. This would lead to inaccurate realization of the high-pass cut-off frequency and limit the achievable linearity. Other techniques based on switched- capacitors wherein the high-pass cut-off frequency depends on the ratio of capacitors is a preferable technique when higher linearity is desired. While targeting accurate and high linearity techniques for the implementation of the high-pass cut-off frequency, in this thesis, alternative structures using ΔΣ modulator that incorporates the HP filter is explored. This thesis focuses on developing topologies using standard state-space forms to arrive at HP ΔΣ topologies that meet the signal and noise transfer requirements. The objectives of the thesis are the following:

- To develop a structured methodology for proposing HP ΔΣ structures using state-space forms
- To compare the proposed HP ΔΣ ADC structures in terms of their noise contributions
- To analyze the high-pass integrator and its impact in terms of noise contribution and the effect of integrator non idealities on the performance of the ADC
- Build a circuit level schematic of the HP ΔΣ ADC to functionally verify the method proposed

1.3. THESIS ORGANIZATION

The remainder of the thesis is organized as follows. In Chapter 2, the structure of the heart is briefly explained followed by the origin and generation of the ECG. The cardiac arrhythmias and the specifications and standards for development of the devices are also explained. In Chapter 3, a design methodology for state-space based HP ΔΣ ADCs is proposed and mathematically verified at the system level. In Chapter 4, the proposed structures are evaluated in terms of their total noise contributions. In Chapter 5, the design choices and the impact of circuit non-idealities on the performance of the HP ΔΣ modulator is investigated. In Chapter 6, the circuit level implementation is described and the simulation results are summarized. In Chapter 7, the conclusions and future work are described.

2

THE HEART, ECG SIGNAL AND DEVICE CHARACTERISTICS

In this chapter, the background involving functioning of the heart, origin of the ECG, cardiac arrhythmias and the standards and specifications for designing an ECG recording device will be discussed. In Section 2.1, the structure and the working of the heart are described. Section 2.2 describes the electrical activation of cells, the origin of the ECG signals and its electrical characteristics followed by the characteristics of ECG in Section 2.3. In Section 2.4, the various cardiac arrhythmias are briefly mentioned while focusing on atrial fibrillation. The IEC standards, the electrode device configuration and the target specifications are discussed in Section 2.5. Conclusions are summarized in Section 2.6.

2.1. STRUCTURE AND THE FUNCTIONING OF THE HEART

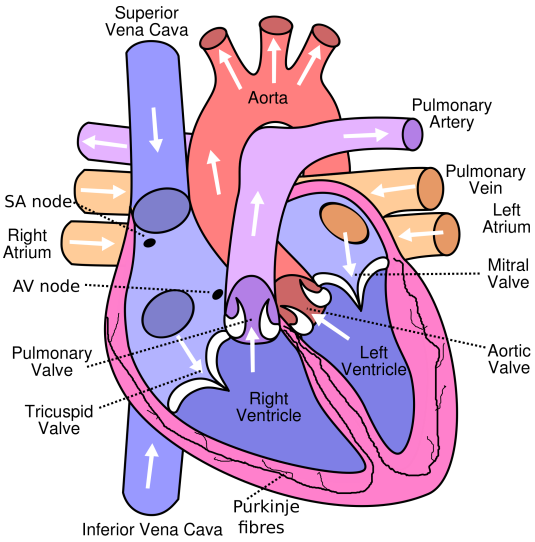


Figure 2.1: Structure of the heart
[9]

The heart is a small muscular organ about the size of a closed fist located in the mediastinum, a region between the sternum and vertebral column. The pericardium surrounds and protects the heart. Three layers form the wall of the heart , i.e., the epicardium, the myocardium and the endocardium. Myocardium makes up for 95 % [10] of the heart and is responsible for the pumping action. The heart has four chambers, two receiving chambers called the atria and two pumping chambers called the ventricles. The right and the left atrium are separated by a thin partition called the intratrial septum

while the ventricles are separated by the intraventricular septum. The right atrium and left atrium are separated from the corresponding ventricles by the tricuspid and the bicuspid mitral valve respectively, as shown in Figure 2.1. The valves open and close in response to changes in pressure in the heart and they ensure the one-way flow of blood [11].

The circulation of blood throughout the body is controlled by the pumping action of the heart. With each beat, the heart pumps blood into two closed circuits arranged in series, the system circulation, where the blood goes to and from the body, and pulmonary circulation, to and from the lungs. During pulmonary circulation, the blood is enriched with oxygen in the lungs through respiration and the oxygenated blood is circulated throughout the body. The left atrium of the heart receives oxygen rich blood from the lungs and passes it to the left ventricle through the mitral valve. The left ventricle then pumps the blood to the rest of the body through smaller arteries. The right atrium of the heart receives deoxygenated blood through systemic circulation from all parts of the body and passes it onto the right ventricle through the tricuspid valve [11]. The right ventricle pumps the blood to the lungs for oxgenation of blood. Once the blood flows in the ventricle, the mitral and the tricuspid valves close on the left and the right side respectively, to prevent the back-flow of the blood in the atria [10]. This entire process constitutes one heart beat or cycle. A network of specialized cardiac muscle fibres is responsible for the conduction system, the electrical activities in the heart leading to the generation of ECG and will be discussed in the following sections.

2.2. CARDIAC CONDUCTION SYSTEM, ACTION POTENTIAL AND THE GENERATION OF ECG

Self excitable specialized cardiac fibres called autorhythmic fibres are responsible for the setting the heart rhythm and function as a natural pacemaker. They also provide the path for the conduction system that ensures the execution of the electrical events in a coordinated manner which is required for the proper functioning of the heart as a pump. The excitation of the heart begins in the sino atrial (SA) node (which contains the autorhythmic fibres) located in the right atrial wall. The cardiac action potential defined as the difference between the internal and external membrane potential and differs significantly in various regions of the heart. Because the potentials differ greatly, the electrical characteristics of each region are distinct. The cardiac impulse originates at the SA node and propagates through the atria leading to the contraction of the atria. It conducts through the cardiac fibres of the atria and reaches the atrioventricular (AV) node which is present between the atria and the ventricles. It then enters the ventricle through the AV bundle. Finally, the cardiac potential reaches the Purkinje fibres and the ventricles then contract. The pacemaker potential in the SA node and the action potential of the ventricular fiber will be explained in the following paragraphs.

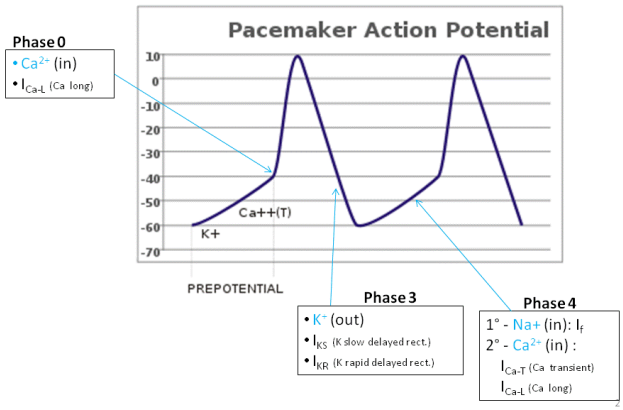


Figure 2.2: Action potential of the autorhythmic fibres of SA node
[12]

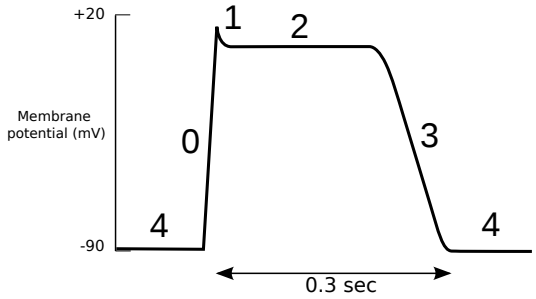


Figure 2.3: Action Potential
[12]

After reaching the threshold voltage, the autorhythmic fibres in the SA node fire action potentials, which is at a much faster rate than other areas and therefore they act as a natural pacemaker as shown in Figure 2.2. On the other hand, the action potential of the ventricular fibres have a resting potential of about -90 mV [10]. The flow of ions across the membranes causes the potentials to rise and fall. Inside the cell membrane, potassium ions K^+ and phosphates are present. Outside the cell, sodium Na^+, calcium Ca^{2+} and chlorine ions Cl^- are present. When the ventricular fibre reaches the threshold voltage due to an action potential, the sodium channels open rapidly. The channels allow sodium ion inflow leading to depolarization. After reaching a potential of 10 mV, the Na^+ inflow decreases. The potential is maintained by the release of Ca^{2+}. The inflow of the Ca^{2+} ions is balanced by the outflow of the K^+ ions. The resting membrane potential is restored when the Ca^{2+} ion channels close while the K^+ ions continue to flow and this process is called re-polarization. The action potential leads to contraction as Ca^{2+} ion concentration increases in the fibre. Figure 2.3 shows the different phases of the action potential denoted by Phase 0 to Phase 4. Phase 4 refers to the resting membrane potential. Phase 0 denotes the depolarization of the wave and the slope represents the maximum rate of change of potential. In Phase 1, the notch is due to the flow of Cl^-, K^+ and Ca^{2+} ions. In Phase 2 denoted by a plateau region, the inflow of Ca^{2+} ions is balanced by the outflow of K^+ ions. Phase 3 represents the repolarization phase.

Electrical signals are generated throughout the body as the action potentials conduct through the heart and can be detected on the surface of the body. These electrical signals can be recorded using an electrocardiograph and is called an electrocardiogram. The recorded ECG is the result of the cardiac action potential generated by the cardiac muscle fibres. This record can be used for diagnosis of any abnormality in the heart. In the following section, the ECG signal generation and its correlation with the atrial and the ventricular polarization and depolarization will be described.

2.3. ELECTROCARDIOGRAM

Electrodes are placed on the surface of the body to record the ECG. The ECG is a composite wave that is a result of the net potential difference generated by the cardiac muscle fibres. A set of ten electrodes, one on each of the arms and the legs, and six positions on the chest, are used to obtain 12 different leads using the electrocardiograph as shown in Figure 2.4. For a detailed nomenclature of the leads of the ECG, the reader can refer to [4]. Each of the leads carry information about the working of the heart. By appropriate interpretation of the recorded ECG, information regarding the conducting pathway and possible damage to any region of the heart or the cause of chest pain or increased heart rate can be determined.

2.3.1. CHARACTERISTICS OF THE ECG SIGNAL

In a typical ECG record [14], in each heart beat, three distinguished waves appear. They are the P wave, the QRS complex and the T wave as shown in Figure 2.5. The P wave represents atrial depolarization which originates at the SA node and propagates through the atria to the AV node. After the P wave, the atria contract and there is a short delay before the ventricular contraction begins. The action potential propagates through the AV bundle, Purkinje fibres and the ventricular fibres resulting in ventricular

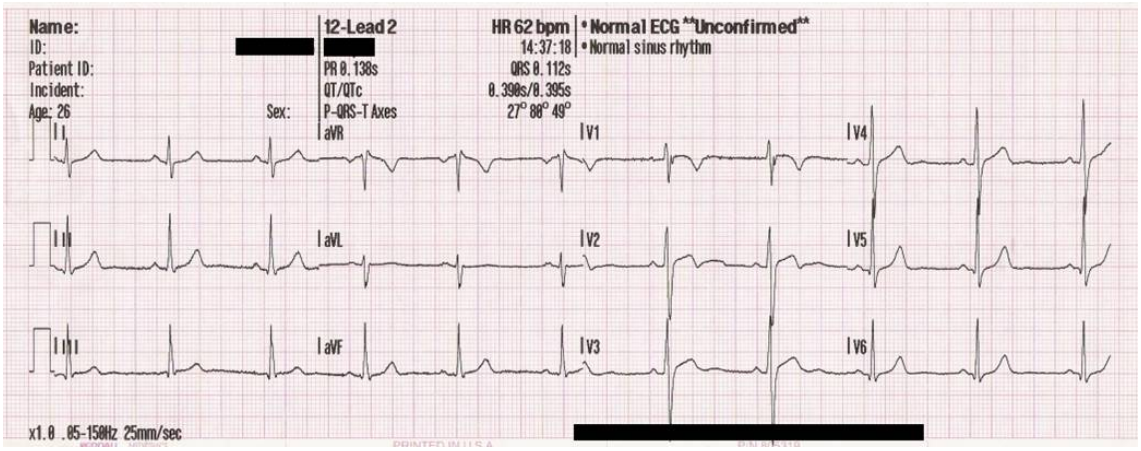


Figure 2.4: 12 lead ECG
[13]

depolarization. This is represented by the QRS complex. The atria undergo repolarization as well but this does not appear in the ECG as it is masked by a large QRS complex wave. The QRS complex is followed by ventricular contraction represented by the ST segment. Repolarization of ventricles is represented by the T wave. After the T wave appears, the ventricles relax and thus complete one ECG cycle.

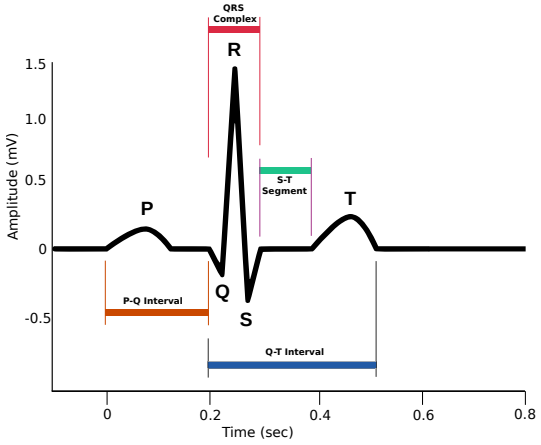


Figure 2.5: Electrocardiogram
[13]

2.4. ARRHYTHMIAS

The magnitude of the amplitude of the waves in an ECG, the time spans between waves and the presence or absence of waves could indicate abnormalities in the functioning of the heart.

By carefully analyzing the recorded ECG and comparing with normal ECGs, the heart disease can be diagnosed. Figure 2.6 illustrates some cardiac arrhythmias. In Figure 2.6a, some of the P waves are not immediately followed by the QRS complex and the T wave. Second degree block is characterized by delay or interruption of the action potential through the AV node. Figure 2.6b represents atrial fibrillation caused by the asynchronous contraction of the atria and ventricles. It is characterized by irregular R-R intervals, no distinct P waves and irregular P-R intervals. The rhythm of the heart is both irregular and the efficiency of the pumping reduces. In Figure 2.6c, irregularity is observed between the QRS complexes. Ventricular tachycardia originates in the ventricles and is characterized by frequent ventricular contractions. Figure 2.6d represents ventricular fibrillation. There is no clearly defined P, QRS or T wave and the phenomenon is characterized by lack of synchronized activity on the ECG

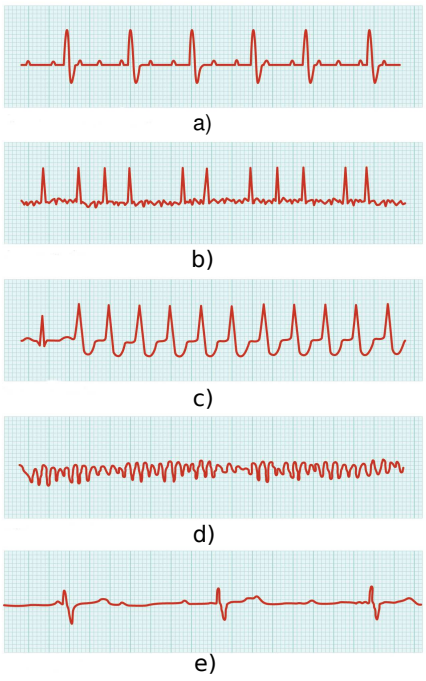


Figure 2.6: Representative arrhythmias. a)Second degree block b)Atrial fibrillation c)Ventricular tachycardia d)Ventricular fibrillation e)Third degree block

[15]

record. As ventricular pumping stops, the blood circulation would cease leading to complete failure of the body. Third degree AV block is represented by Figure 2.6e. Some of action potential impulses originating at the SA node do not reach the AV node and there is little or no conduction through the AV node to the rest of the heart. In this type of arrhythmia, the heart beats occur independent of the P waves.

Figure 2.7 shows a time domain signal of a typical ECG. The inset shows a magnified view of the signal and the waves can be observed clearly. The raw ECG data were taken from the MIT-BIH database [16]. The FFT of the time domain signal was taken to determine the PSD plot and is shown in Figure 2.8. For the sake of comparison, the time domain ECG signal during the occurrence of atrial fibrillation is shown in Figure 2.9. The inset shows an enlarged view of a part of the ECG signal which shows the absence of P-waves and irregular QRS waves. The corresponding FFT plot is shown in Figure 2.10. The diagnosis of atrial fibrillation can be made from the recorded ECG. It is characterized by the irregular R-R waves and the absence of P waves as can be seen clearly in the inset of time domain plot in Figure 2.9.

In designing an ECG recording device and in order to preserve the information contained in the ECG for proper diagnosis, the IEC has laid out standards for the device manufacturers. These standards serve as a guideline to set the specifications and device configurations which are explained in the next section.

2.5. IEC STANDARD, SPECIFICATIONS AND THE CONFIGURATION OF THE ECG PATCH

The IEC or the American Heart Association (AHA) have established standards for the recording and acquisition of ECG signals that serve as a guideline to set the specifications of the ECG measurement devices. For example, IEC 60601-2-47 elaborates on the requirements for the performance of ambulatory electrocardiographs [5]. According to the standard, an electrode is defined as a sensor that is in contact with the body that conducts the electrical signal for detection while the lead is defined as the voltage difference between the electrodes. The input impedance should be greater than 10 MΩ. The common

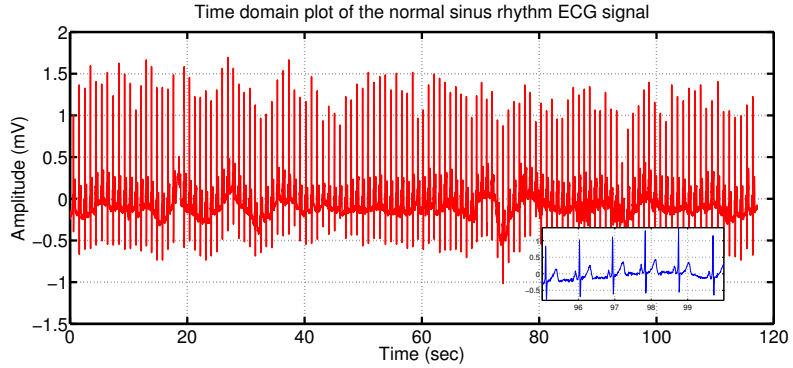


Figure 2.7: Time domain ECG signal (normal sinus rhythm)

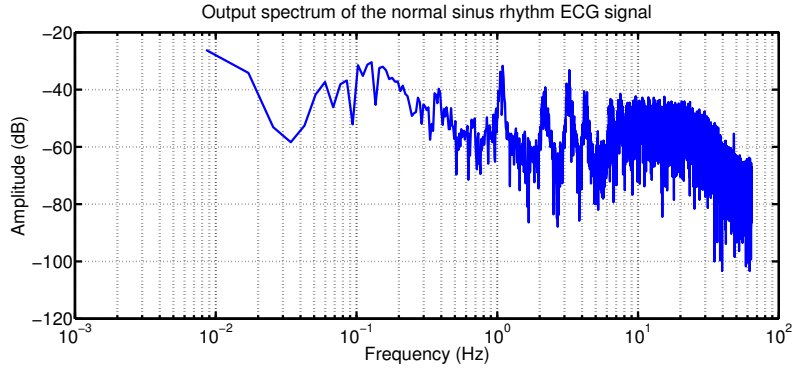


Figure 2.8: PSD of ECG signal (normal sinus rhythm)

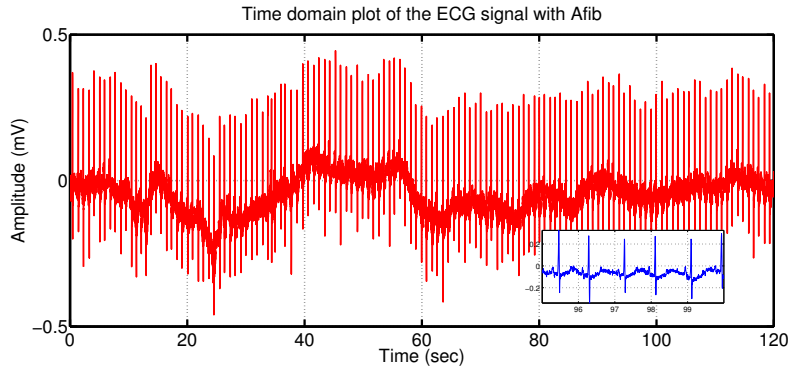


Figure 2.9: Time domain ECG signal (atrial fibrillation)

mode rejection should be at least 60 dB. The total noise referred to the input should not exceed 50 μV p-v over a 10 s period. For the detection of atrial fibrillation, a signal bandwidth of 0.67 - 40 Hz is sufficient, and in view of any future application requirement, the system is being designed for a signal bandwidth of 0.5-200 Hz. This set of specifications form the general overall system specification. More elaborate block wise specification will be derived and discussed in the following chapters.

The proposed design of the ECG patch device is similar to the one shown in Figure 2.11. It consists of three electrodes placed 35 mm apart. The placement of the electrodes with respect to each other is as shown in Figure 2.12. Although two electrodes would be sufficient to record the ECG signal, three electrodes would be make the position or the orientation of the patch rotation and translation invariant. The electronic module would be clipped onto the substrate patch. For each recording the electrodes and the substrate would be changed while retaining the electronic module. The ECG patch is battery operated and would use Li/MnO2 based batteries. for example CR 2430 with a rated capacity of 280 mAh. It is aimed at continuously recording the ECG for at least 48 hours.

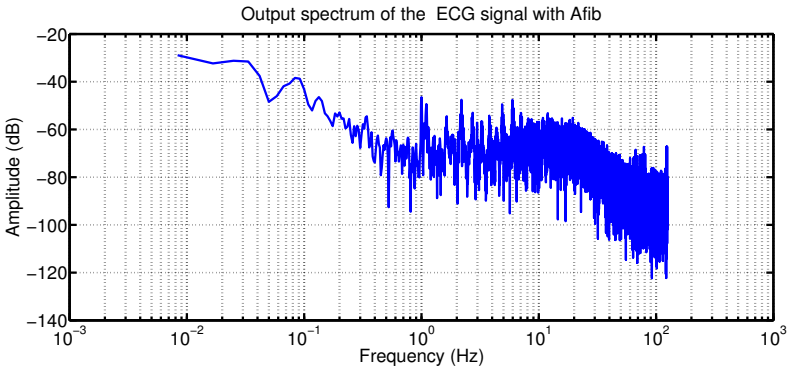


Figure 2.10: PSD of ECG signal (atrial fibrillation)

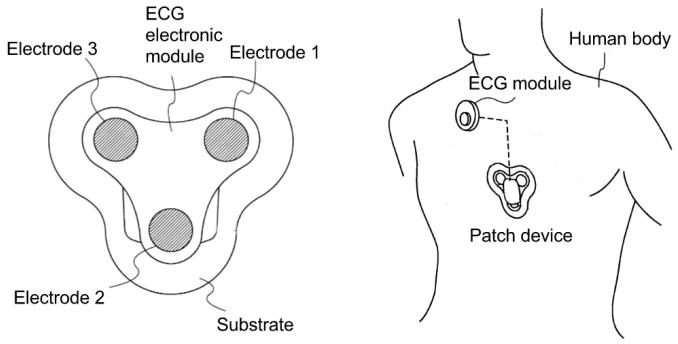


Figure 2.11: Patch device
[17]

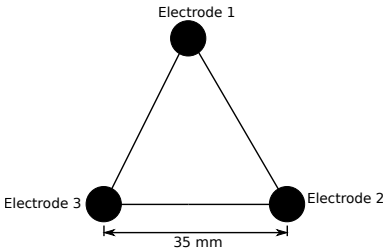


Figure 2.12: Electrode placement

2.6. CONCLUSIONS

In this chapter, an overview was given about the functioning of the heart and the generation of the ECG signal. The ECG signal is generated through a complex set of steps involving the movement of ions across the membrane and leading upto the generation of the cardiac signal. The characteristics of the ECG wave and the various cardiac arrhythmias were discussed in brief. Finally, the chapter concludes with the ECG system specifications and the patch device.

3

State-space based high-pass ΔΣ converters: A design methodology

In this chapter, a synthesis procedure for developing the state-space based high-pass delta-sigma (ΔΣ) converters is described. The aim of the analysis is to propose structures that are suitable for designing the analog front-end for ECG signal acquisition which incorporates high-pass (HP) filtering for a given set of constraints. In the proposed approach, standard state-space forms are applied for developing the ΔΣ topologies satisfying the HP characteristic of the loop filter. Each of the resulting state-space based high-pass ΔΣ ADCs offer various degrees of freedom while satisfying the transfer function requirements.

In Section 3.1, some of the possible approaches that can be taken to develop the analog front end for a biomedical acquisition system are discussed. The basic theory and background about a conventional ΔΣ ADC is explained in Section 3.2. In Section 3.3, the need and significance of a strucutred approach towards developing the HP ΔΣ ADCs is explained . In Section 3.4, the proposed methodology is described followed by Section 3.5 where the structures are elaborated in detail. It is followed by Section 3.6, where the conclusions of the chapter are summarized.

3.1. Top level approaches

Conventionally, a complete analog front-end for a given application includes a combination of various circuit blocks such as a pre-amplifier (pre-amp), a low pass filter (LPF), a high-pass filter (HPF), a programmable gain amplifier (PGA), an anti-aliasing filter (AAF) (in case an analog LPF is not used) and an analog to digital converter (ADC) for digitizing the signal. Designers adopt different approaches for partitioning and implementing amplification, filtering and digitization. Figure 3.1 summarizes several of the possible approaches.

In each of the approaches, filtering can either be fully implemented in the analog domain, or in the digital domain, or partly in analog and in the digital domain i.e., mixed signal domain. A band pass filter (BPF), a PGA and an ADC are used to realize the analog front end (AFE) [7]. A BPF and a fixed amplifier gain is implemented in a single block where the BPF is implemented with the help of a capacitor and pseudoresistors [6] [18]. An integrator in the feedback loop around the amplifier can be used to implement HP cut-off [19]. In many applications, the HP cut- off frequency of the ECG signal bandwidth corresponds to a time constant of 20 s which is a challenge for implementation on chip with respect to area occupation and the accuracy of the cut-off frequency. Mixed signal feedback technique has previously been used with ΔΣ ADC [20] and boxcar sampling ADC [21] to implement the high-pass integrator.

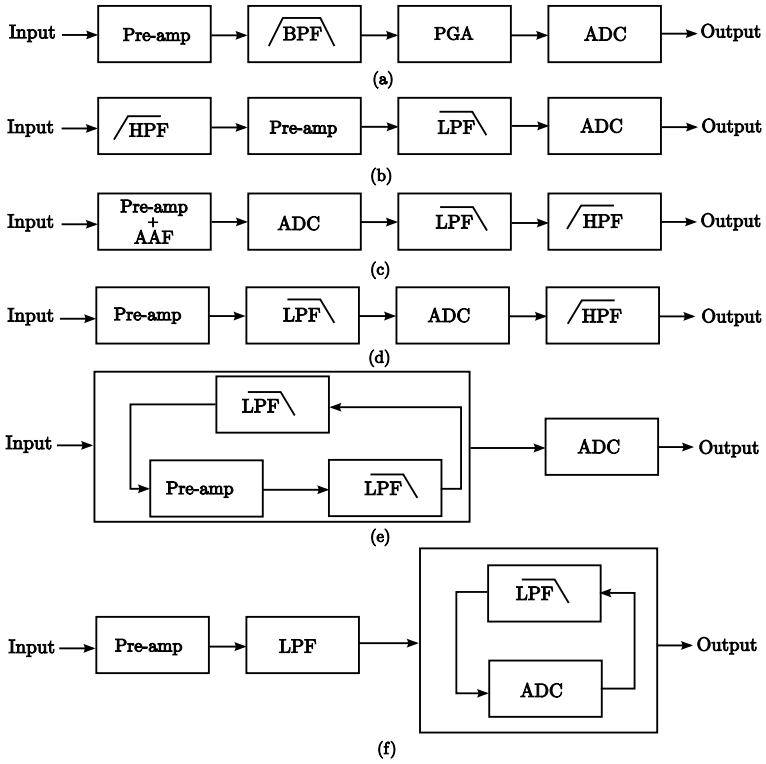


Figure 3.1: Several possible top level approaches

Table 3.1: SAR vs ΔΣ ADC

	SAR	Delta-Sigma
Benefits	Low power consumption High sampling speed	High resolution Inherently linear
Limitations	Component matching issues limit resolution	High power consumption

Among the several top level approaches, the one shown in Figure 3.1f will be adopted in this thesis project to implement the HP filter. It is expected that the excess noise due to the feedback loop would be suppressed by the gain from the earlier stages. An integrator with low pass filter characteristic in negative feedback connected from the output to the input would result in a high-pass filter characteristic in the signal path which is necessary to realize the high-pass cut-off frequency.

Regarding the choice of ADC, both SAR and ΔΣ ADCs are competitive structures. The final choice is application dependent and they have several benefits and limitations. In this thesis, a ΔΣ ADC is chosen due to its inherent linearity. While the SAR ADCs are used for low power consumption, their linearity is limited by the component mismatch. Table 3.1 compares the two types of ADCs. ΔΣ ADCs take advantage of noise shaping property to achieve very low quantization noise. Before delving into the high-pass ΔΣ topologies, it is of vital importance to describe the basic structure and functioning of a conventional ΔΣ architecture which is elaborated in the following section.

3.2. CONVENTIONAL ΔΣ ADC

At the heart of a ΔΣ converter is a loop filter, a 1-bit comparator and a 1-bit DAC. A simplified top level block diagram of a ΔΣ converter is shown in Figure 3.2 The loop filter consists of integrators or resonators which could be either continuous time or discrete time filters. The 1-bit ADC is a clocked comparator operating at a sampling frequency, f_s. A 1-bit DAC is a switch that assigns analog values

to the output of the comparator. Although the multibit DACs can also be used, single bit modulators are preferred for their inherent linearity. A detailed discussion on these various choices regarding the different circuit blocks will follow in Chapter 5.

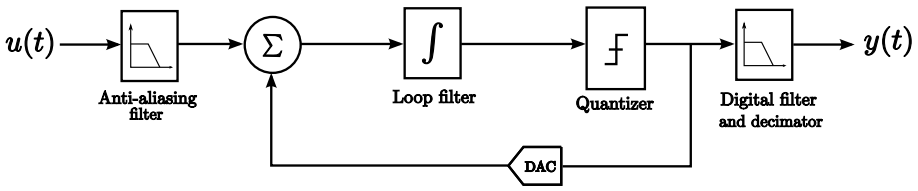


Figure 3.2: Simplified top level block diagram of ΔΣ ADC

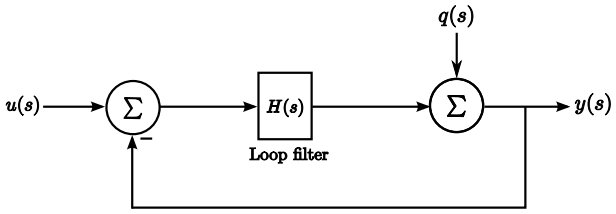


Figure 3.3: Linear model of ΔΣ modulator

To illustrate the noise shaping property of the ΔΣ converters, the linear model of the ΔΣ converter is shown in Figure 3.3. The quantization error is a random variable and uncorrelated with the input and is therefore, assumed to have statistical properties. The quantizer is modeled by an additive white noise source [22]. The non-linear quantizer is now replaced by a linear model which simplifies the analysis of the ΔΣ converters [23].

Assuming a continuous-time representation of the loop filter, linear analysis is done in Laplace domain. However, an equivalent analysis in z-domain can also be done for a discrete-time loop filter implementation. Referring to Figure 3.3, the poles and the zeros of the system with respect to the signal input and the quantization noise input can be mathematically illustrated through the signal transfer function (STF) and noise transfer function (NTF) respectively. The STF and NTF are given by

$$STF = \frac{y(s)}{u(s)} = \frac{H(s)}{1+H(s)}; \quad NTF = \frac{y(s)}{q(s)} = \frac{1}{1+H(s)} \tag{3.1}$$

where y(s) is the output signal, u(s) is the input signal and q(s) is the quantization noise.

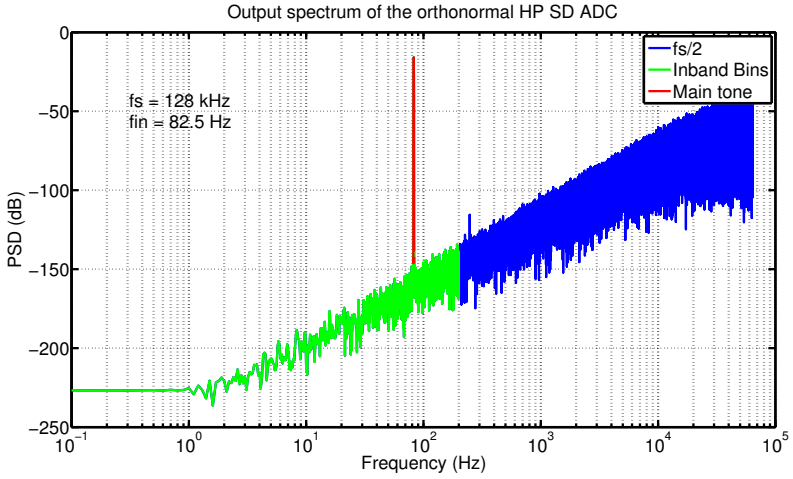


Figure 3.4: NTF of conventional 2nd order ΔΣ ADC

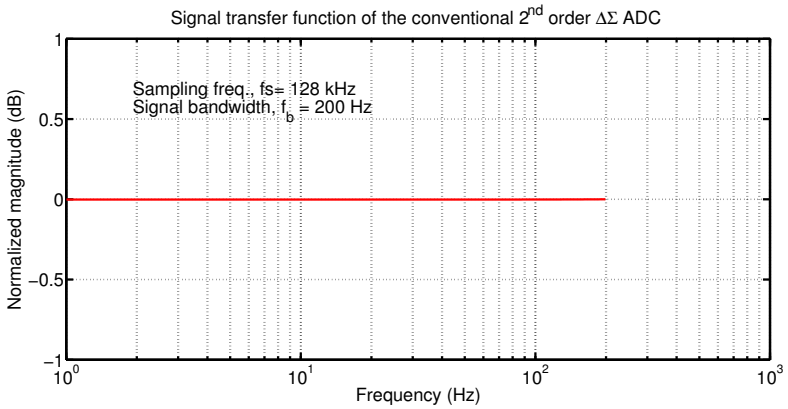


Figure 3.5: STF of conventional 2nd order ΔΣ ADC

From Equation 3.1, it can be seen that the input signal is low pass filtered while the quantization noise is suppressed by the loop filter. The NTF and STF of a conventional 2nd order ΔΣ modulator are shown in Figure 3.4 and 3.5 respectively. It can be seen that the shaping of the noise is 2^{nd} order shaped with a slope of 40 dB/dec. The input frequency is denoted by the maintone (in red) while the signal bandwidth by the inband bins (in green) and the noise bins (in blue) upto the Nyquist frequency and this convention will be followed throughout the thesis.

3.3. SIGNIFICANCE OF THE PROPOSED METHODOLOGY

Depending on the application, the range of bandwidth of the ECG signal is subset of the frequency range 50 mHz to 200 Hz. It is possible to partition the lower and the upper cut-off frequencies to realize them in separate blocks. As opposed to low pass signal transfer in conventional sigma delta converters, in this thesis, the signal transfer function is generalized to accommodate a low-pass, high-pass, notch or a bandpass filter characteristic. To develop ΔΣ topologies that satisfy the application requirements, the existing standard state-space forms namely biquad, orthonormal and canonical structures are used. Each of the state-space forms have certain degrees of freedom and differ in their properties. These properties will determine the overall performance of the ΔΣ structures. For the sake of simplicity and clarity, the investigation is limited to third order systems.

Conventionally, ΔΣ converters have a low pass signal transfer function. A structured design procedure is necessary that makes use of the existing state-space forms to arrive at the desired high-pass ΔΣ structures. The following section elaborates on the utilization of the existing standard state-space forms, evaluation of the coefficients and the placement of the quantizer in order to satisfy the signal and noise transfer functions of the high-pass ΔΣ ADCs while keeping the application constraints and requirements in mind.

3.4. PROPOSED DESIGN METHODOLOGY

Designing a system that incorporates filtering and digitization using an orthogonal design methodology allows us to systematically arrive at the different topologies while optimizing the performance metrics relevant to low voltage and low power designs such as dynamic range, sensitivity to coefficient variations and sparsity of these topologies. For a given state-space form, the coefficients can be evaluated for their contribution to the desired signal characteristic and noise transfer requirements. It is initially assumed that the signal transfer function could either be low-pass, high-pass, bandpass or notch. In this specific application, a high-pass signal transfer function is the requirement. For a given system of n^{th} order and the required signal transfer type, one can develop the corresponding topologies.

A design methodology based on state-space forms is proposed to develop a ΔΣ converter system which meets the requirement of both the NTF and STF. The required STF is a high-pass characteristic. A

generic 3rd order system which consists of a 2nd order $\Delta\Sigma$ modulator and an integrator in the feedback loop is evaluated. Depending on the design requirements as per specifications, a higher order modulator could be chosen. Based on the filter requirements of the application and the practical constraints, the coefficients of the state-space form are chosen.The coefficients of the state-space form correspond to physical components to be realized in silicon which play a significant role in determining the noise, area and power consumption. Therefore, the fewer the number of non-zero coefficients, the lesser the area occupied on chip. At higher orders, the number of non-zero coefficients is larger. Sparsity will be a significant metric only at higher orders and will therefore be a secondary criterion for the selection of an optimal topology. As mentioned earlier, the investigation is limited to third order systems and evaluation of sparsity is beyond the scope of this thesis. However, an interested reader is referred to Haddad's work [24] [25] for further reading.

For a given transfer function, it is known that the state-space description is not unique. In the following subsections, a few well known state-space forms such as biquadratic, observable canonical, controllable canonical and orthonormal forms will be analyzed for their suitability for developing $\Delta\Sigma$ ADC topologies.

For the choice of an optimal design topology, the specifications of the loop filter are as follows :

1. STF is a high-pass characteristic (with at least a single-pole roll off).
2. NTF is a high-pass transfer characteristic with the order of noise shaping (real zeros at DC and/or presence of complex conjugate zeros) equaling the order of the modulator.
3. Possibility of filter implementation in the analog, digital or mixed signal domain

The dynamic range which is determined by the maximum signal that is processable without clipping at the upper limit and the internally generated noise in the system defining the lower limit will be used as a performance criteria to evaluate the various $\Delta\Sigma$ topologies. Also, the integrators can be internally scaled without changing the overall transfer function to exploit the maximum available range given by the supply voltage and the given technology.

In this thesis, the investigation is limited to the use of one quantizer. Although fundamentally multiple quantizers could be used and the output can be summed in the binary domain, the use of one quantizer is a practical constraint. In other words, single loop modulators are being explored.

The proposed design procedure that generates the $\Delta\Sigma$ topologies while implementing filtering and noise shaping as desired is shown in the flowchart in Figure 3.6. The starting point in the flowchart is the selection of the order of the system and then the state-space type. The coefficients of the selected state-space form are evaluated to satisfy the signal transfer function depending on the application requirement. The constraint on the quantization noise transfer is taken into account and the quantizer is placed such that the NTF is satisfied. The STF and the NTF requirements of the loop filter are finally verified by transfer function calculations. In case the requirements are not met, the coefficients are assessed again for their contribution to the transfer function. The process is repeated until both signal and noise transfer functions are satisfied. Finally, the state-space form is redrawn as a $\Delta\Sigma$ topology.

For demonstration, the proposed method will be applied on standard state-space forms as shown in the next section. The methodology is exemplified in subsections 3.5.1 to 3.5.4. Here, the state-space forms will be transformed into corresponding $\Delta\Sigma$ topologies according to the steps listed out in the flow chart.

3.5. STATE-SPACE DESCRIPTION

A dynamic system can be described using a set of 1st order differential equations. The general state-space description of an nth order system is given by

$$\dot{\mathbf{x}}(t) = \mathbf{A}\mathbf{x}(t) + \mathbf{b}u(t) \tag{3.2}$$

$$y(t) = \mathbf{c}^{\mathbf{T}}\mathbf{x}(t) + du(t) \tag{3.3}$$

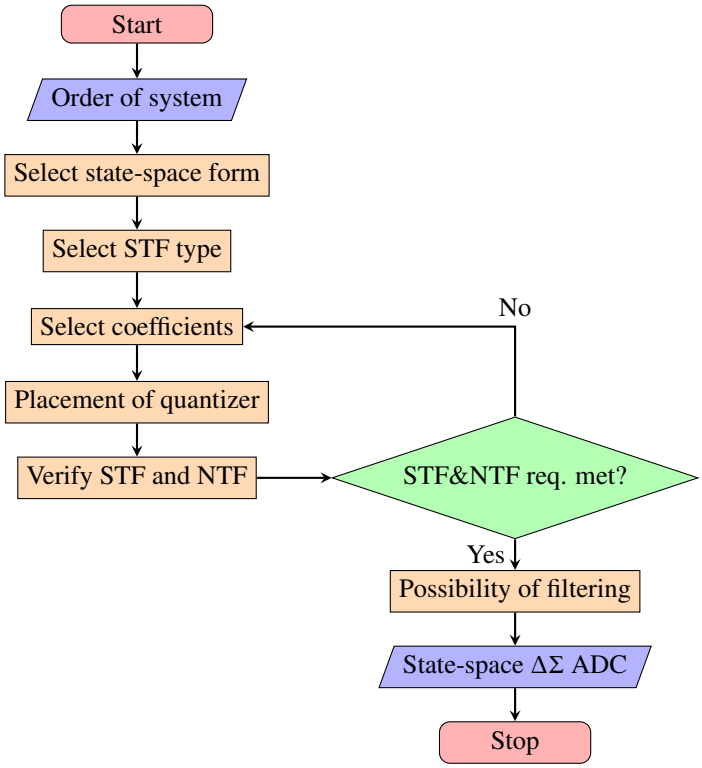


Figure 3.6: Flowchart of the state-space approach for ΔΣ topologies

where $\mathbf{x}(t)$ is an n x 1 vector representing the integrator states or outputs, $\mathbf{A}$ is an n x n state matrix that describes how the integrators are interconnected through feedback and feedforward paths, where n is the number of integrators or the order of the system, $\mathbf{b}$ is an n x 1 vector that describes how the input signal is applied to the integrators, $\mathbf{c}$ is an n x 1 vector that contains the set of coefficients that multiply the output states and summed together and d is a scalar that represents the feedthrough component from the input directly to the output. $u(t)$ and $y(t)$ are the input and the output signal respectively.

3.5.1. BIQUAD FORM

A cascade of biquadratic blocks (for even order systems) and a 1^{st} order block (in case of odd order systems) can be used to construct higher order systems. Any stable transfer function can be implemented as a cascade of biquads. The block diagram of a 3^{rd} and an n^{th} order biquad is shown in Figure 3.7. The coefficients of biquad state-space form are also shown in the figure.

Starting from the standard state-space representation of a biquad, it is possible to arrive at the corresponding ΔΣ structure by determining the effect of each coefficient on the location of poles and zeros of the signal and the noise transfer functions. It is assumed that the signal enters the system only through the first integrator, i.e. $b_{12} = d = 0; b_{11} \neq 0$. In order to obtain the desired STF, the 1^{st} order integrator in cascade can be used in a negative feedback loop. The scaling coefficient of the integrator will determine the high-pass cut-off frequency. Although a first order high-pass characteristic is analyzed here, higher order roll off can be designed if required.

Finite non-zero values of a_{11} and a_{22} lead to the displacement of the zeros of the NTF away from DC and hence, optimal noise shaping in the bandwidth cannot be achieved. Therefore, the values of a_{11} and a_{22} equal 0; finite non zero value of a_{12} leads to the existence of complex zeros of the NTF. For optimum performance, the value of a_{12} is chosen such that the complex poles occur within the bandwidth. If $a_{12} = 0$, all the zeros are at DC. In both the cases, the desired NTF can be achieved. To minimize the number of physical components, the value of a_{12} is made zero.

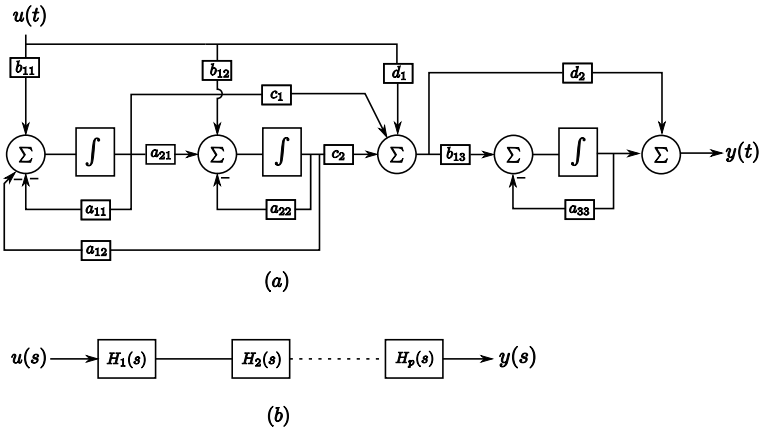


Figure 3.7: (a) 3rd order biquad form (b) nth order biquad

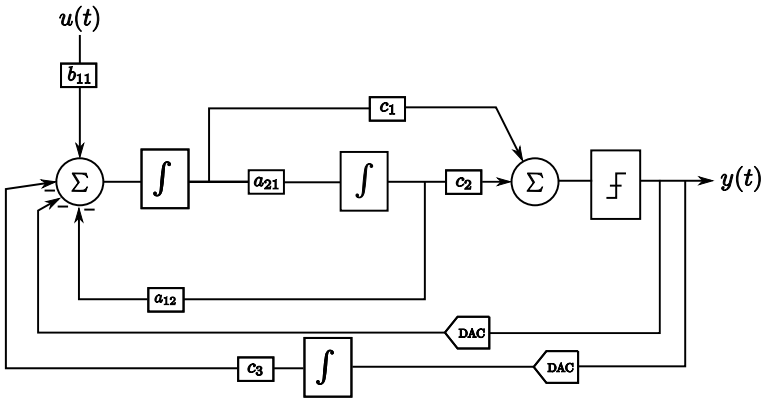


Figure 3.8: Biquad based 2nd order HP ΔΣ ADC

A 2nd order ΔΣ modulator with a 1st order high-pass loop is drawn and shown in Figure 3.8. The biquad and the 1st order integrator are in cascade. The quantizer is positioned between the biquad and the integrator in the feedback loop.

A linear model of the biquad form based HP ΔΣ in the s-domain is as shown in Figure 3.9. The quantizer is replaced by a white noise source for linear analysis as motivated in Section 3.2. Let $k_1$and k_3 be the scaling coefficients of the first and the high-pass integrator respectively (not shown in the linear model). a_{21} is the scaling coefficient of the second integrator.

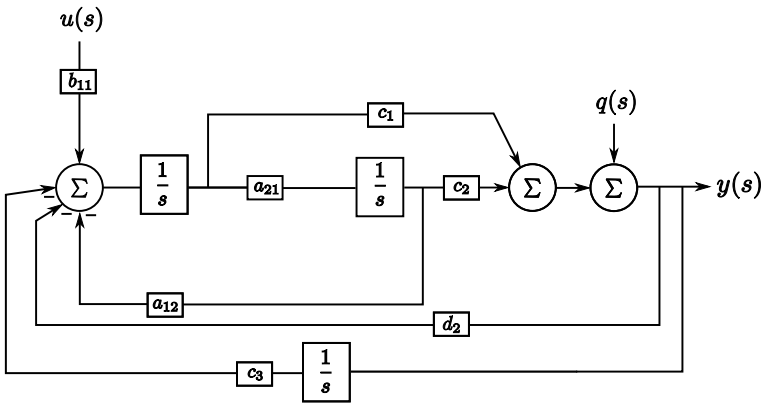


Figure 3.9: Linear model of biquad based 2nd order HP ΔΣ ADC

The STF of the biquad based HP ΔΣ ADC can be derived and written as

$$STF = \frac{sb_1k_1(c_1s + a_{21}c_2)}{s^3 + k_1d_2c_1s^2 + (k_1d_2a_{21}c_2 + k_1a_{21}a_{12})s + k_1k_3a_{21}c_2c_3} \tag{3.4}$$

Similarly, the NTF of the biquad based HP ΔΣ ADC can be derived and written as

$$NTF = \frac{s(s^2 + a_{21}a_{12}k_1)}{s^3 + k_1d_2c_1s^2 + (k_1d_2a_{21}c_2 + k_1a_{21}a_{12})s + k_1k_3a_{21}c_2c_3} \tag{3.5}$$

The location of the poles can be determined by solving the 3rd degree characteristic equation (CE):

$$CE = s^3 + k_1d_2c_1s^2 + (k_1d_2a_{21}c_2 + k_1a_{21}a_{12})s + k_1k_3a_{21}c_2c_3 \tag{3.6}$$

The roots of the CE determine the three poles of the system. The poles can either be a set of all real poles or a set of one real pole and a pair of complex conjugates. One of the poles p_1, close to DC which is a strong function of c_3 determines the high-pass cut-off frequency. Solving a third degree equation is not trivial and therefore MATLAB can be used to obtain the solution to the equation.

$$s^3 + k_1d_2c_1s^2 + (k_1d_2a_{21}c_2 + k_1a_{21}a_{12})s + k_1k_3a_{21}c_2c_3 = 0 \tag{3.7}$$

As the frequency of the pole location is very small, s^2 and s^3 are made zero and Equation 3.7 can be written as

$$(k_1d_2a_{21}c_2 + k_1a_{21}a_{12})s + k_1k_3a_{21}c_2c_3 = 0 \tag{3.8}$$

Assuming real zeros (at DC), $a_{12} = 0$. For very low frequencies, Equation 3.8 can be approximated as

$$s \approx p_1 = -\frac{c_3k_3}{d_2} \tag{3.9}$$

From Equation 3.9, we observe that p_1 is a function of k_3, c_3 and d_2 which determines the exact location of the pole. By setting the values of these coefficients, the pole location and therefore the high-pass cut-off frequency can be accurately fixed.

3.5.2. OBSERVABLE CANONICAL FORM

The observable canonical state-space type is used to develop the observable canonical based ΔΣ topology. The output of the system is fed back to the input of each of the integrators through coefficients which determine the poles of the system. The block diagram of the standard observable form is shown in Figure 3.10.

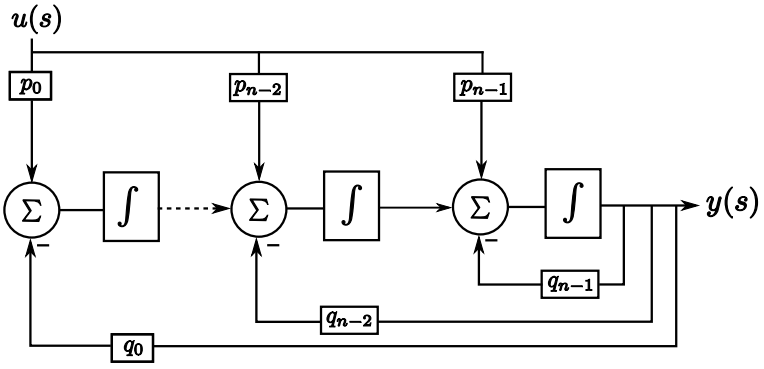


Figure 3.10: Block diagram of the nth order observable canonical form

The state-space description of the observable canonical form is given by

$$\mathbf{A} = \begin{bmatrix} 0 & 0 & 0 & \dots & 0 & -q_0 \\ 1 & 0 & 0 & \dots & 0 & -q_1 \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ 0 & 0 & \dots & 0 & 0 & -q_{n-2} \\ 0 & 0 & \dots & 0 & 1 & -q_{n-1} \end{bmatrix}; \quad \mathbf{b} = \begin{bmatrix} p_0 \\ p_1 \\ \vdots \\ p_{n-2} \\ p_{n-1} \end{bmatrix}; \quad \mathbf{c}^{\mathbf{T}} = [0 \quad 0 \quad \dots \quad 0 \quad 1]; \quad d = 0 \tag{3.10}$$

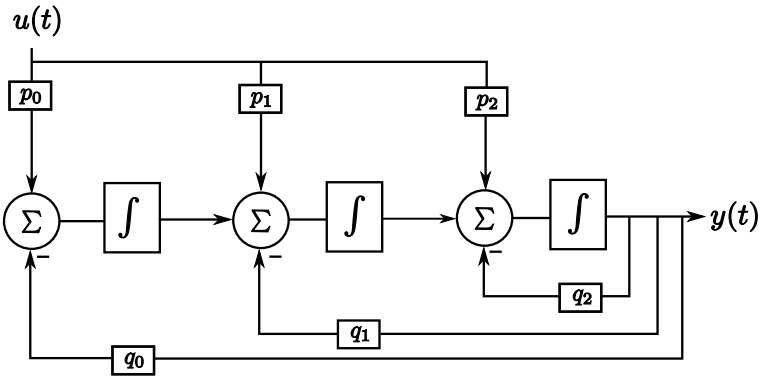


Figure 3.11: Block diagram of the 3rd order observable canonical form

To obtain a high-pass characteristic, $p_0 = 0$ referring to Figure 3.11. We assume that the signal enters the system through the first integrator only. Therefore, $p_1 \neq 0$ and $p_2 = 0$.

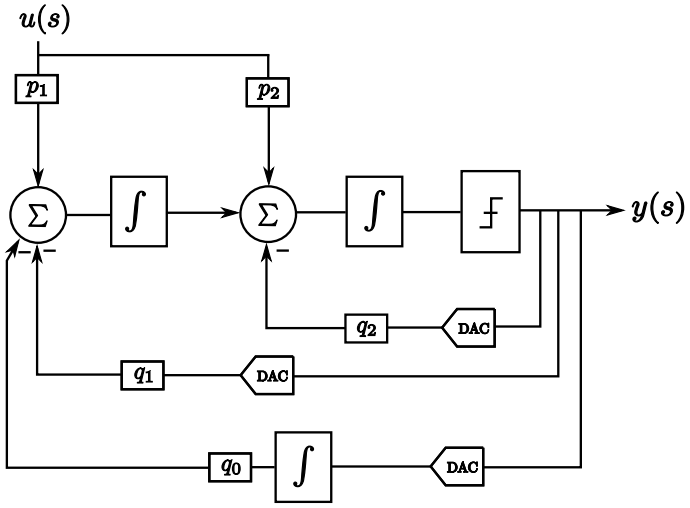


Figure 3.12: Observable canonical based 2nd order HP ΔΣ ADC

The 2nd order ΔΣ modulator with a 1st order HP integrator is shown in Figure 3.12. The quantizer is placed after the 3rd integrator. The linear s-domain model of the observable canonical form based ΔΣ is as shown in Figure 3.13.

The STF is given by the following equation

$$STF = \frac{s(p_2 k_2 s + p_1 k_1 k_2)}{s^3 + k_2 q_2 s^2 + k_1 k_2 q_1 s + k_1 k_2 k_3 q_0} \tag{3.11}$$

The NTF is given by the following equation

$$NTF = \frac{s^3}{s^3 + k_2 q_2 s^2 + k_1 k_2 q_1 s + k_1 k_2 k_3 q_0} \tag{3.12}$$

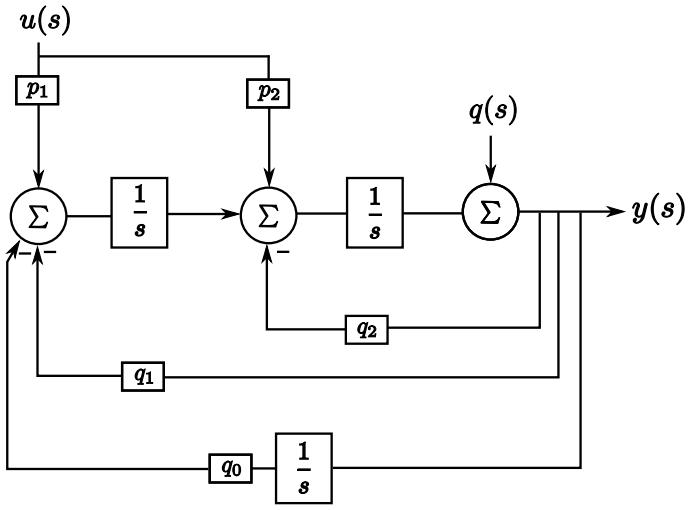


Figure 3.13: Linear model of observable canonical based 2nd order HP ΔΣ ADC

From Equation 3.11 and 3.12 , it is verified that the STF and NTF requirements of the observable ΔΣ converter are met. For the STF, there is at least one zero at DC (single pole roll off) and three zeros at DC for the NTF.

One solving the CE, the location of the HP pole close to DC can be determined.

$$s^3 + k_2 q_2 s^2 + k_1 k_2 q_1 s + k_1 k_2 k_3 q_0 = 0 \tag{3.13}$$

The location of the pole predominantly depends on the value of q_0 and q_1.

3.5.3. CONTROLLABLE CANONICAL FORM

In the controllable canonical form, the integrator outputs are connected through feedback to the control input. The block diagram of the nth order controllable canonical form is shown in Figure 3.14.

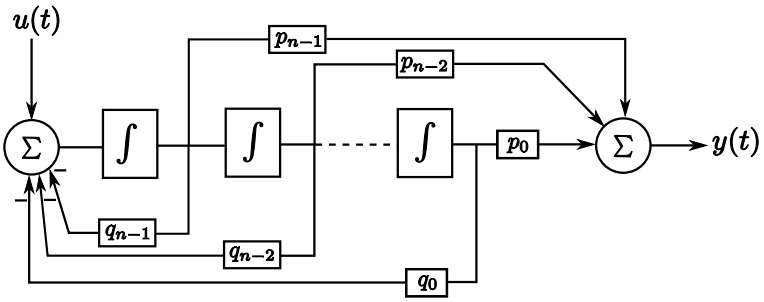


Figure 3.14: nth order controllable canonical filter

The state-space description of the controllable canonical form is given by

$$\mathbf{A} = \begin{bmatrix} 0 & 1 & 0 & \dots & 0 \\ 1 & 0 & 0 & \dots & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ 0 & 0 & 0 & \dots & 1 \\ -q_0 & -q_1 & -q_2 & \dots & -q_{n-1} \end{bmatrix}; \quad \mathbf{b} = \begin{bmatrix} 0 \\ 0 \\ \vdots \\ 0 \\ 1 \end{bmatrix}; \quad \mathbf{c}^{\mathbf{T}} = \begin{bmatrix} p_0 & p_1 & \dots & p_{n-2} & p_{n-1} \end{bmatrix}; \quad d = 0 \tag{3.14}$$

Referring to Figure 3.15, to meet the high-pass filter requirement, the value of $p_0 = 0$. The controllable canonical based 2nd order ΔΣ converter is drawn and shown in Figure 3.16

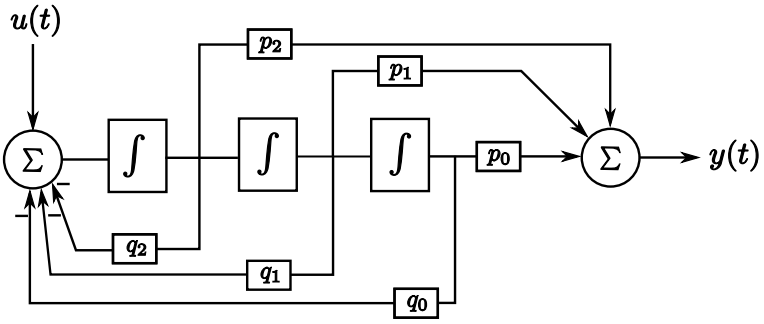


Figure 3.15: Block diagram of the 3rd order controllable canonical form

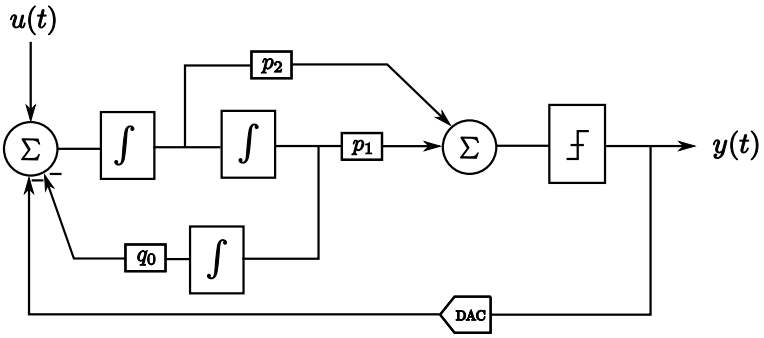


Figure 3.16: Controllable canonical based 2nd order ΔΣ ADC

A linear model of the controllable canonical form based ΔΣ in the s-domain is as shown in Figure 3.17.

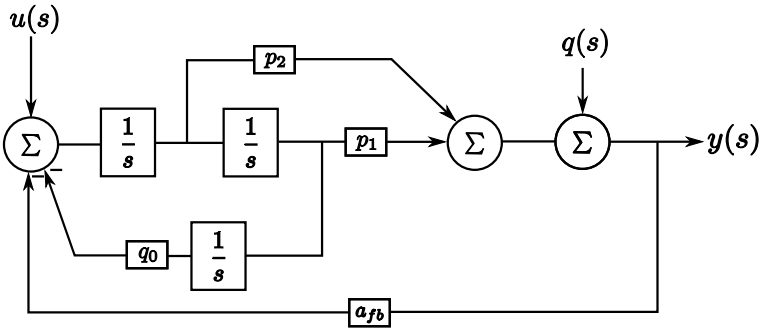


Figure 3.17: Linear model of controllable canonical based 2nd order ΔΣ ADC

To meet the STF requirement, p_0 is equal to 0. To obtain the desired NTF, q_2 and q_1 equal 0.

The STF and the NTF equation can be written as

$$STF = \frac{b_1 k_1 s(p_2 s + p_1 k_2)}{s^3 + a_{fb} k_1 p_2 s^2 + a_{fb} k_1 k_2 p_1 s + k_1 k_2 k_3 q_0} \tag{3.15}$$

$$NTF = \frac{s^3 + k_1 k_2 k_3 q_0}{s^3 + a_{fb} k_1 p_2 s^2 + a_{fb} k_1 k_2 p_1 s + k_1 k_2 k_3 q_0} \tag{3.16}$$

From the Equation 3.15, it can be seen that there exists one zero at DC which satisfies the STF requirement. From Equation 3.16, solving the CE gives us one real zero and a pair of complex poles which is dependent on the value of q_0.

Only analog implementation of the integrator in the feedback loop is possible. The HP pole location is not independent of the location of the optimal NTF zeros. In other words, p_1 cannot be set independently. There exists a tradeoff between the optimal quantization noise performance and the exact location of the high-pass cut-off frequency.

3.5.4. ORTHONORMAL FORM

Orthonormal ladder filters, a state-space structure that is scaled for optimum dynamic range and less sensitive to component variations can be used for realizing high order arbitrary stable transfer functions [26].

Figure 3.18 shows the block diagram of a standard orthonormal ladder filter. While the coefficients in the feedback structure are used to realize the poles, the coefficients in the output summing stage are used to realize the zeros. A 3rd order orthonormal filter is drawn in Figure 3.19.

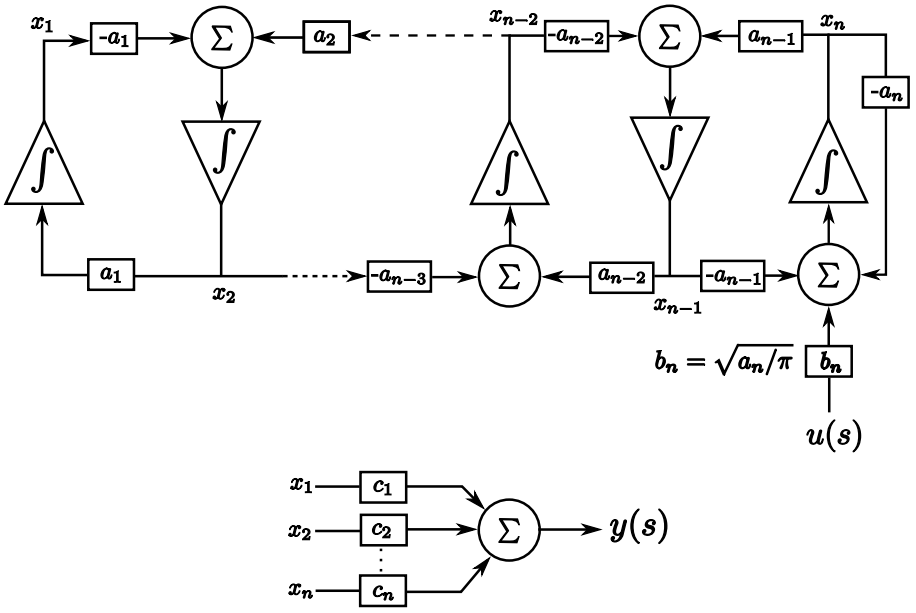


Figure 3.18: Block diagram of the nth order orthonormal ladder filter

The state-space description of the observable canonical form is given by

$$\mathbf{A} = \begin{bmatrix} 0 & a_1 & & \dots & & 0 \\ -a_1 & 0 & a_2 & \dots & & 0 \\ & -a_2 & 0 & a_3 & \dots & \\ \vdots & & \ddots & \ddots & \ddots & \vdots \\ 0 & & \dots & -a_{n-2} & 0 & a_{n-1} \\ 0 & & \dots & & a_{n-1} & a_n \end{bmatrix}; \quad \mathbf{b} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ \vdots \\ 0 \\ \sqrt{\frac{a_n}{\pi}} \end{bmatrix}; \quad \mathbf{c}^{\mathbf{T}} = [c_1 \quad c_2 \quad c_3 \quad \dots \quad c_{n-1} \quad c_n]; \quad d = 0 \tag{3.17}$$

In order to meet the STF requirement of the 2nd order orthonormal based HP ΔΣ ADC, the existing standard orthonormal form is modified by adding a feedback loop in order to introduce a zero in the STF, between the input of the first integrator and the output of the summing stage resulting in a structure as shown in Figure 3.20. Filtering can be done either in the analog, digital or mixed signal domain. An important point to note is the difference between the biquad and the orthonormal based HP ΔΣ converter structures. Although the structures look similar, the orthonormal structure has a unique set of coefficients while the biquad can have several different sets of coefficients that satisfy the transfer function requirements. Besides, the differences are clearly highlighted at higher order structures. Since

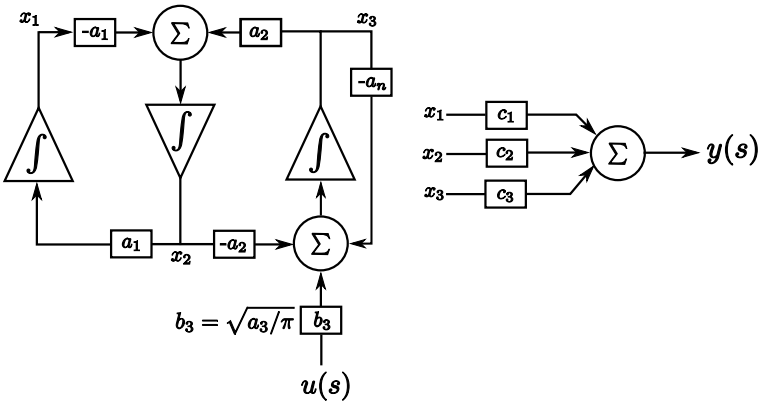


Figure 3.19: Block diagram of the 3rd order orthonormal form

the investigation is limited to 3rd order filters, the analysis of higher order structures is beyond the scope of this thesis.

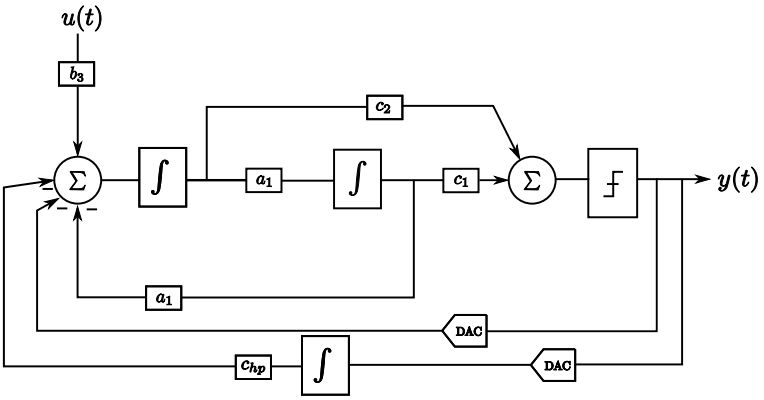


Figure 3.20: Orthonormal form based 2nd order ΔΣ ADC

The linear model of the orthonormal form based ΔΣ in s-domain is shown in Figure 3.21.

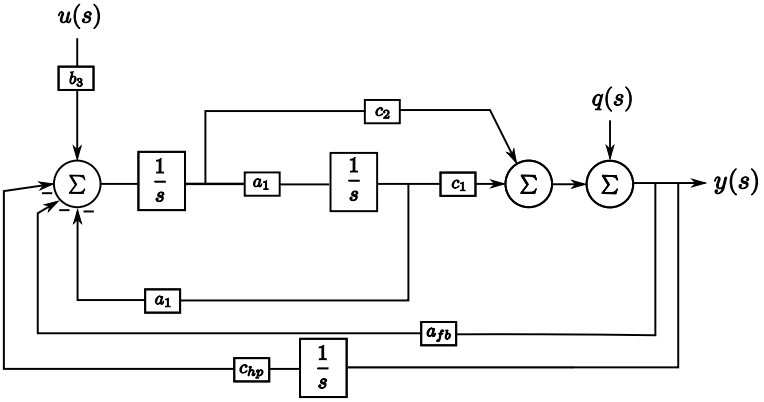


Figure 3.21: Linear model of orthonormal form based 2nd order ΔΣ ADC

The STF and the NTF equations can be written as

$$STF = \frac{sb_3k_2(c_2s + a_1k_1c_1)}{s^3 + k_2a_{fb}c_2s^2 + k_2k_1a_{fb}a_1s + k_1k_2k_3a_1c_1c_{hp}} \tag{3.18}$$

Table 3.2: Coefficients of the ΔΣ topologies

Coefficient	Orthonormal HP ΔΣ	Coefficient	Observable HP ΔΣ
a_1	1	p_1	0.5
b_3	0.5	p_2	0
c_1	1	q_1	1
c_2	2	q_2	2
c_{hp}	0.0005	q_0	0.0005

$$NTF = \frac{s(s^2 + a_1^2)}{s^3 + k_2 a_{fb} c_2 s^2 + k_2 k_1 a_{fb} a_1 s + k_1 k_2 k_3 a_1 c_1 c_{hp}} \tag{3.19}$$

For demonstration, the orthonormal and the observable based ΔΣ ADC topologies are modeled and analyzed on MATLAB. The coefficients of the topologies are given in Table 3.2. In order to have the NTF zeros of the orthonormal based HP ΔΣ topology at DC, the coefficient a_1, between the output of the 2^{nd} integrator and the input of the 1^{st} integrator is made zero.

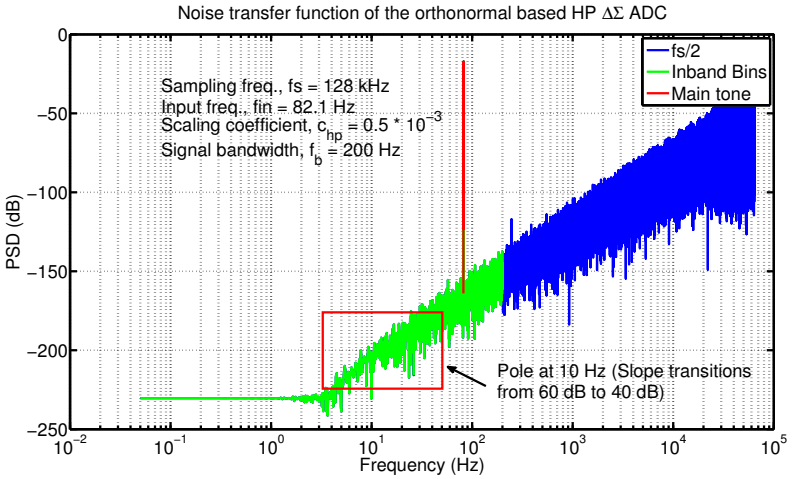


Figure 3.22: NTF of the orthonormal based HP ΔΣ topology

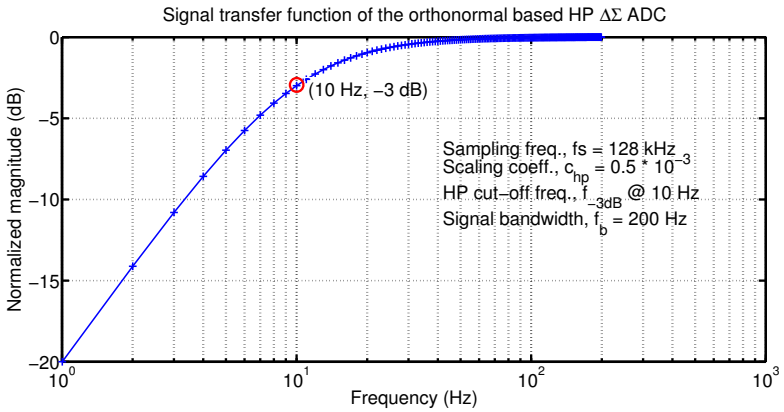


Figure 3.23: STF of the orthonormal based HP ΔΣ topology

Figure 3.22 and 3.23 show the NTF due to quantization noise (q-NTF) and the STF of an orthonormal form based HP ΔΣ modulator respectively. The NTF starts with 60 dB/decade slope due to the existence of three zeros at the origin. At the frequency of 10 Hz, the slope reduces to 40 dB/decade as it encounters a pole. The STF has a zero at the origin which satisfies the high-pass requirement and

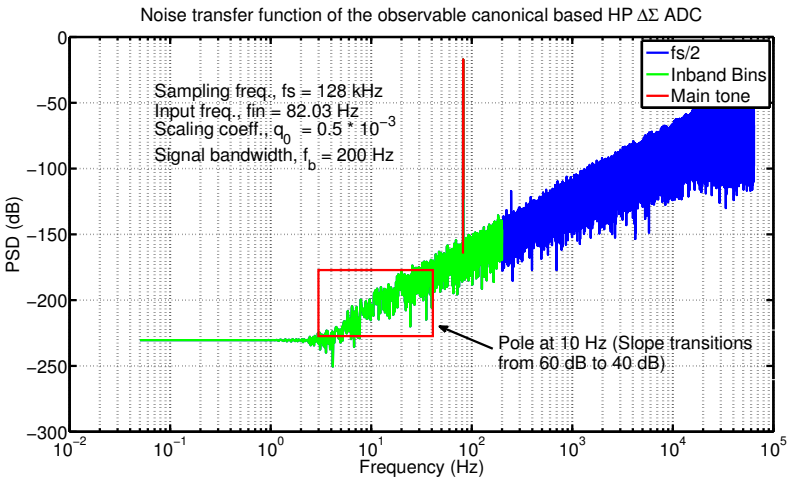


Figure 3.24: NTF of the observable based HP ΔΣ topology

starts with a slope of 20 dB/decade. The -3 dB point is given by the location of the first pole which determines the high-pass cut-off frequency of the signal band.

Figure 3.24 and 3.25 show the q-NTF and the STF of the observable canonical based HP ΔΣ modulator respectively.

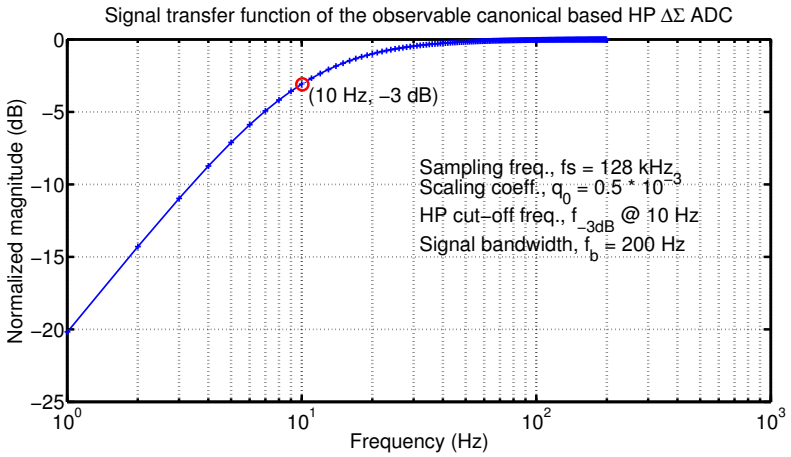


Figure 3.25: STF of the observable based HP ΔΣ topology

3.6. CONCLUSIONS

In this chapter, a methodology was proposed to develop state-space based HP ΔΣ topologies. The four resulting state-space based HP ΔΣ topologies are qualitatively evaluated. Although all the topologies meet the initial requirements, each of them differ in their properties. The interconnections between the integrators vary among different topologies that lead to varying noise performance and dynamic range.

A qualitative comparison of topologies is summarized in Table 3.3. From the table, it can be observed that only analog implementation of the high-pass integrator is possible with the controllable canonical based ΔΣ ADC. Furthermore, the coefficient responsible for setting the high-pass cut-off frequency also determines the location of the complex zeros of the NTF. Though the controllable canonical based ΔΣ satisfies the STF and NTF requirements mathematically, it is an inferior topology for the application in comparison to the others. The rest of the topologies offer the design freedom to set the coefficient

Table 3.3: State-space based HP ΔΣ topologies: A qualitative comparison

State-space	**Biquad**	**Observable canonical**	**Controllable Canonical**	**Orthonormal**
Disadvantage	Biquads in cascade can be used to realize higher order structures but may require modification for stability.	The output is fed back to the input of each of the integrators which imposes tough swing requirements on the integrator.	The zeros of the NTF are given by $s^3 + q_0 = 0$, where q_0 also determines the location of the HP pole; Pole location cannot be independently set.	Existing orthonormal state-space form had to be modified in order to satisfy the STF requirement.
Advantage	Each biquad can be tuned independently while imposing relaxed swing requirements on the integrators.	Only real NTF zeros can be produced while the rest of the topologies offer the freedom to choose between real and complex set of zeros.	The integrator outputs are summed at the output thereby, relaxing the swing requirements of the integrators.	Unique set of coefficients can be derived for any given stable transfer function. The calculation of the coefficients can be automated.
Filtering	Filtering can be done either in analog/digital/mixed signal domain.	Filtering can be done either in analog/digital/mixed signal domain.	Filtering can be done only in the analog domain.	Filtering can be done either in analog/digital/mixed signal domain.

responsible for the HP cut-off independently and will be evaluated in the following chapter.

4

Dynamic range optimization of high-pass ΔΣ ADCs

In this chapter, the HP ΔΣ topologies that were developed in Chapter 3 will be compared in terms of the total noise contribution of the integrators. Transfer functions from the input of the system to the output of the integrators and input of the integrators to the output of the system called the intermediate functions (IF's) will be used to evaluate the topologies. In Section 4.1, the intermediate functions are derived. The integrator noise sources of the topologies are modeled and the frequency response of the thermal noise transfer functions of the HP ΔΣ are qualitatively analyzed. In Section 4.2, the quantitative measures to evaluate the IF's with respect to the input are described. It is followed by Section 4.3 where the L_2-norm of the IF's are obtained after scaling and can be used to compare the dynamic range of the HP ΔΣ ADC topologies. Finally, the main conclusions of the chapter are summarized in Section 4.4.

4.1. Intermediate Functions

The Laplace domain equivalent of the state-space formulation of the dynamic system in time-domain as described in Section 3.5 is given by

$$s\mathbf{x}(s) = \mathbf{A}\mathbf{x}(s) + \mathbf{b}u(s) \tag{4.1}$$

$$y(s) = \mathbf{c}^{\mathbf{T}}\mathbf{x}(s) + du(s) \tag{4.2}$$

where the vector $\mathbf{x}(s)$ represents the integrator output states, the vector $\mathbf{A}$ represents the interconnection coefficients among the n integrators, the vector $\mathbf{b}$ contains the coefficients that scale $u(s)$ as applied to the integrator inputs , $\mathbf{c}$ contains the coefficients that multiply by the integrator outputs to form the output $y(s)$ and d is a scalar coefficient that contributes to the output directly from the input.

After rearranging the terms in Equation 4.1, we get

$$\mathbf{x}(s) = (s\mathbf{I} - \mathbf{A})^{-1}\mathbf{b}u(s) \tag{4.3}$$

Dividing the right hand side (RHS) and the left hand side (LHS) of Equation 4.1 by $u(s)$, we obtain,

$$\frac{\mathbf{x}(s)}{u(s)} = (s\mathbf{I} - \mathbf{A})^{-1}\mathbf{b} \tag{4.4}$$

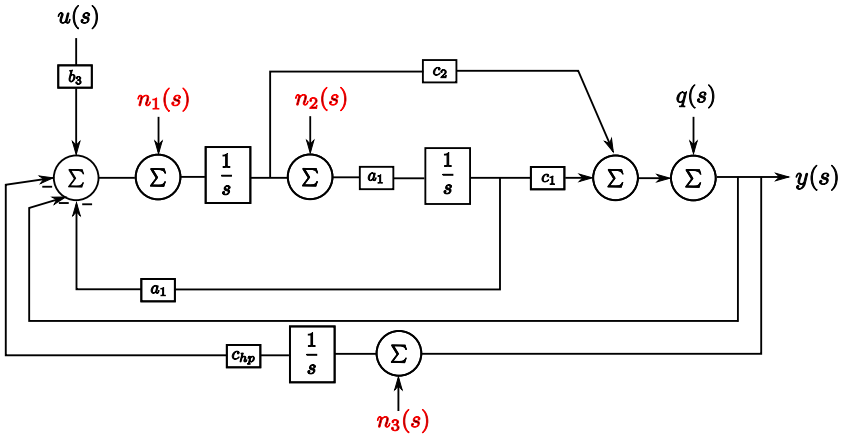


Figure 4.1: Thermal noise sources in orthonormal HP ΔΣ ADC

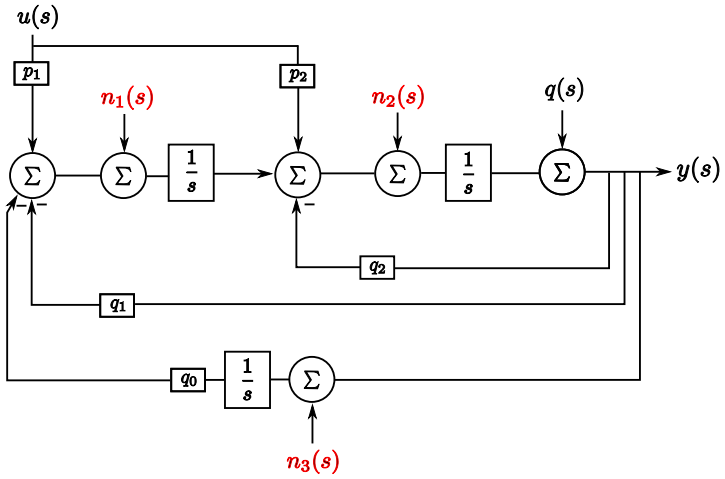


Figure 4.2: Thermal noise sources in observable HP ΔΣ ADC

The transfer function obtained from Equation 4.2 and 4.4 is given by

$$h(s) \triangleq \frac{y(s)}{u(s)} = \mathbf{c}^{\mathbf{T}}(s\mathbf{I} - \mathbf{A})^{-1}\mathbf{b} + d \tag{4.5}$$

A 3rd order system consisting of a 2nd order ΔΣ modulator and a 1st order HP loop is analyzed here but can be extended to a higher order modulator as well. For simplicity and for the purpose of illustrating the application of the developed method, a 3rd order system is considered sufficient for the analysis. For a 2nd order modulator, the topologies of orthonormal and biquad based HP ΔΣ are similar, but differ in their coefficients. At higher orders, the biquad based ΔΣ modulator resulting from a cascade of biquads would require modifications for achieving a stable system [27]. In this chapter, the performance of the orthonormal HP ΔΣ and the observable HP ΔΣ are evaluated and compared.

In order to study the noise performance of the topologies, the set of intermediate functions $\mathbf{g}(s)$, defined as the transfer function from the input of the integrators to the system output is derived. Let the noise sources at the input of the first, second and the third integrators as shown in Figures 4.1 and 4.2 be denoted by $n_1(s)$, $n_2(s)$ and $n_3(s)$ respectively. Let the output of the first, second and the third integrator be denoted by $x_1(s)$, $x_2(s)$ and $x_3(s)$ respectively. The input and the output of the system is given by $u(s)$ and $y(s)$ respectively. In order to estimate the contributions of each of the integrators, we derive the transfer function equations of $y(s)$ with respect to each of the noise input sources.

From 4.4, the set of intermediate functions $\{f_i(s)\}$ defined as the transfer function from the input of the system to the integrator outputs is given by

$$f_i(s) \triangleq \frac{x_i(s)}{u(s)}$$

and the vector $\mathbf{f}(s)$ is given by

$$\mathbf{f}(s) = (s\mathbf{I} - \mathbf{A})^{-1}\mathbf{b} \tag{4.6}$$

With the signal input $u(s)$ and the direct feedthrough coefficient d made zero, from 4.1, 4.2, rearranging the terms and substituting for $x(s)$, the set of intermediate functions $\{g_i(s)\}$ is given by

$$g_i(s) \triangleq \frac{y(s)}{n_i(s)}$$

and the vector $\mathbf{g}(s)$ is given by

$$\mathbf{g}^{\mathbf{T}}(s) = \mathbf{c}^{\mathbf{T}}(s\mathbf{I} - \mathbf{A})^{-1} \tag{4.7}$$

The IF's of the orthonormal and the observable HP $\Delta\Sigma$ modulators are derived in the following subsections.

4.1.1. ORTHONORMAL HP $\Delta\Sigma$ MODULATOR

The IF $\mathbf{f}(s)$ of the orthonormal HP $\Delta\Sigma$ modulator consists of a set of functions $\{f_1(s), f_2(s), f_3(s)\}$ given by

$$f_1(s) = \frac{x_1(s)}{u(s)} = \frac{k_1 b_1 s^2}{s^3 + k_1 c_2 a_{fb} s^2 + (k_1 a_{21} a_{fb} c_1 + k_1 k_3 c_{hp} c_2)s + c_{hp} a_{21} c_1 k_1 k_3} \tag{4.8}$$

$$f_2(s) = \frac{x_2(s)}{u(s)} = \frac{k_1 a_{21} b_1 s}{s^3 + k_1 c_2 a_{fb} s^2 + (k_1 a_{21} a_{fb} c_1 + k_1 k_3 c_{hp} c_2)s + k_1 k_3 c_{hp} a_{21} c_1} \tag{4.9}$$

$$f_3(s) = \frac{x_2(s)}{u(s)} = \frac{k_1 k_3 b_1 (c_2 s + a_{21} c_1)}{s^3 + k_1 c_2 a_{fb} s^2 + (k_1 a_{21} a_{fb} c_1 + k_1 k_3 c_{hp} c_2)s + k_1 k_3 c_{hp} a_{21} c_1} \tag{4.10}$$

The IF $\mathbf{g}(s)$ of orthonormal HP $\Delta\Sigma$ modulator consists of a set of functions $\{g_1(s), g_2(s), g_3(s)\}$ given by

$$g_1(s) = \frac{y(s)}{n_1(s)} = \frac{k_1 (c_2 s + a_{21} c_1) s}{s^3 + k_1 a_{fb} c_2 s^2 + (k_1 a_{fb} a_{21} c_1 + k_1 k_3 c_{hp} c_2)s + k_1 k_3 c_{hp} a_{21} c_1} \tag{4.11}$$

$$g_2(s) = \frac{y(s)}{n_2(s)} = \frac{c_1 a_{21} s^2}{s^3 + k_1 a_{fb} c_2 s^2 + (k_1 a_{fb} a_{21} c_1 + k_1 k_3 c_{hp} c_2)s + k_1 k_3 c_{hp} a_{21} c_1} \tag{4.12}$$

$$g_3(s) = \frac{y(s)}{n_3(s)} = \frac{k_1 k_3 c_{hp} (c_2 s + a_{21} c_1)}{s^3 + k_1 a_{fb} c_2 s^2 + (k_1 a_{fb} a_{21} c_1 + k_1 k_3 c_{hp} c_2)s + k_1 k_3 c_{hp} a_{21} c_1} \tag{4.13}$$

With respect to the noise input sources n_1,n_2 and n_3, the transfer function to the output is given by Equation 4.11 - 4.13. The values of the coefficients of the orthonormal HP $\Delta\Sigma$ topology are given in Table 3.2. Apart from that, the values of the integrator scaling coefficients given by k_1, k_2 and k_3 and the coefficient a_{fb} is unity. From the linear model, Figure 4.3 shows the frequency responses of the thermal noise transfer functions (from linear model). From MATLAB simulations, as shown in Figure 4.4 - 4.6 ,the noise of the first and second integrator is shaped by first order and second order high pass transfer function respectively whereas, the noise of the feedback integrator is low pass filtered. The slope of the thermal noise transfer changes as it encounters the first pole. Figure 4.6 shows the superposition of the noise from the feedback integrator and the quantization noise.

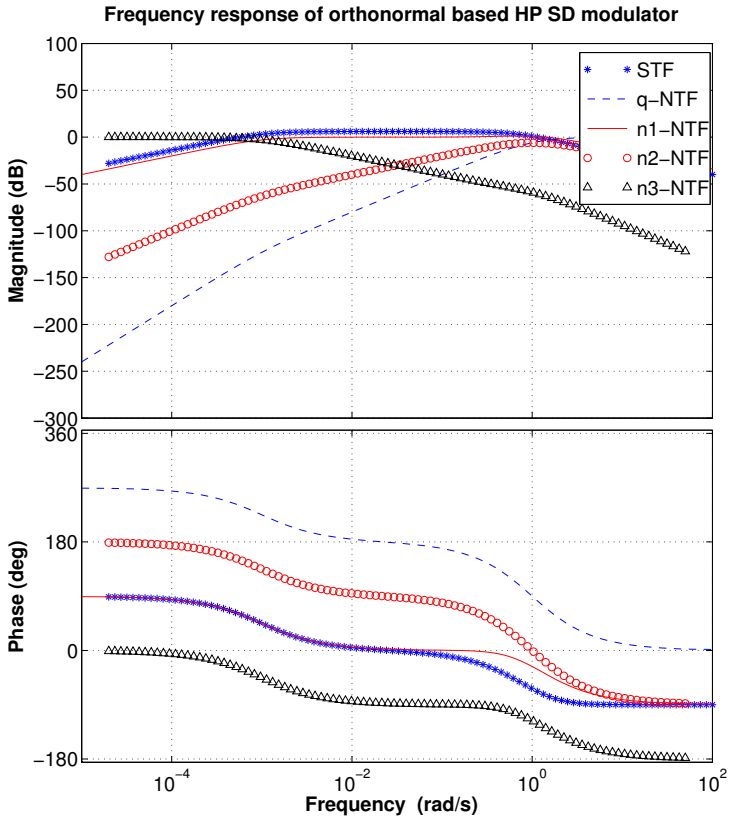


Figure 4.3: Frequency responses of the thermal noise transfer functions of the orthonormal HP ΔΣ topology

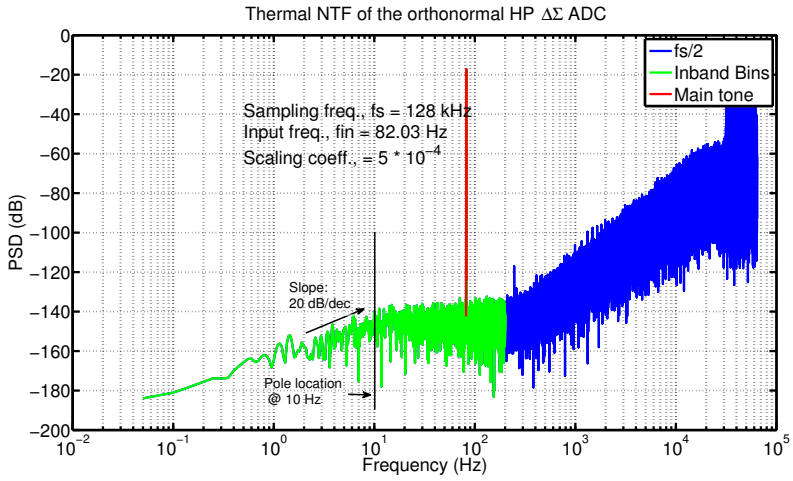


Figure 4.4: Intermediate function g_1 of orthonormal HP ΔΣ modulator

4.1.2. OBSERVABLE CANONICAL HP ΔΣ MODULATOR

The IF $\mathbf{f}(s)$ of the observable HP ΔΣ modulator consists of a set of functions $\{f_1(s), f_2(s), f_3(s)\}$ given by

$$f_1(s) = \frac{x_1(s)}{u(s)} = \frac{k_1 p_1 s(s + k_2 q_2)}{s^3 + k_2 q_2 s^2 + k_1 k_2 q_1 s + k_1 k_2 k_3 q_0} \tag{4.14}$$

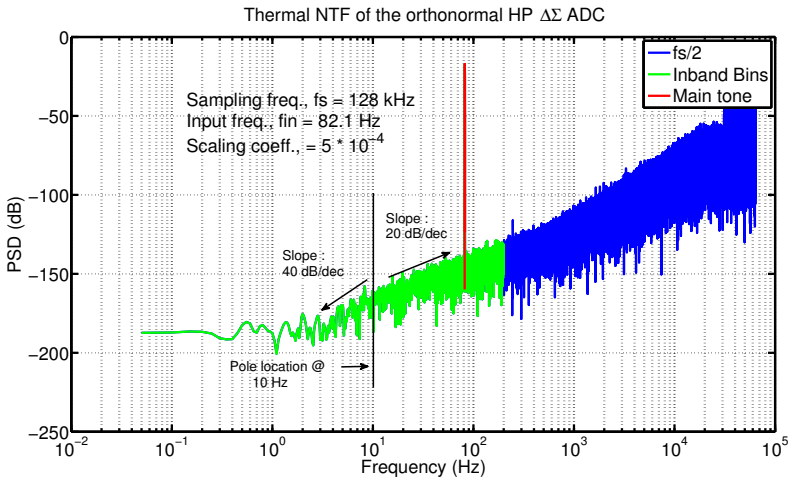


Figure 4.5: Intermediate function g_2 of orthonormal HP ΔΣ modulator

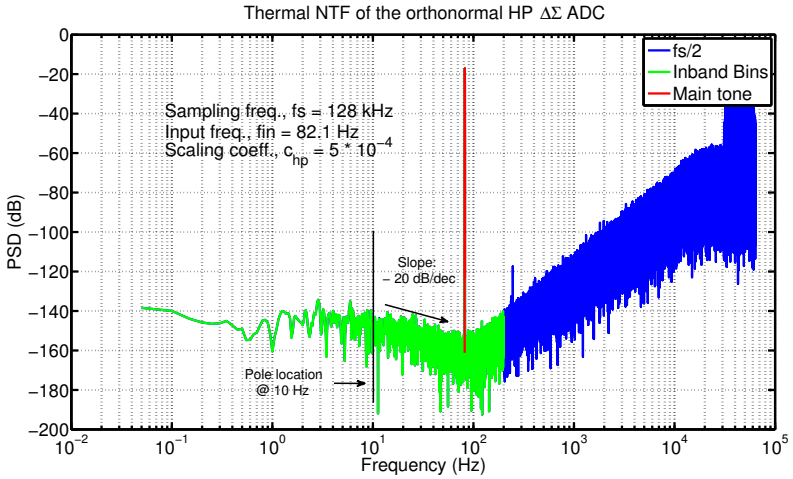


Figure 4.6: Intermediate function g_3 of orthonormal HP ΔΣ modulator

$$f_2(s) = \frac{x_1(s)}{u(s)} = \frac{k_1 k_2 p_1 s}{s^3 + k_2 q_2 s^2 + k_1 k_2 q_1 s + k_1 k_2 k_3 q_0} \tag{4.15}$$

$$f_3(s) = \frac{x_3(s)}{u(s)} = \frac{k_1 k_2 k_3 p_1}{s^3 + k_2 q_2 s^2 + k_1 k_2 q_1 s + k_1 k_2 k_3 q_0} \tag{4.16}$$

The IF $\mathbf{g}(s)$ of the observable HP ΔΣ modulator consists of a set of functions $\{g_1(s), g_2(s), g_3(s)\}$ given by

$$g_1(s) = \frac{y(s)}{n_1(s)} = \frac{k_1 k_2 s}{s^3 + k_2 q_2 s^2 + k_1 k_2 q_1 s + k_1 k_2 k_3 q_0} \tag{4.17}$$

$$g_2(s) = \frac{y(s)}{n_2(s)} = \frac{k_2 s^2}{s^3 + k_2 q_2 s^2 + k_1 k_2 q_1 s + k_1 k_2 k_3 q_0} \tag{4.18}$$

$$g_3(s) = \frac{y(s)}{n_3(s)} = -\frac{k_1 k_2 k_3 q_0}{s^3 + k_2 q_2 s^2 + k_1 k_2 q_1 s + k_1 k_2 k_3 q_0} \tag{4.19}$$

The thermal noise transfer function equations for the observable canonical based HP ΔΣ modulator is given by Equation 4.17 - 4.19. As was the case with orthonormal form based HP ΔΣ topology, the noise due to first and second integrator has first and second order high pass transfer function shaping, whereas for the feedback integrator, the noise is low pass filtered. Figures showing similar noise trend as shown in 4.11-4.13 are also obtained for the observable HP ΔΣ modulator.

Due to the noise source n_1, the noise shaping is 1^{st} order, which is similar to the shaping of the input signal. Since the noise of the feedback integrator is shaped by first order low pass characteristic,it contributes significantly to the total noise. It can be concluded that the noise from the 1^{st} integrator contributes to maximum noise. The second major contributor to noise is the feedback integrator which means that the care has to be taken to minimize noise from this feedback loop to ensure the desired noise floor. Therefore, the 1^{st} integrator and the feedback integrator need to fulfill the noise requirements of the entire ADC. It is interesting to note that, the noise introduced by the feedback integrator is relatively less significant as compared to a system that has a feedback structure such as this but does not introduce a pole close to DC. In such a case, the the noise will appear throughout the signal band and increase the noise floor. Therefore, the noise of such a feedback structure needs to be carefully designed to achieve the desired resolution.

4.2. MEASURES TO EVALUATE THE IF'S $\{f_i(s)\}$ AND $\{g_i(s)\}$

Quantitative evaluation of the performance of the ΔΣ modulators dictate the need for mathematical norm of the signals, which measures the magnitudes of signal levels at the output of the integrators and the system. The choice of the measure or norm depends strongly on the type of input signal and the application of the system. In the following subsections, these terms are defined and the different types are elaborated.

4.2.1. NORM OF A SIGNAL

Signal and system norms which give a mathematical measure of the magnitudes of the involved signals is necessary for quantitative evaluation of the performance of the system. A brief description of the system norms that are useful in performance evaluation is as follows.

The L_p norm of a signal $v(t)$ is defined as

$$\|v\|_p = \left(\int_0^\infty |v(t)|^p dt\right)^{1/p}, p \geq 1 \tag{4.20}$$

As an example, the L_2 norm of $v(t)$ is given by

$$\|v\|_2 = \left(\int_0^\infty |v(t)|^2 dt\right)^{1/2} \tag{4.21}$$

Another, often used norm is the L_∞-norm. The L_∞ norm of $v(t)$ is given by

$$\|v\|_\infty = \max_t |v(t)| \tag{4.22}$$

4.2.2. TYPES OF SIGNAL

Two important types of signal relevant to the application will be described here. They are

- Sinusoidal input: For a sinusoidal input with a peak amplitude A_p, an appropriate mathematical norm of the signal is the L_∞ norm.
- Power spectrum: If the input signal is assumed to be white, the output power spectrum at the output of the integrators is calculated and the root-mean-square value is given by the L_2 norm of the signal.

Table 4.1: Orthonormal HP ΔΣ topology

Signal/Noise gain	Before scaling		Scaling factor	After scaling	
	$f_i(j\omega)$	$g_i(j\omega)$	α_i	$f_i(j\omega)$	$g_i(j\omega)$
1st integrator	2.500312e-01	1.118062e+00	3.9995	1	2.795504e-01
2nd integrator	2.499063e-01	5.000624e-01	4.0015	1	1.249688e-01
HP integrator	1.581336e+01	1.581336e-02	0.0632	1	2.500625e-01

Table 4.2: Observable HP ΔΣ topology

Signal/Noise gain	Before scaling		Scaling factor	After scaling	
	$f_i(j\omega)$	$g_i(j\omega)$	α_i	$f_i(j\omega)$	$g_i(j\omega)$
1st integrator	5.590869e-01	5.000625e-01	1.7886	1	2.795784e-01
2nd integrator	2.500313e-01	5.000625e-01	3.9995	1	1.250313e-01
HP integrator	1.581337e+01	1.581337e-02	0.0632	1	2.500625e-01

4.3. DYNAMIC RANGE ANALYSIS

The dynamic range of the ΔΣ modulator is determined by the maximum signal and the minimum signal handling capabilities of the integrators. The interconnections between the integrators in the filter ie. the **A** and the **c** matrices are different for different topologies. Dynamic range is defined as the ratio of the largest and the smallest signals the system can handle determined by two limits

- Maximum processable signal as determined by distortion or amplifier saturation
- Minimum level as determined by internally generated noise

In order to optimize the dynamic range of the ΔΣ modulator, two approaches can be taken:

1. Optimize the dynamic range of the chosen topology through scaling of the integrators
2. Optimize the interconnects of a general state-space model to arrive at a fully optimized filter [28]

4.3.1. SCALING

In this thesis, scaling of integrators is carried out to optimize the dynamic range of the orthonormal and observable HP ΔΣ modulators. Scaling is the process of readjusting the internal gain coefficients in order to adjust the internal signal swing to a range appropriate to the supply voltage or the signal power at the output remains equivalent such that the overall transfer function from the input to the output remains unchanged [29].

The magnitude of the signal is scaled by the factor α_i which is determined by

$$\alpha_i = \frac{M}{\|f_i\|_2} \tag{4.23}$$

where M is the maximum acceptable signal magnitude at the integrator outputs.

After the set of intermediate functions given by the vector $\mathbf{f}(s)$ are appropriately scaled, the vector $\mathbf{g}(s)$ is scaled by the inverse factors $(\frac{1}{\alpha_i})$. The total noise power of the all the integrators given by $\sum_i \|g(j\omega)\|_2^2$ can be evaluated and used as a figure of merit [30] for comparing the noise performance of the HP ΔΣ topologies.

The noise gain of the integrators after scaling of the two topologies are summarized in Table 4.1 and 4.2.

Table 4.3: Noise power

Topology	**Total noise power** $\sum_{i=1}^{3} \|g_i(j\omega)\|_2^2$
Orthonormal	0.15629688
Observable	0.15632816

4.4. CONCLUSIONS

In this chapter, scaling is done to optimize the dynamic range of the topologies. Noise gain $\mathbf{g}(s)$ and signal gain $\mathbf{f}(s)$ of the individual integrators are calculated. Two important conclusions can be drawn from this evaluation. Firstly, the total noise power of the orthonormal HP ΔΣ topology is slightly lower than the observable canonical HP ΔΣ topology as shown in Table 4.3. Therefore, the orthonormal form HP ΔΣ topology is a better structure.

Secondly, it was observed from the frequency response of the thermal noise transfer functions and the noise calculations that the first integrator and the feedback integrator both contribute significantly to the total noise power immaterial of the topology chosen as can be seen from the noise shaping. Therefore, when feedback loops are implemented in any system, it has to be carefully designed such that the noise is minimized.

5

Design choices for the implementation of orthonormal high-pass ΔΣ ADC

In the previous chapters, a method was proposed to develop high-pass ΔΣ (HP ΔΣ) topologies for the acquisition of ECG signals and based on the dynamic range calculations, the orthonormal HP-ΔΣ was chosen for implementation. For the actual realization of the modulator, design considerations pertaining to the block level implementation of the ADC will be described in this chapter. Design choices are made after comparison at the block level for a suitable implementation of the modulator. In Section 5.1, the integrator non-idealities are investigated which are necessary for gaining system level insight and also set the minimum integrator requirements. It is followed by Section 5.2 where the choice of DAC type is made and conclusions are summarized in Section 5.3.

The loop filters can either be implemented in the continuous-time (CT) or discrete-time (DT) domain. CT filters can be implemented using g_m-C or opamp-RC techniques whereas the DT filters can be implemented using switched-capacitor circuits. Although DT implementation is preferable with respect to accuracy of the gain and linearity of the integrators, high sampling and settling requirements make it less favorable as compared to its CT counterpart. The continuous and discrete-time implementations are compared and the benefits and limitation of each are summarized in Table 5.1. With respect to the application, a CT implementation is chosen. Due to the requirement of high linearity, a single bit quantizer is chosen and a comparison between multi-bit and single-bit is summarized in Table 5.2.

While 1^{st} order modulators are shown to be stable unconditionally, it requires a large OSR and hence larger power consumption, to achieve the target ENOB. Satisfying the constraint of using a single quantizer according to the set of constraints set in Chapter 4, a single loop modulator is chosen. From the Equation 5.1, a 2^{nd} order orthonormal ΔΣ ADC can achieve the desired resolution of 12 bits. For single loop modulators, a modulator order greater than 2 has a tendency towards instability [23]. Although 64 kHz would have been sufficient to suppress the quantization noise such that it can be neglected, it would result in extremely large R and C values in case of opamp RC or ultra low g_m values

Table 5.1: Continuous Time vs Discrete Time implementation

	CT integrator	**DT integrator**
Benefits	Implicit anti-aliasing filter (AAF)	Good linearity
	Relaxed sampling and settling requirements	Good accuracy
	Low power consumption	Robustness to process variations
Limitations	Prone to integrator non-idealities	Need for a dedicated AAF
	Prone to jitter and excess loop delay	Higher power consumption

Table 5.2: Multibit vs single bit quantizer

Multi bit DAC	**1-bit DAC**
Higher SNR for lower OSR	High SNR for medium OSR
Greater stability for high order	Poor stability for high order
Degraded linearity	Inherently linear
Complex linearization techniques	Can be avoided

Table 5.3: Summary of the orthonormal HP ΔΣ ADC

ADC specification of orthonormal HP ΔΣ ADC	
Signal bandwidth	200 Hz
Order of the modulator	2
Order of the system	3
Oversampling ratio	320
Sampling frequency	128 kHz

in case of g_m- C implementation. Larger C values would also require larger current to drive them to minimize the effect of finite slew rate. The inband noise (IBN) due to quantization [31] is given by the Equation 5.1

$$IBN = \frac{\Delta^2}{12} \frac{\pi^{2N}}{(2N+1)OSR^{2N+1}} \tag{5.1}$$

where Δ is the step size , OSR is the oversampling ratio and N is the order of the modulator.

After taking all of the previously mentioned issues into consideration, the sampling frequency is set at 128 kHz. The ADC specification is summarized in Table 5.3. To limit the output swing of the integrators, scaling coefficients are introduced to contain the swing well within the supply voltage limits. The coefficients of the orthonormal ΔΣ topology and the integrator scaling constants are given in Table 5.4.

5.1. INTEGRATOR IMPLEMENTATION

For the continuous time integrator implementation, opamp-RC and g_m- C are both good candidates. The ideal integrator transfer function (ITF) of the opamp RC and the g_m- C integrator is given by

$$ITF_{RC,i} = \frac{k_i f_s}{s} = \frac{1}{sRC} = \frac{\omega_u}{s} \tag{5.2}$$

$$ITF_{\frac{gm}{C},i} = \frac{k_i f_s}{s} = \frac{g_m}{sC} = \frac{\omega_u}{s} \tag{5.3}$$

Table 5.4: Coefficient values of the orthonormal HP ΔΣ ADC

Coefficient	**Value**
b_1	0.5
a_{fb}	1
c_1	1
c_2	1
k_1	0.5
a_{21}	0.5
c_{hp}	$50 \cdot 10^{-6}$

Table 5.5: g_m- C vs opamp RC integrators

Performance criteria	opamp RC	g_m- C
Linearity	+ + +	+
Tunability	+	+ + +
Dynamic range	+ + +	+ +
Power consumption	+	+ + +

where k_i is the integrator coefficient of the i^{th} integrator, f_s is the sampling frequency and ω_u is the unity gain frequency in radians. The unity gain frequency (in Hz) is given by

$$f_u = \frac{k_i f_s}{2\pi} \tag{5.4}$$

Table 5.5 lists out the benefits and limitations of the two implementations [23]. Due to the use of resistances, the distortion in the opamp-RC is inversely proportional to the harmonic distortion which makes it a better candidate for integrator implementation if good linearity is desired [32]. Based on the comparison presented in Table 5.5, due to better linearity and dynamic range opamp RC is chosen. Also opamp-RC is less sensitive to parasitics as compared to gm-C. Tunability is not a huge concern as it can be implemented using a tunable capacitive array without the need for tunable g_m's. The design of the first integrator is crucial as it is sets the performance of the ADC. In addition to that, the noise due to the high pass integrator can also the limit the overall performance as it was observed in Section 4.1 in Chapter 4. Therefore, both first and the HP integrator need to meet the minimum requirement of the integrator gain bandwidth and DC gain to suppress the errors due to the finite effects of integrator non idealities. In the next Section,the effect of these non idealities will be investigated qualitatively and quantitatively to satisfy minimum requirement to prevent degradation of the ADC performance.

5.1.1. EFFECT OF INTEGRATOR FINITE DC GAIN

Taking into the finite DC gain effect of the integrator into account, the non ideal ITF can be expressed as

$$ITF_{RC,A_0} = \frac{\frac{k_i f_s}{s}}{1 + \left(\frac{1 + \frac{k_i f_s}{s}}{A_0}\right)} = \frac{k_i f_s}{\frac{s(1+A)}{A} + \frac{k_i f_s}{A}} \tag{5.5}$$

By approximating $(1 + A) \approx A$, Equation 5.5 reduces to

$$ITF_{RC,A_0} \approx \frac{k_i f_s}{s + \frac{k_i f_s}{A_0}} \tag{5.6}$$

where A_0 is the finite DC gain of the integrator.

Comparing Equation 5.6 to the ideal transfer function 5.2, it is observed that the pole at the origin is displaced to $\frac{k_i f_s}{A_0}$. The finite DC gain is modeled as a leaky integrator and the performance of the ADC is observed as the DC gain is varied from 40 dB to 10 dB. As shown in Figure 5.1, a minimum DC gain of 80 dB for a sampling frequency of 128 kHz and an input frequency of 82.1 Hz, is required to prevent significant degradation in the overall performance of the modulator. The values of the coefficients of the modulator are given in Table 3.2.

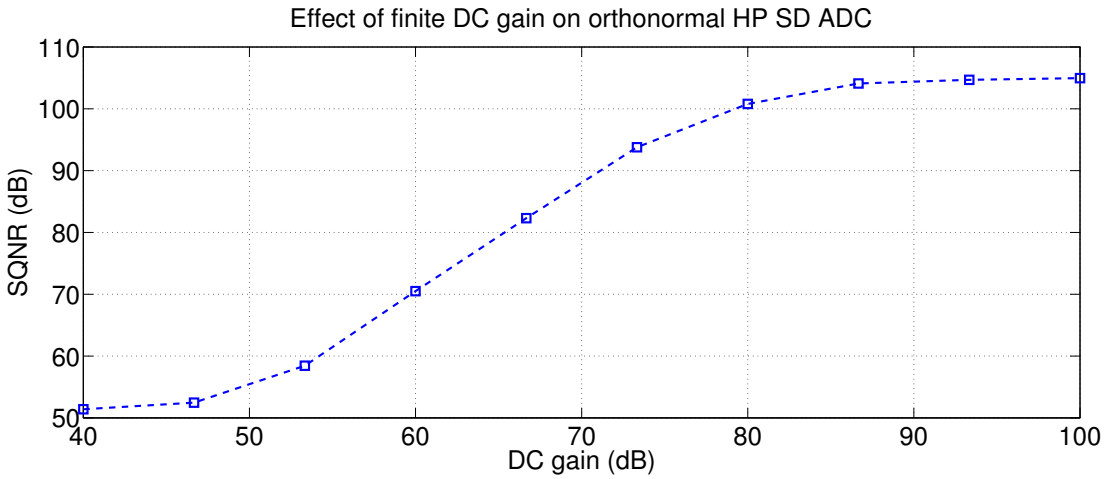


Figure 5.1: Simulated SNR vs finite DC gain

5.1.2. EFFECT OF INTEGRATOR FINITE GBW

In order to take the finite GBW of the integrator into account, A can be expressed in terms of frequency dependent gain and Equation 5.6 can be rewritten as

$$ITF_{RC,GBW} = \frac{\frac{k_i f_s}{s}}{s + \frac{k_i f_s}{A(s)}} \tag{5.7}$$

where A(s) is the frequency dependent gain and is expressed by

$$A(s) = \frac{A_0}{1 + \frac{s}{\omega_u}} \tag{5.8}$$

The unity gain bandwidth of the integrator, GBW is given by

$$GBW = A_0 \omega_u \tag{5.9}$$

Substituting Equation 5.8 and 5.9 in 5.7 and simplifying, we obtain,

$$ITF_{RC_{GBW,A_0}} = \frac{\frac{k_i f_s}{s} \frac{GBW}{GBW + k_i f_s}}{1 + \frac{s}{GBW + k_i f_s} + \frac{k_i f_s + s}{s(A_0 + 1)}} \tag{5.10}$$

Assuming that A_0 has a finite large value while meeting minimum DC gain requirements, the equation is simplified to

$$ITF_{RC_{GBW,A_0}} = \frac{\frac{k_i f_s}{s} \frac{GBW}{GBW + k_i f_s}}{1 + \frac{s}{GBW + k_i f_s}} \tag{5.11}$$

Comparing Equation 5.7 with 5.2, the impact of finite GBW is the presence of a gain error which is multiplied with the integrator time constant. The impact of the finite GBW on the performance of the modulator can be seen in Figure 5.2 where the SQNR varies with normalized GBW given by the factor c. It can be observed that a GBW of 0.6 times $2\pi f_s$ is sufficient to prevent degradation in the performance of the ADC as shown in Figure 5.2.

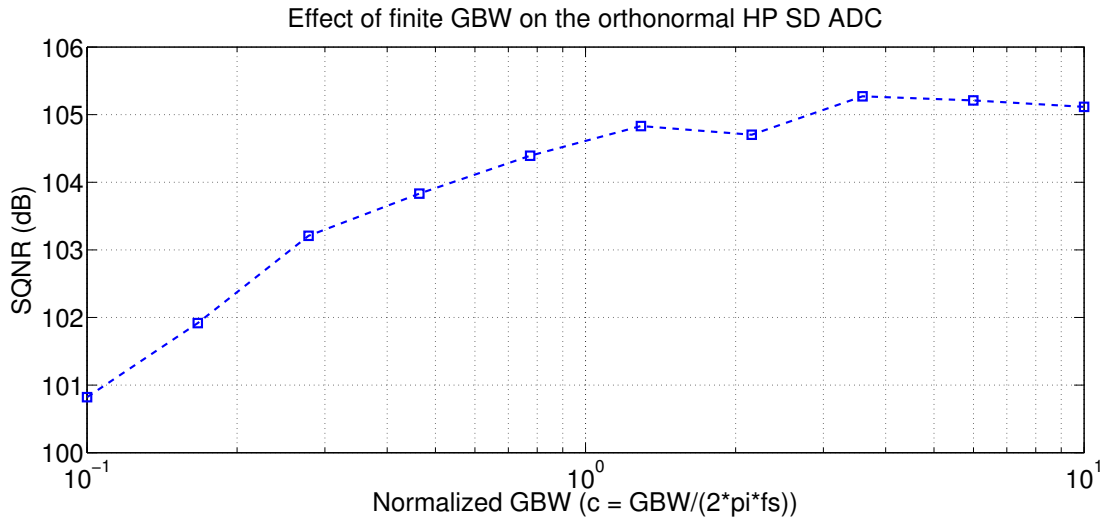


Figure 5.2: Simulated SNR vs finite GBW

5.1.3. EFFECT OF INTEGRATOR RC VARIATION

The integrator coefficient can vary due to process variations. The change in the time constant can be modeled as a gain error and the modified ITF can be written as

$$ITF_{RC,\Delta_{RC}} = \frac{1}{sRC} \cdot \frac{1}{(1+\Delta_{RC})} = \frac{k_i f_s}{s} \cdot \frac{1}{(1+\Delta_{RC})} \tag{5.12}$$

The time-constant is varied from −40% to +40%. From simulations, the effect of RC variation on the ADC performance can be seen in Figure 5.3. On negative variation, the coefficient increases and this leads to a slight decrease in the inband noise but leads to instability if reduced further. On positive variation of the time constant, the inband noise increases steadily and degrades the performance. To simulate the worst case scenario, the time constants of all the integrators are varied to the same extent. The SQNR decreases by 3 dB due to the variation in the time-constant. In actual practice, the values of resistor and capacitor varies independently and not necessarily suffer from the same amount of variation.

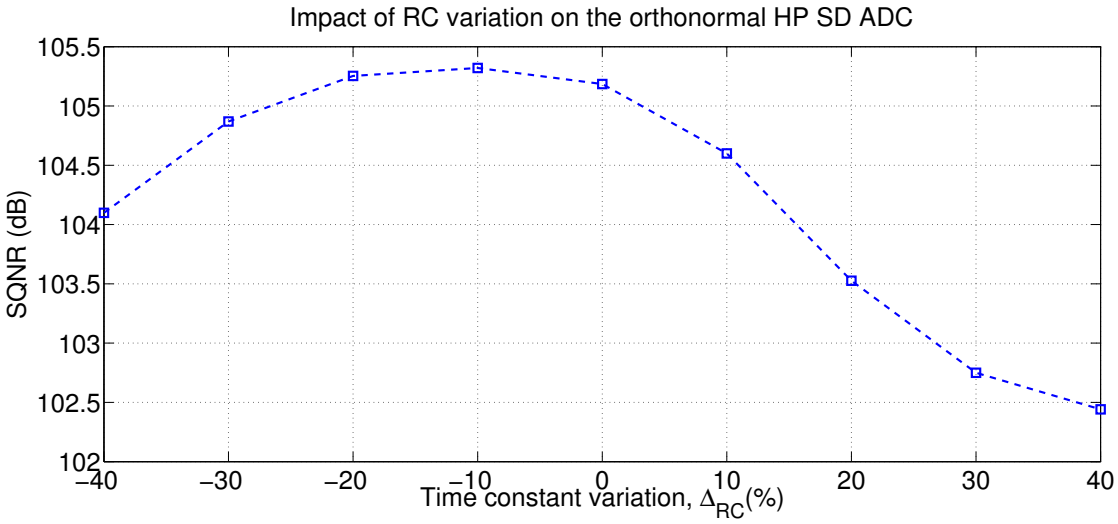


Figure 5.3: Simulated SNR vs RC variation

5.2. QUANTIZER AND DAC NON IDEALITIES

Although timing errors exist both in the CT and DT integrator implementations, it impacts the CT integrator more as the errors are continuously accumulated through the feedback loop. In this section, the impact of the temporal errors , i.e., clock jitter σ_j , and excess loop delay τ_d on the orthonormal HP ΔΣ will be investigated. Common DAC output waveforms include non return to zero (NRZ), return to zero (RZ) and half delayed RZ (HRZ) pulses as shown in Figure 5.4.

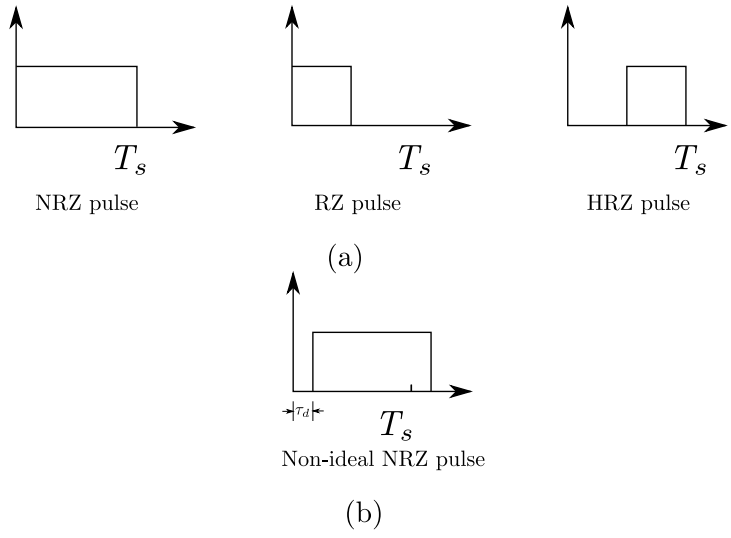


Figure 5.4: Commonly used DAC waveforms

5.2.1. EFFECT OF EXCESS LOOP DELAY

Excess loop delay refers to the constant delay in the feedback loop which arises due to the time delay between the quantizer clock pulse and the DAC pulse which is then the output of the quantizer. This delay can be expressed as

$$\tau_d = \rho_d T_s \tag{5.13}$$

where τ_d is the excess loop delay, T_s is the sampling time and ρ_d is parameter dependent on the transit frequency of the transistors in the technology f_T, sampling frequency f_s and the number of transistors in the feedback path n_t [33] and can be written as

$$\rho_d \approx \frac{n_t f_s}{f_T} \tag{5.14}$$

Finite excess loop delay disturbs the loop filter of the DT equivalent of the modulator and introduces second order effects making it unstable [33]. However, for biomedical applications, the sampling frequency used is usually low and particularly in this thesis the f_s is only 128 kHz. Thus, ρ_d amounts to a very small value. The operating frequency of the transistor in 0.18μm AMS technology is about 4 GHz. This means that τ_d amounts to a very small fraction of T_s and therefore the resulting error can be neglected. NRZ DAC is chosen for implementation due to the simple circuitry needed. Although NRZ waveform suffers from excess loop delay, it can be neglected.

5.2.2. EFFECT OF CLOCK JITTER

Clock jitter can be defined as random noise that adds to the modulator feedback signal and impacts the DAC waveform thereby increasing the noise floor and decreasing the effective resolution of the ADC. Since clock jitter affects the NRZ DAC based modulators less severely than the RZ or HRZ type [34],

Table 5.6: Summary of the circuit non-idealities and its impact on orthonormal HP ΔΣ ADC

Non-ideality	Impact on performance	Comment
Finite integrator DC gain	Increased noise floor	DC gain >80 dB
Finite integrator GBW	Increased noise floor and instability	Normalized factor, c >0.6
Integrator RC variation	Increased noise floor and instability	Use of tuning circuitry
Clock jitter	Increased noise floor	Can be neglected
Excess loop delay	Instability	Can be neglected

we will choose to implement an NRZ based DAC. Also clock jitter is more of an issue at much higher sampling frequencies [31] . For a sampling frequency of 128 kHz, the noise error due to clock jitter can be neglected.

Although CT implementation is prone to jitter and excess loop delay which can degrade the overall performance, as clearly seen in Section 5.2.2 and 5.2.1, its effect can be neglected for this analysis and design.

5.3. CONCLUSIONS

In this chapter, decisions with respect to block level implementation of the orthonormal HP ΔΣ ADC were made. The results of this chapter set the minimum requirements on the circuit specifications of the integrators. The integrator non idealities were modeled and simulated in MATLAB to study the impact on the performance of the orthonormal HP ΔΣ ADC. The effect of timing errors were also discussed. The minimum DC gain required is 80 dB. The minimum GBW required is $0.6 \cdot 2\pi \cdot f_s$. The effect of circuit non-idealities is summarized in Table 5.6. NRZ type is chosen for DAC implementation.

6

Circuit design of orthonormal high-pass ΔΣ modulator and Simulation results

The orthonormal high-pass ΔΣs are targeted at implementing a high-pass cut-off frequency for ECG signal bandwidth with good accuracy and linearity. In Chapter 5, circuit specifications for the circuit blocks were obtained through system level simulations which will be used in this chapter to realize the circuit blocks. Section 6.1 describes the top level circuit block diagram. In Section 6.2, the design of opamp used in the implementation of the integrator is described. In Section 6.3, the design of a 1-bit quantizer is described followed by Section 6.4 describing the design of DAC. In Section 6.5, the design of the fully-differential switched-capacitor very large time constant (SCVLT) Nagaraj integrator is described. Section 6.6 presents the simulation results of the designed system. The chapter concludes with Section 6.7 where the existing HP ΔΣ techniques are compared in terms of achievable accuracy and linearity of the HP cut-off frequency and the overall performance of the designed system is discussed.

6.1. Proposed architecture of orthonormal HP ΔΣ modulator

A simplified top level schematic of the proposed orthonormal HP ΔΣ ADC architecture is illustrated in Figure 6.1. For the signal bandwidth of 200 Hz, the sampling clock frequency is set at 128 kHz to achieve the desired resolution. The 2^{nd} order orthonormal HP ΔΣ has been implemented in 0.18 μm AMS technology.

Opamp-RC integrators are used to realize the first and the second integrator due to better linearity performance than the g_mC integrators as described in detail in Section 5.1. The integrator amplifiers are implemented using the two-stage opamp topology. Due to the requirement of large capacitance values, the amplifiers are designed with a high current driving capability to prevent performance degradation due to slewing. The second integrator specifications are much relaxed and are optimized with respect to power. The resistance and the capacitance values are calculated based on the scaling coefficients. A dual-input dynamic comparator is used as a summer and quantizer. This approach, as compared to a conventional adder, is less power consuming. A very large time-constant switched-capacitor integrator [35] is used to realize the HP integrator in the feedback loop.

Table 6.1 presents the values of the passive components used in the Figure 6.1. Although a sampling frequency of 64 kHz is sufficient to obtain the target resolution, a higher value needs to be chosen to keep the resistance and capacitance values of the integrators within reasonable limits. The relationship between sampling frequency, the integrator time constant, the resistance and capacitance is explained

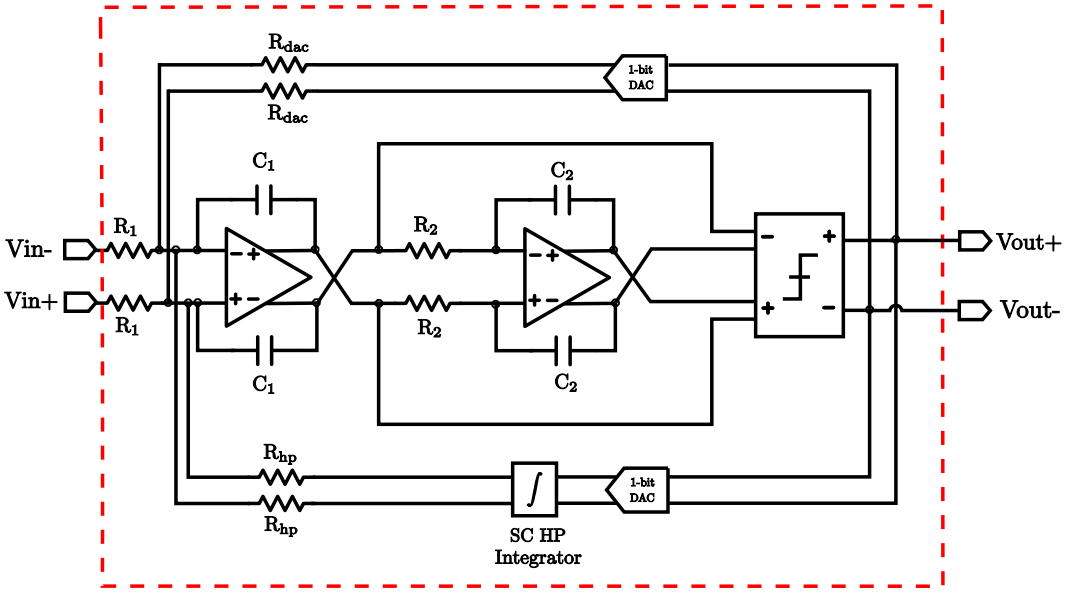


Figure 6.1: Simplified top level circuit block diagram of CT orthonormal HP ΔΣ modulator

Table 6.1: Passive components used in the orthonormal HP ΔΣ modulator

Passive components	Value
R_1	1 MΩ
R_2	2 MΩ
C_1	15 pF
C_2	7.5 pF
R_{dac}	1 MΩ
R_{hp}	1 MΩ

in Section 5.1. The sampling frequency cannot arbitrarily be made very high due to the requirement of extremely large capacitor ratios of the switched-capacitor high-pass integrator. Taking all these factors into consideration, the sampling frequency is set at 128 kHz.

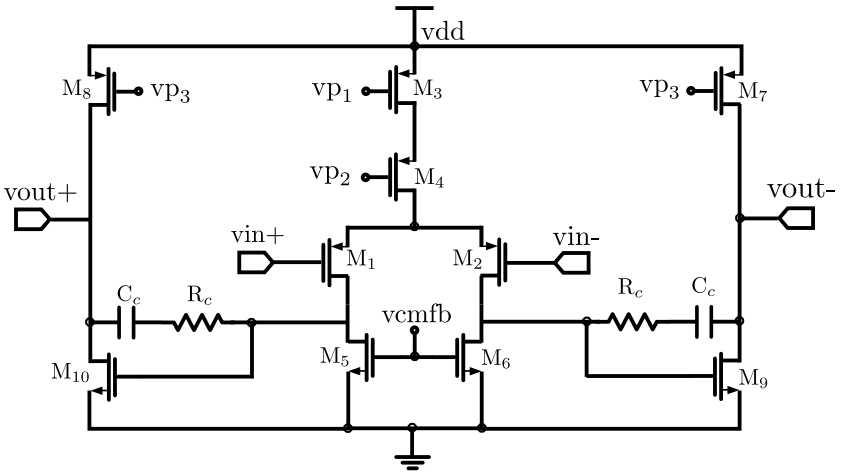
6.2. DESIGN OF FIRST INTEGRATOR

The operational amplifier implemented is a two-stage topology as shown in Figure 6.2a. The advantage of using a two-stage opamp is that the noise, gain and the swing requirements can be met separately. The first integrator is required be to designed for low noise and high gain. It should also meet the linearity specification for the entire modulator. The amplifier consists of a differential input for the first stage, a common source output for the second stage and a common mode feedback (CMFB) circuit. Large PMOS input transistors M_{1-2} are used to minimize flicker noise. The common source stage is chosen to obtain maximum signal swing. The opamp is Miller compensated using capacitor C_c. A resistor R_c is placed in series with C_c to cancel the right half plane zero that is introduced by the compensation capacitor. The value of of R_c is chosen such that the zero introduced by g_{m9} is canceled according [36] to the equation

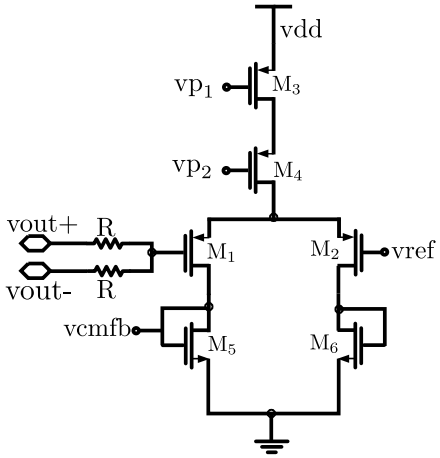
$$\omega_z \approx \frac{1}{C_c(g_{m9}^{-1} - R_c)} \tag{6.1}$$

The CMFB block is shown in Figure 6.2b. Vref is set at 0.9 V.

The open loop gain of the amplifier is more than 85 dB with a phase margin higher than 60 degrees as set by system simulations in Chapter 5. The magnitude and phase plot are shown in Figures 6.3a and



(a) Two-stage opamp

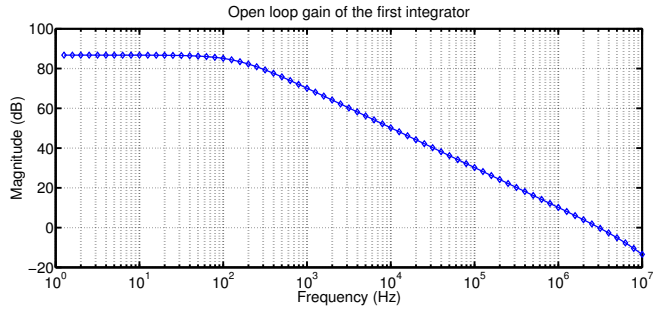


(b) CMFB block

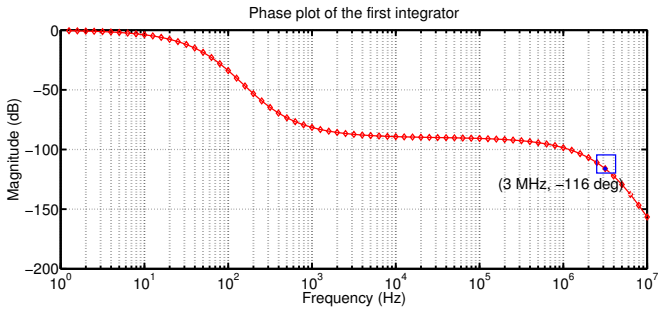
Figure 6.2: Schematic of first integrator

Table 6.2: Design parameters of the first integrator

Component	**Value**
R_c	1 kΩ
C_c	2 pF
V_{ref}	0.9 V
Transistor	**W/L(μm)**
M_{1-2}	200/2
M_3	20/1
M_4	10/2
M_{5-6}	30/1
M_{7-8}	100/1
M_{9-10}	100/1



(a) Open loop gain of the amplifier



(b) Phase plot of the amplifier

Figure 6.3: Bode plot of the 1st integrator

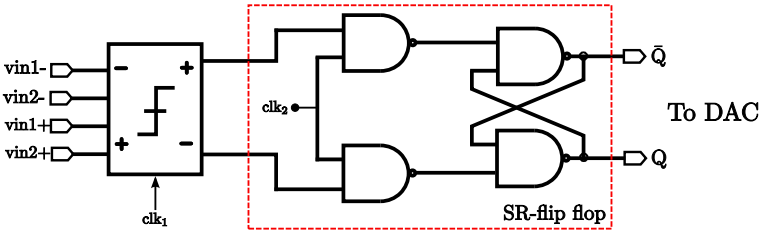
6.3b. This ensures that the effect of integrator non-idealities on the performance of the modulator is minimized.

The second integrator is also a two-stage topology but optimized with respect to power. Errors due to non-idealities of the integrator and noise is suppressed when referred to the input of the modulator. Therefore, the requirements of the integrator are more relaxed. Since the second integrator has to drive only half of the capacitive load as compared to the first, the current in the second stage is reduced. Also, the impact of finite slew rate of the second integrator is suppressed by the first integrator. The compensation capacitor is set to 1.5 pF. The current consumption of the first and the second stage is 0.18 μA and 1.5 μA respectively.

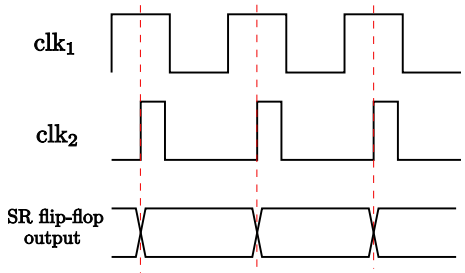
6.3. DESIGN OF 1-BIT QUANTIZER

The 1-bit quantizer consists of a comparator and an SR - flip flop. A comparator converts the difference between the inputs to a digital output. A latch connected after the comparator is enabled by a slightly delayed clock signal that synchronizes the outputs of the comparator. Figure 6.4 shows the comparator and the SR-flip flop along with the timing diagrams.

A latched comparator is used since it uses positive feedback to reduce the decision time. A reset clock phase is needed to clear the data after each decision. Among the existing latched comparators, such as the static latched comparators, Class AB - latched comparators and dynamic latched comparators, a selection can be made after comparing them in terms of power consumption, speed and kickback noise. The large voltage variations in the internal nodes which are coupled to the input of the comparator, disturbing the input voltage, is referred to as the kickback noise [37]. In case of static latched comparators, the kickback noise is low, but it consumes static power with slow regeneration. class-AB latched comparators are faster and consume less power than static counterparts, but higher kickback noise is generated. Dynamic latched comparators present the lowest power consumption since the current flows only during the regeneration phase whereas the class-AB comparators have current flowing in the regeneration and the reset phase. Although the dynamic comparators are the fastest and least power consuming comparators, they also generate more kickback noise. Offset of the comparators is suppressed by the loop gain of the modulator and therefore, is not a huge concern. In this thesis, a



(a) Block diagram of the 1-bit comparator and the SR-flip flop



(b) Timing waveform

Figure 6.4: Block diagram of the quantizer with the clock timing waveform

dynamic latched comparator is chosen for low power consumption.

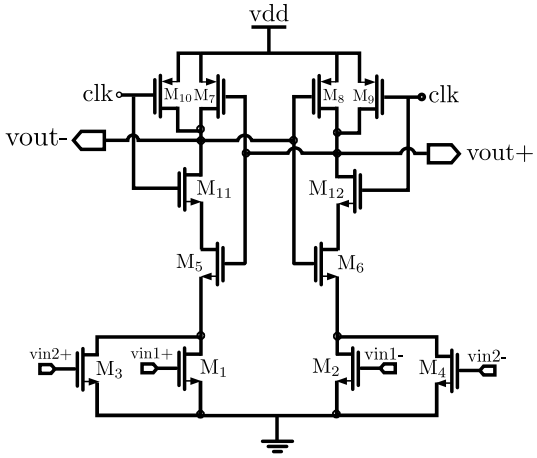


Figure 6.5: Comparator

Figure 6.5 shows the architecture of the dynamic latched comparator. It is implemented as a quadruple-input dynamic comparator that incorporates both the coefficients, c_1 and c_2, and the summing of the coefficients, thus saving both power and area. The circuit operates in two phases

- Reset phase
  When the clock signal is low, transistors M_{9-10} and M_{11-12} are ON and the output nodes are charged to supply voltage in each cycle.
- Evaluation phase
  When the clock signal is high, a voltage difference between the inputs of the comparator causes the current in one of the branches to increase, causing the gate-source voltage of the PMOS transistor to increase. The cross coupled inverters drive one of the output nodes low while the other goes high.

The transistor parameters of the dynamic comparator are given in Table 6.3. The clocked SR-flip flop as shown in Figure 6.4a serves two purposes. During the reset phase, when both the comparator outputs are charged to vdd, the SR flip flop holds the previous decision of the comparator in each cycle. It

Table 6.3: Parameters of the dynamic comparator

Transistor	W/L (um)
M_{1-2}	2/0.36
M_{3-4}	2/0.36
M_{5-6}	0.5/0.18
M_{7-10}	1/0.18
M_{11-12}	0.5/0.18

Table 6.4: SR-flip flop truth table

clk_2	S	R	Q
0	X	X	HOLD
1	0	0	HOLD
1	0	1	0
1	1	0	1
1	1	1	-

also synchronizes the output of the comparator. Table 6.4 presents the truth table of the SR-flip flop. When the clock enable is low, the latch is in HOLD phase. As it can be seen from the timing diagram in Figure 6.4b and the comparator schematic in Figure 6.5, the race condition where both the inputs and the clock are high never occurs since the inputs are ON (or high) only when clk_1 and clk_2 are low.

6.4. DESIGN OF DAC

Figure 6.4 shows the implementation of DAC switches, realized by transmission gates. A reference voltage of 200 mV is used. With the common-mode voltage of 0.9 V, the positive reference voltage of 1.1 V and a negative reference voltage of 0.7 V is used. The outputs of the quantizer Q and $\bar{Q}$ are connected to the input of the DAC. In the design system, there are two DACs used. The outputs of one of the DACs are connected to the inputs of the 1st integrator. Another DAC is used in the HP loop connected to the inputs of the switched-capacitor integrator.

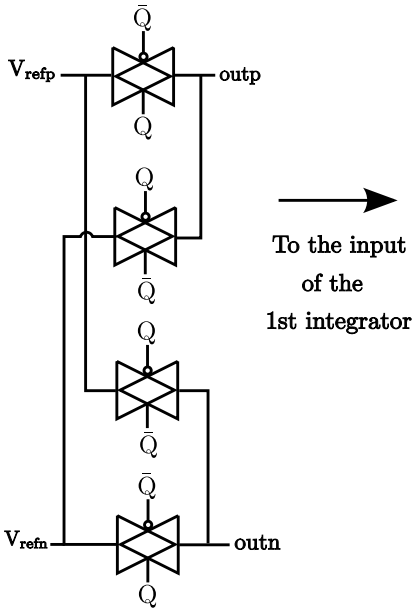


Figure 6.6: DAC

6.5. DESIGN OF SC VERY LARGE TIME CONSTANT NAGARAJ INTEGRATOR

To realize large time constants, switched-capacitors can be used to obtain accurate cut-off frequencies at the expense of larger area consumption. The technique proposed by Nagaraj [35] is area efficient and parasitic insensitive switched-capacitor integrator and can be used to achieve sub-Hz frequencies with good accuracy. This technique is implemented targeting sub-Hz cut-off frequency of the HP integrator.

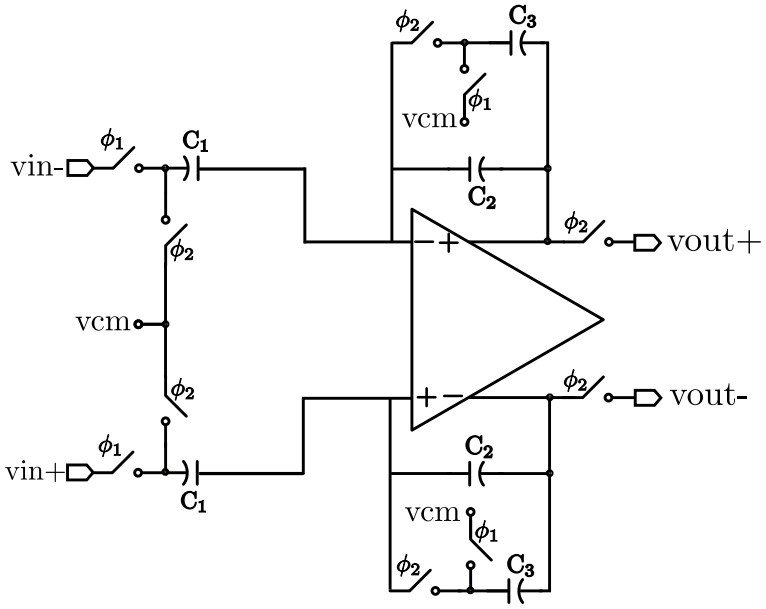


Figure 6.7: SC Nagaraj integrator

From Figure 6.7, it can be seen that the integrator consists of three different capacitors, a few switches switches and an OTA. The circuit operates in two non-overlapping phases. During phase 1, capacitor C_1 is charged to q_1 given by $q_1 = C_1 V_{in}$ which is transferred to capacitor C_2. The charge is balanced (q_2 is equivalent to q_1) but the voltage across the capacitor C_2 is either amplified or attenuated depending on the ratio of the capacitors.

Output voltage during phase 1 is given by

$$V_o = \frac{q_2}{C_2} \tag{6.2}$$

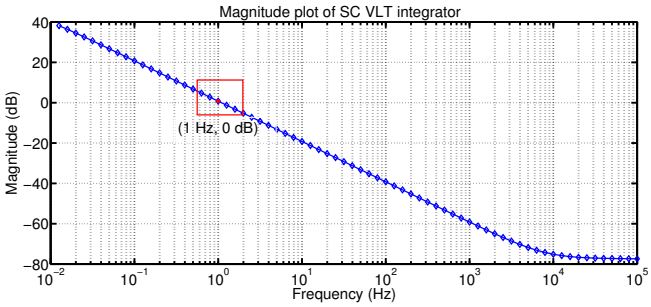
The intermediate voltage, V_o is stored in capacitor C_3. During phase 2, the charge stored in C_2 is withdrawn by C_1. The small amount of charge stored in C_3 is redistributed with the large capacitor C_1. As a result, a small fraction of the charge in C_3 is integrated by C_2. C_2 is a large capacitor (tens of pF) that is responsible for both scaling and integration and consequently 50% of the capacitance area is saved.

The integrator transfer function of the Nagaraj integrator in discrete-time domain is given by

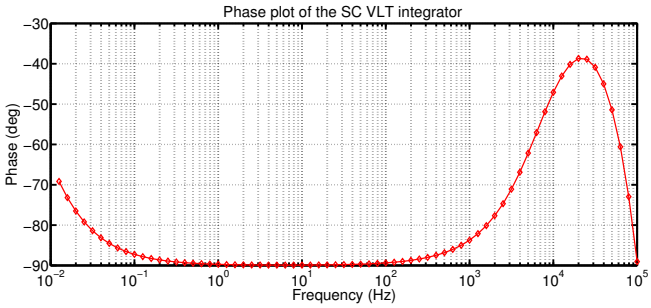
$$H(z) = -\frac{1}{\left[1+\frac{C_3}{C_2}\right]} \frac{C_1}{C_2} \frac{C_3}{C_2} \frac{z^{-1/2}}{1-z^{-1}} \tag{6.3}$$

The unity gain frequency, f_u of the integrator is given by

$$f_u = \frac{1}{2\pi} \frac{1}{\left[1+\frac{C_3}{C_2}\right]} \frac{C_1}{C_2} \frac{C_3}{C_2} f_{clk} \tag{6.4}$$



(a) Magnitude plot of the integrator



(b) Phase plot of the integrator

Figure 6.8: Integrator transfer function of the SC HP integrator

Table 6.5: Design parameters of HP integrator

Parameter	**Component**
C_1	0.5 pF
C_2	45 pF
C_3	0.2 pF
f_{clk}	128 kHz

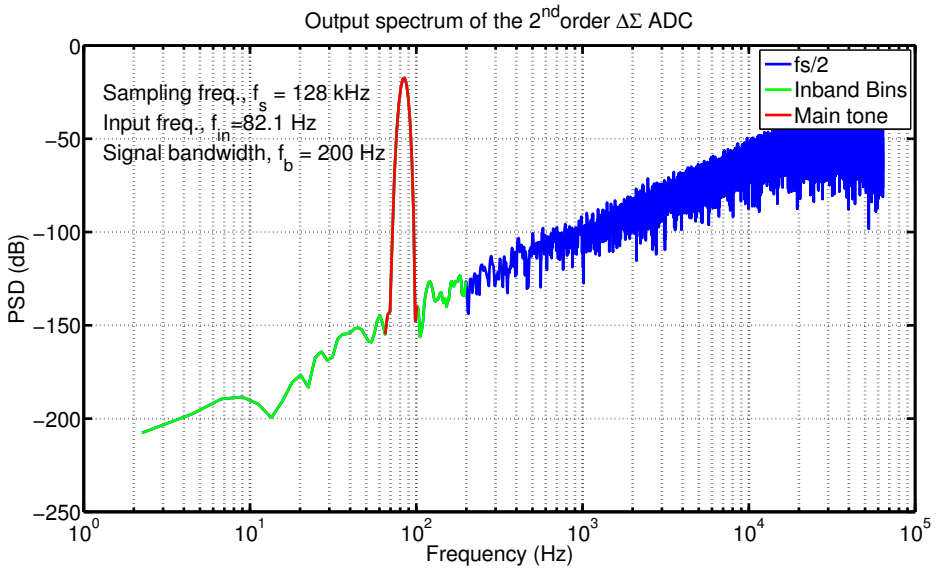


Figure 6.9: Output spectrum of the 2nd order ΔΣ for fin = 82.1 Hz

where f_{clk} is the clock frequency and is equal to the sampling frequency of the ΔΣ modulator.

The values of the capacitances and the clock frequency used in the high-pass integrator is summarized in Table 6.5. The value of the input capacitor C_1 is selected based on the allowed upper thermal noise limit and also the area constraint. This set of design parameters gives a time constant of 1 s and a unity gain frequency of 1 Hz for the designed integrator. The modulator is tested at 1 Hz due to simulation time constraints. It is possible to increase capacitor C_2 at the expense of larger area consumption or decrease the capacitor C_1 at the expense of increased noise-floor. By increasing C_2 to 63 pF while retaining the values of the other components as is, the high-pass cut-off frequency can be set at 0.5 Hz.

Figure 6.8 plots the integrator transfer function of the Nagaraj integrator. It can be seen in the plot that the unity gain frequency of the integrator is at 1 Hz with a -20 dB/decade slope roll off in the signal bandwidth range.

6.6. SIMULATION RESULTS

In this section, the results of the simulations carried out in the 0.18 μm AMS technology will be described.

6.6.1. EFFECTIVE NUMBER OF BITS

The output spectrum of the 2nd order ΔΣ without the HP loop is plotted in Figure 6.9. As it can be seen from the plot, the second and third order harmonics are sufficiently suppressed.

The output spectrum of the orthonormal HP ΔΣ ADC for fin = 82.1 Hz and fin = 1.1 Hz are plotted in Figures 6.10 and 6.11. As seen in the system simulations in Chapter 4, the noise from the HP integrator is low pass filtered with a slope of 20 dB/decade. From these plots, it can be concluded that the noise contributions from the HP integrator dominate at lower frequencies while the noise from the first integrator dominate at high frequencies.

6.6.2. POWER CONSUMPTION

The distribution of power consumption in the system, block-wise can be seen in Table 6.6. The first integrator is the most power consuming block in the system since it responsible for meeting the linearity

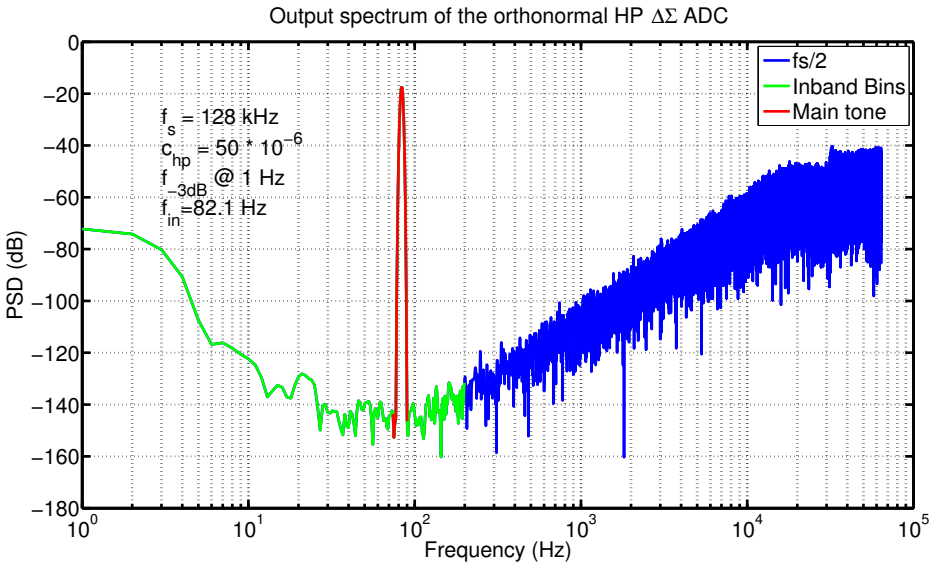


Figure 6.10: Output spectrum of the 2nd order orthonormal HP ΔΣ for fin = 82.1 Hz

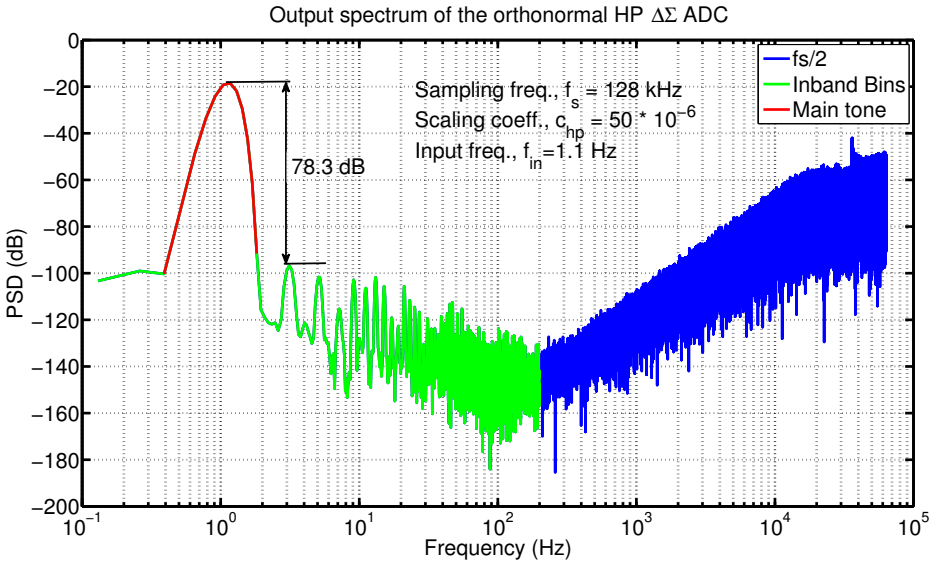


Figure 6.11: Output spectrum of the orthonormal HP ΔΣ for fin = 1.1 Hz

Table 6.6: Distribution of current consumption

Circuit block	Power consumption (in uA)
First integrator	76.6
SC integrator	65.4
Second integrator	3.7
Dynamic comparator & summer	0.005
Rest of the digital blocks	0.4
Total power consumed	146

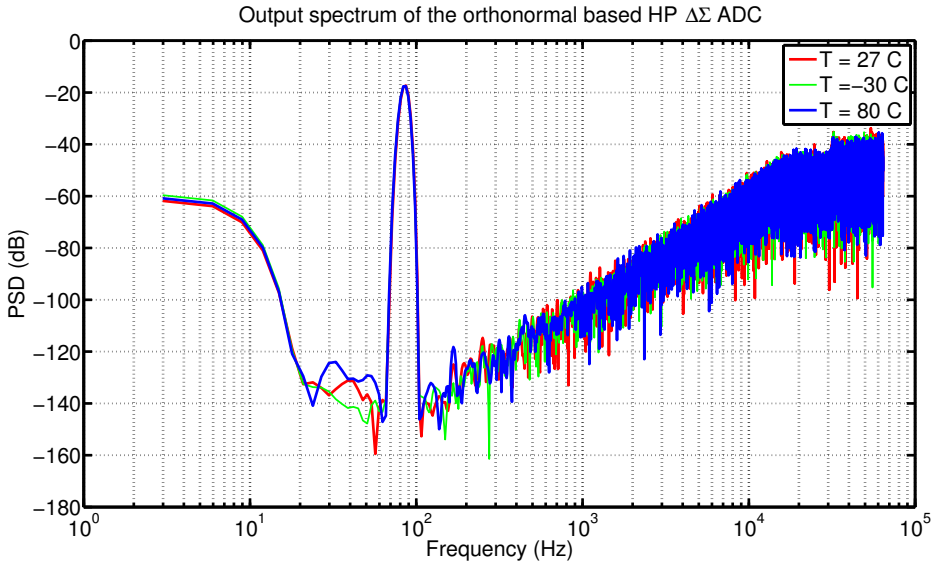


Figure 6.12: Impact of temperature on ΔΣ ADC for fin = 82.1 Hz

and noise requirements of the entire modulator. The second most power consuming block is the SC integrator in the HP loop. The total current consumption is about 146 μA from a supply voltage of 1.8 V.

6.6.3. EFFECT OF TEMPERATURE AND PROCESS VARIATIONS

Figure 6.12 plots the effect of temperature variation on the output of the orthonormal HP ΔΣ modulator. As it can be seen, the performance degrades slightly at higher temperatures. The input referred noise of the amplifiers increase as temperature increases. The noise from the switched-capacitor integrator in the sampling phase is directly proportional to temperature. Also, the transconductance of the amplifier decrease leading to an increase in noise in the integrating phase. Although both noise and distortion are slightly higher, they still meet the desired resolution.

In order to test the designed modulator for the impact of process variation, process corner simulations are carried out. In 0.18μm AMS technology, six different corners apart from the typical mean (tm) case are available. They are :

- wp - worst power, also known as fast NMOS and fast PMOS. In this case, fast refers to lowest possible threshold voltage.
- ws -worst speed, also known as slow NMOS and slow PMOS. In this case, slow refers to highest possible threshold voltage.
- wo - worst one, also known as fast NMOS but slow PMOS.
- wz - worst zero, also known as slow NMOS but fast PMOS.

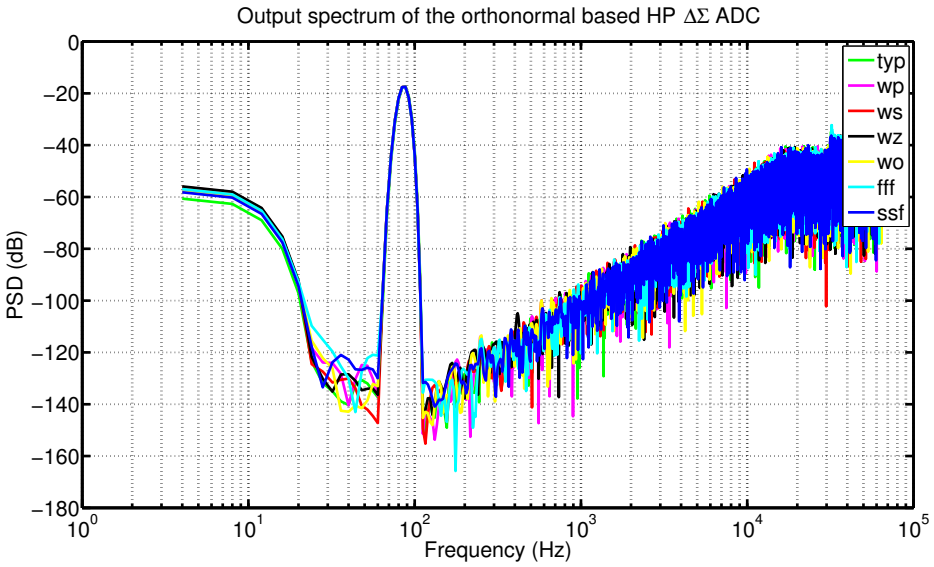


Figure 6.13: Impact of process variations on orthonormal HP ΔΣ modulator

- fff - fast fast functional.
- ssf - slow slow functional.

6.7. PERFORMANCE COMPARISON WITH THE STATE OF THE ART

Table 6.7 presents the performance comparison of different existing techniques to realize the very large time constant on chip. Realization of the high-pass cut-off can be achieved by analog (A) or digital (D) techniques. Among the techniques, pseudoresistors [7], [6] can be used to achieve very large time constant values but with limited linearity. If higher linearity is desired, switched-capacitor based techniques can be used. In [19], a traditional switched-capacitor is used which makes the area consumption higher. The capacitor multiplier [38] depends on g_m, R, and C and is therefore less accurate. A digital low-pass filter is used in [21] which leads to very accurate high-pass cut-off frequency, but requires a multi-bit DAC which limits the achievable linearity. In this work, the high-pass cut-off frequency is a function of ratio of capacitors only and therefore achieves upto 1% accuracy and as seen in Table 6.8, a linearity of 12 bits is obtained which places the designed HP ΔΣ modulator among the state of the art designs.

In the designed modulator, the high pass cut-off frequency is implemented using ratio of capacitors which is much more accurate and robust to PVT variations as compared to implementation using g_m and current sources. The achieved resolution is better than in [20] at the expense of higher power. Although the power consumption is much higher due to opamp-RC integrator implementation compared to g_m-C, the harmonic distortion is suppressed due to the use of resistors. Also, it is more robust with respect to process and temperature variations. Table 6.8 compares the performance of the designed high pass ΔΣ modulators with the other HP ΔΣ modulators in literature.

Table 6.7: Comparison of techniques for obtaining high-pass cut-off frequency

	This work	**Cantoya (TCAS-II)**	**Muller (JSSC)**	**Rezaee (JETCAS)**	**Denison (JSSC)**	**Harrison (JSSC)**
Year	2016	2013 [38]	2012[21]	2011 [7]	2007 [19]	2003 [6]
Technology	0.18 μm	0.5 μm	65 nm	0.18 μm	0.8 μm	0.18 μm
Type of biosignal	ECG	-	Neural	Neural	Neural	Neural
Bandwidth (Hz)	0.5 - 200	1.5 M	10 k	0.5 - 50 k	0.05 - 100	0.025 - 7.2 k
Technique [A or D]	Nagaraj SC integrator [A]	Capacitor multiplier [A]	IIR-filter [D]	Pseudo-resistors [A]	SC integrator [A]	Pseudo-resistors [A]
Accuracy of HP cut-off	Upto 1 %	Very low	High accuracy	Very low	Upto 1 %	Very low
Robustness of HP cut-off (to PVT)	Very high	Medium	Very high	Very low	Very high	Very low
Variables determining HP cut-off	Ratio of capacitors only	g_m, R, C	-	R, C	Ratio of capacitors only	R, C

Table 6.8: Performance comparison of recent CMOS HP $\Delta\Sigma$ modulators

	This work	**Mohan [20]**
Year	2016	2013
Tehnology	0.18 μm AMS	0.18 μm AMS
Supply voltage (V)	1.8	1.5
Architecture	2^{nd} order CT HP $\Delta\Sigma$	1^{st} order CT HP $\Delta\Sigma$
Integrator implementation	Opamp-RC	g_m-C
Sampling frequency (kHz)	128	256
Order of the HP loop	1	1
Bandwidth (Hz)	0.5 - 200 Hz	1 - 200 Hz
SNDR (dB)	76	62
ENOB	12 - bit	10 - bit
Power (μA)	146	7.5
HP cut-off frequency	Depends on ratio of capacitors only	Depends on g_m and a current source

7

Conclusions and Future research work

7.1. Conclusions

For recording ECG signals, an accurate high-pass cut-off frequency extending below sub-Hz has to be obtained to meet the bandwidth specification as determined by the specific application. Sub-Hz frequencies translate to large time constants that need to be realized physically. In order to develop an integrated system on chip for ECG applications, there is a need to integrate these large time constants. In this thesis, a structured electronic design methodology is proposed to develop high pass $\Delta\Sigma$ topologies.

The following research contributions are made in this thesis

1. In Chapter 3, a method is proposed to develop HP $\Delta\Sigma$ topologies using standard state space forms. As opposed to conventional $\Delta\Sigma$ structures that are either low pass or band pass, a different approach is taken where the signal transfer function is generalized to include high pass and notch filter transfer as well. It is shown that the proposed HP $\Delta\Sigma$ topologies satisfy the signal and noise transfer functions resulting from biquad, observable and controllable canonical, and orthonormal state space forms.
2. In Chapter 4, the intermediate functions given by the vectors $\mathbf{g}(s)$ and $\mathbf{f}(s)$ of the $\Delta\Sigma$ topologies are derived. The following observations are made :
   (a) The individual noise contribution of each of the integrators is analyzed and it is shown that the high pass integrator contributes significantly to the total noise of the system. Therefore, structures with a local or global feedback (HP loop around the pre-amplifier), mixed signal or not, need to be designed carefully for better noise performance.
   (b) Another important observation is that the noise from the high pass integrator is low pass filtered and is significant only at lower frequencies. Due to the low pass filtering action, the harmonics generated due to the HP integrator are also suppressed. The noise from the first integrator dominates the signal bandwidth with 2^{nd} order noise shaping.
   (c) $\sum_{i=1}^{3} \|g_i(j\omega)\|_2^2$ which gives the total noise power of the integrators is used as the noise figure of merit to compare orthonormal and observable HP $\Delta\Sigma$ topologies. It is shown that the orthonormal HP $\Delta\Sigma$ structure has a slightly better noise performance and is a preferred choice for implementation.
3. In Chapter 5, the performance of the 2^{nd} order orthonormal HP$\Delta\Sigma$ topology is evaluated for the integrator non-idealities i.e, finite DC gain, finite gain bandwidth and integrator coefficient variation. From the simulation results, a finite DC gain of 80 dB and a finite gain bandwidth of πf_s Hz for the first and the high pass integrator is sufficient to ensure minimum performance

degradation due to the integrator non-idealities. It is also observed that there is no significant degradation in the performance of the modulator due to time constant variation of upto ±40%.

4. In Chapter 6, it is shown that the designed orthonormal HP ΔΣ modulator achieves a resolution of 12 bits. A very large time constant switched capacitor is used to achieve the high pass cut off frequency of 1 Hz with high accuracy. Also, the corner and temperature analysis show that the designed modulator is pretty robust to process and temperature variations.

7.2. FUTURE RESEARCH WORK

In this thesis, only four HP ΔΣ topologies are developed. The other state space forms such as Hess and Schur decompositions can also be used to develop the corresponding ΔΣ topologies. Apart from applying various scaling techniques on the topologies to maximize the available dynamic range, finding the optimal state space for HP ΔΣ structures would be an exciting problem to work on. Apart from dynamic range, sensitivity can also be used as a criterion to evaluate various topologies.

In order to design higher order ΔΣ structures, matrix description needs to be developed. When each of the topologies are specified by matrices, its easier to obtain the intermediate functions computationally. They can then be evaluated directly for the performance criteria. There is a need for a software tool that includes the standard state space forms and generalized filter structures which would aid in developing the corresponding ΔΣ topologies. Based on the methodology proposed in this thesis, a program on MATLAB/C++ can be written to produce scaled state space based ΔΣ structures that have optimum dynamic range. Although there exists the delsig toolbox by Schreier and an online synthesis tool called the Ulm Sigma-Delta Synthesis Tool, they do not take a general signal transfer function into account, rather a low-pass or a bandpass filter characteristic.

Although a single quantizer is used to develop all the topologies in this thesis, multiple quantizers can also be used. This would result in bringing down the sampling frequency which would then make the implementation of the large time constant on-chip, both power and area efficient. Structures utilizing more than one quantizer specifically aiming at HP ΔΣ structures are worth investigating.

In order to achieve lower power consumption, g_m-C integrators could be used at the cost of lower linearity. If the analog front end is to be designed for a large number of electrodes, low power and low area would be an important criteria. Hence, the use of very large capacitors and resistors need to be minimized. A hybrid combination of the types of integrators could also be used to obtain an optimized system.

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