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# A split-cavity design for the incorporation of a DC bias in a 3D microwave cavity

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We report on a technique for applying a DC bias in a 3D microwave cavity. We achieve this by isolating the two halves of the cavity with a dielectric and directly using them as DC electrodes. As a proof of concept, we embed a variable capacitance diode in the cavity and tune the resonant frequency with a DC voltage, demonstrating the incorporation of a DC bias into the 3D cavity with no measurable change in its quality factor at room temperature. We also characterize the architecture at millikelvin temperatures and show that the split cavity design maintains a quality factor  $Q_i \sim 8.8 \times 10^5$ , making it promising for future quantum applications. *Published by AIP Publishing.*  
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In recent years, interest in 3D waveguide cavity resonators has been revived in the Josephson junction quantum bit (qubit) community.<sup>1–7</sup> Significantly enhanced relaxation and decoherence times on the order of hundreds of microseconds have been demonstrated for qubits in 3D cavities.<sup>7</sup> The 3D architecture has also enabled the measurement of entangled qubits,<sup>6</sup> single-photon Kerr effect<sup>2</sup> as well as the Autler-Townes effect.<sup>3</sup> So far, these results are achieved without the need of applying DC currents or voltages to the devices embedded in the cavities. However, the ability to do so would significantly expand the application of 3D cavities, just as the introduction of a DC bias into a coplanar waveguide cavity made it much more versatile.<sup>8–10</sup> For example, such a DC bias could enable the tuning of a membrane in a 3D optomechanical device.<sup>11</sup> For qubit measurements, an on-chip flux bias can be added by applying a DC current bias to allow frequency tunability of the qubit.

Having galvanic access to a quantum device inside a 3D cavity presents a significant challenge. Planar geometries have a 1D confinement of the electromagnetic field and thus allows access from the side of the cavity.<sup>8,9</sup> In 3D architectures, currents run along a closed 3D surface: incorporating wires into devices inside the cavity without compromising the cavity quality factor is challenging. One study reports a technique of doing so by inserting a sample with wires on a printed circuit board (PCB) board into a hole in the side of the 3D cavity.<sup>12</sup> These DC wires enabled manipulation of a quantum dot inside the cavity although this method suffered from a relatively low quality factor  $Q_L = 1350$ .

Here, we introduce a method for biasing a 3D cavity while maintaining an internal quality factor of  $Q_i = 8.75 \pm 0.03 \times 10^5$ . The dimensions of our near-rectangular cavity are illustrated in Fig. 1(a). The rounded corners in the xy-plane have a diameter equal to the height of the y-coordinate. According to a finite element simulation shown in Fig. 1(b), the resonant frequency of the lowest TE101 mode is expected to be around 7.816 GHz. The color corresponds to the magnitude of the electric field in the zx-plane, at the center of which the field reaches maximum. The measured resonant frequency of the bare cavity is  $f_0 = 7.743$  GHz at room temperature and ambient

conditions. The loaded Q-factor at room temperature is  $Q_L = 3920$ . Many implementations use a 3D cavity that is cut in half to allow for a nanodevice to be placed inside. The device is usually fabricated on a dielectric substrate and placed in the center to allow maximum interaction with the electric field. The idea in this article is to use this separation to our advantage by keeping the two halves galvanically separated and applying a DC voltage across it to bias the nanodevice. Such a connection could be achieved through a custom-designed substrate including connections to the back side of the substrate.

In designing the location of the split in the rectangular 3D cavity, it is important to consider how currents flow within such a resonant structure. For the fundamental mode of the cavity, electrons oscillate back and forth between the plates with the largest area via the side walls. One can see

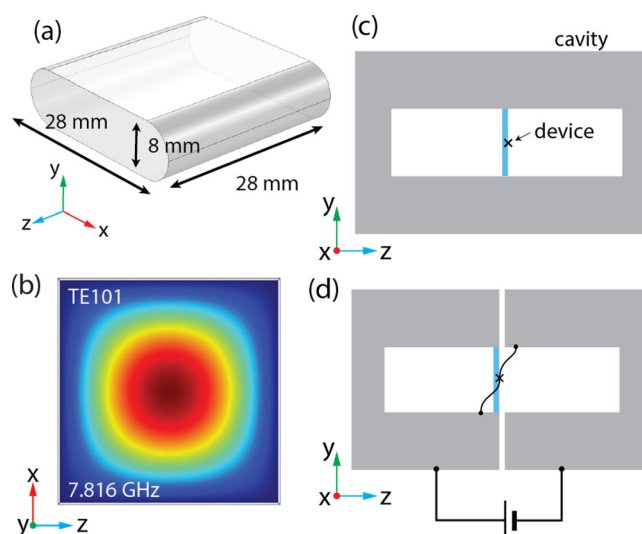


FIG. 1. Implementation of a galvanically accessible 3D cavity by a split-cavity design. (a) Design of the 3D cavity. (b) Electric field magnitude of the TE101 mode modelled by COMSOL. (c) A standard implementation of a nanodevice embedded inside 3D cavity without galvanic access. The blue line represents the substrate on which the device is fabricated, silicon or sapphire, for example. (d) Our proposed modification to the cavity geometry to allow a DC bias to be applied.

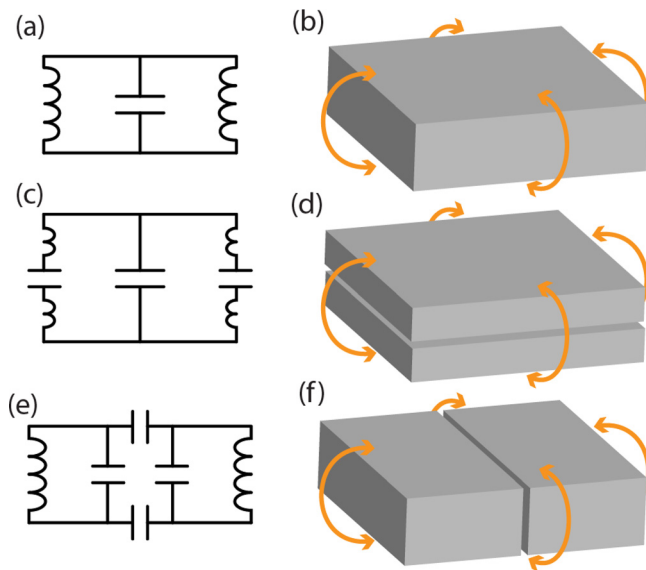


FIG. 2. Minimizing losses of the TE<sub>101</sub> mode of a split-cavity through choice of orientation of splitting the cavity. (a) An LC circuit representation of a cavity resonating in the fundamental mode. (b) A corresponding 3D representation of a box cavity where the orange arrows show the direction of current flow. For the TE<sub>101</sub> mode, the current paths along the side walls act as inductors, and the top and bottom walls as capacitor plates. (c) and (d) A circuit diagram and 3D representation of one proposed method of galvanically separating the box cavity. When introducing a separation perpendicular to the current flow, this adds capacitances between the inductors of the fundamental mode. (e) and (f) A circuit diagram and 3D representation of the method of separating the box cavity we use here for the incorporation of the DC bias. The plane of separation is parallel to the direction of current flow.

this as a simple LC circuit, where the top and bottom plates act as a capacitor and the current path along the side walls as an inductance. There are two ways we can split this cavity, parallel or perpendicular to the direction of current flow. Figs. 2(c) and 2(d) show a split cavity where the cut is perpendicular. Such a geometry creates additional capacitances in between the inductors which turns it into a dipole antenna, potentially causing losses by radiation. An alternative geometry would be to split the cavity as depicted in Figs. 2(e) and 2(f). The circuit diagram changes by splitting the capacitance of the LC circuit and separating these by two more capacitances. Since there is a far lower current density at the split, there likely is less chance of radiation losses. A thorough investigation into the losses from seams in cavities is given in Ref. 13.

Similar to the coaxial pin used to couple microwaves in and out of the cavity via the readout port, adding a DC wire that fully enters the cavity would have a significant impact on the cavity Q-factor as it would act as an antenna and contribute heavily to radiative losses. It is in principle possible to partially suppress this leakage using low pass filters although this presents challenges in terms of the loss rates of the elements and maintaining sufficient grounding to limit radiative losses. In the approach presented here, we avoid such potential problems by separating the two hemispheres of the cavity with a thin layer of insulator and using them directly as electrodes. The interface of the two halves forms a large capacitor that acts as a low-pass filter. We directly apply the DC voltage on the aluminum blocks, which can then be accessed from inside the cavity to connect the DC signals to the device, as

illustrated in Fig. 1(d). Using superconducting wires from the two halves of the cavity to devices embedded in it, such as qubits, one can then apply voltage or current biases to the devices. This could also potentially be implemented with traces directly on the sapphire substrates used to hold the devices in the cavity. The bandwidth of this DC bias scheme is limited by the capacitance between the two hemispheres and can be carefully engineered. For a 50  $\Omega$  source impedance supplying the DC signals and a 100  $\mu\text{m}$  layer Kapton tape insulator with a 180 pF capacitance between the hemispheres, we estimate the bandwidth for the DC signals to be around 18 MHz and could be even higher if the driving were provided by a lower impedance source.

To demonstrate the viability of biasing a split 3D cavity, we first present measurements studying how the quality factor is affected by introducing this split at room temperature. In Fig. 3(a), we show a full spectrum sweep as allowed by our vector network analyzer when the cavity is closed and when the cavity halves are separated by around 1.07 mm. Both configurations display a fundamental frequency, however with a slight shift: 7.74 GHz when closed, 7.62 GHz when opened, about a 1.6% change. This percentage shift was predicted well by finite element simulations by increasing the length of the box resonator, ignoring the open walls

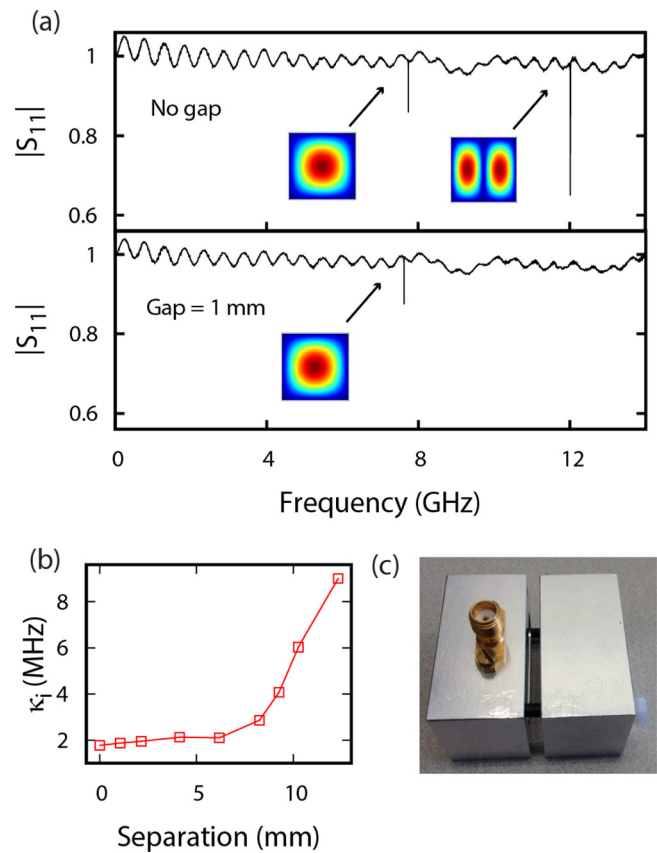


FIG. 3. Experimental observations from room temperature measurements showing that the TE<sub>101</sub> mode is not affected to first order even for relatively large gaps. (a) Full spectrum of the reflection coefficient for a (top) closed cavity and (bottom) a cavity separated by 1.07 mm measured at room temperature. The disappearance of the second mode is attributed to the restriction of current across the two halves. (b) A graph of the internal dissipation rate  $\kappa_i$  as a function of cavity separation. (c) A picture of the setup we used to separate the cavity halves. The screws used to connect them were surrounded by an insulating layer.

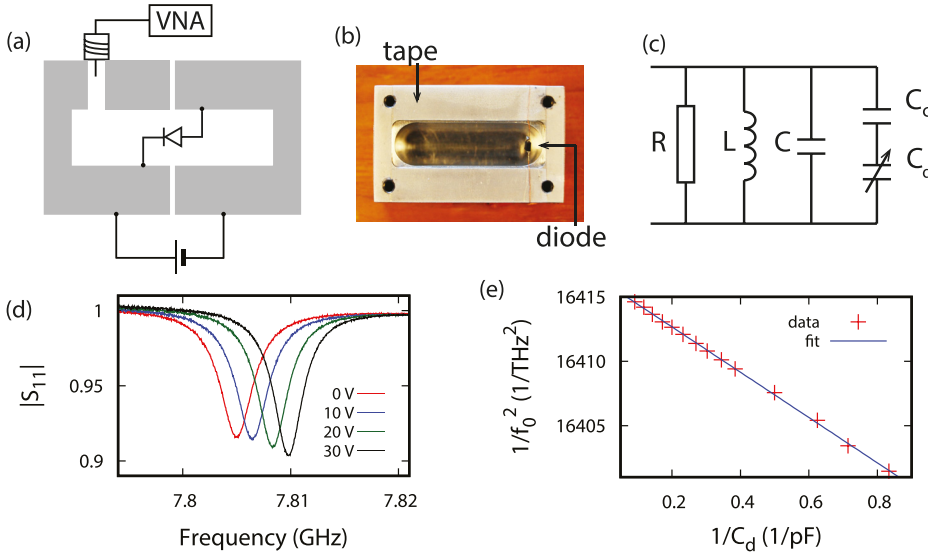


FIG. 4. Proof-of-concept demonstration of a DC tuneable 3D cavity using an embedded reverse biased diode. (a) Schematic of the experimental setup. The diode is reverse-biased by an external voltage applied across the cavity and the resonant frequency is measured reflectively. (b) A photograph of one half of the aluminum cavity. (c) An equivalent circuit diagram. The tuneable diode capacitance  $C_d$  is coupled in parallel to the main cavity through  $C_c$ . (d) Representative  $S_{11}$  curves measured by the vector network analyzer at room temperature as the bias voltage is varied. The resonant frequency is shifted but the quality factor preserves. (e) Inverse square of the resonant frequency as a function of the inverse of the diode capacitance.

in the region of the gap. There is also a second mode, TE201, at 12.02 GHz, but this can only be detected when the cavity is closed. One can understand this by the fact that the TE201 mode has a large component of current that flows across the split. When the two halves are separated, this current is presented with a large impedance from the capacitor and is therefore strongly suppressed. Even up to very large gaps on the order of millimeters, the linewidth of the TE101 mode, shown in Fig. 3(b), is relatively constant, indicating that at room temperature, the radiative losses are negligible even for millimeter gaps between the two halves.

To demonstrate the principle of DC operation of a device inside a cavity, we embed a diode (NXP BB131) inside the cavity. The diode capacitance can be tuned by a reverse voltage bias and the cavity resonant frequency is subsequently shifted. The interface of the left and right halves is separated

by a thin layer of scotch tape which acts as an insulator (0.05 mm thickness), and nylon screws are used to avoid shorts. Inside, the anode (cathode) of the diode is attached to the right (left) half of the cavity. An external DC voltage source is attached to the aluminum blocks, reverse-biasing the diode via the cavity walls. One half of the actual cavity is shown in Fig. 4(b). An equivalent parallel circuit model is illustrated in Fig. 4(c), in which the resistance  $R$ , the inductance  $L$ , and the capacitance  $C$  model the basic resonance while the capacitance of the diode  $C_d$  is coupled to the circuit in the model via an effective coupling capacitor  $C_c$ .

We perform a reflection measurement with an input power of 0 dBm. In Fig. 4(d), we plot the reflection coefficient  $S_{11}$ , normalized by the off-resonant background as a function of the frequency  $f$ . The resonant frequency  $f_0$  shifts to higher values as we increase the reverse bias voltage  $V$

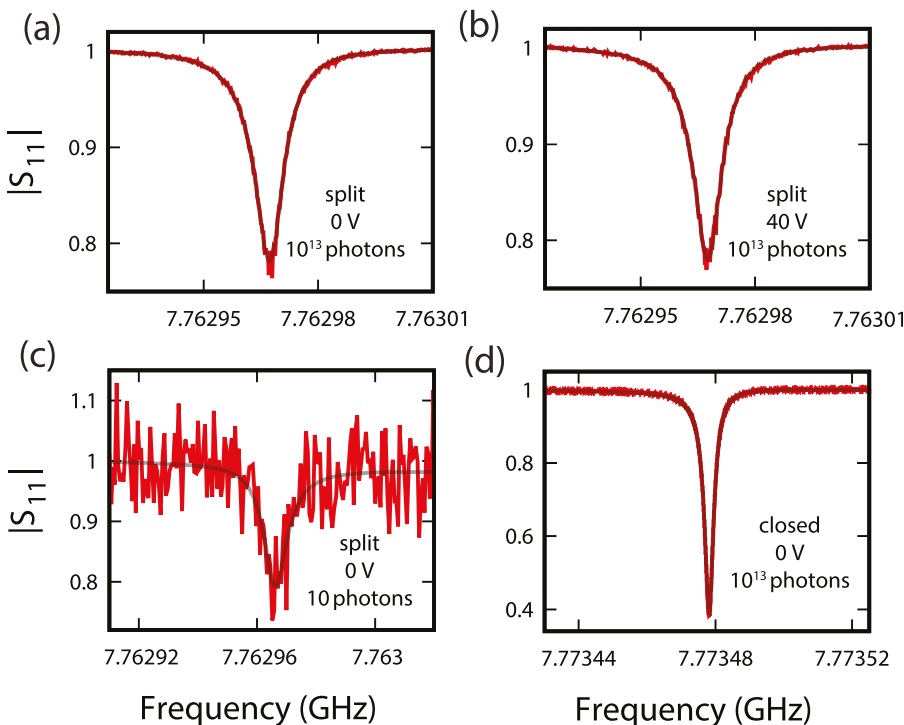


FIG. 5. Characterization of the internal losses of a split cavity at 16 mK inside a dilution refrigerator. Reflection coefficient measurement of a split cavity separated by  $100\ \mu\text{m}$  Kapton tape at  $P_{\text{in}} = -30\ \text{dBm}$  and a DC voltage of 0 V (a) and 40 V (b) with a quality factor  $Q_i = 8.75 \pm 0.03 \times 10^5$  and  $Q_i = 8.82 \pm 0.03 \times 10^5$ , respectively. (c) A reflection measurement at  $P_{\text{in}} = -148\ \text{dBm}$  (average photon occupation  $N = 10$ ), with  $Q_i = 8 \pm 1 \times 10^5$ . (d) Reflection measurement of a closed cavity at  $P_{\text{in}} = -30\ \text{dBm}$  showing an intrinsic quality factor  $Q_i = 2.748 \pm 0.001 \times 10^6$ . Black transparent lines indicate fits to the data.



applied on the diode. The quality factors of the cavity show no signs of decrease for  $V$  as high as 30 V and also show no systematic change compared to the quality factor of the cavity without diode at room temperature. The loaded quality factor is  $Q_L \approx 2084$  at 0 V and  $Q_L \approx 2292$  at 30 V. From the circuit diagram in Fig. 4(c), we can derive  $\omega_0^{-2} = L(C + (1/C_c + 1/C_d)^{-1})$ , where  $\omega_0 = 2\pi f_0$ . Assuming  $C_d \gg C_c$ , rewriting  $1/\omega_0^2$  as  $y$  and  $1/C_d$  as  $x$ , the above equation can be rearranged into a linear equation  $y = L(C + C_c) - LC_c^2 x$ . Using the value of  $C_d$  corresponding to each  $V$  provided by the diode data sheet, we plot  $1/f_0^2$  as a function of  $1/C_d$  and perform a linear fit as shown in Fig. 4(e). We further approximate the value of the characteristic impedance  $Z_0 = \sqrt{L/C}$  to be  $Z_{TE101} \approx 540 \, \Omega$  and obtain the following parameters:  $L \approx 10 \, \text{nH}$ ,  $C \approx 35 \, \text{fF}$ , and  $C_c \approx 6.65 \, \text{fF}$ .

To investigate the feasibility of the split-cavity technique for quantum experiments, in Fig. 5 we show the response of a split-cavity design made from 6061 aluminum alloy measured at a temperature of 16 mK. Kapton tape of 100  $\mu\text{m}$  thick was used to galvanically isolate the two halves of the cavity. Fig. 5(a) shows the reflection coefficient without any voltage bias, and Fig. 5(b) shows the same when applying 40 V. Both measurements reveal similar quality factors,  $Q_i = 8.75 \pm 0.03 \times 10^5$  and  $Q_i = 8.82 \pm 0.03 \times 10^5$ , respectively, where the errors are statistical errors from the fit. Although the internal quality factor from such fits, determined by the depth of the dip in the reflection coefficient, can include systematic error from cable reflections, we also estimate a lower bound of the internal quality factor from the loaded quality factor obtained from the resonance linewidth. For all cryogenic measurements reported here, we find a lower bound of  $Q_i > 7.5 \times 10^5$  (see [supplementary material](#) for discussion). Fig. 5(c) shows a measurement at a cavity input power  $P_{\text{in}} = -148 \, \text{dBm}$  (10 photons) with a fit that corresponds to an intrinsic quality factor of  $Q_i = 8 \pm 1 \times 10^5$ . This independence of internal losses to input power has been observed in previous experiments and is one of the key advantages of 3D cavities over planar resonators.<sup>14</sup> For the closed cavity with no Kapton tape, we find an intrinsic quality factor  $Q_i = 2.748 \pm 0.001 \times 10^6$ . Although the split cavity has a smaller quality factor, the reported  $Q_i > 7.5 \times 10^5$  is sufficient to enable sensitive quantum experiments in a 3D microwave architecture.

In conclusion, we have demonstrated a simple method of applying a DC bias up to 40 V in a 3D microwave cavity that maintains a high quality factor. We show that the intrinsic quality factor can be as high as  $Q_i = 8.75 \pm 0.03 \times 10^5$  at dilution refrigerator temperatures, making it suitable for use in 3D implementations of microwave nano and quantum devices.

See [supplementary material](#) for a thorough documentation of the cryogenic measurements.

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