Single-grain Si TFTs for high-speed flexible electronics

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ABSTRACT

Existent flat-panel display is mechanically stiff because it requires external connection of IC chips. At its present stage, displays with a-Si, metal oxide semiconductor or organic TFTs require still external connection of data driver and controllers, because of their low carrier mobilities. We will review our recent progress on direct formation of high speed Si circuits fabricated with a plastic compatible temperature. Large Si grains with a diameter of 4 microns were formed on predetermined positions by a pulsed laser crystallization process with a plastic compatible temperature. High performance transistors were fabricated inside a single Si grain.

1. INTRODUCTION

In the recent information era, people need to extract valuable information and to communicate with others in an interactive way at anytime and anywhere. A light-weight, rugged and flexible multifunctional display with data input, processing, storage and wireless-communication will be helpful in this purpose. Plastic substrates are an ideal platform for development of light-weight and ultra-large displays owing to their compatibility with roll-to-roll processing.

Although extensive research and development has been carried out on electronic paper (e-paper) and OLED display, none of the methods demonstrated satisfies all the functional requirements mentioned above. Existent e-reader and tablet PC are still partly stiff because the final system requires external connection of display drivers and controllers. Those limitations are caused by lack of a suitable material and fabrication technique for producing high-speed circuits on a flexible sheet.

We propose a technique that overcomes the problems by forming high speed Si circuits directly on a plastic substrate. The precursor Si will be formed at a plastic substrate compatible temperature. Laser crystallization will then be used for forming Si grains at predetermined positions. Transistors will be fabricated in the grain; hence having the same properties as those of SOI-FETs. The high performance TFTs can be used not only for pixel switches, but also for both gate and data driver circuits, memories, processing unit and radio-frequency circuits on a flexible substrate. This will enable elimination of the silicon chips connected to a flexible substrate and hence realize the super e-paper: a flexible sheet-type personal computer in which there is a display, display-driver, memories, a central processing unit and a wireless communication unit on a polymer substrate as shown in the Fig. 1.

This paper gives overview and recent progress on direct formation of the single-grain Si TFTs at an ultra low temperature (below 150^{o}C). We first investigated SiO_2 deposited by ICP-CVD at 80°C. We could achieve a very low interface trap density in the order of 10^{10} $cm^{-2}eV^{-1}$ despite of the low deposition temperature. Large Si grains with a diameter of 4 microns were formed on predetermined positions by a pulsed laser crystallization process with a plastic compatible temperature. High quality SiO_2 was used for fabricating TFTs inside the grain under 100°C. The field mobility for the electron was able to reach 225 cm^2/Vs.

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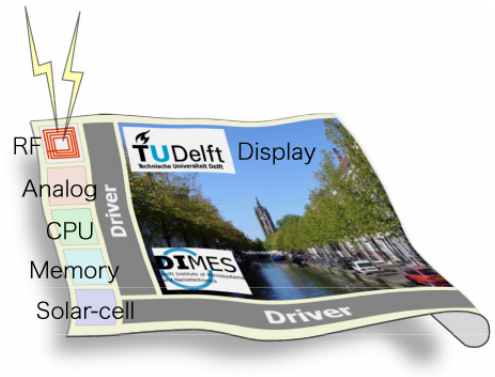

Figure 1. Schematic of fully flexible display system integrated with high-speed data communication, storage, and processing units.

2. SINGLE-GRAIN SILICON FOR HIGH-SPEED FLEXIBLE ELECTRONICS

2.1 Amorphous-Si, organic and metal oxide TFTs on a flexible substrate

As for the plastic substrate material, because of its high optical transparency, low cost, and chemical compatibility with most semiconductor process, polyethylene terephthalate (PET) seems to be an ideal candidate. The maximum allowed temperature is however approximately 120°C.

Standard process temperature of amorphous silicon (a-Si) TFT is about 350°C. The temperature can be lowered by lowering deposition temperature of a-Si and SiN, allowing us to form a-Si TFTs on a plastic compatible temperature. [1] For example, LG.Philips demonstrated a 14.1 inch full-color e-paper based on the micro-capsule method and hydrogenated amorphous silicon (a-Si:H) TFTs directly formed on a thin metal substrate with a process temperature below 200°C. However the low electron mobility of a-Si:H of less than 1 cm^2/Vs will become a barrier for integrating data driver and controlling circuits on the same substrate. Another serious issue is the bad reliability of the a-Si:H TFT fabricated at the low-temperature.

Organic semiconductors are attractive materials for fabricating TFTs at a low temperature [2-4]. In particular, a polymer [5] allows us to deposit the semi-conductor film locally with a printing technique, such as the ink-jet process. This allows us to have a low-cost and large area process. In 2010, Sony http://www.youtube.com/watch?v=9OvTLg4i2_U has developed rollable OLED display with the organic semiconductor TFTs integrated with gate driver. However, electron mobility and reliability of the organic semiconductors are even less than those of the a-Si:H, therefore it is very difficult to integrate peripheral driver and control circuit.

Transparent amorphous metal oxide semiconductors, such as In-Ga-Zn-O (a-IGZO)[6], have attracted a lot of attention s recently as the material can offer higher mobility than a-Si and organic counterparts. The a-IGZO can be formed easily on a plastic substrate even at room temperature and solution based technique. The hole mobility is higher than that of a-Si, however, it is still limited to 20cm^2/Vs. Another disadvantage is that hole mobility is extremely low and there exist so far no p-type metal oxide semiconductor TFTs available. The lack of CMOS configuration will increase power consumption.

2.2 Poly-crystalline Si TFTs on a flexible substrate

Excimer-laser crystallization of a-Si has been used for production of LCDs based on poly-Si TFT on a glass substrate. [7] The high maximum process temperature, which is around 400°C, is primary due to de-hydrogenation of a-Si before laser crystallization. The temperature could be reduced if de-hydrogenation step is performed by laser annealing or another

deposition that provides a-Si having no hydrogen is employed as a precursor material. By doing so, the pulsed laser crystallization of a-Si can form polycrystalline Si directly on a plastic substrate as heat diffusion length in SiO_2 during the short melt and regrowth process is fortunately very short; about a few hundred nm. On a plastic substrate coated with a buffer layer of the SiO_2, poly-Si TFTs have been fabricated [8].

Alternatively, ready-made poly-Si TFTs on a glass substrate with high temperature process can be detached and transferred to a flexible plastic substrate. In 2006, EPSON co. Ltd presented a prototype of an A6-size e-paper having a high resolution of 1536×2048 pixels with an integrated display driver with a method called SUFTLA method. Here polycrystalline silicon TFTs that are fabricated on a glass substrate was firstly bonded with another glass substrate on the surface with a water soluble adhesive bond. Excimer-laser irradiates from the original glass substrate side and, with laser ablation, the substrate is removed. After bonding with a plastic sheet with a permanent adhesive bond, the temporal glass substrate is removed in water. The layer transfer process requires additional steps, thus the increased production cost and decreased yield are critical issues. Therefore direct formation of TFT on to a flexible substrate is desired.

In any case, reported electron mobility of the poly-Si TFTs is in the order of 50-100cm^2/Vs. The relatively low value is because the polycrystalline silicon includes a lot of random grain boundaries due to formation of random and small grain formation in the film. Such random boundaries become electrical barriers against carriers and significantly decrease carrier mobility. Thus removal of the grain boundaries by enlargement and location-control of the grain is crucially important.

2.3 Single-grain Si TFTs as a solution

In order to integrate various kinds of functions, such as gate and data drivers, data storage, processing unit and wireless communication unit on a flexible plastic substrate, TFT needs to have electron mobility of more than 500 cm^2/Vs. We propose single-grain Si TFTs as a solution for this. The single-grain Si TFT is a transistor that is fabricated inside a single grain of silicon. If location of individual silicon grain is accurately controlled, the position of channel region of FETs can also be aligned inside the island. The 2D location control of Si grains can eliminate inclusion of the random GBs and therefore should perform like SOI-MOSFET.

DIMES have actually fabricated the single-grain Si TFT in a single grain silicon whose location is controlled by so called μ-Czochralski method[9, 10]. The μ-Czochralski method developed by DIMES can control the position of the grains by using a narrow cavity inside a substrate as shown in Fig. 2. The process has a locally increased thickness of precursor a-Si film filling a cavity (grain-filter) in a substrate. Upon excimer-laser irradiation, the grain filter melts non-completely, whereas the surrounding melts completely. During vertical growth of the pre-existing seeds in the grain filter, occlusion of grains occurs reducing the number of growing grains. By increasing the aspect ratio, only single grain can be filtered out from many pre-existing fine grains.

Experimental details for forming the grain-filter structure has been described elsewhere [10]. The hole diameter was approximately 100 nm and a 250 nm thick a-Si film was then deposited by LPCVD. A single 56 ns long XeCl (308nm) excimer-laser light irradiates the Si surface. Large Si grains with a grain size of up to 9 μm were aligned in predetermined positions [10, 11]. By fabricating TFTs on each grain we achieved 600 cm^2/Vs of mobility [12]. Not only the discrete transistors, analog and RF building blocks were designed and fabricated [13]. An operational amplifier and a voltage reference demonstrate DC gain of 50 dB and power supply rejection ratio of 50 dB, respectively. With a cut-off frequency of the SG-TFTs of about 5 GHz, a RF cascode amplifier circuit is demonstrated with an operation frequency of 430MHz with a channel length of 1.5 μm.

Thus, SG-Si TFT fabrication by the μ-Czochralski method exhibits similar characteristics as SOI-FETs and is a promising option for realizing the Super e-paper. The TFTs were, however, fabricated with a maximum process temperature of 550ºC due to LPCVD deposition of precursor a-Si, which is obviously much higher than resistant temperature of a plastic substrate. If such a high performance TFT could be fabricated at an ultra-low process temperature, the device could be applied to a direct formation of system circuits (e.g., memory, CPU) as well as a high quality display on a plastic foil.

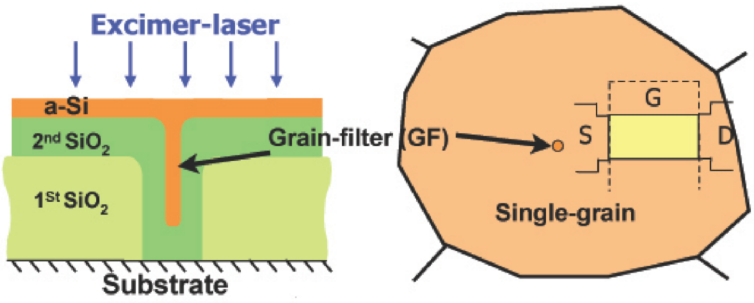

Figure 2. Schematic of μ-Czochralski (grain-filter) process (left) and single-grain Si TFTs (right).

3. LOCATION CONTROL OF SILICON GRAINS ON POLYMERIC SUBSTRATE

In this section we will discuss ultra low-temperature formation of location-controlled silicon grains. Amorphous-Si were deposited either by sputtering or evaporation on a substrate having the structure of the μ-Czochralski process.

3.1 Sputtered Si combined with the μ-Czochralski process

A-Si film can be deposited by sputtering at a deposition temperature below the plastic deformation temperature. Excimer-laser crystallization of the a-Si film causes no thermal damage to the plastic substrate if the two are separated by a thin (< 0.5 μm thick) buffer layer – such as SiO_2, which can be deposited at an ultra-low temperature as well. This is because a short but intense pulse of laser energy is absorbed fully by the a-Si surface, and the heat diffusion length in such a short time is not more than 300 nm in SiO_2. Unfortunately, sputtered α-Si is easily ablated by the explosive evolution of the trapped ambient gas (such as Ar) during excimer-laser crystallization, resulting in a grain size smaller than 300 nm. Ablation can be avoided by thermal annealing at 500◦C before laser crystallization. However, high-temperature annealing is clearly not suitable for plastic substrates. Thus the suppression of ablation without high-temperature post-annealing poses a big challenge for the direct preparation of high-quality Si on plastic substrates.

First, optimization of the sputtered Si was performed as it is easily ablated with excimer-laser. A-Si was sputtered on non-structured oxidized Si wafer with various bias conditions. An α-Si film was deposited by DC pulsed magnetron sputtering from a circular 12 inch intrinsic Si target (99.9999%) on the SiO_2 (100nm)/c-Si substrate. Deposition is performed in a pure argon atmosphere at 0.16 Pa. The frequency *f* of DC pulses is 150 kHz and the pulse width is 2.6 μs. The deposited a-Si film is crystallized with a pulsed XeCl excimer laser at room temperature. It is found that, when a bias is applied during the sputtering, the α-Si film is easily ablated during laser crystallization, even at a lower energy density than the complete melt condition. However, α-Si film deposited without bias can endure well beyond the complete melt condition without the ablation[14]. For 140 nm-thick α-Si film, the grain has a diameter of 1.8 μm with a petal-like shape. These grains can be obtained in a large energy density window.

Then μ-Czochralski process (grain filter) was combined with the sputtered a-Si to obtain location-controlled grains. A 250 nm thick a-Si was sputtered on oxidized Si wafers with holes (grain filters) having a diameter of 100 nm in the SiO_2. Single shot of excimer-laser light was irradiated to the structure. Despite of a worse step coverage of the sputtered film, grains with a maximum diameter of 4 μm can be successfully obtained at the predetermined positions (Fig.3).

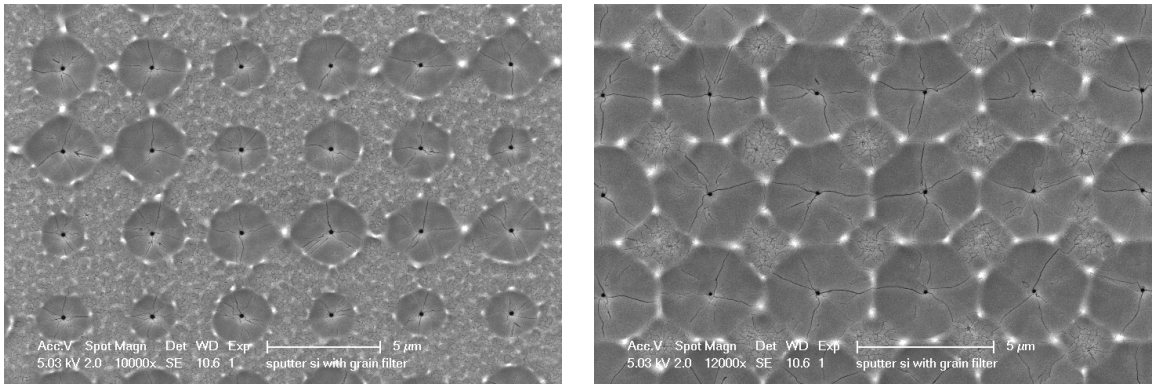

Figure 3. SEM image of grains grown from a 250 nm thick sputtered a-Si film crystallized at 875 mJ/cm^2 (left) and 900 mJ/cm^2 (right).

3.2 Evaporated Si and μ-Czochralski process

Next, we have used evaporation for deposition of a-Si film. Evaporation can deposit a-Si without hydrogen nor argon with relatively simple way. In this case, we have used a quasi-plastic substrate with 8 μm thick polyimide layer coated on a Si wafer (Fig.4). The grain filter structure was fabricated on the substrate. 250 nm thick a-Si was then deposited on the structure. In a high-vacuum chamber, silicon in a crucible was melted by electron-beam irradiation and evaporated to the substrate mounted on rotating table. Finally excimer-laser with an energy density of 700mJ/cm^2 irradiated the surface. Figure 4 shows optical microscope view of the crystallized sample. It can be seen that silicon grains having a diameter of 2 μm have been regularly placed on the matrix of the grain filter.

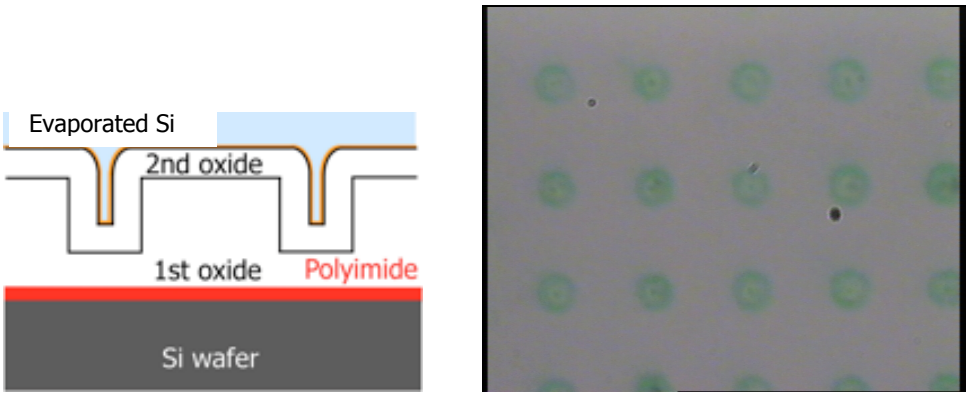

Figure 4. (Left) Cross-sectional view of the structure used for evaporated silicon. (Right) Optical microscope view of laser crystallized silicon film. Distance between the grain filter is 6 microns. Si grains, which is in green color, have the diameter of about 2 microns.

4. HIGH QUALITY SiO_2 DEPOSITED AT ULTRA-LOW-TEMPERATURE

For high performance TFTs, a high quality gate oxide with an interface quality as good as that of a thermal oxide is required to meet the high quality Si. However, the difficulty lies in obtaining those SiO_2 at ultra-low-temperature, i.e., a temperature below 100°C, for application in a flexible display on a plastic integrated with system circuits.

4.1 Issues in SiO_2 deposition

There are many methods to deposit an oxide at around 400°C such as by tetraethoxysilane (TEOS), electron cyclotron resonance plasma-enhanced chemical vapor deposition (ECR-PECVD), and reactive plasma deposition. The ECR can

realize SiO_2 with a Dit of $2x10^{10}$ eV^{-1}. However, those processes cannot realize good interface property at a very low deposition temperature. At an ultra-low temperature, the SiO_2 layer tends to become less dense and more porous, hence, low quality interface with Si because of less chemical reaction at the growing surface. Inductively coupled plasma chemical vapor deposition (ICP-CVD) has many advantages, such as independent control of ion energy and current, high electron concentration, and wide pressure range. These can allow less ion damage to the Si surface and a high density of reactive radicals. Thus, it can deposit high quality SiO_2 with good interface property. However, the deposition temperature reported so far is 250°C, which is still too high for the plastic electronics.

4.2 SiO_2 deposited by ICP

We used an ICP-CVD deposition system, which consists of a plasma generator, a planer-type inductor, and a ceramic chamber. Radio-frequency RF power with a frequency of 13.65 MHz was applied to the inductor. ICP was generated in a ceramic chamber that is encircled by an inductive coil. RF power was applied to the coil with a frequency of 13.56 MHz. Plasma was excited by an electric field generated by a transformer from the rf current in a conductor. The changing magnetic field of the conductor induces an electric field in which the plasma electrons are accelerated. Oxygen was fed though an up gas shower and subjected to the plasma, while the SiH_4 (diluted in 95% He gas) was fed through a gas ring just above the heat chuck and reacted with oxygen radicals to form SiO2. The standard process condition is as follows: 9.2 sccm O_2 flow, 150 sccm SiH_4/He flow, 2 Pa pressure, and 500 W rf power. The oxygen plasma treatment was for 5 s, which was introduced just before the deposition to oxidize the surface and ensure a high oxygen/silane ratio at the interface during growth. It also stabilized the plasma before the deposition. Different depositions of SiO_2 were also performed with the pressure range of 2–8 Pa and SiH_4/He flow of 80–240 sccm.

4.3 Electrical properties of the SiO_2

Metal-oxide-semiconductor capacitors were processed on p-type (100) silicon wafers with a resistivity of 5–10 Ohm cm. After the wafer dip etching in 0.55% HF solution for 4 min to remove the native oxide, SiO_2 was deposited under various conditions. We have also deposited TEOS by PECVD at 350°C for comparison. Then aluminum was sputtered on the oxide surface and patterned onto an area of 0.1225 cm^2 by photolithography and reactive ion etching. The back side of the wafer was also covered with Al to form an ohmic contact. All the processes were kept under 100°C.

Capacitance–voltage (C-V) measurement was used to investigate the interface characteristic. Interface density Dit was calculated from low (100 Hz) and high frequency (1MHz) C-V measurements. Figure 5 shows the C-V characteristic of SiO_2 deposited at the standard conditions. The good matching of the low and high frequency C-V in the accumulation and transition regions indicates a high quality interface with Si. The interface trap density as a function of the applied gate voltage Dit-V_{AG} within the bandgap is extracted from the high and low frequency C-V characteristics. The Dit was calculated to be 1.48×10^{10} $cm^{-2}eV^{-1}$ and the threshold voltage Vth was 0 V.

The current–voltage (I-V) characteristic of SiO_2 was measured. Figure 5 (right) shows the current density (J) as a function of the applied electrical field (F) for the SiO_2 deposited with the standard deposition conditions. Resistivity, defined by a resistance at an electrical field E of 1 MV/cm, is $4.7x10^{14}$ Ohm cm. Breakdown field (E_B), defined by an E value when J is at $1x10^{-6}$ A/cm^2, is 5.6 MV/cm.

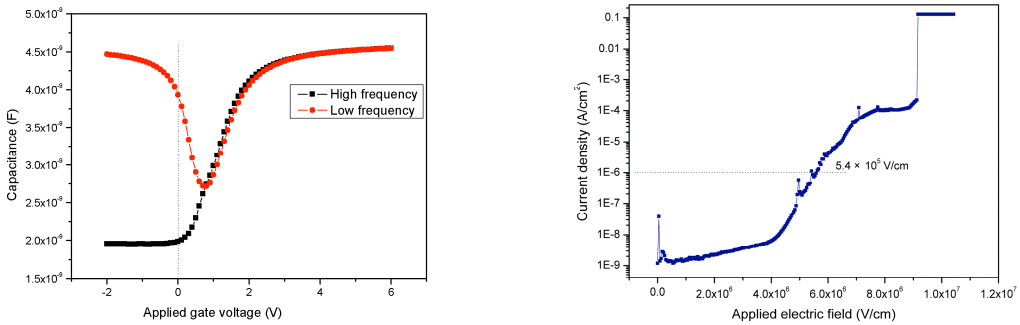

Figure 5. C-V (left) and J-E (right) curves of MOS capacitor with the SiO_2 deposited at 80°C by ICPECVD.

5. SINGLE-GRAIN SI TFTS FABRICATED AT ULTRA-LOW-TEMPERATURE

In this section we report single-grain Si TFTs fabricated at 100°C.

5.1 Fabrication process

The SiO_2 film deposited by ICPECVD was used as a gate insulator for the TFTs. The TFTs used in this experiment were fabricated with the micro-Czochralski process under 100°C. A 250 nm amorphous Si was sputtered at 100°C. Then the amorphous Si was crystallized by an excimer laser with an energy density of 900 mJ/cm^2. The grain size was 4 μm after laser crystallization.

After patterning Si island, 100 nm SiO_2 oxide was deposited by ICP-CVD and a 675 nm Al gate was sputtered. After patterning the gate, the source and drain were doped with 10^{16} ions/cm^2 by phosphorus implantation at 30 keV for the n-channel. The dopants were activated by an excimer laser at 300 mJ/cm^2. The channel width and length were 1 micro m.

Subsequently, Al is sputtered at a room temperature and patterned as a gate. Both channel length and width is 1 micron. The channel is made inside the grain and positioned outside the grain filter. Source and drain region is made with ion-implantation of phosphorus and activation by the excimer-laser irradiation at a room temperature. Finally source and drain electrodes are made by Al sputtering at a room temperature.

5.2 Measurement results

Figure 6 shows the transfer characteristic (I_D-V_G) and output characteristics (I_D-V_D) of TFTs. The field effect mobility evaluated in the linear region at low V_D was estimated to be 225 cm^2/V s. Subthreshold slope of the SG-TFTs is 0.494 V/dec.

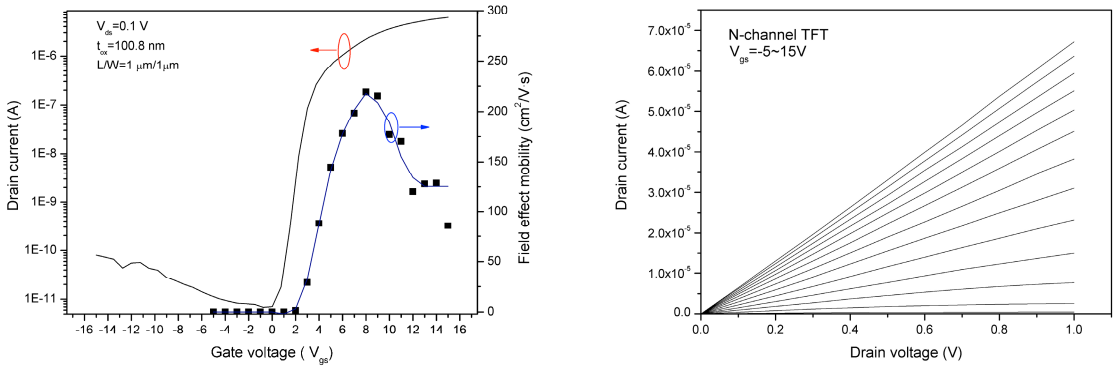

Figure 6. Transfer (left) and output (right) characteristics of single-grain silicon TFTs fabricated with process temperature of 100°C.

6. CONCLUSIONS

This paper gave overview and recent progress on direct formation of the single-grain Si TFTs at an ultra low temperature (below 150°C) for future complete integration of high-speed digital and analog circuits on a flexible display. Large Si grains with a diameter of 4 μm were formed on predetermined positions by the μ-Czochralski process with a pulsed laser crystallization process with a plastic compatible temperature. We then introduced SiO_2 deposited by ICP-CVD at 80°C. We could achieve a very low interface trap density in the order of 10^{10} $cm^{-2}eV^{-1}$ despite of the low deposition temperature. Finally the high quality SiO_2 was used for fabricating TFTs inside the grain with a process temperature under 100°C. The field mobility for the electron was able to reach 225 cm^2/Vs.

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