Winding Design of Series AC inductor for Dual Active Bridge Converters

Shen, Zhan; Wang, Huai ; Shen, Yanfeng; Qin, Zian; Blaabjerg, Frede

DOI
10.1109/APEC.2018.8341068

Publication date
2018

Document Version
Final published version

Published in
Proceeding of IEEE-APEC' 2018

Winding Design of Series AC inductor for Dual Active Bridge Converters

Zhan Shen*, Huai Wang*, Yanfeng Shen*, Zian Qin†, Frede Blaabjerg *
zhs@et.aau.dk, hwa@et.aau.dk, yaf@et.aau.dk, Z.Qin-2@tudelft.nl, fbl@et.aau.dk
*Department of Energy Technology, Aalborg University, Aalborg, Denmark
†Faculty of Electrical Engineering, Mathematics and Computer Science, Delft University of Technology, Delft, Netherlands

***Abstract*— The ac resistance and parasitic capacitance of the inductor are the primary considerations in the winding design for the dual-active bridge converter (DAB). They are dependent of up to four independent structure variables. The interactive restrictions between those variables makes the design difficult. In this paper, the core-related capacitances between the central limb, side limb, yoke and winding are derived, and a local optimization for it is proposed. Moreover, a total winding capacitance design method is proposed by mapping the four dimensional problem into two dimensions. The analysis and design are verified by finite element method simulations and experimental results on a 100 kHz prototype are performed.**

***Index Terms*—Dual active bridge, Series inductor, Ac resistance, Parasitic capacitance.**

I. Introduction

The dual-active bridge converter (DAB) is a promising topology in applications e.g. electric vehicles, dc power systems, solid-state transformers [1, 2]. A series ac inductor is necessary for its ac link (c.f. Fig. 1). The ac resistance and parasitic capacitance of the inductor are the key considerations for the winding structure [3–7]. In winding design process, the design input variables such as the mean length per turn (MLT) and number of turns N are usually given. The optimal design of winding ac resistance depends mainly on conductor diameter d_i and the number of layers p. On the other hand, the parasitic capacitance C is dependent on two more structure variables: layer insulation distance a_iso and winding to central limb insulation a_1 (c.f. Fig. 2). So the winding design is a four dimensional problem with interactive restrictions of each other. In high frequency magnetics, not only the winding capacitance C_w, but also the capacitance due to the core C_cw and shield C_s should be taken into account [8–11]. For the ETD shape core, the capacitance between the winding and the side limb C_cw2 becomes very serious when the volume of the winding is large enough. Unlike the formation of central limb capacitance C_cw1 and yoke capacitance C_cw3, there is no bobbin between the side limb core and the winding. So the impact of the side limb is easy to be neglected and causes a huge C_cw2 in some cases. In general, a comprehensive winding design considering all the problems is important for high frequency ac inductor.

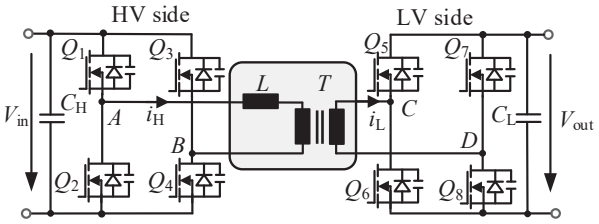


Fig. 1. Schematic of a Dual active bridge converter (DAB).

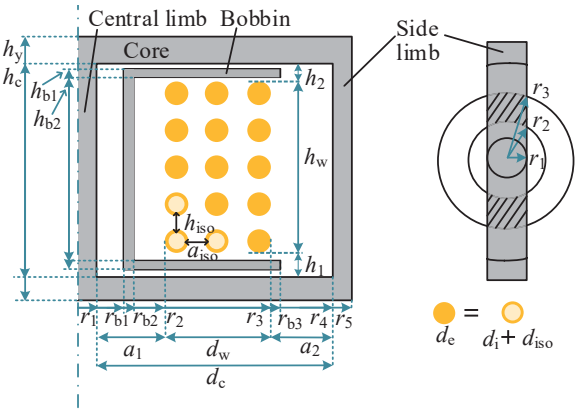


Fig. 2. Inductor cross section, top view and structure parameters.

In this paper, analytical formulas considering the side limb capacitance C_cw2 and yoke capacitance C_cw3 are derived and verified by both FEM and experimental results, making it possible for a local optimization on the core-related capacitance C_w. Further, a winding design method for the ac resistance and capacitance is proposed. Finally, inductors for a DAB prototype is designed with the proposed method and experimental results are presented.

II. Winding Ac Resistance Modeling and Minimization

The ac resistance R_ac is determined by Dowell and it is a function of number of layers p and the penetration ratio $\triangle$ [12, 13]:

$$R_\mathrm{ac} = f_0(p, \triangle) = R_\mathrm{dc} F_\mathrm{r} = R_\mathrm{dc} \triangle [\nu_1 + \frac{2}{3}(p^2 - 1)\nu_2], \quad (1)$$

978-1-5386-1180-7/18/$31.00 ©2018 IEEE

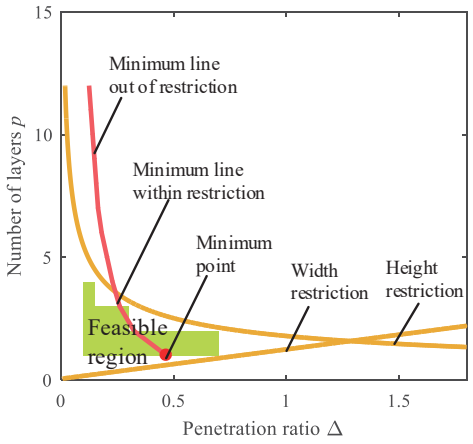


Fig. 3. Inductor winding design map of the ac resistance.

where

$$\triangle = \frac{d_{\mathrm{i}}}{\delta}, \tag{2}$$

R_{dc} is the dc resistance, F_{r} is the ac resistance ratio, d_{i} is the diameter of conductor, δ is the skin depth, ν_1 and ν_2 are coefficients, which are the function of $\triangle$. For an inductor application, although the accuracy of the expression is not guaranteed [14, 15], the relative relationship of ac resistance for each (p, $\triangle$) case still has a reference value and it is comparable. Then if the number of layers m is also decided, there is an optimum Δ_{opt} for a minimum ac winding resistance [16–20]. The corresponding optimum diameter is then derived with Δ_{opt} and δ. The design method in [21] uses the core window width and the height as restrictions (Fig. 3):

$$d_{\mathrm{c}} = pd_{\mathrm{i}} + (p-1)a_{\mathrm{iso}} + a_1 + a_2, \tag{3}$$

$$h_{\mathrm{c}} = td_{\mathrm{i}} + (t-1)h_{\mathrm{iso}} + h_1 + h_2, \tag{4}$$

where d_{c}, h_{c} is the width and height of the window, t is the number of conductors per layer, d_{i} is the conductor diameter, a_{iso} and h_{iso} are the layer isolation in width and height direction, a_1, a_2, h_1, h_2 is the creep distances between the core and the winding in width and height directions, separately.

III. Winding Parasitic Capacitance Modeling

Neglecting the turn to turn capacitance in multi-layer windings, there are four kinds of parasitic capacitances due to the structure of the core and winding: inter-layer capacitance C_{ll}, central limb capacitance C_{cw1}, side limb capacitance C_{cw2}, and top and bottom yoke capacitance C_{cw3}.

The parasitic capacitance of the multi-layer winding can be modeled by connecting the layer to layer capacitance C_{ll} [22]:

$$C_{\mathrm{w}} = k_{\mathrm{lc}} \cdot C_{\mathrm{ll}}(p-1)(\frac{2}{p})^2, \tag{5}$$

where k_{lc} is equal to 1/3 or 1/4 dependent on the wiring direction. C_{ll} is calculated by parallel plate capacitance:

$$C = k_{\mathrm{cw}} \cdot \varepsilon_0\varepsilon_{\mathrm{eq}}\frac{A_{\mathrm{pla}}}{d} = k_{\mathrm{cw}} \cdot \varepsilon_0\varepsilon_{\mathrm{eq}}\frac{2\pi h(r+d/2)}{d}, \tag{6}$$

where:

$$h = h_{\mathrm{w}}, \quad d = d_{\mathrm{eff}}, \quad r = r_{\mathrm{eq}} - d/2, \quad \varepsilon_{\mathrm{eq}} = \varepsilon_i, \tag{7}$$

$k_{\mathrm{cw}} = 1$ is the weigh factor, h_{w} is the height of the winding, $d_{\mathrm{eff}} = (a_{\mathrm{iso}} - 2r_{\mathrm{iso}}) + d_{\mathrm{e}} - 1.15d_{\mathrm{i}} + 0.26(h_{\mathrm{iso}} + d_{\mathrm{i}})$ is the effective distance between layers [23], ε_i is the effective permittivity, separately.

The central limb capacitance C_{cw10} can also be predicted with equation (6) by the parameter assignment [9]:

$$h = h_c, \quad d = r_2 - r_1 + d_{\mathrm{e}}/2, \quad r = r_1, \quad \varepsilon_{\mathrm{eq}} = \varepsilon_{\mathrm{b1}}, \tag{8}$$

where $k_{\mathrm{cw}} = 1$, h_{c} is the height of the window, d is distance from inner layer to the core, r is from inner core to axis, $\varepsilon_{\mathrm{b1}}$ are equivalent relative permittivity.

If the layer p increases, the outer radius of the winding r_3 may be very close to the inner radius of side limb core r_4. The related side limb capacitance C_{cw20} begins to increase and can be predicted with the same equation (6) with:

$$h = h_c, \quad d = r_4 - r_3 + d_{\mathrm{e}}/2, \quad r = r_3, \quad \varepsilon_{\mathrm{eq}} = \varepsilon_{\mathrm{b2}}, \tag{9}$$

$\varepsilon_{\mathrm{b2}}$ here differs from $\varepsilon_{\mathrm{b1}}$ for the C_{cw10}, for ETD core, there is no bobbin between outer winding and side limb. The weight factor k_{cw} for the ETD core refers to the ERXP simulation model in [24], it determines the impact on the side limb core through a top-view circle r_3 percentage, and can be simplified to:

$$k_{\mathrm{cw}} \approx 4r_1/(2\pi r_3) \approx 4r_1/(\pi r_1 + \pi r_4). \tag{10}$$

The factor calculation formula can be changed according to different core structures.

The top and bottom yoke capacitance C_{cw30} is also increased with layer number p, with $k_{\mathrm{cw}} = 1$ and:

$$A_{\mathrm{pla}} \approx 4r_1(r_3 - r_2), \quad d = (h_{\mathrm{c}} - h_{\mathrm{w}})/2, \quad \varepsilon_{\mathrm{eq}} = \varepsilon_{\mathrm{b3}}, \tag{11}$$

where $\varepsilon_{\mathrm{b3}}$ is equivalent permittivity.

Assume that the winding is numbered from 1 to N according to wiring order, the potential of each turn is from U_1 to U_{N}, U_0 is voltage difference in each layer, and the potential of the core is U_{C}. The difference of them is U_{d}:

$$U_{\mathrm{d}} = U_1 - U_{\mathrm{C}}. \tag{12}$$

The voltage ratio is defined as $k_{\mathrm{U}} = U_{\mathrm{d}}/U_0$. The equivalent core-related capacitance C_{cw} can be gain by expressing the energy stored in the system, as is given in Appendix A. The total capacitance C_{ind} is the sum of C_{w} and C_{cw}:

$$\begin{aligned} C_{\mathrm{ind}} &= C_{\mathrm{w}} + C_{\mathrm{cw1}} + C_{\mathrm{cw2}} + C_{\mathrm{cw3}} \\ &= C_{\mathrm{w}} + \underbrace{k_{\mathrm{c1}} \cdot C_{\mathrm{cw10}} + k_{\mathrm{c2}} \cdot C_{\mathrm{cw20}} + k_{\mathrm{c3}} \cdot C_{\mathrm{cw30}}}_{C_{\mathrm{cw}}}, \end{aligned} \tag{13}$$

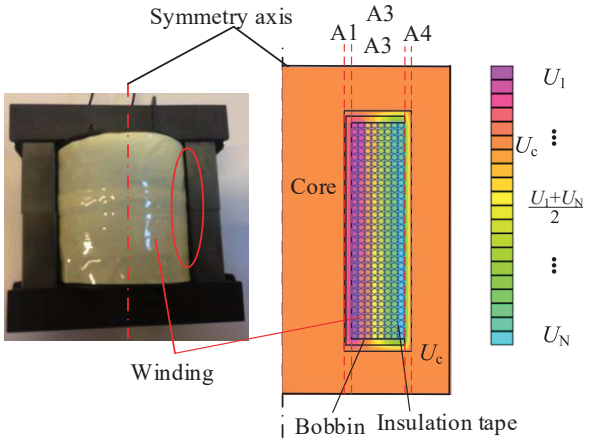
with:

$$k_{\mathrm{c1}} = \frac{3k_{\mathrm{U}}^2 + 3k_{\mathrm{U}} + 1}{3p^2}, \tag{14}$$

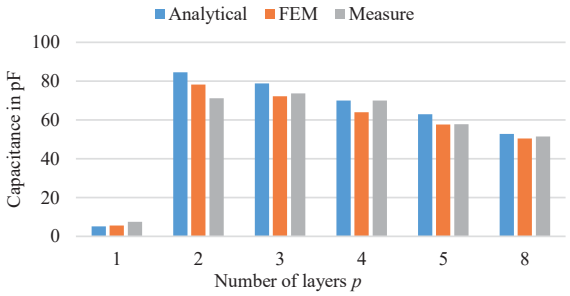
$$k_{\mathrm{c2}} = \frac{3k_{\mathrm{U}}^2 + (6p-3)k_{\mathrm{U}} + (3p^2 - 3p + 1)}{3p^2}, \tag{15}$$

$$k_{\mathrm{c3}} = \frac{6k_{\mathrm{U}}^2 + 6pk_{\mathrm{U}} + (2p^2 - p + 2)}{3p^2}. \tag{16}$$

The core of the inductor is floating, so the potential U_{C} is between U_1 to U_{N}, which means $-p < k_{\mathrm{U}} < 0$. For normal situation, the inner side of the winding is more close to the central limb core, thus the range of k_{U} can narrow to $-p/2 < k_{\mathrm{U}} < 0$. The determination of exact value of k_{U} is difficult and can only be extracted by experiment or finite element



(a) Prototype 8 and its 2D FEM simulation of the electric potential.



(b) Total capacitance C_{ind}, floating core

Fig. 4. The analytical, simulation, and experimental results of the capacitance of the prototypes with different number of layers p.

TABLE I
PROTOTYPE WINDING SPECIFICATION OF P1 TO P8

Parameters	Value	Units
Core type	ETD 59/31/22	
Core material	N97	
Bobbin type	B66398	
Number of layers p	1, 2, 3, 4, 5, 8	
Turns in one layer t	34	
Winding diameter d_{i}	1	mm

simulation. On the other hand, C_{cw} is a quadratic function of k_{U} and the rate of change is not large in this range, so $k_{\mathrm{U}} = -p/4$ is assumed, and is verified below.

A series of inductor prototypes are built and tested, named P1, P2, ... P5 and P8 to verify the impact of C_{cw}. They are all with the same configuration except different number of layers p, and the detailed information is shown in Table I. A comparison is given in Fig. 4. The experimental results are extracted with the resonant method performed by the Keysight impedance analyzer E4990A [9, 25]. In Fig. 4(a), the potential of the core in simulation is close to 1/4 of (U_{N}-U_1), which verifies the assumption. The analytical and simulation error may due to the simplification of the model structure, the

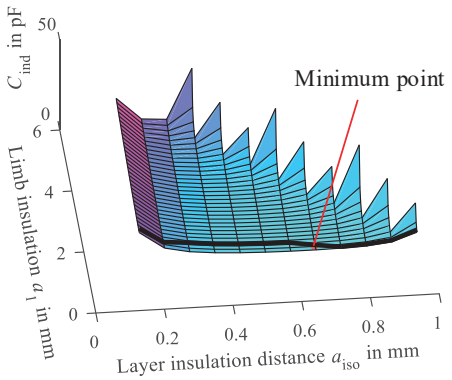


Fig. 5. Total capacitance C versus a_1 and a_{iso}, the iteration minimum result is marked with a red filled circle.

disordered winding arrangement of prototype and impact of the core, and it is in a reasonable range.

IV. Winding Parasitic Capacitance Optimization

Unlike ac resistance, there are no comparable amount of analytical tools for the control or optimization of winding capacitance. This is due to that the total capacitance C_{ind} is more structure-dependent and it is mainly dependent on four variables: number of layer p, penetration ratio $\triangle$, layer insulation a_{iso} and winding to central limb distance a_1.

On one hand, the importance of the winding position is usually ignored and a_1 is close to the bobbin outside radius r_{b2}, meaning directly wrapping the first layer on the bobbin. However, a careful selection of a_1 will be helpful to reduce the core-related capacitance C_{cw}. C_{cw} includes three parts, if the other parameters are fixed, the center limb capacitance C_{cw1} decreases with the increase of a_1, the side limb capacitance C_{cw2} increases with a_1, and the yoke capacitance C_{cw2} keeps stable. If the total creep distance $a_1 + a_2$ is fixed, an optimum a_1 can be found, which leads to a minimum C_{cw}. If $a_{1\mathrm{opt}}$ is always chosen for the calculation C_{cw} under each a_{w}, then $a_{1\mathrm{opt}}$ becomes a function of a_{w}, the local optimum minimum C_{cwopt} then becomes a function of total winding core distance a_{w}: $C_{\mathrm{cwopt}} = f_1(a_{\mathrm{w}})$.

On the other hand, for a fixed layer p and penetration ratio $\triangle$, the ac resistance with equation (1) can be calculated, and a_{w} is also fixed. But the winding capacitance still changes with a_{iso}: $C_{\mathrm{w}} = f_2(a_{\mathrm{iso}})$. For the core-related capacitance, considering the relationship between a_1, a_{iso} and a_{w} with equation (3), there is $C_{\mathrm{cw}} = f_3(a_1, a_{\mathrm{iso}})$. Combining the f_2 and f_3 we obtain a relationship with a_1, a_{iso} and total capacitance C_{ind} in each (p, $\triangle$) case. This is an optimization problem of two-variable functions:

$$C_{\mathrm{ind}} = f_4(a_1, a_{\mathrm{iso}}). \tag{17}$$

With the $a_{1\mathrm{opt}}$ and a_{isoopt}, the solution of minimum C_{ind} can be obtained, as illustrated in Fig. 5, where $p = 7$ and $\triangle = 0.2$. The other constructions are the same as given in Table I. The hidden part of Fig. 5 is when $a_{1\mathrm{opt}}$ and a_{isoopt} are large and lead to $a_{\mathrm{isoopt}} < 0$.

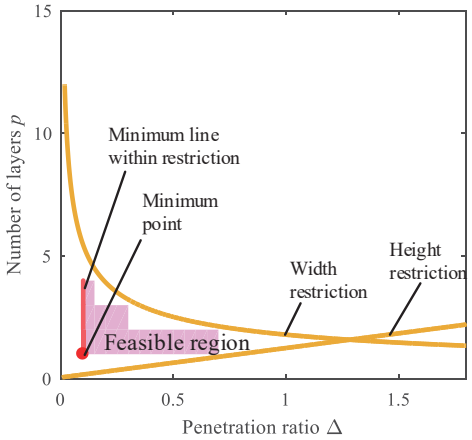


Fig. 6. Inductor winding design map of the parasitic capacitance.

TABLE II
WINDING DESIGN INPUTS

Parameters	Value	Units
Core type	ETD 44/22/15	
Core material	N87	
Bobbin type	B66366	
Number of turns p	12	
Number of strands k_{str}	90	
Diameter restrictions, minimum torrance value:		
Inner layer width a_{iso}	0.074	mm
Inner winding and core width a_1	1.4	mm
Outer winding and core width a_2	1.4	mm
Inner layer height h_{iso}	0.074	mm
Inner winding and core height h_1	1.4	mm
Outer winding and core height h_2	1.4	mm

Finally, with the ($a_{1\mathrm{opt}}$, a_{isoopt}) in each (p, $\triangle$) case, the minimum C_{ind} in the (p, $\triangle$) coordinate can be obtained in Fig. 6. The four dimensional optimization problem (p, $\triangle$, $a_{1\mathrm{opt}}$, a_{isoopt}) is now in two dimensions (p, $\triangle$). With the boundary of equation (3) and (4), the feasible area is illustrated and the global minimum point can be found, as plotted in a red point.

V. Optimal Winding Design Considering Ac Resistance and Parasitic Capacitance

Inductors for a 100 kHz dual active bridge prototype is designed to illustrate the design method. The core, bobbin, winding, and diameter restrictions as design input are illustrated in Table II. The capacitance C_{ind} and ac resistance R_{ac} in (p, $\triangle$) coordinate is given in Fig. 3 and 6. The relationship between C_{ind} and R_{ac} is plotted in Fig. 7 and the Pareto front is with red line. It is easy to find that all the points on the Pareto front is shown with the $p = 1$ situation. The slope of the front is not quite large, so the capacitance of the point at the right side on the line and at the left side are all in an

TABLE III
WINDING DESIGN OUTPUTS

Parameters	Value	Units
Number of layers p	1	
Turns in one layer t	12	
Winding diameter d_{i} output	0.15	mm
Winding diameter d_{i} chosen	0.20	mm
Inner layer distance a_{iso}	0	mm
Inner winding and core distance a_1	3.92	mm
Winding resistance R_{ac} @ 100 kHz	12.6	mΩ
Total Capacitance C	2.1	pF

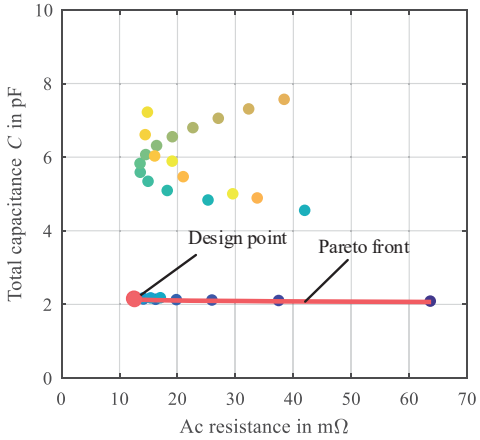
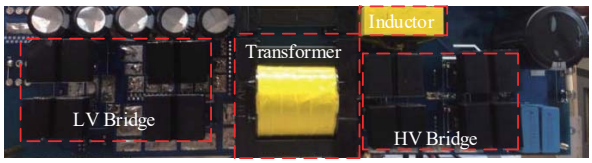


Fig. 7. Pareto optimization of ac resistance and total capacitance.

acceptable range. However, the ac resistance of the left side point is reduced dramatically, and it is chosen as the design point, as illustrated in the red point. The final design output is illustrated in Table III. The self capacitance of Litz wire is not considered, however, it is fair to do the optimization design with the same type of Litz. A smaller strand diameter (90 × 0.10 mm) is chosen with the increased ac resistance and reduced capacitance with only a one layer and smaller self capacitance. For comparison, a design with the same core, bobbin but larger strand diameter (6 × 15 × 0.2 mm) is compared. Unlike the optimum design using one bundle with 6 strands 15 × 0.2 mm twisted together, the comparable one uses six one bundle Litz wires winding vertically in parallel, and directly attached on the bobbin, meaning $a_1 = r_{\mathrm{b2}} - r_1$, leading to 4 layers with a_{iso} = 0.11 mm. The designed inductor has a measured total capacitance of 1.9 pF, while the comparison design is 80.8 pF, which means 42.5 times increase of capacitance.

The inductor is put on the high voltage side of the DAB, as it is given in Fig. 8. The experimental results in the voltage balanced operation is in Fig. 9. v_{AB}, v_{CD} and i_{L} are HV and LV side voltages and HV side current of the the optimum inductor, $i_{\mathrm{L,c}}$ is HV side current of the compared inductor.

(a) Sampling and Control Board



(b) Power Board

Fig. 8. Inductor in a 100 kHz dual active bridge protptype.

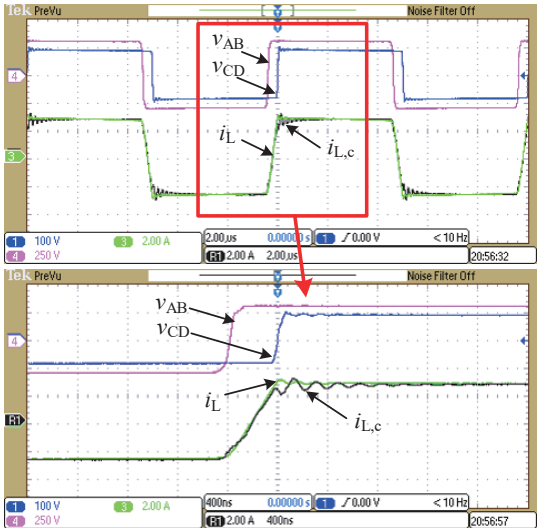


Fig. 9. Waveform of the voltage balance operation, with a zoom view below.

Both situations are with the same input voltage of 302.5V, while the optimum one has the total system efficiency of 97.0%, and comparison one with 96.8%, separately. From the comparison, the current ringing of the small-parametric-capacitance inductor is significantly reduced, which is helpful for the increase of efficiency.

VI. Conclusions

An expression of the parasitic capacitance of the inductor is derived considering the core-related capacitance. Six prototypes have been built and the analytical, FEM simulation, and experimental results illustrate the importance of core-related capacitance. An ac resistance and parasitic capacitance optimization method is proposed and experimentally verified in this paper for inductor winding design. With a local optimization of core-related capacitance, the proposed method compresses a four dimensional optimization to a two dimensional problem. An inductor winding design case for a DAB converter is discussed. It results in 42.5 times parasitic capacitance reduction, a small current ringing and an efficiency increase with the proposed optimization method, compared to the alternative design.

Appendix A
Derivation of the Core-Related Capacitance

For two conductive layers, if the voltage difference between them is constant and a parallel plate model is considered, the layer capacitance C_{ll} can be calculated easily with equation (6). If a linear potential distribution is assumed along the layer, the voltage difference at one side is U_{D1} and at the other side is U_{D2}, the total system energy is [23]:

$$W = \frac{C_l}{6}(U_{D1}^2 + U_{D1}U_{D2} + U_{D2}^2). \tag{A.1}$$

Assume a linear voltage distribution along the winding and core, the energy of A1 to A3 region in Fig. 4(a) can be expressed as W_1 to W_3:

$$W_1 = C_{\mathrm{cw10}}\frac{U_{\mathrm{d}}^2 + U_{\mathrm{d}}(U_{\mathrm{d}} + U_0) + (U_{\mathrm{d}} + U_0)^2}{6}, \tag{A.2}$$

$$\begin{aligned} W_2 =& C_{\mathrm{cw20}}\frac{[U_{\mathrm{d}} + (p-1)U_0]^2 + (U_{\mathrm{d}} + pU_0)^2}{6} \\ &+ \frac{[U_{\mathrm{d}} + (p-1)U_0](U_{\mathrm{d}} + pU_0)}{6}, \end{aligned} \tag{A.3}$$

$$\begin{aligned} W_3 =& C_{\mathrm{cw30}}\frac{U_{\mathrm{d}}^2 + U_{\mathrm{d}}(U_{\mathrm{d}} + pU_0) + (U_{\mathrm{d}} + pU_0)^2}{6} \\ &+ \frac{(U_{\mathrm{d}} + U_0)^2 + [U_{\mathrm{d}} + (p-1)U_0]^2}{6} \\ &+ \frac{(U_{\mathrm{d}} + U_0)[U_{\mathrm{d}} + (p-1)U_0]}{6}. \end{aligned} \tag{A.4}$$

On the other hand, the energy in A1 to A3 can be expressed as the core-related capacitance C_{cw}:

$$W_{\mathrm{cw}} = \frac{C_{\mathrm{cw}}}{2}(pU_0)^2. \tag{A.5}$$

Equaling $W_{\mathrm{cw}} = W_1 + W_2 + W_3$ and compare the factors of C_{cw10} to C_{cw30}, equation (14) to (16) can be obtained as results.

References

[1] R. De Doncker, D. Divan, and M. Kheraluwala, "A three-phase soft-switched high-power-density DC/dc converter for high-power applications," *IEEE Trans. Ind. Appl.*, vol. 27, no. 1, pp. 63–73, Jan. 1991.

[2] G. Ortiz, C. Gammeter, J. Kolar, *et al.*, "Mixed mosfet-igbt bridge for high-efficient medium-frequency dual-active-bridge converter in solid state transformers," in *Proc. IEEE Wksp. Control Model. Power Electron (COMPEL)*, 2013, pp. 1–8.

[3] J.-P. Vandelac and P. Ziogas, "A novel approach for minimizing high-frequency transformer copper losses," *IEEE Trans. Power Electron.*, vol. 3, no. 3, pp. 266–277, Jul. 1988.

[4] C. Sullivan, "Optimal choice for number of strands in a litz-wire transformer winding," *IEEE Trans. Power Electron.*, vol. 14, no. 2, pp. 283–291, Mar. 1999.

[5] J. Biela and J. W. Kolar, "Using transformer parasitics for resonant converters-a review of the calculation of the stray capacitance of transformers," *IEEE Trans. Ind. Appl.*, vol. 44, no. 1, pp. 223–233, Jan. 2008.

[6] P. Thummala, H. Schneider, Z. Zhang, *et al.*, "Investigation of transformer winding architectures for high-voltage (2.5 kV) capacitor charging and discharging applications," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5786–5796, Aug. 2016.

[7] M. A. Saket, M. Ordonez, and N. Shafiei, "Planar transformers with near-zero common-mode noise for flyback and forward converters," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1554–1571, Feb. 2018.

[8] Q. Yu and T. W. Holmes, "A study on stray capacitance modeling of inductors by using the finite element method," *IEEE Trans. Electromagn. Compat.*, vol. 43, no. 1, pp. 88–93, 2001.

[9] L. Dalessandro, F. da Silveira Cavalcante, and J. W. Kolar, "Self-capacitance of high-voltage transformers," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 2081–2092, Sep. 2007.

[10] J Biela, D Bortis, and J. Kolar, "Modeling of pulse transformers with parallel-and non-parallel-plate windings for power modulators," *IEEE Trans. Dielect. Elect. Insulation*, vol. 14, no. 4, p. 1, Aug. 2007.

[11] X. Liu, Y. Wang, J. Zhu, *et al.*, "Calculation of capacitance in high-frequency transformer windings," *IEEE Trans. Magn.*, vol. 52, no. 7, pp. 1–4, Jul. 2016.

[12] P. Dowell, "Effects of eddy currents in transformer windings," *Proc. Inst. Electr. Eng.*, vol. 113, no. 8, pp. 1387–1394, Aug. 1966.

[13] M. K. Kazimierczuk, *High-frequency magnetic components*. West Sussex, U.K.: John Wiley & Sons, 2009.

[14] P. Wallmeier, "Improved analytical modeling of conductive losses in gapped high-frequency inductors," *IEEE Trans. Ind. Appl.*, vol. 37, no. 4, pp. 1045–1054, Jul. 2001.

[15] J. D. Pollock, "Optimizing winding designs for high-frequency magnetic components," PhD thesis, NH, U.S.A.: Dartmouth College, 2008.

[16] M. Perry, "Multiple layer series connected winding design for minimum losses," *IEEE Trans. Power App. Syst.*, vol. PAS-98, no. 1, pp. 116–123, 1979.

[17] B. Carsten, "High frequency conductor losses in switch-mode magnetics," in *Proc. HPFC*, 1986, pp. 155–176.

[18] W. G. Hurley and W. H. Wölfle, *Transformers and inductors for power electronics: Theory, design and applications*. John Wiley & Sons, 2013.

[19] R. Wojda and M. K. Kazimierczuk, "Winding resistance of litz-wire and multi-strand inductors," *IET Power Electron.*, vol. 5, no. 2, pp. 257–268, 2012.

[20] K. V. Iyer, K. Basu, W. P. Robbins, *et al.*, "Determination of the optimal thickness for a multi-layer transformer winding," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2013, pp. 3738–3741.

[21] Z. Shen, Z. Li, L. Jin, *et al.*, "An ac resistance optimization method applicable for inductor and transformer windings with full layers and partial layers," in *Proc. IEEE Appl. Power Electron. Conf. Exposit.*, IEEE, 2017, pp. 2542–2548.

[22] H. Zuhrt, "Simple approximate formulas for the self capacitance of multi-layer coils," *Elekrotech. Zeitschrift*, vol. 55, pp. 662–665, Jul. 1934.

[23] E. Snellinq, *Softferrites: Properties and applications*. Butterwortlm, 1988.

[24] A. Hoke and C. Sullivan, "An improved two-dimensional numerical modeling method for e-core transformers," in *Proc. IEEE Appl. Power Electron. Conf. Exposit.*, vol. 1, 2002, pp. 151–157.

[25] H. Y. Lu, J. G. Zhu, and S. Y. R. Hui, "Experimental determination of stray capacitances in high frequency transformers," *IEEE Trans. Power Electron.*, vol. 18, no. 5, pp. 1105–1112, Sep. 2003.