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A Compact Integrated High-Voltage Pulser Insensitive to Supply Transients for 3D Miniature Ultrasound Probes

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***Abstract*—In this paper, a compact high-voltage (HV) transmit circuit for dense 2D transducer arrays used in 3D ultrasonic imaging systems is presented. Stringent area requirements are addressed by a unipolar pulser with embedded transmit/receive switch. Combined with a capacitive HV level shifter, it forms the ultrasonic HV transmit circuit with the lowest reported HV transistor count and area without any static power consumption. The balanced latched-based level shifter implementation makes the design insensitive to transients on the HV supply caused by pulsing, facilitating application in probes with limited local supply decoupling, such as imaging catheters. Favorable scaling through resource sharing benefits massively arrayed architectures while preserving full individual functionality. A prototype of 8 x 9 elements was fabricated in TSMC 0.18 μm HV BCD technology and a 160 μm x 160 μm PZT transducer matrix is manufactured on the chip. The system is designed to drive 65 V peak-to-peak pulses on 2 pF transducer capacitance and hardware sharing of 6 elements allows for an area of only 0.008 mm^2 per element. Electrical characterization as well as acoustic results obtained with the 6 MHz central frequency transducer are demonstrated.**

***Index Terms*—BCD technology, CMOS, high-voltage level shifter, high-voltage pulser, PZT transducer, supply transient, transmit/receive switching, ultrasound**

I. Introduction

Ultrasonic imaging is widely used in medicine for its versatile and nondestructive nature. In recent years, integrated circuit research is working on enabling further applications and, at the example of catheter-based devices for intra-cardiac echocardiography (ICE), moving from 2D to 3D visualization [1]. A major challenge in this transition is posed by the necessity of 2D transducer arrays with around 1000 elements and small pitches in the order of 100 to 200 μm to achieve sufficient image quality. To maximize the imaging aperture within probe tips with around 3 mm diameter, circuitry to transmit pressure waves and receive echoes on the same transducer need to be matched to the element area.

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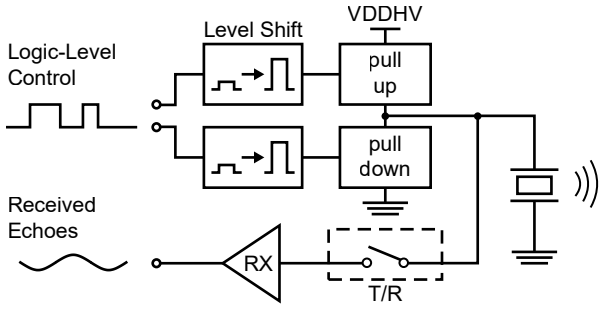

Fig. 1. Common ultrasound system with level shifters, a pulser and transmit/receive (T/R) switch to receive electronics (RX).

For transducer actuation, small circuits have been achieved through the use of standard CMOS devices [2], [3]. These however can not provide sufficient signal to noise ratio (SNR) at relevant imaging depths due to limited output pressure and the attenuation of ultrasound in the medium. Therefore, high-voltage (HV) transistors are typically applied despite their large size and transmit/receive (T/R) switches are used to protect the receive path from high potential differences [4] - [6]. A common topology is shown in Fig. 1. While a class-A pulser topology as in [7] is area saving, the associated large static power consumption and tissue heating are undesirable and push-pull architectures are more common. These can be unipolar [8], [9] or bipolar [4] - [6], leading to a trade-off between less out-of-band energy for bipolar pulses at the expense of several more HV transistors.

The pull-up path is typically implemented with a HV PMOS and a HV level shifter is required to drive from logic supply levels. The voltage gap can be bridged by HV devices such as transistors [4], [8] or capacitors [10], the latter being preferable in terms of area but more sensitive to HV supply transients preventing regular operation, their cause being high transient pulsing currents and inductive loops, especially in catheter-based probes with limited local supply decoupling.

This work presents a unipolar pulser with an embedded T/R switch and a capacitive HV level shifter. The architecture is designed for beneficial scaling with large arrays and employs a latch-based high-side topology that enables pulsing in the presence of significant HV supply transients. The system is designed for driving a 160 μm x 160 μm PZT transducer element with a central frequency of 6 MHz but the presented techniques are also applicable to other transducers once scaled.

This paper is organized as follows. Section II presents the implementation of the transmit circuit, including the pulser, the HV level shifter and an on-chip regulator. Section III details

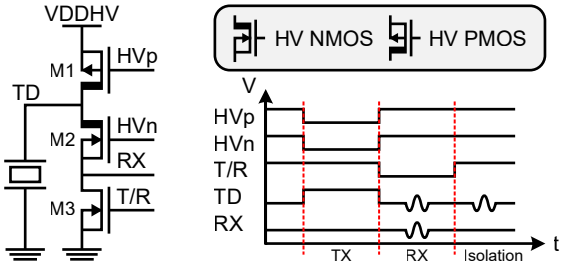

Fig. 2. Structure and timing of the proposed unipolar pulser.

the fabricated prototype and discusses electrical and acoustical measurements. The paper ends with a comparison to the prior art and a conclusion.

II. Circuit Implementation

A. High-Voltage Pulser

The proposed HV pulser design is shown in Fig. 2. The pull-up and pull-down paths are realized with a single HV transistor, M1 and M2, each, enabling compact unipolar pulsing. Similar to the bipolar design in [4], a T/R switch M3 is integrated in the pulser. This can be implemented as a smaller 5V transistor given that the HV NMOS shields the RX node from rising above its breakdown voltage.

The transducer array is on one side directly bonded to the ASIC on nodes TD while on the other side an aluminium foil provides a common low impedance path to ground. A transmit event is initiated by closing M1 and keeping M2 open, pulling the transducer to the HV supply. To end the pulse, the transducer is then pulled to ground by closing M2 and opening M1. During this repeatable transmission phase, M3 remains closed to prevent any damage to it. In the receive phase, M3 and M1 are open while M2 conducts incoming signals to the receive electronics.

B. High-Voltage Level Shifter

While HV transistors can sustain large source to drain potential differences, their gates typically still have a limited breakdown voltage. To enable logic-level control, the HV PMOS of the pulser therefore has to be driven with a level shifter. Fig. 3 shows two common ways to bridge such potential gaps with HV devices [4], [10].

The implementation with a HV transistor and a pull-up resistor provides a reliable and simple solution at the expense of using large HV devices. In addition, the pull-up resistor has to provide sufficient current to pull up the large pulser transistor with sufficient slew rate, leading to static power consumption. These issues can be addressed with a capacitor-based design given that the bridging components are smaller and can be implemented in metal layers. This however has issues with transients on the HV supply. The transistors can be kept within their safe operation range with additional diodes but the capacitors will maintain their charge and cause an undefined overdrive on the HV PMOS of the pulser or in the worst case flipping of the high-side latch formed between M3 and M4. In area-limited catheter-based probes with substantial inductive supply loops, this can be particularly problematic

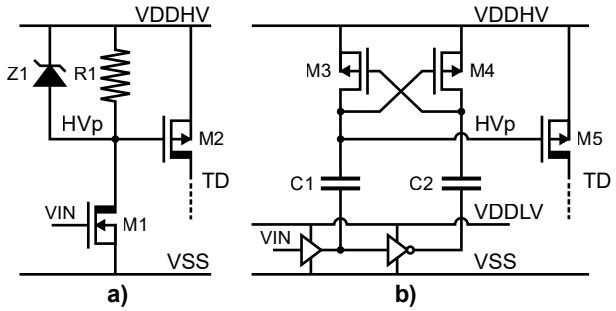

Fig. 3. Level shifter architectures based on a) HV transistors and b) capacitors.

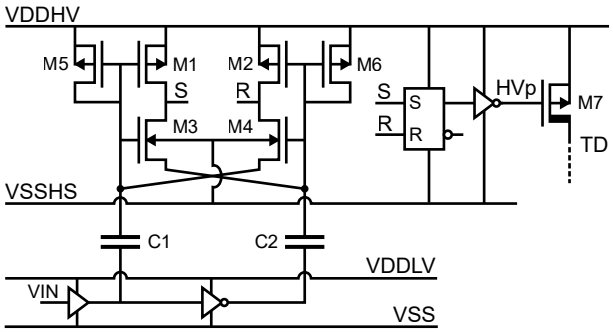

Fig. 4. Proposed supply transient insensitive, capacitor-based HV level shifter.

as the highest current transients on the HV supply occur during pulsing and dedicated transient-reduction techniques are difficult to integrate without area penalty or compromising the pulse shape.

Fig. 4 shows the proposed HV level shifter designed to enable a small footprint in large arrays without introducing supply transient sensitivity. The HV gap is still bridged with capacitors C1 and C2 but as the high-side circuitry poses a much smaller capacitive load than the large HV PMOS, their size can be reduced while maintaining the same attenuation towards the top plates. The capture circuit accepts differential signals from the low side while rejecting common mode inputs. A differential input signal causes transistors M1/M3 and M2/M4 to act like inverters towards the attached reset-set (RS) NAND latch. If the capacitor top plate potentials however get close to each other, as could happen in the event of ripple on the HV supply VDDHV, potentials at nodes R and S will remain high, leading the RS latch to maintain its output state. For a low common mode, transistors M1 and M2 directly connect the output of the capture circuit to VDDHV and a high common mode leads M3 and M4 to connect the common mode to the output. The high-side capture circuit serves the additional purpose of shielding the mismatch-sensitive latch with a less vulnerable structure, making the system more reliable than a direct high-side latch implementation. An output inverter is driving the HV PMOS transistor to present a small load to the latch and enable it to switch quickly.

Unlike its conventional counterpart, this capacitive level shifter maintains the overdrive on the pull-up device of the HV pulser through a driver in a separate supply domain provided by an on-chip regulator generating VSSHS. Capacitive coupling maintains the potential difference even in the event of HV supply transients and the HV PMOS conductivity therefore remains stable. The high-side transistors of the level

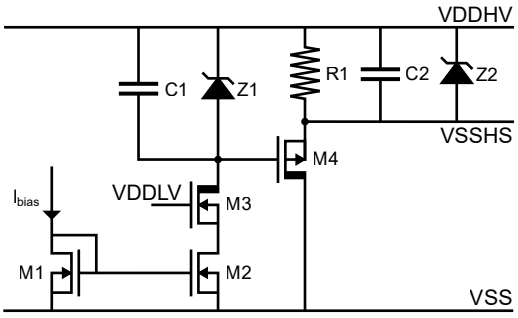

Fig. 5. Regulator for high-side low supply.

shifter can be small low voltage devices as they are shielded from the substrate potential with an isolation pocket. This pocket can be shared among multiple level shifters, making the device beneficial for arrayed architectures. Should HV supply transients cause potential differences between the capacitor top plates and gate regions of the low voltage transistors to become close to their breakdown limit, parasitic diodes of transistors M3 to M6 will dissipate excess charge.

C. High-Side Regulator

To provide the low voltage pocket for driving the HV PMOS of the pulser, VSSHS, a supply 5V lower than the HV supply, is generated on the periphery of the chip. The circuit is shared by the whole array and implemented as a basic HV PMOS source follower as shown in Fig. 5. The zener diode Z1 provides an input 5.6 V lower than the HV supply and is biased with a low current from a current mirror. The HV NMOS M3 shields the current mirror transistor M2 by preventing its drain to pass the low voltage supply, VDDLV, enabling a small footprint with a defined mirror ratio. VSSHS is therefore regulated to VDDHV $-$ 5.6 V $+$ $V_{th,p}$, $V_{th,p}$ being the HV PMOS threshold voltage.

The additional capacitor C1 provides a high frequency path to protect the gate of HV PMOS M4 in the event of HV supply transients. The decoupling capacitor C2 is sized to accommodate transient currents from driving the HV PMOS pulser transistors and can be as low as 100 pF for at least 20 consecutive pulses of all elements in this design. While the source follower can provide sufficient sinking capabilities for the application even with a low quiescent current, an additional zener diode Z2 is added for sourcing capabilities in case of an unexpected drop of the regulated output. The power consumption of the regulator is negligible compared to the level shifter and pulser operation.

III. Measurement Results

A prototype chip has been fabricated in TSMC 180 nm HV BCD technology. It features an array of 8 by 9 elements and contains a pulser as well as an analog frontend per element. The element pitch is 160 µm x 160 µm of which 27 % is occupied by transmit-related structures, leading to an area per element of 0.008 mm^2. The HV level shifters of 6 elements are laid out together to share their isolation ring for the high-side circuitry. Next to a 65 V high-voltage supply, a 5 V and a 1.8 V supply are used in the transmit circuitry to provide level

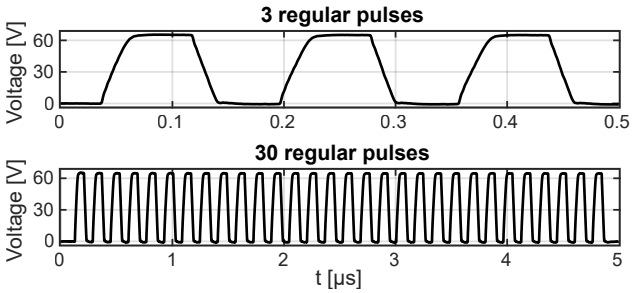

Fig. 6. Electrical measurement of 3 and 30 pulses from the proposed pulser.

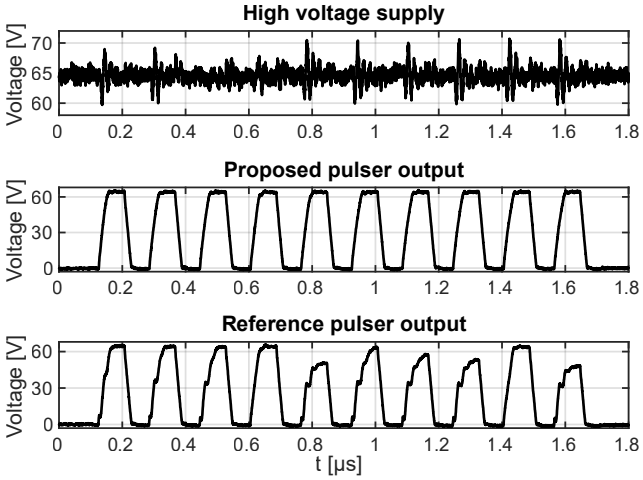

Fig. 7. Comparison of pulsing with the proposed and reference HV level shifter in the presence of supply ripple with 27 nH added supply inductance.

shifting and logic-level control options. The consumed power largely depends on the imaging mode and is dominated by dynamic power consumption of driving the transducer. On-chip 160 pF VDDHV decoupling is added according to an estimation of how much could be integrated in a full device.

Electrical characterization has been performed with a 2 pF capacitive load emulating the transducer capacitance. Different pulse sequences are evaluated and shown in Fig. 6. Next to the regular array with transducers, two separate pulsers are installed at the periphery of the chip. One performs HV level shifting with the proposed design as the rest of the array while the other implements a capacitive level shifting scheme as shown in Fig. 3 with added zener diodes to protect the high-side transistors against breakdown during measurement. This additional setup is used to study the behavior of the two circuits when subjected to the same HV supply transients. Since this prototype however is more than ten times smaller than an actual imaging device and therefore also has much lower transient pulsing current, a series inductor is inserted in the HV supply connection. Fig. 7 shows the supply variation caused by the 72 element array with an additional inductance of just 27 nH, implementing a low estimate of the supply ripple a full device could experience. The reference structure already shows variation of the pull-up path conductivity up to complete opening, resulting in an irregular pulse shape and imaging artifacts. The proposed circuit in contrast shows little variation from the regular pulse shape even at the highest tested inductance of 220 nH.

Acoustic verification of the chip is performed with a PZT

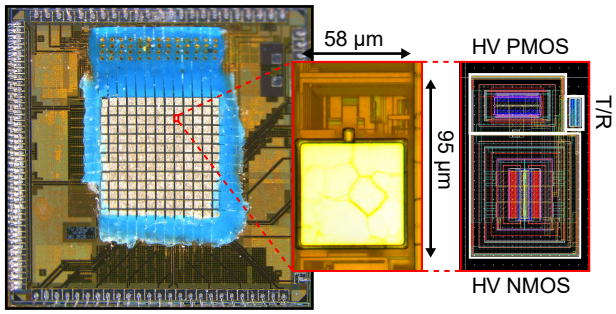

Fig. 8. Die micrograph with PZT transducer array and pulser inset as microscope image and layout view.

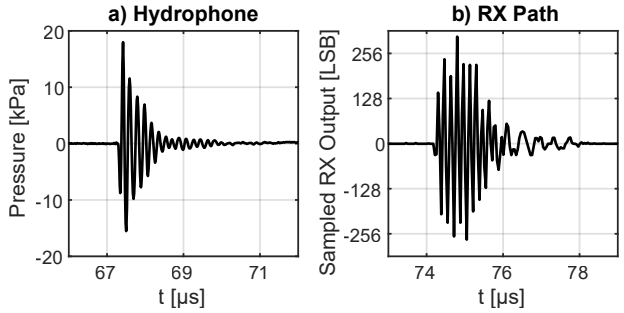

Fig. 9. One transmitted pulse measured by a hydrophone at about 10 cm distance in a) and reflected at about 5.5 cm from plate-reflector, received by the on-chip analog frontend and sampled at 24 MHz in b).

transducer matrix with a central frequency of 6 MHz. Fig. 8 shows a die photo with the array manufactured on top of the chip. Pulses with a peak amplitude of 65 V are driven from the on-chip pulsers to the bottom plate of the transducer elements posing a 2 pF capacitive load. The top plate of the transducer stack is in a final step connected to an aluminium ground foil that is shared by the whole array and connected to the transmit ground potential of the chip. Fig. 9 a) shows the pressure measurement obtained with a hydrophone in water, 10 cm in front of the surface of the assembly. A single pulse was fired from a row of nine elements and the waveform as well as a peak-to-peak pressure level of 34 kPa are in good agreement with our expectations. Verification of the ability to perform pulse-echo measurements is obtained in a second experiment in which a plate reflector is installed in front of the array. After transducer actuation, the embedded T/R switch is opened and received echoes are channeled to the included analog frontend [11]. The obtained results are subsequently sampled at 24 MHz and displayed in Fig. 9 b).

Table I compares the presented transmit circuitry to the prior art. It is expected that the HV level shifter can similarly be applied to bipolar pulsers and that realization of the transmit circuitry in an SOI technology as in [6] would lead to further area reduction due to smaller lateral HV device dimensions and enable higher driving voltages.

IV. Conclusion

A HV transmit circuit for catheter-based ultrasound probes is presented. A compact pulser with integrated T/R switch is driven with a novel HV level shifter that is insensitive to HV supply transients. The level shifter does not require any HV transistors, has no static power consumption and benefits from application in large 2D arrays as used for 3D ultrasonic imaging. Electrical and acoustical measurement results that verify the functionality and performance of the presented techniques have been presented.

TABLE I
Comparison with the Prior Art

	Integrated HV Transmitter			
	This Work	JSSC'20 [4]	JSSC'19 [6]	ESSCIRC'14 [9]
Technology	**180nm HV BCD**	180nm HV BCD	180nm HV SOI	180nm HV BCD-SOI
Max output	**65 V_{pp}**	60 V_{pp}	138 V_{pp}	100 V_{pp}
Pulse freq.	**6 MHz**	9 MHz	2 MHz	10 MHz
Load	**2 pF**	18 pF	Not Stated	23 pF
Area	**0.008 mm^2**	0.167 mm^2	0.04 mm^2 [a]	0.12 mm^2 [a]
# DMOS	**2**	10	10	3
# HV Diodes [b]	**0**	4	2	0
T/R embedded	**yes**	yes	no	no
Level shifter	**capacitive**	HV MOS	HV MOS	HV MOS
Pulser	**unipolar**	bipolar	bipolar	unipolar

[a] Not Including T/R. [b] Including zener diodes.

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