A low noise, low power dynamic amplifier with common mode detect and a low power, low noise comparator for pipelined SAR-ADC

by

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A thesis submitted in partial fulfillment for the degree of Master of Science

in the

Electronics Research Laboratory
Faculty of Electrical Engineering, Mathematics and Computer Science
DELFT UNIVERSITY OF TECHNOLOGY

August 2012

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Declaration of Authorship

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Abstract

Faculty of Electrical Engineering, Mathematics and Computer Science
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This thesis presents a high gain, low noise and low power dynamic residue amplifier and a low power, low noise dynamic comparator designed in TSMC 28nm process for a two step Pipelined SAR-ADC.

The cascoded integrator dynamic residue amplifier (CIDRA) achieves a gain of 30dB with THD of 47dB (11 mV pp input). The input referred noise across temperature and process corner is 55 μV and it operates at a frequency of 500MHz while the energy consumption is 390 fJ. The low power and low noise pseudo-latch preamp dynamic comparator (PLPDC) shows a delay of 250pSec for a differential input of 16 pV and consumes 91 fJ (current is 91 μA for 100 MHz clock) of energy. The input referred offset is 4 mV (σ).

Acknowledgements

I came to TUDelft with an intention to learn new trends and to get different perspective about micro electronic design. Through this dissertation with confidence I can say that I have successfully met those objectives. The reason for my confidence are the people who taught me, guided me and supported me. And I would like to acknowledge these people who helped me during my entire masters project.

First and foremost, I would like to thank my supervisor, Dr. Klaas Bult for providing me this wonderful opportunity to work at Broadcom amongst an outstanding group of engineers. His knowledge and experience in analog design was a source of inspiration for me to take up challenging project out of my comfort zone. This internship would not have been possible without him. Detailed discussions with him are responsible for most of my learnings in this project. It was really a pleasure and honour to work under his guidance.

I would like to thank my promoter, Prof. Dr. John Long for providing the support and valuable feedback on my thesis, and taking care of all the administrative tasks involved in doing a masters thesis. I sincerely appreciate the patience he has shown, while correcting mistakes in my thesis.

I would also like extend my special thanks to Dr. Frank van der Goes for the mentor-ship and encouragement. In spite of his busy schedule Frank was always enthusiastic for discussions. Those interesting discussions have immensely helped me to understand the system, solve the circuit level issues and make circuits compatible to the system.

I learnt from my supervisors, that the presentation of the idea is as important as the idea by itself. Their valuable feedbacks on my thesis have helped me present the circuits in a simple but in a effective manner.

I would like to thank all the engineers at Broadcom Bunnik, in particular Chris

Ward, Stefano Bozzola, Sijia Wang, Erol Arslan, Rohan Sehgal, Davide Vecchi, Jan Mulder, Jan Westra and Xiaodong Liu for numerous technical discussions and advices. And I consider myself very fortunate to have access to best of the best analog/RF design engineers. Els was always there for helping me out with all the administrative tasks, Thanks for being there.

The courses that I took during the first year of my masters were very inspirational, as they have shown me different approaches of thinking about analog design. Those courses have motivated me to think different. I would like to thank all the professors for those courses.

Leaving my family and coming to Delft was one of the hardest decision I made. It would be hard to put contributions of my parents (Prabhu and Sunanda) and my wife (Seema) in couple of lines. In simple words *"My parents are the living gods"*. And my wife has been the source of my strength which helped me go through tough times. Without their sacrifices, support, confidence, love and care this would never have happened. I am very thankful to my uncles (Basu kakar and Patted mamar), aunts (Nirmala aunty and Leela aunty) and Radhika for being there with my parents in my absence.

During the second year of my masters, I stayed with Th. M. Matton and J.W.Matton-Vermeulen. They have been very helpful and understanding, just like I would imagine my grand parents. I am very thankful to them for everything.

Finally I would like to thank all of my friends in India and Netherlands for all the support and encouragement. I have had very good memories with my friends which I will cherish for rest of my life.

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Chapter 1

Introduction

The analog to digital converter (ADC) is one of the key components in communication systems. The low-power operation of ADCs help to reduce heat dissipation, thus allowing the use of low-cost packages. Low-power operation also increases battery life in hand-held communication devices. In such a communication system, the sampling rate needs to be in the range of giga-samples per second (greater than 1GS/s [1]). Time-interleaved ADC which has multiple ADC lanes operating in parallel, can meet high speed requirements. The input is sampled by each ADC lane successively separated by an equal time interval. It implies that each ADC lane can sample at a lower frequency (hundreds of MHz) than the overall ADC sampling frequency (giga-hertz). Based on internal research, Broadcom proposed the specification for a single ADC lane as given in Table 1.1.

TABLE 1.1: Sample specifications of the ADC lane

Parameter	Specification	Units
Supply	1	Volts
Sampling clock	100	MHz
Peak-peak input signal	1.4	Volts
Reference voltage	0.7	Volts
ENOB	12	bits
Power	1	mW

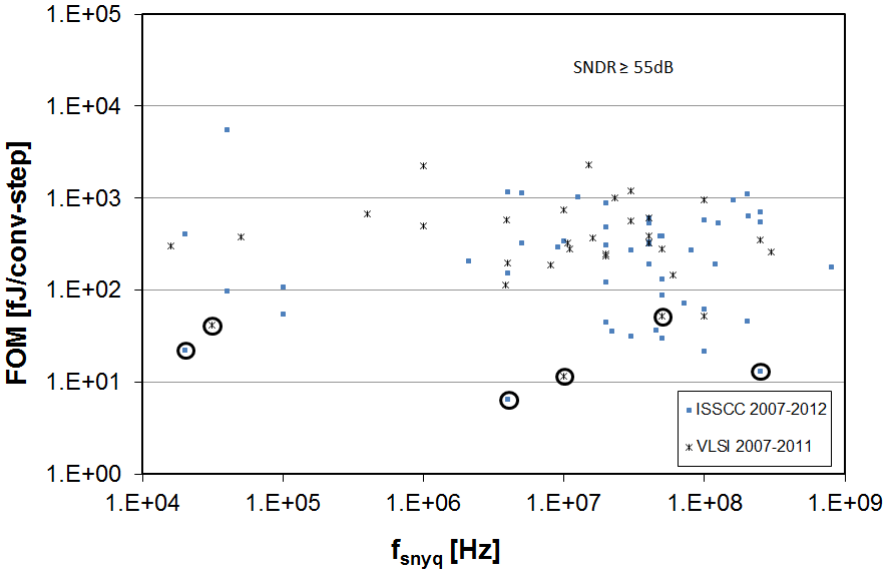

FIGURE 1.1: Figure of merit (FoM) verses Nyquist frequency (fsnyq) of recently published ADCs with SNDR≥55 [2]

1.1 ADC survey

As the required effective number of bits of the targeted ADC is 12, recently published ADCs with SNDR greater than 55dB were filtered from [2]. From the filtered list, low-power ADCs were considered for the implementation (eventually Broadcom intends to reach a figure of merit of 1fJ/conversion). Figure 1.1 shows figure of merit (FoM) vs Nyquist frequency (fsnyq) of recently published ADCs with an SNDR≥55dB. Some of the ADCs with a low FoM are also listed in Table 1.2 (highlighted with circles in Figure 1.1). It turns out that ADC types with a low FoM are mostly successive approximation (SAR) or pipelined SAR-ADCs. Hence, both SAR and pipelined SAR-ADCs were considered for the study, but to meet the desired specifications of the ADC shown in Table 1.1, a pipelined SAR-ADC is considered for implementation. The reasoning behind the selection is explained in Chapter 2.

In this design the pipelined SAR-ADC has two stages, and each stage is a SAR-ADC with a residue amplifier between them (see Figure 1.2). Apart from meeting noise and gain specifications, the residue amplifier should consume low energy (for this design, 400fJ). The concept of dynamic amplification has been used in the past

TABLE 1.2: ADCs which have achieved low figure of merit (FoM) [2]

	First author	ADC type	Sampling rate	SNDR (dB)	FoM (fJ/conversion)	Year of publication
1	Harpe	SAR	4MS/s	58.3	6.5	2012
2	Liu	SAR	100MS/s	56	11.6	2010
3	Verbruggen	Pipelined SAR	250MS/s	56	13.2	2012
4	Liu	SAR	100MS/s	60.29	21.9	2010
5	Walker	SAR	31.3kS/s	60.3	41.5	2011
6	Lee	Pipelined SAR	50MS/s	64.37	51.8	2010

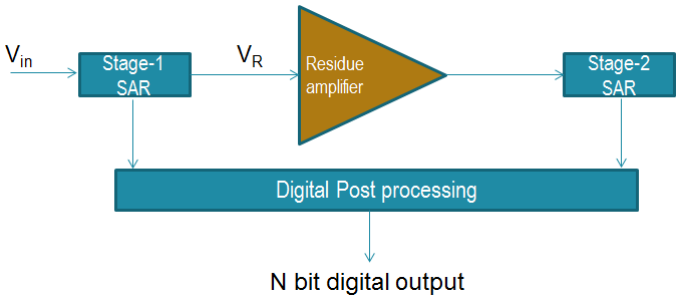

FIGURE 1.2: Block diagram of pipelined SAR-ADC

[3–5] for ADC designs. These ADCs consume power in the range of few mili-watts (1.4mW, 2.6mW and 1.7mW respectively). Hence, dynamic circuits have been chosen as a category of circuits for the study (more reasoning is provided in Chapter 3 and 4). In this dissertation, a low-noise, low-power cascoded-integrator dynamic residue amplifier (CIDRA) and a low-power, low-noise pseudo-latch preamp dynamic comparator (PLPDC) are designed for a pipelined SAR-ADC, to meet the proposed specification of Table 1.1.

1.2 Specifications of the residue amplifier and comparators

Let us assume that the ADC will be designed such that effective number of bits (ENOB) of the ADC is limited by thermal noise. The primary specifications for both amplifier and comparators are the input referred noise and the energy consumption. Considering an overall ENOB of 12 bits and 1mW power consumption, the budget for the input referred noise power and the energy consumption for the residue amplifier is shown in Table 1.3. Design of the residue amplifier with these specifications is the primary objective of this dissertation. Tables 1.4 and 1.5 show the input referred noise and energy consumption of the comparators for stage 1 and stage 2 respectively. The derivation of specifications for the sub-modules is presented in Chapter 2.

TABLE 1.3: Primary specifications of the residue amplifier

Parameter	Typical	Units
Gain	16	V/V
Noise @ input	50	μVolts
Energy/cycle	400	fJ
Settling period	1	nsec

TABLE 1.4: Primary specifications of the stage 1 comparator

Parameter	Typical	Units
Noise @ input	300	μVolts
Energy/cycle	100	fJ
Delay (LSB input)	250	psec

TABLE 1.5: Primary specifications of the stage 2 comparator

Parameter	Typical	Units
Noise @ input	450	μVolts
Delay (LSB input)	150	psec

1.3 Organization of this thesis

Chapter 2 gives brief overview of SAR and pipelined SAR-ADC architectures. Chapter 3 describes the operating modes of the transconductance amplifier along with a mathematical analysis of the noise and gain of this amplifier. Chapter 4 presents a detailed analysis of basic dynamic structures for voltage amplification using the integration principle. Chapter 4 also presents the dynamic amplifier and its design methodology. Chapter 5 gives a brief survey of dynamic comparators and presents a pseudo-latch based dynamic comparator and its design methodology. The configuration and calibration options for the dynamic amplifier and dynamic comparator are discussed in Chapter 6. Chapter 7 concludes this dissertation with specification compliance matrices.

Chapter 2

Overview of SAR-ADC and pipelined SAR-ADC

This chapter begins with definitions of ADC performance metrics. The subsequent section gives an introduction of the SAR-ADCs and its operation. The noise and energy requirements of the comparator for each cycle of the SAR-ADC are also analysed in section 2. Section three explains how a pipelined SAR architectures can reduce the energy consumption compared to just a SAR-ADC. The ADC concepts presented in this chapter is the result of a literature survey of recently published papers and discussion with my supervisors, they are not original ideas. These concepts are described to provide the motivation for the design of an amplifier and comparator. Specifications for the amplifier and comparators are derived in the final section.

2.1 ADC performance metrics

Differential non-linearity (DNL) is defined as the deviation of the step size in a non-ideal data converter from the ideal. If X_k is the transition point between

successive codes k-1 and k, then the DNL of the ADC can be expressed as

$$DNL(k) = ((X_{k+1}–X_k) - LSB)/LSB, \tag{2.1}$$

where least significant bit (LSB) is the ideal step size for that particular ADC [6].

Integral non-linearity (INL) is defined as the deviation of the actual transfer function from the straight line passing through the mid-points of the ideal input-output characteristic. The INL can be expressed as

$$INL(k) = \sum_{l=0}^{k} DNL(l). \tag{2.2}$$

However, usually it is measured as the deviation with respect to a best-fit line. The use of best-fit line corrects for any gain and offset errors, which are acceptable in many applications, and gives more information about harmonic distortion [6].

Total Harmonic Distortion (THD) is defined as the ratio of the root-mean-square (RMS) sum of all harmonic components to the RMS value of the fundamental in a certain frequency band. In decibels,

$$THD = 20\log \frac{\sqrt{\sum_{i=2}^{j} A^2(kf_{in})}}{A(f_{in})}, \tag{2.3}$$

where $A(kfin)$ is the amplitude of the harmonic tone present at the k-th multiple of input frequency, fin.

Third-order intermodulation distortion (IM3) appears for multi-tone input signal, as the non-linearity of the ADC causes mixing of the spectral components, generating tones at the sum and the difference of integer multiples of the input frequencies. For example, if the two input tones are at frequencies f1 and f2, then due to non-linearity of the ADC the two tones gets mixed. Two of the dominant

spectral components (assuming a symmetric, differential design) that result due to this mixing will be of frequencies (2f1-f2) and (2f2-f1). The IM3 is calculated as the ratio of the RMS sum of these two tones to RMS value of the fundamental (f1 and f2) [6].

Signal-to-noise and distortion ratio (SNDR) is the ratio of the power of the fundamental to the total noise and distortion power within a certain frequency band, and can be written as,

$$SNDR = 10\log\left(\frac{\text{signal power}}{\text{total noise and distortion power}}\right)\text{ dB}. \tag{2.4}$$

The SNDR depends on both the amplitude and the frequency of the signal. At low input levels, SNDR is limited by noise, while distortion dominates for higher signal levels.

Effective number of bits (ENOB) [8] of an ADC is a measure determined from the SNDR,

$$ENOB = \frac{SNDR - 1.76}{6.02}. \tag{2.5}$$

Figure of Merit (FoM) is a simple metric used to measure the energy efficiency of an ADC. While a number of FoMs have been proposed, the most popular one [7] takes into account the power consumption, signal bandwidth and the effective resolution of the ADC in the following way,

$$FoM = \frac{\text{Power Consumption}}{2^{ENOB}.min\{2BW, f_s\}}, \tag{2.6}$$

where BW is bandwidth and f_s is the sampling frequency.

The comparator has limited time to settle. The metastability occurs when the output of the comparator reaches a voltage that is not detected by the following logic. The metastable condition introduces errors in the system. The error probability (P(e)) [6] of comparator can be estimated in terms of the least significant

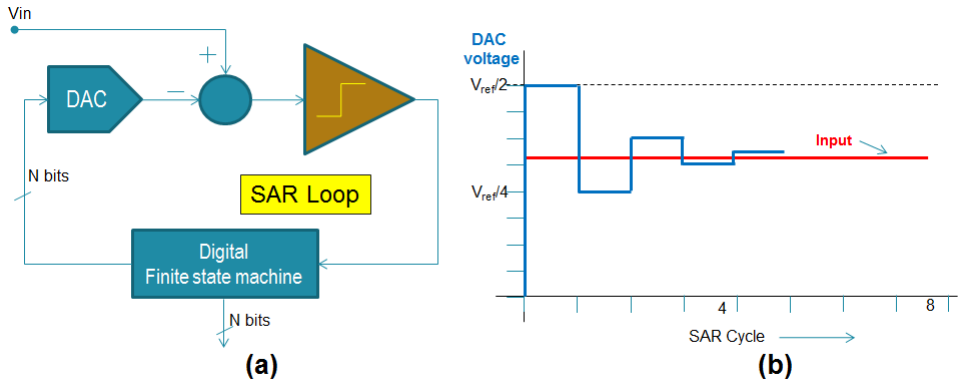

FIGURE 2.1: (a)SAR loop (b)5 cycles of SAR Loop with binary DAC

bit (V_{LSB}) and the minimum voltage (V_{min}) the comparator can detect (without metastable condition) as,

$$P(e) = \frac{V_{min}}{V_{LSB}}. \tag{2.7}$$

The error probability of comparator should be several order lower than the system bit error rate (BER).

2.2 SAR-ADC

Figure 2.1(a) shows the block diagram of the typical successive approximation loop, and Figure 2.1(b) shows 5 SAR cycles with an N-bit binary digital to analog converter (DAC) and a comparator in the negative feedback SAR loop [8]. For a binary DAC, the SAR cycle starts with the initial DAC voltage at $\left(\frac{V_{ref}}{2}\right)$, and decreases by $\left(\frac{V_{ref}}{4}\right)$ during the next cycle. The DAC voltage changes by one-half of the previous DAC voltage every cycle. Negative feedback in the SAR loop ensures that the DAC voltage moves such that the error between the input and the DAC voltage is reduced as directed by the comparator decision. At the end of N SAR cycles, the error will be $\left(\frac{V_{ref}}{2^N}\right)$.

For a SAR-ADC with a binary DAC, every cycle needs to converge to $\frac{V_{ref}}{2^N}$. If the comparator makes an error (due to offset or noise), there is no mechanism

to correct the code and all the SAR-ADC cycles must be low noise (decided by ENOB of the ADC) events.

2.3 Pipelined SAR-ADC

Figure 2.2 shows a 14 bit pipelined SAR architecture. Two SAR-ADCs are pipelined with a residue amplifier (DRA) in between.

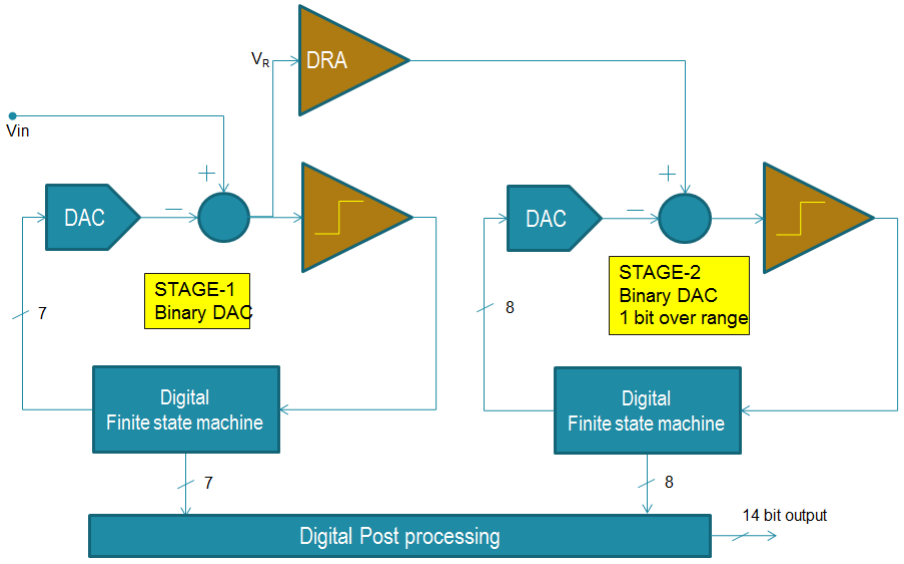

FIGURE 2.2: 14-bit pipelined SAR architecture

If the second stage has over-range (refer to [6] for over-range and digital error correction), based on the second stage digital code errors introduced by comparator (due to offset or noise) are digitally corrected. Depending on the over-range the noise specification of the first stage comparator can be relaxed. The second stage of the pipeline receives an amplified residue as input. Based on the gain of the residue amplifier the noise requirements of subsequent pipelined stages are relaxed. Hence, residue amplification is the only one low noise event compared to single SAR-ADC (see figure 2.3). Because of these advantages, the pipelined SAR-ADC as proposed in [5, 9, 10] is becoming one of the popular choices for a low power ADC. The noise from the residue amplifier must be low enough (similar to the comparator noise specification in a SAR-ADC), and power consumption is

comparable to a comparator in a binary SAR-ADC. The exact noise specifications are derived in the next section.

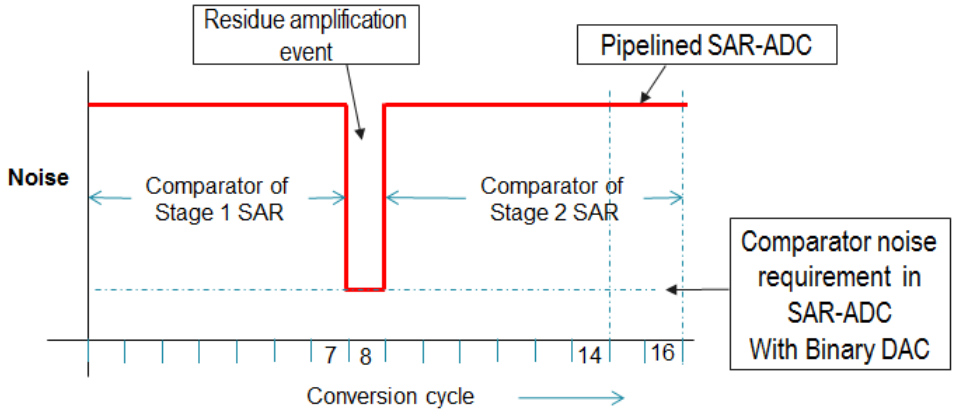

FIGURE 2.3: Comparator/residue amplifier noise requirement for SAR-ADC and pipelined SAR-ADC

2.4 Derivation of specifications for residue amplifier and comparator

Table 1.1 gives the ADC lane specifications. To meet these ADC specifications, a two-stage pipelined SAR-ADC architecture is chosen. The resolution of Pipelined SAR-ADC is limited by thermal noise (residue amplifier, DAC and comparator), distortion (residue amplifier and DAC) and the quantization noise. The ADC will be designed such that its resolution (ENOB=12bits) is limited by thermal noise. The ADC is designed for 14 bits so that the quantization noise does not limit ENOB.

Having a high residue amplifier gain relaxes the noise requirements of the second stage. The residue amplifier chosen for implementation is open loop (refer to Chapter 4), and the input swing is limited. Hence, at least seven bits need to be resolved in the first pipelined stage such that the residue is small enough for the amplifier to be linear. Rest of the 7 bits are resolved in the second pipelined stage

with an additional bit for over-range [6].

The reference voltage for the ADC is ±0.7V (see Table 1.1). For ENOB of 12, the total noise budget for the ADC is $\frac{1.4}{2^{12}\times\sqrt{12}} \simeq 100uV$ [8]. To meet the total noise specification, the input referred noise budget for the residue amplifier is 50uV. Since the second pipelined stage needs to resolve 7 bits, from equation (2.5) the THD of the residue amplifier should be greater than $(7+1)\times 6.02 + 1.76 \simeq 50dB$. The comparator in the second stage is designed for input referred noise of 450uV. With a residue amplifier gain of 16 (i.e., 2^4), the total input referred noise due to amplifier and second stage comparator is $\sqrt{50u^2 + \left(\frac{450u}{16}\right)^2} = 57uV$, which is still within the total noise budget.

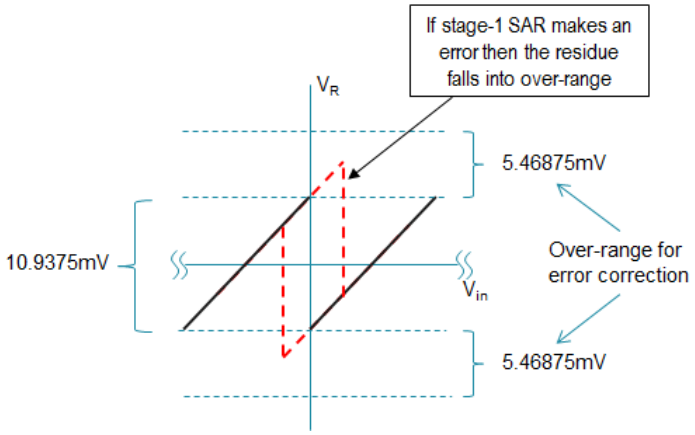

FIGURE 2.4: Over-range to correct the error from first stage of the pipelined SAR-ADC

Considering that the first stage resolves 7 bits, the residue for the second stage would be $\frac{1.4}{2^7} = 10.9375mV$. The over-range [6] is budgeted to be ±5.46875mV (see Figure 2.4). If the stage-1 SAR makes an error then the residue would fall in to over-range, this error can be digitally corrected (refer [6] for over-range and error correction). After offset correction the comparator (first stage) offset is budgeted to be less than ±1mV. Also, the 3σ input referred noise of the comparator is budgeted for 1mV, which makes input referred noise of the comparator less than 333uV. The errors due to the comparator of the first stage can be digitally corrected. The rest of the over-range is left for switching noise at the input of the

comparator. As explained before the noise budget for second stage comparator is 450uV.

During one ADC conversion, the comparator and the DAC of the stage-1 SAR switch seven times, and the comparator and the DAC of the stage-2 SAR switch eight times. The energy/cycle budget for stage-1 comparator is 100fJ (the energy/conversion will be 700 fJ), and for stage-2 comparator energy/cycle will be slightly less as it has more relaxed noise specification. The residue amplifier operates only once in the entire conversion cycle and the energy budget is 400 fJ/cycle (refer to section C.2 in Appendix C).

The clock frequency for the ADC is 100 MHz. Both stage-1 SAR and stage-2 SAR have 5 nsec each for the conversion. In stage-1, 1 nsec is allocated for residue amplifier operation and 4 nsec is budgeted for 7 comparator cycles. In stage-2 all of the 5 nsec is budgeted for 8 comparator cycles.

Based on the above discussions the proposed specifications of the residue amplifier are shown in table 2.1. Specifications of stage-1 comparator and stage-2 comparator are given in Table 2.2 and Table 2.3 respectively.

TABLE 2.1: Residue amplifier specifications (†option for calibration)

Parameter	Min	Typ	Max	Units
Supply		1		Volts
Input common mode		0.6		Volts
Settling period †		1		nsec
Differential Input		11	22	mVolts
Gain †		16		V/V
Noise @ input		50		μVolts
THD	50			dB
Energy/cycle		400		fJ

TABLE 2.2: Stage1 comparator specifications

Parameter	Min	Typ	Max	Units
Supply		1		Volts
Input common mode		0.6		Volts
Delay (LSB input)			250	psec
Noise @ input			300	μVolts
Energy/cycle		100		fJ

TABLE 2.3: Stage2 comparator specifications

Parameter	Min	Typ	Max	Units
Supply		1		Volts
Input common mode		0.6		Volts
Delay (LSB input)		150		psec
Noise @ input			450	μVolts

2.5 Summary

In this chapter, the SAR-ADC architecture has been introduced. Noise and energy requirements of the comparator were presented. Splitting the SAR-ADC into two stages with a gain stage in between, reduces the noise requirements of comparator. That leads to the Pipelined SAR-ADC. The impact of the residue amplifier specifications on the specifications of pipelined SAR-ADC were briefly analysed. A high gain, low-power and low-noise residue amplifier is critical for reduction of overall power consumption. Finally to quantify the problem definition, the amplifier and the comparator specifications were derived.

Chapter 3

Noise bandwidth of a discrete time amplifier

This chapter describes two operating cases (steady-state mode and integrator mode) of a transconductance amplifier based upon the output noise behaviour. Noise and gain of the two modes are analysed and compared using an example, and conclusions are presented. Since the application is an ADC, analysis is restricted to the discrete-time mode.

3.1 Step response of a transconductance amplifier

Let us consider an amplifier with low-pass (considering a resistor and a capacitor) transfer function and time constant of τ_o (see Figure 3.1a). For a DC step input; Figure 3.1b shows the response of the transconductance amplifier when $T_s >> \tau_o$, and Figure 3.1c shows the response of the transconductance amplifier when $T_s << \tau_o$, which is a ramp (like an integrator). For the condition $T_s >> \tau_o$ (henceforth referred to as the steady-state mode), the output noise power is not a function of time. For the condition $T_s << \tau_o$ (this condition is modified in next section so

that it is consistent with both gain and noise analysis) the output noise power is a function of time (henceforth referred to as the integrator mode).

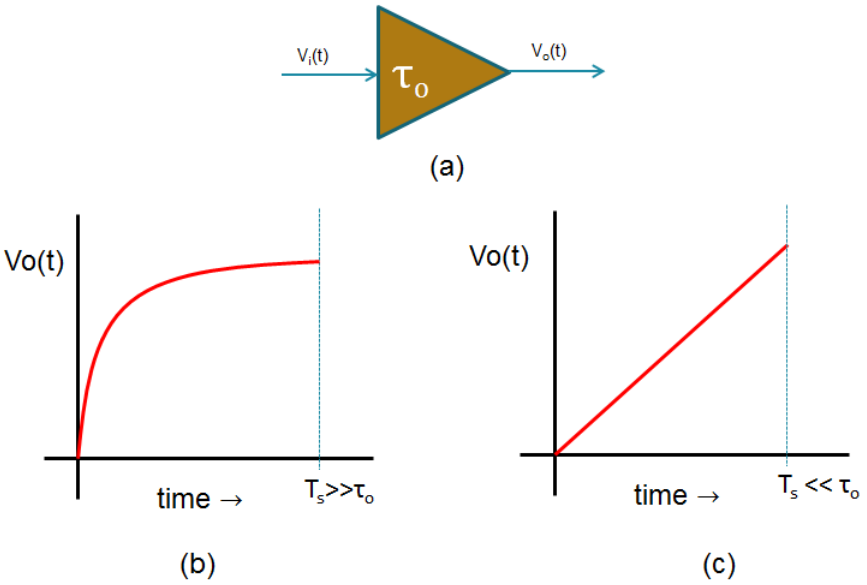

FIGURE 3.1: Step response of transconductance amplifier (a) Transconductance amplifier with time constant τ_o(b)steady-state mode response (c) integrator mode response

In the next section, it will be mathematically shown that for a fixed response time T_s, operating in the integrator mode shows smaller noise bandwidth compared to steady-state mode. Hence, the integrator mode achieves a smaller input-referred noise compared to the steady-state mode.

Please note that the words steady-state mode (indicates stationary noise) and integrator mode (indicates non-stationary noise) are used in this thesis to indicate specific conditions relating to the output noise behaviour only. In this thesis, the integrator mode implies integrator-like behaviour of the transconductance amplifier. It refers mainly to the integration of thermal noise on the load capacitor.

3.2 Gain and noise of the transconductance amplifier in the steady-state and integration modes of operation

One of the well-known methods for voltage amplification is to convert an input voltage into a current using a transconductance amplifier, and subsequently having the output current flow through a load impedance, which generates an amplified version of the input voltage [11]. A model of a transconductance amplifier is shown in Figure 3.2. The source S_{xo} represents all of the noise generated in the g_m cell, and all other components are noise free.

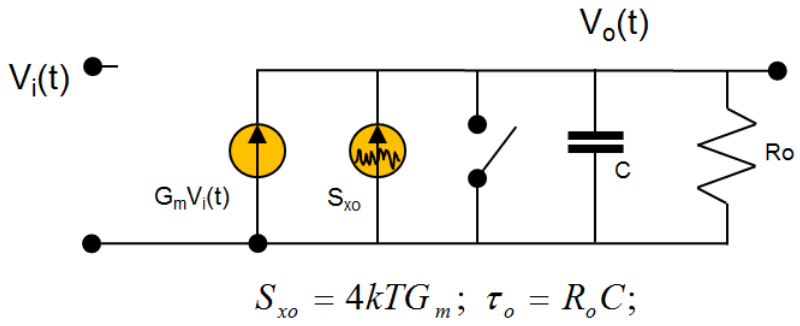

FIGURE 3.2: Transconductance amplifier model ($t \leq 0$ switch is closed; $t > 0$ switch is open)

A unit step input is assumed for this analysis. The output voltage of the transconductance amplifier (shown in the Figure 3.2) can be expressed as,

$$V_o(t) = V_i(t)\,(G_m R_o)\left(1 - e^{-\frac{t}{\tau_o}}\right). \tag{3.1}$$

The output voltage across the capacitor is a function of the time. Mathematically, two cases of operation can be derived. For the steady-state mode $t >> \tau_o$, and $t << \tau_o$ for the integrator mode. Substituting in to equation (3.1) for the condition defining steady-state gives,

$$V_o(t) = V_i(t)\,(G_m R_o). \tag{3.2}$$

Similarly, for the integrator mode ($t << \tau_o$), and

$$V_o(t) = V_i(t)\left(\frac{G_m}{C}t\right). \tag{3.3}$$

For steady-state mode of operation, noise is modelled as a wide-sense-stationary (WSS) noise source. The expected noise power at any given time for a WSS noise source is fixed. Circuits like comparators are dynamic in nature and the WSS noise model cannot be used in such a case. The noise is not stationary in such circuits because the mean and variance of the noise power changes with the time. In a recent paper [12], a method to analyse non-stationary noise has been described. Equations from (3.4) to (3.8b) are repeated from paper [12] to summarize the analysis. The output variance of a non-stationary noise source is given by,

$${\sigma_y}^2(t) = \frac{1}{2}S_{xo}\int_0^t |h_n(\alpha)|^2 d\alpha. \tag{3.4}$$

Where S_{xo} is the power spectral density (PSD) of the input noise source and $h_n(\alpha)$ is the impulse response from the noise source to the output. S_{xo} is modelled as a thermal noise source for the circuit of Figure 3.2, given by

$$S_{xo} = 4kTG_m. \tag{3.5}$$

The impulse response from noise source to output for the model shown in Figure 3.2 is,

$$h_n(t) = \frac{1}{C}e^{-\frac{t}{\tau_o}}. \tag{3.6}$$

Substituting equations (3.5) and (3.6) into equation (3.4), the output noise can be determined as,

$${v_{on}}^2(t) = \frac{kT}{C}(G_m R_o)\left[1 - e^{-\frac{2t}{\tau_o}}\right]. \tag{3.7}$$

Considering the gain equation (3.1) the condition for integrator mode $t << \tau_o$ is sufficient but it is not consistent with the noise equation (3.7). Hence, it is changed to $t << \frac{\tau_o}{2}$. For steady-state mode the condition remains as $t >> \tau_o$. From equation (3.7), the output noise for steady-state mode ($t >> \tau_o$) and integrator mode ($t << \frac{\tau_o}{2}$) can be derived as given by equations (3.8a) and (3.8b), respectively.

$$v_{on}{}^2(t) = \frac{kT}{C}(G_m R_o), \tag{3.8a}$$

$$and \quad v_{on}{}^2(t) = \frac{2kTG_m}{C^2}t. \tag{3.8b}$$

By dividing the output noise power by the square of the gain term, the noise can be referred to the input. For steady-state ($t >> \tau_o$), equation (3.8a) should be divided by square of equation (3.2), and the corresponding input referred noise power is given as,

$$v_{in1}{}^2 = \overbrace{\left(\frac{4kT}{G_m}\right)}^{Noise\ source\ at\ input} \quad \overbrace{\left(\frac{1}{4R_oC}\right)}^{Noise\ Bandwidth} . \tag{3.9}$$

Similarly, for the integrator mode ($t << \frac{\tau_o}{2}$) by dividing the equation (3.8b) with the square of equation (3.3) the input referred noise can be given as,

$$v_{in2}{}^2(t) = \overbrace{\left(\frac{4kT}{G_m}\right)}^{Noise\ source\ at\ input} \quad \overbrace{\left(\frac{1}{2t}\right)}^{Noise\ Bandwidth} . \tag{3.10}$$

In equations (3.9) and (3.10), first part is a noise source $\left(\frac{S_{xo}}{G_m^2}\right)$, and the second part is the noise bandwidth. It is represented in two parts, so that comparison between steady-state and integrator mode is simplified.

3.3 Comparison of steady state mode and integrator mode

In an ADC for a given clock frequency, the settling time required for the amplifier is fixed. Equations (3.9) and (3.10) show that for a given time period 't' both gain and noise bandwidth can be different in each of the two modes. Let $t = T_s$ be the transconductance amplifier operation time period.

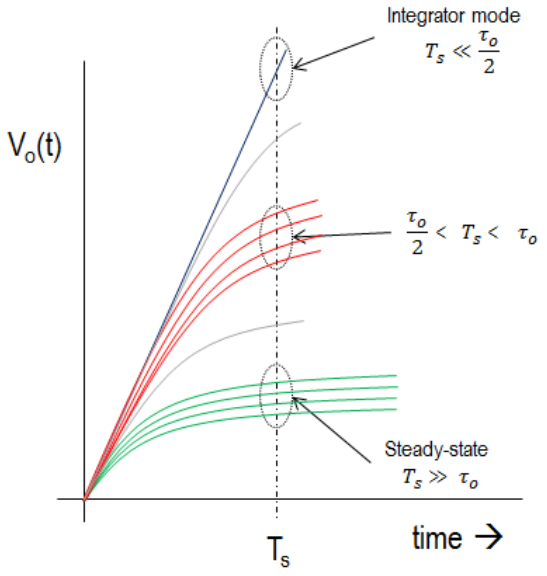

FIGURE 3.3: Step response of transconductance amplifier versus time for different time constant R_o values ($\tau_o = R_oC$)

Figure 3.3 shows the step response of a transconductance amplifier versus time for different R_o values ($\tau_o = R_oC$). For steady-state mode R_o is very small such that $T_s >> \tau_o$, and for the integrator mode R_o is very large such that $T_s << \frac{\tau_o}{2}$. The condition $\frac{\tau_o}{2} < T_s < \tau_o$ indicates the transition from steady-state mode to integrator mode.

If the transconductance amplifier is designed to operate in the steady-state mode, the condition is $T_s >> \tau_{o1}$ (refer section 3.2) where $\tau_{o1} = R_{o1}C$. Let us consider a case where the required accuracy is N bits, where N is greater than 3. For N greater than 3 bit accuracy the settling time should be $T_s = n\tau_{o1}$ where $n > 2$ (refer to section C.3 in AppendixC). The gain of the transconductance amplifier

in the steady-state mode is given by,

$$Gain_{SS} = (G_m R_{o1}), \tag{3.11}$$

and the noise bandwidth (from equation (3.9)) is given by,

$$NBW_{SS} = \left(\frac{1}{4R_{o1}C}\right). \tag{3.12}$$

For the integrator mode, the condition is $T_s << \frac{\tau_{o2}}{2}$, where $\tau_{o2} = R_{o2}C$. To meet the integration mode condition, the output impedance R_{o2} of transconductance amplifier is increased (which also implies that $R_{o2} >> R_{o1}$). The integration period is still the same (T_s). The period T_s can be substituted with $n\tau_{o1}$ for the purpose of comparison between the two modes. The gain of the transconductance amplifier in the integrator mode is given by,

$$Gain_{IM} = \left(\frac{G_m T_s}{C}\right) = nG_m R_{o1}, \tag{3.13}$$

$$\Rightarrow Gain_{IM} = nGain_{SS}, \quad where\ n > 2. \tag{3.14}$$

Noise bandwidth of the transconductance amplifier in the integrator mode is given by,

$$NBW_{IM} = \left(\frac{1}{2T_s}\right) = \left(\frac{2}{n}\right)\left(\frac{1}{4R_{o1}C}\right). \tag{3.15}$$

$$\Rightarrow NBW_{IM} = \left(\frac{2}{n}\right) NBW_{SS}, \quad where\ n > 2. \tag{3.16}$$

From equations (3.14) and (3.16) the following conclusions can be drawn. For a fixed amplification time, the integrator mode shows less input-referred noise compared to steady-state mode due to the smaller noise bandwidth. For a fixed amplification time, the integrator mode achieves a higher gain than the steady-state mode. Figure 3.4 shows step response of transconductance amplifier in the integrator mode for different $\frac{G_m}{C}$ values. As long as transconductance (G_m) and integration period (T_S) is constant the input referred noise will not change even

though the slopes are different. Hence, slope can be adjusted to get the similar gain as that of steady-state mode. However, in the integrator mode the output is a function of time and it does not settle during T_s. Hence, to use the integrator mode for voltage amplification, it is essential that the integration time is well controlled to ensure final accuracy.

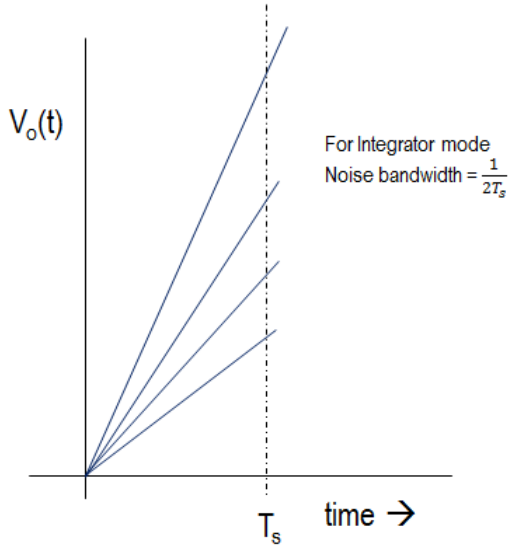

FIGURE 3.4: Step response of transconductance amplifier in the integrator mode versus time for different $\frac{G_m}{C}$ values

To confirm the above analysis, large-signal simulation was done using the model in Figure 3.2 with transient noise (a feature available in Cadence Spectre). The simulation is done for fixed sampling time of 1 nsec and transconductance is 1 mS. The time constant τ has been varied from 0.1 nsec to 100 nsec (by varying resistor R_o). Figure 3.5 shows the simulation results. The input-referred noise for the integrator mode is less than that for steady-state mode.

It will be seen in the next chapter that dynamic amplifiers inherently operate in the integrator mode. Hence, dynamic circuits were chosen for study and the design of the residue amplifier.

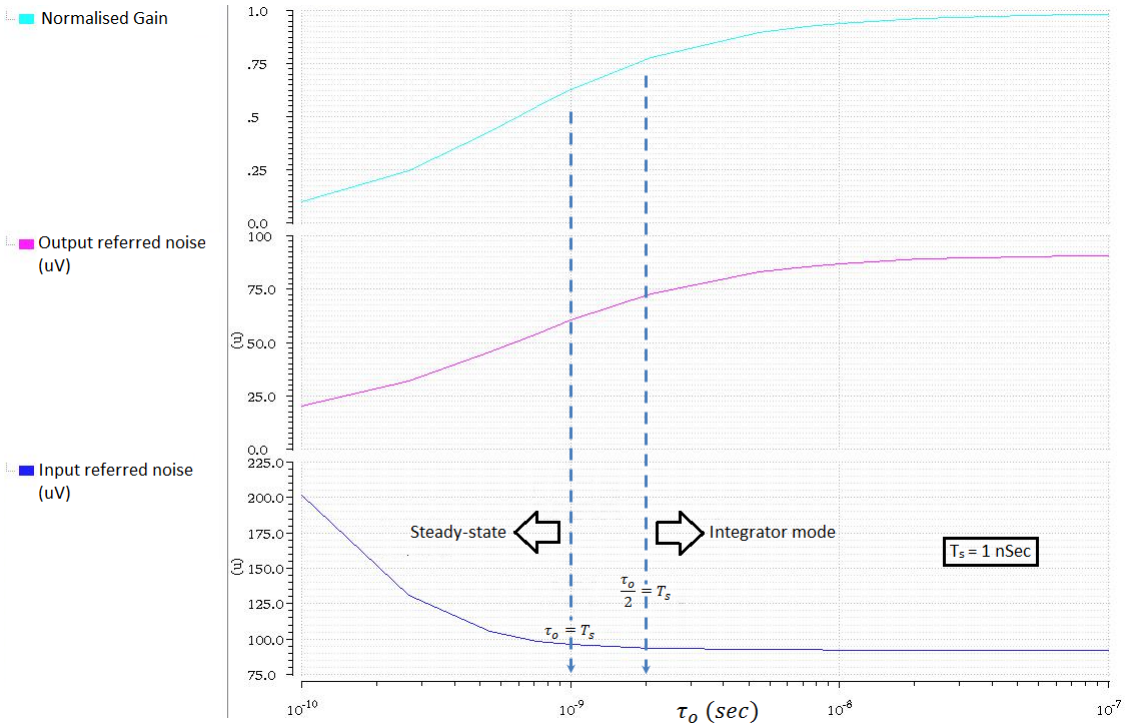

FIGURE 3.5: Gain, output referred noise and input referred noise versus τ_o

3.4 Summary

Based on the output noise behaviour, two modes of operation of transconductance amplifier were discussed in this chapter. The two modes were compared in terms of gain and noise. With a mathematical analysis using the non-stationary noise model of the transconductance amplifier, it was shown for a given clock frequency that the integrator mode is more beneficial in terms of noise. This analysis was supported by simulation results. Due to low noise, the residue amplifier topology operating in the integrator mode is considered for the residue amplification in Chapter 4.

Chapter 4

Dynamic residue amplifier

This chapter presents a detailed analysis of a single-stage integrator and a cascoded integrator, and compares them in terms of gain and noise. As it was discussed in Chapter 3, the integrator output does not settle. Hence, to complete the topology of the dynamic amplifier a common-mode detect circuit is included to generate the stop signal, creating a cascoded integrator dynamic residue amplifier (CIDRA). The gain, noise and linearity of the CIDRA are then further analysed theoretically. Finally, simulation results are presented to support the analysis.

4.1 Gain of the dynamic amplifier circuits

The concept of dynamic amplifiers is not new as they have been a part of dynamic comparators as pre-amplifiers. Recently dynamic amplifiers have also been published [3–5, 13]. Typical characteristic of these dynamic amplifiers is that they do not need a constant DC bias current. The power consumption of dynamic amplifiers is proportional to clock frequency. As explained in Chapter 3, operating in the integrator mode is beneficial in terms of noise and gain. In the following sections two dynamic amplifier circuits are analysed for residue amplification in a pipelined ADC application, and both of them operate in the integrator mode.

4.1.1 Single-stage integrator

A simple integrator can be built using one transistor pair (for differential operation). Figure 4.1 shows a simple (and intuitive) circuit of a dynamic amplifier.

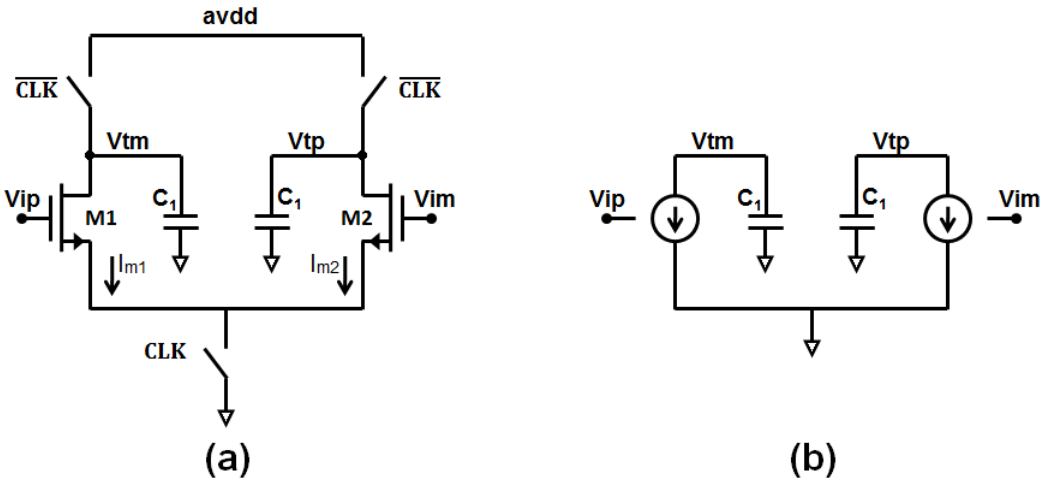

FIGURE 4.1: (a) Single-stage integrator (b) Equivalent small signal model of single-stage integrator

The functionality of the single-stage integrator (used in [13]) is explained graphically in Figure 4.2. The operation can be explained in three phases.

In the first phase, CLK is low. It is the reset phase for the amplifier. In this phase, the capacitors C_1 are charged to avdd. The input pair is off.

In the second phase, CLK is high. The tail of the input pair discharges to ground and hence the input pair turns ON. The input pair is in the saturation state. The differential nodes V_{tm} and V_{tp} discharge in proportion to the differential input ($\Delta V_{in} = V_{ip} - V_{im}$) through the input pair. Integration happens in this phase simultaneously the output common-mode moves towards the ground.

The CLK is high in the third phase. The differential output signal builds on output capacitors C1. It continues to build until either V_{tm} or V_{tp} reach ground potential. In this phase, the input pairs are close to the linear region. The output signal should be stored at the end of the phase-2 when the transistors are still in saturation.

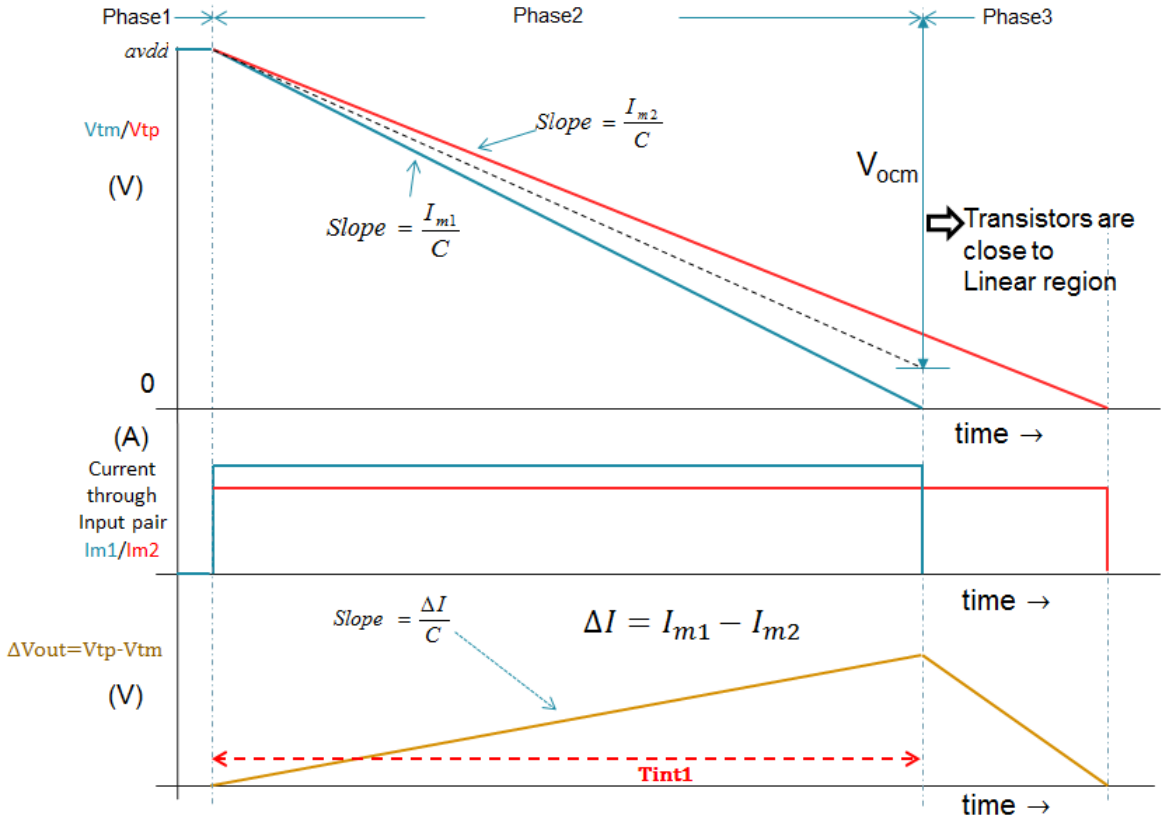

FIGURE 4.2: Graphical explanation of single-stage integrator functionality

The expression for the gain for the single-stage integrator can be given by the following equation (refer to the section C.1 in Appendix C),

$$A_o = \frac{T_{int1} g_{m1}}{2C_1}. \tag{4.1}$$

Where g_{m1} is the transconductance of each device in the input pair (assuming small ΔI). The integration time T_{int1} can be expressed in terms of output common-mode voltage (V_{ocm}) as,

$$T_{int1} = \frac{V_{ocm} C_1}{I_m}. \tag{4.2}$$

In this expression I_m is the output common mode current ($\frac{I_{m1}+I_{m2}}{2}$) and can be expressed as (assume basic MOS equation):

$$g_{m1} = \frac{2I_m}{V_{gt}}, \tag{4.3}$$

where V_{gt} is equal to $V_{gs} - V_{tn}$ of the input pair. By substituting equations (4.2) and (4.3) into equation (4.1), the expression for the gain can be simplified as,

$$A_o = \frac{V_{ocm}}{V_{gt}}. \tag{4.4}$$

As the differential output voltage (Vtp-Vtm) increases over time, the output common-mode voltage droops (see Figure 4.2). For a given output common-mode voltage and overdrive, the gain is fixed. For example, if the V_{gt} is 80mV (assuming that input pair is biased in weak inversion [14]) and the output common-mode voltage is 0.5V, the gain is 6.25. This limitation in gain comes because of limited supply voltages (1V in our design). The limitation in gain can be overcome by cascoding the integrator as explained in the next section.

4.1.2 Cascoded integrator

The optimization of a single-stage integrator is less flexible due to few design parameters. The cascoded integrator (see Figure 4.3) has two integrators connected in series. The gates of the cascode devices are shorted to node V_{cb} (a DC supply unless otherwise mentioned).

Its functionality can be described in 5 phases. The 5 phases are also illustrated graphically in Figure 4.5.

In phase-1 CLK is low. It is the reset phase for the amplifier. In this phase, both capacitors C_1 and C_2 are charged to avdd. The input pair (M1 and M2) and the cascode pair (M3 and M4) are cut-off.

In the second phase, CLK is high (see Figure 4.4(a)). The source of the input pair discharges to ground and hence the input pair turns ON, and it is saturated. The cascode pair is still off. Nodes V_{tm} and V_{tp} discharge proportional to ΔV_{in}

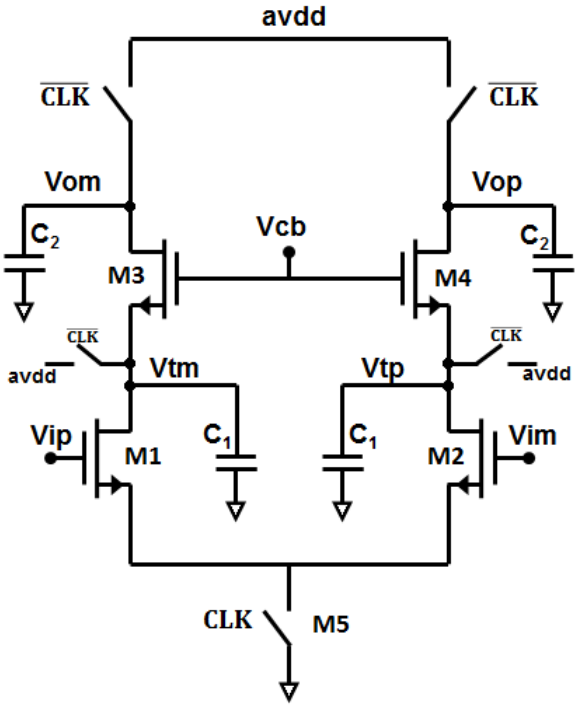

FIGURE 4.3: Cascoded integrator

through the input pair, while differential voltage $\Delta V_t = V_{tm} - V_{tp}$ increases over time. Integration happens in this phase (shown as T_{int1} in Figure 4.5).

In phase-3, CLK is high. When V_{tm}(or V_{tp}) drops one Vt below V_{cb}, the corresponding cascode device turns on (see Figure 4.4(b)) and is in saturation. Approximately half of the common-mode current flows out of C2 connected at V_{om} (or V_{op}). Now that the cascode device is on, it prevents V_{tm}(or V_{tp}) from dropping further. Hence, ΔV_t starts dropping towards ground, and Δt_{12} (only one cascode device is on) is proportional to the differential input voltage (see Figure 4.5). Hence, the differential voltage that is integrated at node V_{om} during Δt_{12} is proportional to the input voltage.

In phase-4, CLK is high. When the other node V_{tp}(or V_{tm}) also drops Vt below V_{cb}, the second cascode device also turns ON, and is in saturation (see Figure 4.4(c)). The cascode pair prevents V_{tp}(or V_{tm}) from dropping further. The differential output voltage continues to grow proportional to the differential input voltage but with a smaller slope compared to phase-3. The output common-mode voltage drops further.

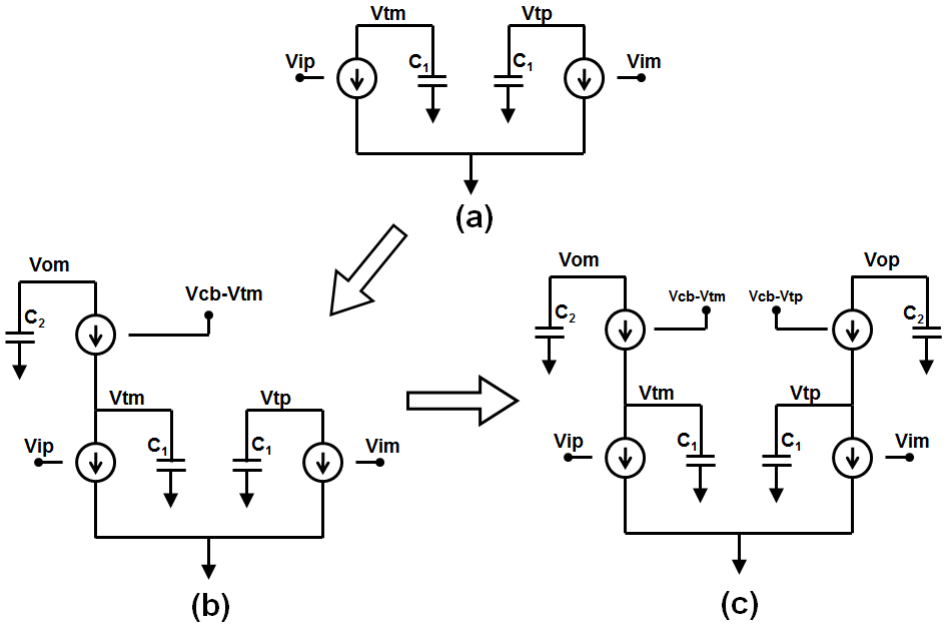

FIGURE 4.4: Small signal models of Figure 4.3 (a) for phase-2 (b) for phase-3 (c) for phase-4

In phase-5, CLK is still high. In this phase, both cascode devices enter the linear region. The beginning of phase-5 can be controlled by V_{cb}. Even though the output voltage continues to grow, the linearity of the transfer function degrades. Hence, it is essential that the differential voltage in phase-4 is stored, and that the circuit is prevented from entering in to phase-5.

The output voltage across the cascoded integrator continues to integrate starting from the amplified voltage produced by the first stage, like two cascaded single-stage integrators. This is equivalent to increasing the supply voltage for a single-stage integrator.

At the end of the $t_{int1} + \Delta t_{12}$ time period, the output voltage always follows the line $\frac{\Delta I}{C_2}$ (see Figure 4.5). The gain at the end of the integration period $T_{int1} + T_{int2}$ can be expressed as given below,

$$A_o = \frac{g_{m1}}{2C_2} \left(T_{int1} + T_{int2}\right). \tag{4.5}$$

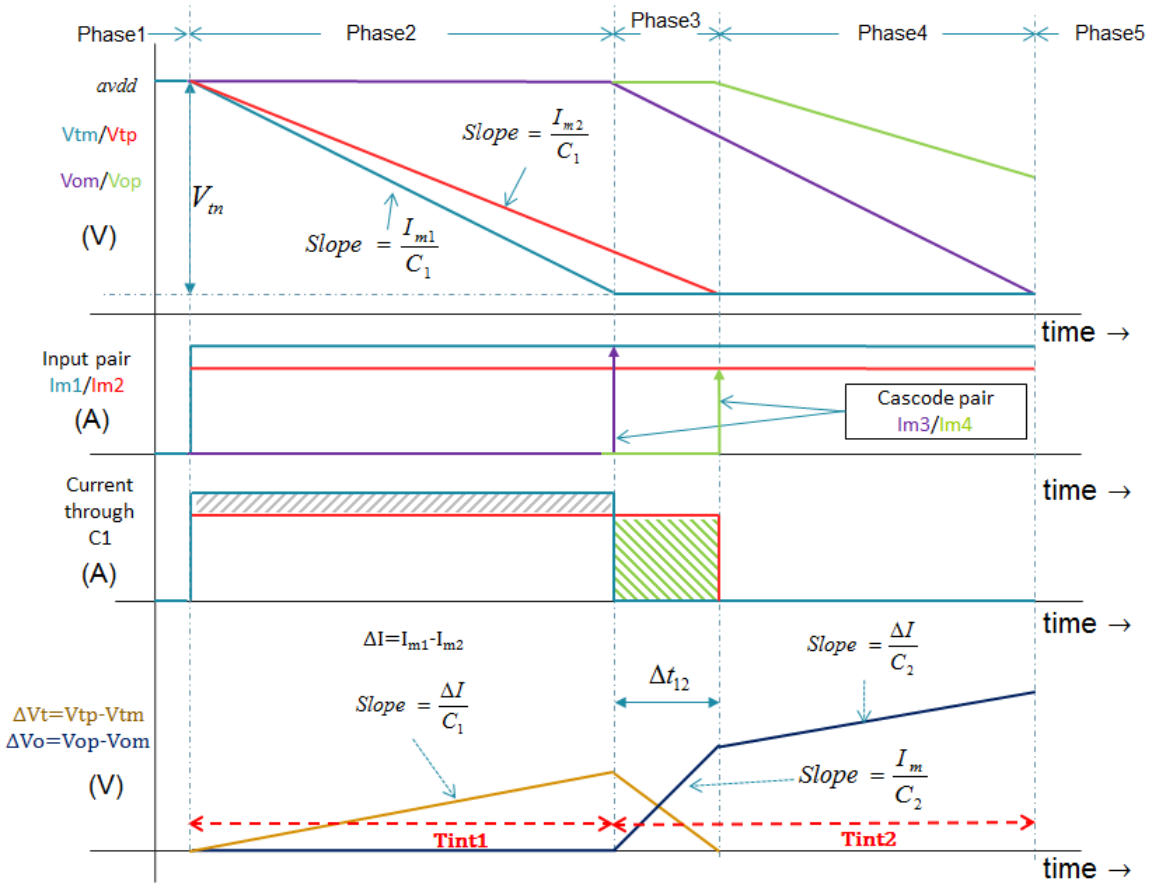

FIGURE 4.5: Graphical explanation of cascoded integrator functionality (C1=C2=C)

Where g_{m1} (assuming that $I_{m1} - I_{m2}$ is very small) is the transconductance of each device in the input pair. For very small input (ΔV_{in}), Δt_{12} is very small compared to $T_{int1} + T_{int2}$. The integration periods T_{int1} and T_{int2} can be expressed in terms of output common-mode voltage drop (V_{tn}) as given by following equations (for mathematical simplicity the common-mode voltage drop during T_{int1} at the drain of the input pair is assumed to be the same as the output common-mode voltage drop during T_{int2}),

$$T_{int1} = \frac{V_{tn} C_1}{I_m}, \tag{4.6}$$

$$T_{int2} = \frac{V_{tn} C_2}{I_m}. \tag{4.7}$$

Where I_m is the common-mode current given by the equation,

$$g_{m1} = \frac{2I_m}{V_{gt}}. \tag{4.8}$$

By substituting equations (4.6), (4.7) and (4.8) in to equation (4.5) the expression for the gain can be simplified as,

$$A_o = \frac{V_{tn}}{V_{gt}}\left(1 + \frac{C_1}{C_2}\right) \tag{4.9}$$

By comparing equation (4.9) with equation (4.4) it is clear that cascoded integrator can achieve higher gain compared to the single-stage integrator by properly adjusting the ratio of C_1 and C_2. This circuit operates in integrator mode, where output impedance of transistors does not influence the gain. Hence, cascoding alone does not increase the gain. The gain increases by cascoding, as long as C_1 exists and $C_1 > C_2$. However, the maximum gain can not be more than $g_m^2 r_o^2$ (where g_m and r_o are transconductance and output impedance of transistors M1-M4 respectively) [14].

4.2 Noise of the single-stage integrator and the cascoded integrator

From equation (3.10) of Chapter 3, the input-referred noise of the single-stage integrator at the end of the integration period (i.e., $Tint1$ in Figure 4.2) can be expressed as,

$$V_{inoiseSI}^2 = \frac{2kT}{\left(\frac{g_{m1}}{2}\right)}\frac{1}{T_{int1}}. \tag{4.10}$$

By substituting T_{int1} from equation (4.2) (and I_m from equation (4.3)) into the equation (4.10), the input-referred noise of the single-stage integrator can be further simplified as,

$$V^2_{inoiseSI} = \frac{2kT}{C_1}\frac{V_{gt}}{V_{ocm}}. \tag{4.11}$$

The factor 2 appears in the equation (4.11) because of the differential pair. Consider figures 4.3 and 4.5 for the noise analysis of cascoded integrator. The noise is modelled in phase4 (see Figure 4.5). The major contributor is the noise of the input pair. Since the cascode pair is degenerated by a MOSFET in saturation, it is assumed that the cascode pair does not contribute any noise. The noise from the input pair is present during the entire integration period, $T_{int1} + T_{int2}$. Currents Im1, Im2, Im3 and Im4 are assumed to be equal (i.e., I_m) for the rest of the noise analysis. The period Δt_{12n} used in the following equations highlights that it is Δt_{12} due to noise.

As explained previously, during T_{int1} the cascode pair is off and noise (from the input pair) is integrated at the nodes V_{tm} and V_{tp}. During T_{int2} the cascode pair turns on, and noise is integrated at the output nodes. To calculate the total output noise at the end of the period $T_{int1} + T_{int2}$, it is essential that noise during the period T_{int1} is included in the analysis.

The output referred noise for the cascoded integrator structure can be determined with the following approach. Assuming that the input voltage is zero the large signal behaviour of the circuit would still follow the graphical representation as shown in Figure 4.5. Noise can be found by mainly considering the behaviour in phase2 and phase4. Phase3 also exists, but the period Δt_{12n} is very small compared to $T_{int1} + T_{int2}$ as it is only due to noise. For the mathematical analysis of the noise, calculating the period Δt_{12n} due to noise is essential. Hence, first the noise voltage (V_{n1}) at the end of the period T_{int1} is calculated using equation (3.8b). Then the noise voltage (V_{n1}) is converted into the period Δt_{12n} using the common-mode slope of nodes Vtm and Vtp, which is $\frac{I_m}{C_1}$ (see Figure 4.6).

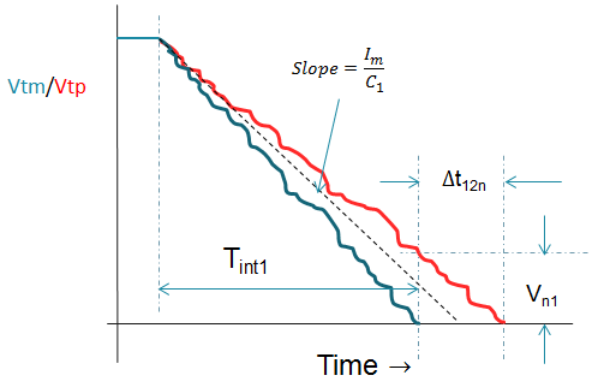

FIGURE 4.6: Calculation of the period Δt_{12n} due to the noise

Considering that the cascode pair (M3 and M4) is off, the noise power at the nodes Vtp and Vtm during the phase2 can be written as (see the equation (3.8b)),

$$V_{n1}^2 = \frac{2kT\frac{g_{m1}}{2}}{C_1^2} T_{int1}. \tag{4.12}$$

The corresponding Δt_{12n} due to the input pair noise can be expressed as,

$$\Delta t_{12n}^2 = \left(\frac{C_1}{I_m}\right)^2 V_{n1}^2. \tag{4.13}$$

During the period Δt_{12n}, the noise generated at the nodes Vtp or Vtm is transferred to output nodes Vop or Vom through one of the cascode transistors. Current I_m flows through the cascode and C2. Hence, the noise power due to Δt_{12n} at the output is given by,

$$V_{n12}^2 = \Delta t_{12n}^2 \left(\frac{I_m}{C_2}\right)^2 = \left(\frac{C_1}{C_2}\right)^2 V_{n1}^2. \tag{4.14}$$

Assuming that the noise current flows only into C_2, the expression for the output noise power during T_{int2} can be expressed as (refer to equation (3.8b)),

$$V_{n2}^2 = \frac{2kT\frac{g_{m1}}{2}}{C_2^2} T_{int2}. \tag{4.15}$$

Even though the noise powers V_{n12}^2 and V_{n2}^2 originate from the same source, they are calculated at different time instances. Hence, the total output referred noise

at the end of period $T_{int1} + T_{int2}$ can be expressed as,

$$V_{onoise}^2 = V_{n12}^2 + V_{n2}^2. \tag{4.16}$$

By substituting the noise powers from phase2 (4.14) and phase4 (4.15) into equation (4.16), the output-referred noise can be written as,

$$V_{onoise}^2 = \left(\frac{C_1}{C_2}\right)^2 V_{n1}^2 + \frac{kTg_{m1}}{C_2^2} T_{int2}. \tag{4.17}$$

By substituting equation (4.12) into equation (4.17), the output referred noise can be further simplified as,

$$V_{onoise}^2 = \frac{kTg_{m1}}{C_2^2} \left(T_{int1} + T_{int2}\right). \tag{4.18}$$

The noise can be referred to the input of amplifier as given below,

$$V_{inoise}^2 = \frac{V_{onoise}^2}{A_o^2}. \tag{4.19}$$

By substituting equation (4.5) into equation (4.19), the input-referred noise can be further expressed as,

$$V_{inoise}^2 = \left(\frac{4kT}{g_{m1}}\right) \frac{1}{(T_{int1} + T_{int2})}. \tag{4.20}$$

The equation (4.20) shows that, the input-referred noise still follows the basic integration principles of single-stage integrator (as explained in Chapter 3) even though the structure is cascoded. By substituting T_{int1} and T_{int2} from equations (4.6), (4.7) and (4.8) into equation (4.20), the input-referred noise of the cascoded integrator can be further simplified as,

$$V_{inoise}^2 = \left(\frac{2kT}{C_1 + C_2}\right) \frac{V_{gt}}{V_{tn}}. \tag{4.21}$$

By comparing equation (4.21) with equation (4.11) it is clear that as long as the

total capacitance is kept constant (and $V_{ocm} = V_{tn}$), the input-referred noise remains the same for both the single-stage and the cascoded integrators. However, the cascoded integrator can achieve a higher gain by redistributing the capacitors, without degrading noise or increasing the total capacitance. As long as the total capacitance is same, the energy consumption also remains the same.

4.3 Comparison between single-stage integrator and cascoded integrator using simulations

To verify the predictions from sections 4.1 and 4.2, large-signal simulations were done (with the circuit parameters given in Table 4.1) for the single-stage integrator (see Figure 4.1a) and the cascoded integrator (see Figure 4.3). The input pair (M1 and M2) of the single-stage integrator is same as that of the cascoded integrator. The simulation is done with a total capacitance of 140 fF.

TABLE 4.1: Parameters used for simulations of schematic shown in Figure 4.3

Parameter	Value
Input pair (M1 and M2)	$40 \times \frac{1\mu}{0.06\mu}$
Cascode pair (M3 and M4)	$20 \times \frac{1\mu}{0.06\mu}$
Tail switch (M5)	$10 \times \frac{1\mu}{0.03\mu}$
C1	80 fF
C2	60 fF
Supply	1 V
Input common-mode	0.5 V

The gain, noise and the energy consumption are compared between the single-stage integrator and the cascoded integrator (see Figure 4.7). Increasing the size of capacitor C1 for single-stage integrator reduces the noise because the integration period increases (integration period must be changed due to common-mode droop). For C1 equal to 140fF (integration period of around 330psec), the noise

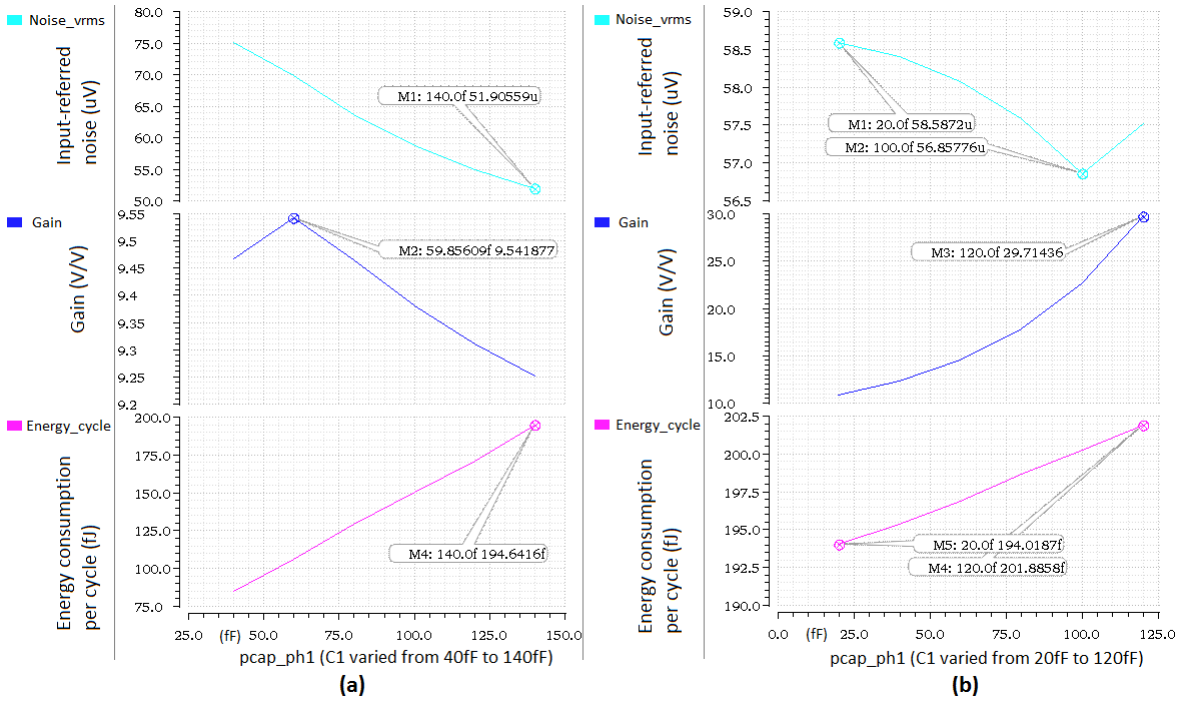

FIGURE 4.7: (a)The input-referred noise, gain and energy consumption of the single-stage integrator. Capacitor (C1) is varied from 40 fF to 140 fF (b) The input-referred noise, gain and energy consumption of cascoded integrator. Ratio between C_1 and C_2 is varied while keeping $(C_1 + C_2)$ constant (equal to 140 fF)

of the single-stage integrator is 52uV. The redistribution of capacitance does not change the noise (between 56uV and 59uV) in the cascoded integrator. However, the redistribution of the capacitors helps to increase the gain. Since the total capacitance is same, the energy consumed by the cascoded integrator is almost similar to the single-stage integrator ($\simeq$ 200fJ). For a single-stage integrator, the gain for C1=40fF is smaller than for C1=60fF because of the leakage current.

For a cascoded integrator with a total capacitance of 140fF (assuming $T = 300^oK$ Vtn=0.5V and Vgt=0.08V) the expected input-referred noise is 97.3uV (see equation (4.21)). To be consistent with Chapter 3 the noise from MOSFET is considered as $4kTg_m$ instead of $\frac{8}{3}kTg_m$. The parasitic capacitors are neglected in the calculation. Hence, estimated noise is higher than the simulated noise (58uV). And for $C_1 = 80fF$ and $C_2 = 60fF$ the expected gain is 14.6 V/V (see equation (4.9)), and the simulated gain is 17.5 V/V.

4.4 Linearity of the cascoded integrator

As analysed before, to ensure a linear transfer function for the amplifier, it is essential that the output voltage is stored before the devices enter the linear region at the end of phase4. To measure the linearity, a two-tone simulation was done for cascoded integrator (for circuit parameters see Table 4.1). Figure 4.8a shows the total harmonic distortion (THD) calculated from a two-tone simulation. The output was sampled at different points around the peak of the differential output (indicated by ptstop in Figure 4.8).

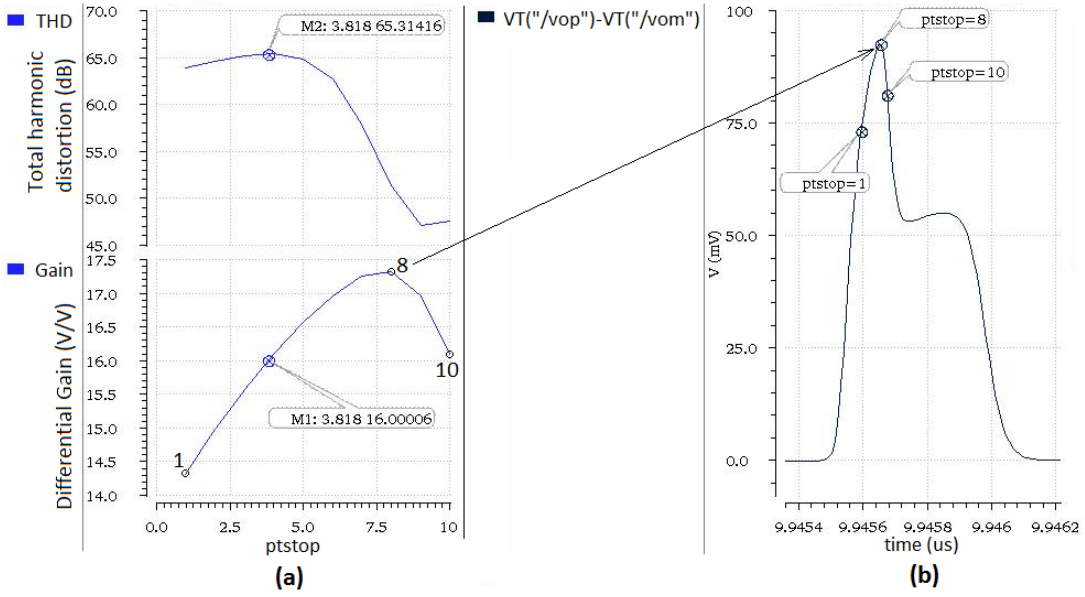

FIGURE 4.8: Simulation of linearity of the cascoded integrator with two-tone (50 MHz and 51 MHz) input with 11 mV pk-pk (see Table 4.1 for other parameters) (a) THD and gain versus sampling instance (ptstop) (b) Differential outputs versus time

As discussed in Chapter 2, resolving more bits in the second pipelined stage is more energy efficient. The higher the amplifier gain the smaller the energy consumption in the second stage, as higher noise can be tolerated from the second stage. Gains of up to 30 are possible with this circuit. However, the choice of gain also depends on linearity. For a fixed gain the linearity depends on the input voltage swing. A gain of 16 is assumed for design as it simplifies the digital post processing of two ADC outputs. To measure the linearity of the cascoded integrator, a two-tone (50MHz and 51MHz) simulation was performed (see Figure 4.8). If 7 bits are

resolved in the first stage, then the residue is 11mV peak to peak. For an 11mV (peak to peak) input (each tone with 5.5mV pk-pk) with a gain of 16, the THD at the output is 65 dB (see Figure 4.8a), which is sufficient to resolve rest of the 8 bits in the second stage. The maximum linearity (65 dB) is limited by the linearity of the differential input pair. The non-linearity of the basic differential pair occurs because the drain current is proportional to the square of the Vgt of the input pair [14]. The THD when the gain peaks is poor, because the devices are in the linear region.

4.5 Dynamic residue amplifier with cascoded integrator and common-mode detect

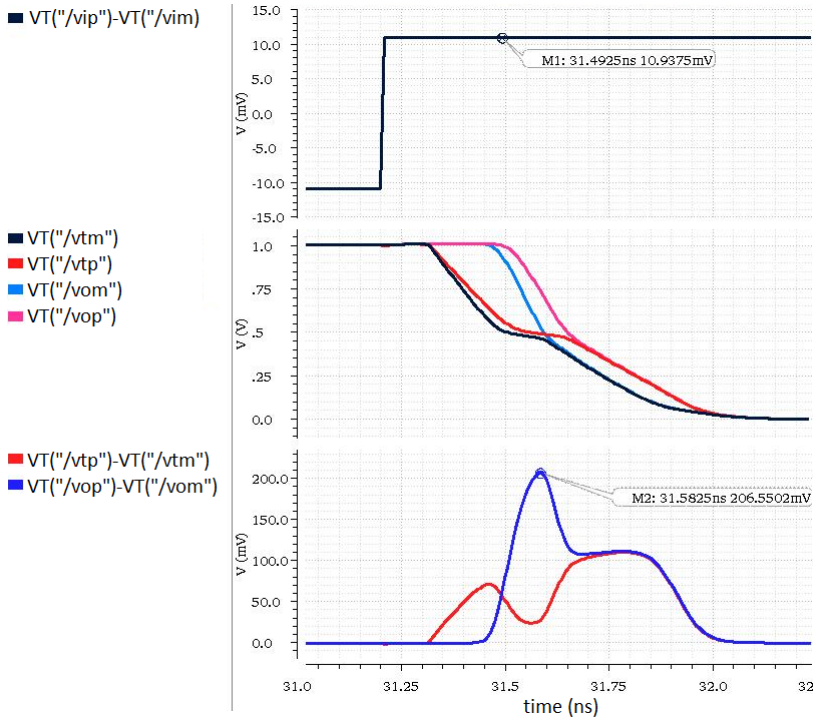

FIGURE 4.9: Simulation of the cascoded integrator of Figure 4.3 (see Table 4.1 for parameters)

As seen in Figure 4.9 the differential output falls back to zero, and the differential output must be stored before the devices enter the linear region (see Figure 4.8). To store the differential output voltage the gate of the cascode devices (M3 and

M4 in Figure 4.3) can be switched from Vcb to zero volts. Two approaches can be followed to generate this stop signal for the gate. First, an independent clock generator can be used. However, synchronization of clock with respect to amplifier (across process and temperature corner) and the jitter or the noise of such a clock generator must be considered in the design. The other approach is to generate the stop signal as a function of the output common-mode voltage. The noise of the output nodes is well controlled (designed for specified noise) and thus generated stop signal will be synchronous with the amplifier. Hence, following the second approach a common-mode detect circuit has been developed as described in the following section.

4.5.1 Common-mode detect

The output of the cascoded integrator (Vop and Vom in Figure 4.3) is input to the common-mode detect circuit. The output of common-mode detect circuit should be high if $\left(\frac{Vop+Vom}{2}\right)$ is above a threshold ($\simeq$ 0.5V). When $\left(\frac{Vop+Vom}{2}\right)$ falls below the threshold, the output of the common-mode detect should be low.

Figure 4.10(a) shows the concept of common-mode detect circuit. For an NMOS input cascoded integrator, two parallel PMOS transistors would cancel the differential signal at the output and will be sensitive to the common-mode voltage alone. The current flowing in the PMOS transistors needs to be dropped across a load (see Figure 4.10(b)). Having a resistor as the load would consume DC current, hence a complementary (CMOS) topology is used. A NAND circuit is suitable (see Figure 4.10(c)). The output of NAND gate needs to be inverted and then connected to gate of the cascode. Thus, the overall operation of the common-mode detect is an AND.

Figure 4.11 shows the complete schematic of cascoded integrator dynamic residue amplifier (CIDRA). Turning off the cascode prevents C2 from discharging. Along

with C2, if C1 is also stopped from discharging, more energy can be saved as the smaller the voltage change across the capacitor the smaller the energy consumption ($C_{tot}V^2$, where $C_{tot} = 2(C_1 + C_2)$). Hence, the clock for the tail switch has been gated (a simple digital AND gate) with V_{cb}, and the energy consumption of CIDRA is therefore significantly less than $C_{tot}V^2$.

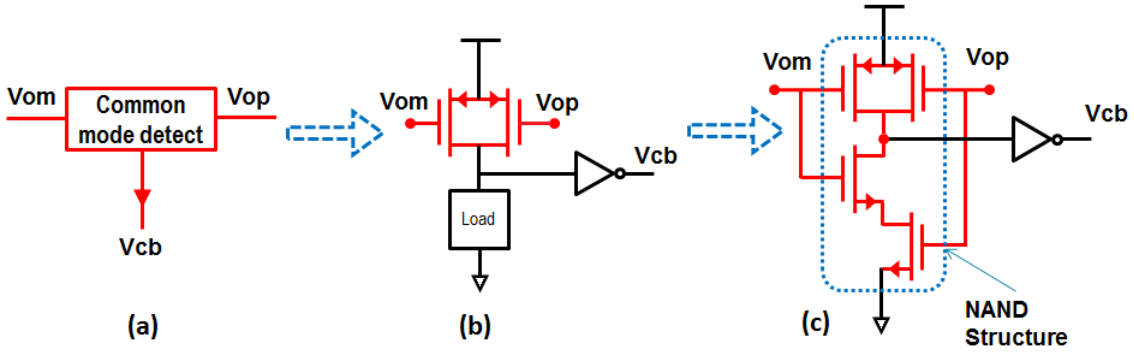

FIGURE 4.10: The concept for common-mode detect circuit

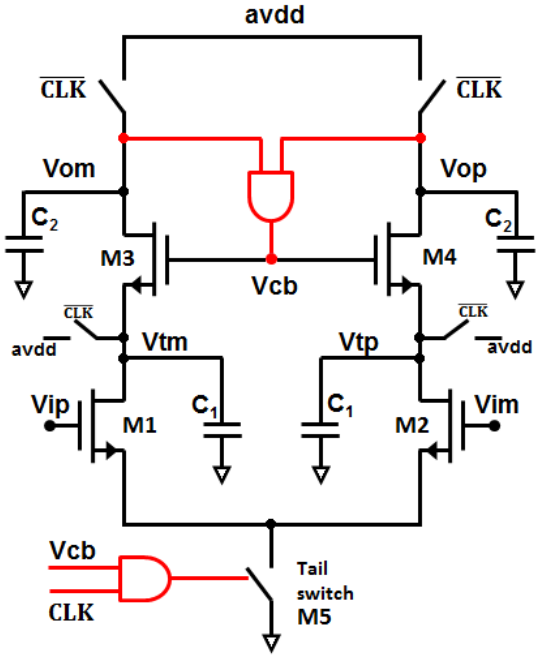

FIGURE 4.11: Cascoded integrator dynamic residue amplifier (CIDRA)

Figure 4.12 shows one transient cycle of the CIDRA. When the clock (phi1) goes high, nodes Vtp and Vtm start to integrate the input voltage. Outputs Vop and Vom are initially at the supply voltage as the cascodes are off. Hence, the output of the common-mode mode detect (Vcb) is high. When nodes Vtp and Vtm drop one V_t below the gate of the cascode pair, the cascode pair turns on

and an amplified differential signal develops at outputs Vop and Vom. Meanwhile, the output common-mode voltage $\left(\frac{Vop+Vom}{2}\right)$ drops towards the ground. When it crosses a threshold voltage ($\simeq$ 0.5 V) the output voltage common-mode detect (Vcb) becomes zero. The cascode pair turns OFF when the gate voltage (Vcb) drops to zero. With the cascode pair turned off, the amplified differential output voltage remains stored across the output capacitors, C_2.

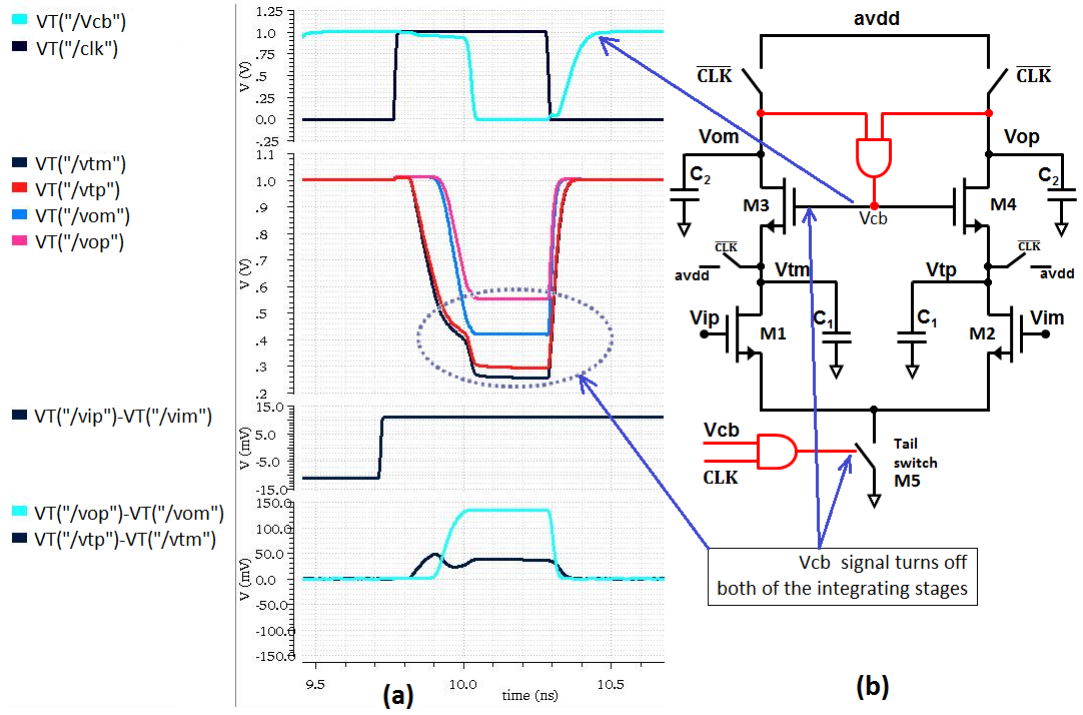

FIGURE 4.12: The transient simulation of CIDRA (a) One transient cycle (b) the CIDRA circuit (see Table 4.1 for parameters)

With the common-mode detect circuit, the stop signal becomes a function of the output common-mode voltage of the amplifier. The most critical specification of the common-mode detect circuit is its sensitivity towards the signal. If the common-mode detect circuit is sensitive to differential-mode signal, the integration period would vary according to the signal level and hence the gain would be a function of the signal, causing distortion. To make the common-mode detect less sensitive to the differential signal, following two changes were included in the NAND circuit. Firstly, parallel PMOS transistors are degenerated by resistors (M7-M8, in Figure 4.13 transistors in the linear region), and secondly the NMOS load is made symmetric (M1-M4). The improved common-mode detect circuit is

shown in Figure 4.13.

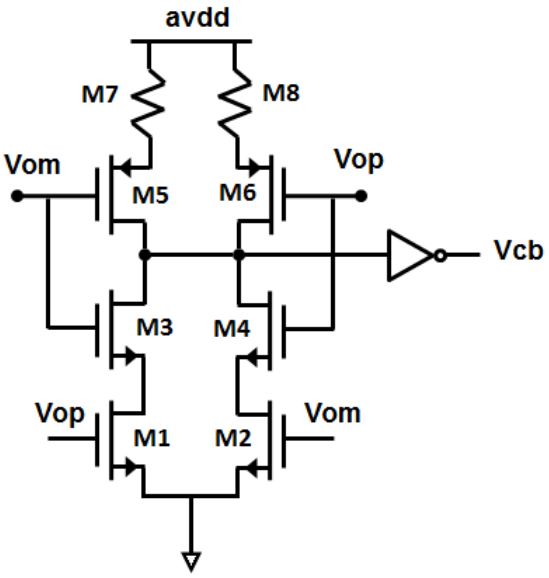

FIGURE 4.13: A symmetric common-mode detect circuit with source degeneration

Table 4.2 shows a comparison of THD (from two-tone simulations) for different conditions. The common-mode detect circuit is sized such that threshold is around 0.5 V. All of the methods have a same integration period and similar gain. From the table, it is clear that with a symmetric and degenerated common-mode detect circuit, the amplifier THD is 57dB, which is sufficient to resolve 8 bits in the second stage.

TABLE 4.2: THD comparison for different common-mode detect methods (Input=11mV pk-pk, 50MHz and 51MHz)

Common-mode detect method	Gain	THD Before Sample	THD after Sample
Ideal CMD	15	64dB	61dB
Simple AND gate	16.7	62dB	50dB
Symmetric and Degenerated AND gate	16.78	62dB	57dB

4.5.2 Design methodology for CIDRA

The absence of DC bias current makes the design of dynamic structures unconventional. Even though the gain and noise depend on similar circuit parameters they can be optimized orthogonally. Given noise, gain and T_{tot} specifications, the following design methodology can be adopted for the design of CIDRA.

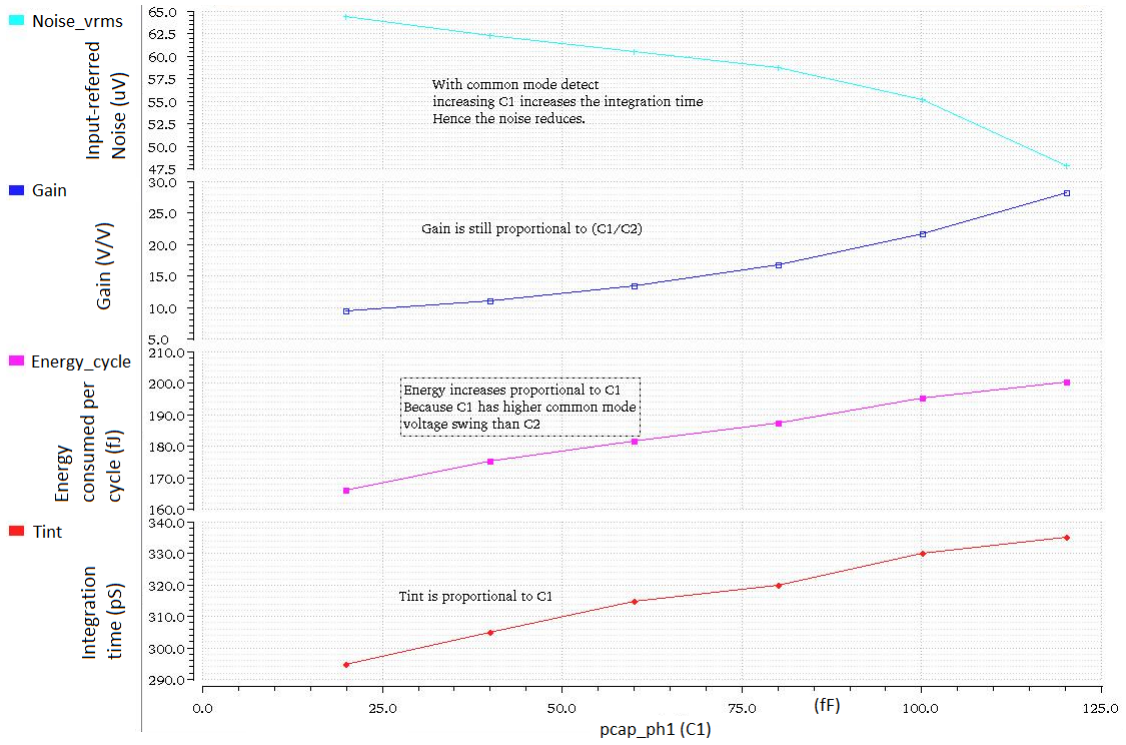

FIGURE 4.14: The input-referred noise, gain, energy and integration time as a function of C1 (*pcap_ph*1), where C1+C2=constant.

As C_1 increases, the total integration period T_{int} (see Figure 4.14 $T_{int} = T_{int1} + T_{int2}$) increases. Hence, increasing C1 (while keeping $C_1 + C_2$ constant) reduces the noise. Increasing C_1 increases the gain (see equation (4.21)). Even though the sum $C_1 + C_2$ is constant, energy increases with increasing C_1 because the common-mode voltage swing is higher across C_1.

The minimum value of C_2 is determined by the gate capacitance of the cascode. When V_{cb} switches from the supply to ground, the cascoded devices turn off and gate charge is injected into C_2. However, C_2 is the stage-2 DAC capacitance in

this design. Hence, for all practical purposes the minimum C_2 is determined by the resolution of the second stage SAR.

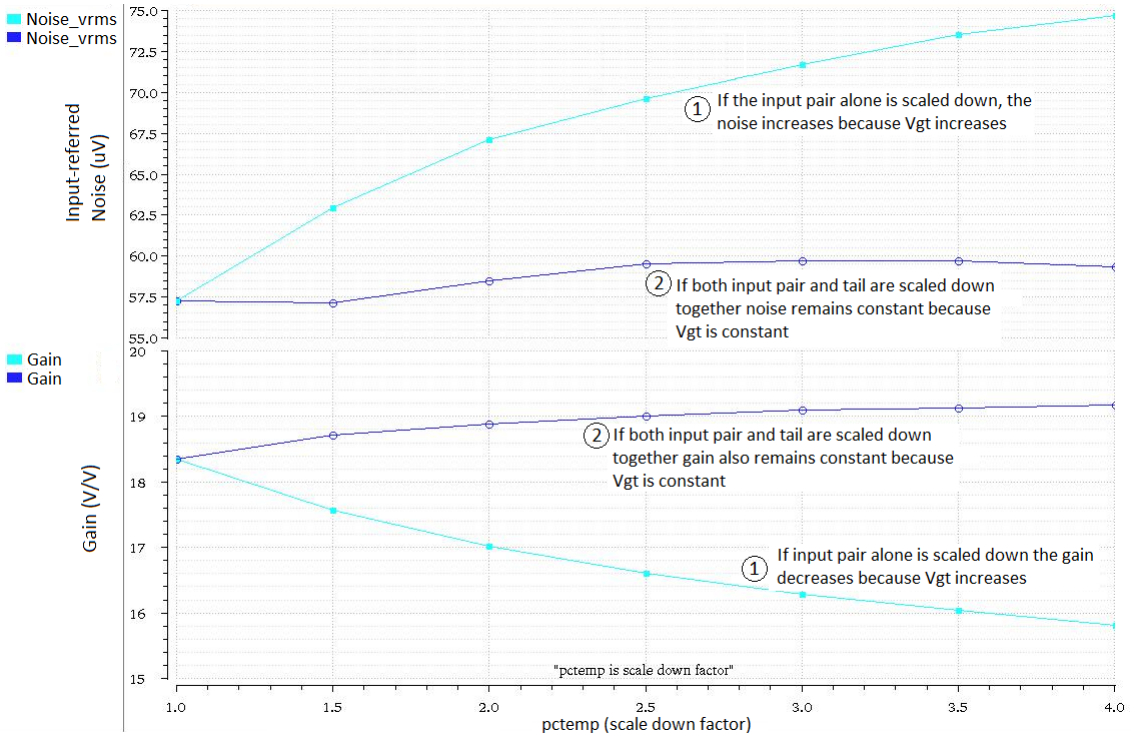

FIGURE 4.15: Input-referred noise and gain versus the aspect ratio $\left(\frac{W}{L}\right)$ scale down factor (pctemp) for input pair and tail transistor.

The gain is inversely proportional to V_{gt} of the input pair (see equation (4.9)). Hence reducing V_{gt} of the input pair increases the gain. The input-referred noise is proportional V_{gt} (see equation (4.21)), hence, reducing V_{gt} of the input pair reduces noise. Both the input pair size and the tail transistor size (switch or active source) of CIDRA decides the V_{gt} of the input pair. Scaling down the input and tail (M1,M2 and M5 in Figure 4.11) transistors together keeps both the noise and gain constant while the parasitics are reduced (see Figure 4.15).

4.5.3 Design parameters of CIDRA

Based on the design methodology explained in the previous section the transistor and capacitor sizes are finalized. The minimum capacitor C_2 for the second

pipelined stage (SAR2) is 100 fF (considering DAC resolution in the second stage). Considering C_2 and the parasitic capacitance due to common-mode detect circuit, the capacitor C_1 has been scaled up such that the typical gain is around 20 (see equation (4.21)). Table 4.3 lists the final design parameters for the casoded integrator. Table 4.4 shows the design parameters of common-mode detect circuit. Corner simulations of this design are presented in Appendix A.

TABLE 4.3: Design parameters of CIDRA in Figure 4.11

Parameter	Value
Input pair (M1 and M2)	$40 \times \frac{1\mu}{0.06\mu}$
Cascode pair (M3 and M4)	$20 \times \frac{1\mu}{0.06\mu}$
Tail switch (M5)	$10 \times \frac{1\mu}{0.03\mu}$
C1	400 fF
C2	100 fF
Supply	1 V
Input common-mode	0.6 V

TABLE 4.4: Design parameters of common-mode detect shown in Figure 4.13

Parameter	Value
NMOS (M1 - M4)	$\frac{0.12\mu}{1\mu}$
PMOS (M5 and M6)	$4 \times \frac{0.36\mu}{0.03\mu}$
Degenerating PMOS (M7 and M8)	$20 \times \frac{0.12\mu}{0.08\mu}$

4.6 Summary

Along with an introduction to dynamic amplifiers, two dynamic amplifier structures were discussed. Noise, energy consumption and gain were analysed in detail for both single-stage and cascoded integrators. The cascoded integrator shows an advantage in terms of gain. A common-mode detect circuit has been developed from a NAND gate circuit. Combining the integrator and common-mode detect

circuits, a cascoded integrator dynamic residue amplifier (CIDRA) has been presented. For the given noise and gain specifications, a design methodology has been presented for the CIDRA to optimize its energy consumption and speed.

Chapter 5

Dynamic Comparator

In the first section of this chapter, comparator circuits are discussed. In the subsequent section, a low power, low noise pseudo-latch preamp dynamic comparator (PLPDC) topology is presented. Three different comparators are compared in terms of noise, delay and energy consumption. The chapter concludes with a description of the design methodology and simulation results of the PLPDC.

5.1 Comparator circuits

Comparators are key modules for data converters as level detection is an important part of the overall operation. Minimizing the noise of the comparator is essential for high resolution ADCs. When compared to a SAR-ADC, the noise specifications of the comparators are relaxed in the pipelined SAR-ADC. The maximum noise allowed for the first stage comparator is limited by the over-range [6] in the second pipelined stage, and the maximum noise allowed for the second stage comparator is decided by the gain of the residue amplifier. In a SAR-ADC conversion cycle, the comparator and the DAC are the most active switching modules. Hence it is essential that comparator meets the noise and speed specification with the lowest power. Dynamic comparators do not need DC bias current, and they also follow

noise integration principles (refer to Chapter 3). Therefore, dynamic comparators are chosen for the study and the implementation.

5.1.1 Sense amplifier

Figure 5.1 shows one of the well-known latch-type sense amplifier circuits used in memories. Different variations of this circuit are present in the literature [15, 16]. The sense amplifier topology partially (M1-M4 and M7) resembles cascoded integrator (see Figure 4.3 in Chapter 4). In addition to cascoded integrator the sense amplifier has PMOS transistors (M5 and M6) and the outputs are cross coupled. The functionality of this comparator is explained in five phases (see Figure 5.1).

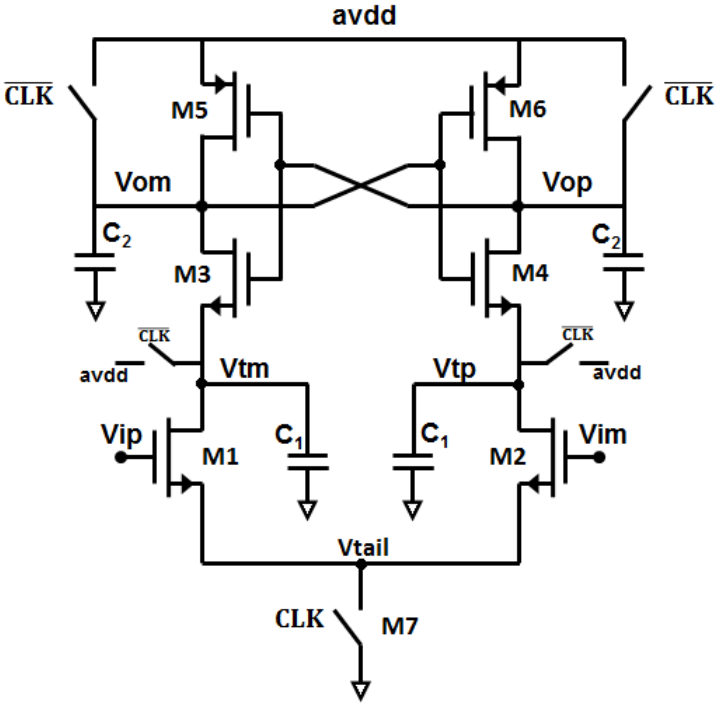

FIGURE 5.1: Sense amplifier based comparator

The first four phases of sense amplifier operation also resembles the cascoded integrator operation (see section 4.1.2 in Chapter 4). Till the forth phase the PMOS transistors remain cut-off, and the input signal is amplified by the cascoded integrator structure. Hence, first four phases can be considered as preamp part of the comparator operation.

The output noise power of this comparator is determined by the preamp phases of the operation. Since the preamp operation is similar to cascoded integrator operation, the integrator based noise analysis explained in section 4.2 of Chapter 4 is also applicable for this structure. As per the analysis, increasing the capacitance at nodes V_{tm}/V_{tp} and V_{om}/V_{op} increases the integration period and the noise reduces.

The fifth phase begins when the output V_{om}(or V_{op}) drops one PMOS threshold voltage below supply, the transistor M6 turns ON first and after a delay of (Δt_{12}) other PMOS (M5) also turns ON. The latch comprising of two inverters (M3, M5, M4 and M6) becomes active. The pre-amplified signal at nodes Vop and Vom is further amplified by latch until the absolute differential output voltage reaches to supply.

During the latch operation all the transistors (M1-M7) are ON, and there is a direct path from supply to ground. The longer the latch period, the more the current is leaked from supply to ground (especially with small differential input voltage). This direct current does not help in any way for the operation, hence, it should be reduced.

For low noise, latch needs large transistors, and large transistors increase the parasitic capacitors. During the latch operation the voltage changes at the outputs (Vop/Vom) and (Vtp/Vtm) couple to the input of the comparator through the parasitic capacitors (C_{gd} of input pair) leading to unwanted kick-back noise.

5.1.2 Double-tail comparator

Figure 5.2 shows a two stage comparator [17] which is inspired by the double-tail comparator [18]. Due to two stages, the preamp and the latch can be optimized independently. The first stage (M1-M3 in the Figure 5.2a) of this circuit is a single-stage integrator (refer to section 4.1.1 in Chapter 4) and the second stage is cross-coupled latch (M4-M9 in Figure 5.2b). The gain of the single-stage integrator is less than the cascoded integrator gain. The lack of gain in the first stage makes

the noise produced by the second stage also significant in the total noise power at the output. Hence, this comparator circuit is noisier than the sense amplifier (see Table 5.5). However, since it has two-stages the kick-back noise from latch to the input will be smaller than the sense amplifier.

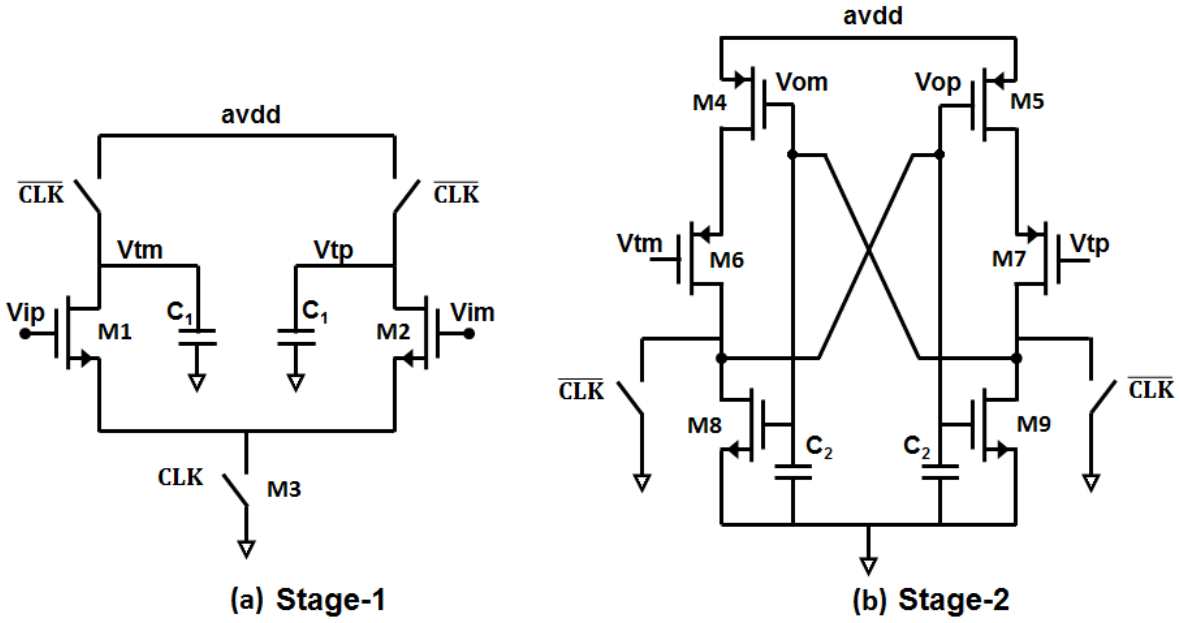

FIGURE 5.2: Double-tail comparator (a) Stage-1 (b) Stage-2

5.1.3 Pseudo-latch preamp dynamic comparator (PLPDC)

Table 5.1 summarises the advantages and disadvantages of the two comparators discussed previously. Having a cascoded integrator in the first stage is beneficial for low noise. To reduce direct current from supply to ground, the latch should be as small as possible and also fast. Increasing the gain of the pre-amplifier helps to reduce the input-referred noise due to the latch, thus allowing a reduction of the latch size. Considering these aspects, a two-stage pseudo-latch preamp dynamic comparator (PLPDC) (see Figure 5.3) has been derived.

The preamp includes a cascoded integrator. Unlike the sense amplifier, the absence of PMOS transistors in the preamp avoids any direct current from the supply to ground. The cross-coupling of the NMOS cascodes increases the gain due to positive feedback. The cross-coupling in the preamp is done with only NMOS

TABLE 5.1: Advantages and disadvantages of the sense amplifier and the double-tail comparators

Comparator type	Advantage	Disadvantage
Sense amplifier	It has cascoded integrator as preamp (high gain structure), which is good for low input-referred noise	For low noise the latch needs large transistors. Large transistors in latch increase power consumption due to direct path from supply to ground
Double-tail	It has two stages, allowing independent optimization of the latch. Smaller kick back noise	It has single-stage integrator as preamp (small gain). Hence, noise due to second stage is also significant, thus input-referred noise is high.

and no PMOS, hence the name pseudo-latch preamp. Due to the large gain in the preamp (compared to the single stage integrator) the second stage (latch) can be small (compared to preamp) making the circuit power efficient. For better noise performance, the latch in the double-tail circuit needs M6 and M7 to be bigger, which adds parasitic capacitance. The transconductance of M6 and M7 in the double-tail is less compared to the sense amplifier because of degeneration. Because of the above two reasons, the second stage of the double-tail comparator is slow compared to the sense amplifier. Hence, the sense amplifier circuit (without tail transistor M7) is used as the second stage. Figure 5.4 shows one transient cycle of PLPDC, and the functionality is explained below in four phases.

In the first phase CLK is low. It is the reset phase for the comparator, and all of the transistors are OFF.

In the second phase, CLK is high. The source (Vtail in Figure 5.3a) of the input pair discharges to ground, and hence the input pair turns ON, and it is saturated. The differential nodes V_{tm1} and V_{tp1} discharge in proportion to ΔV_{in} through the input pair. Integration of the input signal at Vip and Vim happens in this phase.

In the third phase, CLK is high. When V_{tm1}(or V_{tp1}) drops one Vt below V_{tp2} (or V_{tm2}), the corresponding cascode device M3 (see Figure 5.3a) turns on, and

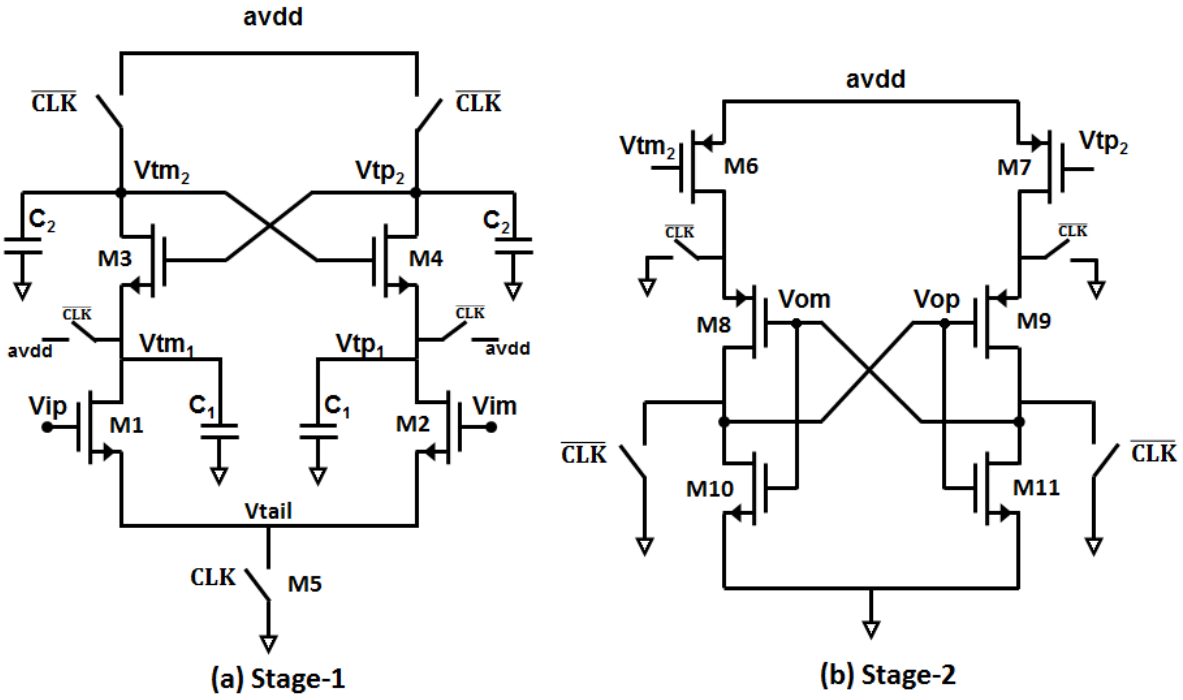

FIGURE 5.3: Pseudo-latch preamp dynamic comparator

it is in saturation. Half of the common-mode current flows out of V_{om} (or V_{op}). The period (Δt_{12}) for which only one of the cascode (M3) is ON is proportional to the differential input voltage. Hence, the differential voltage that is integrated at node V_{tm2} during that period (Δt_{12}) is proportional to the input voltage. As V_{tm2}(or V_{tp2}) starts dropping faster due to latch (M3 and M4) action, it slows down the discharging of the node V_{tp2}(or V_{tm2}). The voltage difference between the nodes V_{tp2} and V_{tm2} would eventually reach the threshold of NMOS (due to the pseudo-latch). This is the preamp phase of the comparator, and it is similar to the cascoded integrator operation (see section 4.1.2 in Chapter 4).

In the forth phase, CLK is high. When the output of preamp V_{tm2} (or V_{tp2}) drops by one threshold voltage (of PMOS) below the supply, PMOS transistor M6 (see Figure 5.3b) turns on first. And after some delay the other PMOS transistor M7 also turns on. The cross-coupled latch (M8-M11) further amplifies the signal until the absolute differential output voltage reaches the supply.

To verify the theoretical analysis, all three comparators were simulated. All three designs have similar transistor sizes in the first stage (see tables 5.2, 5.3 and 5.4).

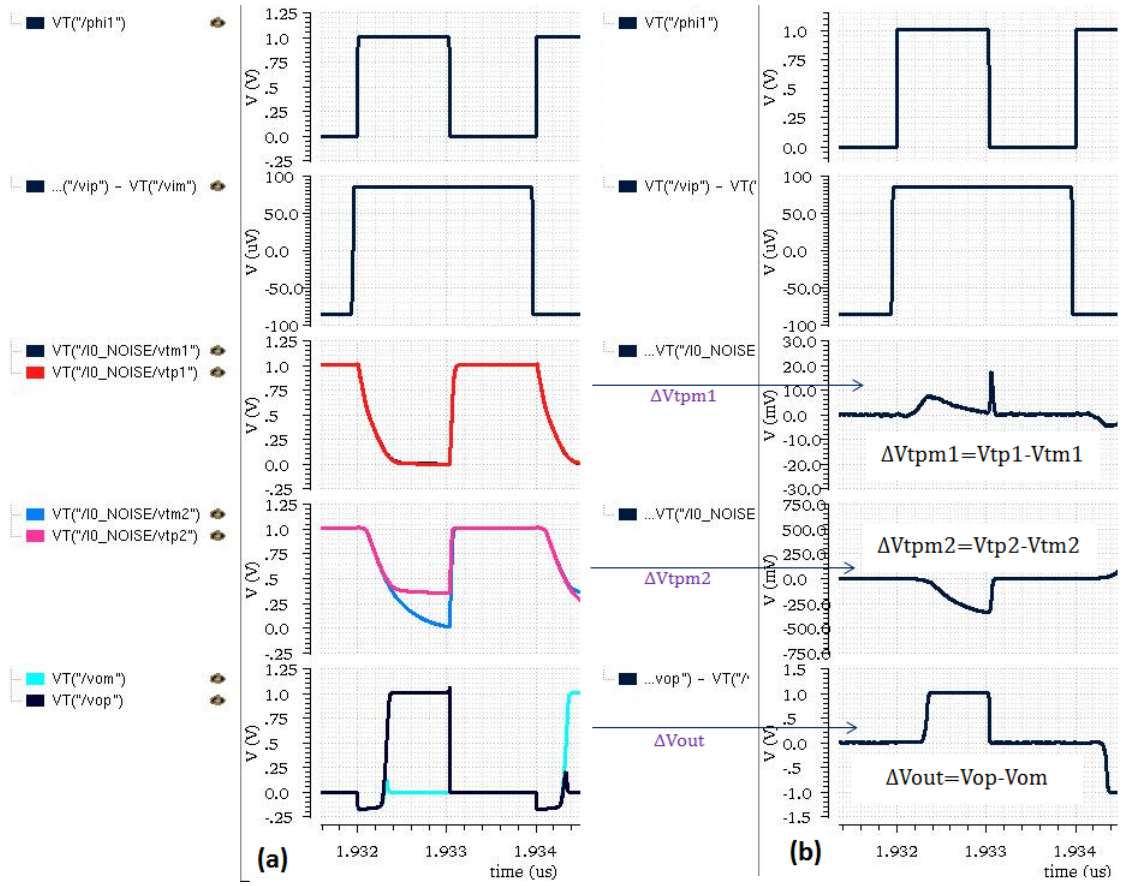

FIGURE 5.4: A transient decision cycle of the PLPDC of Figure 5.3 (a) individual node voltages (b) differential voltages

The second stage latch is 30 times smaller than the preamp for both the double-tail comparator and the PLPDC. The second stage input pair (M6 and M7) for the double-tail is made slightly bigger than the PLPDC, because for the same size double-tail was showing very high input-referred noise. However, the size is increased, ensuring that total energy consumption of the double-tail is similar to the PLPDC.

TABLE 5.2: Parameters of sense amplifier comparator (see Figure 5.1) used for comparison

Parameter	Value
Input pair (M1 and M2)	$8 \times \frac{1\mu}{0.03\mu}$
NMOS Cascode pair (M3 and M4)	$4 \times \frac{1\mu}{0.03\mu}$
PMOS pair (M5 and M6)	$4 \times \frac{1\mu}{0.03\mu}$
Tail switch (M7)	$4 \times \frac{0.5\mu}{0.03\mu}$
C1	3fF
C2	3fF
Supply	1V
Input common-mode	0.6V

TABLE 5.3: Parameters of double-tail comparator (see Figure 5.2) used for comparison

Parameter	Value
Input pair (M1 and M2)	$8 \times \frac{1\mu}{0.03\mu}$
Tail switch (M3)	$4 \times \frac{0.5\mu}{0.03\mu}$
2nd stage PMOS (M4 and M5)	$\frac{0.24\mu}{0.03\mu}$
2nd stage PMOS input pair (M6 and M7)	$2 \times \frac{1\mu}{0.03\mu}$
2nd stage NMOS (M8 and M9)	$\frac{0.24\mu}{0.03\mu}$
C1	3fF
C2	3fF
Supply	1V
Input common-mode	0.6V

TABLE 5.4: Parameters of the PLPDC (see Figure 5.3) used for comparison

Parameter	Value
Input pair (M1 and M2)	$8 \times \frac{1\mu}{0.03\mu}$
NMOS cascode pair (M3 and M4)	$4 \times \frac{1\mu}{0.03\mu}$
Tail switch (M5)	$4 \times \frac{0.5\mu}{0.03\mu}$
2nd stage PMOS input pair (M6 and M7)	$\frac{0.5\mu}{0.03\mu}$
2nd stage PMOS (M8 and M9)	$\frac{0.24\mu}{0.03\mu}$
2nd stage NMOS (M10 and M11)	$\frac{0.24\mu}{0.03\mu}$
C1	3fF
C2	3fF
Supply	1V
Input common-mode	0.6V

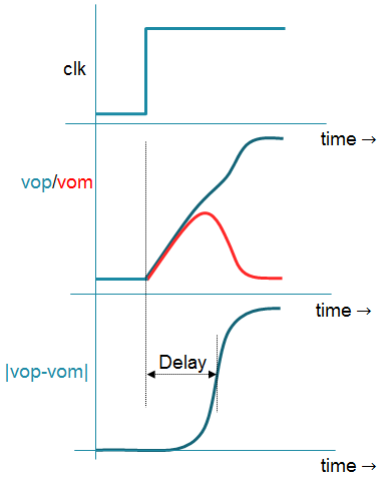

FIGURE 5.5: Comparator delay measurement

The comparator delay is measured as shown in Figure 5.5, where vop and vom are the comparator outputs. Figure 5.6 shows the comparison between the three circuits in terms of time delay and energy consumption as a function of input voltage. The table 5.5 shows the comparison between three comparators.

The following conclusions are specific to the simulation results for the parameters shown in tables 5.2, 5.3 and 5.4. Due to lack of the gain in the first stage, the double-tail comparator is slow and noisy (416 uV) compared to other two circuits. To meet the similar input referred noise as sense amplifier (151uV), the capacitors in double tail comparator needs to be increased by more than twice $\left(\frac{416u}{151u} = 2.75\right)$,

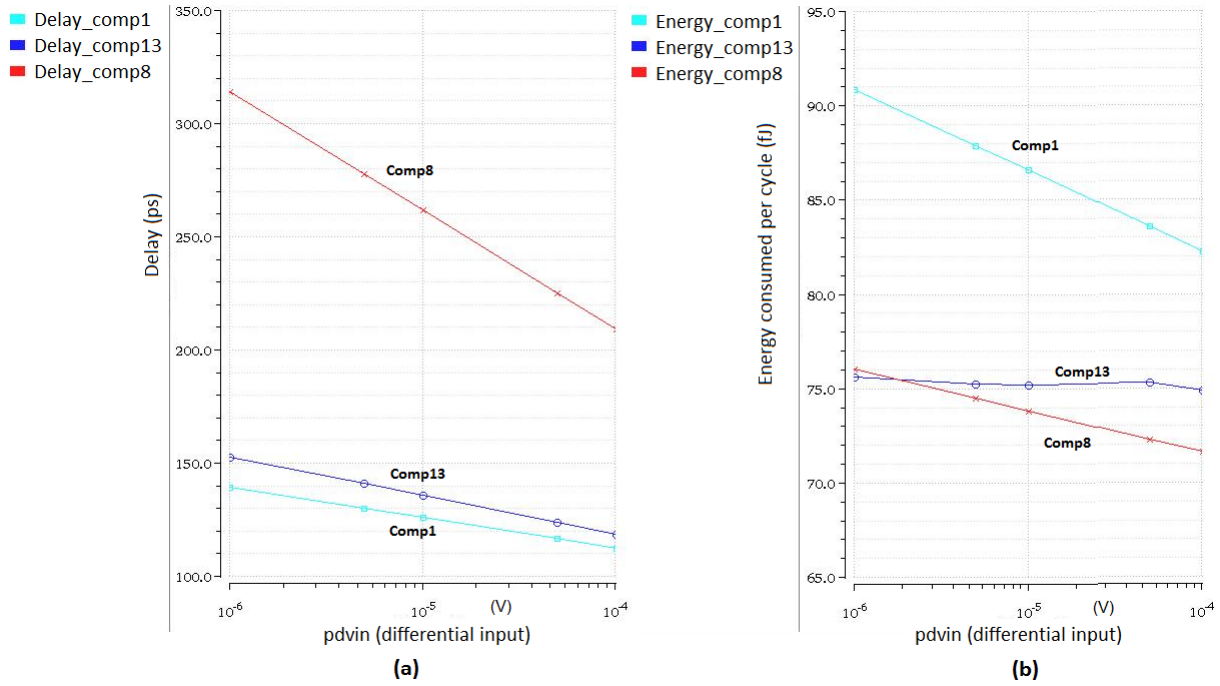

FIGURE 5.6: All the three comparators designed with similar transistor sizes (comp1=Sense amplifier; comp8=Double-tail comparator; comp13=PLPDC) (a) Delay vs differential input voltage (pdvin) (b) Energy consumed vs differential input voltage (pdvin)

and the energy consumption will also increase proportional to the capacitor. The large latch in the sense amplifier comparator leaks current during the latching phase and it is a function of input (see Figure 5.6). The PLPDC consumes slightly less energy compared to sense amplifier for similar input referred noise and delay (see Figure 5.6 and Table 5.5). Since comparator is switched several times during the SAR cycle (14 times), reduction in comparator power would be helpful. Since PLPDC is a two-stage circuit with a small latch, it will show less kick back noise compared to sense amplifier.

TABLE 5.5: Comparator comparison († error probability for 250ps operation time)

Comparator	Delay (1 μV input)	Energy (1 μV input)	Input referred noise	Error probability †
Sense amplifier	140 psec	91 fJ	151 μV	$10^{-9.23}$
Double-tail	310 psec	75 fJ	416 μV	$10^{-0.73}$
PLPDC	150 psec	75 fJ	154 μV	$10^{-8.13}$

5.2 Design methodology for the PLPDC

The design methodology of the PLPDC is similar to the CIDRA because both of them use a cascoded integrator. The following design methodology explains the optimization of speed and energy for a given noise specification for the comparator.

Keeping the input pair in weak inversion ensures low noise. Increasing C_1 and C_2 together reduces noise, but it also increases the delay and energy consumption (see Figure 5.7).

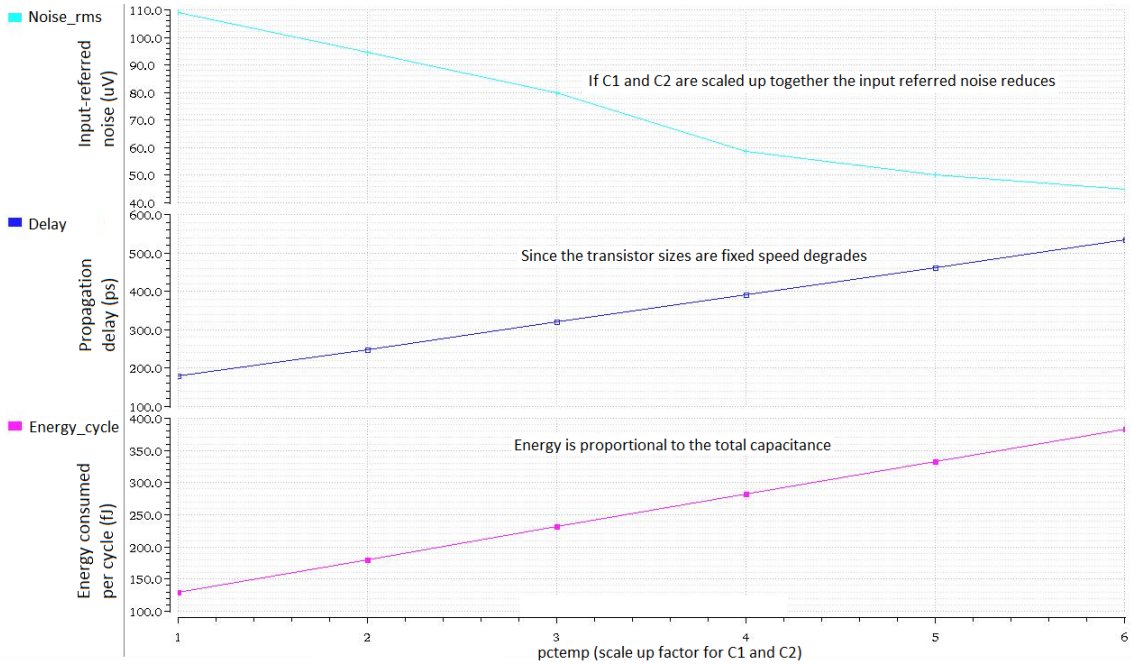

FIGURE 5.7: The input-referred noise , energy and delay as function of C1 and C2. The variable pctemp is the scale up factor for C1 and C2.

As discussed previously for the cascoded integrator, increasing C_1 for a fixed total capacitance of $C_1 + C_2$ gives higher gain in the preamp section. Hence, the noise remains constant but the speed improves (as illustrated by Figure 5.8).

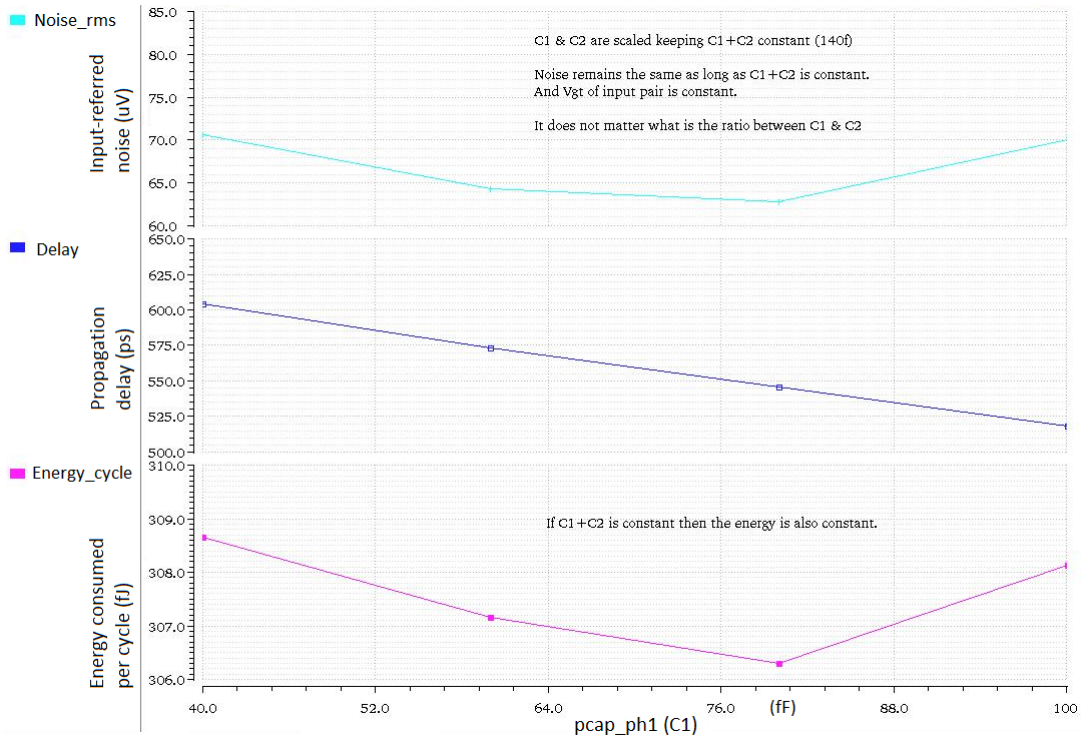

FIGURE 5.8: Input-referred noise, gain, energy and time delay as a function of C1 (*pcap_ph*1), where C1+C2=constant.

Once the noise specification is satisfied, scaling down the transistor sizes reduces the kickback noise and any additional energy loss. Figure 5.9 shows the effect of scaling down of the input pair and the tail transistor on the input-referred noise. If the input pair alone is scaled down, then the input-referred noise increases. However, if the tail switch is scaled down as well, V_{gt} of the input pair remains constant and hence the input-referred noise remains constant. On the other hand, if both the input pair and tail transistors are scaled up together, the speed of the circuit improves (see Figure 5.10), while the input-referred noise remains the same. Based on this design methodology the transistor and capacitor sizes are finalized. Tables 5.6 and 5.7 show the design parameters of the PLPDC for stage-1 and stage-2 SAR-ADCs, respectively. Corner simulations for these designs have been presented in Appendix A.

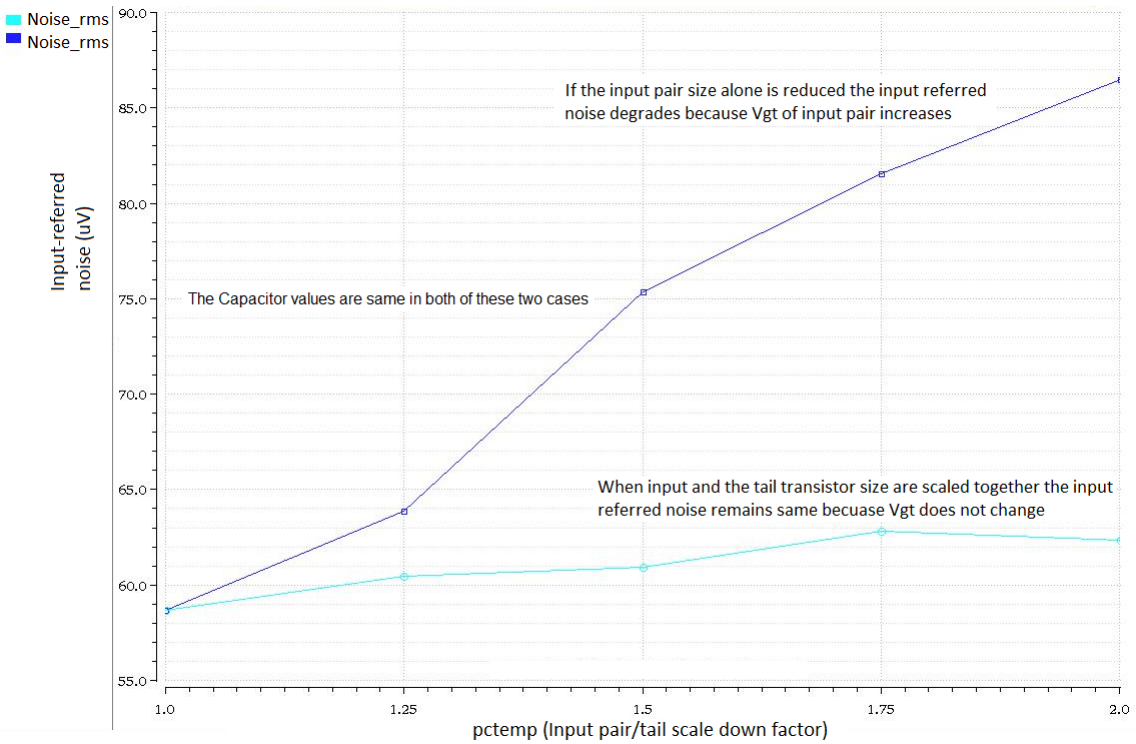

FIGURE 5.9: Input-referred noise versus the aspect ratio $\left(\frac{W}{L}\right)$ scale down factor (pctemp) for input pair and tail transistor.

TABLE 5.6: Final parameters of the PLPDC for stage-1 (see Figure 5.3)

Parameter	Value
Input pair (M1 and M2)	$12 \times \frac{1\mu}{0.03\mu}$
NMOS cascode pair (M3 and M4)	$6 \times \frac{1\mu}{0.03\mu}$
Tail switch (M5)	$4 \times \frac{0.5\mu}{0.03\mu}$
2nd stage PMOS input pair (M6 and M7)	$\frac{0.5\mu}{0.03\mu}$
2nd stage PMOS (M8 and M9)	$\frac{0.24\mu}{0.03\mu}$
2nd stage NMOS (M10 and M11)	$\frac{0.24\mu}{0.03\mu}$
C1	24 fF
C2	5.6 fF
Supply	1 V
Input common-mode	0.6V

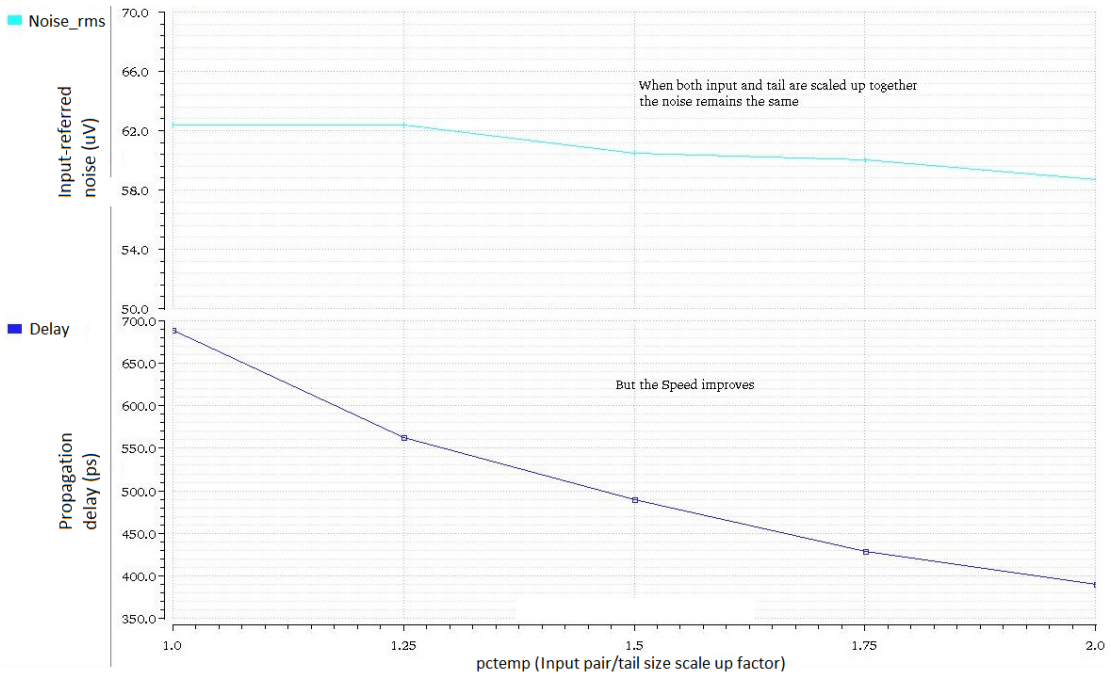

FIGURE 5.10: Input-referred noise and time delay versus the aspect ratio $\left(\frac{W}{L}\right)$ scale up factor (pctemp) for input pair and tail transistor.

TABLE 5.7: Final parameters of the PLPDC for stage-2 (see Figure 5.3)

Parameter	Value
Input pair (M1 and M2)	$8 \times \frac{1\mu}{0.03\mu}$
NMOS cascode pair (M3 and M4)	$4 \times \frac{1\mu}{0.03\mu}$
Tail switch (M5)	$2 \times \frac{0.5\mu}{0.03\mu}$
2nd stage PMOS input pair (M6 and M7)	$\frac{0.5\mu}{0.03\mu}$
2nd stage PMOS (M8 and M9)	$\frac{0.24\mu}{0.03\mu}$
2nd stage NMOS (M10 and M11)	$\frac{0.24\mu}{0.03\mu}$
C1	6 fF
C2	2.8 fF
Supply	1 V
Input common-mode	0.6 V

5.3 Summary

Three different comparator circuits were compared in this chapter. The pros and cons of each were discussed. For the design presented in Table 5.2, Table 5.3 and Table 5.4, the double tail comparator is noisy and slow compared PLPDC. For the similar noise performance the PLPDC consumes slightly less energy compared to sense amplifier. Finally, for a given noise specification, a design methodology has been presented for the PLPDC to optimize its speed and energy consumption.

Chapter 6

Calibration and configuration

The cascoded integrator dynamic residue amplifier (CIDRA) and pseudo-latch preamp dynamic comparator (PLPDC) need additional calibration and configurations in order to have better control over gain, noise and offset. In this chapter, gain calibration and a configuration option for integration time for the CIDRA are discussed. The final section presents an offset cancellation setup for the PLPDC. The simulations are done for process corners (listed in Table 6.1) and also as the temperature is varied from -40^oC to 125^oC.

TABLE 6.1: Process corners used for simulations

Name	Description
typicalmid.scs	Both NMOS and PMOS are in the typical corner.
fasthigh.scs	Both NMOS and PMOS are in the fast corner.
fnsphigh.scs	The NMOS is in the fast and the PMOS is in the slow corner.
snfphigh.scs	The NMOS is in the slow and the PMOS is in the fast corner.
slowhigh.scs	Both NMOS and PMOS are in the slow corner.

6.1 Gain calibration for the CIDRA

The CIDRA is an open-loop structure. The gain can be controlled by controlling the overall integration time. The integration period is determined by the initial

voltage($Vtpm_{ic}$) at the drain of the input pair and the gate voltage of the cascode pair (Vcb) (see Figure 6.1). A more generic expression for the gain of CIDRA can be given as,

$$A_{og} = \left[\frac{Vtpm_{ic} - (Vcb - V_{tn})}{V_{gt1}}\right]\left(1 + \frac{C_1}{C_2}\right). \tag{6.1}$$

If $Vtpm_{ic} = Vcb$, then equation (6.1) is same as that of equation (4.9). Although the typical maximum gain of that CIDRA is as high as 30, a gain of 16 (i.e., 2^4) is selected after considering linearity, process (see Table 6.1) and temperature variations. Figure 6.2 shows that with an appropriate initial condition at node $Vtpm_{ic}$, a gain of 16 is achievable across all corners.

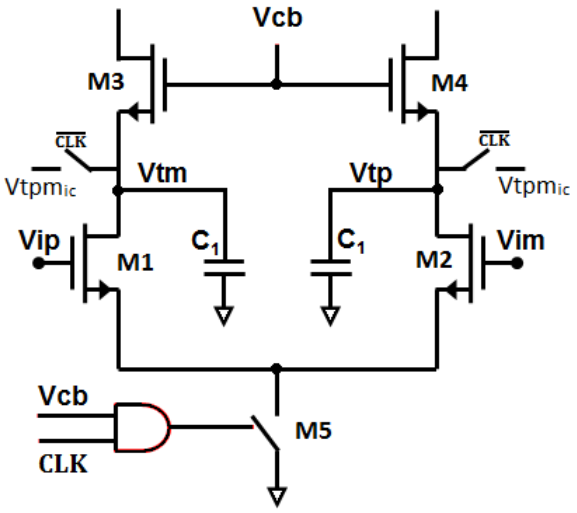

FIGURE 6.1: Input pair and cascode pair of CIDRA

6.2 Integration time configuration for CIDRA

For external noise sources like the DAC switches and reference, the CIDRA acts as a low-pass filter. The bandwidth of the CIDRA can be controlled by varying its integration time. This idea was suggested by Dr. F.M.L. Van Der Goes. Integration time, hence bandwidth can be controlled by varying the tail current (I_{tail}),

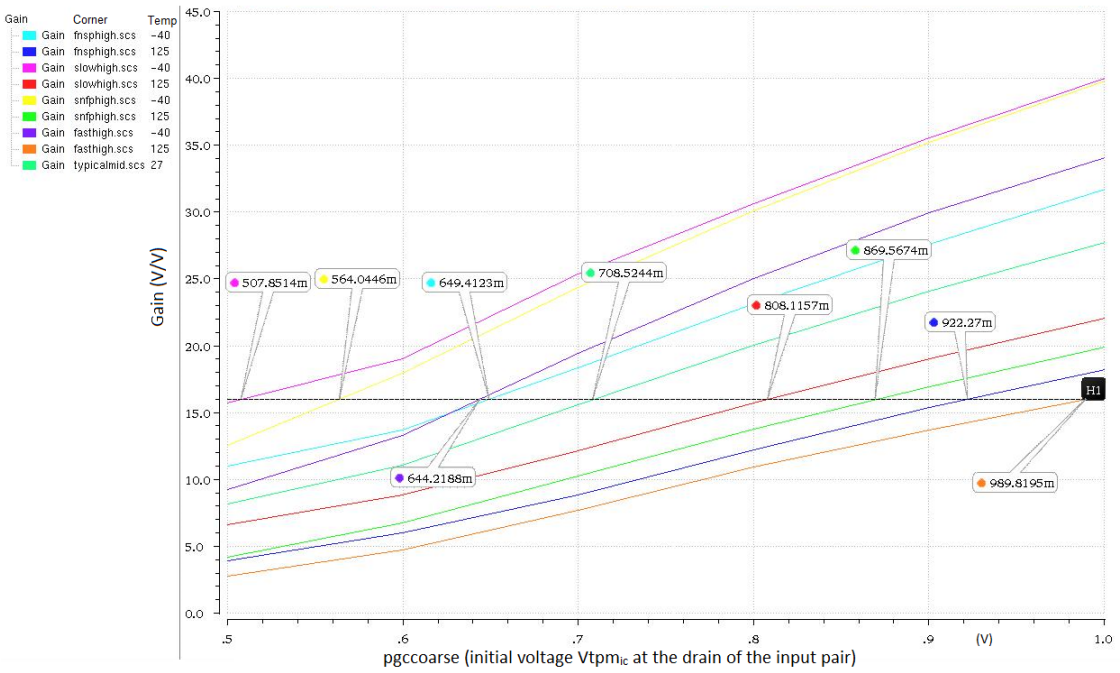

FIGURE 6.2: Gain versus $Vtpm_{ic}$ (pgccoarse in the picture) across process and temperature corner

so the tail switch is replaced by a current source (see Figure 6.3).

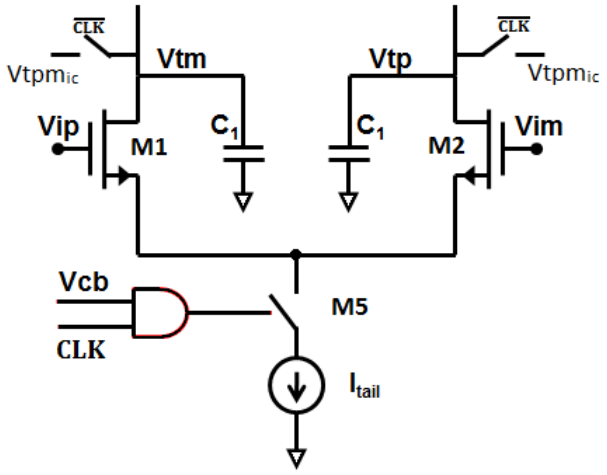

FIGURE 6.3: Tail current source for integration time configuration

The V_{gt} (overdrive) of input pair varies as the square root of the tail current. The gain should be calibrated to account for any changes due to variations in a tail current. To limit the external noise due to the DAC switches (effective resistance is 100 Ω) and the reference buffer (output impedance is 1kΩ), the integration time of 1nsec (refer to equation (3.10)) is required (see Figure 6.4) across all process

(see Table 6.1) and temperature corners. The actual tail current is scaled by 150 times the pibias using a current mirror.

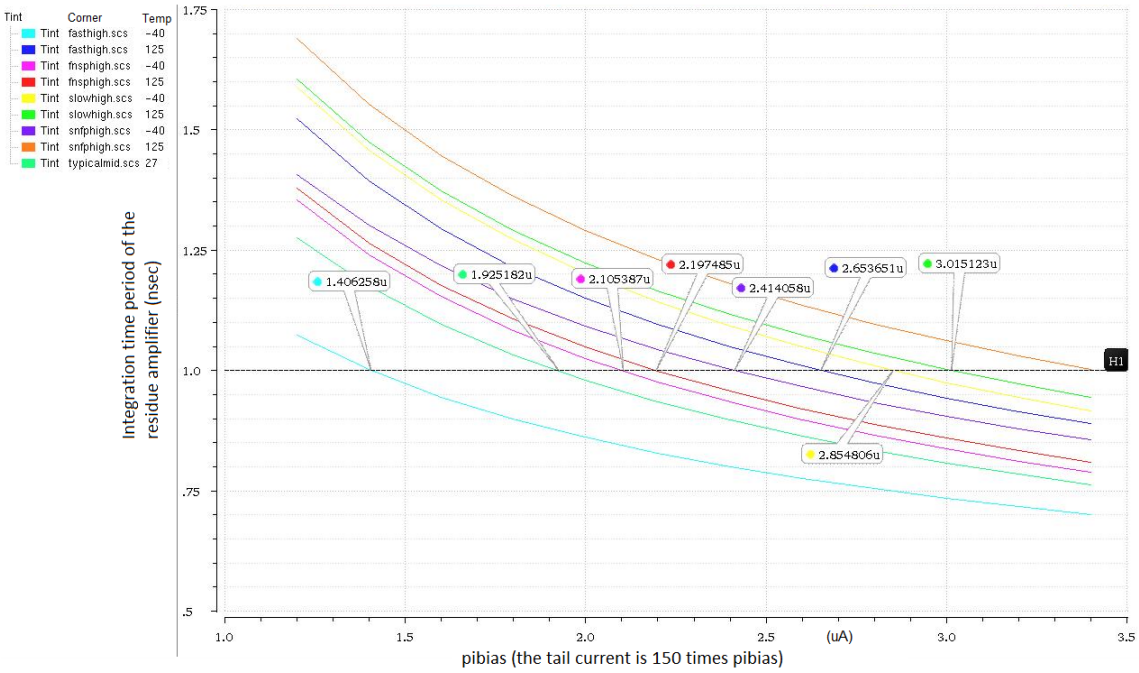

FIGURE 6.4: Integration time Vs tail current (150 times pibias)

6.3 Flicker noise reduction in CIDRA

Due to the dynamic operation of the CIDRA, a simple technique has been used to reduce flicker noise. By frequently switching the input pair between strong inversion and accumulation the flicker noise can be reduced [19] (suggested by Dr. Klaas Bult). The interface traps can be flushed (hence reducing the flicker noise) by bringing the device into accumulation. An additional switch M6 is introduced at the source of the input pair (see Figure 6.5) to bias the transistors in the accumulation mode during the CIDRA inactive phase in order to reduce flicker noise.

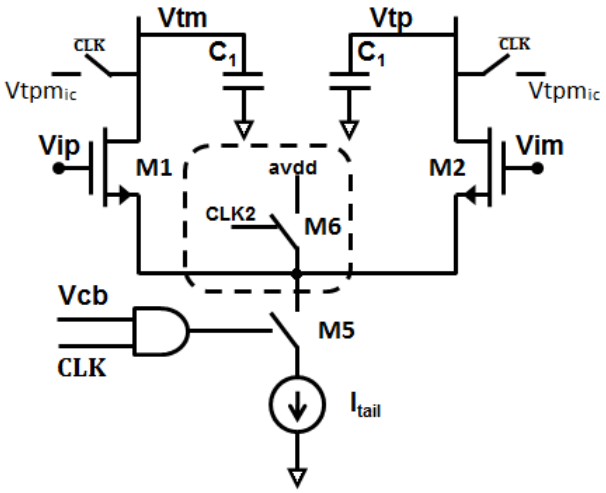

FIGURE 6.5: Switch for flicker noise reduction

6.4 Offset cancellation for PLPDC and CIDRA

Offset of the PLPDC is cancelled by adding a parallel input pair (M1' and M2' in Figure 6.6). The gate voltage of the new input pair is varied to cancel the offset. This idea was suggested by Dr. F.M.L. Van Der Goes, and it is an existing technique used in Broadcom. Since this additional input pair leaks the charge from C_1 without integration, the noise performance degrades. Hence, the area of offset cancelling pair M1' and M2' is scaled down by a factor of 6 compared to input pair M1 and M2 to reduce the charge leakage.

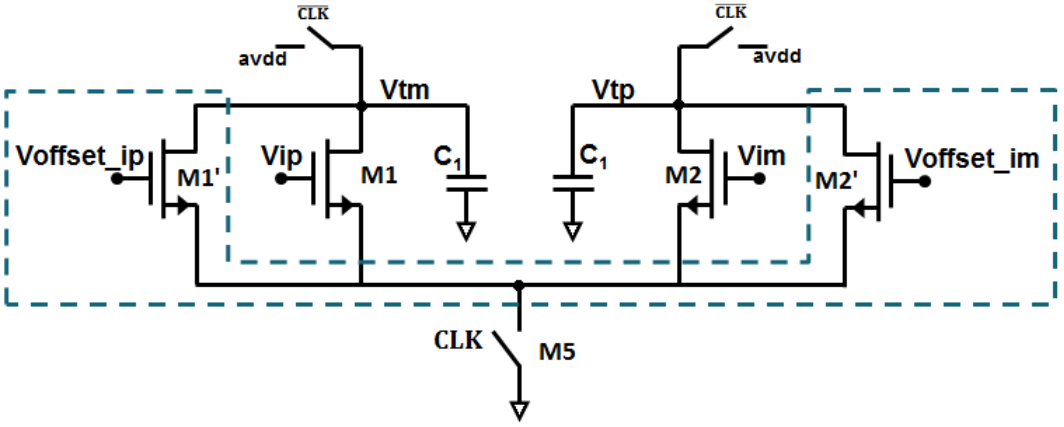

FIGURE 6.6: Offset cancellation for PLPDC

The offset of the CIDRA is cancelled by changing the DC reference voltage at the gate of the input pair. It can be implemented as part of the DAC. The offset of

the PLPDC can also be cancelled with a similar method (but it is not used in this implementation).

6.5 Summary

In this chapter, a gain calibration method and a technique to configure the integration time for the CIDRA was presented. A simple technique to reduce flicker noise by switching off the input pair was discussed. Finally, an offset cancellation method for the PLPDC was presented.

Chapter 7

Conclusions

In this chapter, my contributions to this project are clearly described. In the second section, the thesis is summarized by comparing the simulated results with expected specifications for the amplifier and the comparator. In the final section, some design improvements are suggested.

7.1 Contributions

To build a low power and high resolution ADC, the SAR ADC and the pipelined SAR-ADC architectures as described in the chapter 2 were suggested by my supervisors in Broadcom, Dr. Klaas Bult and Dr. F.M.L. Van Der Goes. My supervisors directed me towards dynamic circuits to build the residue amplifier and the comparator considering pipelined SAR-ADC as application.

- The residue amplifier (CIDRA) has two parts, a cascoded integrator and a common mode detect circuit. I have derived cascoded integrator based on the existing single-stage integrator circuit, and the common-mode detect circuit was derived based on the existing NAND circuit. I have also done the theoretical analysis (noise, gain and energy) for CIDRA.

- The comparator (PLPDC) has two parts, a preamp and a latch. I have derived the preamplifier circuit based on the existing sense-amplifier comparator, and the latch is sense amplifier itself without tail switch.
- To complete the designs, I have done corner simulations, layout (28nm) and post layout simulations for both CIDRA and PLPDC.

7.2 Summary

A survey of low power ADCs was presented in Chapter 1. The SAR based ADCs were found to be low power ADCs. A brief introduction to SAR-ADC and pipelined SAR-ADC was given in Chapter 2. With a low noise and low power residue amplifier, the pipelined SAR-ADC can reduce power (compared to SAR-ADC).

The two operating modes (steady-state mode and integrator mode) of the transconductance amplifier were described in Chapter 3. The input-referred noise of a transconductance amplifier for both of the modes was analysed. For a given time period, the transconductance amplifier operating in the integrator mode shows smaller input-referred noise compared to steady-state mode.

To build the residue voltage amplifier, a single-stage integrator and cascoded integrator which operate in the integrator mode were analysed in Chapter 4. In single-stage integrator, the gain is limited. Also, the gain and noise are interdependent. The cascoded integrator allows orthogonal optimization of gain, noise and speed. To complete the voltage amplifier topology a common-mode detect circuit was included to store the amplified differential output voltage, and cascoded integrator dynamic residue amplifer (CIDRA) was designed. The chapters ends with design methodology of the CIDRA.

In Chapter 5 advantages and disadvantages of sense amplifier and double-tail comparators were discussed. Based on the two comparators an improved pseudo-latch preamp dynamic comparator (PLPDC) was derived, that consumes less energy compared to sense amplifier. The topology and operation of PLPDC preamp resembles cascoded integrator. Hence, the design methodology of PLPDC is also similar to cascoded integrator.

The calibration and configuration options for the CIDRA and PLPDC were described in Chapter 6. The CIDRA has been provided with a voltage controlled calibration option to vary the gain. The integration time can be varied to control the noise from the references and the DAC switches. In addition a switch has been provided to reduce the flicker noise. The PLPDC has been provided with a parallel input pair for offset cancellation.

Table 7.1 gives the specification compliance matrix for the CIDRA (the circuit parameters are shown in tables 4.3 and 4.4). Compared to single-stage integrator, the CIDRA achieves 12dB higher gain for the same noise and the energy consumption. As explained in Chapter 2, the energy consumed by the amplifier is around 400fJ, which is comparable to the energy consumed by a comparator (see section C.2 in appendix C) for similar noise performance.

The proposed pseudo-latch preamp dynamic comparator consumes less energy compared to a sense amplifier based comparator for the same noise performance. Tables 7.2 and 7.3 give the specification compliance matrix for comparator in the first and second stages, respectively (the circuit parameters are shown in tables 5.6 and 5.7).

In this dissertation, a high gain, low noise, low power cascoded integrator dynamic residue amplifer (CIDRA) and a low noise, low power pseudo-latch preamp dynamic comparator (PLPDC) were designed (schematic and layout) in 28nm CMOS

TABLE 7.1: Specification compliance matrix for residue amplifier

		Expected			Simulated		
Specification	Min	Typ	Max	Min	Typ	Max	Units
Supply		1			1		Volts
Input common mode		0.6			0.6		Volts
Settling period		1		0.9	1	1.6	nsec
Differential Input		11	22		11	22	mVolts
Gain		16		10	16	30	
Noise @ input		50		41	49	55	μVolts
THD	50			50.5	56.5		dB
Energy		400			390		fJ

TABLE 7.2: Stage1 comparator specification compliance matrix († offset before correction)

		Expected			Simulated		
Specification	Min	Typ	Max	Min	Typ	Max	Units
Supply		1			1		Volts
Input common mode		0.6			0.6		Volts
Delay (LSB input)			250	110	150	250	psec
Noise @ input			300		150	260	μVolts
Energy/cycle		100			92		fJ
Input offset†				-11		11	mVolts

technology. The amplifier and the comparator are designed for Pipelined SAR-ADC application.

7.3 Limitations and suggestions for future work

- Since CIDRA is open-loop amplifier, maximum THD of the CIDRA is limited by a input differential pair. Hence, a calibration loop can be added to increase the linearity. It would also help to utilize the output swing of the CIDRA.

TABLE 7.3: Stage2 comparator specification compliance matrix († offset before correction)

		Expected			Simulated		
Specification	Min	Typ	Max	Min	Typ	Max	Units
Supply		1			1		Volts
Input common mode		0.6			0.6		Volts
Delay (LSB input)		150		104	137	225	psec
Noise @ input		300	450		266	435	μVolts
Energy/cycle		-			80		fJ
Input offset†				-14		14	mVolts

- Since CIDRA is an open-loop amplifier, the gain varies with process, temperature and supply voltage. Hence, a feedback loop (either digital or analog) can be implemented to control the gain of the CIDRA.
- A second stage can be added to increase the gain of the amplifier.
- The gain has a dependency on the initial voltage at the drain of cascodes at the beginning of amplification phase. Although, the supply is disconnected from the amplifier during the amplification phase, the supply needs to have good line and load regulation and also should be low noise.

Appendix A

Temperature and process corner simulation plots

A.1 Simulations of the CIDRA

The process and temperature corner simulations are done for CIDRA (for the parameter sizes shown in tables 4.3 and 4.4). The CIDRA has been calibrated for the gain and integration time orthogonally without altering the noise specification (refer to table A.1). The actual tail current is scaled by 150 times pibias using current mirror. The figures A.1, A.2, show that the gain and integration time can calibrated and brought close to 16 and 1nsec respectively. Maximum noise is 55 μV and maximum energy is 880 fJ. For the same calibration condition the figure A.3 shows that the minimum THD and IM3 are greater than 50dB and 53dB respectively. The mismatch simulations (refer to figures A.4 and A.5)show that maximum offset of the CIDRA is $\pm$2.6 mV (σ), and after the correction the offset can be reduced to $\pm$160 μV (σ).

TABLE A.1: CIDRA : Initial drain voltage of input pair (pgccoarse) and tail current (pibias) calibration values

Corner	Temperature	pibias	pgccoarse
typicalmid.scs	27^oC	1.9uA	709mV
slowhigh.scs	-40^oC	2.9uA	508mV
slowhigh.scs	125^oC	3uA	808mV
snfphigh.scs	-40^oC	2.4uA	570mV
snfphigh.scs	125^oC	3.4uA	870mV
fnsphigh.scs	-40^oC	2.1uA	650mV
fasthigh.scs	125^oC	2.2uA	922mV
fasthigh.scs	-40^oC	1.4uA	644mV
fasthigh.scs	125^oC	2.7uA	990mV

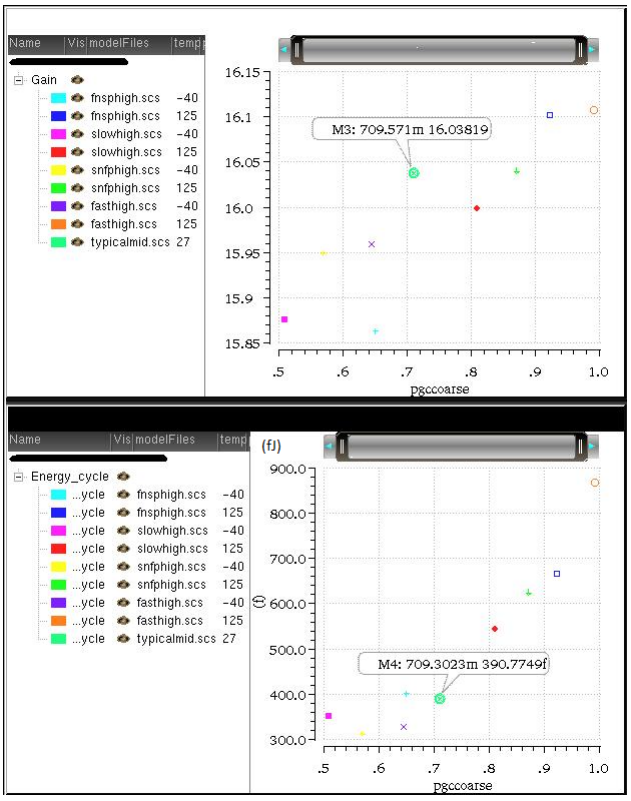

FIGURE A.1: CIDRA : Temperature and Corner simulations results of Gain and Energy/cycle

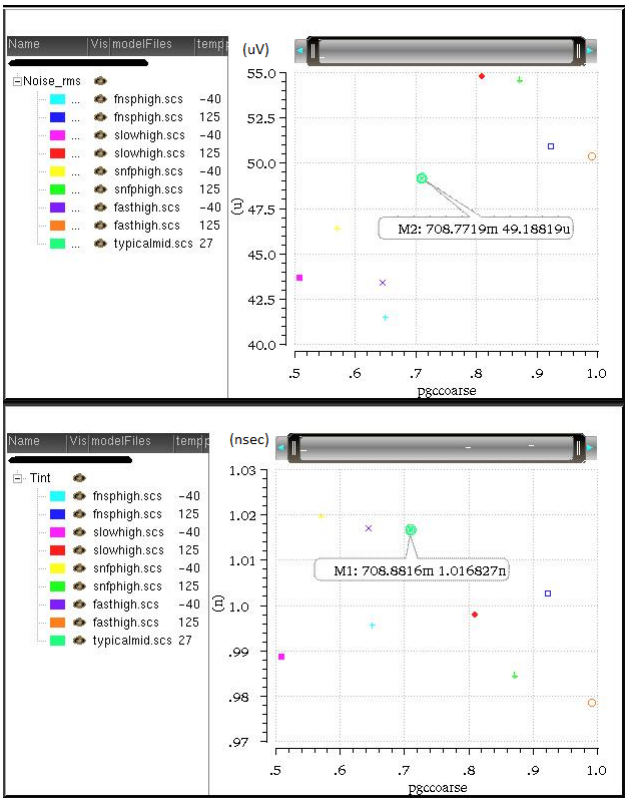

FIGURE A.2: CIDRA : Temperature and Corner simulations results of Noise(input referred) and Integration time

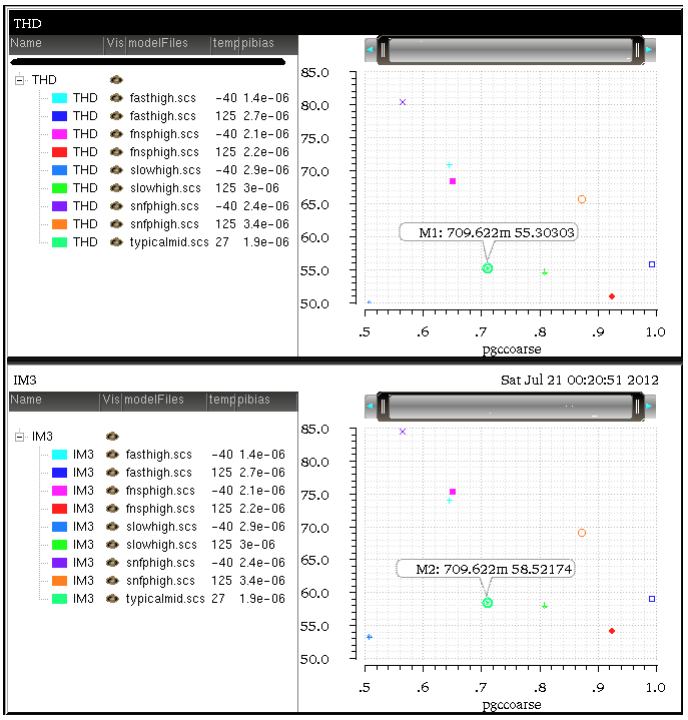

FIGURE A.3: CIDRA : Temperature and Corner (two tone) simulation results of THD and IM3

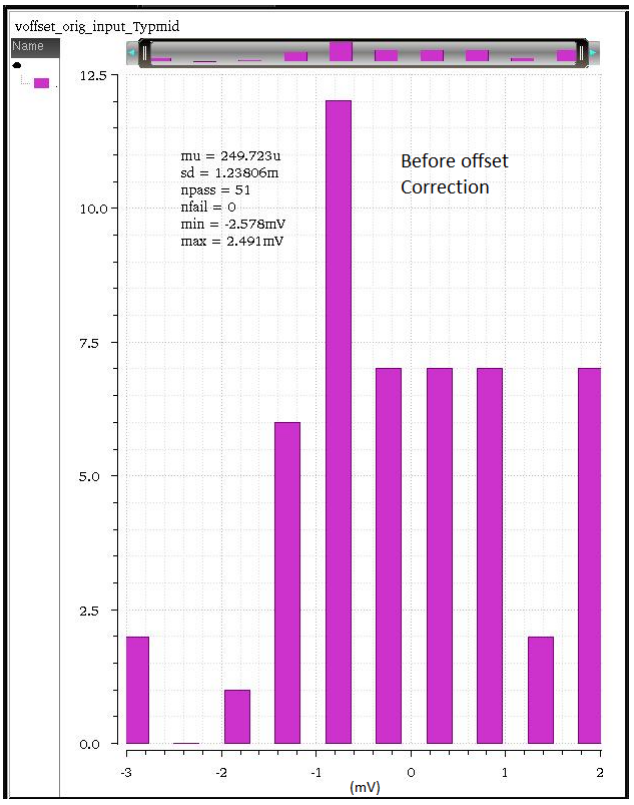

FIGURE A.4: CIDRA : Input referred offset before correction

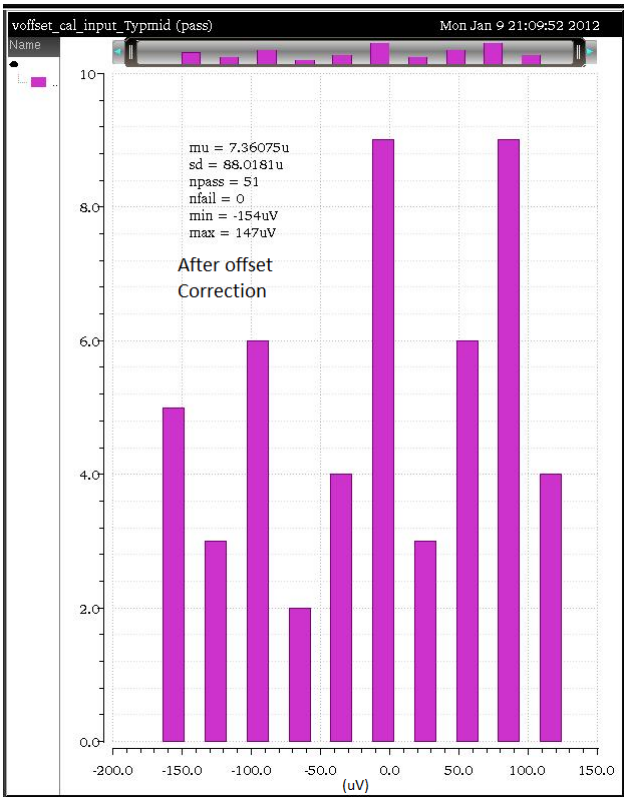

FIGURE A.5: CIDRA : Input referred offset after correction

A.2 Simulations of the PLPDC

The figures A.6 and A.7 show that for process corner and temperature variations (for the parameter sizes shown in tables 5.6 and 5.7). The maximum noise voltage and delay of the comparator in the first pipeline stage is 265 μV and 260psec respectively, and the maximum energy consumed is 110fJ. For the comparator in the second stage, the maxim noise is around 440 μV and the maximum energy consumed is 120fJ (refer to figures A.8 and A.9). For the comparator in the second stage, only the first stage is scaled down to reduce the kick back noise. Hence, the noise degrades and also the gain from preamp reduces.

For the comparator in the first stage, the figures A.10, A.11 and A.12 show the original offset, offset after correction and the voltage required at the parallel input pair to correct the offset respectively. Similarly for the comparator in the second stage, the figures A.13, A.14 and A.15 show the original offset, offset after correction and the voltage required at the parallel input pair to correct the offset respectively.

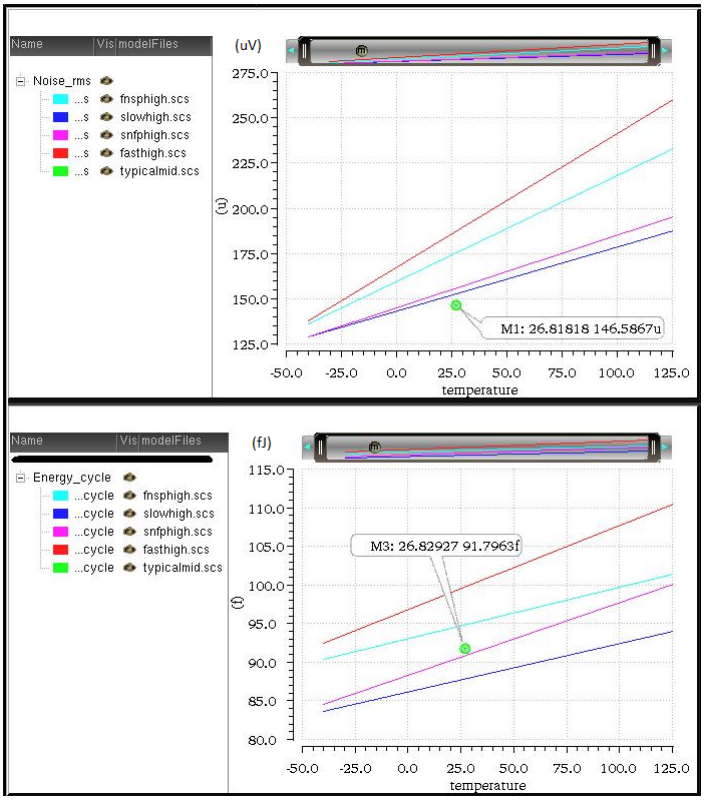

FIGURE A.6: Comparator-1 : Temperature and Corner simulations results of Noise(input referred) and Energy/cycle

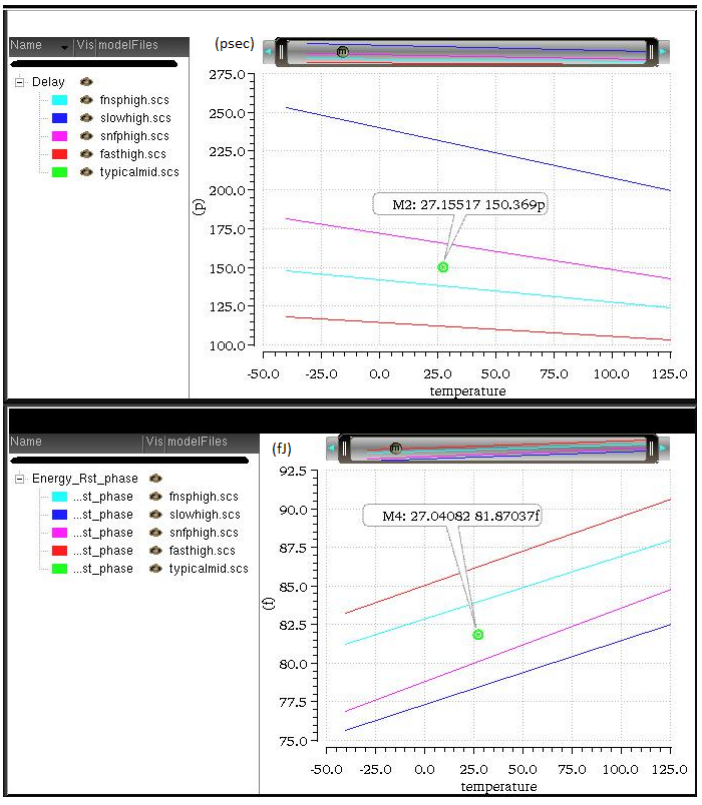

FIGURE A.7: Comparator-1 : Temperature and Corner simulations results of Delay) and Energy/cycle in the reset phase

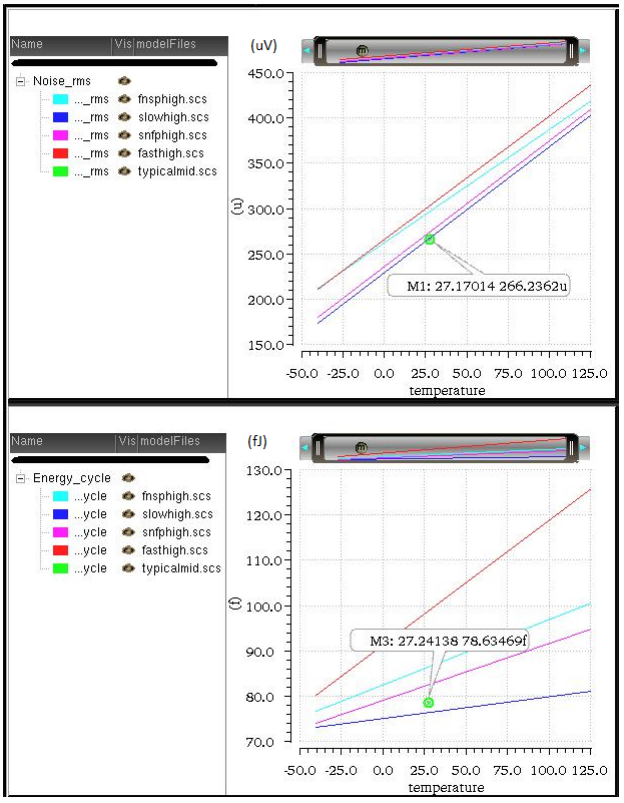

FIGURE A.8: Comparator-2 : Temperature and Corner simulations results of Noise(input referred) and Energy/cycle

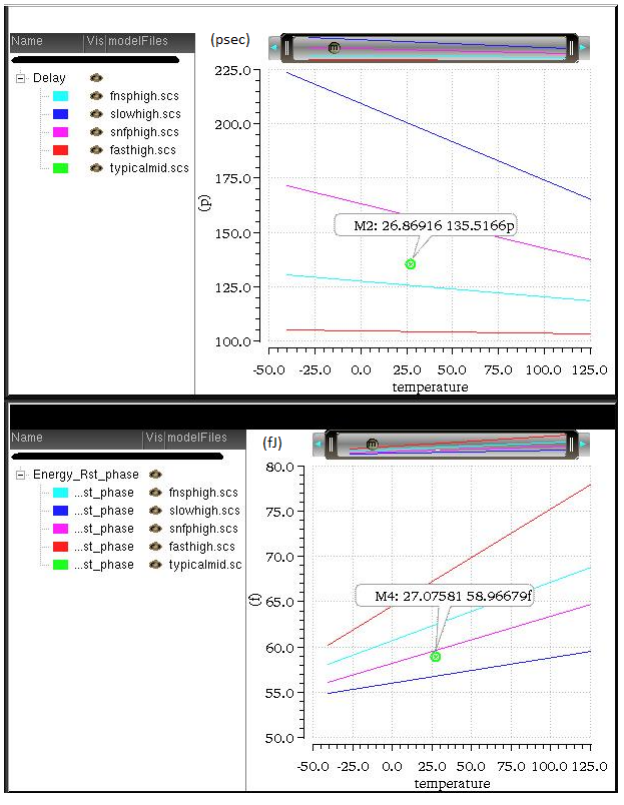

FIGURE A.9: Comparator-2 : Temperature and Corner simulations results of Delay) and Energy/cycle in the reset phase

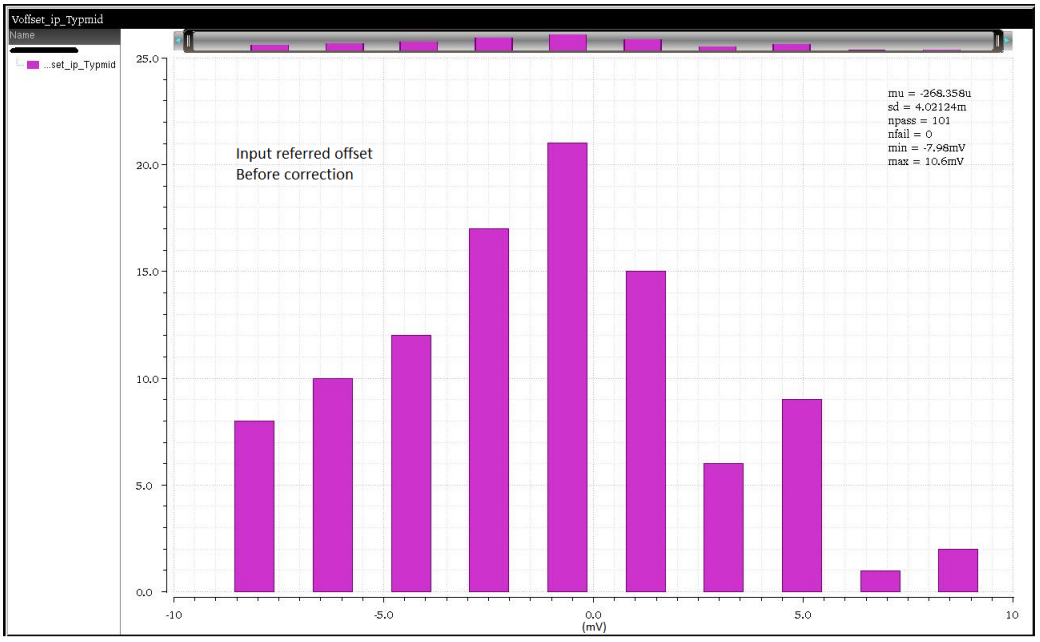

FIGURE A.10: Comparator-1 : Input referred offset before correction

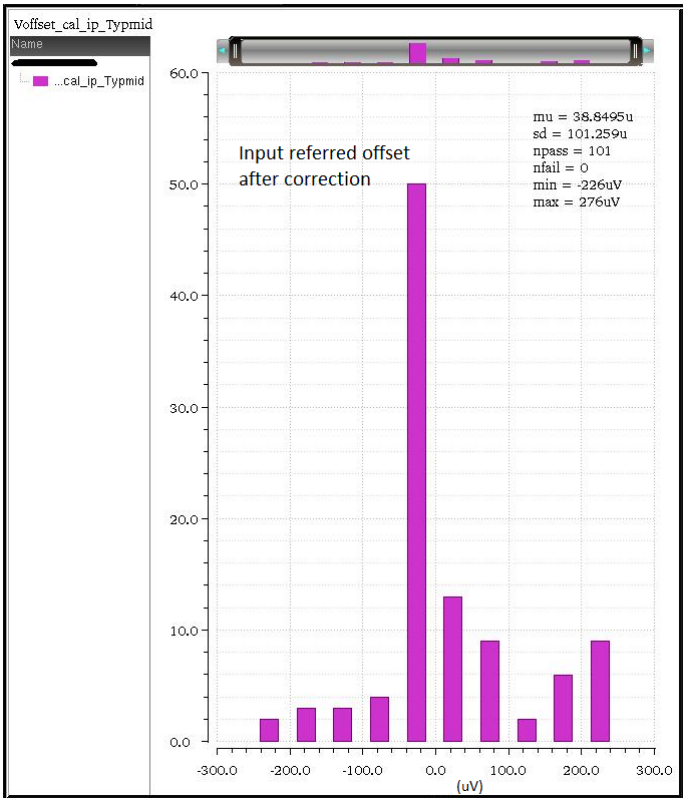

FIGURE A.11: Comparator-1 : Input referred offset after correction

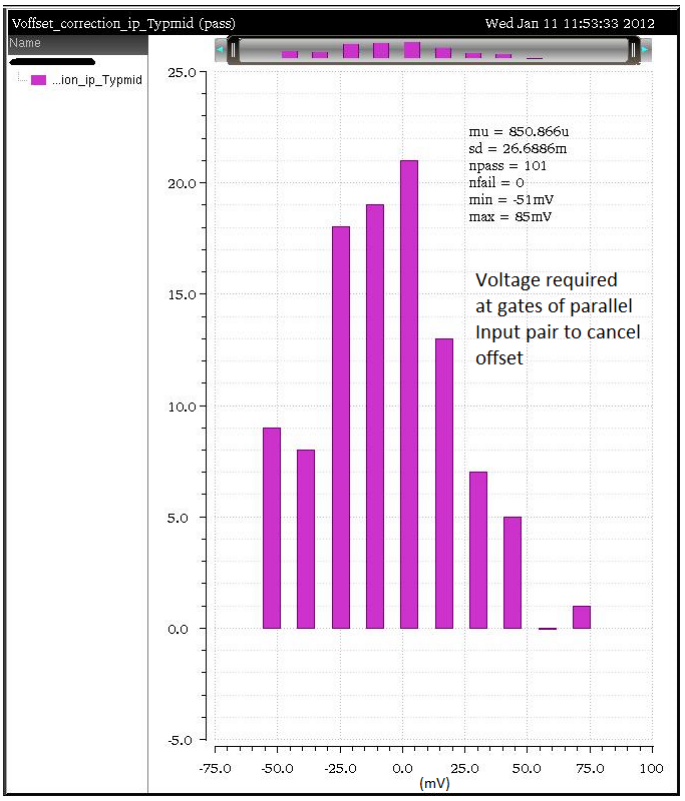

FIGURE A.12: Comparator-1 : voltage at gate of parallel input pair to cancel offset

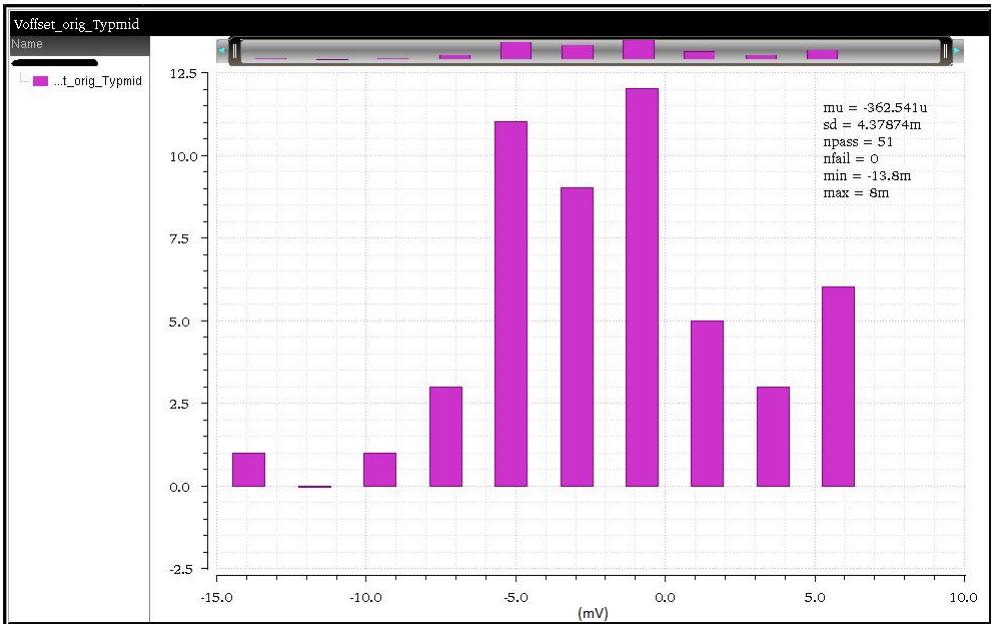

FIGURE A.13: Comparator-2 : Input referred offset before correction

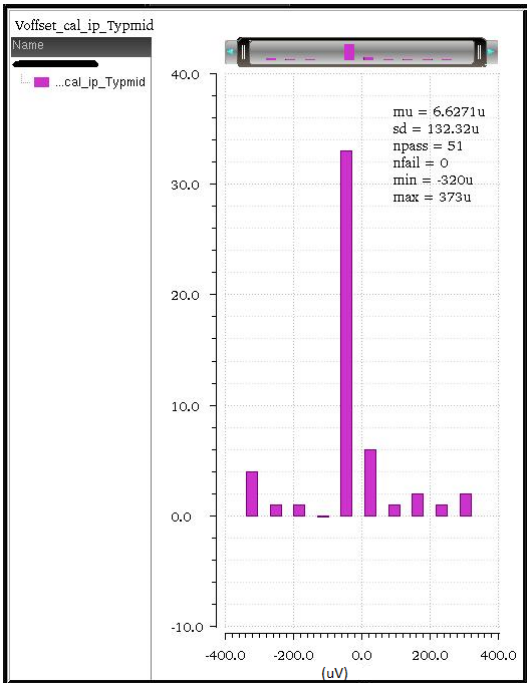

FIGURE A.14: Comparator-2 : Input referred offset after correction

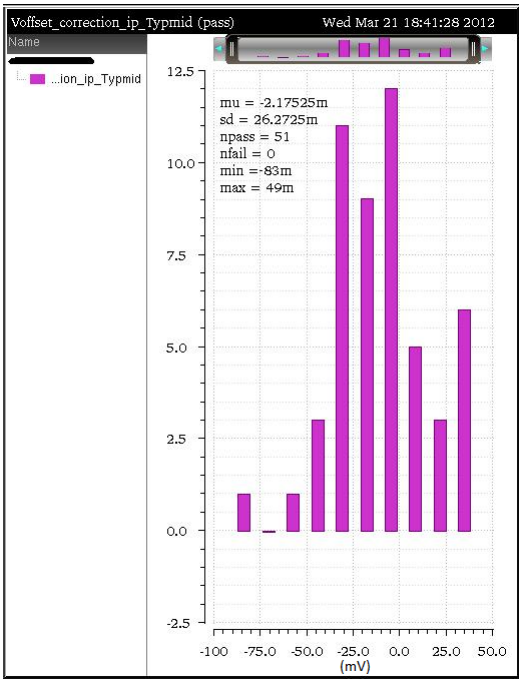

FIGURE A.15: Comparator-2 : voltage at gate of parallel input pair to cancel offset

Appendix B

Layout and post layout simulations

The layouts of CIDRA and PLPDC-1 and PLPDC-2 were done in 28nm. Figures B.1, B.2 and B.3 show the layouts of CIDRA, PLPDC-1 and PLPDC-2 respectively.

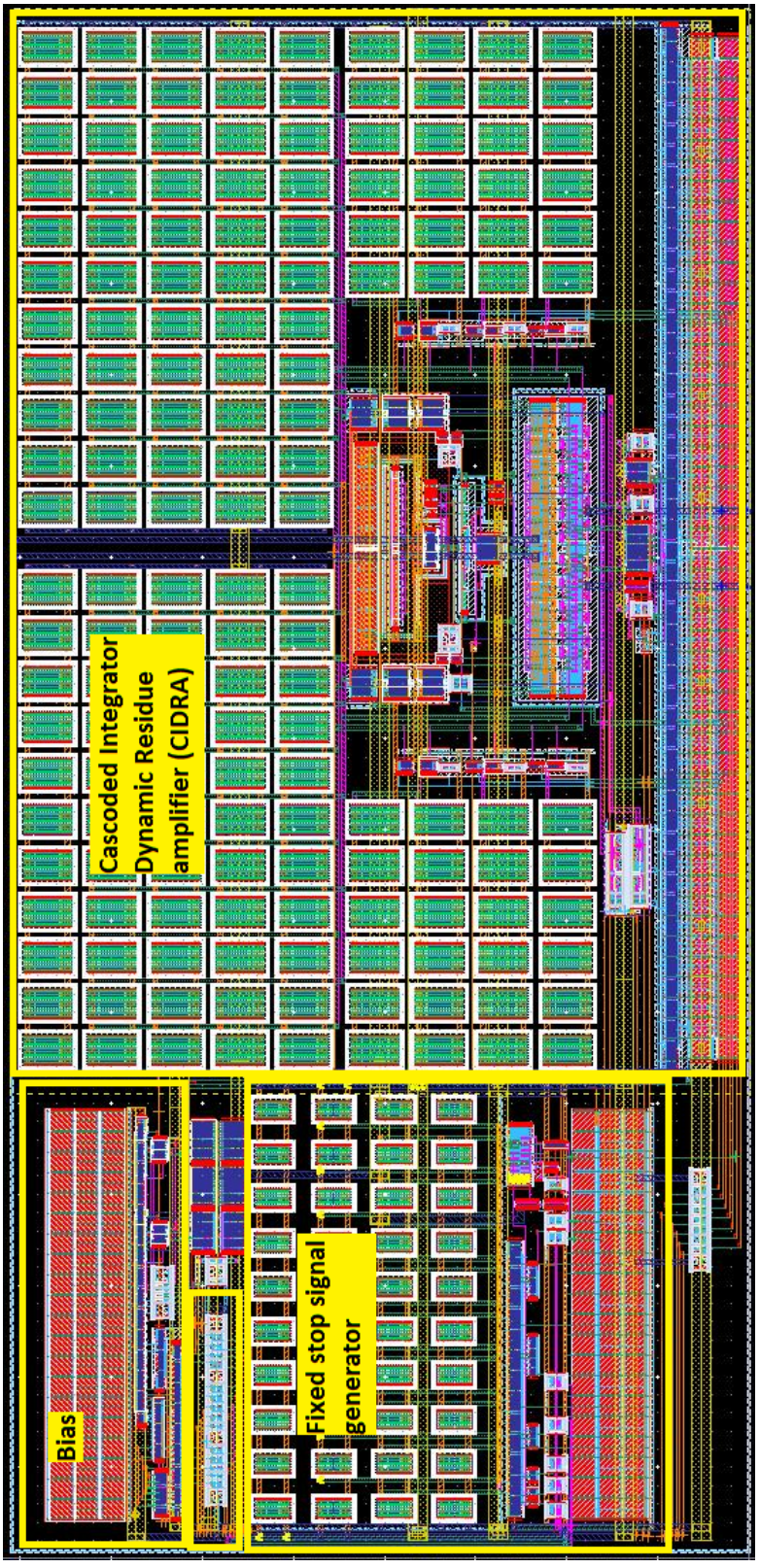

FIGURE B.1: CIDRA : Layout, and the size (width,hight) of this module is (85μm,41μm)

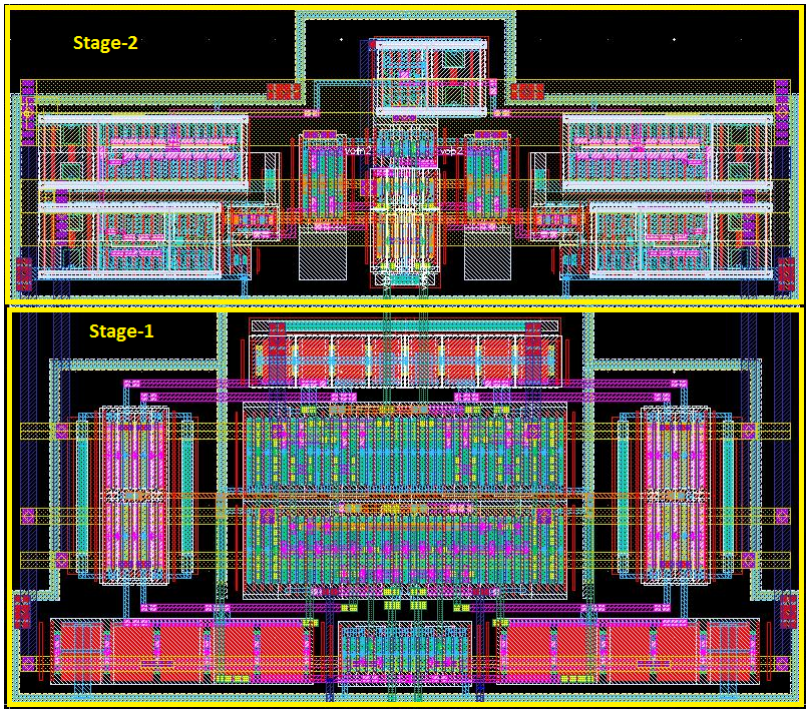

FIGURE B.2: PLPDC-1: Layout, and the size (width,hight) of this module is (12μm,11μm)

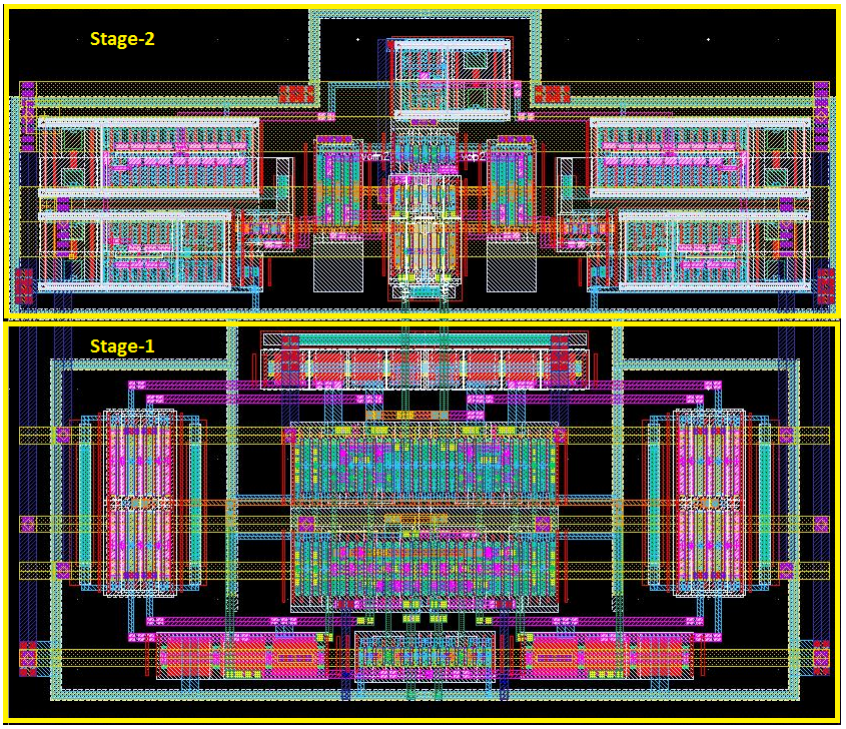

FIGURE B.3: PLPDC-2: Layout, and the size (width,hight) of this module is (12μm,11μm)

The post layout simulations using the parasitic extracted netlists were done. The comparison between the schematic simulations and the post layout simulations are shown in tables B.1, B.2 and B.3 for CIDRA, PLPDC-1 and PLPDC-2 respectively. The figure B.4 shows the transient waveforms for comparing CIDRA schematic design with the CIDRA layout. The gain in the post layout simulation is smaller than the schematic. The figures B.5 B.6 show the differential outputs of PLPDC-1 and PLPDC-2 respectively for schematic design and layout. As expected the layouts are slower than schematics. The speed degradation of layout of PLPDC-2 is more than that of PLPDC-1. The probable cause for that is, increased parasitic capacitance (C_2) at the output of preamp (refer to figure 5.3), which reduces the gain of the preamp.

TABLE B.1: CIDRA : Comparison between schematic and post layout simulations

Parameter	Schematic	Post Layout	Unit
Gain	15.88	15.33	-
Energy/Cycle	410	452	fJ
Integration time	1.08	1.2	nSec
Input offset due to parasitic mismatch	0	73	uV

TABLE B.2: PLPDC-1 : Comparison between schematic and post layout simulations

Parameter	Schematic	Post Layout	Unit
Delay	162	190	pSec
Energy/Cycle	127	145	fJ
Input offset due to parasitic mismatch	0	620	uV

TABLE B.3: PLPDC-2 : Comparison between schematic and post layout simulations

Parameter	Schematic	Post Layout	Unit
Delay	154	220	pSec
Energy/Cycle	85	102	fJ
Input offset due to parasitic mismatch	0	337	uV

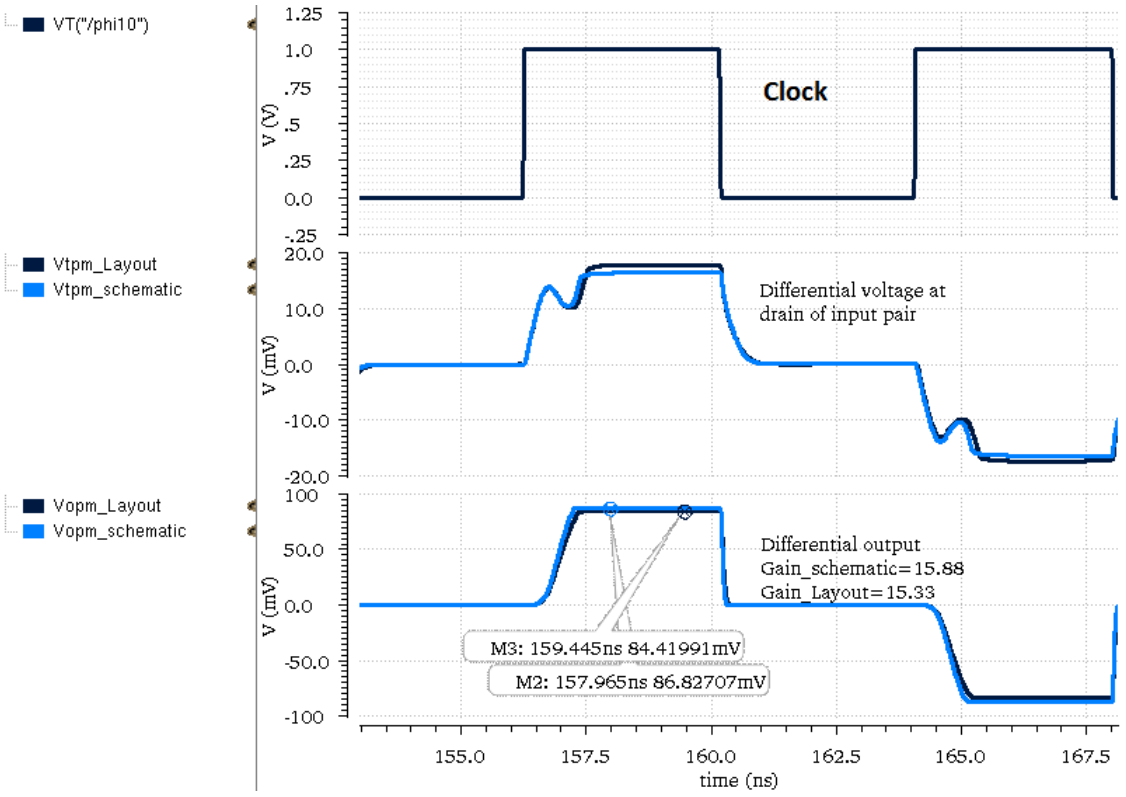

FIGURE B.4: CIDRA : Differential voltage at drain of input pair and differential output of schematic and post layout simulations

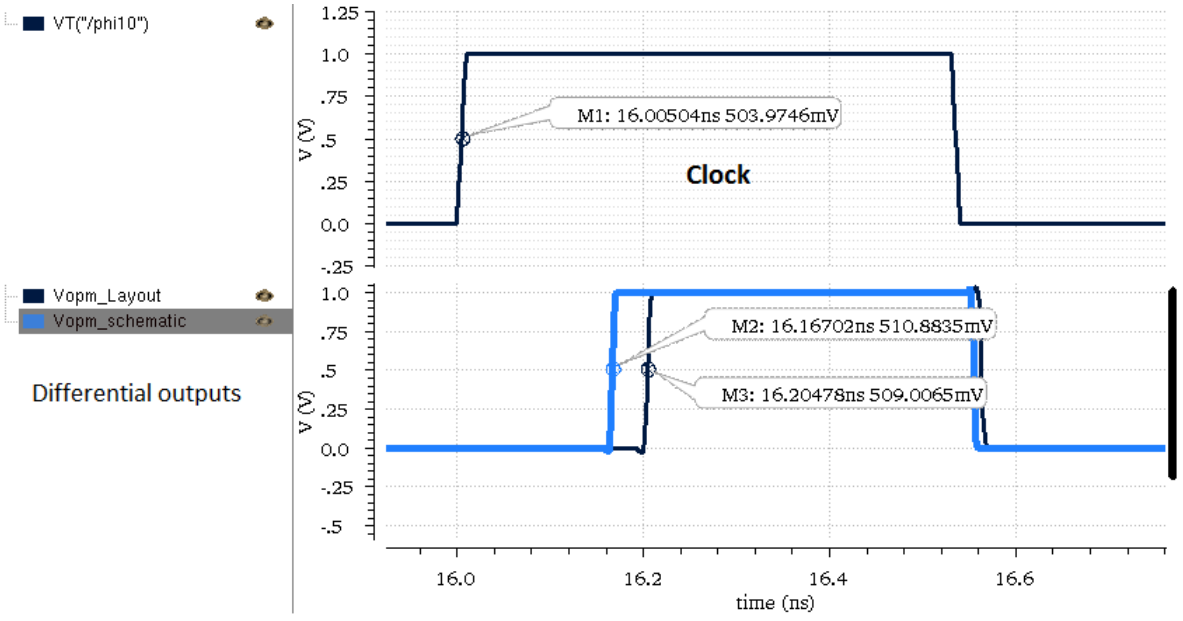

FIGURE B.5: PLPDC-1 : Differential output voltage of schematic and post layout simulations

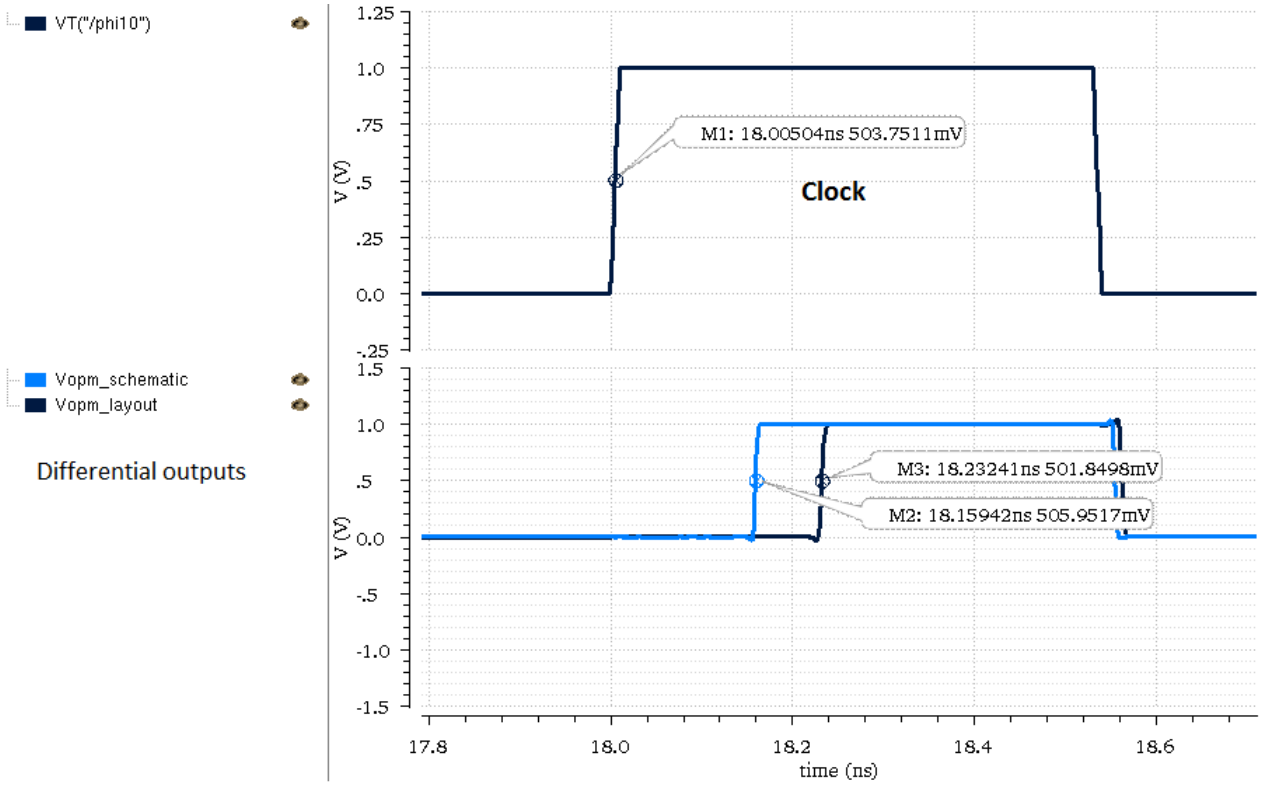

FIGURE B.6: PLPDC-2 : Differential output voltage of schematic and post layout simulations

Appendix C

Appendix C

C.1 Gain of the differential single-stage integrator

The gain of the single stage integrator (refer to figure 4.1) can be derived as given below. The output voltages can be expressed as,

$$V_{tp} = V_{ocm} - T_{int}\frac{I_{m2}}{C_1}, \tag{C.1a}$$

$$V_{tm} = V_{ocm} - T_{int}\frac{I_{m1}}{C_1}. \tag{C.1b}$$

Hence the differential output voltage is,

$$\Delta V_{out} = V_{tp} - V_{tm} = -\frac{T_{int}}{C_1}(I_{m2} - I_{m1}). \tag{C.2}$$

Assuming simplified MOS model, the currents through the input pair can be expressed as,

$$I_{m2} = \frac{g_m}{2}\left(V_{icm} + V_{im} - V_{tn}\right), \tag{C.3a}$$

$$I_{m1} = \frac{g_m}{2}\left(V_{icm} + V_{ip} - V_{tn}\right). \tag{C.3b}$$

The differential output current can be expressed as,

$$I_{m2} - I_{m1} = -\frac{g_m}{2}(V_{ip} - V_{im}) = -\frac{g_m}{2}\Delta V_{in}. \tag{C.4}$$

By substituting equation (C.4) into equation (C.2), the output voltage and gain can be expressed as,

$$\Delta V_{out} = \frac{T_{int}}{C_1}\frac{g_m}{2}\Delta V_{in}, \tag{C.5}$$

$$\Rightarrow Gain = \frac{T_{int}}{C_1}\frac{g_m}{2}. \tag{C.6}$$

C.2 The noise and energy consumption of sense amplifier based comparator

To estimate the energy for SAR some initial simulations were done with a sense amplifier based comparator (as shown in the figure 5.1). The parameters used for simulations are shown in the table C.1. To reduce the noise the total capacitance C1 and C2 have been scaled up (refer to figure C.1). From the figure it can be seen that to achieve the input referred noise less than 50uV, the comparator needs around 400 fJ of energy.

TABLE C.1: Parameters of the figure 5.1 used for estimation of energy consumption

Parameter	Value
Input pair (M1 and M2)	$16\frac{1\mu}{0.03\mu}$
NMOS Cascode pair (M3 and M4)	$8\frac{1\mu}{0.03\mu}$
PMOS pair (M5 and M6)	$8\frac{1\mu}{0.03\mu}$
Tail switch (M5)	$4\frac{0.5\mu}{0.03\mu}$
C1	10fF
C2	17.5fF
Supply	1V
Input common-mode	0.6V

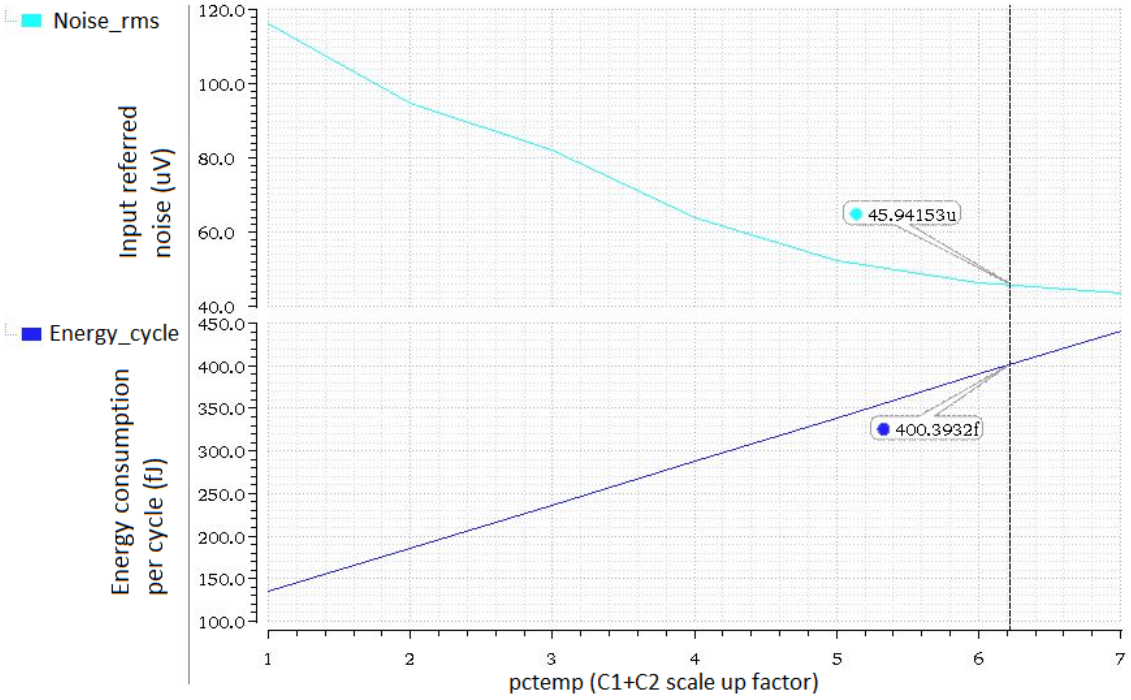

FIGURE C.1: The input referred noise and the energy consumption of a sense amplifier based comparator

C.3 Steady-state settling period and accuracy

The step response of the transconductance amplifier (as shown in Figure 3.2) for normalized gain is given by the following equation,

$$V_o(t) = V_i(t)\left(1 - e^{-\frac{t}{\tau_o}}\right). \tag{C.7}$$

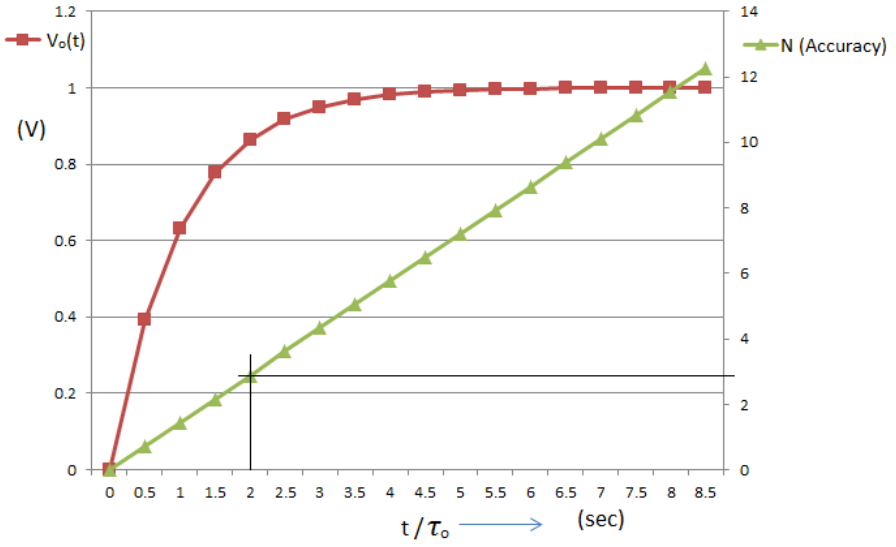

FIGURE C.2: Step response of the transconductance amplifier and accuracy(bits) versus normalized settling time

For step input the normalized output voltage as function of time (normalized by τ_o of the circuit) is shown in Figure C.2. The error between the input voltage and output voltage normalized by input voltage is given as,

$$V_{nerr} = \frac{V_i(t) - V_o(t)}{V_i(t)} = e^{-\frac{t}{\tau_o}}. \tag{C.8}$$

For the output to be N bit accurate, the error should be less than one LSB ($\frac{1}{2^N}$). Hence,

$$\frac{1}{2^N} = e^{-\frac{t}{\tau_o}}. \tag{C.9}$$

From equation (C.9), the accuracy achieved as function of settling time can be written as,

$$N = \frac{1}{log_e 2}\left(\frac{t}{\tau_o}\right). \tag{C.10}$$

The accuracy (N) is also plotted in Figure C.2. For greater than 3 bit accuracy the settling period needs to be higher than $2\tau_o$.

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