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Zero-sequence current suppression control for fault current damper based on model predictive control

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ABSTRACT

In a multi-terminal direct current (MTdc) system based on a modular multilevel converter (MMC), high-speed and large interruption capability direct current circuit breakers (dc CBs) are required for dc fault interruption. However, commercializing these breakers is challenging, especially offshore, due to the large footprint of the surge arrester. Hence, a supplementary control is required to limit the rate of current rise along with the fault current limiter. Furthermore, the operation of the dc CB is not frequent. Thus, it can lead to delays in fault interruption. This study proposes the indirect model predictive control (MPC)-based zero-sequence current control. This control provides dc fault current suppression by continuously controlling the zero-sequence current component using circulating current suppression control (CCSC) and by providing feedback to the outer voltage loop and inner current loop of MMCs. The proposed control is simulated for pole-to-pole and pole-to-ground faults at the critical fault location of an MTdc system. The simulation is performed in Real Time Digital Simulator (RTDS) environment, which shows that the predictive control reduces the rate of rise of the fault current, providing an additional 3 ms after the dc fault occurrence to the dc CB to clear the fault. Besides, the energy absorbed by the dc CB's surge arrester during the pole-to-pole and pole-to-ground fault remains the same with the proposed control.

1. Introduction

High power direct current transmission grid with a meshed modular multilevel (MMC) converter is considered a promising technology for extensive offshore wind power integration in Europe [1]. Europe's expected new wind farm capacity of 116 GW during 2022-2026 [2]. Based on submodules' (SMs) design and configuration, the MMC technology is classified into half-bridge (HB), full-bridge (FB), and Hybrid MMC [3]. However, HB-MMCs are commissioned due to their lower footprint and cost. This comes up with another drawback: the need for direct current (dc) fault interruption capability. Unlike ac systems, dc systems do not have a natural current zero crossing during a fault period; therefore, a direct current circuit breaker (dc CB) is needed. Different dc CBs have been proposed, prototyped, and tested in the last decade for application in the MTdc systems [4–6]. The dc fault interruption in HB-MMC-based MTdc systems has to be ultra-fast (< 3 ms) due to the high rate of rise of the dc current. In practice, to limit the fault current, the Fault Current Limiters, in the form of rectors, are added and used for dc fault detection [7]. However, the high value of the inductance (> 150 mH) impacts the controllability of converters and increases the capital cost of the dc grid [8].

Another method to control the fault current is to regulate the pole-to-pole voltage near the converter, known as a Fault Current Suppression (FCS) method. In [9,10], a combination of hybrid-MMC and droop control is applied, which regulates the arm voltage as a way to decrease the fault current. A similar concept for an HB-MMC is used in [11,12]. Furthermore, the authors also compared different methods of FSC. Similarly, [13] provides a soft current suppression control in the outer voltage loop. In [14], a notch filter is applied to extract the dc component and to regulate the fault current only during the fault occurrence. The suppression methods mentioned earlier imply proportional-integral (PI)-based control action, either in the outer voltage loop or by using a circulating current suppression control (CCSC). In [15], a suppression control was proposed for the FB-MMC MTdc using CSCC and a protection scheme. These controls are based on a mode selection during the fault; thus, the stability of these controls is undetermined [16,17]. The fault interruption creates a temporary instability in the dc grid, propagating into ac systems where renewable energy resources are connected, which are more susceptible to disturbances. Hence, post-fault clearance is crucial. In the existing literature dealing with suppression control, MTdc systems are simplified for the

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offshore grid and its control for the offline simulation. Thus, the dynamics of the offshore grid is removed. The existing suppression controls are implemented with PI, which introduces inherent slower performance limitations [18,19]. An optimization-based control like MPC demands high computation time. Thus, in literature, MPC-involved studies use offline simulation as the dependence on time is removed. In practice, the controller's control action must be in the acceptable time range. Hence, the real-time simulator provides us to investigate the same accept besides other advantages. The Hardware in Loop (HiL) setup indicates the physical connection of FPGA with the RTDS for the type 4 converter model as explained in [18].

In the CCSC, a zero-sequence component of dqz-frame current representation can be viewed as one-third of the dc current (i_{dc}). However, in the traditional strategies, this current is either left uncontrolled [20] or employed in energy control [21]. In this paper, we propose a controller for the mentioned zero-sequence current to decrease the fault amplitude and smooth the fault recovery. Furthermore, the model predictive control (MPC) has proven its superiority over conventional PI control in controlling complex non-linear, multiple-input multiple-output (MIMO) systems in different industrial sectors [22].

This paper introduces the indirect MPC-based zero-sequence current control employed for dc fault current suppression. The CCSC provides a reference to the outer voltage control (OVC) and direct voltage control (DVC). The proposed suppression control provides control during a dc fault, which regulates the fault current amplitude by reducing the rate of rise of the fault current. As a result, it provides an extra time margin for fault detection or dc CB breaker operation without affecting the circulating current suppression in the MMC arm. Additionally, better post-fault recovery is achieved. The proposed control can also be added to traditional PI control without creating system instability due to quadratic cost function formulation. Furthermore, the performance of CCSC is tested under different faults in the real-time digital simulator (RTDS) with the detailed equivalent models of the offshore wind farm, HB-MMC, and dc CBs.

In Section 2, the configuration of the MMC and the existing controls are analyzed. The proposed indirect MPC-based method is described in Section 3. The MTdc setup and the simulation results are elaborated in Section 4. Finally, meaningful conclusions are presented in Section 5.

2. MMC model and control

A decade of development in the modelling of MMCs has led to an accurate MMC non-linear model [19]. The dynamics of the MMC can be formulated by using two components, Σ and Δ, which represent the dc and ac characteristics of the converter, respectively. By applying the Clarke-Park transformation, the Σ and Δ ac components are translated into the stationary $dq-$frame:

$$\frac{d}{dt}\left(\vec{i}^{\Delta}_{dq}\right) = \frac{\vec{v}^{\Delta}_{Mdq} - \left(\omega L^{ac}_{eq} J_2 + R^{ac}_{eq} I_2\right)\vec{i}^{\Delta}_{dq} - \vec{v}^{G}_{dq}}{L^{ac}_{eq}}, \tag{1a}$$

$$\frac{d}{dt}\left(\vec{i}^{\Sigma}_{dq}\right) = -\frac{\vec{v}^{\Sigma}_{Mdq} + \left(R_{arm} I_2 - 2\omega L_{arm} J_2\right)\vec{i}^{\Sigma}_{dq}}{L_{arm}}, \tag{1b}$$

$$\frac{d}{dt}\left(i^{\Sigma}_{z}\right) = \frac{v_{dc}}{2L_{arm}} - \frac{v^{\Sigma}_{Mz} + R_{arm}\, i^{\Sigma}_{z}}{L_{arm}}, \tag{1c}$$

where $L^{ac}_{eq} = L_r + \frac{L_{arm}}{2}$, $R^{ac}_{eq} = R_r + \frac{R_{arm}}{2}$, $J_2 = \begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix}$, $I_2 = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$, and

$$i^{\Delta}_{d,q} = i^{U}_{d,q} - i^{L}_{d,q}, \quad i^{\Sigma}_{d,q,z} = \frac{i^{U}_{d,q,z} + i^{L}_{d,q,z}}{2}, \tag{2a}$$

$$v^{\Delta}_{Md,q} = \frac{-v^{U}_{Md,q} + v^{L}_{Md,q}}{2}, \quad v^{\Sigma}_{Md,q,z} = \frac{v^{U}_{Md,q,z} + v^{L}_{Md,q,z}}{2}. \tag{2b}$$

The definition of the zero-sequence component current is given with Eq. (1c). Its physical importance is actually its influence on the dc current since $i_{dc} = 3i^{\Sigma}_{z}$.

2.1. MMC control design

In the MTdc, each onshore converter consists of three primary control loops [23], namely, OVC, inner current control (ICC) and CCSC, as shown in Fig. 1. Fig. 2 highlights the PI controls of the onshore and offshore converters. The OVC provides references to the ICC. The setpoints to the OVC are provided by the *Dispatch level* via TCP/IP communication interface, as it is shown in Fig. 1. The setpoint signals include dc voltage $V_{dc,ref}$, ac voltage $V_{ac,ref}$, active $P_{ac,ref}$ and reactive $Q_{ac,ref}$ power, and frequency f. The selection of these signals depends upon the control mode (i.e. constant dc voltage, grid forming, active-reactive power control-mode). Dispatch controls are typically operated by the system operators. The system operators provide the setpoint based on the power ac/dc power flow and day-ahead demand.

The ICC loop generates the modulating voltages ($v^{\Delta}_{M,dq}$) based on the feedforward terms ($v^{\Delta}_{g,dq}$ and v_{dc}). The ICC and OVC are only responsible for the fundamental and the odd-harmonic components of the ac grid current. The CSCC controls the dc and even harmonic components of the ac grid current. The presence of the even harmonic results in losses within the converter. Hence, these currents are suppressed by generating modulated voltage ($v^{\Sigma}_{M,dq}$), and as a result, only the dc component is present.

The offshore converter consists of DVC and CCSC. The DVC is the simplest form of grid-forming control [23]. Like onshore converters, the offshore converter receives setpoint commands from the dispatch control. Generated modulated voltages ($v^{\Delta,\Sigma}_{M,dqz}$) are then applied to lower level control (LLC), which comprises $dq-abc$ transformation and sort and select submodule modulation. Traditionally, these controls are implemented using the PI controller by transforming ac measurements from the abc-frame into the stationary dq-frame using a phase lock loop (PLL) except grid forming control, which uses an oscillator [20]. The control system of the type-4 wind turbines is the same as reported in [18].

3. MPC-based zero-sequence current control

As the name indicates, the MPC's prediction and accuracy are purely determined by the system's behaviour. The dq-frame mathematical model of the MMC is represented by Eqs. , and is rewritten in a matrix discrete form as:

$$\begin{bmatrix} \Delta\vec{x}(k+1) \\ \vec{y}(k+1) \end{bmatrix} = \overbrace{\begin{bmatrix} \mathbf{F}(T_s) & o^T \\ \mathbf{H}(T_s)\mathbf{F}(T_s) & 1 \end{bmatrix}}^{A_d} \overbrace{\begin{bmatrix} \Delta\vec{x}(k) \\ \vec{y}(k) \end{bmatrix}}^{\vec{x}_m(k)} \tag{3a}$$

$$+ \overbrace{\begin{bmatrix} \mathbf{G}(T_s) \\ \mathbf{H}(T_s)\mathbf{G}(T_s) \end{bmatrix}}^{B_d} \Delta\vec{u}(k), \tag{3b}$$

$$\vec{y}_m(k) = \overbrace{\begin{bmatrix} 0 & \mathbf{I} \end{bmatrix}}^{C_d} \vec{x}_m(k), \tag{3c}$$

where $k \in \mathbb{N}$ indicates discrete time step, $\mathbf{H}(T_s)$ is an identity matrix, whereas $\mathbf{F}(T_s) = e^{\mathbf{A}\, T_s}$ and $\mathbf{G}(T_s) = \mathbf{A}^{-1}\left(e^{\mathbf{A}\, T_s} - \mathbf{I}\right)\mathbf{B}$. Matrices $\mathbf{A}$ and $\mathbf{B}$ are defined as

$$\mathbf{A} = \begin{bmatrix} -\frac{R_{arm}}{L_{arm}} & 2\omega & 0 & 0 & 0 \\ -2\omega & -\frac{R_{arm}}{L_{arm}} & 0 & 0 & 0 \\ 0 & 0 & -\frac{R_{arm}}{L_{arm}} & 0 & 0 \\ 0 & 0 & 0 & -\frac{R^{ac}_{eq}}{L^{ac}_{eq}} & -\omega \\ 0 & 0 & 0 & \omega & -\frac{R^{ac}_{eq}}{L^{ac}_{eq}} \end{bmatrix}, \tag{4a}$$

$$\mathbf{B} = \mathrm{diag}\left\{-\frac{1}{L_{arm}}, -\frac{1}{L_{arm}}, -\frac{1}{L_{arm}}, \frac{1}{L^{ac}_{eq}}, \frac{1}{L^{ac}_{eq}}\right\}, \tag{4b}$$

with $T_s \in \mathbb{R}$ as the sampling time, with value $T_s = 40\,\mu s$. Furthermore, the augmented state is defined as $\Delta\vec{x}(k) = \vec{x}(k) - \vec{x}(k-1)$, where $\vec{x}(k) \in$

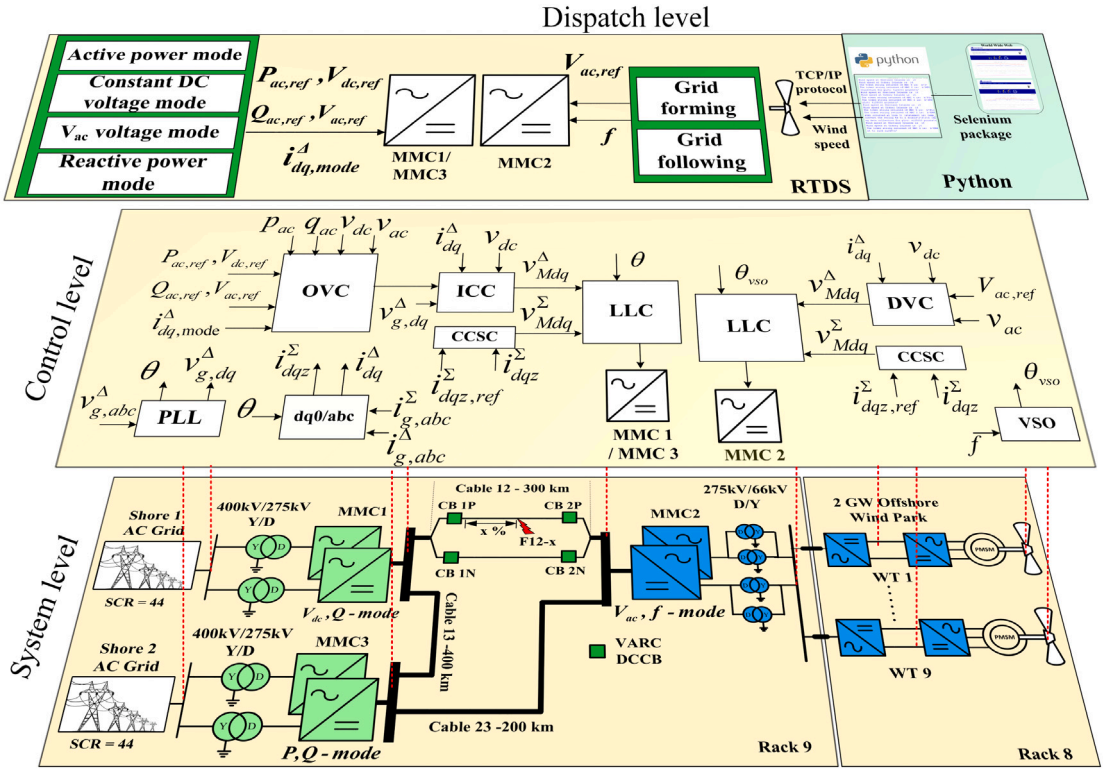

Fig. 1. Circuit and control hierarchy of Three terminal ±525 kV bipolar Mtdc simulated systems (The red dotted line indicates the ac-dc measurement).

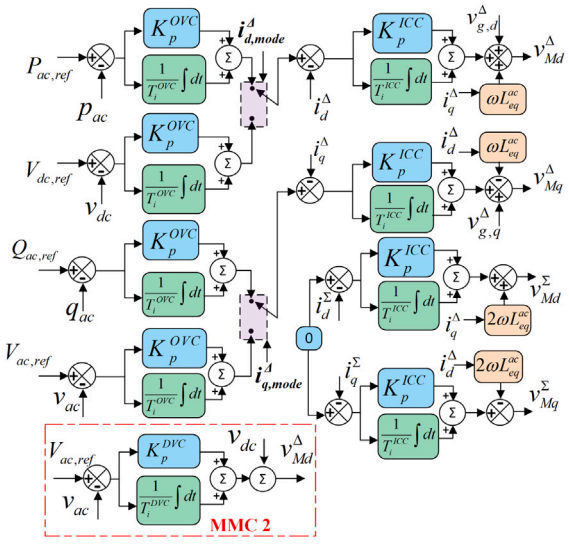

Fig. 2. The traditional PI-based MMC control design.

$\mathbb{R}^5$ indicates the system state vector at kth instant and $\vec{x}(k-1)$ indicates the vector of states for the previous sampling instance $k-1$. Similarly, the augmented input is defined as $\Delta\vec{u}(k) = \vec{u}(k) - \vec{u}(k-1)$, where $\vec{u}(k)$ represents the system inputs at kth instant and $\vec{u}(k-1)$ indicates the past inputs.

The vector $\vec{x} = [i_d^{\Sigma},\ i_q^{\Sigma},\ i_z^{\Sigma},\ i_d^{\Delta},\ i_q^{\Delta}]^T$ represents state variables, while $\vec{u} = [v_{Md}^{\Sigma},\ v_{Mq}^{\Sigma},\ v_{Mz}^{\Sigma} - \frac{v_{dc}}{2},\ v_{Md} - v_d^{\Delta},\ v_{Mq} - v_q^{\Delta}]^T$, $\vec{u} \in \mathbb{U} = [-1, 1]^5 \subset \mathbb{R}$, represents system inputs. Similarly to [18], the future control sequence is represented by the discrete Laguerre network, $\vec{\eta} \in [-1, 1]^5 \subset \mathbb{R}$, which is determined by solving the optimal control problem, and minimizing the objective (cost) function, subjected to the equality and inequality constraints:

$$\min_{\vec{\eta}} J = \sum_{i=1}^{N_p} \|\vec{x}_m(k+i|k)\|_{\mathbf{Q}}^2 + \|\vec{\eta}\|_{\mathbf{R}}^2 + I_m e(k), \tag{5a}$$

$$\text{subject to } \mathbf{M}\vec{\eta} \le \vec{b}, \tag{5b}$$

$$\vec{x}_m(k+i|k) = \vec{r}(k) - \vec{y}_m(k|k). \tag{5c}$$

Here, $\mathbf{Q} \succeq 0$ and $\mathbf{R} \succ 0$ are weighting matrices, and $N_p = 20 \in \mathbb{I}^+$ is the prediction horizon. For variables $\vec{x}_m(k)$, vector $r(k) \in \mathbb{R}^5$ is a reference signal. The Matrix $\mathbf{M}$ and the column vector $\vec{b}$ are related to the constraint information of the rate, and amplitude [18]. In reality, there will be an error due to the modelling or the signal noise. However, these disturbances can be considered in the optimal control problem, which is represented by $e(k)$. With $e(k)$ is denoted the error between the system's measured signal and the plant's predicted signal at kth instance. $I_m \succ 0$ is the weight matrix. The reference determination of the differential-current components (denoted as $i_{d,q}^{\Delta}$) remains the same as of the traditional control hierarchy as explained in Section 2.A. The CCSC mainly suppresses additive currents in the traditional control. However, the zero-sequence current component (i_z^{Σ}) reference is left uncontrolled. The previous section explains that the MMC current on dc side can be represented by the zero-sequence current component. In this paper, zero-sequence current reference is calculated by using the active power injected/absorbed in the ac system and the dc voltage as shown in Fig. 3.

To reduce the dc fault current, one of the methods is to reduce the voltage across the dc CB line inductance (l_{line}). The dc link voltage at the MMC terminals must be reduced to reduce the voltage across the dc CB line inductance. This decrease in the dc link voltage will further

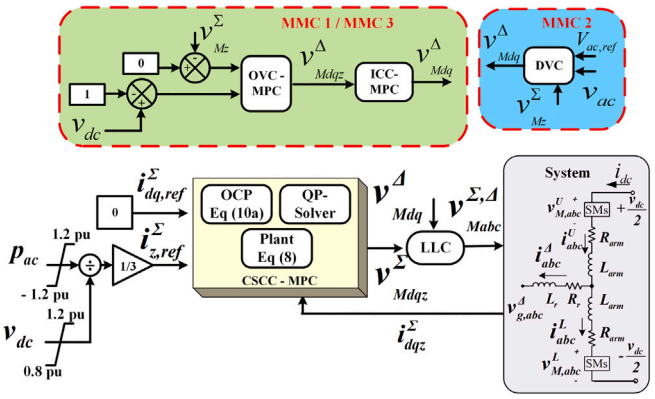

Fig. 3. Block diagram of implemented zero-sequence current control.

Table 1
Circuit parameter for the simulated system.

Parameter		Values
Rated capacity		2000 MVA
Control Mode	MMC1	V_{dc}, Q
	MMC2	V_{ac}, Q
	MMC3	P, Q
dc link voltage (v_{dc})		± 525 kV
Number of Submodules per arm (N_{sm})		240
Arm capacitance (C_{arm})		22 μF
Arm inductance (L_{arm})		42 mH
Arm resistance (R_{arm})		0.544 Ω
Transformer leakage reactance (l_r)		0.18 p.u
ac converter voltage (onshore)		275 kV
ac system voltage (onshore/offshore)		400 kV/66 kV
dc CB line inductance (l_{line})		120 mH
cable resistance per km (R_{cable})		9 mΩ
ac frequency (f)		50 Hz

decline the fault current rate of rise. During the steady state operation, the active power and the dc link voltages are inside the prescribed limits (i.e., ±1.2 p.u, and 0.8 p.u–1 p.u, respectively). Hence, the calculated zero-sequence current component (i.e $i^{\Sigma}_{z,ref} = \frac{p_{ac}}{3v_{dc}}$) remains the same as the measured zero-sequence current (i^{Σ}_{z}). Thus, no control action is provided by zero-sequence current control. However, during the dc fault period, the active power P_{ac} increases, and the dc link voltage v_{dc} decreases, which leads to saturation of the calculated zero-sequence current. Hence, the zero-sequence current control provides the control action, which temporally reduces the dc link voltage. With the reduction in the dc link voltage, the rate of rise of fault current is reduced. Further, this control action is added to the outer voltage loop and direct voltage control in the case of grid forming converters (as shown in Fig. 3) to ensure that both ac and dc component values remain within the operating limits.

4. Experimental studies

The state-of-the-art model for the ±525 kV, 2 GW dc terminals is designed and simulated to demonstrate the proposed control advantages. The multiterminal dc grid adopted in this work is a modification of the benchmark model provided by Cigre's workgroup B4.74 [20]. The following modifications are carried out in Cigre's workgroup B4.74:

- The original benchmark model rated dc link voltage as ±500 kV. However, the proposed dc-link voltage for the North Sea multi-terminal dc grid is ±525 kV. Hence, the converter and control parameters had to change to meet this requirement. In addition to this, ac voltages offshore and onshore have to be altered based on the requirements.
- The original benchmark model consists of 500 kV overhead transmission line connection, which needs to be replaced by the dedicated metallic return 525 kV submarine cables. Data for this cable have been adopted from an ongoing project.
- The original benchmark model does not include offshore components like the wind turbine model, scaling transformer, and 66 kV submarine ac cable. Hence, based on the requirement, we changed the topology and included the offshore components.

Fig. 1 shows the simulated three terminals ±525 kV metal return bipolar MTdc system programmed for the real-time simulation in the RSCAD/RTDS. The system is divided into two zones (i.e., onshore and offshore). The onshore system consists of two converters (i.e., MMC1 and MMC3). Each platform is connected to two 1 GW MMC converters. The onshore platforms are connected to a strong grid, with a short circuit ratio of $SCR = 44$, by two converter transformers with a rating of 400/275 kV, 1250 MVA. Similarly, the offshore platform has two 1 GW MMC converters connected to a wind farm via 275/66 kV, 1250 MVA. This transformer also acts as a scaling transformer. The offshore platform is connected to the wind park by a 66 kV ac cable with a distance of 7 km. The ground for the MTdc is provided at the onshore platform with a resistance value of 0.01 Ω. Type 4 converter model (detailed equivalent model, implemented on FPGA) is used for MMC 1 and MMC 2, whereas MMC 3 is modelled as type 5 (averaged RTDS model) [23]. The setup is comprehensively described in [18].

The onshore zone is connected to the offshore zone by three 2 GW, 525 kV HVdc cables with the ratings given in Fig. 1. Cable 12 has two VSC-assisted resonant current (VARC) dc circuit breakers (CBs) at each cable's end. This VARC dc CB is scaled to 525 kV with a fault interruption capability of 20 kA [5]. The wind park has nine Type-4 wind turbines, each with a rating of 2 MW at 16 m/s. Since this paper investigates dc system-level dynamics, the averaged model of a back-to-back converter of a type 4 wind turbine is considered. This back-to-back converter is modelled using Descriptor State-Space (DSS) modelling approach [24]. The grid side converter controls the dc link voltage of the type 4 wind turbine and provides reactive power support at the point of common coupling. In contrast, the machine side converter controls the torque and stator terminal voltage of the PMSM. The wind speed data is updated in real-time through a North Sea sensor using a python script [18].

Table 1 highlights the circuit parameters for the converters given in Fig. 1. The proposed controls are located in both offshore and onshore converters. In the onshore grid-tie converter station, MMC1 controls dc voltage (V_{dc}, Q-mode), whilst MMC3 controls active power (P, Q-mode). The offshore converter MMC2 is a grid-forming converter (v_{ac}, f-mode). The data for the cable are adopted from the ongoing project [25].

In a steady state, MMC2 injects an active power of 2 GW into the dc grid generated by the wind power plant. MMC3 injects an active power of 1 GW into the onshore ac grid. In order to keep the dc-link voltage constant, the remaining power is absorbed by MMC1 and injected into the onshore ac grid. Due to a full selective protection scheme being introduced [5], the internal protection of converters is disabled. The rated fault current interruption capability of the VARC dc CB is set to 20 kA, and the operating time of the dc CB is 5 ms. Furthermore, the dc fault detection is not instantaneous, so a 1 ms delay is introduced. Due to the multi-timestep simulation in the real-time simulator, the interested areas are modelled in small timesteps (2–3 μs) using processors and FPGAs. As a result, accuracy is maintained at an acceptable level. Since we investigate the control action by the proposed controller, this modelling accuracy is sufficient.

4.1. Fault amplitude identification

To identify the current hotspot in the MTdc during the fault, two different types of faults at two different cable locations are simulated.

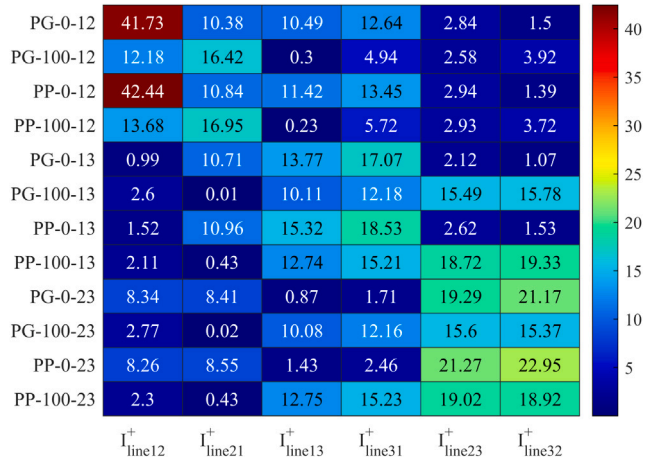

Fig. 4. Fault amplitude in kA at 6 ms for different fault types and locations in MTdc.

This work selects a positive pole-to-ground (PG) dc fault and a positive pole-to-negative pole (PP) dc fault. These faults are located at the MMC1's terminal (0%) and near the opposite terminal (100%). The nomenclature; $PG-0-12$ in Fig. 4 indicates the PG dc fault at the terminal in cable 12. Similarly, $PG-100-12$ indicates the PG dc fault at the opposite terminal of cable 12. Furthermore, I^{+}_{linexy} indicates the current measured in the cable xy from x terminal of the cable.

Fig. 4 indicates the fault current measured at $t = 6$ ms without any fault current limiting scenario at different locations during different faults. The analysis shows that, for a given MTdc system at rated power, the PG and the PP fault near the MMC1 create fault currents with amplitudes 41.73 kA and 42.44 kA, respectively. Similarly, the fault near MMC2, on cable 23 produces the second highest fault current. The converters' pre-fault condition and the operating mode determine the fault current amplitude. Since MMC1 regulates the dc link voltage to a constant value, the fault near this terminal results in a high fault current. Similarly, the fault near MMC2 produces a high fault current due to the ac power infeed. Hence, the subsequent study considers the fault near MMC1 and MMC2 on cable 12.

To understand the impact of the proposed control strategies, the following cases are investigated:

C1 Traditional PI control without zero-sequence current control.
C2 MPC control without zero-sequence current control.
C3 Traditional PI control with zero-sequence current control.
C4 MPC control with zero-sequence current control.

4.2. Dc fault at MMC1's terminal

In this scenario, the PG and PP faults are applied at the terminal of MMC1. Furthermore, the impact of protection delay (i.e delay in fault detection or dc CB operation) (t_d) is investigated for all cases and summarized in Tables 2 and 3. From these tables, it can be seen that the fault is interrupted by the dc CB with both traditional PI controls and MPC for $t_d = 1$ ms. Compared to PI control, during PG fault with MPC, the peak fault current in CB1P dc CB and MMC1 is lower by 0.7 kA and 1.26 kA, respectively. These lower values result from the MPC's fast control action on the state variables of MMC. However, this results in decreasing of dc link voltage at MMC1 ($v_{dc,MMC1}$) by 16% compared with the rated voltage, which is referred as undershoot in this and subsequent sections. Furthermore, the settling time is increased by 50 ms. However, the fast control action helps the dc CB to absorb less energy. As the t_d increases, the peak amplitude of the fault current increases, and as a result, dc CB in the PI controlled system fails to interrupt. However, the MPC during the PG fault only adds up a surplus of 0.5 ms delay before the dc CB fails to interrupt the fault. A similar

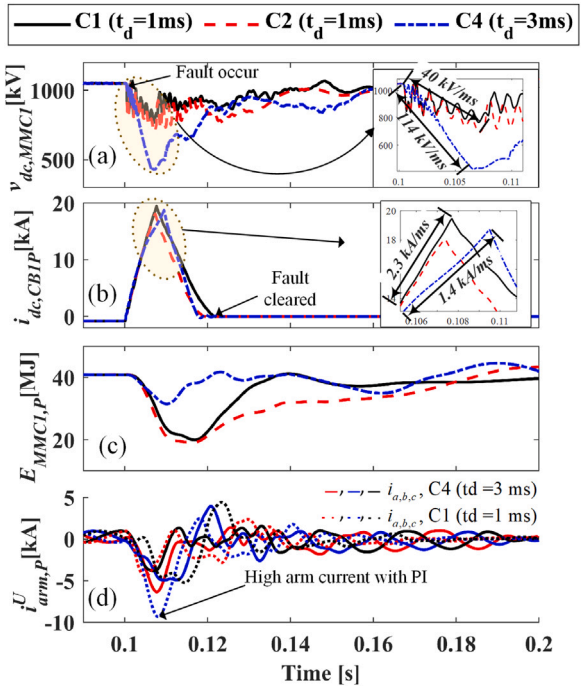

Fig. 5. Impact of proposed control during PP fault at MMC1 terminal: (a) MMC1's terminal voltage [kV]; (b) Line Current [kA] in CB1P dc CB; (c) Total Energy stored in the MMC1 [MJ]; and (d) Upper arm current of MMC1 [kA].

trend is observed with a higher fault current and undershoot in dc link voltage from rated voltage during the PP fault as shown in Table 3.

With the proposed control over i_z^{Σ} current, in PI's and MPC's CCSC, the sensitivity of the t_d is minimized to a greater extent. The system can withstand a higher delay, with a lower fault current in the converter and in the dc CB. This results in lower energy absorption in the dc CB's surge arrester during dc fault. The energy absorbed by the traditional PI-controlled MMC is 30% (PG) and 40% (PP) higher than that of the MPC-controlled MMC with the proposed control over i_z^{Σ} current for $t_d = 3$ ms during the PG and the PP fault, respectively. Furthermore, the settling time is shortened due to the active power feedback in the proposed control. However, a significant undershoot in $v_{dc,MMC1}$ from rated dc link voltage is observed with the proposed control. It is also interesting to observe that the energy absorbed during the PG and PP fault interruption remains the same, indicating reduced stress on the surge arrester during the PP fault. As a result, an increase in t_d does not influence increase of the absorbed energy drastically.

Fig. 5 highlights the significance of the proposed control compared to the PI and MPC in the time domain for PP fault. During the fault period, the MMC with the proposed control has $\frac{dv}{dt}$ of −114 kV/ms, while PI and MPC controlled MMC1 has $\frac{dv_{dc,MMC1}}{dt}$ of −40 kV/ms. The high value of $\frac{dv_{dc,MMC1}}{dt}$ creates a reduction in $\frac{di_{dc,CB1P}}{dt}$ of fault current as seen Fig. 5(b). Furthermore, the proposed control prevents a large drop in converters' energy. Hence, it protects the sub-modules during fast transients. The arm currents of the converts are smaller compared to traditional PI-controlled MMC, as seen in Fig. 5(d).

4.3. Dc fault at MMC2's terminal

In this case, a PG and a PP fault are applied at the MMC2 terminal. The effect of protection delay is investigated for all cases and is summarized in Table 4 and 5, respectively. The dc fault near MMC2 creates a high rate of rise of fault current, which results in current interruption failure. The high value of $\frac{dv_{dc,MMC2}}{dt}$ is caused by the wind park's power infeed. Hence, MMC2 is very sensitive to the delay of the

Table 2
Performance of different cases under the pole-to-ground fault at the MMC1 terminal.

Pole-to-ground fault		Peak in $i_{dc,CB1P}$	Peak in $i_{dc,MMC1}$	Undershoot in $V_{dc,MMC1}$	Settling time of $V_{dc,MMC1}$	Energy SA	Status
PI without i_z^{Σ} control	t_d = 1 ms	17.70 kA	15.30 kA	916.31 kV (−12.73 %)	0.13 s	69.25 MJ	Interrupts
	t_d = 1.5 ms	37.01 kA	24.36 kA	533.87 kV (−49.15 %)	Inf	0.00 MJ	Fails
	t_d = 2 ms	36.93 kA	24.46 kA	534.68 kV (−49.07%)	Inf	0.00 MJ	Fails
	t_d = 2.5 ms	36.84 kA	24.51 kA	532.94 kV (−49.24 %)	Inf	0.00 MJ	Fails
	t_d = 3 ms	36.78 kA	24.57 kA	533.79 kV (−49.16 %)	Inf	0.00 MJ	Fails
MPC without i_z^{Σ} control	t_d = 1 ms	17.00 kA	14.04 kA	881.92 kV (−16.00 %)	0.18 s	55.38 MJ	Interrupts
	t_d = 1.5 ms	18.77 kA	15.18 kA	867.75 kV (−17.35 %)	0.19 s	62.27 MJ	Interrupts
	t_d = 2 ms	32.63 kA	22.14 kA	538.90 kV (−48.67 %)	Inf	0.00 MJ	Fails
	t_d = 2.5 ms	32.55 kA	22.18 kA	539.94 kV (−48.57 %)	Inf	0.00 MJ	Fails
	t_d = 3 ms	32.47 kA	22.14 kA	540.47 kV (−48.52 %)	Inf	0.00 MJ	Fails
PI with i_z^{Σ} control	t_d = 1 ms	15.59 kA	11.52 kA	789.86 (−24.78%)	0.18 s	42.5 MJ	Interrupts
	t_d = 1.5 ms	16.53 kA	12.49 kA	790.77 (−24.69%)	0.18 s	47.96 MJ	Interrupts
	t_d = 2 ms	17.57 kA	13.36 kA	789.43 (−24.82%)	0.29 s	53.51 MJ	Interrupts
	t_d = 2.5 ms	18.8 kA	13.88 kA	790.13 (−24.75%)	0.29 s	59.83 MJ	Interrupts
	t_d = 3 ms	47.1 kA	29.51 kA	517.49 (−50.72%)	Inf	0 MJ	Fails
MPC with i_z^{Σ} control	t_d = 1 ms	15.03 kA	9.5 kA	739.02 (−29.62%)	0.16 s	32.33 MJ	Interrupts
	t_d = 1.5 ms	15.76 kA	10.71 kA	739.51 (−29.57%)	0.17 s	36.55 MJ	Interrupts
	t_d = 2 ms	16.5 kA	11.5 kA	738.56 (−29.66%)	0.17 s	40.4 MJ	Interrupts
	t_d = 2.5 ms	17.34 kA	11.95 kA	736.82 (−29.83%)	0.16 s	44.05 MJ	Interrupts
	t_d = 3 ms	18.53 kA	12.53 kA	735.28 (−29.97%)	0.16 s	48.78 MJ	Interrupts

Table 3
Performance of different cases under the pole-to-pole fault at the MMC1 terminal.

Pole-to-pole fault		Peak in $i_{dc,CB1P}$	Peak in $i_{dc,MMC1}$	Undershoot in $V_{dc,MMC1}$	Settling time of $V_{dc,MMC1}$	Energy SA	Status
PI without i_z^{Σ} control	t_d = 1 ms	19.46 kA	16.4 kA	767.07 kV (−26.95 %)	0.19 s	84.32 MJ	Interrupts
	t_d = 1.5 ms	43.24 kA	24.94 kA	−14.22 kV (−101.35 %)	Inf	0 MJ	Fails
	t_d = 2 ms	43.16 kA	25.13 kA	−13.62 kV (−101.3 %)	Inf	0 MJ	Fails
	t_d = 2.5 ms	43.08 kA	25.18 kA	−13.88 kV (−101.32 %)	Inf	0 MJ	Fails
	t_d = 3 ms	43 kA	25.25 kA	−13.98 kV (−101.33 %)	Inf	0 MJ	Fails
MPC without i_z^{Σ} control	t_d = 1 ms	18.06 kA	14.7 kA	691.54 kV (−34.14 %)	0.19 s	63.95 MJ	Interrupts
	t_d = 1.5 ms	37.88 kA	22.69 kA	−10.72 kV (−101.02 %)	Inf	0 MJ	Fails
	t_d = 2 ms	37.67 kA	22.76 kA	−15.06 kV (−101.43 %)	Inf	0 MJ	Fails
	t_d = 2.5 ms	37.57 kA	22.79 kA	−14.02 kV (−101.34 %)	Inf	0 MJ	Fails
	t_d = 3 ms	37.44 kA	22.87 kA	−13.36 kV (−101.27 %)	Inf	0 MJ	Fails
PI with i_z^{Σ} control	t_d = 1 ms	15.71 kA	11.34 kA	535.32 kV (−49.02%)	0.25 s	44.57 MJ	Interrupts
	t_d = 1.5 ms	16.63 kA	12.4 kA	530.33 kV (−49.49%)	0.26 s	50.27 MJ	Interrupts
	t_d = 2 ms	17.71 kA	13.12 kA	520 kV (−50.48%)	0.27 s	56.11 MJ	Interrupts
	t_d = 2.5 ms	19.13 kA	13.61 kA	535.75 kV (−48.98%)	0.26 s	64.22 MJ	Interrupts
	t_d = 3 ms	49.91 kA	28.1 kA	−16.5 kV (−101.57%)	Inf	0 MJ	Fails
MPC with i_z^{Σ} control	t_d = 1 ms	15.15 kA	9.27 kA	417.64 kV (−60.22%)	0.18 s	33.31 MJ	Interrupts
	t_d = 1.5 ms	15.87 kA	10.49 kA	418.39 kV (−60.15%)	0.18 s	37.55 MJ	Interrupts
	t_d = 2 ms	16.65 kA	11.36 kA	418.08 kV (−60.18%)	0.18 s	41.61 MJ	Interrupts
	t_d = 2.5 ms	17.52 kA	11.87 kA	422.06 kV (−59.8%)	0.18 s	45.39 MJ	Interrupts
	t_d = 3 ms	18.71 kA	12.21 kA	421.38 kV (−59.87%)	0.17 s	50.34 MJ	Interrupts

operation of dc CB, and the dc CB line inductance. However, with the application of the proposed zero-sequence current PI and MPC control, the delay sensitivity is removed for both types of faults as illustrated in Tables 4 and 5 for PP and PG faults. The energy absorption and the peak fault current through CB2P and MMC2 for both controls differ by less than 1%. The constant current source behaviour of the grid-forming converters causes this. Moreover, on average, the settling time is improved by 100 ms in the MPC-controlled system. Furthermore, the undershoot in dc link voltage at MMC2 $v_{dc,MMC2}$ from rated dc link voltage during the PP fault is higher compared to the undershoot during the PG fault.

5. Conclusion

In this paper, a new MPC zero-sequence current control for the MMC converter is proposed, which influences the dc link voltage control. The proposed control method controls the additive zero sequence current component, and it can provide an extra window of 3 ms for fault detection or dc CB operation. This control is especially beneficial for a converter that directly influences the dc grid. The proposed control ensures the same energy absorption in the surge arrester during terminal PP and PG faults at the converter, which regulates the dc voltage of MTdc. The proposed controller can also be added to the existing PI-controlled converter. However, the slower nature of the existing PI control strategies cause a larger settling time of the dc link voltage.

There is a trade-off between the dc link voltage and the fault current. Based on the priority, suitable control constraints need to be set up. However, the implementation of this control reduces the time dependence on the protection algorithm, breaker operation, and fault current limiters by increasing the reaction time window. Hence, it provides more time for the proper reaction of the dc CB during the dc

Table 4
Performance of different cases under the pole-to-ground fault at the MMC2 terminal.

Pole-to-ground fault		Peak in $i_{dc,CB1P}$	Peak in $i_{dc,MMC2}$	Undershoot in $V_{dc,MMC2}$	Settling time of $V_{dc,MMC2}$	Energy SA	Status
PI without i_z^{Σ} control	t_d = 1 ms	36.33 kA	14.77 kA	572.04 kV (−45.52%)	Inf	0 MJ	Fails
	t_d = 1.5 ms	36.41 kA	14.46 kA	568.81 kV (−45.83%)	Inf	0 MJ	Fails
	t_d = 2 ms	36.36 kA	14.49 kA	570.08 kV (−45.71%)	Inf	0 MJ	Fails
	t_d = 2.5 ms	36.37 kA	14.43 kA	568.81 kV (−45.83%)	Inf	0 MJ	Fails
	t_d = 3 ms	36.4 kA	14.43 kA	569.14 kV (−45.8%)	Inf	0 MJ	Fails
MPC without i_z^{Σ} control	t_d = 1 ms	30.12 kA	15.97 kA	606.88 kV (−42.2%)	Inf	0 MJ	Fails
	t_d = 1.5 ms	29.99 kA	15.74 kA	605.47 kV (−42.34%)	Inf	0 MJ	Fails
	t_d = 2 ms	29.85 kA	15.49 kA	604.13 kV (−42.46%)	Inf	0 MJ	Fails
	t_d = 2.5 ms	29.84 kA	15.1 kA	607.27 kV (−42.16%)	Inf	0 MJ	Fails
	t_d = 3 ms	29.75 kA	14.85 kA	605.14 kV (−42.37%)	Inf	0 MJ	Fails
PI with i_z^{Σ} control	t_d = 1 ms	14.73 kA	5.51 kA	723.09 kV (−31.13%)	0.26 s	32.98 MJ	Interrupts
	t_d = 1.5 ms	15.41 kA	5.56 kA	719.83 kV (−31.44%)	0.27 s	36.07 MJ	Interrupts
	t_d = 2 ms	15.99 kA	5.56 kA	716 kV (−31.81%)	0.27 s	38.39 MJ	Interrupts
	t_d = 2.5 ms	16.62 kA	5.51 kA	715.35 kV (−31.87%)	0.26 s	40.63 MJ	Interrupts
	t_d = 3 ms	17.48 kA	5.56 kA	719.83 kV (−31.44%)	0.25 s	43.04 MJ	Interrupts
MPC with i_z^{Σ} control	t_d = 1 ms	14.51 kA	5.06 kA	701.06 kV (−33.23%)	0.16 s	27.69 MJ	Interrupts
	t_d = 1.5 ms	15 kA	5.06 kA	700.16 kV (−33.32%)	0.17 s	29.15 MJ	Interrupts
	t_d = 2 ms	15.59 kA	5.07 kA	701.49 kV (−33.19%)	0.17 s	30.84 MJ	Interrupts
	t_d = 2.5 ms	16.01 kA	5.05 kA	700.58 kV (−33.28%)	0.17 s	31.85 MJ	Interrupts
	t_d = 3 ms	16.6 kA	5.05 kA	700.8 kV (−33.26%)	0.18 s	33.18 MJ	Interrupts

Table 5
Performance of different cases under the pole-to-pole fault at the MMC2 terminal.

Pole-to-pole fault		Peak in $i_{dc,CB2P}$	Peak in $i_{dc,MMC2}$	Undershoot in $V_{dc,MMC2}$	Settling time of $V_{dc,MMC2}$	Energy SA	Status
PI without i_z^{Σ} control	t_d = 1 ms	39.26 kA	14.71 kA	−20.01 kV (101.91%)	Inf	0 MJ	Fails
	t_d = 1.5 ms	39.14 kA	14.66 kA	−19.1 kV (−101.82%)	Inf	0 MJ	Fails
	t_d = 2 ms	39.09 kA	14.61 kA	−20.47 kV (−101.95%)	Inf	0 MJ	Fails
	t_d = 2.5 ms	39.09 kA	14.64 kA	−20.16 kV (−101.92%)	Inf	0 MJ	Fails
	t_d = 3 ms	39.19 kA	14.67 kA	−19.53 kV (−101.86%)	Inf	0 MJ	Fails
MPC without i_z^{Σ} control	t_d = 1 ms	35.42 kA	16.22 kA	−44.7 kV (−104.26%)	Inf	0 MJ	Fails
	t_d = 1.5 ms	35.31 kA	16.08 kA	−40.77 kV (−103.88%)	Inf	0 MJ	Fails
	t_d = 2 ms	35.15 kA	15.85 kA	−33.77 kV (−103.22%)	Inf	0 MJ	Fails
	t_d = 2.5 ms	35.11 kA	15.46 kA	−29.99 kV (−102.86%)	Inf	0 MJ	Fails
	t_d = 3 ms	34.94 kA	15.25 kA	−19.57 kV (−101.86%)	Inf	0 MJ	Fails
PI with i_z^{Σ} control	t_d = 1 ms	15.25 kA	4.98 kA	324 kV (−69.14%)	0.27 s	39.34 MJ	Interrupts
	t_d = 1.5 ms	16 kA	5 kA	324.31 kV (−69.11%)	0.27 s	42.87 MJ	Interrupts
	t_d = 2 ms	16.75 kA	4.98 kA	323.68 kV (−69.17%)	0.25 s	46.39 MJ	Interrupts
	t_d = 2.5 ms	17.56 kA	5.01 kA	324.28 kV (−69.12%)	0.24 s	49.49 MJ	Interrupts
	t_d = 3 ms	18.63 kA	4.98 kA	324.24 kV (−69.12%)	0.22 s	53.77 MJ	Interrupts
MPC with i_z^{Σ} control	t_d = 1 ms	15.15 kA	4.97 kA	307.95 kV (−70.67%)	0.23 s	32.88 MJ	Interrupts
	t_d = 1.5 ms	15.89 kA	5.04 kA	307.74 kV (−70.69%)	0.18 s	35.64 MJ	Interrupts
	t_d = 2 ms	16.57 kA	5.04 kA	307.95 kV (−70.67%)	0.18 s	38.52 MJ	Interrupts
	t_d = 2.5 ms	17.26 kA	5.04 kA	307.61 kV (−70.7%)	0.18 s	40.45 MJ	Interrupts
	t_d = 3 ms	17.99 kA	5.11 kA	308.5 kV (−70.62%)	0.18 s	42.86 MJ	Interrupts

fault. Furthermore, the energy absorption during the fault is reduced. Therefore, the footprint of the dc CB is reduced, and thus, it provides a low-cost solution.

More work will be done in the near future to investigate the sensitivity of this control on the latency, converter parameters, and topology change. Besides, the constraints on the system and fault conditions will be defined by considering the dc CB protection.

CRediT authorship contribution statement

Ajay Shetgaonkar: Conceptualization, Methodology, Software, Validation, Writing – original draft, Visualization, Formal analysis. **Marjan Popov:** Writing – review & editing, Supervision, Investigation. **Peter Palensky:** Supervision, Writing – review & editing, Project administration. **Aleksandra Lekić:** Resources, Writing – review & editing, Supervision, Funding acquisition, Project administration, Formal analysis.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

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