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A Fast High Sensitivity Power Transfer Device Approach for (sub)mm-wave applications

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***Abstract* — In this paper, we present a low-noise, high-gain readout hardware to be used in conjunction with (sub)mm-wave zero bias detectors, to enable high sensitivity (i.e., ~ -50 dBm) and fast (i.e., below a second at -50 dBm) power detection.**

The developed hardware employs a cascade of two (COTS) programmable gain amplifier (PGA), capable of reaching up to 90 dB gain (volt to volt), each providing an input referred noise level of 16 nV/√Hz. The signal is then digitized on the same board via a 500 kHz 12bit ADC, providing an SNR of 74 dB. The digitized signal is then readout via an ST microcontroller and transferred to the operator PC via a USB interface. The sensitive bias voltages for the PGAs are provided via the microcontroller, or alternatively can be fed by an external lab grade supply to further improve on the (already high) supply noise rejection from the first stage PGA. The proposed hardware is designed to interface with VDI zero bias detectors, high responsivity and low NEP diodes (around 2000 V/W and below 12 pW/√Hz, respectively) operating in monomodal waveguide bands up to 500 GHz. In this contribution we demonstrate the usage of the developed hardware with WR10, WR6.5, WR5 and WR 3 ZBD diodes.

***Index Terms* — mm-wave, power detector, zero bias diode, large-signal.**

I. Introduction

The request for improved measurement capabilities is also growing with the increase of the commercial interest in the frequency spectrum above 100 GHz. It has been shown that VNA-based mm-wave extender test-benches can support a large spectra of non-linear measurements when absolute power is transferred from a power sensor to the VNA receivers [1][2]. In addition, when operating at different back-off levels from their saturated value, it is important to monitor the quality of the "quasi-CW" stimulus coming from the extenders, as discussed in [3]. With the increased maturity of the technologies and design concept operating in these frequencies, i.e., above 20 dB gain and P1dB ~16 [4], the drive level from the mm-wave extender needs to be (often) backed-off from saturated power more than 20 dBc, requiring a careful characterization of the drive spectrum quality.

Within this last step, the speed and the sensitivity of current power detectors operating in the above 100 GHz range provide a foreseeable bottleneck. The VDI PM5 [5], which is the de-facto standard for sub-THz power measurement, provides longer measurement times when being employed in the high sensitivity scale setting (i.e., 12 sec wait time for 90% response and 31 sec for 99% on the lowest scale according to its datasheet) and has a sensitivity limit in the order of ~-38 dBm. We propose in this work a low-noise high-gain readout hardware to be used in conjunction with (sub)mm-wave zero bias detectors [6], see Fig. 1, to enable fast and high sensitivity (i.e., ~ -50dBm) power detection to mitigate this time characterization bottleneck.

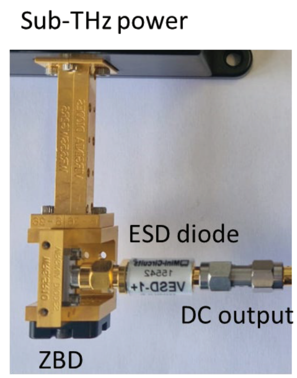


Fig. 1: VDI WR6.5 zero bias detector with ESD protection.

This paper is organized as follows: first, the readout PCB is described and the details of the design choices are provided. Secondly, the system (ZBD plus readout) responsivity, is presented for the WR10, WR6.5, WR5 and WR3 bands, validating the interoperability of the circuitry across different ZBDs. To conclude, the speed response in the lower power ranges is shown and compared with the PM5 response at the same power to validate the claim of high speed characterization of the proposed solution.

II. Readout Board Design

The design requirement for the readout board is to operate between a maximum power of -5dBm (defined by the input compression point of the ZBD) and -50dBm (chosen as the power level where only linear characterization would occur). When assuming a responsivity in the order of 2000 V/W, the above defined range translates into a voltage range from 20μV to 0.635V. A block diagram of the board can be seen in Fig. 2.

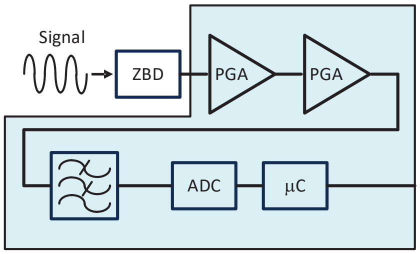


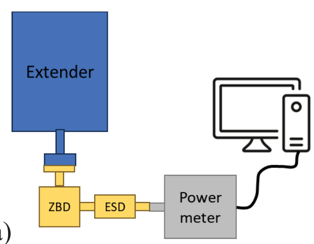
Fig. 2: Readout board block scheme (i.e., highlighted).

The board consists of two PGAs, an RC filter, an ADC and a microcontroller. The LTC2312-12 ADC, with 12 bit resolution, is selected for this design. A 3.3 V supply voltage is applied to it with a reference voltage of 2.048 V, yielding an LSB level of 500µV. In order to reach the (selected) minimum level, the selected PGAs (Ti 117) can provide up to 90 dB of voltage gain, with a very low input noise level of 16 nV/√Hz. Moreover, a low pass RC filter is placed in between the PGAs and the ADC to reject the noise below 1.59 MHz. The signal is then fed to the microcontroller (Nucleo-L412KB) and read out by a PC.

III. Readout Board Characterization

The readout board was then used to characterize the responsivity of two VDI ZBD in the WR10, WR6.5, WR5 and WR 3 bands, in a configuration as shown in Fig. 3.

a)



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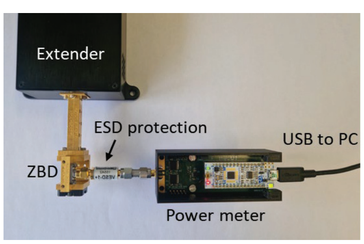
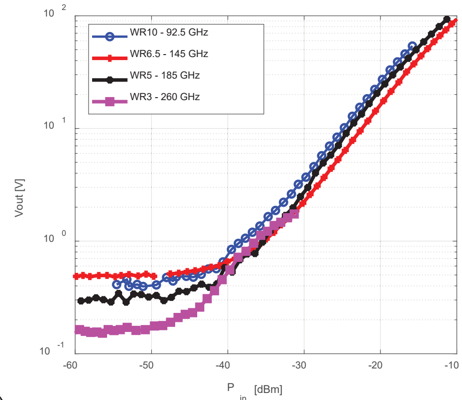
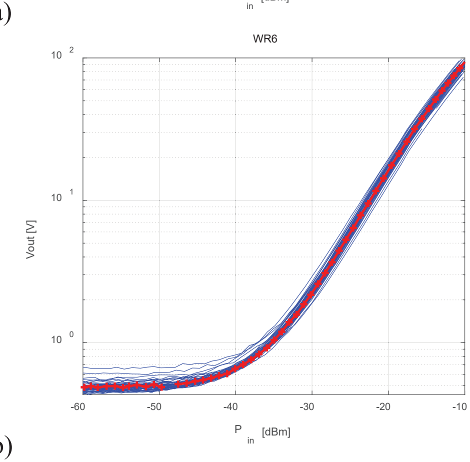


Fig. 3: a) Schematic of the measurement setup, b) photograph of the setup used in WR6.5.

The VNA and the extender are controlled using MMW STUDIO [7], whereas the absolute power calibration is achieved using a VDI Erikson PM5 when the modules are operating at full power, as presented in [8].



a)



b)

Fig. 4: Graph of the readout voltage V_{out} measured by the power transfer device as a function of the inserted mm-wave power P_{in} computed using the system depicted in Fig. 3 for: a) the WR10, WR6.5, WR5 and WR3 bands, where only the mid band response curve is shown and b) WR6.5 where all the traces in the band (step of 1 GHz) and the mid band response are shown.

The readout voltage V_{out} measured by the power transfer device as a function of the inserted mm-wave power P_{in} for the WR10, WR6.5, WR5 and WR3 bands (mid band response) are shown in Fig. 4.a. The characterization curves across frequencies in a given band are shown for the WR6.5 module in Fig. 4.b, where a step of 1 GHz is considered. These curves represent the 2D (frequency and power) look up table to be used by the operator when the power meter is used in measurement mode.

To provide a further validation of the increased speed in the lower power level characterization of the propose approach the following test was carried out:

1) The PM5 was used to measure a power setup of ~3dB around -15dBm and -8 dBm, employing the two most sensitive scales of the instrument (200µW and 2mW, respectively), as shown in Fig. 5. As can be seen, when the higher resolution range is selected (i.e., 200µV) the PM5 increases the internal average, resulting in a lower number of points per second. Moreover, the higher response time in this scale results in an increased

characterization time for the quasi-CW characterization case discussed in Section I.

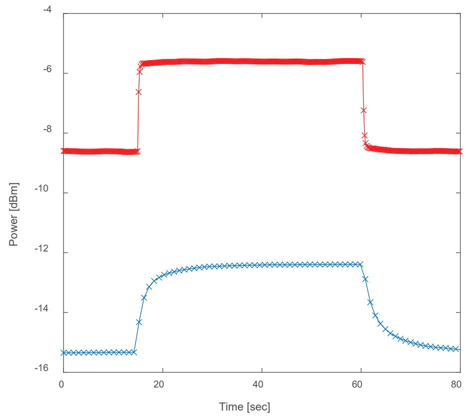
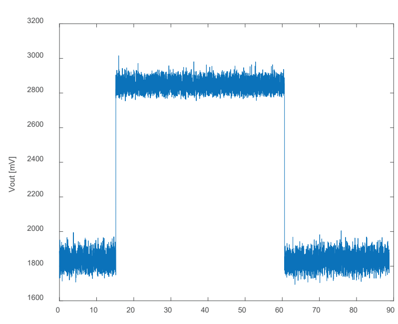
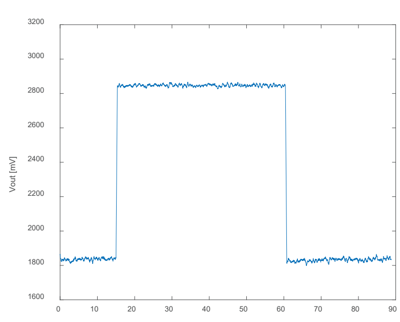


Fig. 5: PM5 measurement of a source (mm-wave extender) power step in the WR6.5 band of ~3dB. Red trace measurement around -5dBm with a 2mV range, blue trace, measurement around -15dBm with a 200µV range.

2) The ZBD diode with the readout board was then used to measure a similar power step of ~3dB around -15dBm, as shown in Fig. 6. The high speed ADC allows a large number of points per second readout (i.e., no applied average and PGA gain set to 25), as shown in Fig. 6.a. When an average of 32 is employed a high resolution readout is obtained without increase in settling time, as shown in Fig. 6.b.



a)



b)

Fig. 6: Response of the ZBD with readout board shown in Fig. 3, when the test configuration of point 2) is carried out, a) no average, b) 32 point average.

IV. Conclusion

A readout board to be used in combination with a (sub)mm-wave zero bias diode was presented to enable high sensitivity (i.e., ~ -50 dBm) and fast (i.e., below a second at -50 dBm) power detection. The readout board architecture has been described and the preliminary results in terms of the board responsivity and the readout speed were presented. The current concept can provide a path to enable accurate high speed characterization of the quasi-CW conditions of mm-wave extenders when operating at back off levels above 20 dBc.

V. Acknowledgment

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