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Packaging Technologies for Single-Side Cooling SiC Power Modules With Low Parasitic Inductance: A Review

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ABSTRACT Due to the better performance of the Wide Band Gap (WBG) devices, there has been a paradigm shift toward WBG-based power modules for diverse applications like Electric Vehicles (EVs). However, the high parasitic inductance value of power modules hinders these devices from unlocking their full potential. Therefore, this paper comprehensively reviews SiC-based Single Side Cooling (SSC) power modules that benefit from low parasitic inductance. The paper also discusses the need to develop newer power modules using modern packaging methods. The surveyed power modules are categorized into three main groups, namely wire bonding, hybrid, and 3D packaging methods. This classification contains several vital parameters of the studied power modules, such as nominal and Double Pulse Tests (DPT) power ratings, parasitic inductance, size, etc. The main features and characteristics corresponding to the reviewed power modules' packaging methods and techniques are also briefly described. Finally, a thorough discussion about challenges and future trends is highlighted before concluding the paper.

INDEX TERMS Hybrid packaging, power modules, parasitic inductance, single side cooling (SSC), SiC semiconductor packaging, wire bonding packaging, wide band gap (WBG) devices, 3D packaging.

I. INTRODUCTION

Nowadays, due to the increasing concerns about environmental issues, the demand for the electrification of transportation, especially Electric Vehicles (EVs), is soaring rapidly. In this regard, the global EV share is expected to reach 22.1% in 2025, then 44.9% in 2030, and further increase to 69.7% in 2035. Global volumes are projected to rise from 14.2 million in 2023 to 71.6 million units in 2035 [1]. The ongoing shift toward renewable energy sources and the transformation to electrification is a key solution to this challenge, particularly in the transportation sector. According to the European Environmental Agency (EEA) report [2], transport accounted for about one-third (29%) of the EU's greenhouse gas emissions in 2022, and this quota is expected to grow. However, it is estimated that greenhouse gas emissions from the transportation sector will decrease by about 14% and 37% in 2030 and 2050, respectively, compared to 2022. Despite these reductions, much stronger efforts will be required to achieve the EU's goal of a 90% reduction in emissions from this sector by 2050 [2]. Given these expectations, advancements across various domains have become a growing concern for EVs and the utility grid [3], [4], [5], [6], [7], [8], [9], [10].

One of the most effective ways to reach these goals in EVs is by improving the overall performance of the power inverter. To achieve this, improving the performance of the power modules, which are the heart of the power inverters, is essential. This improvement can be made from various perspectives, including efficiency, reliability, manufacturing cost, complexity, and better operation under harsh conditions specific to EVs. Fortunately, these aspects can be significantly improved by replacing Si semiconductors in power modules with their WBG counterparts. Since their initial emergence in the 1990s [11], WBG and Ultra Wide Band Gap (UWBG)

TABLE 1. Silicon, WBG and UWBG Characteristics Comparison [12], [13]

Parameter (Unit)	Si	SiC	GaN	Diamond	AlN
Bandgap (eV)	1.12	3.26	3.44	5.45	6.2
Critical electric field (MV/cm)	0.3	2	3.8	10	12
Breakdown voltage (kV)	0.6	10	1.2	10	10
Dielectric constant(-)	11.8	10	9.5	5.5	8.5
Electron mobility ($cm^2/V-s$)	1500	950	2000	3800	300
CTE ($\times 10^{-6}$/K)	2.6	5	5.6	0.8	5.2
Thermal conductivity (W/m-K)	150	490	130	2200	285
Melting Point (°C)	1415	2830	2573	4373	2200

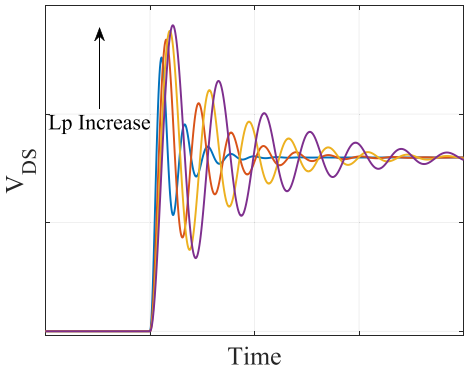


FIGURE 1. The effect of parasitic inductance on the drain-source voltage (V_{DS}) during turn-off time interval (L_p(*Purple*) > L_p(*Orange*) > L_p(*Red*) > L_p(*Blue*)).

semiconductors have shown significant potential to be a replacement for Si in power modules as they exhibit superior properties in terms of electrical performance and thermal behavior. For comparison, some of these factors are reported in Table 1. When these features are translated into device specifications, WBG semiconductors can achieve superior performance metrics compared to silicon (Si) devices. Specifically, WBG devices offer increased breakdown voltage and current capacity, and enhanced operating temperatures. Furthermore, they can deliver faster switching speeds alongside reduced switching losses, all of which contribute to their advantageous performance over conventional Si counterparts.

Among these characteristics, the higher breakdown voltage and switching power losses can be directly related to the parasitic inductance of the package. The relations between the parasitic inductance, breakdown voltage, and switching power losses are discussed in detail. As mentioned, like other WBG devices, SiC semiconductors can have faster switching speed as compared to their Si peers. Generally, this feature results in lower power losses. To analyze this, the following equation calculates the power loss during the switching process [14]:

$$P_{Loss(switching)} = \frac{1}{2} \times f_{sw} \times v_{DS} \times i_{DS} \times (t_r + t_f) \qquad (1)$$

where f_{sw}, v_{DS}, i_{DS}, t_r, and t_f are the switching frequency, voltage, and current values of the switch at the switching moment, rise time, and fall time, respectively.

Clearly, the faster switching speed of SiC renders lower t_r and t_f. Thus, from the above equation, the switching power loss is less for higher speed switching. Nevertheless, this advantage can be compromised if the parasitic inductance is large. This is due to the fact that the fast switching, combined with the large value of parasitic inductance, results in high voltage overshoots. Specifically, the stored energy in the parasitic inductance, L_p, imposes an overshoot on the power switch, given by $L_P \times di/dt$, during its turn-off period. This overshoot can exceed the semiconductor's maximum blocking voltage, potentially leading to device failure. The first way to avoid this failure is to consider a high margin between the nominal voltage of the switch and the applied voltage to the module. As a consequence, a large overdesign should be considered to handle the voltage overshoot, leading to additional costs. Another way is to reduce the switching speed by increasing the gate resistance. This solution, based on (1), increases the switching power loss, jeopardizing the fast switching feature of the SiC semiconductor. The third solution is implementing power modules with lower parasitic inductance. Consequently, the applied voltage to the power module can be increased to more values closer to the nominal value, e.g., optimal design, without losing the fast switching speed capability. The last solution paves the way for exploiting the most out of the SiC semiconductor while no features are compromised.

The visual sketch of the overshoot and oscillations during the turn-off interval is drawn in Fig. 1. Briefly, as the parasitic inductance increases, (a) the oscillation frequency increases, (b) the voltage overshoot rises, and (c) the rise time extends.

Switching oscillations also adversely affect power converters, leading to electromagnetic interference (EMI), increased power loss, voltage and current overshoots, shoot-through, cross-talk, and potential device damage [15], [16], [17], [18], [19]. The EMI can degrade the reliability and stability of adjacent devices, control circuits, and load [17], [20], [21]. EMI mitigation requires filters, which increase the volume and cost of the converter [22].

With respect to these challenges, innovative power module packaging solutions are essential to enhance performance and ensure compatibility with WBG technologies, especially for those applications that demand higher voltage and power density, like EVs. Consequently, researchers have paid great attention to innovative packaging solutions to implement power modules that benefit from the full advancements of WBG devices [23].

To analyze the effect of the layout on the self-inductance and mutual inductance in detail, these values are calculated and studied for two adjacent conductors. As depicted in Fig. 2, the self-inductance value for two adjacent conductors, with the length L, width W, and thickness t, can be written as follows.

$$L_{\text{self}} = \frac{\mu_0 L}{2\pi}\left[\frac{2L}{W+t} + 0.5 + 0.2235\frac{W+t}{2L}\right] \qquad (2)$$

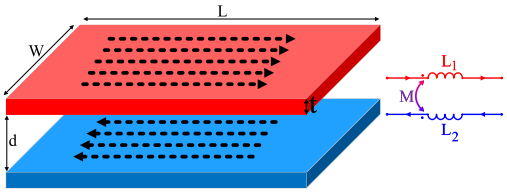


FIGURE 2. Two adjacent conductors and their inductance.

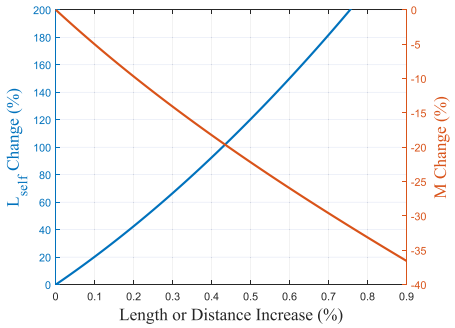


FIGURE 3. Self and mutual inductance change rate as a function of length (for self inductance) or distance (for mutual inductance) ($L = 10mm, d = 1mm, W = 2mm$).

where μ_0 is the permeability of the vacuum.

Based on the sensitivity analysis, the impact of length (L) on the self-inductance is higher than the width (W). The thickness also has the lowest effect. Fig. 3 demonstrates how L_{self} rate changes with increased length. Specifically, a 50% rise in length results in L_{self} increasing by 180%, making it 2.82 times the original value.

In addition, the mutual inductance between these two adjacent conductors can be derived as follows.

$$M = \frac{\mu_0 L}{2\pi} \ln \left[\frac{L}{d} + \sqrt{1 + \left(\frac{L}{d}\right)^2} - \sqrt{1 + \left(\frac{d}{L}\right)^2} - \frac{d}{L} \right] \quad (3)$$

where d is the distance between the two conductors. Fig. 3 also plots the change rate of M as a function of the distance change. For example, a 50% increase in the distance between two conductors results in a 22% decrease in the mutual inductance value. To better show the relation between the self, mutual, and equivalent inductances of two adjacent conductors, a 3D plot of these values versus L and d is sketched in Fig. 4.

These three sketches primarily indicate that increasing length elevates the total parasitic inductance. Therefore, maintaining a short Current Commutation Loop (CCL) is essential. Secondly, the mutual inductance is significantly affected by distance. It is reduced as the distance increases. This is physically expected due to the fact that a short distance magnifies the mutual inductance flux. Emphasizing the importance of the close allocation of current paths with opposite currents. On one hand, this increases the risk of insulation failure and blocks the heat dissipation path. On the other hand, long distances can decrease the mutual inductance effect, leading to more parasitic inductance. Therefore, it is vital to have an optimized distance between elements in the power module.

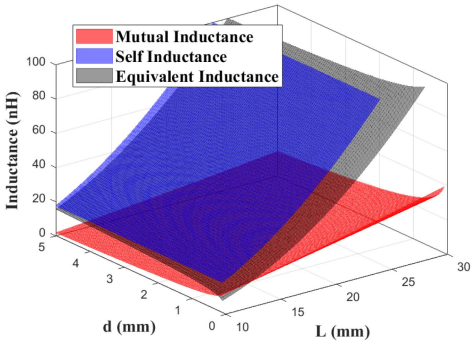


FIGURE 4. 3D plot of the self, mutual, and equivalent inductances.

The above calculations confirm the substantial effect of the layout and structure of a power module on its self-inductance and mutual inductance. Hence, the effort to propose new geometries has garnered significant attention. Importantly, due to the broad scope of power modules using wide bandgap semiconductors, this paper concentrates specifically on packaging methods and techniques for SSC modules incorporating SiC semiconductors.

There are numerous review papers about different aspects of power modules, namely the insulation challenges of high voltage and high power density WBG and UWBG power modules packages [24], SiC-based power modules' packaging technologies, and challenges [25] togehter with their layout, material system and integration [26], medium voltage SiC-based technology impact on high power applications [27], application, challenges, and future development of SiC technology in electrified vehicles [28], pressure contact packaging for WBG power modules and associated opportunities and challenges [29], hybrid packaging methods for SiC-based power module [30], WBG-based power modules' topside interconnections [31], and challenges for medium and high voltage SiC-based power modules [32].

Even though these reviews have explored diverse imperative aspects of WBG-based power modules, no study has focused on those novel layouts and techniques that are utilized to implement SSC SiC-based power modules with low parasitic inductance. First, the power modules with SSC are cheaper and simpler to implement. Second, the lower parasitic inductance paves the way for operation close to the nominal voltage with less concern about the overshoot. Therefore, this paper conducts an in-depth review covering various packaging methods and approaches for packaging SiC-based power modules with SSC. The main classifications for this survey are wire bonding, hybrid, and 3D packaging methods.

Obviously, DSC power modules can offer superior performance in heat dissipation due to their capability of extracting heat from both sides of the chips. This feature results in lower junction temperature and higher power density. However, in scenarios prioritizing simplicity and cost over maximum thermal performance, the SSC power module is a suitable choice in various applications considered by academia and industry [33], [34], [35]. Specifically:

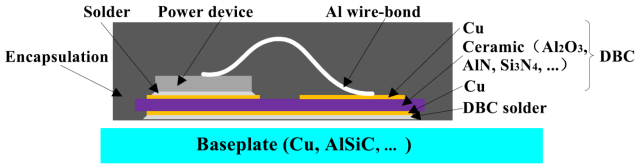


FIGURE 5. Conventional packaging structure with wire bonding [36].

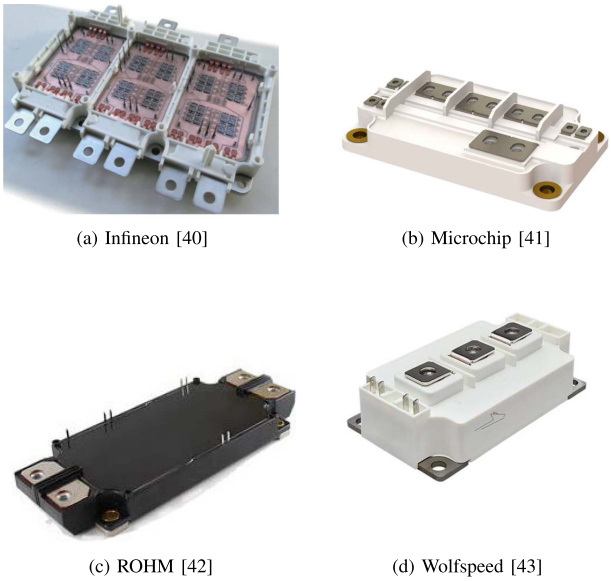
- *Cost and Manufacturability:* SSC modules are often built with fewer layers and involve a straightforward assembly process and methods, such as single-sided attachment to either a baseplate or a heatsink. This streamlines production costs and supports higher-volume manufacturing. On the other hand, DSC power modules manufacturing necessitates precise alignment of two cooling surfaces and the use of supplementary materials like heat spreaders on the top side.
- *Mechanical Stability:* Considering the cooling mechanism on one side, SSC systems may present reduced risks of delamination or mismatches in thermal expansion (CTE mismatch) in challenging environments, thereby improving long-term reliability for utilization in areas such as EVs, industrial drives, aerospace, etc.
- *System Integration and Compatibility:* SSC power modules align well with standard packaging standards and existing system designs, facilitating easier retrofitting or upgrades without necessitating redesigns for dual cooling paths.

The rest of the paper is organized as follows. Sections II and III present an extensive study of wire bonding based and hybrid packaging methods, outlining their main parameters and feature explanations. Then, Section IV analyses 3D packaging-based power modules similar to the former sections. In Section V, the future trends are pointed out after denoting the challenges related to each packaging method. Moreover, the power modules' parasitic inductance, voltage, and current ratings are broadly compared. Finally, Section VI concludes the paper.

II. WIRE BONDING BASED PACKAGING

Wire-bonded structures have been the most popular choice for power module packaging for many years. A typical overview of a conventional power module employing the wire bonding packaging is shown in Fig. 5. In this method, Si or WBG-based bare dies are attached to a substrate with a ceramic insulating layer, namely Al_2O_3 and Si_3N_4. Then, the wire bonding technique is employed to realize the required power and control connections. Moreover, lead frames make $DC+$, $DC-$, and AC connections. Finally, a proper material encapsulates the device for better mechanical stability and insulation purposes [31], [37].

Due to its long use and popularity, wire bonding is a mature, cheap, and versatile packaging technology for constructing power modules. Therefore, the industry has used it regularly to implement its products. These power modules usually suffer from large parasitic inductance, e.g, $>$ 20 nH [38], [39]. However, there are power modules from industry that can reduce the parasitic inductance to lower values [40], [41], [42], [43]. Fig. 6 shows some industrial power modules. These power modules can offer relatively low parasitic inductance. Moreover, they benefit from the 62 mm form factor, simplifying their replacement with their older Si-based peers.



(a) Infineon [40] (b) Microchip [41]

(c) ROHM [42] (d) Wolfspeed [43]

FIGURE 6. Industrial power modules with wire bonding interconnection.

Like the industry, there are many efforts in academia to implement power modules with low parasitic inductance while using wire bonding interconnection. For example, in [44], the concept of realizing interleaved current loops in the internal structure of the power modules is used to attain low parasitic inductance. Even though the parasitic inductance is low compared to the conventional power modules with wire bonding, the power module significantly suffers from unbalanced current sharing among its parallel chips. An interleaved current loop structure is also utilized in [45] and its insight is shown in Fig. 7(a). Based on this figure, the anti-parallel phase leg units cancel out the mutual inductance effect, rendering low total parasitic inductance. It is noteworthy that the parasitic inductance reduction depends on how many phase-leg units are used. In other words, there is no solution to suppress parasitic inductance inside these phase legs. Apart from the unavailable current sharing analysis of the reported power module, considering the high number of chips in each switching position, e.g, 24, the current rating of the power module is relatively low. To achieve simultaneous low parasitic inductance and balanced current sharing, a multi-chip double-end sourced wire-bonded power module is investigated in [46]. The results show that adopting a parallel current path inside the power module and interleaved terminals can reduce parasitic inductance drastically, about 50%, as compared to the conventional design. This new layout offers symmetric power loops for

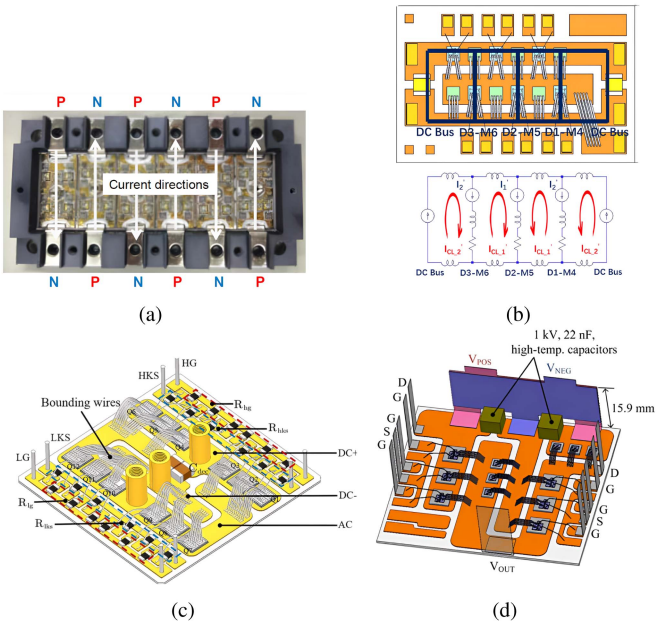


FIGURE 7. (a) Power module with interleaved anti-parallel current loops [45] (b) Double-end sourced power module [46] (c) Optimized wire bonding and paralleled current loops [47], (d) Power module with laminated bus bars and parallel current loops [52].

every parallel-connected MOSFET, contributing to uniform switching performance and ensuring balanced dynamic current sharing between them. For better understanding, Fig. 7(b) clarifies the mutual inductance cancellation circuit and module structure. Parallel current loops alongside wire bonding and terminals optimization are employed in [47] to propose a high-current power module. This power module not only benefits from low parasitic inductance, but also the current sharing profile among the parallel chips has been enhanced. Fig. 7(c) depicts the isometric view of the power module. It should be mentioned that the balanced current sharing profile is the consequence of making symmetrical current paths in the power module. However, to form these symmetrical paths, wire bonds must be implemented with different heights and positions. Besides, the driving loops use ferrite beads to optimize the current sharing performance. It is crystal clear that these adjustments lead to a complex fabrication process of the power module.

The mentioned concept with paralleled $DC+$ and $DC-$ vertical bus bars is employed in [48], [49], [50] for obtaining low parasitic inductance. Nevertheless, the terminal configuration elevates the likelihood of busbar detachment, raising concerns about system reliability. Moreover, the thermal analysis in [48], [49] uncovers a high-temperature difference between paralleled chips. This temperature difference leads to the different threshold voltages for chips, which cause unbalanced current sharing among them. This issue degrades the long-term reliability of the power module. Although high current capacity is realized in [50], there is no information about the current sharing among the paralleled SiC bare dies. Also in industry, Wolfspeed and Microchip utilized parallel vertical bus bars in their structures [41], [43] to lower total parasitic inductance.

Trench MOSFETs and P-cell/N-cell concept are used in [51] to build a multi-chip power module with low power losses. The embedded decoupling capacitors and P-cell/N-cell design concepts are realized to minimize the CCL and limit the total power loop inductance to 6 nH. Yet, the power module suffers from unbalanced current sharing. The P-cell/N-cell internal structure, along with laminated bus bars and paralleled current loops, is used to decrease the parasitic inductance of the power module in [52]. In addition, this power module is able to handle junction temperatures up to 200 °C in its steady state operation. Despite using three chips in parallel, the current rating of this power module is limited, making it inappropriate for high-power applications. Fig. 7(d) illustrates the 3D model of the suggested power module. As this figure clarifies, the parallel current loops are made with the help of the two $DC+$ ports and the $DC-$ port between them.

Also, in [53], a small parasitic inductance is achieved by substrate pattern optimization. Similar to the previous studies, the power module experiences uneven current distribution due to temperature differences among its paralleled chips. Another imperative drawback is the incorporation of an insulating gasket between the $DC+$ and $DC-$ terminals, which increases the production process's expense and intricacy.

To tackle the current sharing challenge effectively, the presented power module in [54] achieves current balance improvement and low parasitic inductance by a symmetrical layout. First, the symmetric structure for the terminals is implemented, and then, to enhance mutual inductance cancellation, a staggered formation for the terminals is employed. The final scheme of the power module, which shows the staggered pattern and the CCL, is sketched in Fig. 8(a). To even further decrease the parasitic inductance, the power module in [55] uses parallel loops with reverse current direction. This power module offers lower parasitic inductance compared to [54] without compromising the balanced current performance. The internal view and the current paths are shown in Fig. 8(b).

Another attempt is made to improve the current sharing problem in [56]. In this power module, 3D current loops are achieved without adding components to the primary substrate. Hence, the authors called their structure a 2.5D packaging method. In addition to benefiting from a balanced current sharing, the total parasitic inductance of the power module is 2.31 nH. This power module's cross-section view and structure with the associated CCL are shown in Fig. 9. Based on this figure, the power module effectively achieves mutual inductance cancellation. Nonetheless, the bent shape of $DC+$ and $DC-$ terminals and incorporating a polyimide (PI) insulation film between them increases the complexity and cost of production.

There are also efforts in industry to achieve both low parasitic inductance and balanced current sharing between parallel switches. DENSO in [57] has made a perpendicular

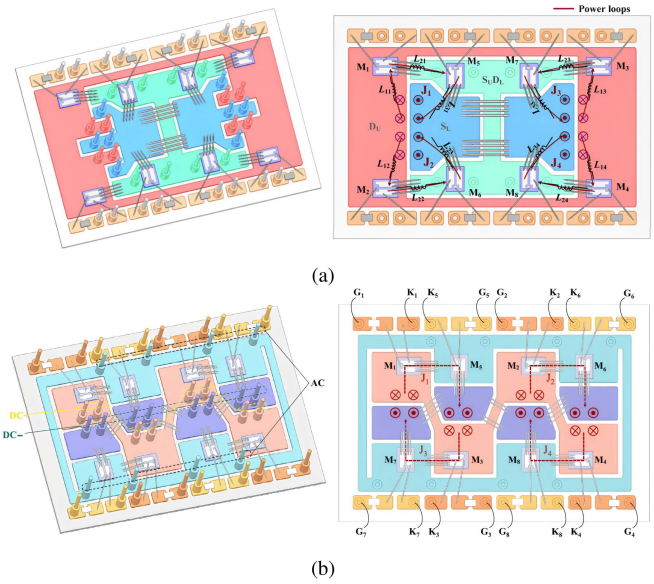


FIGURE 8. (a) Staggered terminal power module and its current loop [54] (b) Power module with parallel reverse current loops [55].

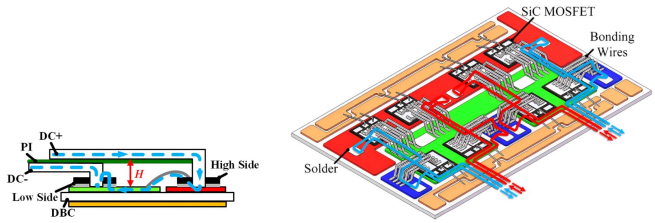


FIGURE 9. Power module with 2.5D wire bonding packaging [56].

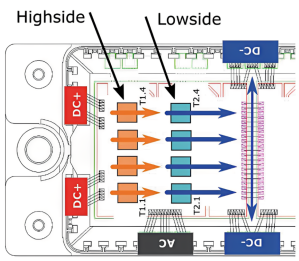
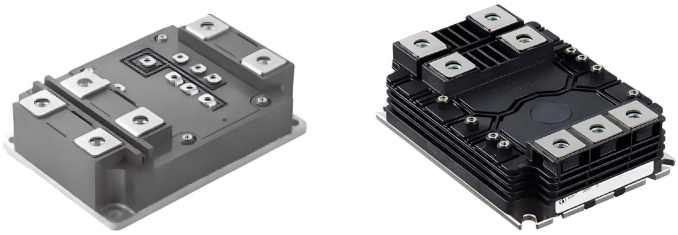


FIGURE 10. Power module from DENSO [57].

connection between the $DC+$ and $DC-$ terminals and the main current path to make the parasitic distribution more equal inside the power module. The structure of this power module is shown in Fig. 10. While the scheme achieves balance in self-inductance within the power module, it falls short in current sharing performance. This issue is because the uneven distribution of the mutual inductance makes the effective parasitic inductances different. Needless to say, the effective value is derived by the summation of the self and mutual inductances. The current sharing performance has been enhanced in the HybridPACK Drive SiC power module developed by Infineon [40]. The designers tried to reduce the source



(a) Power module from Fuji [61]

(b) Power module from Infineon [62]

FIGURE 11. Medium voltage power modules from industry.

to $DC-$ parasitic elements' values. This approach helps to decrease the difference between the applied gate-source voltage to the paralleled chips. Moreover, due to the use of double parallel loops, the power module offers 8 nH parasitic inductance.

Industry initiatives have also expanded to incorporate medium-voltage power modules for various applications such as rail traction, heavy-duty industrial E-mobility, ultra-fast DC chargers, etc. Hence, Mitsubishi [58], TOSHIBA [59], and Wolfspeed [60] have developed power modules with 3.3 kV and 770 A $\sim$ 800 A nominal power rating to address the needs for high-power applications. While maintaining nearly the same power ratings, Fuji has developed a power module with a parasitic inductance equal to 10 nH [61]. This value for parasitic inductance is lower in comparison to the previously mentioned power modules. Moreover, this power module employs trench gate MOSFETs to reduce the $R_{DS(on)}$ and therefore the total power losses. On the other hand, the built power module by Infineon is able to offer the same parasitic inductance while increasing the current rating by 25% [62]. Fig. 11 shows the power modules from Fuji and Infineon.

Furthermore, to meet the needs for high-voltage applications such as solid state transformers, high-voltage circuit breakers, and power conversion for naval ships [63], [64], [65], Wolfspeed has developed extra-high-voltage (XHV) power modules with a 10 kV voltage rating, namely XHV-6 and XHV-9. The XHV-6 power module has a three-phase configuration and six parallel dies in each switching cell [66]. Since three separate submodules are used in this power module, any failed submodules can be easily replaced with a new one, resulting in high modularity and continuous service. However, thermal analysis indicates a junction temperature difference among the paralleled dies, resulting in asymmetrical current sharing and reduced long-term reliability of the power module. Besides, the XHV-9 power module features a half-bridge layout and can be utilized in various applications, such as high-voltage power conversion [67], [68]. Nevertheless, the used XHV-9 power module in [69] presents a high parasitic inductance value, e.g., $>$ 20 nH. Obviously, at higher voltage levels, the adverse effect of the large parasitic inductance value is more drastic. This issue limits the switching speeds or induces large voltage overshoots on

TABLE 2. Wire Bonding Modules With SiC Semiconductor Comparison

Ref	PR-Chip, (DPT)	Structure	IGD	PI (nH)	TR ($^\circ K/W$)	NoPS	Size (mm^3)	PD (kW/L)	EDC
[40] ※	1200V/400A, (N/A/N/A)	3 Phase Inverter	No	8	0.11 (j-f)	8	$90.75 \times 128 \times 12.8$	N/A	No
[41] ※	1200V/754A, (N/A/N/A)	Half Bridge	No	3	0.04 (j-c)	N/A	$108 \times 62 \times 22$	N/A	No
[42] ※	1200V/567A, (N/A/N/A)	Half Bridge	No	14.1	0.08 (j-c)	N/A	$152 \times 62 \times 21$	N/A	No
[43] ※	1200V/175A, (N/A/N/A)	Half Bridge	No	11.1	0.19 (j-c)	N/A	$105 \times 62 \times 31$	N/A	No
[44]	N/A/N/A, (600V/120A)	Half Bridge	No	9	N/A	6	N/A	N/A	No
[45]	1200V/360A, (600V/120A)	Half Bridge	No	3.8	N/A	24	N/A	N/A	No
[46]	1200V/108A, (300V/60A)	Half Bridge	No	7.97	N/A	3	N/A	N/A	Yes
[47]	1700V/1260A, (550V/1015A)	Half Bridge	No	5.27	N/A	18	N/A	N/A	Yes
[49]	1200V/588A, (600V/120A)	Half Bridge	No	4.8	N/A	6	N/A	N/A	No
[50]	900V/900A, (650V/900A)	Half Bridge	No	5.5	N/A	12	$130 \times 62 \times 18$	N/A	Yes
[51]	1200V/240A, (600V/120A)	Half Bridge	No	6.6	N/A	6	N/A	N/A	Yes
[52]	1200V/60A, (540V/30A)	Half Bridge	No	11.1	N/A	3	$48.4 \times 42.8 \times 15.9$	N/A	Yes
[53]	1200V/500A, (N/A/N/A)	Half Bridge	No	7.77	N/A	4	N/A	N/A	N/A
[54]	1200V/N/A, (800V/80A)	Half Bridge	No	3.54	N/A	4	N/A	N/A	No
[55]	1200V/181A, (400V/120A)	Half Bridge	No	2.69	N/A	4	N/A	N/A	No
[56]	1200V/520A, (600V/380A)	Half Bridge	No	2.31	N/A	4	N/A	N/A	No
[57]※	N/A/N/A, (750V/130A)	Full Bridge	No	15	N/A	4	N/A	N/A	No
[58]※	3300V/800A, (N/A/N/A)	Half Bridge	No	15	0.02 (j-c)	N/A	$140 \times 100 \times 40$	N/A	No
[59]※	3300V/800A, (N/A/N/A)	Half Bridge	No	12	0.03 (c-c)	N/A	$140 \times 100 \times 40$	N/A	No
[60]※	3300V/770A, (N/A/N/A)	Half Bridge	No	11	0.03 (j-c)	N/A	$144 \times 100 \times 40$	N/A	No
[61]※	3300V/750A, (1800V/750A)	Half Bridge	No	10	N/A	N/A	$140 \times 100 \times 38$	N/A	No
[62]※	3300V/1000A, (N/A/N/A)	Half Bridge	No	10	0.02 (j-c)	N/A	$140 \times 100 \times 40$	N/A	No
[66]※	10000V/240A, (N/A/N/A)	3 Phase Inverter	No	16	0.02 (j-c)	6	$195 \times 125 \times 24$	N/A	No
[72]	1200V/126A, (700V/25A)	Half Bridge	Yes	1.1	N/A	2	N/A	N/A	Yes

PR: Power Rating, IGD: Integrated Gate Driver, PI: Parasitic Inductance in CCL, TR: Thermal Resistance, j-c: Junction to Case, j-f: Junction to Fluid, c-c: Channel to Case, NoPS: Number of Parallel Switches in each commutation cell, PD: Power Density, EDC: Embedded Decoupling Capacitor
※: from Industry

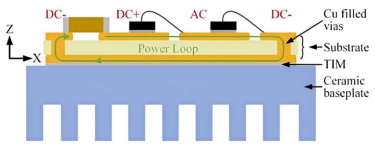


FIGURE 12. Power module with vertical power loop [72].

the power switches. Additionally, medium- and high-voltage power modules confront several challenges, including EMI issues, cross-talk and mistriggering, as well as special gate drive considerations, and E-field mitigation [24], [32], [70], [71].

Vertical power loop is another concept that researchers have utilized to reach simultaneous low parasitic inductance and capacitance in a lightweight power module [72]. The vertical loop increases the mutual inductance cancellation, resulting in a very low total power loop parasitic inductance. The cross-sectional view of this power module is depicted in Fig. 12. In addition, the $DC-$ path acts as a shield between the output port and the ground, leading to low parasitic capacitance between the output port and the ground. Obtaining low parasitic capacitance is crucial owing to its detrimental role on the Common Mode (CM) circulation current, Electromagnetic Interference (EMI) issues, and the switching performance [73], [74]. It is noteworthy that using a DBC with vias makes this power module complex and costly compared to a simple DBC.

Various attributes such as nominal power rating for the used chips and conducted DPT, their structure, gate-driver integration, parasitic inductance, thermal resistance, number of parallel switches in each commutation cell, size, reported power density, and Embedded Decoupling Capacitor (EDC) for the power modules with wire bonding method are outlined in Table 2. One can see that the parasitic inductance values for the wire bonding method range from 1.1 nH to 15 nH. This difference originates from the current loop structure, e.g., the ability to realize proper mutual inductance cancellation, and length. For example, the power modules from industry usually have larger parasitic inductance due to the fact that their structure is more similar to the conventional wire bonding method. On the other hand, those power modules with an innovative configuration for mutual inductance cancellation, like [45], [49], [54], [55], [56], are capable of offering parasitic inductance below 5 nH. Moreover, a very low parasitic inductance is achieved in [72] by establishing mutual inductance cancellation and a short current loop simultaneously.

Although these power modules can offer low parasitic inductance, the wire bonding method suffers from multiple shortcomings. The main drawbacks are high parasitic inductance value, poor thermal performance, and reliability concerns. These issues are explained in Section V in detail.

III. HYBRID PACKAGING

Hybrid packaging for power modules is a technology that blends various interconnection and packaging technologies to achieve improved electrical, thermal, and mechanical performance. It generally takes traditional wire bonding and marries it with sophisticated methods like planar structures, embedded dies, Printable Circuit Boards (PCBs), etc. By integrating various technologies, hybrid packaging tries to optimize cost and performance. Hybrid packaging leverages the benefits of each method, utilizing wire bonds for gate connections while using planar copper clips for source/drain pathways to

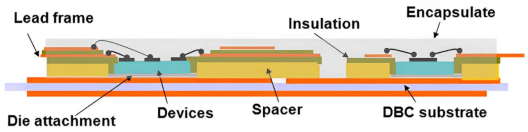


FIGURE 13. Hybrid power module (rectifier) [75].

FIGURE 14. Hybrid power module with planar connection (for power loop) and wire bonding (for gate-loop) [76].

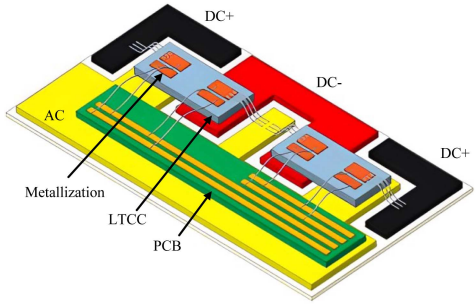


FIGURE 15. Hybrid power module with planar connection and wire bonding [77].

reduce parasitic inductance and enhance current capacity. Hybrid packaging is especially beneficial for SiC-based modules, where thermal and switching speed requirements are high, and hence, there is a need for advanced design approaches.

To provide an extensive assessment, this section studies those power modules whose structure is implemented by employing hybrid packaging techniques. This packaging method combines planar and wire bonding, PCB, and stacked substrates.

A. HYBRID POWER MODULES WITH PLANAR STRUCTURE AND WIRE BONDING INTERCONNECTIONS

Moving toward advanced packaging techniques, the interconnection between the top of the semiconductor dies was first replaced in the early steps by a planar type of interconnection [31]. Shortly, this method became a preferred approach in power electronics packaging due to its advantages, such as reduced parasitic inductance, higher current capacity, and enhanced reliability. Consequently, leading companies like Mitsubishi and Tesla have used this method [33]. The implemented power modules use planar laedframes for the power loop and wire bonding for the control loop. Therefore, the benefits of the mature wire bonding method, along with high current capacity and low parasitic inductance, can be attained simultaneously.

Wire bonding and the planar packaging technique have been used to implement a SiC-based three-phase rectifier in [75]. Accordingly, low parasitic inductance and a more straightforward fabrication process are carried out due to using a planar structure and wire bonding interconnection, respectively. This hybrid power module's cross-section is demonstrated in Fig. 13. Based on this figure, spacers, insulation, and lead frames are used based on the planar packaging method, and wire bonds are used to realize topside interconnections.

To achieve low parasitic inductance, the proposed power module in [76] benefits from a planar-based structure. In other words, a copper lead frame is mounted on top to build the electrical connections between the upper and lower switching cells in a half-bridge structure. Additionally, the wire bonding method is used to deliver gate signals, leading to a simple implementation of the power module. The current commutation path is shown in Fig. 14, revealing a good mutual inductance cancellation. However, the lack of balanced current sharing between the paralleled chips in the upper switching cell and uneven thermal resistance of the upper and lower switching cells, between the chips and the heatsink, deteriorates the reliability of this power module.

Like the efforts in industry, specialists in Fraunhofer have reported a compact power module capable of operating at high junction temperatures up to 400 °C [77]. Hence, this power module benefits from the SiC semiconductors' ability to work at high temperatures. In this power module, bare dies are embedded into a Low-Temperature Co-fired Ceramics (LTCC) substrate. Fig. 15 shows the planar configuration of the PCB, for delivering gate signals, and the LTCC substrates on the baseplate. Then, the bond wire forms the power loop. Due to the low thermal conductivity of LTCC, thermal vias should be used in this power module's structure, rendering complex and costly fabrication.

B. POWER MODULES WITH PCB AND FPCB

Another type of hybrid structure for power modules that utilizes PCBs is investigated in this section. Since PCBs can bring design versatility, space and weight saving, and improved signal integrity for interconnections, they are a suitable choice for attaining power modules with more advanced structures.

Several hybrid SiC-based power modules comprising a DBC substrate and a multilayer PCB are studied in [78], [79], [80]. These power modules also use wire bonding to fulfill the required routes. The use of a single bare die in each switching cell makes their current rating very limited. It should be noted that reaching a high current rate in these power modules necessitates more vias, leading to higher manufacturing costs.

Due to the shielding of the output port from the ground, the parasitic output-to-ground capacitor of the power module in [80] diminishes significantly, leading to lower EMI issues and common-mode current. A cross-sectional view of this power module is shown in Fig. 16.

Given that Flexible PCBs (FPCB) allow for bendability and simplified assembly, they can also be used for realizing the desired connections in power modules. FPCBs can offer the advantages of PCBs along with their flexibility.

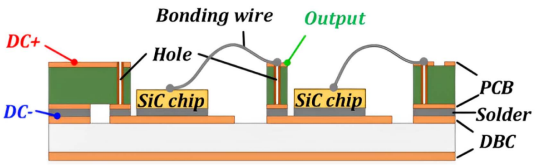


FIGURE 16. PCB+DBC+Wire bonding power module with low parasitic inductance and capacitance [80].

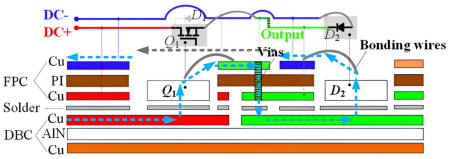


FIGURE 17. Hybrid FPCB+DBC based power modules [82].

Better thermal performance and reduced power losses have been achieved with the help of FPCB in the power module reported in [81]. In addition, the power loop and gate loop parasitic inductances have dropped 52% and 76%, respectively, as compared to the wire bonding method. A two-layer FPCB is attached to the top and bottom SiC dies with its top layer as $DC-$. The $DC+$ and AC potentials are implemented on the DBC. Nevertheless, there is no information about the current sharing and implementation process.

To combat the limited current challenge, the proposed FPCB-based power module in [82] expands the number of parallel bare dies in each switch to six. This power module is capable of offering 0.79 nH parasitic inductance and three-sided cooling. The latter feature shrinks the volume of the heatsink by 50% in comparison to the typical commercial power module from Wolfspeed (CAS120M12BM2). $DC-$, AC, and gate-driving terminals are all connected to the module through FPCB, allowing for excellent interconnection compliance. Fig. 17 indicates the cross-section layout of the power module. The absence of current sharing analysis hinders the evaluation of power module performance for high-power applications. Moreover, the thermal analysis was done under conditions drastically different from those of a power module that operates for high-power applications. The considered power loss for each MOSFET is 4.95 W, and each diode is 0.068 W for a 20 kW/20 kHz three-phase inverter, while the power loss for each bare die is usually considered about 100 W or more [83], [84], [85]. Hence, this significant difference makes the thermal analysis almost inapplicable for high-power applications such as EVs.

C. STACKED SUBSTRATE POWER MODULES

Stacking substrates is another way to tackle EMI problems and mitigate parasitic inductance simultaneously. Mainly by making a serial connection of parasitic capacitors from the output port to the ground. Hence, the stacking technique drastically decreases the output parasitic capacitor, resulting in mitigated EMI issues. Moreover, low parasitic inductance

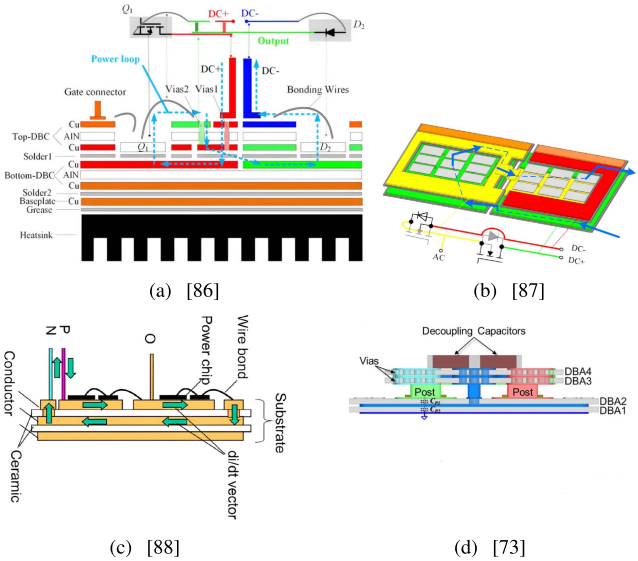


FIGURE 18. Stacked substrate-based power modules.

is obtained through effective mutual inductance cancellation. This section studies various layouts applying these techniques to implement new hybrid power modules.

Two DBCs are stacked to make a current path with high mutual inductance cancellation in [86]. In this design, bare dies are attached to the bottom DBC to lower the thermal resistance. The top DBC and wire bonding are used to form the relevant current paths. 73% reduction in overshoot, 10% higher switching speed, and 57% lower power losses, as compared to a Wolfspeed commercial power module (CAS120M12BM2), are accomplished by this power module. Fig. 18(a) displays the lateral view of the power module. Despite using the lower DBC for bonding the bare die, the thermal resistance is still high in comparison to the other power modules implemented based on the hybrid method. Moreover, the power module suffers from a defective current sharing performance.

Stacked DBCs are used in [87] to implement a power module with low parasitic inductance. This configuration allows the integration of 18 chips for each switching cell in the power module, drastically enhancing the current rating. The authors claimed that the manufacturing process is simple due to the use of separate DBCs. Although the authors noted the high current capacity as a major advantage of the power module, there is no current sharing analysis, which is vital for those power modules with a high number of bare dies in parallel. The lack of proper current sharing and thermal analysis makes assessing its operation under heavy loads challenging. Finally, the need for connectors between DBCs deteriorates the device's reliability. Fig. 18(b) displays a 3D model of the mentioned power module with the current path.

The stacked DBCs and wire bonding method, for topside interconnections, are incorporated to implement a power module with low parasitic inductance and capacitance in [88].

Unlike the power module in [86], the bare dies are placed on the top DBC. This positioning helps mitigate EMI-oriented issues better; however, it adds to the thermal resistance of the power module. The authors have indicated that the impact of the additional layers on the overall thermal resistance is minimal. Nevertheless, it is essential to note that the study was conducted under the assumption of an unrealistically low power dissipation, which does not align with practical scenarios. The introduced power module is indicated in Fig. 18(c). This configuration is enhanced in [89] with an integrated RC snubber. Moreover, using a ceramic substrate with higher thermal conductivity, e.g, Si_3N_4, is proposed to decrease the thermal resistance.

To further mitigate EMI issues and attain low parasitic inductance, a configuration with stacked DBCs and PCB is studied in [90]. The parasitic capacitance is less than $1pF$, which is much lower than $63.9pF$ associated with discrete devices [80]. Additionally, stacked design assists proper mutual inductance cancellation, which results in low parasitic inductance. Despite these pros, the high thermal resistance, due to the allocation of the chips on the top DBC, is a crucial drawback of the power module.

So far, the importance of the low parasitic inductance for low voltage power modules, e.g, < 3.3 kV, was discussed. Obviously, at the higher voltage levels, the effects of the parasitic inductance are more detrimental to the overall performance. Moreover, high dv/dt results in high CM current, EMI issues, and poor switching performance.

To address these challenges, a medium voltage power module with low EMI issues and high-speed switching is introduced in [73]. This power module employs four stacked Direct Bonded Aluminum (DBA) layers. Beyond hosting bare dies, two bottom DBAs are used to lower the electric field's intensity and to reduce the common-mode current circulation. Vias and posts serve dual purposes. First, they make the topside interconnections. Second, they construct the central aluminum layer that connects the lower DBAs to the decoupling capacitors. The parasitic inductance and capacitance are 4.4 nH and 35.7 pF, respectively. Then, spring terminals are used to deliver gate and source signals. Fig. 18(d) demonstrates the lateral view of this power module. This scheme shows the high thermal resistance between the bare dies and the heatsink. Overall, the lack of thermal analysis does not allow for an accurate assessment. A different medium-voltage power module is introduced in [91]. The power module's parasitic inductance is 5.6 nH. However, the terminals have not been considered in this calculation. This power module also uses an optimized layout for the stacked DBCs to lower parasitic capacitance to $28pF$. Although these advantages exist, the *AC* terminal pads are realized through PCBs on the upper DBC. This design approach significantly adds to the complexity and cost of the manufacturing process. About the high thermal resistance of the power modules with stacked DBCs configuration, it should be mentioned that if the chips are mounted on the top DBC, the heat has to go through more thermal resistances. e.g., two layers of ceramic, as compared to those power modules with a single DBC. Moreover, due to the very low resistivity of the copper in DBCs, the main thermal resistance is attributed to the ceramic layer in the substrate. Based on the reported thermal resistances, the power modules in [88] and [91] have relatively lower thermal resistance than [86] despite employing a stacked DBC structure. This is because modules in [88] and [91] use Si_3N_4 as a ceramic in their DBC, while the module in [86] uses Al_2O_3. The thermal conductivity of Si_3N_4 is two to three times higher than that of Al_2O_3 [26]. It is noteworthy that the use of Si_3N_4 results in more cost for the final product. Therefore, a trade-off should be made between the cost and thermal resistance for implementing a power module.

Table 3 outlines the important parameters of the investigated hybrid power modules. The parasitic inductance reduction of the power modules based on the hybrid method is strongly linked to the adoption of planar conductors, stacked substrates, or PCB/FPCB-based interconnects. Benefiting from these techniques, the parasitic inductance values are usually kept below 5 nH. Considering the power modules using planar layout, except for the module in [75], they offer parasitic inductance around 2–4 nH because of attaining proper mutual inductance cancellation [76] and short current paths [77]. Then, in order to suppress both the parasitic inductance and capacitance, power modules with the help of PCBs are implemented in [78], [79], [80]. These power modules mostly introduce parasitic inductance values lower than 4 nH. With the help of a shielding structure, these modules offer low parasitic capacitance. Like the use of PCBs, the power modules with the stacked DBCs configuration also offer low parasitic capacitance. However, except for the power module in [86] with a very low parasitic inductance, their parasitic inductance values are higher than 4.4 nH. Finally, the ultra-low value in [82] is obtained by employing FPCB with six parallel dies, which both shortens the commutation loop and provides strong coupling between current paths.

IV. 3D POWER MODULES

Three-dimensional packaging for power modules is a sophisticated technique that mounts components vertically and stacks them to deliver a compact, high-performance module [92], [93], [94], [95]. In contrast to conventional two-dimensional designs, 3D packaging utilizes the third dimension to minimize current paths and effectively increase the mutual inductance cancellation. Overall, it allows for improved switching performance, which is beneficial for power modules based on SiC.

A convenient way to realize a 3D-based power module is the flip-chip method. Flip-chip bonding is used in [96] to remove wire bonds, thus attaining a low parasitic inductance equal to one-third of the conventional wire bonding-based module. The metallic connectors and the substrate make a short 3D current path with a proper mutual inductance cancellation. The lateral view of the power module, while the CCL is shown, is expressed in Fig. 19. The flip-chip method

TABLE 3. Hybrid Power Modules With SiC Semiconductor Comparison

Ref	PR-Chip, (DPT)	Structure	IGD	PI (nH)	TR $(^\circ K/W)$	NoPS	Size (mm^3)	PD (kW/L)	EDC
[73]	10000V/30A, (5000V/20A)	Half Bridge	No	4.4	N/A	3	$70 \times 80 \times 20$	N/A	Yes
[75]	N/A	6 in 1 (Rectifier)	No	16	N/A	1	$35 \times 18 \times 0.7$	N/A	No
[76]	N/A/N/A, (800V/400A)	Half Bridge	No	3.71	N/A	4	N/A	N/A	No
[77]	N/A	Half Bridge	No	2.4	0.59 (j-f)	2	N/A	N/A	No
[78]	1200V/10A, (600V/7.4A)	Half Bridge	No	3.8	N/A	1	N/A	N/A	Yes
[79]	1200V/24A, (400V/20A)	Half Bridge	No	3.38	0.38 (j-h)	1	$24 \times 15 \times 8$	23.15	Yes
[80]	1200V/24A, (400V/20A)	Half Bridge	No	5.5	N/A	1	N/A	N/A	Yes
[81]	620V/20A, (600V/20A)	Half Bridge	No	4.87	N/A	3	$73.5 \times 21 \times 1.3$	N/A	No
[82]	1200V/120A, (400V/120A)	Half Bridge	No	0.79	N/A	6	$53 \times 45.5 \times 62$	19.3	Yes
[86]	1200V/120A, (400V/120A)	Half Bridge	No	1.8	0.65 (j-c)	6	$93.5 \times 47.5 \times 12.1$	32	Yes
[87]	1200V/1500A, (800V/500A)	Half Bridge	No	4.74	N/A	18	N/A	N/A	No
[88]	1200V/120A, (600V/60A)	Half Bridge	No	4.5	0.14 (j-f)	2	N/A	70	No
[89]	1200V/100A, (600V/100A)	Half Bridge	No	4	N/A	1	N/A	N/A	No
[90]	1200V/36A, (400V/20A)	Half Bridge	No	4.5	N/A	1	N/A	N/A	No
[91]	10000V/N/A, (5000V/N/A)	Half Bridge	No	5.6 WT	0.14 (j-c)	3	$97 \times 99 \times 44$	N/A	Yes

j-h: Junction to Heat sink, WT: Without Terminals

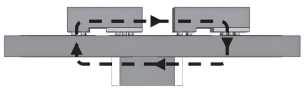


FIGURE 19. Lateral view of the power module with flip-chip bonding [96].

is also used in [97], [98] to introduce an ultra-low parasitic inductance power module. Bare dies are connected to the bottom and top DBCs by means of soldering and solder balls, respectively. To lower thermal resistance, the micro channel coolers are integrated into the baseplate of the power module. Although the benefits are clear, incorporating a laser-engraved cooler into the bottom substrate and vias into the top DBC increases the power module's complexity and cost. The authors have used five chips in parallel to improve the current capacity. Nevertheless, the current sharing analysis is not available.

PCB embedded is an effective method to implement power modules with compact structure, reduced volume and weight [99], [100], [101]. Moreover, the PCB embedded modules offer low parasitic inductance and resistance by implementing 3D current paths for both the power and gate-driving loops. This approach is used in [102] to implement a compact power module with only 1 mm thickness. This module is able to offer about 90% lower parasitic inductance in both the gate-driver and power loops compared to a half-bridge module built by TO-247 discrete switches. Nevertheless, this compact configuration raises concerns about the power module's mechanical strength in harsh environments like EVs. To even further reduce the thickness of the PCB embedded power modules, an ultra-compact module, e.g, $< 1mm$, is introduced in [103]. The thickness of this structure is only $0.47mm$. The current flow path in the power module is shown in Fig. 20(a). Despite offering a low thermal resistance, the lack of adequate mechanical strength is a concerning drawback of this power module.

To elevate the current capacity to 200 A, while preserving the ultra-compact size, the PCB-embedded power module in [104] uses two chips in parallel. This power module also

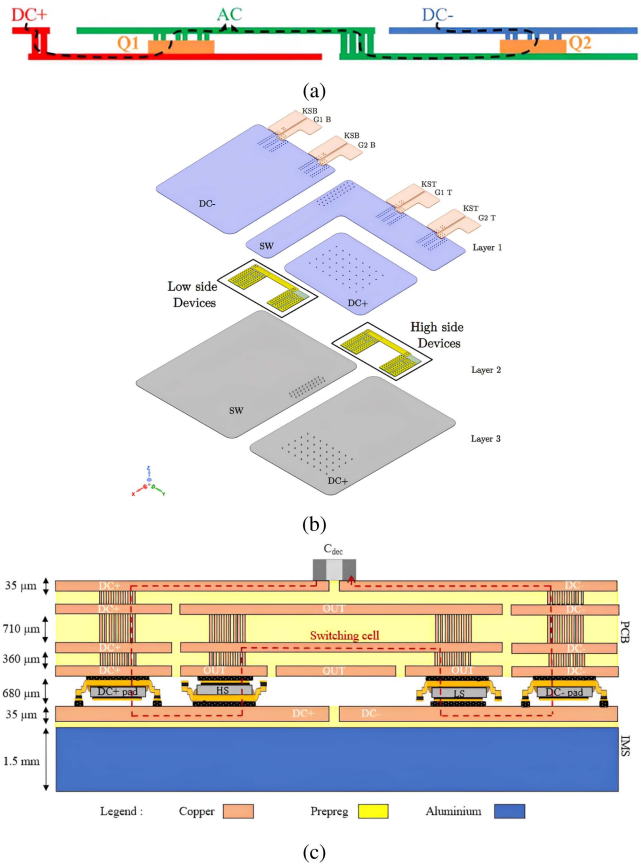


FIGURE 20. PCB embedded power modules (a) Current path of the ultra-compact power module [103], (b) Exploded sketch of the power module with high current capacity [104], (c) Cross-section view of the flip-chip+PCB power module [105].

uses *AC* and *DC+* copper pads as an interface to directly dissipate heat from the bare dies to the heatsink. The exploded view of this power module is demonstrated in Fig. 20(b). As can be seen, the internal structure allows for proper mutual inductance cancellation, leading to a very low parasitic inductance. However, the reference does not provide any analysis

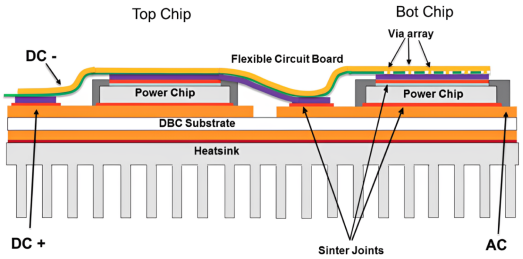


FIGURE 21. Cross section view of the power module with FPCB from Semikron [106].

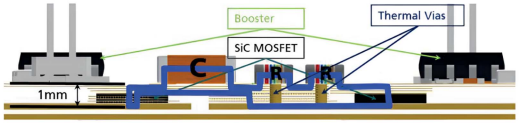


FIGURE 22. LTCC cavity-based power module developed by Fraunhofer and Hitachi, cross-section view and the power loop (blue line) [108].

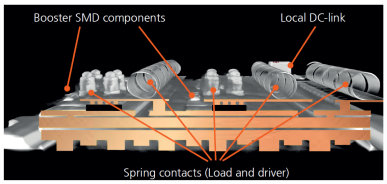


FIGURE 23. Power module developed by Fraunhofer [109].

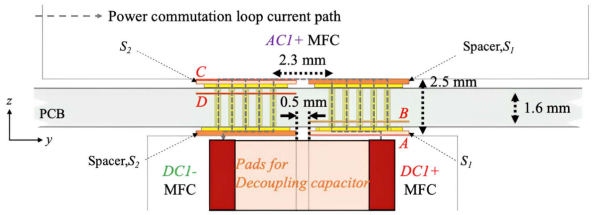


FIGURE 24. Power module with Quasi-DSC and multi-functional busbars [110].

of the current sharing performance or thermal analysis. Therefore, its performance for high-power applications can not be assessed accurately.

By using a flip-chip connection and embedding SiC chips into a PCB, a 3D power module is reported in [105]. This power module benefits from an ultra-low, parasitic inductance. In this power module, chips are sandwiched between a 4-layer PCB and an Insulated Metal Substrate (IMS), as indicated in Fig. 20(c). The obtained results clarify that the flip-chip technique reduces the parasitic inductance by about 40% compared to the conventional power modules without the flip-chip connection, thanks to shorter CCL. However, the module's power rating makes it an unsuitable choice for high-power applications.

Like the efforts in academia to attain high current capacity, Semikron has introduced a power module with FPCB in [106]. This power module is based on SKiN technology [107] and employs eight power switches in parallel to extend the current rating to 400 A. Less power loss, as compared to Si-based power modules, compact structure, and very low parasitic inductance are other advantages offered by the power module. Despite conducting high-current tests on the module, the current sharing analysis is unavailable. The cross-section schematic of this power module is drawn in Fig. 21.

Fraunhofer and Hitachi have developed a power module for EV applications [108]. SiC chips are embedded in this power module into an LTCC substrate. Moreover, a 3D-printed water cooler made of aluminum sinks the generated heat, as clarified in Fig. 22. The 3D current path brings proper mutual inductance cancellation, creating low parasitic inductance. In addition to the CCL, the gate loop parasitic inductances are more suppressed since the DC link capacitors and gate drivers are located close to the chips. However, using LTCC elevates the cost and complexity of the manufacturing.

In another attempt, Fraunhofer developed a power module to achieve very low parasitic inductance and low thermal resistance [109]. This power module uses a multilayer Si_3N_4 ceramic substrate. With the help of vias and spring contacts, the two top layers form electrical connections. Furthermore, the bottom layer contains an integrated heat sink. The cross-sectional view of this power module is shown in Fig. 23. Despite offering the merits mentioned above, the integrated heat sink and the need for drilling vias in the ceramic substrates result in a costly and complex manufacturing process.

To implement a very low inductance and compact power module, a vertical CCL concept with Multi Functional Components (MFCs) is proposed in [110]. Since MFCs are used to a) realize $DC+$, $DC-$, and AC connections, b) act as heat sinks, and c) host decoupling capacitors, they are called multi-functional MFCs. In this power module, high-side and low-side switches are connected to the sides of a PCB. The power module's cross-section view is demonstrated in Fig. 24. There is no thermal analysis in the paper. However, as can be seen, the heat is dissipated from the chips via both the MFCs and PCB vias. Hence, the authors consider it as Quasi-Double Side Cooling (QDSC). In other words, the heat can not be extracted like the DSC method, but the cooling is better than SSC. This figure also demonstrates that the heat sinks are included in the power loop and are not isolated. Furthermore, the high current capacity for PCB means higher costs. This issue hinders the use of the power module in high-power applications.

An orthogonal DBC substrate and prismatic structure are used to establish 3D current paths in [111]. This configuration drastically cancels mutual inductance, alleviating total parasitic inductance. This study's result reveals that the 3D power path's parasitic inductance is 31.3% lower than its 2D peers. However, it should be noted that the manufacturing process includes bending elements and making an orthogonal substrate. Besides the 3D power path, the study in [112] considers symmetrical 3D allocation of the chips to attain a balanced current sharing profile. Analysis shows a symmetric current

TABLE 4. 3D Power Modules With SiC Semiconductor Comparison

Ref	PR-Chip, (DPT)	Structure	IGD	PI (nH)	TR ($°K/W$)	NoPS	Size (mm^3)	PD (kW/L)	EDC
[96]	1200V/40A, (300V/35A)	Half Bridge	No	4.88	N/A	1	N/A	N/A	Yes
[97]	1200V/300A, (800V/60A)	Half Bridge	No	0.93	N/A	5	N/A	N/A	No
[102]	1200V/N/A, (950V/116A)	Half Bridge	No	2.3	0.2 (j-c)	1	$20.3 \times 31.1 \times 1$	N/A	No
[103]	1200V/103A, (800V/25A)	Half Bridge	No	2.4	0.074 (j-c)	1	$37.1 \times 18.5 \times 0.47$	N/A	No
[104]	1200V/200A, (600V/45A)	Half Bridge	No	1.5	N/A	2	$48 \times 32 \times 0.35$	N/A	No
[105]	150V/78A, (48V/40A)	Half Bridge	No	0.8	N/A	2	N/A	N/A	Yes
[106]※	1200V/400A, (600V/400A)	Half Bridge	No	1.4	N/A	8	N/A	N/A	No
[108] ※	N/A/N/A, (750V/160A)	Half Bridge	Yes	8.4	0.21 (j-Co)	2	N/A	N/A	No
[109] ※	1200V/160A, (N/A/N/A)	Half Bridge	No	1.7	0.26 (j-f)	N/A	$48 \times 48 \times 5$	N/A	Yes
[110]	1200V/98A, (600V/30A)	Half Bridge	Yes	1.35	0.45* (j-a)	1	N/A	N/A	Yes
[111]	1200V/50A, (1050V/50A)	Half Bridge	No	12.4	0.3 (j-c)	1	$15 \times 15 \times 15$	N/A	No
[112]	N/A/N/A, (150V/30A)	Half Bridge	No	4	N/A	3	N/A	N/A	No

j-Co: Junction to Coolant, *: calculated by authors

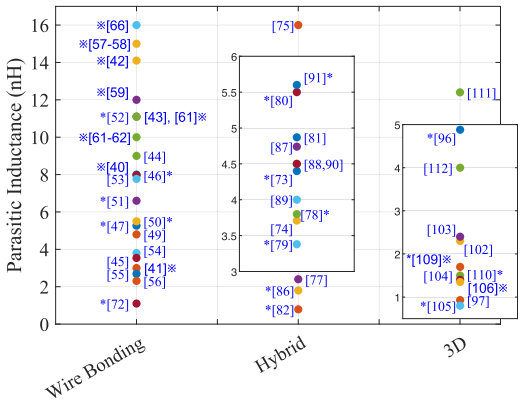


FIGURE 25. Wire bonding, 3D, and hybrid packages parasitic inductance, *: using EDC.

distribution due to the chips' location in a circle-shaped DBC. Despite these merits, the power module's overall reliability is diminished due to the use of wire bonding for connections. A limited power rating is another obstacle to using it for high-power applications.

The important parameters of the investigated 3D power modules and their main characteristics are outlined in Table 4. The parasitic inductance values in this table confirm the effectiveness of 3D current routing. Although there are a few modules whose parasitic inductance is larger than 4 nH [96], [108], [111], most of them are below 3 nH. For instance, using the chip embedding method, both in PCB and ceramic substrate, and the QDSC method enable the power modules in [104], [106], [109], [110] to offer very low parasitic inductance values. Then, the use of the flip-chip technique paves the way for acquiring ultra-low parasitic inductance values [97], [105]. The associated shortcomings of the 3D packaging method are summarized in Section V.

V. CHALLENGES AND FUTURE TREND

A. CHALLENGES

Packaging SiC-based power modules with minimal parasitic inductance and thermal resistance is crucial yet difficult to harness their capabilities in high-frequency, high-temperature, and high-power applications. In previous sections, various packaging methods for achieving these merits were surveyed. However, every method comes with its pros and cons.

To begin with, low-inductance power modules with wire bonding interconnections were reviewed. As mentioned, the use of wire bonding has several drawbacks. Firstly, as mentioned in the Introduction section, large voltage overshoots and severe switching oscillations increase the power losses, intensifying EMI and cross-talk issues.

Secondly, from a thermal standpoint, wire bonding restricts heat dissipation from the junction of the power module to only one side, e.g, SSC. Therefore, DSC cannot be achieved with the wire bonding interconnection. Additionally, the smaller footprint of the WBG devices limits the number of usable wire bonds.

Thirdly, from a reliability perspective, wire bond lift-off or cracks due to thermal cycling have been the most critical failure mode [113]. This issue results in numerous failures and adversely influences the module's overall performance and lifetime [114].

Regardless of the reduction of parasitic inductance, other issues related to the wire bonding method persist, and the studied power modules cannot address them properly. Therefore, enhanced packaging methods are needed to eliminate the problems and challenges related to wire bonding based packaging.

As stated in Section III, the hybrid packaging method offers several advantages. However, it also presents certain disadvantages that require attention. To begin with, the use of planar structures and wire bonding inherits all the limitations associated with wire bonding in these power modules. Additionally, incorporating PCBs into hybrid power modules poses some challenges that affect the performance of hybrid power modules. The primary concern is the CTE (Coefficient of Thermal Expansion) mismatch between the PCB and DBC, which causes significant reliability challenges [115]. Moreover, the inadequate thermal properties of PCBs hinder efficient heat dissipation [116].

The stacked DBCs method, due to its multilayer structure, increases thermal resistance and raises reliability concerns. Additionally, the fabrication of stacked DBC modules is more complex than that of single-layer DBC. The demand for precise alignment and bonding of stacked layers makes manufacturing costly and less efficient.

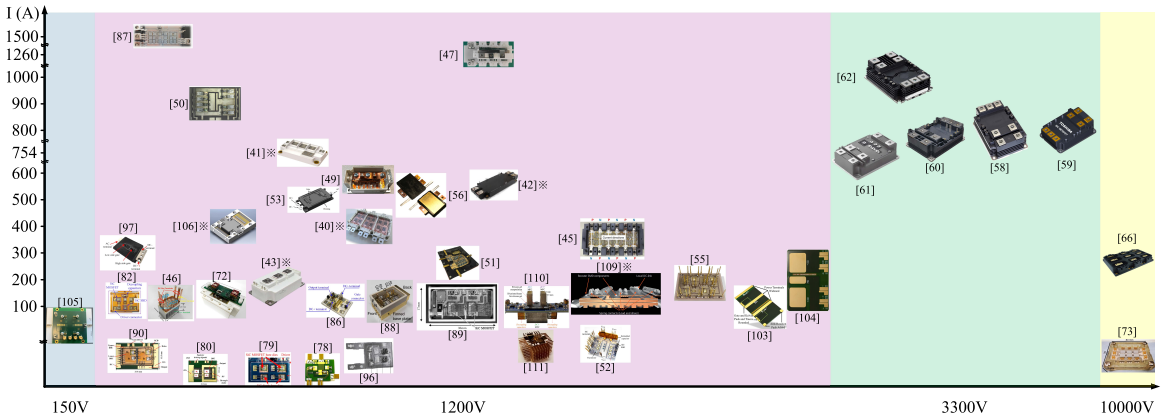


FIGURE 26. Surveyed power modules' voltage and current rating.

Section IV concludes that the 3D configurations are practical solutions to attain low parasitic inductance compared to their 2D counterparts. This method approaches this merit via shortening the CCL or increasing the mutual inductance cancellation in three dimensions. Yet, these advantages come at a cost. Deploying 3D power modules is pricier and requires more time than traditional 2D power modules. Moreover, the high accuracy alignment and connection of more elements bring more complexity. Besides, using the third dimension usually means utilizing more elements, raising reliability concerns.

The parasitic inductance values offered by every packaging method are shown in Fig. 25. Those power modules with EDC in their structures are depicted with "*". It is worth mentioning that due to the high number of references for power modules with the hybrid and 3D packaging methods, their values are magnified for a part of the diagram.

Juxtaposing all these values clarifies that power modules built by 3D and hybrid methods can offer very low, $< 2nH$, and ultra-low, $< 1nH$, parasitic inductance compared to the wire bonding method. Moreover, it should be mentioned that the academic designs usually achieve lower parasitic inductance due to several factors, including a) highly customized layouts, b) advanced prototyping techniques (e.g., optimized trace routing, integrated decoupling capacitors, or novel substrate materials), and c) a focus on performance optimization in controlled, small-scale environments without the constraints of mass production. In contrast, industrial counterparts prioritize factors such as manufacturability, robustness against environmental stresses, compliance with industry standards (e.g., automotive or aerospace qualifications), cost-effectiveness, and ease of integration into systems, which can necessitate compromises like standardized packaging, larger form factors, or additional protective elements that inadvertently increase parasitic inductance [32]. Hence, these differences allow the power modules from academia to have lower parasitic inductance in comparison to their industrial peers.

As mentioned before, hybrid and 3D packaging come with higher cost and complexity than wire bonding. A trade-off must be evaluated. For applications prioritizing low cost and simplicity, wire bonding is preferable; otherwise, hybrid and 3D packaging methods are superior. Notably, for high current applications, the hybrid packaging method is advantageous.

For those power modules with available nominal voltage and current rating, their distribution is shown in Fig. 26. [41], [47], [49], [50], [87] showcase power modules that are particularly notable for their current ratings. Nevertheless, as discussed before, no current sharing analysis is available except for [47] and [49]. The lack of proper current sharing performance in this power module is an essential shortcoming. Thus, their long-term reliability is highly questionable.

PD is also an important factor in comparing power modules, especially for high-power applications with weight and volume concerns. Unfortunately, except for a few studies, there is not enough information about this characteristic in the inspected power modules. However, in order to make the comparison section more complete and broader, it has been considered in the comparison tables.

An essential factor in comparing power modules, in addition to previously discussed features, is their final cost. Regrettably, aside from certain industrially developed modules, this information is missing from the references reviewed. Consequently, this vital element has been disregarded in this paper. Nonetheless, the relative cost of different methods is compared, although precise data on this aspect is unavailable. Additionally, the advantages and disadvantages linked to every packaging method and sub-method are outlined in Table 5 with details for a better review.

At the end of this subsection, the introduced power modules are categorized based on the most important advantages and disadvantages in Table 6, including the packaging methods and sub methods. This classification helps to realize the specific packaging methods and references associated with each important merit or demerit. For example, no power module based on the wire bonding method can offer ultra-low parasitic inductance. Moreover, integrating PCB into the power module usually results in a low current rating.

TABLE 5. Packaging Techniques and Their Features Based on Wire Bonding, Hybrid and 3D Methods

Ref	Detailed Packaging Technique/ Manufacturer	Features
Wire Bonding Based Packaging Techniques		
[40]※	HybridPACKTM Drive-Infineon	Proper for high current applications, Low parasitic inductance, Balanced current sharing performance, Larger size compared to the trend in academia
[41]※	Microchip-SP6LI	Proper for high current applications, Low parasitic inductance, Benefiting from 62mm standard, Larger size compared to the trend in academia
[42]※	ROHM-G Series	Proper for high current applications, Relatively low parasitic inductance, Benefiting from 62mm standard, Larger size compared to the trend in academia
[43]※	Wolfspeed	Relatively low parasitic inductance, Benefiting from 62mm standard, Larger size compared to the trend in academia
[44]	Interleaved Current Loops	Low parasitic inductance, Unbalanced current sharing performance
[45]	Interleaved Current Loops (with anti-parallel current paths)	Low parasitic inductance, The reduction rate of the parasitic inductance depends on the number of paralleled phase legs, Low current rating (considering the high number of paralleled chips)
[46]	Double End Source Substrate	Low parasitic inductance, Balanced current sharing performance
[47]	Optimized Wire Bonding, Power Terminals and Parallel Current Loops	Low parasitic inductance, Balanced current sharing performance, Proper for high current applications, Complicated fabrication process
[49]	Interleaved Busbars and Parallel Current Path	Low parasitic inductance, Unbalanced current sharing performance
[50]	Interleaved Busbars and Parallel Current Path	Low parasitic inductance, Proper for high current applications, Benefiting from 62mm standard
[51]	P-cell/N-cell with Trench MOSFETs	Low parasitic inductance, Lower power loss due to the use of Trench MOSFETs, Unbalanced current sharing performance
[52]	Laminated Bus bars and Parallel Current Loops	Relatively low parasitic inductance, Proper for high temperature applications, Limited current despite using three chips in parallel
[53]	Optimized Substrate Pattern	Low parasitic inductance, Proper for high-temperature applications, Complicated manufacturing because of the need for an insulation gasket, Unbalanced current sharing performance
[54], [55]	Symmetric Layout with Staggered Terminals and Reverse Current Coupling	Low parasitic inductance, Proper for high current applications, Balanced current sharing performance
[56]	2.5D wire bonding packaging	Low parasitic inductance, Proper for high current applications, Balanced current sharing performance, Increased production complexity, and cost owing to the need for polyimide (PI) insulator between terminals
[57]※	DENSO	Balanced Current sharing performance, Relatively high parasitic inductance
[58]–[62]※	Mitsubishi, Toshiba, Wolfspeed, Fuji, and Infineon	Relatively low parasitic inductance, Proper for high current applications, Lower $R_{DS(on)}$ (Fuji), Larger size compared to the trend in academia
[66]※	Wolfspeed (XHV-6)	Moderate parasitic inductance, Proper for high voltage applications, Unbalanced current sharing performance
[72]	Vertical Loop Structure (VLS)	Very low parasitic inductance ($<= 2nH$), Low parasitic capacitance, Complex and costly implementation process due to the need for holes in the DBC substrate
Hybrid Packaging Techniques		
[73]	Stacked DBA + Planar	Low parasitic inductance, Low parasitic capacitance, Suitable for medium-voltage applications, High thermal resistance because of the high number of layers in the substrate
[75]	Planar + Wirebond	Low parasitic inductance, Faster manufacturing process as compared to planar packaging, Using wire bonding in the structure
[76]	Planar + Wirebond	Low parasitic inductance, Proper for high current applications, Unbalanced current sharing among paralleled chips, Uneven thermal resistance of the upper and lower switching cells
[77]	Planar (LTCC Substrate)+ Wirebond	Low parasitic inductance, Proper for high temperature applications, Using wire bonds, Complex and costly fabrication process
[78]–[80]	DBC+PCB	Low parasitic inductance, Low parasitic capacitance, Simple connections due to using PCB, Using wire bonding in the structure, Limited current
[81]	DBC + FPCB	Low parasitic inductance, Flexible design, Low mechanical strength
[82]	DBC + FPCB	Ultra-low parasitic inductance ($<= 1nH$), Capability of 3D heat dissipation, Low mechanical strength
[86]	Stacked DBCs	Very low parasitic inductance, Low parasitic capacitance, Unbalanced current sharing performance, Using wire bonding in the structure
[87]	Multiple Stacked DBCs	Low parasitic inductance, Proper for high power applications, No current sharing analysis, Using wire bonding in the structure
[88]	Stacked DBCs	Low parasitic inductance, Low parasitic capacitance, High thermal resistance because of the high number of layers in the substrate, Using wire bonding in the structure
[89]	Stacked DBCs	Low parasitic inductance, Embedded RC snubber, Low parasitic capacitance, High thermal resistance because of the high number of layers in the substrate, Using wire bonding in the structure
[90]	Multi-stacked DBC + PCB	Low parasitic inductance, Ultra low parasitic capacitance ($<= 1pF$), High thermal resistance because of the high number of layers in the substrate, Using wire bonding in the structure
[91]	Stacked DBC+Optimized Copper Pattern	Low parasitic inductance (without considering the terminals), Low parasitic capacitance, Suitable for medium-voltage applications, Costly and complex manufacturing process, Using wire bonding in the structure

Ref	Detailed Packaging Technique/ Manufacturer	Features
3D Packaging Techniques		
[96]	Flip-Chip	Low parasitic inductance, Proper heat dissipation
[97]	Flip-Chip with Micro Cooler	Ultra-low parasitic inductance, Good heat dissipation, Complicated manufacturing process due to using integrated micro cooler channels
[102]	Compact Embedded PCB	Low parasitic inductance, Compact structure, Low mechanical strength
[103]	Ultra-Compact PCB Embedded (with Low Thermal Resistance)	Low parasitic inductance, Low thermal resistance, Ultra-compact structure, Low mechanical strength
[104]	Ultra-Compact PCB Embedded (with High Power)	Very low parasitic inductance, High current rating (as compared to other PCB embedded power modules), Low mechanical strength
[105]	Flip-Chip+PCB	Ultra-low parasitic inductance, Low parasitic capacitance, Limited power rating
[106] ※	DBC+ FPCB / Semikron	Very low parasitic inductance, Proper for high current applications, No current sharing analysis, Flexible design, Low mechanical strength
[108] ※	LTCC Substrate / Fraunhofer and Hitachi	Low parasitic inductance, Embedded RC snubber, High cost and complexity due to the use of LTCC
[109] ※	Multilayer Ceramic Substrate /Fraunhofer	Very low parasitic inductance, Complex and costly manufacturing process
[110]	Quasi-DSC	Very low parasitic inductance (both in the power loop and gate driving loop), Good heat dissipation, Heatsink is included in the power loop, Not suitable for high-power applications
[111]	3D Prismatic	Relatively low parasitic inductance, Good heat dissipation, Complicated manufacturing process due to the need for bending elements and making an orthogonal substrate
[112]	3D Symmetric	Low parasitic inductance, Using wire bonding in the structure, Limited current

TABLE 6. Power Modules Classification Based on the Most Important Advantages and Disadvantages

Packaging Method (Sub method/Manufacturer)	Advantages	Refs
Hybrid (DBC+ FPCB), **3D** (Flip-Chip with Micro Cooler Flip-Chip+PCB)	Ultra-low parasitic Inductance	[82], [97], [105]
Wire Bonding (HybridPACKTM Drive-Infineon, Mitsubishi, Toshiba, Wolfspeed, Fuji, Microchip-SP6LI, ROHM-G Series, Interleaved Busbars and Parallel Current Path, Symmetric Layout with Staggered Terminals and Reverse Current Coupling, 2.5D wire bonding packaging), **Hybrid** (Planar + Wirebond), **3D** (DBC+ FPCB/Semikron)	Proper for High Current Applications	[40], [41], [42], [50], [54], [55], [58], [59], [60], [61], [62], [76], [106]
Wire Bonding (HybridPACKTM Drive-Infineon, Double End Source Substrate, Optimized Wire Bonding, Power Terminals and Parallel Current Loops, DENSO)	Balanced Current Sharing Performance	[40], [46], [47], [54], [55], [56], [57]
Wire Bonding (Vertical Loop Structure (VLS)), **Hybrid** (Stacked DBA + Planar, DBC+PCB, Stacked DBCs, Multi-stacked DBC + PCB), **3D** (Flip-Chip+PCB)	Low Parasitic Capacitance	[72], [73], [78], [79], [80], [86], [89], [90], [105]
Packaging Method (Sub method/Manufacturer)	**Disadvantages**	**Refs**
Wire Bonding (Laminated Bus bars and Parallel Current Loops), **Hybrid** (DBC+PCB), **3D** (Flip-Chip+PCB, Quasi-DSC, 3D Symmetric)	Limited Current/Power Rating	[52], [78], [79], [80], [105], [110], [112]
Wire Bonding (Interleaved Current Loops, Interleaved Busbars and Parallel Current Path, P-cell/N-cell with Trench MOSFETs, Optimized Substrate Pattern), **Hybrid** (Planar + Wirebond, Stacked DBCs)	Unbalanced Current Sharing Performance	[44], [49], [51], [53], [76], [86]

B. FUTURE TREND

The superior performance of WBG semiconductors imposes stricter demands on parasitic inductance, heat dissipation, and thermomechanical stress. Academia and industry contributed to improvements in the power module packaging from the parasitic and thermal viewpoints compared to the conventional packages. The surveyed studies focus more on the power modules' parasitic values and thermal performance. Nevertheless, the reliability, reusability for the end user, the cost, and the complexity of the manufacturing process are usually overlooked. The industry has not widely implemented these new packaging schemes for these reasons. The mainstream packaging method in industry uses wire bonding. Hence, further developments are needed to address these shortcomings in the future.

Wire Bonding Replacement: Initially, the wire bonding connections can be replaced with copper clips since this improvement can suppress the parasitic inductance and increase the current capacity. Industrial manufacturers such as ROHM have also used this method [117].

New and Cheap Hybrid Packaging Method: The Hybrid packaging method is promising to replace the wire bonding method. Future work should focus on implementing lower-cost hybrid power modules, simpler structures, and better cooling characteristics. These works are highly recommended for analysing the whole power module, including the terminals and gate drivers. Since symmetric configuration and dynamic current sharing are the main bottlenecks in the hybrid power modules, they should be studied further.

Simple and Effective Heat Dissipation: Mounting the device on a heatsink is the prevailing cooling method for the power modules. The integrated micro coolers are definitely more efficient in decreasing thermal resistance. However, its use is limited owing to the high cost. The concept of employing the third dimension to construct the current path can be used for cooling, too. Consequently, power modules with multi-dimensional cooling can be implemented for better heat dissipation [82], [111].

Multilevel Power Modules: Earlier, all the investigated power modules had a two-level half-bridge or rectifier structure. Though this configuration has multiple merits, such as low cost, simple structure, and simple control, it suffers from high power loss, low output waveform quality, and high voltage stress across the semiconductors. Multilevel inverters can overcome these problems [118], [119]. Accordingly, several studies have been published on implementing power modules for multilevel configurations [83], [120], [121], [122], [123], [124], [125], [126], [127], [128], [129]. However, almost all the reported converters have been implemented using wire bonding for interconnections. Therefore, there is considerable potential to use a hybrid or 3D packaging method to implement multilevel power modules.

Design Optimization: As the reviewed power modules' packaging methods and techniques showed, there is a paradigm shift toward more compact and complex structures. This trend, however, makes the design phase very challenging for designers in both industry and academia. To overcome this growing problem, using optimization methods and design automation flow are interesting solutions for future work [130], [131], [132], [133], [134]. These methods, with the crucial criteria, can be combined to get the most out of the new packaging methods.

Balanced Current Sharing: As mentioned before, using parallel chips is a convenient way to increase the current-carrying capacity and therefore the power density. However, there are numerous papers omitting the critical current sharing analysis. This is due to the fact that the basic objective of the surveyed studies is to enhance the fundamental design and features of the SSC SiC modules under nominal operating conditions. On one hand, the number of paralleled chips is increased in modern power modules to elevate their power density. On the other hand, the absence of an adequate current sharing profile in paralleled bare dies negatively impacts the long-term reliability of power modules [135], [136], [137]. Due to the significant effect of the circuit parameters on the current sharing profile, future power modules should be able

to offer current sharing profiles without mismatch, guaranteeing better reliability [135].

Insulation Considerations and Extreme Thermal Management: Owing to the growing need to push (U)WBG power modules to elevated power density and operating temperature, the thermal management and insulation stability should be fundamental in future research. Although the DSC technique can offer a superior heat dissipation performance, as compared to the SSC technique, the operating temperature of the (U)WBG devices is still lower than the anticipated range, e.g., 500 °C. To this end, power modules with junction temperatures beyond 250 °C and 400 °C have been introduced so far [138], [139] with the help of proper material. In high-power-density modules, reduced spacing among functional layers elevates the possibility of partial discharge and dielectric breakdown. Conventional encapsulation resins often fail under simultaneous thermal and electrical stress, requiring more advanced materials [24]. Dielectric liquids present a promising alternative, as they are being studied for their ability to enhance both insulation integrity and thermal conductivity [140]. Nevertheless, employing these materials comes with challenges regarding manufacturability, reliability, and cost, which continue to hinder their industrial implementation. Obviously, even though the SSC method is cheaper and simpler to implement, the DSC method is the best way to push (U)WBG power modules to their limits.

VI. CONCLUSION

This paper provides an in-depth analysis of various SiC-based power modules with low parasitic inductance and SSC. These surveyed power modules have been studied in multiple categories based on their packaging methods, such as wire bonding interconnection, hybrid, and 3D. The main advantages and disadvantages of every technique and method are discussed comprehensively. Furthermore, their essential parameters are summarized in each section. Finally, the future trend for the SiC-based power modules is described after explaining the challenges related to every packaging concept.

The collected information, diagrams of cross sections, and CCLs help industry experts and researchers propose new designs and implement new SiC-based power modules. These power modules can offer better performance in many aspects, including parasitic inductance, thermal resistance, reliability, manufacturing process, etc.

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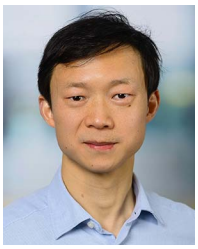

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